

PR420
TMS320VC550x Design 3

FEATURES:

- Provides sequenced core and I/O voltages from input voltages from 1.8 V to 3.0 V.
- /RESET delay fixed at 65 ms minimum, 130 ms typical.
- Linear regulator for quiet core voltage.
- Suitable for dual cell operation
- The current draw on the input power supply is minimized by sequencing the core rail first and then the I/O rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at <http://power.ti.com> then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
 - o <http://focus.ti.com/lit/ds/symlink/tps73601.pdf>
 - o <http://focus.ti.com/lit/ds/symlink/tps61020.pdf>
 - o <http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf>
- Link to application note SLVA118 <http://focus.ti.com/lit/an/slva118/slva118.pdf> to explore the thermal considerations in using linear regulators.

THEORY OF OPERATION:

PR420 consists of a TPS61020 boost converter for the I/O voltage and a TPS73601 linear regulator for the core voltage. The TPS61020 boosts the input voltage to a regulated 3.3 V for the I/O voltage. The TPS73601 linear regulator regulates the input voltage down to the core voltage.

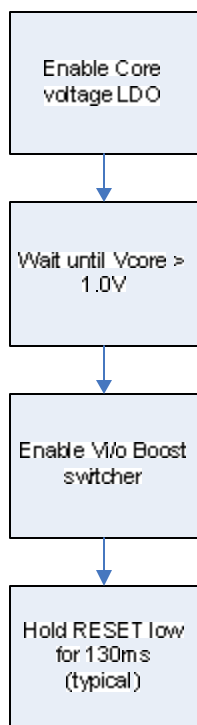
CIRCUIT LIMITATIONS AND CAPABILITIES:

The TPS61020 is capable of supplying about 350 mA of I/O current with an input voltage of 1.8 V. See Figure 1 of the TPS61020 datasheet for the current capability at other input voltages. Higher input voltages allow for higher output current from the TPS61020.

The TPS73601 is capable of supplying 400 mA of core current. The power dissipation of the TPS73601 will be directly proportional to the input voltage and the amount of core current needed. The power dissipation of the TPS73601 is 0.56 Watts with 3 V in and 1.6 V at 400 mA out. This power dissipation gives a 23 degrees C temperature rise for the DRB package. Care should be used when using the DBV package of the TPS73601 since its temperature rise may not be suitable for some applications with high current draw or high input voltages.

Though not preferred, the TPS61020 is also capable of regulating from input voltages higher than the output voltage. TPS61020 will start to operate like a linear regulator once the input voltage is higher than 3.3 V. Therefore, the TPS61020 will still produce a regulated 3.3 V for I/O voltage with up to 5.5 V on the input. Since the TPS61020 is a linear regulator at higher input voltages, its efficiency will decrease substantially and its power dissipation will increase significantly. Additionally, since the TPS73601 linear regulator operates from the same input voltage, it too will have increased dissipated power. Close attention should be paid to the thermal performance of both parts operating in this condition.

POWER UP SEQUENCING:



The circuit will start to ramp up the I/O voltage immediately after the core voltage is above about 1.0V. The 1.0V value will vary with the characteristics of the transistors being used in the sequence circuit. Some systems may require a longer time delay between the core and I/O voltage applications. A capacitor can be added between the base of Q1 and ground to slow the turn on of the I/O voltage. The turn on time would be delayed by the RC time constant created by R1 and the added capacitor.

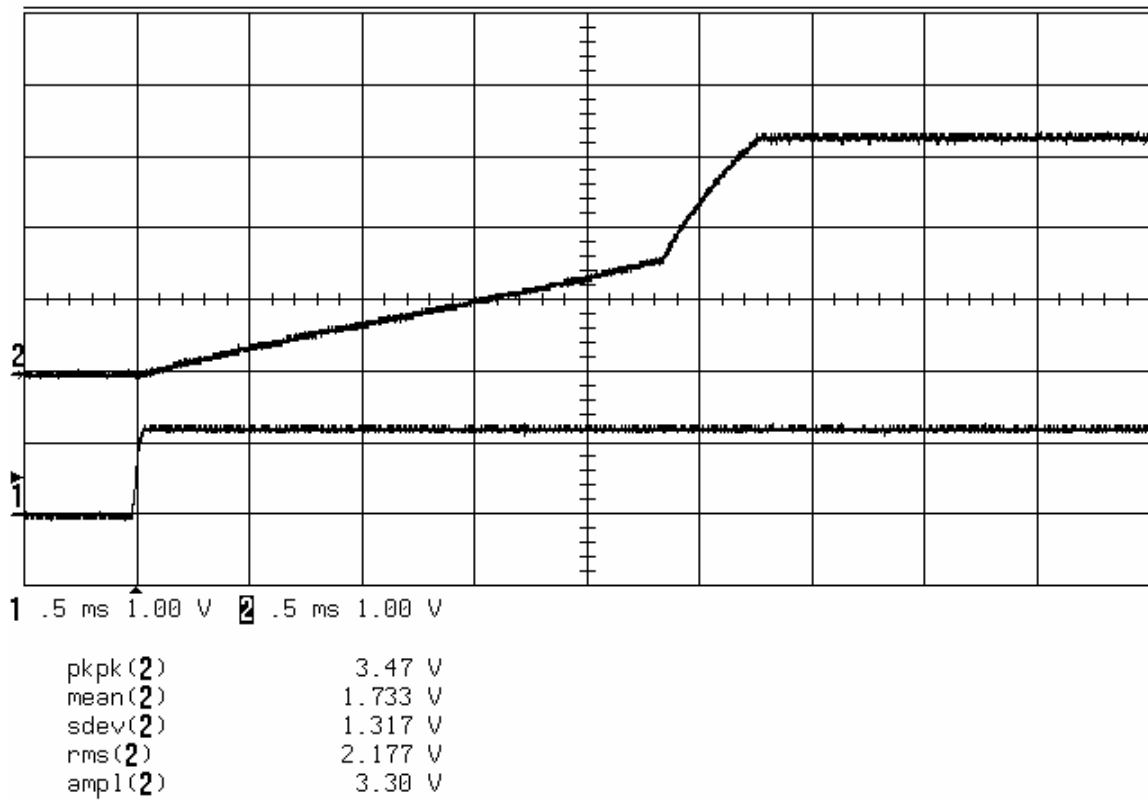
The sequencing circuits can be removed if sequencing is not required. Components R1, R2, R3, Q1 and Q2 can all be removed. The enable pins of both converters can be tied together so that both are enabled at the same time. This will not effect the minimum duration of the RESET signal.

IMPLEMENTATION NOTES:

- **Component selection:**

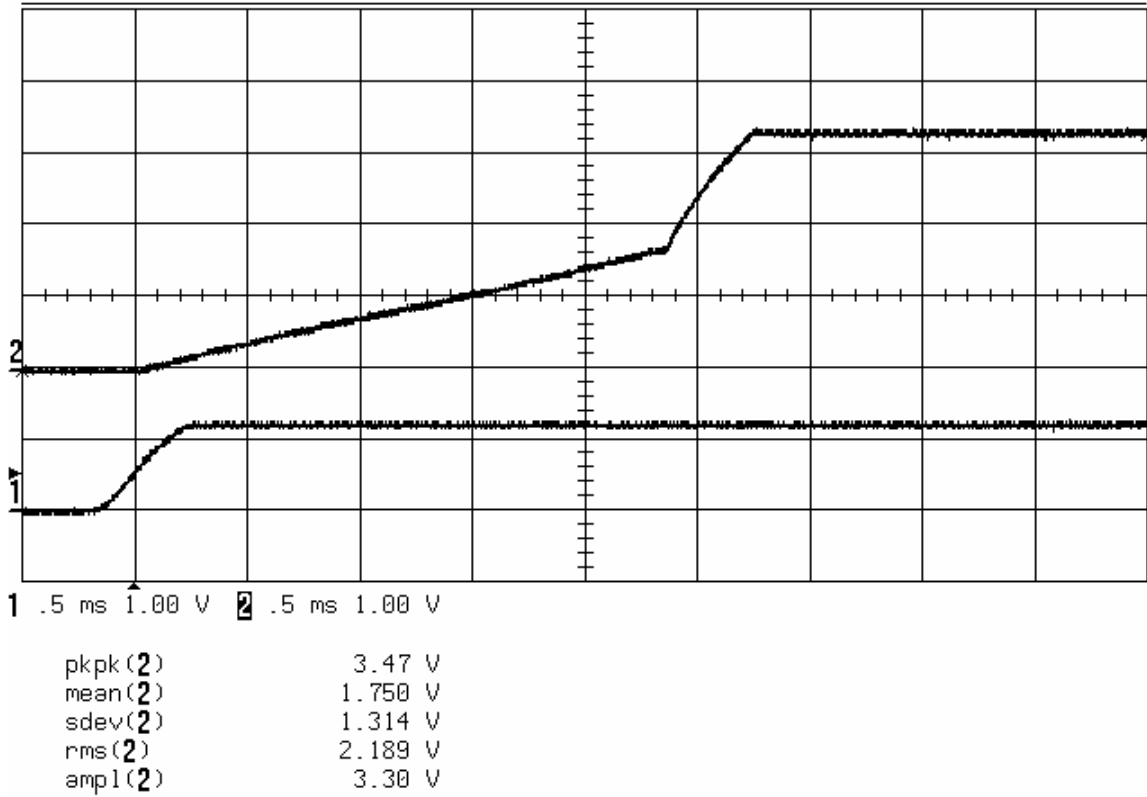
- o If a different capacitor is used for C3 than recommended per the BOM, it must meet the ESR requirements per the TPS73601 datasheet.

WAVEFORMS:



□ NORMAL

Figure 1 - Power up with $V_{IN} = 1.8\text{ V}$, $V_{core} = 1.2\text{ V}$ @ 110 mA, $V_{i/o} = 3.3\text{ V}$ @ 50 mA



□ NORMAL

Figure 2 - Power up from Enable when $V_{IN} = 1.8\text{ V}$, $V_{core} = 1.2\text{ V}@ 110\text{ mA}$, $V_{i/o} = 3.3\text{ V}@ 50\text{ mA}$

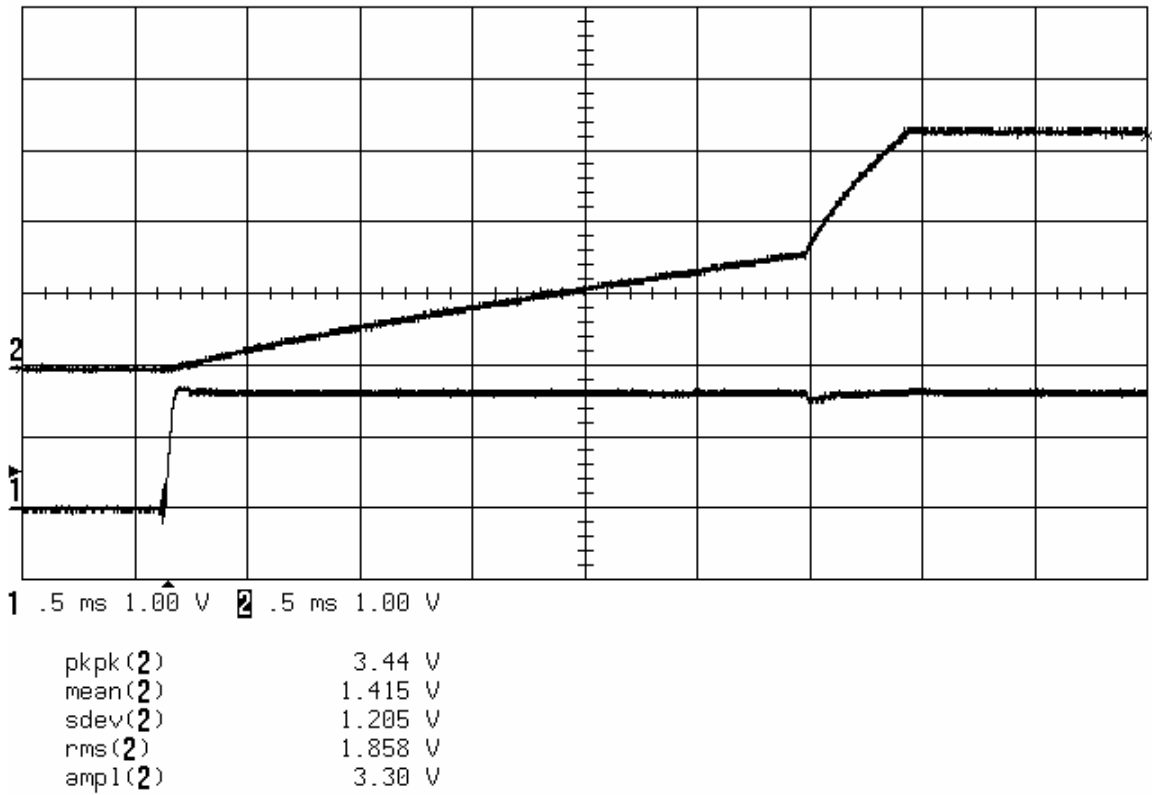


Figure 3 - Power up with $V_{IN} = 1.8\text{ V}$, $V_{core} = 1.6\text{ V}$ @ 267 mA , $V_{i/o} = 3.3\text{ V}$ @ 70 mA

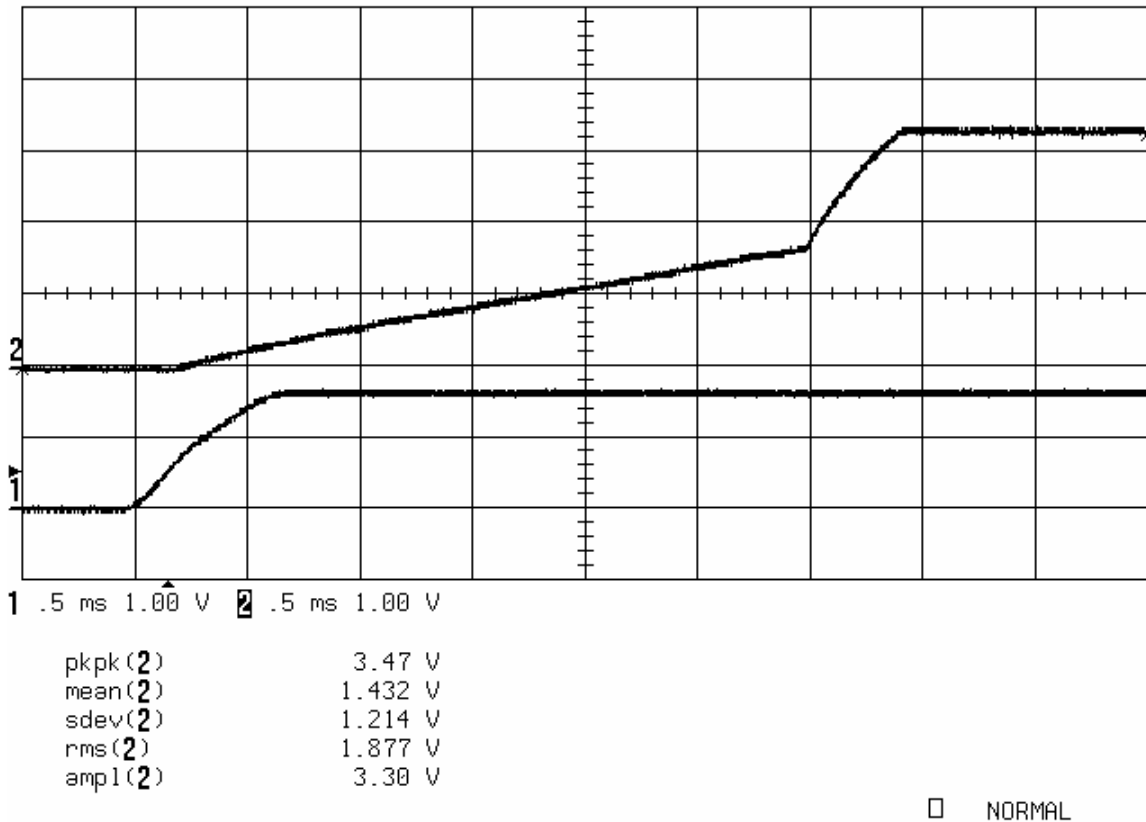


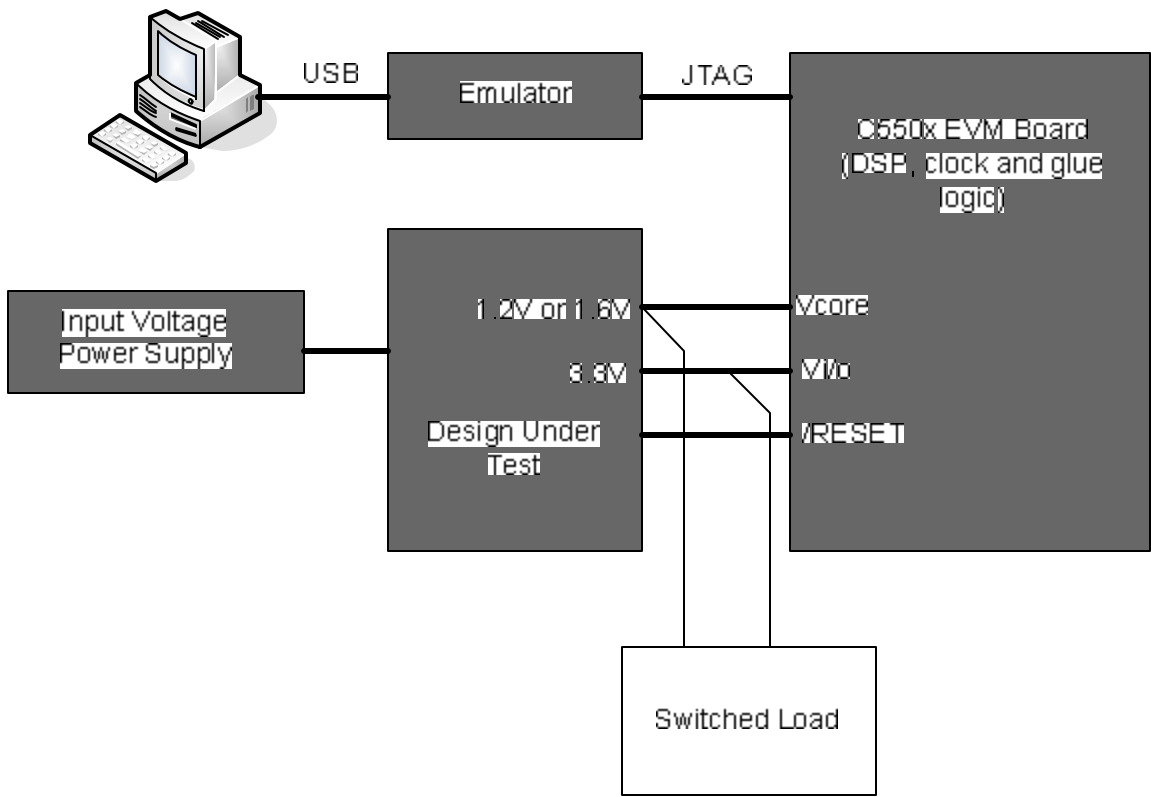
Figure 4 - Power up from Enable when $V_{IN} = 1.8\text{ V}$, $V_{core}=1.6\text{ V @ }267\text{ mA}$, $V_{i/o} = 3.3\text{V @ }70\text{ mA}$

TESTING METHOD:

The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

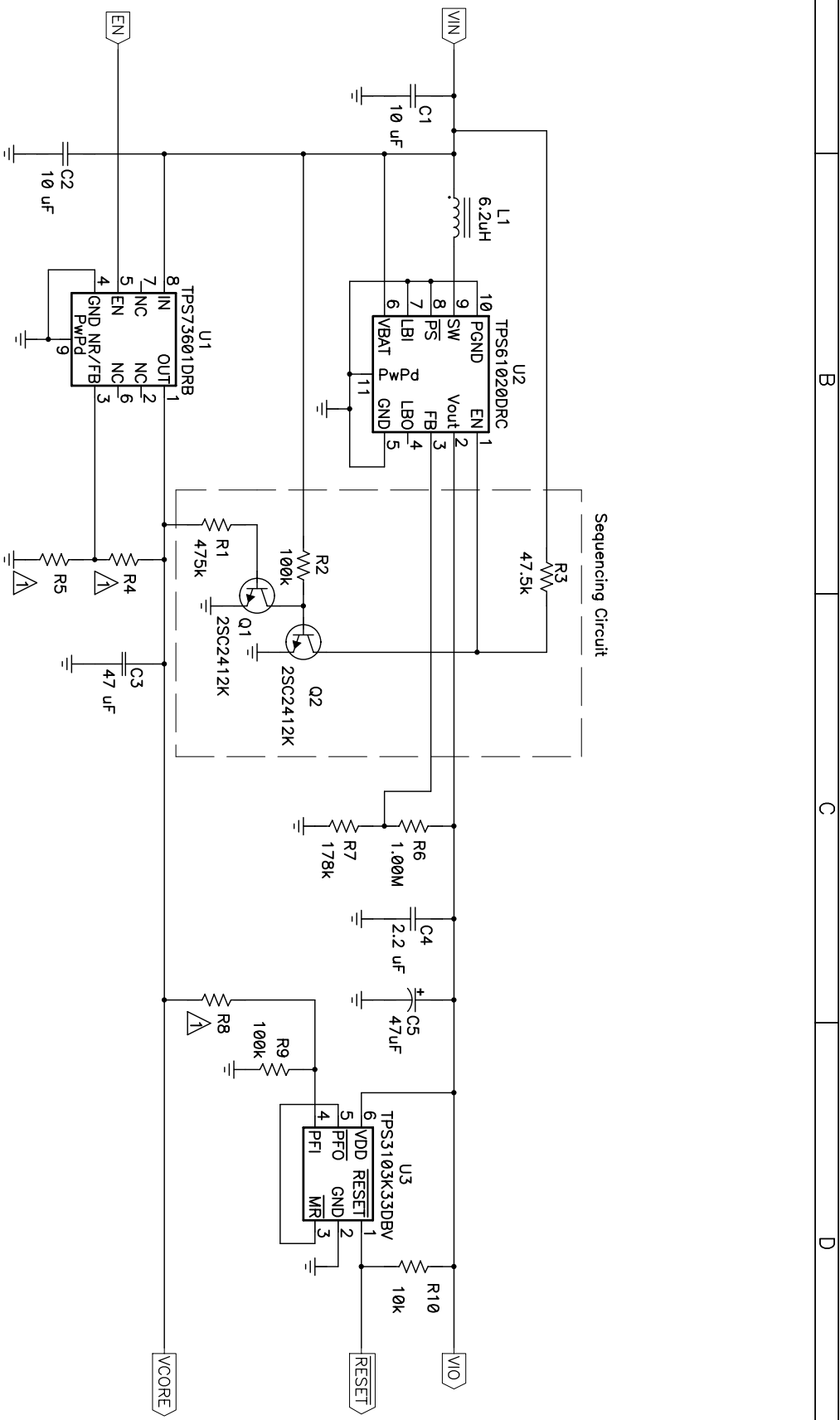
Voltage (V)	Function	Full load current (mA)
1.2	core	110
1.6	core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:



QUESTIONS:

Send an email to <mailto:dsppower@list.ti.com>



Voltage	R4	R5	R8
1.2V	0	Open	97.6k
1.6V	27.4k	82.5k	162k

Title		C5000 DSP Attach Design 3	
Size		for 1.8 < Vmin < 3.0V	
Number	PR420	Rev	
Date	02/14/05	Drawn by	
Filename	pr420.sch	Sheet	of

Filename: PR420_bom.xls						
Date: 02/14/2005						
PR420 BOM						
COUNT						
-001	-002	RefDes	Description	Size	Part Number	MFR
2	2	C1, C2	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J106KE01	muRata
1	1	C3	Capacitor, Ceramic, 47-uF, 6.3-V, X5R, 10%	1210	GRM32ER60J476ME20	muRata
1	1	C4	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J225KC01B	muRata
1	1	C5	Capacitor, Tantalum, 47-uF, 16-V, 110-milliohm, 20%	6032 (C)	594D476X0016C2T	Vishay
1	1	L1	Inductor, SM Toroid, 6.2uH, 1.8-A, 43-milliohms	0.224	CDRH5D28-6R2	Sumida
2	2	Q1, Q2	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
1	1	R1	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
2	2	R2, R9	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R3	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R4	Resistor, Chip, 0-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 27.4k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0	R5	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 82.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R6	Resistor, Chip, 1.00M-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R7	Resistor, Chip, 178k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R8	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R10	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Cap-Free, NMOS, 400mA LDO Regulator With Reverse Current Protection	QFN-8	TPS73601DRB	TI
1	1	U2	IC, Synchronous Boost Converter, Adj V	DRC10	TPS61020DRC	TI
1	1	U3	IC, Ultra Low Current/Supply, Voltage Supervisor	SOT23-6	TPS3103K33DBV	TI

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265