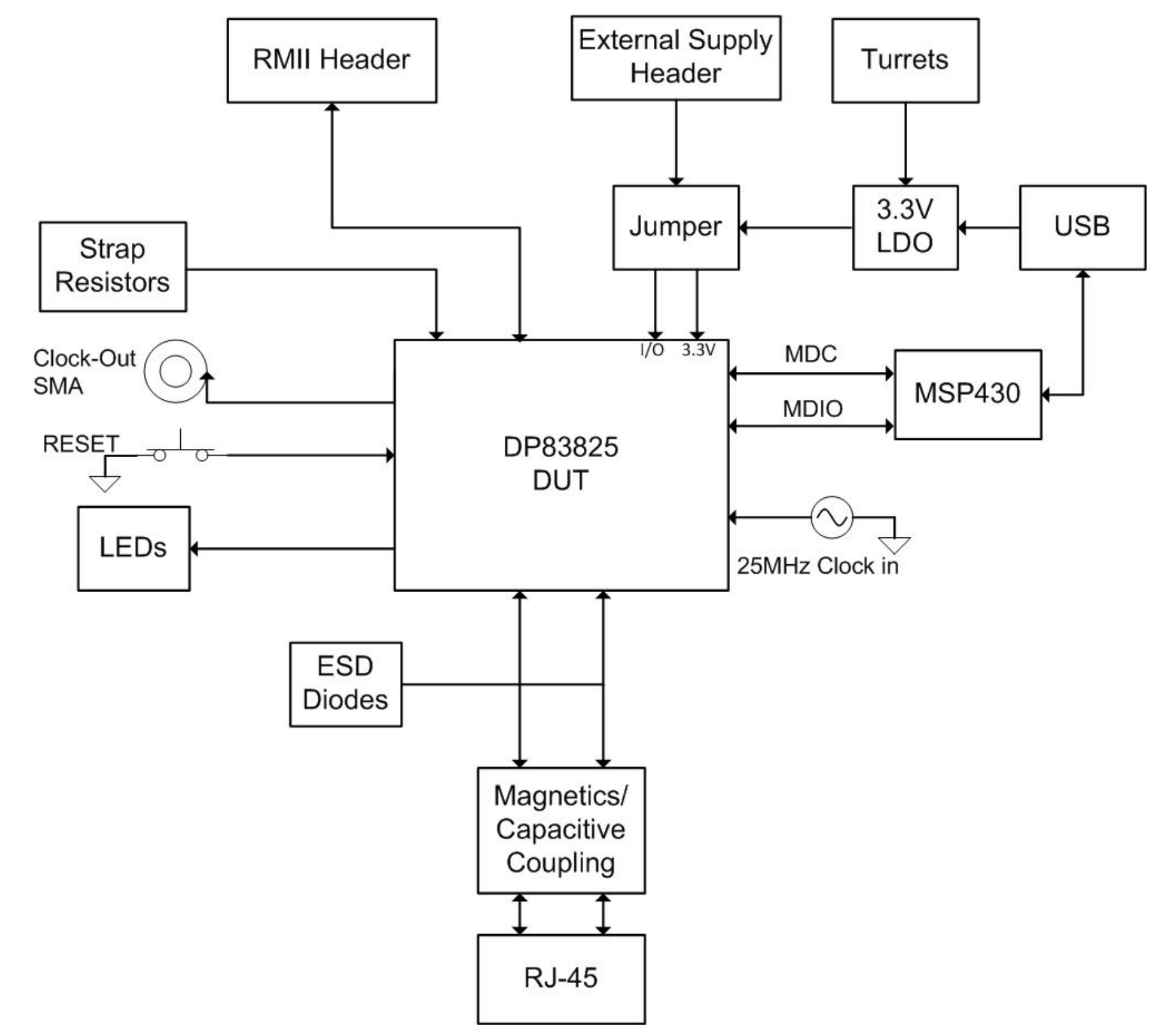
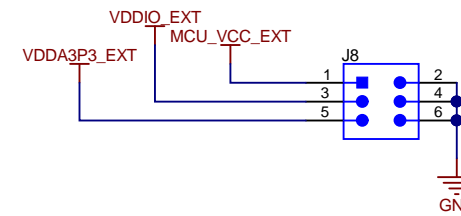
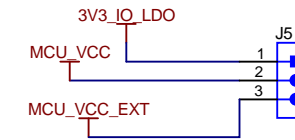
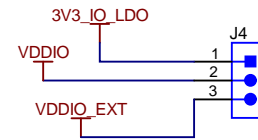
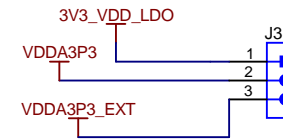
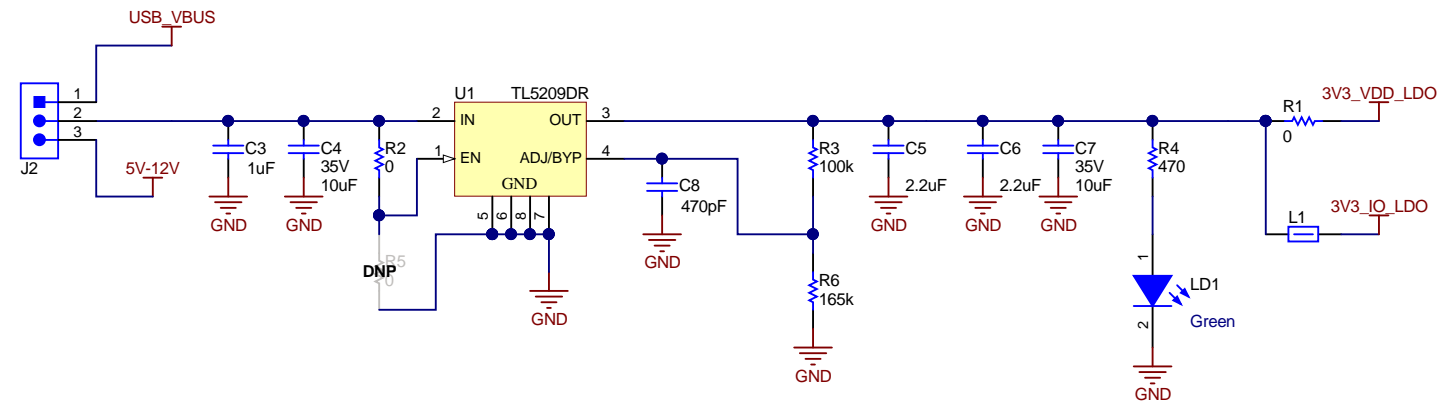
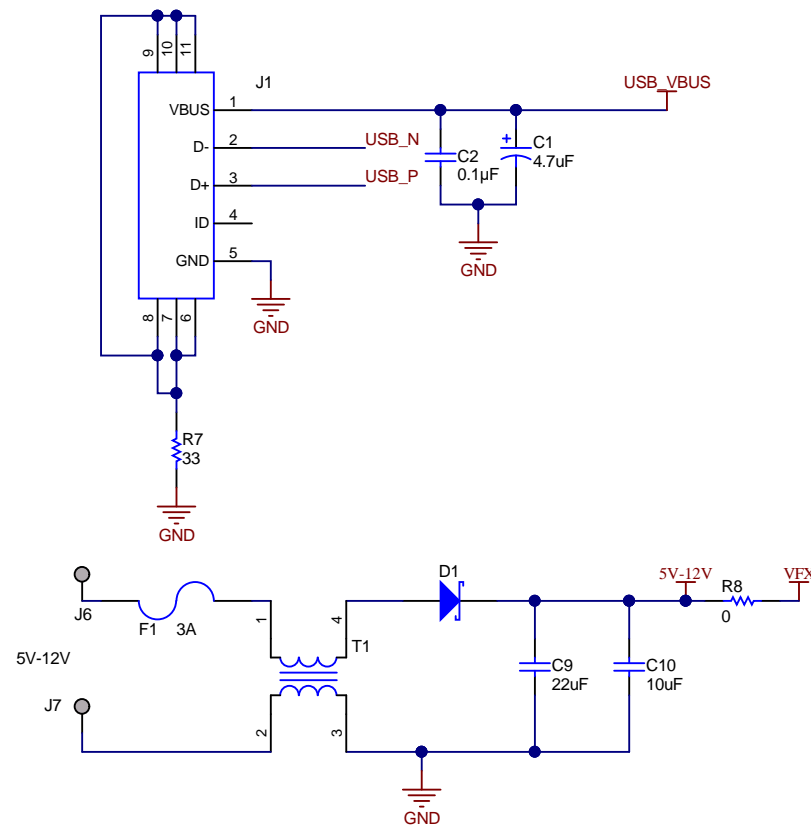


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



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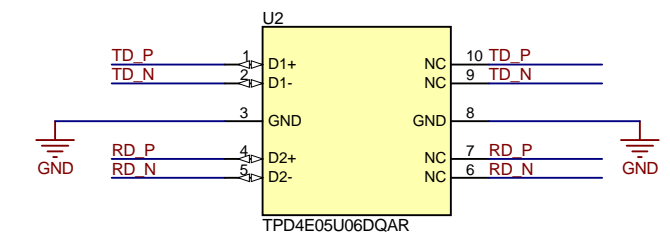
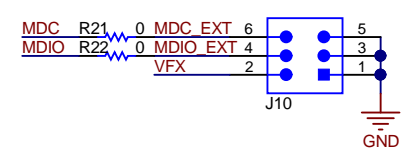
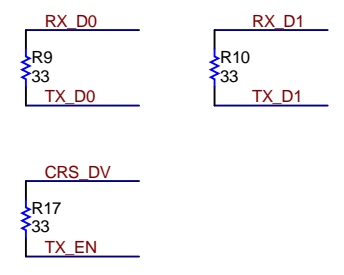
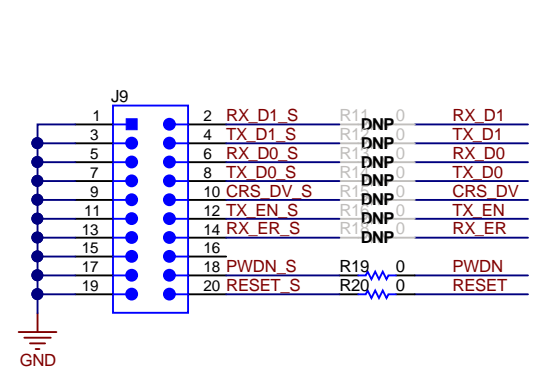
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TID #: N/A	Project Title: DP83825EVM		
Number: HSDC045	Rev: B	Sheet Title: Block Diagram	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 5	
Drawn By: Aniruddha Khadye	File: HSDC045B_CoverSheet.SchDoc	Size: B	
Engineer: Aniruddha Khadye	Contact: https://e2e.ti.com/support/interface/ethernet/		



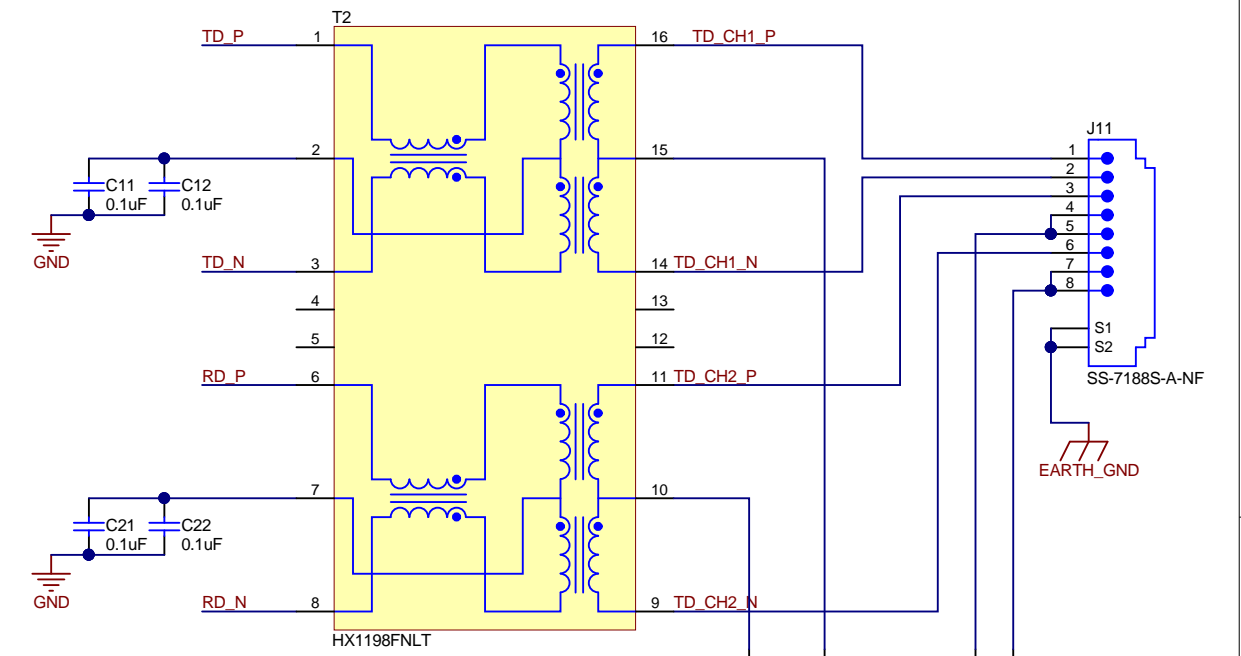
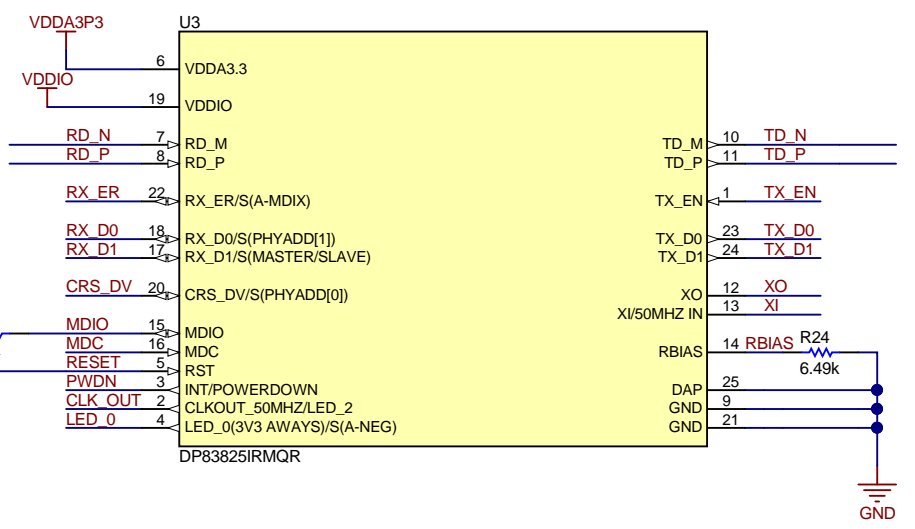
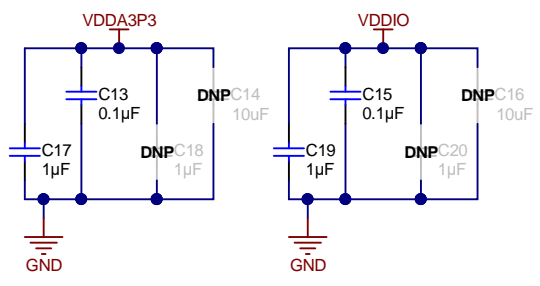
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Drawn By:	File: HSDC045B_Power.SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: https://e2e.ti.com/support/interface/ethernet/	



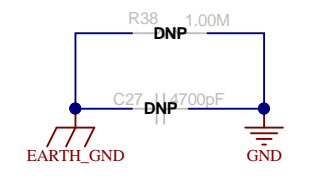
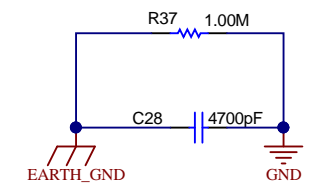
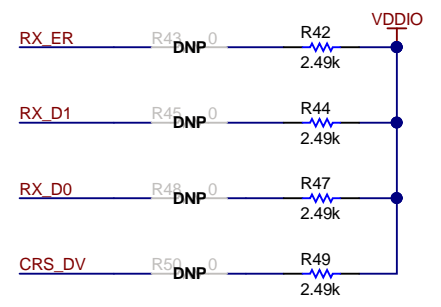
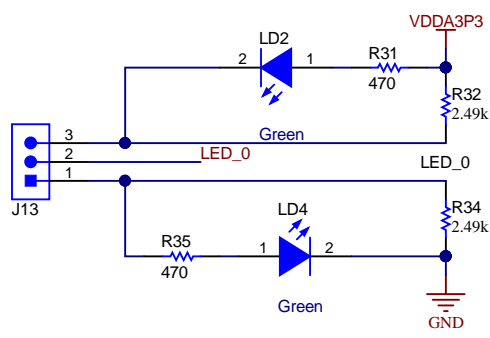
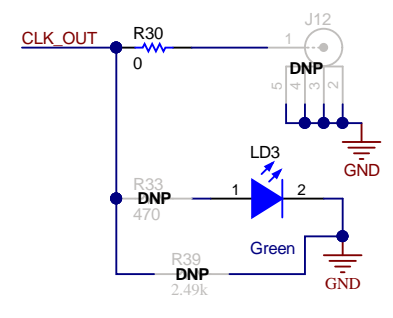
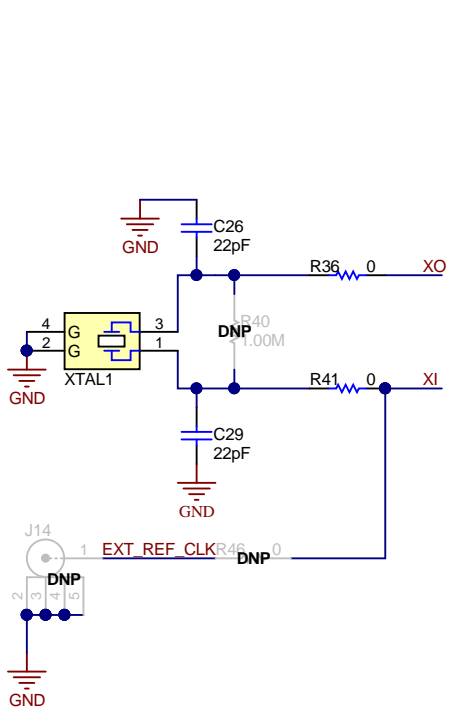
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NOTE: Use all 4 capacitors on VDDA3P3 and VDDIO rails for improved EMI/EMC performance. The values should be 0.01uF, 0.1uF, 1uF, and 10uF. Keep the smallest value capacitor closer to the PHY.



NOTE: Magnetics can have CMC facing the PHY side or facing the cable side. DP83825I can work with both types of Magnetics. It recommended to select magnetics with CMC facing the cable side.

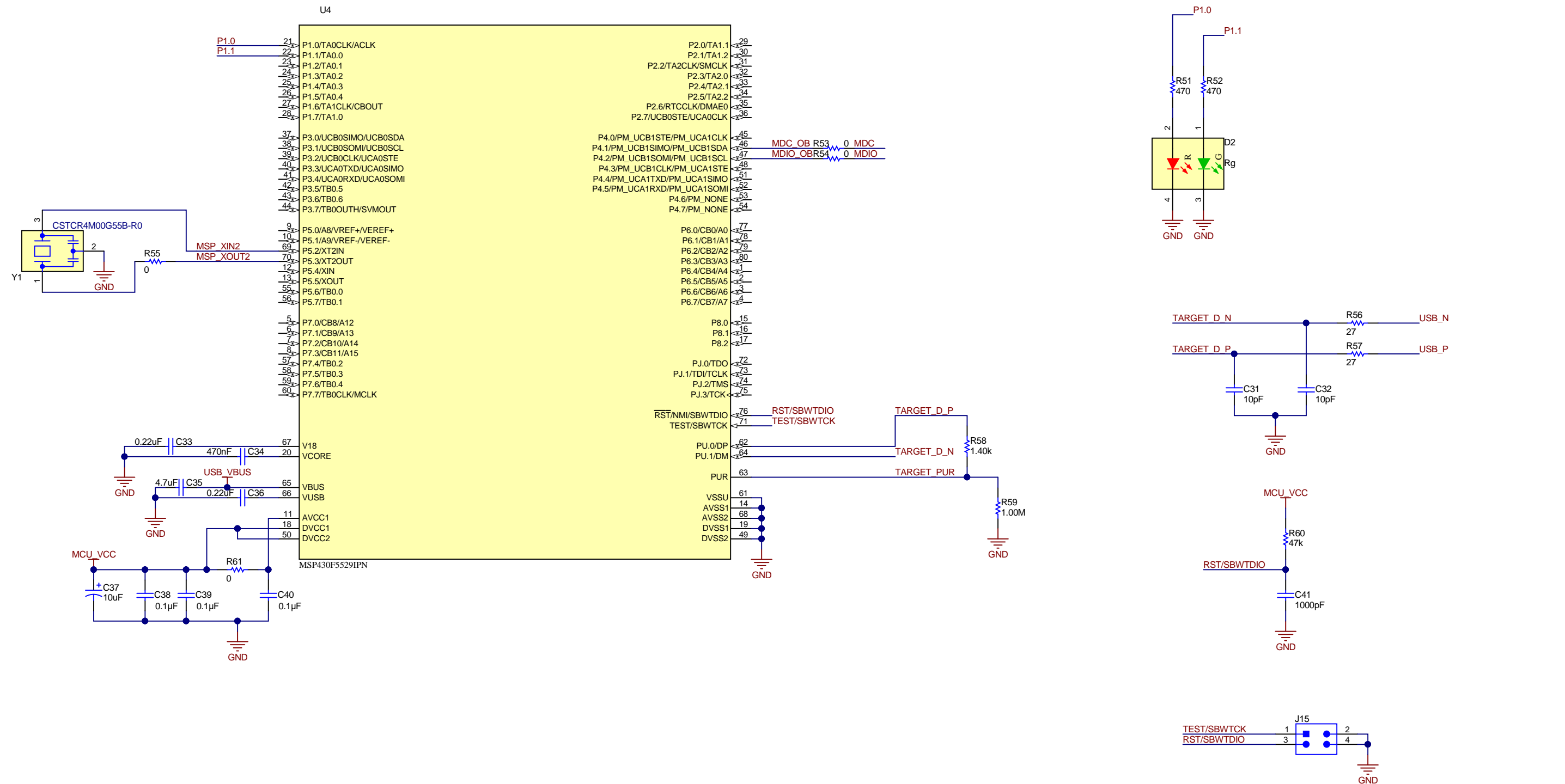


NOTE: Use two 4700pF capacitors between Earth Ground and System Ground to improve EMI/EMC performance.

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TID #: N/A	Project Title: DP83825EVM	
Number: HSDC045	Rev: B	Sheet Title: DP83825
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 5
Drawn By: Aniruddha Khadye	File: HSDC045B_DP83825.SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: https://e2e.ti.com/support/interface/ethernet/	



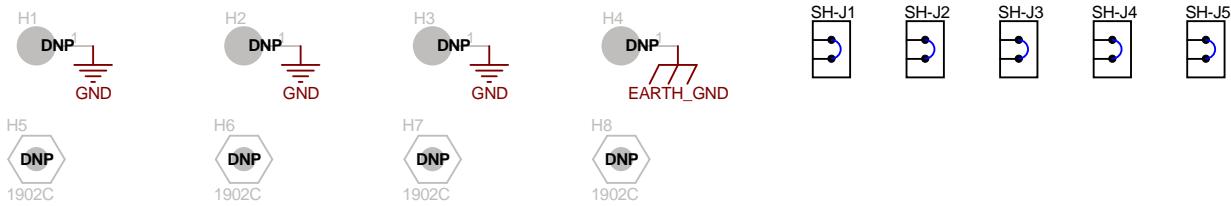


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TID #: N/A	Project Title: DP83825EVM	
Number: HSDC045	Rev: B	Sheet Title: Straps and MSP430
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 5
Drawn By: Aniruddha Khadye	File: HSDC045B_Coms.SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: https://e2e.ti.com/support/interface/ethernet/	



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PCB Rev: B

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ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Orderable: DP83825EVM	Designed for: Public Release	Mod. Date: 7/8/2019
TID #: N/A	Project Title: DP83825EVM	
Number: HSDC045	Rev: B	Sheet Title: Hardware Page
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 5 of 5
Drawn By: Aniruddha Khadye	File: HSDC045B_Hardware.SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: https://e2e.ti.com/support/interface/ethernet/	



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