ADC34RF55 クワッド・チャネル、14 ビット、3GSPS RF サンプリング・データ・コンバータ

1 特長

- 14 ビット、クワッド チャネル、3GSPS ADC
- 最大出力レート:1.5GSPS
- ノイズ・スペクトル密度:
  - 平均化なしで -156dBFS/Hz
  - 2 倍の平均化で -158dBFS/Hz
- シングル・コア (非インターリーブ) ADC アーキテクチャ
- アパーチャ・ジッタ:50fs
- 低いクローズイン残留位相ノイズ:
  - -127dBc/Hz (10kHz オフセット時)
- スペクトラム性能 (f_{IN} = 0.9GHz、-4dBFS 時):
  - 2 倍の内部平均化
  - SNR:62.3dBFS
  - SFDR HD2、3:63dBc
  - SFDR の最大スプリアス:85dBFS
- スペクトラム性能 (f_{IN} = 1.8GHz、-4dBFS 時):
  - 2 倍の内部平均化
  - SNR:63dBFS
  - SFDR HD2、3:68dBc
  - SFDR の最大スプリアス:86dBFS
- 入力フルスケール:1.1、1.35Vpp (2、3.5dBm)
- コード・エラー・レート (CER):10^{-15}
- フルパワー入力帯域幅 (-3dB):2.75GHz
- JESD204B シリアル・データ・インターフェイス
  - 最大レーン速度:13Gbps
  - サブクラス 1 の確定的レイテンシをサポート
- デジタル・ダウンコンバータ
  - ADC チャネルごとに最大 2 つの DDC
  - 複雑な出力:4 倍～128 倍のデシメーション (間引き)
  - 48 ビット NCO による位相コヒーレント周波数ホッピング
  - 高速周波数ホッピング:1µs 未満
- 消費電力:1.2W/チャネル
- 電源:1.8V、1.2V

2 アプリケーション

- フェーズド・アレイ・レーダー
- ソフトウェア無線 (SDR)
- スペクトル・アナライザ
- 高速デジタイザ
- ケーブル・インフラストラクチャ
- 電子兵器
- 通信インフラ

3 概要

ADC34RF55 は、シングル コアの 14 ビット、3GSPS、クワッド チャネル A/D コンバータ (ADC) であり、最大 3GHz の入力周波数での RF サンプリングをサポートします。このデザインは、信号対雑音比 (SNR) を最大化し、-156dBFS/Hz のノイズ スペクトル密度を実現します。追加の内蔵 ADC とオンチップ信号平均化を使用すると、ノイズ密度は -158dBFS/Hz に向上します。

各 ADC チャネルは、位相コヒーレント周波数ホッピングをサポートする 48 ビット NCO を使用する、デュアルバンドのデジタル・ダウンコンバータ (DDC) に接続できます。NCO 周波数制御に GPIO ピンを使用すると、1µs 未満で周波数ホッピングを実現できます。

このデバイスは、サブクラス 1 の確定的レイテンシを持つ JESD204B シリアル データ インターフェイスをサポートし、最大 13Gbps のデータ レートを使用します。ADC チャネルごとに 2 つの SerDes レーンしかありません。したがって、バイパス モードでは、サポートされる最大出力データ レートは 1.5GSPS です。チップ上でより高速な ADC サンプリング レートを使用する場合は、デシメーションが必要です。

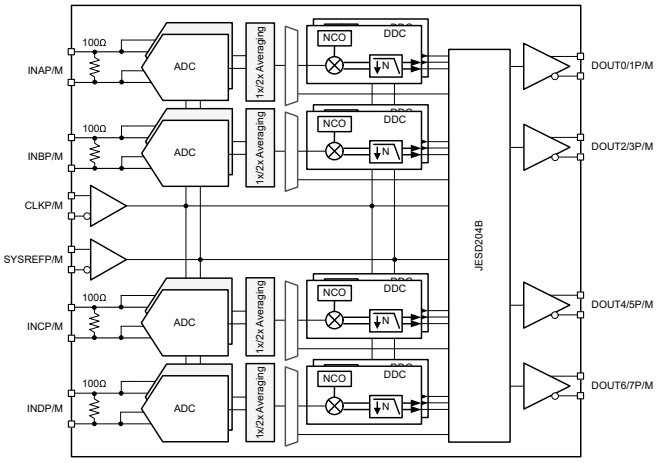
電力効率の優れた ADC アーキテクチャは、1.2W/ch の消費電力を実現し、低サンプリング レートで電力スケーリングを実現します。

製品情報

部品番号	最大サンプリング・レート	パッケージ (1)
ADC34RF55	3GSPS	QFN (64)
ADC34RF52	1.5GSPS	QFN (64)

(1) 詳細については、セクション 10 を参照してください。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



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4 Pin Configuration and Functions

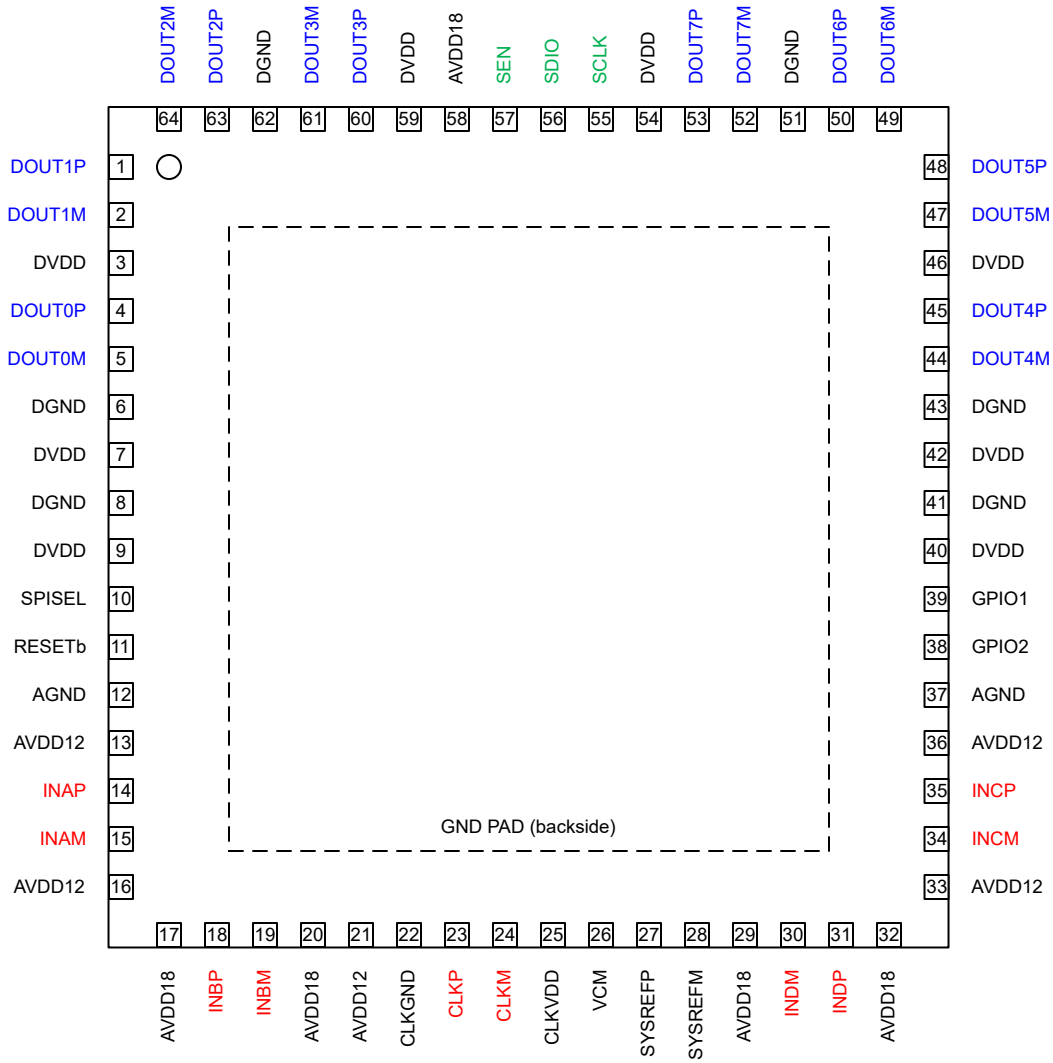

図 4-1. RTD Package, 64 Pin QFN (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ANALOG INPUTS			
INAP	14	I	Differential analog input for channel A. 100 Ω differential internal termination.
INAM	15		
INBP	18	I	Differential analog input for channel B. 100 Ω differential internal termination.
INBM	19		
INCP	35	I	Differential analog input for channel C. 100 Ω differential internal termination.
INCM	34		
INDP	31	I	Differential analog input for channel D. 100 Ω differential internal termination.
INDM	30		
VCM	26	O	Common-mode voltage output for the analog inputs.
CLOCK, SYNCHRONIZATION			

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表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLKP	23	I	Differential sampling clock input. 100 Ω differential internal termination.
CLKM	24		
SYSREFP	27	I	Differential external synchronization input.
SYSREFM	28		
CONTROL			
RESETb	11	I	Hardware reset. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD18.
SEN	57	I	Serial interface enable. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD18.
SCLK	55	I	Serial interface clock input. This pin has an internal 21 kΩ pull-down resistor.
SDIO	56	I/O	Serial interface data input and output. This pin has an internal 21 kΩ pull-down resistor.
GPIO1	39	I/O	GPIO control pin. This pin is configured through SPI interface for power down or NCO control function.
GPIO2	38	I/O	GPIO control pin. This pin is configured through SPI interface for power down or NCO control function.
SPISEL	10	I	Determines the functional of the SPI interface pins: either normal SPI for register programming or fast access to NCO selection only for fast frequency hopping.
DIGITAL DATA INTERFACE			
DOUT0P	4	O	JESD204B high-speed serial data output interface pins for channels A to D. Output lanes can be reordered using the output MUX.
DOUT0M	5		
DOUT1P	1	O	
DOUT1M	2		
DOUT2P	63	O	
DOUT2M	64		
DOUT3P	60	O	
DOUT3M	61		
DOUT4P	45	O	
DOUT4M	44		
DOUT5P	48	O	
DOUT5M	47		
DOUT6P	50	O	
DOUT6M	49		
DOUT7P	53	O	
DOUT7M	52		
POWER SUPPLY			
AVDD18	17,20,29,32, 58	I	Analog 1.8-V power supply
AVDD12	13,16,21,33, 36	I	Analog 1.2-V power supply
CLKVDD	25	I	Clock 1.2-V power supply. Very sensitive to power supply noise. Directly impacts close in aperture phase noise.
DVDD	3,7,9,40,42, 46,54,59	I	Digital 1.2-V power supply
AGND	12,37	I	Analog ground, shorted to thermal pad.
CLKGND	22	I	Clock ground.
DGND	6,8,41,43,51,62	I	Digital ground.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD18		–0.3	2.1	V
Supply voltage range, AVDD12		–0.3	1.4	V
Supply voltage range, CLKVDD		–0.3	1.4	V
Supply voltage range, DVDD		–0.3	1.4	
Voltage applied to input pins	INAP/M, INBP/M, INCP/M, INDP/M	–0.6	1.2	
	CLKP/M	–0.3	VDDCLK + 0.3	
	SYSREFP/M	–0.3	AVDD12 + 0.6	V
	GPIO1/2, PDN, RESET, SCLK, SEN, SDIO, SPISEL	–0.3	AVDD18 + 0.2	V
Peak RF input power (INAP/M, INBP/M, INCP/M, INDP/M)	Differential 100 Ω termination.		12	dBm
Junction temperature, T_J	Junction temperature, T_J		115	°C
Storage temperature, T_{stg}	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD18	1.8 V analog supply	1.75	1.8	1.85	V
AVDD12	1.2 V analog supply	1.175	1.2	1.225	V
CLKVDD	1.2 V clock supply	1.175	1.2	1.225	V
DVDD	1.2 V digital supply	1.175	1.2	1.225	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature			105(1)	°C
	Maximum Operating Junction Temperature Range	125			

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

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5.4 Thermal Information

THERMAL METRIC[1]		ADC34RF5x RTD (QFN) 64 Pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	20.1	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	6.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 3.0 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FS = 3.0 GSPS						
I_{AVDD18}	Supply current, 1.8 V analog supply	Single band, 8x complex decimation, LMFS = 8-8-2-1		340		mA
I_{AVDD12}	Supply current, 1.2 V analog supply			1150		
I_{CLKVDD}	Supply current, 1.2 V clock supply			140		
I_{DVDD}	Supply current, 1.2 V digital supply			2300		
P_{DIS}	Power dissipation			4.9		W
I_{AVDD18}	Supply current, 1.8 V analog supply	2x averaging Single band, 8x complex decimation, LMFS = 8-8-2-1		515	620	mA
I_{AVDD12}	Supply current, 1.2 V analog supply			1800	2320	
I_{CLKVDD}	Supply current, 1.2 V clock supply			160	210	
I_{DVDD}	Supply current, 1.2 V digital supply			3000	4600	
P_{DIS}	Power dissipation			6.9		W
POWER DOWN MODES						
P_{DIS}	Power down mode power consumption			190		mW

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5.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 2.6 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
DNL	Differential nonlinearity	F_{IN} = 10 MHz		± 0.85		LSB
INL	Integral nonlinearity	F_{IN} = 10 MHz		± 3.5		LSB
V_{OS_ERR}	Offset error			± 2		%FSR
$GAIN_{ERR}$	Gain error			± 3		%FSR
$GAIN_{Match}$	Gain matching across channels			± 0.2		dB
ADC ANALOG INPUTS (INAP/M, INBP/M, INCP/M, INDP/M)						
FS	Input full scale	Differential, non-average mode		1.1		Vpp
		Differential, 2x average mode		1.35		
V_{ICM}	Input common model voltage		250	350	450	mV
Z_{IN}	Differential input impedance	Differential at 100 MHz		100		Ω
V_{OCM}	Output common mode voltage			350		mV
BW	Analog Input Bandwidth (-3 dB)	No averaging		2.75		GHz
		2x averaging		2.75		
Phase imbalance, analog input				± 2		deg
Amplitude imablance, analog input				± 1		%
CLOCK INPUT (CLKP/M)						
Input clock frequency			500		3000	MHz
V_{ID}	Differential input voltage			1	2.4	Vpp
V_{ICM}	Input common mode voltage		0.65	0.75	0.85	V
Z_{IN}	Differential input impedance	Differential at 2.6 GHz		100		Ω
Clock duty cycle			45	50	55	%
SYSREF INPUT (SYSREFP/M)						
V_{ID}	Differential input voltage		600	800	1000	mVpp
V_{ICM}	Input common mode voltage	Input common mode voltage	1.05	1.2	1.4	V
Z_{IN}	Differential input impedance			100		Ω
DIGITAL INPUTS (RESET, PDN, SCLK, SEN, SDIO, GPIO1/2, SPISEL)						
V_{IH}	High-level input voltage		0.8			V
V_{IL}	Low-level input voltage				0.4	V
C_I	Input capacitance			0.6		pF
DIGITAL OUTPUTS (SDIO)						
V_{OH}	High-level output voltage	I_{LOAD} = -400 uA	AVDD18 – 0.1	AVDD18		V
V_{OL}	Low-level output voltage	I_{LOAD} = 400 uA			0.1	V
CML SERDES OUTPUTS: DOUT[0..7]P/M						
V_{OD}	Serdes transmitter output amplitude	differential peak-peak		700		mVpp
V_{OCM}	Serdes transmitter output common mode			425		mV
Z_{TX}	Serdes transmitter single ended termination impedance			50		Ω
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA

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5.7 Electrical Characteristics - AC Specifications (Dither DISABLED)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 2.6 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	f_{IN} = 900 MHz, A_{IN} = -20 dBFS no averaging		–155.6		dBFS/Hz
		f_{IN} = 900 MHz, A_{IN} = -20 dBFS 2x averaging		–158.1		
NF	Noise Figure	f_{IN} = 900 MHz, Ain = -20 dBFS, no averaging		20.2		dB
		f_{IN} = 900 MHz, Ain = -20 dBFS, 2x averaging		19.8		dB
SNR	Signal-to-noise ratio no averaging (DDC bypass characterization mode)	f_{IN} = 100 MHz		62.1		dBFS
		f_{IN} = 500 MHz		61.8		
		f_{IN} = 900 MHz		61.7		
		f_{IN} = 900 MHz, Ain = -20 dBFS		63.8		
		f_{IN} = 1.8 GHz		61.1		
		f_{IN} = 2.4 GHz		60.2		
	Signal-to-noise ratio no averaging 8x complex decimation	f_{IN} = 500 MHz		68.5		
		f_{IN} = 900 MHz		68.0		
		f_{IN} = 900 MHz, Ain = -20 dBFS		69.4		
		f_{IN} = 1.8 GHz		66.6		
		f_{IN} = 2.4 GHz		66.0		
	Signal-to-noise ratio 2x averaging (DDC bypass characterization mode)	f_{IN} = 100 MHz		63.6		
		f_{IN} = 500 MHz		63.3		
		f_{IN} = 900 MHz		63.5		
		f_{IN} = 900 MHz, Ain = -20 dBFS		66.3		
		f_{IN} = 1.8 GHz		62.7		
		f_{IN} = 2.4 GHz		62.4		
	Signal-to-noise ratio 2x averaging 8x complex decimation	f_{IN} = 500 MHz		69.7		
		f_{IN} = 900 MHz		68.0		
		f_{IN} = 900 MHz, Ain = -20 dBFS		69.5		
		f_{IN} = 1.8 GHz		67.4		
		f_{IN} = 2.4 GHz		67.0		
SINAD (1)	Signal to noise and distortion ratio (DDC bypass characterization mode)	f_{IN} = 100 MHz		58.2		dBFS
		f_{IN} = 500 MHz		57.9		
		f_{IN} = 900 MHz		55.8		
		f_{IN} = 1.8 GHz		58.2		
		f_{IN} = 2.4 GHz		54.8		
ENOB (1)	Effective number of bits (DDC bypass characterization mode)	f_{IN} = 100 MHz		10.0		Bits
		f_{IN} = 500 MHz		10.0		
		f_{IN} = 900 MHz		10.0		
		f_{IN} = 1.8 GHz		9.9		
		f_{IN} = 2.4 GHz		9.7		

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5.7 Electrical Characteristics - AC Specifications (Dither DISABLED) (続き)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 2.6 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD(1)	Total Harmonic Distortion (First five harmonics) (DDC bypass characterization mode)	f_{IN} = 100 MHz		61		dBc
		f_{IN} = 500 MHz		60		
		f_{IN} = 900 MHz		57		
		f_{IN} = 1.8 GHz		63		
		f_{IN} = 2.4 GHz		57		
HD2(1)	Second Harmonic Distortion (DDC bypass characterization mode)	f_{IN} = 100 MHz		61		dBc
		f_{IN} = 500 MHz		66		
		f_{IN} = 900 MHz		68		
		f_{IN} = 1.8 GHz		66		
		f_{IN} = 2.4 GHz		57		
HD3(1)	Third Harmonic Distortion (DDC bypass characterization mode)	f_{IN} = 100 MHz		66		dBc
		f_{IN} = 500 MHz		62		
		f_{IN} = 900 MHz		57		
		f_{IN} = 1.8 GHz		65		
		f_{IN} = 2.4 GHz		64		
Non HD2,3(1)	Spur free dynamic range (excluding HD2 and HD3) (DDC bypass characterization mode)	f_{IN} = 100 MHz		78		dBFS
		f_{IN} = 500 MHz		75		
		f_{IN} = 900 MHz		78		
		f_{IN} = 1.8 GHz		76		
		f_{IN} = 2.4 GHz		75		
IMD3(1)	Two tone inter-modulation distortion	f_1 = 700 MHz, f_2 = 800 MHz, A_{IN} = -7 dBFS/tone		72		dBFS
		f_1 = 1.5 GHz, f_2 = 1.6 GHz, A_{IN} = -7 dBFS/tone		66		

(1) Performance data shown is prior to decimation filtering. With DDC enabled, performance improves by the decimation filtering process.

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5.8 Electrical Characteristics - AC Specifications (Dither ENABLED)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 3.0 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V, –4-dBFS differential input and dither ENABLED, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Spectral Density	f_{IN} = 900 MHz, A_{IN} = -20 dBFS no averaging	-153.5	–155.1		dBFS/Hz
		f_{IN} = 900 MHz, A_{IN} = -20 dBFS 2x averaging		–157.3		
NF	Noise Figure	f_{IN} = 900 MHz, Ain = -20 dBFS, no averaging		20.7		dB
		f_{IN} = 900 MHz, Ain = -20 dBFS, 2x averaging		20.6		
SNR	Signal-to-noise ratio no averaging[1] [2] (DDC bypass characterization mode)	f_{IN} = 100 MHz		61.7		dBFS
		f_{IN} = 500 MHz		61.8		
		f_{IN} = 900 MHz	58.9	60.9		
		f_{IN} = 900 MHz, Ain = -20 dBFS	62.0	63.3		
		f_{IN} = 1.8 GHz		61.4		
		f_{IN} = 2.4 GHz		61.2		
	Signal-to-noise ratio no averaging 8x complex decimation	f_{IN} = 500 MHz		70.5		
		f_{IN} = 900 MHz		68.0		
		f_{IN} = 900 MHz, Ain = -20 dBFS		69.4		
		f_{IN} = 1.8 GHz		68.0		
		f_{IN} = 2.4 GHz		66.5		
	Signal-to-noise ratio 2x averaging[1] [2] (DDC bypass characterization mode)	f_{IN} = 100 MHz		63.1		
		f_{IN} = 500 MHz		63.4		
		f_{IN} = 900 MHz		62.3		
		f_{IN} = 900 MHz, Ain = -20 dBFS		65.5		
		f_{IN} = 1.8 GHz		63.0		
		f_{IN} = 2.4 GHz		62.1		
	Signal-to-noise ratio 2x averaging 8x complex decimation	f_{IN} = 500 MHz		70.5		
		f_{IN} = 900 MHz		68.0		
		f_{IN} = 900 MHz, Ain = -20 dBFS		69.4		
		f_{IN} = 1.8 GHz		68.0		
		f_{IN} = 2.4 GHz		66.5		
SINAD[1]	Signal to noise and distortion ratio (DDC bypass characterization mode)	f_{IN} = 100 MHz		60.5		dBFS
		f_{IN} = 500 MHz		60.8		
		f_{IN} = 900 MHz		59.5		
		f_{IN} = 1.8 GHz		60.3		
		f_{IN} = 2.4 GHz		58.6		
ENOB[1]	Effective number of bits (DDC bypass characterization mode)	f_{IN} = 100 MHz		10.0		Bits
		f_{IN} = 500 MHz		10.0		
		f_{IN} = 900 MHz		9.8		
		f_{IN} = 1.8 GHz		9.9		
		f_{IN} = 2.4 GHz		9.7		

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5.8 Electrical Characteristics - AC Specifications (Dither ENABLED) (続き)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 3.0 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V, –4-dBFS differential input and dither ENABLED, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD(1)	Total Harmonic Distortion (First five harmonics) (DDC bypass characterization mode)	f_{IN} = 100 MHz		67		dBc
		f_{IN} = 500 MHz		68		
		f_{IN} = 900 MHz		65		
		f_{IN} = 1.8 GHz		69		
		f_{IN} = 2.4 GHz		64		
HD2(1)	Second Harmonic Distortion (DDC bypass characterization mode)	f_{IN} = 100 MHz		64		dBc
		f_{IN} = 500 MHz		69		
		f_{IN} = 900 MHz	61	68		
		f_{IN} = 1.8 GHz		68		
		f_{IN} = 2.4 GHz		60		
HD3(1)	Third Harmonic Distortion (DDC bypass characterization mode)	f_{IN} = 100 MHz		71		dBc
		f_{IN} = 500 MHz		67		
		f_{IN} = 900 MHz	60	63		
		f_{IN} = 1.8 GHz		68		
		f_{IN} = 2.4 GHz		72		
Non HD2,3(1)	Spur free dynamic range (excluding HD2 and HD3) (DDC bypass characterization mode)	f_{IN} = 100 MHz		91		dBFS
		f_{IN} = 500 MHz		89		
		f_{IN} = 900 MHz	78	85		
		f_{IN} = 1.8 GHz		86		
		f_{IN} = 2.4 GHz		86		
IMD3(1)	Two tone inter-modulation distortion	f_1 = 700 MHz, f_2 = 800 MHz, A_{IN} = -10 dBFS/ tone		80		dBFS
		f_1 = 1.5 GHz, f_2 = 1.6 GHz, A_{IN} = -10 dBFS/ tone		75		

(1) Performance data shown is prior to decimation filtering. With DDC enabled, performance improves by the decimation filtering process.
(2) Measured from 100 MHz to FS/2 (ignoring DC to 100 MHz which contains the dither signal)

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5.9 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 2.6 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC TIMING SPECIFICATIONS						
T_{AD}	Aperture Delay			0.17		ns
	Aperure Delay variation			0.07		
T_A	Aperture Jitter			50		fs
Overload recovery time		3-dB overload condition		10		clock cycles
		6-dB overload condition		50		
t_{ADC}	ADC latency from sampling instant to internal hand-off to digital			68		ADC clock cycles
	Internal propagation delay			5		ns
	Latency adder for 2x averaging			4		ADC clock cycles
	Deterministic delay from digital block (DDC (if used) and JESD interface)	LMFS = 8-4-8-10		260		ADC clock cycles
		LMFS = 8-4-2-2		280		
		4x real decimation, LMFS = 8-4-2-2		456		
		4x decimation, F (number of octets) = 2		394		
		4x decimation, F = 4		374		
		4x decimation, F = 8		367		
		8x decimation, F = 2		560		
		8x decimation, F = 4		520		
		8x decimation, F = 8		506		
		8x decimation, F = 16		491		
		16x decimation, F = 2		900		
		16x decimation, F = 4		820		
		16x decimation, F = 8		792		
		16x decimation, F = 16		762		
		16x decimation, F = 32		748		
		32x decimation, F = 2		1596		
		32x decimation, F = 4		1436		
		32x decimation, F = 8		1380		
		32x decimation, F = 16		1320		
		32x decimation, F = 32		1292		
		64x decimation, F = 2		2940		
		64x decimation, F = 4		2620		
		64x decimation, F = 8		2508		
		64x decimation, F = 16		2388		
		64x decimation, F = 32		2332		
		128x decimation, F = 2		5668		
		128x decimation, F = 4		5028		
		128x decimation, F = 8		4804		
		128x decimation, F = 16		4564		
		128x decimation, F = 32		4452		

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5.9 Timing Requirements (続き)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at T_A = 25°C, ADC sampling rate = 2.6 GSPS, 8x complex decimation single band, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, AVDDCLK, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input						
$f_{CLK(SCLK)}$	Serial clock frequency		1		20	MHz
$t_{SU(SEN)}$	SEN to rising edge of SCLK		10			ns
$t_{H(SEN)}$	SEN from rising edge of SCLK		10			ns
$t_{SU(SDIO)}$	SDIO to rising edge of SCLK		10			ns
$t_{H(SDIO)}$	SDIO from rising edge of SCLK		10			ns
SERIAL PROGRAMMING INTERFACE (SDIO) - Output						
$t_{(OZD)}$	SDIO tri-state to driven				10	ns
$t_{(ODZ)}$	SDIO data to tri-state				14	ns
$t_{(OD)}$	SDIO valid from falling edge of SCLK				10	ns
TIMING: SYSREFP/M						
$t_{s(SYSREF)}$	Setup time, SYSREFP/M valid to rising edge of CLKP/M		50			ps
$t_{h(SYSREF)}$	Hold time, SYSREFP/M valid to rising edge of CLKP/M		50			ps
CML SERDES OUTPUTS: DA[0,1]P/M, DB[0,1]P/M, DC[0,1]P/M, DD[0,1]P/M						
f_{Serdes}	Serdes bit rate		0.5	12.8	13.0	Gbps
R_J	Random jitter	RPAT, 12.8 Gbps		0.6		ps
D_J	Deterministic jitter	RPAT, 12.8 Gbps		14.7		ps
T_J	Total jitter, peak-peak	RPAT, 12.8 Gbps		24		ps

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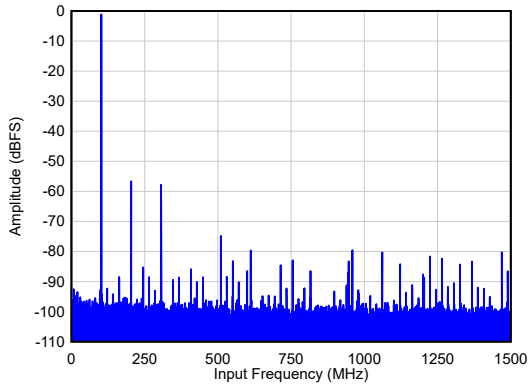
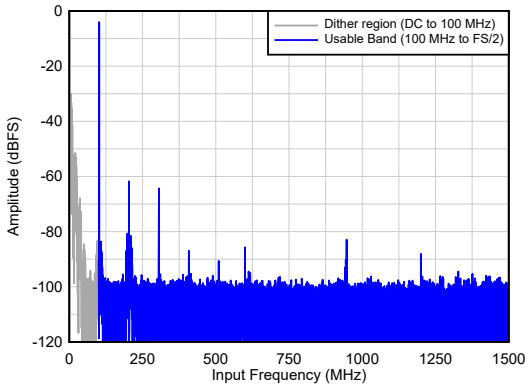
5.10 Typical Characteristics

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



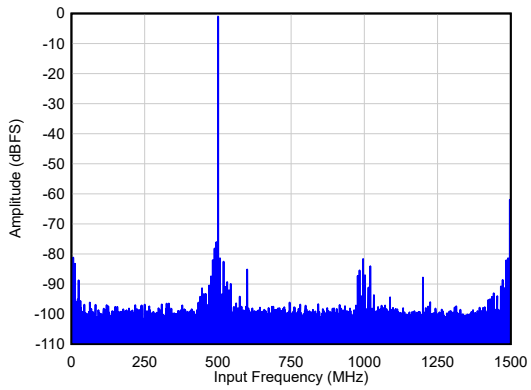
SNR = 62.1 dBFS, SFDR = 57 dBc, Non HD23 = 75 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-1. Single Tone FFT at F_{IN} = 100 MHz



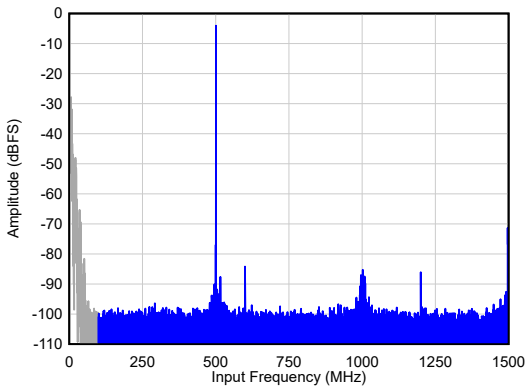
SNR = 61.7 dBFS[1], SFDR = 58 dBc, Non HD23 = 83 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-2. Single Tone FFT at F_{IN} = 100 MHz



SNR = 61.9 dBFS, SFDR = 63 dBc, Non HD23 = 77 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-3. Single Tone FFT at F_{IN} = 500 MHz



SNR = 61.8 dBFS[1], SFDR = 68 dBc, Non HD23 = 84 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-4. Single Tone FFT at F_{IN} = 500 MHz

[1] Measured from 100 MHz to F_S/2

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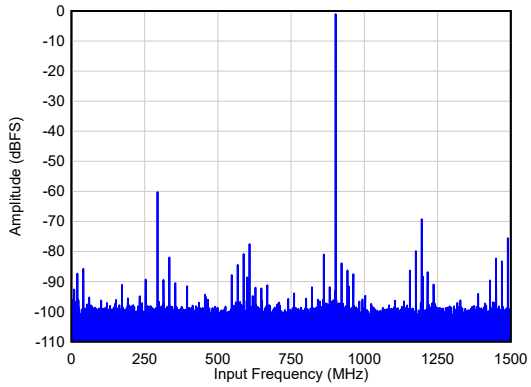
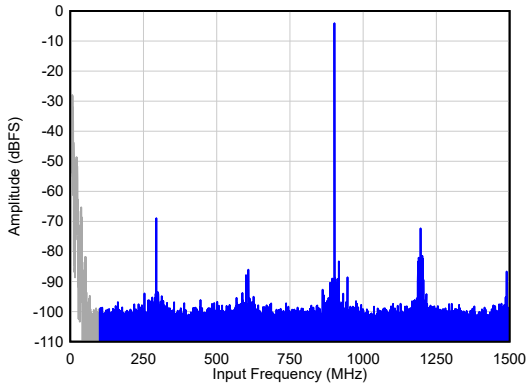
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



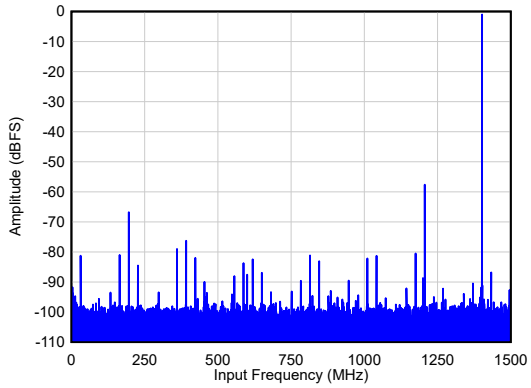
SNR = 61.8 dBFS, SFDR = 60 dBc, Non HD23 = 76 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-5. Single Tone FFT at F_{IN} = 900 MHz



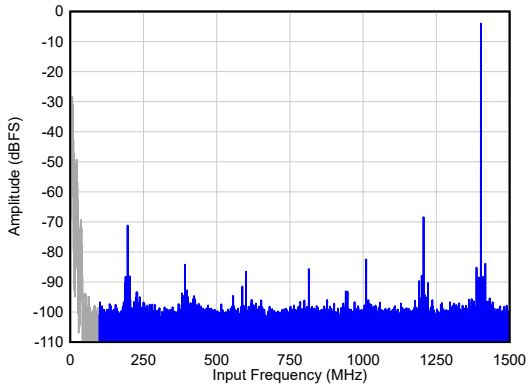
SNR = 60.9 dBFS[1], SFDR = 64 dBc, Non HD23 = 82 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-6. Single Tone FFT at F_{IN} = 900 MHz



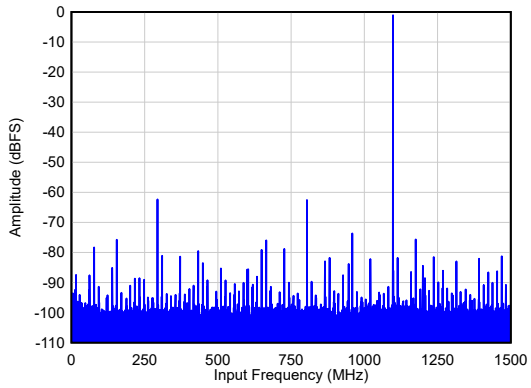
SNR = 62.1 dBFS, SFDR = 57 dBc, Non HD23 = 76 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-7. Single Tone FFT at F_{IN} = 1400 MHz



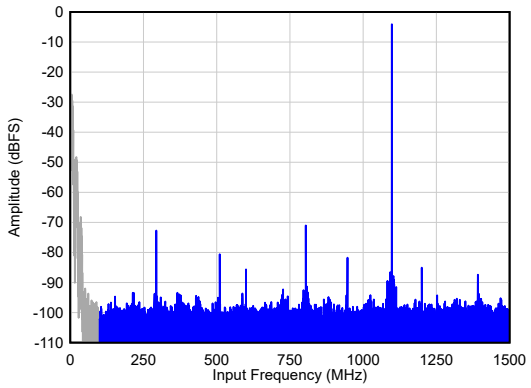
SNR = 62.2 dBFS[1], SFDR = 63 dBc, Non HD23 = 83 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-8. Single Tone FFT at F_{IN} = 1400 MHz



SNR = 60.9 dBFS, SFDR = 62 dBc, Non HD23 = 74 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-9. Single Tone FFT at F_{IN} = 1900 MHz



SNR = 61.2 dBFS[1], SFDR = 67 dBc, Non HD23 = 80 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-10. Single Tone FFT at F_{IN} = 1900 MHz

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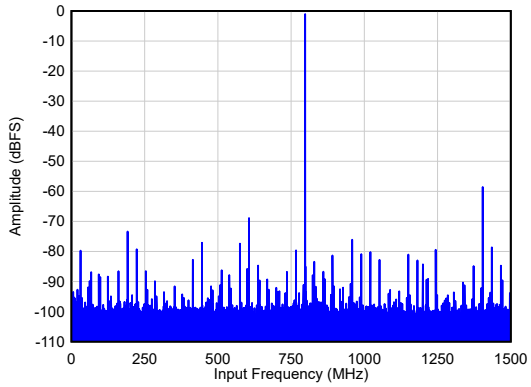
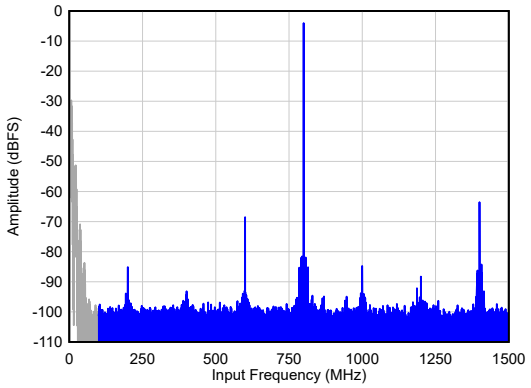
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



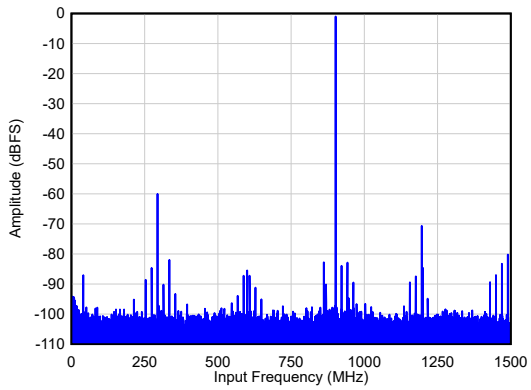
SNR = 60.4 dBFS, SFDR = 58 dBc, Non HD23 = 73 dBFS
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-11. Single Tone FFT at F_{IN} = 2200 MHz



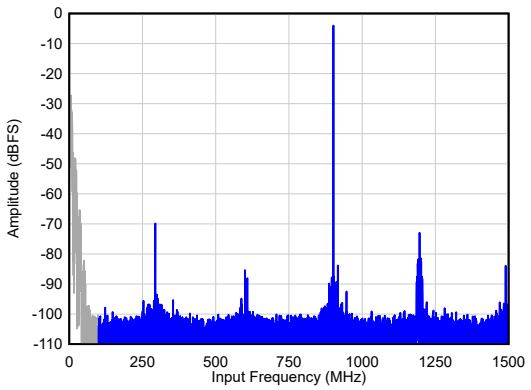
SNR = 61.1 dBFS[1], SFDR = 60 dBc, Non HD23 = 82 dBFS
A_{IN} = -4 dBFS, 1x AVG, Dither = EN

図 5-12. Single Tone FFT at F_{IN} = 2200 MHz



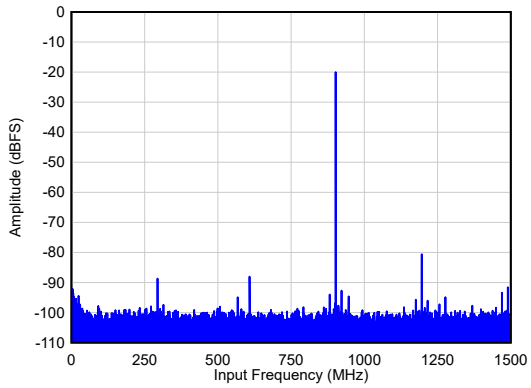
SNR = 63.5 dBFS, SFDR = 59 dBc, Non HD23 = 80 dBFS
A_{IN} = -1 dBFS, 2x AVG, Dither = DIS

図 5-13. Single Tone FFT at F_{IN} = 900 MHz



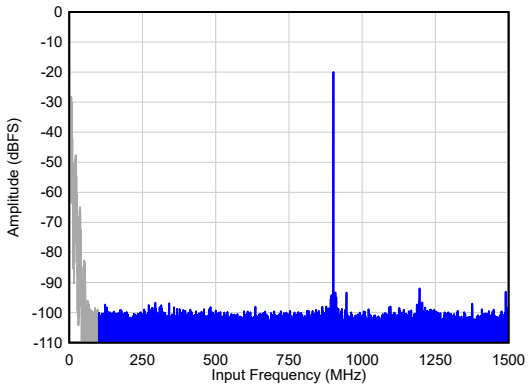
SNR = 62.3 dBFS[1], SFDR = 66 dBc, Non HD23 = 82 dBFS
A_{IN} = -4 dBFS, 2x AVG, Dither = EN

図 5-14. Single Tone FFT at F_{IN} = 900 MHz



SNR = 63.9 dBFS, SFDR = 60 dBc, Non HD23 = 87 dBFS
A_{IN} = -20 dBFS, 1x AVG, Dither = DIS

図 5-15. Single Tone FFT at F_{IN} = 900 MHz



SNR = 63.4 dBFS[1], SFDR = 73 dBc, Non HD23 = 92 dBFS
A_{IN} = -20 dBFS, 1x AVG, Dither = EN

図 5-16. Single Tone FFT at F_{IN} = 900 MHz

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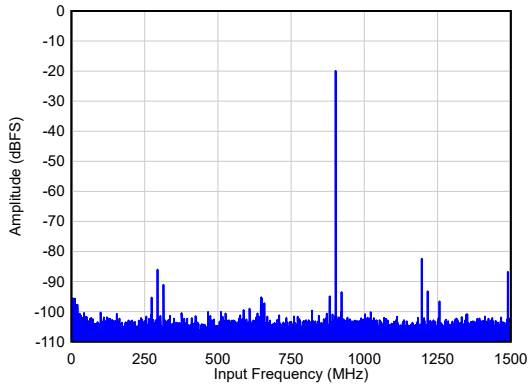
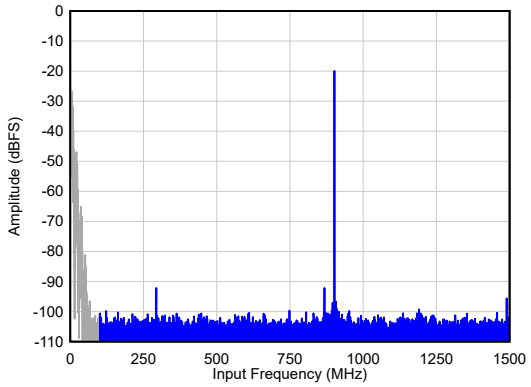
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



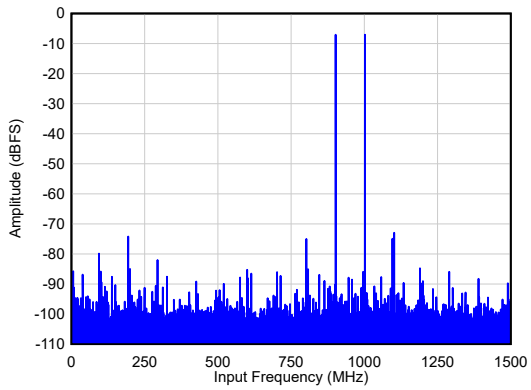
SNR = 66.4 dBFS, SFDR = 63 dBc, Non HD23 = 86 dBFS
A_{IN} = -20 dBFS, 2x AVG, Dither = DIS

図 5-17. Single Tone FFT at F_{IN} = 900 MHz



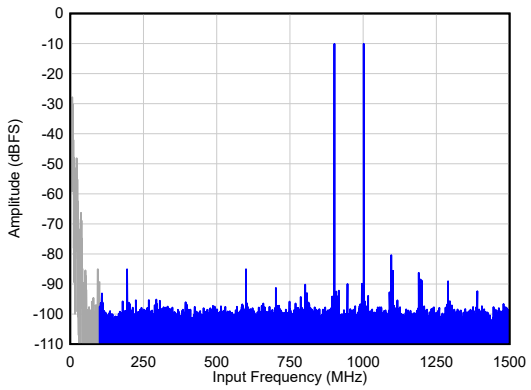
SNR = 65.5 dBFS[1], SFDR = 73 dBc, Non HD23 = 95 dBFS
A_{IN} = -20 dBFS, 2x AVG, Dither = EN

図 5-18. Single Tone FFT at F_{IN} = 900 MHz



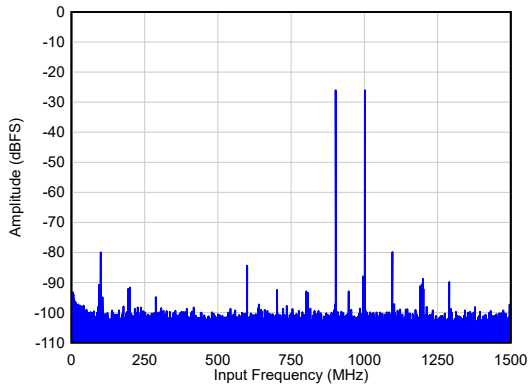
IMD3 = 68 dBc
A_{IN} = -7 dBFS/tone, 1x AVG, Dither = DIS

図 5-19. Two Tone FFT at F_{IN} = 900/1000 MHz



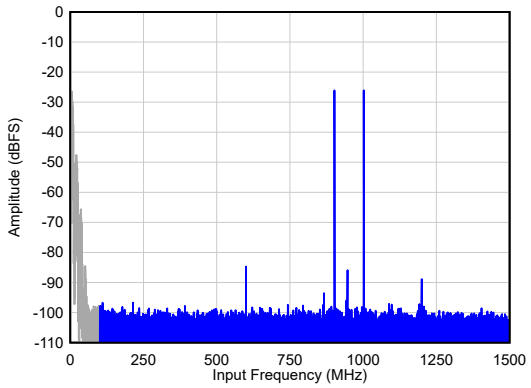
IMD3 = 70 dBc
A_{IN} = -10 dBFS/tone, 1x AVG, Dither = EN

図 5-20. Two Tone FFT at F_{IN} = 900/1000 MHz



IMD3 = 54 dBc
A_{IN} = -26 dBFS/tone, 1x AVG, Dither = DIS

図 5-21. Two Tone FFT at F_{IN} = 900/1000 MHz



IMD3 = 71 dBc
A_{IN} = -26 dBFS/tone, 1x AVG, Dither = EN

図 5-22. Two Tone FFT at F_{IN} = 900/1000 MHz

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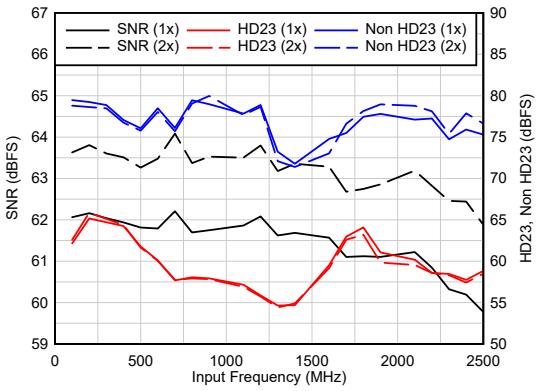
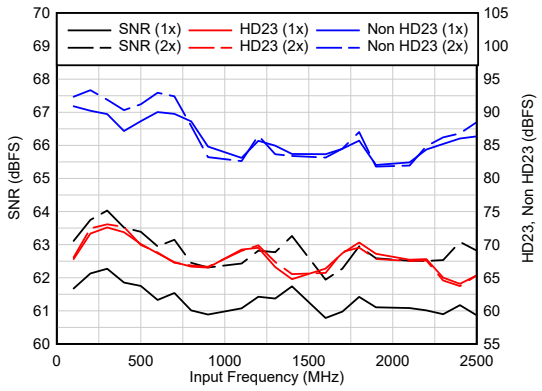
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



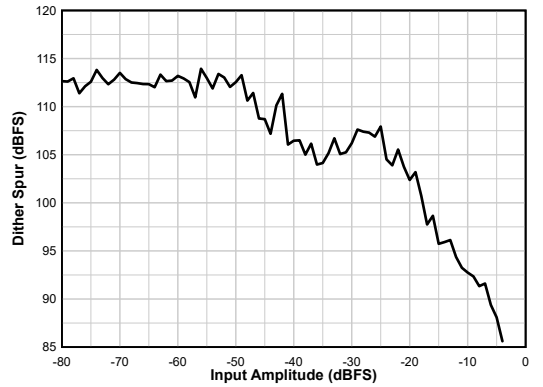
A_{IN} = -1 dBFS, Dither = DIS

図 5-23. AC Performance vs F_{IN}



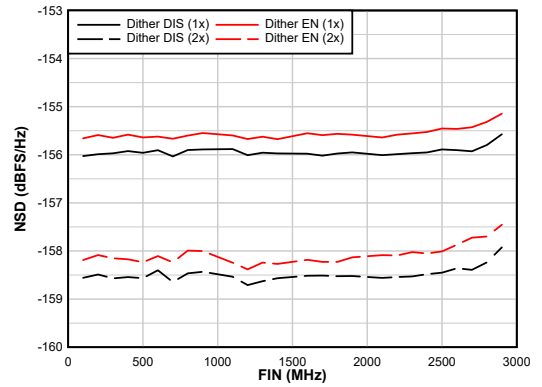
A_{IN} = -4 dBFS, Dither = EN

図 5-24. AC Performance vs F_{IN}



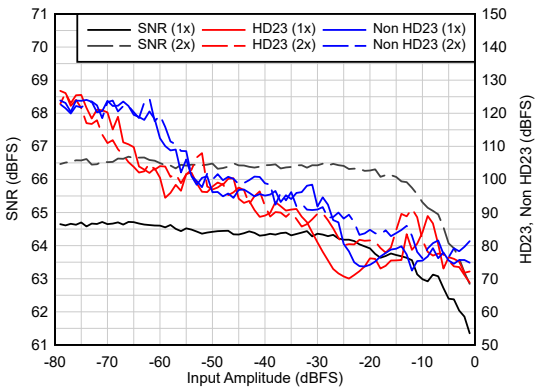
F_{IN} = 900 MHz,

図 5-25. Dither Spur vs A_{IN}



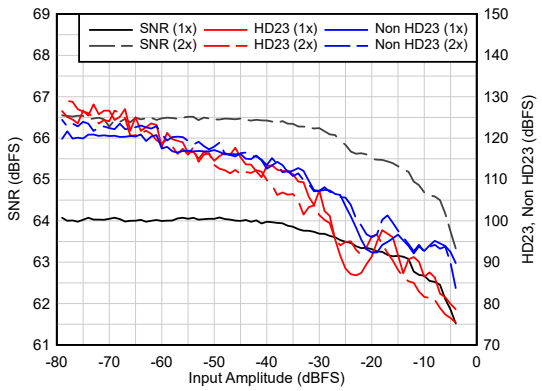
A_{IN} = -20 dBFS

図 5-26. NSD Performance vs F_{IN}



F_{IN} = 900 MHz, Dither = DIS

図 5-27. AC Performance vs A_{IN}



F_{IN} = 900 MHz, Dither = EN

図 5-28. AC Performance vs A_{IN}

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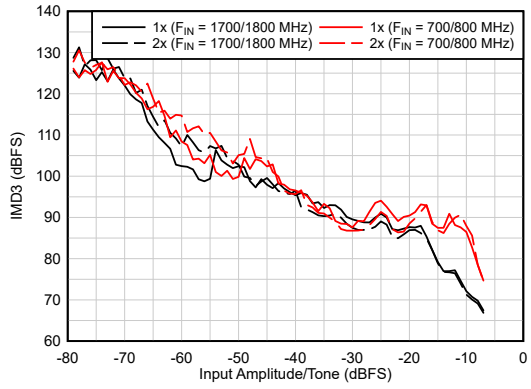
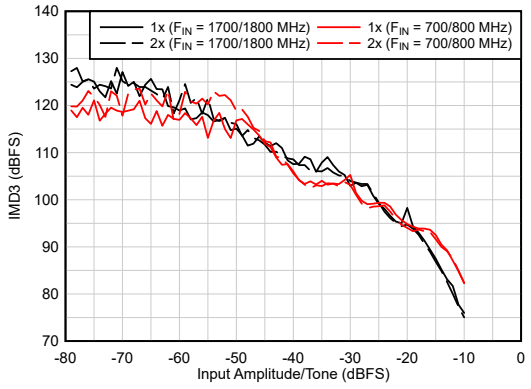
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



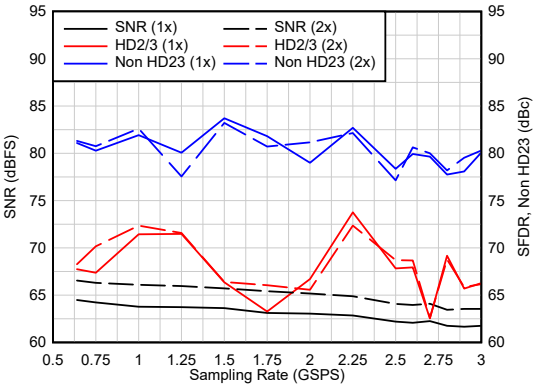
Dither = DIS

図 5-29. IMD3 Performance vs A_{IN}



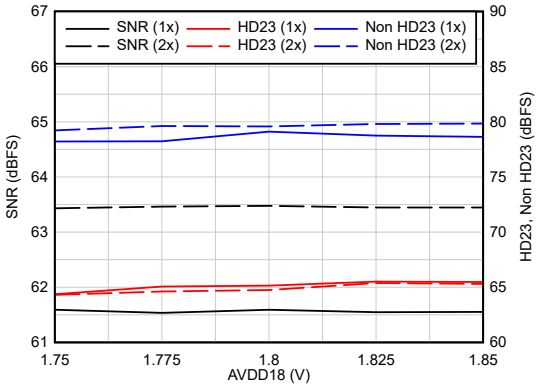
Dither = EN

図 5-30. IMD3 Performance vs A_{IN}



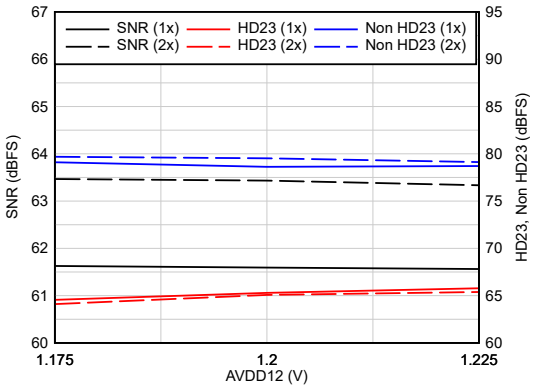
F_{IN} = 900 MHz, A_{IN} = -1 dBFS, Dither = DIS

図 5-31. AC Performance vs F_S



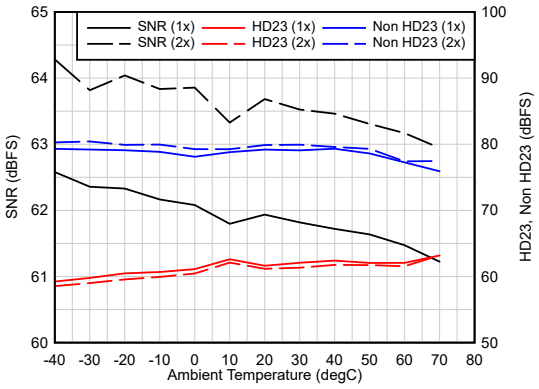
F_{IN} = 900 MHz, A_{IN} = -1 dBFS, Dither = DIS, Other supplies nominal

図 5-32. AC Performance vs AVDD18



F_{IN} = 900 MHz, A_{IN} = -1 dBFS, Dither = DIS, Other supplies nominal

図 5-33. AC Performance vs AVDD12



F_{IN} = 900 MHz, A_{IN} = -1 dBFS, Dither = DIS

図 5-34. AC Performance vs Temperature

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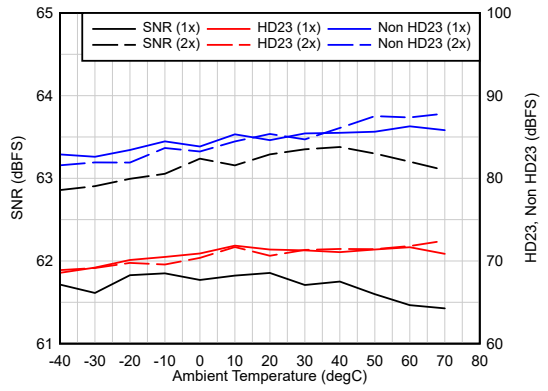
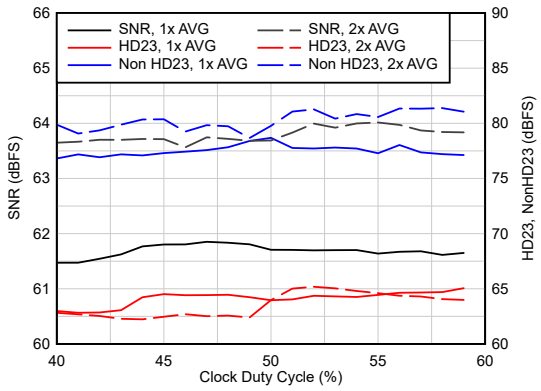
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



F_{IN} = 900 MHz, A_{IN} = -4 dBFS, Dither = EN

図 5-35. AC Performance vs Temperature



F_{IN} = 900 MHz, A_{IN} = -1 dBFS, Dither = DIS

図 5-36. AC Performance vs Clock Duty Cycle

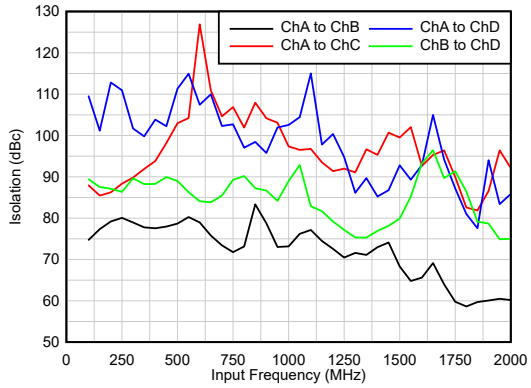
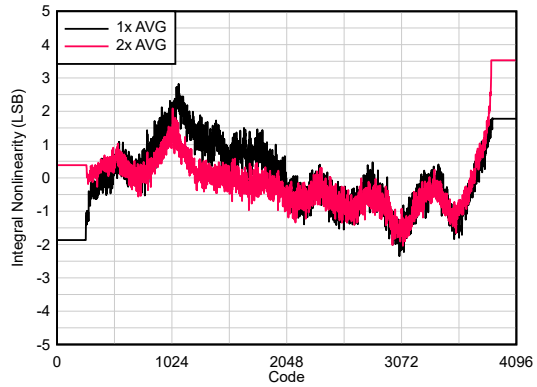
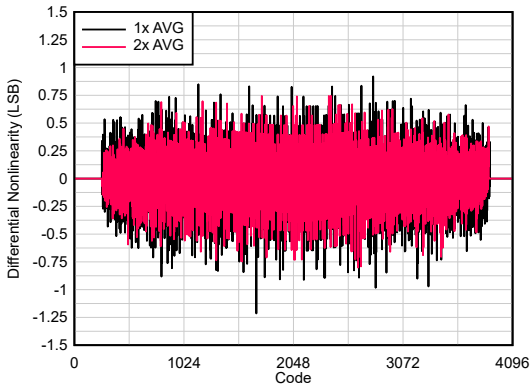


図 5-37. Isolation vs Input Frequency



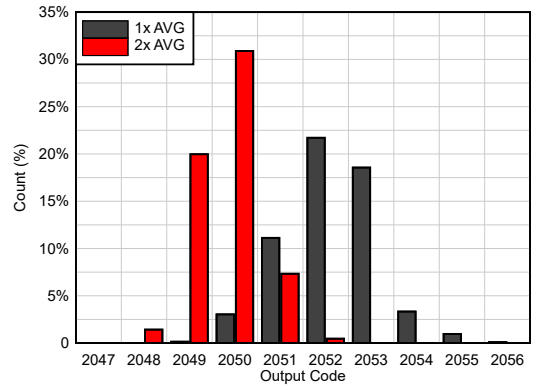
F_{IN} = 900 MHz, Dither = DIS

図 5-38. INL vs Code



F_{IN} = 900 MHz, Dither = DIS

図 5-39. DNL vs Code

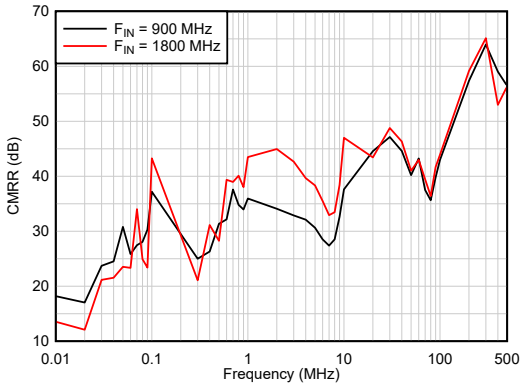


Dither = DIS

図 5-40. DC Offset Histogram

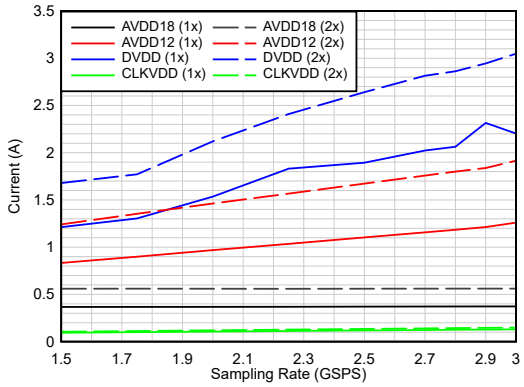
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



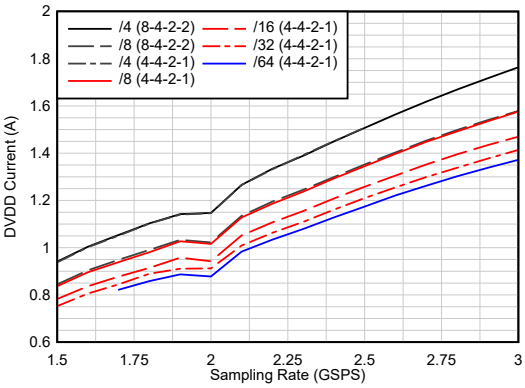
A_{IN} = -1 dBFS, 1x AVG, Dither = DIS

図 5-41. CMRR



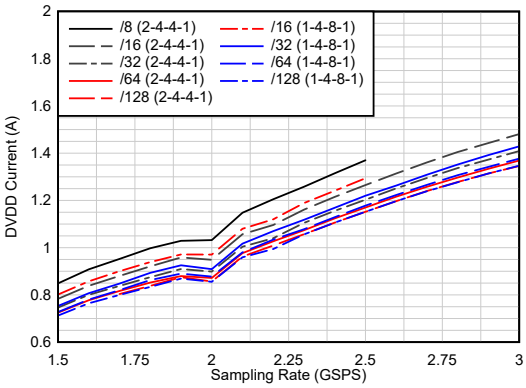
A_{IN} = -1 dBFS, Dither = DIS, DDC Bypass

図 5-42. Current vs Sampling Rate vs Averaging



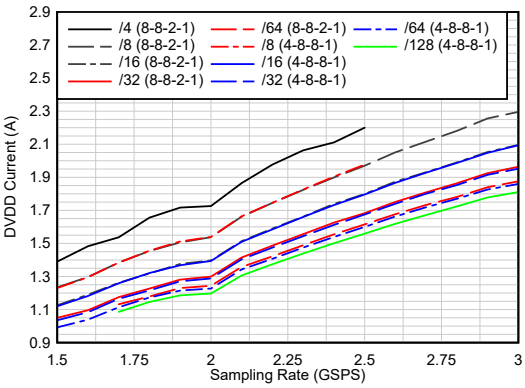
A_{IN} = -1 dBFS, 1x AVG

図 5-43. Current vs Sampling Rate vs Real Decimation



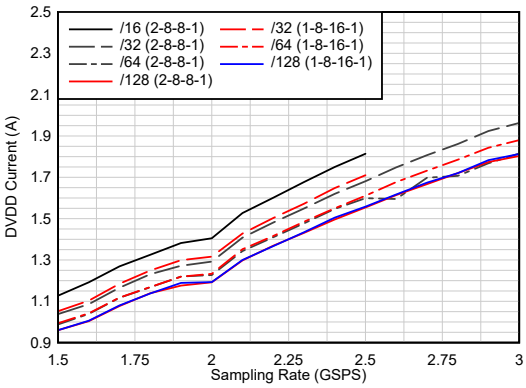
A_{IN} = -1 dBFS, 1x AVG

図 5-44. Current vs Sampling Rate vs Real Decimation



A_{IN} = -1 dBFS, 1x AVG
Single Band Decimation

図 5-45. Current vs Sampling Rate vs Complex Decimation



A_{IN} = -1 dBFS, 1x AVG
Single Band Decimation

図 5-46. Current vs Sampling Rate vs Complex Decimation

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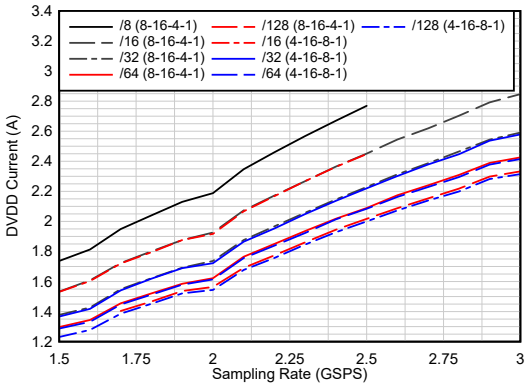
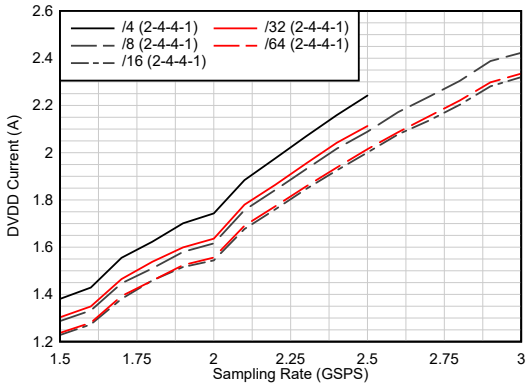
5.10 Typical Characteristics (continued)

Typical values are at T_A = 25°C, ADC sampling rate = 3 GSPS, DDC BYPASS mode (characterization mode only and not supported operating mode to illustrate RAW ADC performance prior decimation), 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted.



A_{IN} = -1 dBFS, 1x AVG
Dual Band Decimation

図 5-47. Current vs Sampling Rate vs Complex Decimation



A_{IN} = -1 dBFS, 1x AVG
Dual Band Decimation

図 5-48. Current vs Sampling Rate vs Complex Decimation

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6 Detailed Description

6.1 Overview

The ADC34RF55 is a single core (non-interleaved) 14-bit, 3 GSPS, quad channel analog to digital converter (ADC). The design maximizes signal-to-noise ratio (SNR) and delivers a noise spectral density of -155 dBFS/Hz. Additional internal ADCs can be used for on-chip averaging to further improve the noise density to as low as -157 dBFS/Hz.

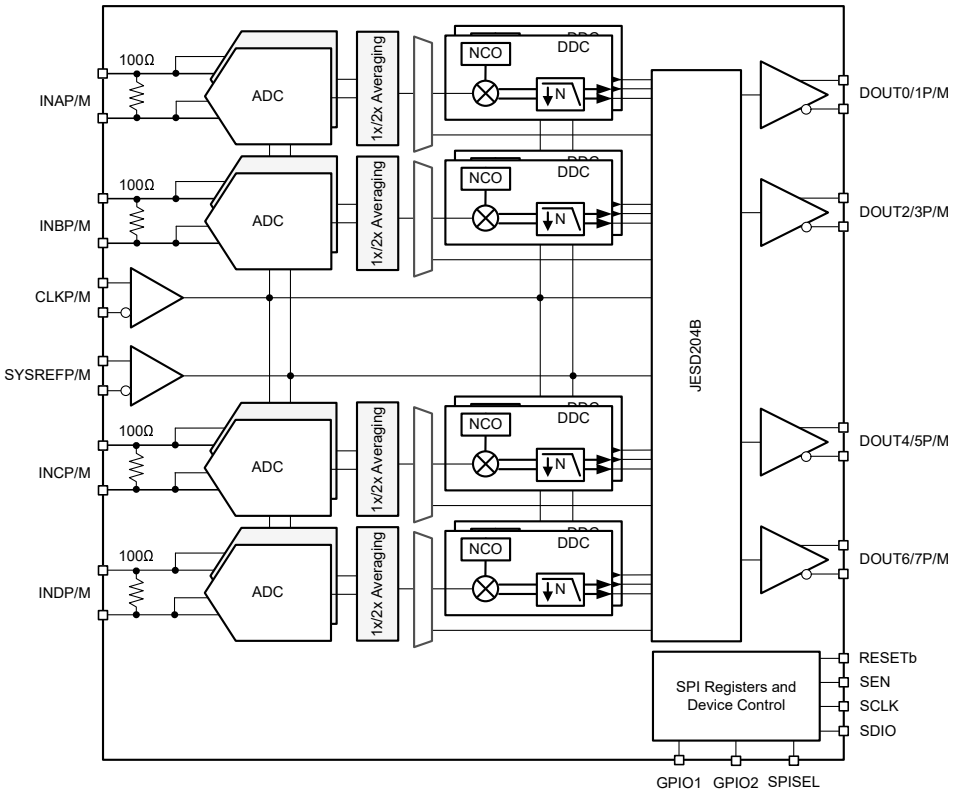
The analog signal input is non-buffered to save power consumption with a nominal differential input impedance of 100 Ω. The full power input bandwidth is 2.7 GHz (-3 dB) and the device supports direct RF sampling with input frequencies in the L- and S-band. The ADC34RF55 is designed for low residual phase noise to support high performance radar applications. The sampling clock input has a dedicated power supply input which requires a clean power supply.

Each ADC channel can be connected to a dual-band digital down-converter (DDC) using a 48-bit NCO which supports phase coherent frequency hopping. Using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1 us. The digital down converters support a wide range of instantaneous bandwidth (IBW) coverage - from single wide band mode with 8x complex decimation to up to two narrow bandwidth channels with as high as 128x complex decimation.

The ADC34RF55 supports the JESD204B serial data interface with subclass 1 deterministic latency using data rates up to 13 GBPS. In bypass mode, 14-bit output is supported up to a sampling rate of 1.3 GSPS. From 1.3 to 1.5 GSPS a 12-bit interface with more efficient data packing can be used at expense of quantization noise. With sampling rates from 1.5 to 3 GSPS, on-chip decimation has to be used with 16-bit output format.

The power efficient ADC architecture consumes 1.1 W/ch at maximum sampling rate and provides power scaling with lower sampling rates.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Analog Inputs

The ADC34RF55 provides up to two internal ADCs per channel for purpose of averaging to improve the noise performance. Two ADCs internally are connected to the same differential input pins as shown in the equivalent input schematic (see 図 6-1). The analog inputs have a differential 100 Ω split termination with internal biasing. When only a single ADC is used, there is a minor parasitic capacitance remaining from the unused ADC.

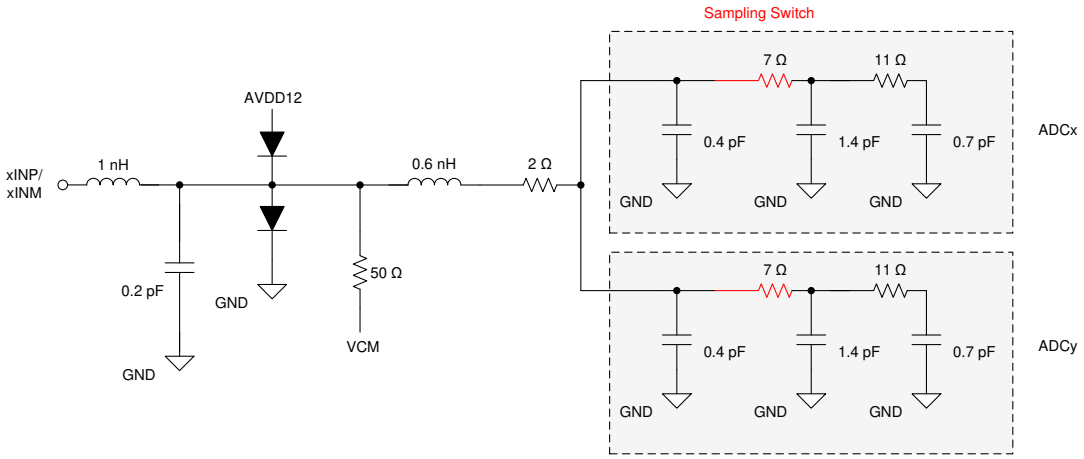

図 6-1. Equivalent input schematic

6.3.1.1 Input Bandwidth and Full-Scale

The input bandwidth (-3 dB) and input fullscale are dependent on what input termination and averaging mode are chosen as shown in the summary in 表 6-1. The bandwidth can be increased by changing the input termination to 50 Ω differential.

表 6-1. Digital averaging vs Full Power Input Bandwidth (–3 dB)

No. of ADCs averaged	ADC inputs used for averaging	Input Bandwidth (-3 dB)	Selected differential input termination	Input Full-scale
Default	INx1	2.75 GHz	100 Ω	+ 2 dBm
2	INx1	2.75 GHz	100 Ω	+ 3.5 dBm

The full power input bandwidth plots with input RESET switch disabled (RSW0) and enabled (RSW1) are shown in 図 6-2.

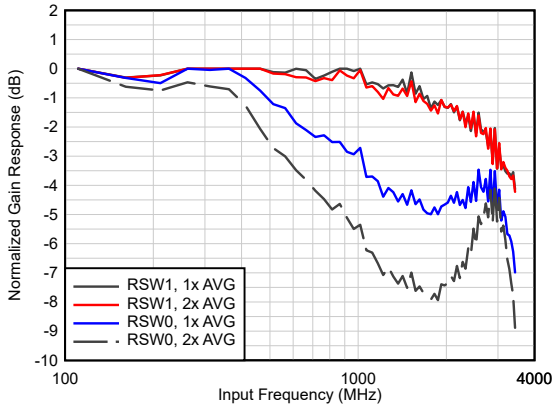

図 6-2. Input Bandwidth - Reset switch DIS

The RESET switch is enabled by default and can be disabled with the following register writes:

表 6-2. Register Write Example for Configuring the RESET Switch

ADDR	DATA	DESCRIPTION
0x05	0x40	Select ANALOG page
0x6D	0xC0	Disable RESET Switch (to enable: 0x00)
0x6E	0x08	Disable RESET Switch (to enable: 0x00)

6.3.1.2 Input Imbalance

The AC performance is sensitive to amplitude and phase imbalance of the analog inputs, as shown in 図 6-3 and 図 6-4 for 1x and 2x internal averaging (F_S = 2.6 GSPS, F_{IN} = 0.9 GHz, A_{IN} = -1 dBFS, dither = DIS) and 図 6-5 and 図 6-6 (F_S = 3.0 GSPS, F_{IN} = 0.9 GHz, A_{IN} = -1 dBFS, dither = DIS).

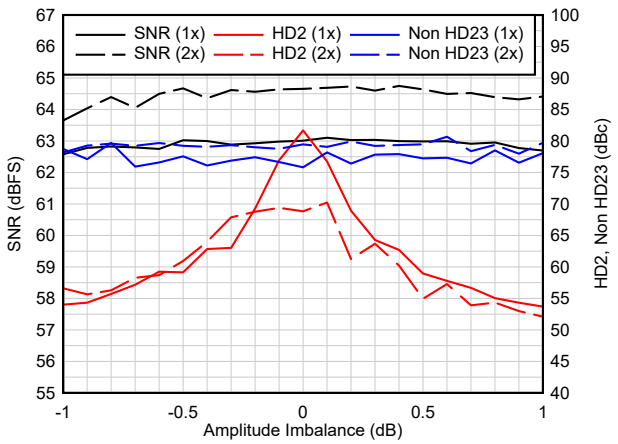

図 6-3. Amplitude Imbalance - 2.6 GSPS

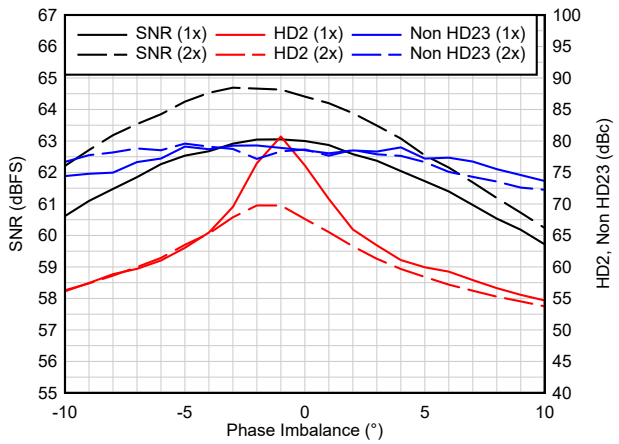

図 6-4. Phase Imbalance - 2.6 GSPS

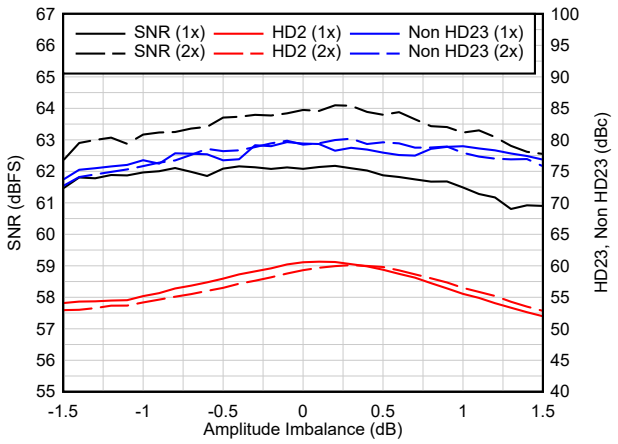

図 6-5. Amplitude Imbalance - 3.0 GSPS

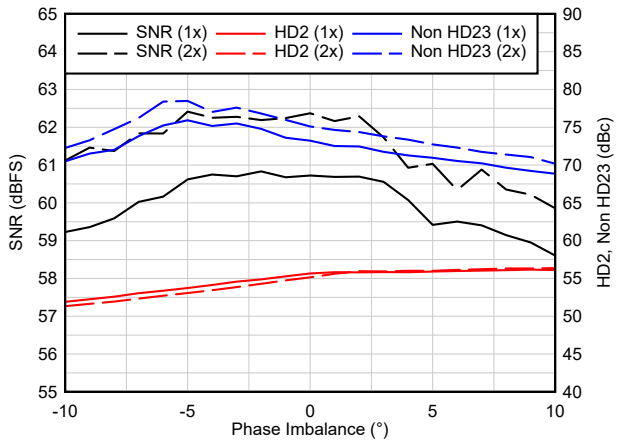

図 6-6. Phase Imbalance - 3.0 GSPS

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6.3.1.3 Over Range Indication

The ADC provides two options (configured using SPI) to indicate if input full scale over range occurred:

- Fast Over range on GPIO1/2 pins: indication is available after approximately 6 clock cycles and the over range indication flag stays high (sticky) until it is cleared via SPI register writes. The over range indicator on GPIO1 is chA and chB OR-ed together while GPIO2 gives OVR for chC and chD OR-ed together.
- Over range embedded in JESD stream: in this configuration the over range indicator is given on the JESD output data stream and replaces the LSB of the output data of the corresponding channel. The indicator is output ahead of the data and is updated every clock cycle.

表 6-3. JESD OVR Latency

Decimation	No. of Bands	OVR Latency (incl JESD, in sampling clock cycles)
DDC Bypass	-	140-144
8	Single (real and complex), dual	44
16	Single (real and complex), dual	80
32	Single (real and complex), dual	152
64	Single (real and complex), dual	296
128	Single (real and complex), dual	584

The overrange output flag (GPIO or JESD) is the output of individual over range flags all ADCs per channel being used. For example, in non-averaged mode the over range indication per channel is for a single ADC while in 2x average mode the over range flag of both ADC cores are OR-ed together. 表 6-4 shows how to configure the OVR using SPI registers.

表 6-4. Programming example to configure the OVR to GPIO or JESD

ADDR	DATA	DESCRIPTION	ADDR	DATA	DESCRIPTION
OVRA/B on GPIO1 and OVRC/DGPIO2, OVR sticky			OVR on JESD		
0x05	0x02	Select DIGITAL page	0x05	0x02	Select DIGITAL page
0x238	0xF0		0x2E	D0	Set D0 = 1 to enable OVR on JESD
0x383	0x02	Enables OVR on GPIO pins	0x05	0x00	
Clear OVR			These extra writes are only needed using decimation		
0x05	0x40	Select ANALOG page	0x05	0x18	Select DDCAB & DDCCD page
0x74	0x04	Clear OVR flag chA/B	0x20	0x06	Enable OVR on JESD
0x74	0x00				
0x84	0x04	Clear OVR flag chC/D			
0x84	0x00				
Change OVR from sticky to non sticky (self clear)					
0x05	0x40	Select ANALOG page			
0x31	0x06	Set OVR to non-sticky			

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6.3.1.4 Analog out-of-band dither

The ADC34RF55 provides optional (enabled via SPI writes) analog out-of-band, large amplitude dither. It has a bandwidth of approximately 20 MHz located at DC and an adjustable amplitude with a maximum dither power of approximately -20 dBFS (PAR ~ 9 dB). The dither is completely rolled-off into the noise floor within approximately 100 MHz as illustrated in 図 6-7. Since the dither is large, the amplitude is recommended for the signal input not to exceed -2.5 dBFS to avoid input saturation. The dither signal also couples to the input signal and, depending on input frequency, can degrade the close in phase noise for offsets > 1 MHz.

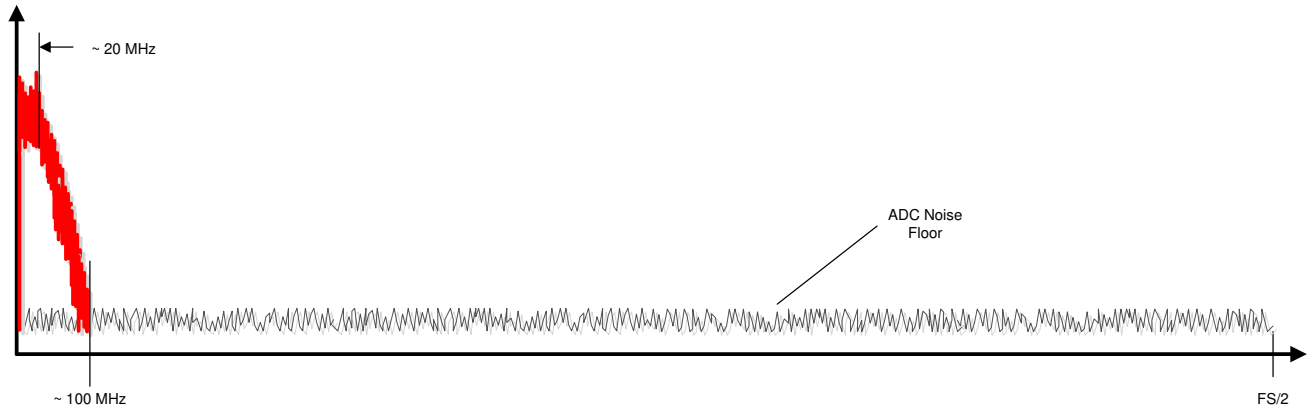

図 6-7. Analog out-of-band dither

In the frequency domain, the dither signal shows up in individual tones as shown in 図 6-8. The dither update frequency can be adjusted with the dither divider setting. The dither update frequency is: F_S / 4 / 2047 / 'Dither Divider'. In the frequency spectrum, there is a 2 larger dither spurs at F_{IN} +/- F_S / 4 / 'Dither Divider'.

By default, the divider is set to 50, which translates to a dither spur spacing of approximately 7 kHz. A divider setting of 32 translates to a dither spacing of approximately 11 kHz as shown in 図 6-9. The lower the divider setting, the higher the dither tone frequency. 図 6-9 also shows that the dither energy reduces as the offset frequency increases. Less dither energy reduces the higher harmonic spur improvement.

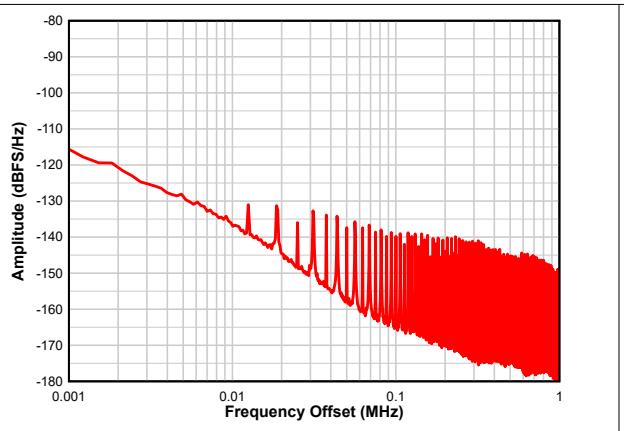

図 6-8. Dither Close-Up

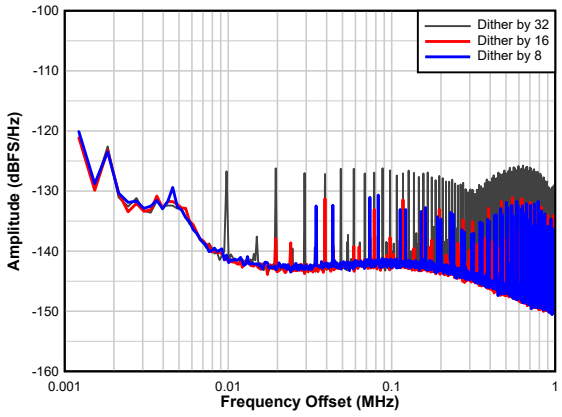

図 6-9. Dither vs Dither Divider Setting

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The analog dither must be enabled in multiple locations. The different dither amplitudes must be used based on the internal averaging as shown in 表 6-6.

表 6-5. Recommended dither amplitude settings

Mode	Amplitude	Dither Amp1	Dither Amp2
1x AVG	±1024 codes	0	0
1x AVG	±768 codes	0	-4
2x AVG	±1024 codes	3	0
2x AVG	±768 codes	0	0

The internal analog dither can be enabled via the following register writes. After enabling the dither (or changing the dither amplitude) another calibration needs to be performed. See 表 6-6.

表 6-6. Register write example for configuring the internal dither

ADDR	DATA	DESCRIPTION	ADDR	DATA	DESCRIPTION
0x05	0x40	Select ANALOG page	0xB1	0x00	Sets dither divider. 0x00 = /50
0xA8	0x00	DITHER AMP1: 3 = 0x80, 0 = 0x00	0xB2	0x00	
0xCD	0x00	DITHER AMP2: -4 = 0x40, 0 = 0x00	0xAF	0x18	
0x05	0x00		0xAF	0x10	0x10 = dither ENABLED, 0x90 = dither DISABLED
0x04	0x01		0x04	0x01	
0x20	0x04		0x20	0x00	
0x91	0x40		0x04	0x00	
0xAF	0x10				

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6.3.2 Sampling Clock Input

The internal sampling clock path is designed for the lowest residual phase noise contribution. The sampling clock circuitry requires a dedicated low noise power supply for best performance. The internal residual clock phase noise is also sensitive to clock amplitude. For best performance, the clock amplitude must be larger than 1 V_{PP}. The phase noise improves by 3 dB per 2x averaging; however, at higher input frequencies the clock path contribution reduces the improvement.

表 6-7. Internal Aperture Clock Phase Noise (F_S = 3 Gsps, V_{IN} = 1 V_{PP})

Frequency Offset (MHz)	Amplitude (dBc/Hz)
0.001	-117
0.01	-127
0.1	-137
1	-147
10	-154
250	-160

The clock input and ADC sampling circuitry have an amplitude noise component which modulates on to the sampled input signal. Unlike phase noise, the amplitude noise does not scale with input frequency. Amplitude noise is only affected by the sampling reset switch as shown in 図 6-10 and 図 6-11. This noise component can dominate the close in noise performance at lower input frequencies.

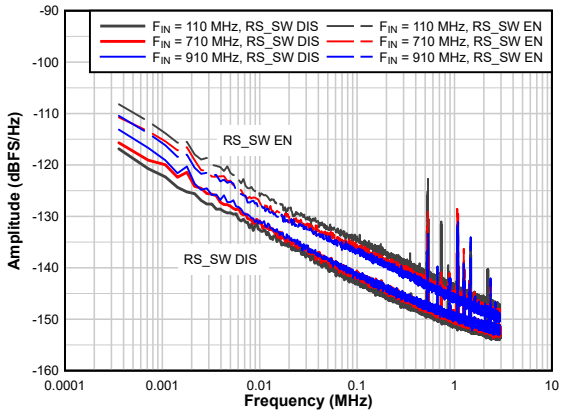

図 6-10. Amplitude Noise vs Input Frequency

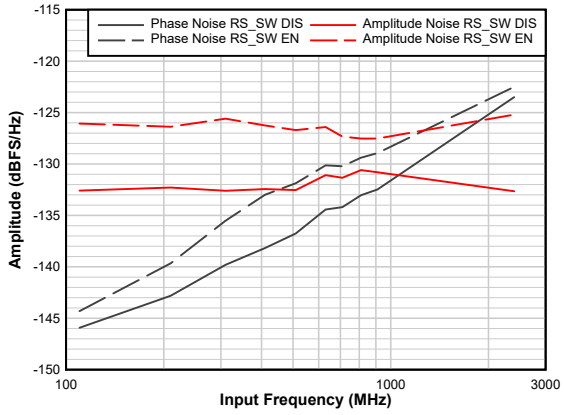

図 6-11. Amplitude and Phase noise at 10 kHz offset vs Input Frequency

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The internal aperture jitter is also dependent on the amplitude of the external clock input signal. 図 6-12 and 図 6-13 show the expected SNR performance with dither on/off across clock amplitude (F_S = 2.6 GSPS).

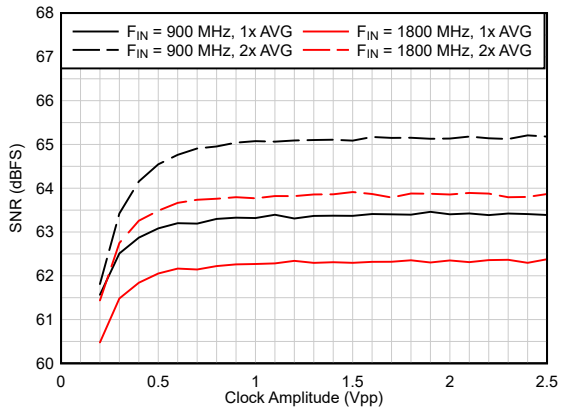

図 6-12. SNR vs Clock Amplitude (Dither OFF)

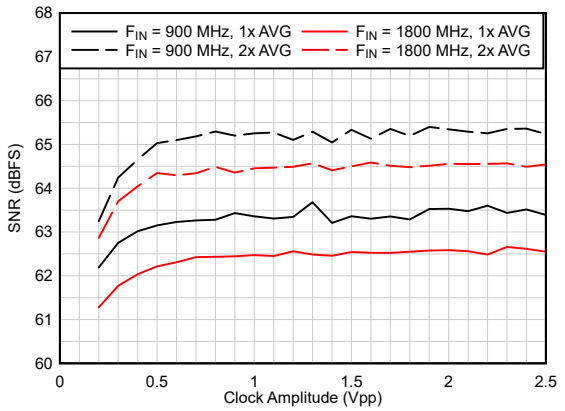

図 6-13. SNR vs Clock Amplitude (Dither ON)

The sampling clock input is internally terminated to 100 Ω differentially and provides a return loss better than 10 dB (see 図 6-14). The clock input consists of a single clock input buffer followed by a dedicated clock buffer for ADCA/B as well as ADCC/D. When averaging two ADCs internally, there is some decrease in clock buffer noise which is correlated and does not improve with averaging.

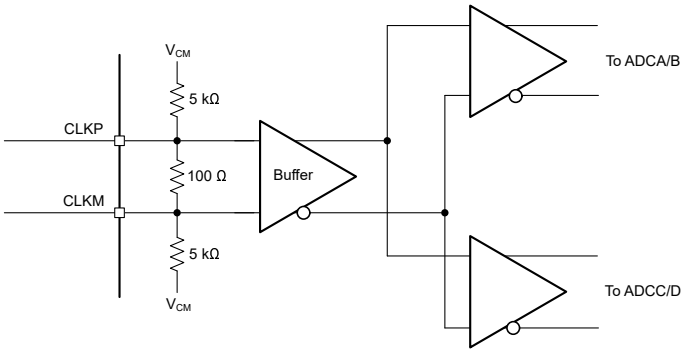

図 6-14. Clock Input Internal Circuitry

6.3.3 ADC Foreground Calibration

The internal ADC architecture is sensitive to temperature changes. The ADC34RF55 contains two additional internal ADC cores (one for channel A/B and one for channel C/D) which are used when one of the ADCs is in calibration. ADCs are calibrated as pairs where one ADC at a time is connected to the internal calibration DAC. The calibration is configured via SPI register writes and is executed using SPI register writes or using the GPIO1 pin. When executed, the calibration takes approximately 23 ms x 3 GSPS / F_S per ADC pair (approximately 11.5 ms x 3 GSPS / F_S per ADC). The example in 図 6-15 shows 2x internal averaging where 4 ADC cores (#1,2,3,4 for chA/B and #6,7,8,9 for chC/D) are used in operation and ADCs #5 and #10 for calibration.

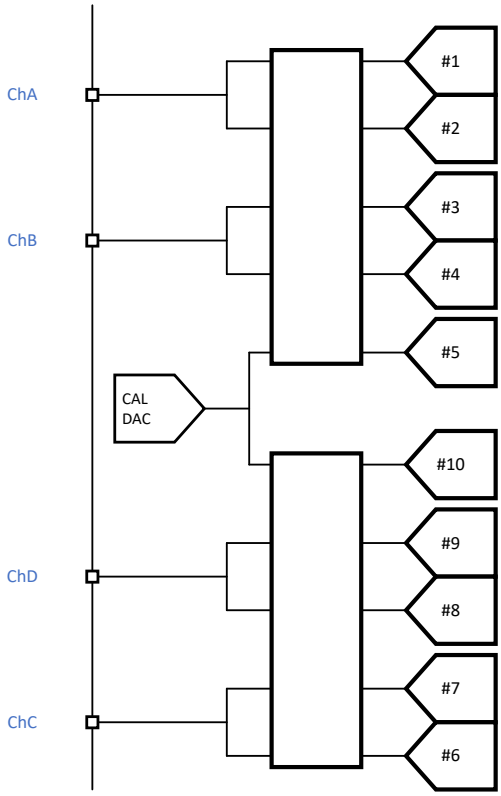

図 6-15. Internal ADC setup for 2x averaging mode

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6.3.3.1 Calibration Control

図 6-16 shows a timing diagram of the calibration control using GPIO1 pin.

When GPIO1 transitions to LOW logic state:

- an ADC pair gets swapped out within approximately 120 ns
- a new calibration gets triggered immediately

If GPIO1 is being held low when the calibration of an ADC pair is completed, the next ADC pair is switched and a new calibration is triggered. The order in which ADC pair gets calibrated can be configured via SPI to serial or random.

When using 2x averaging for example, the calibration must be executed for 5 ADC pairs to make sure all ADCs in use have been calibrated recently.

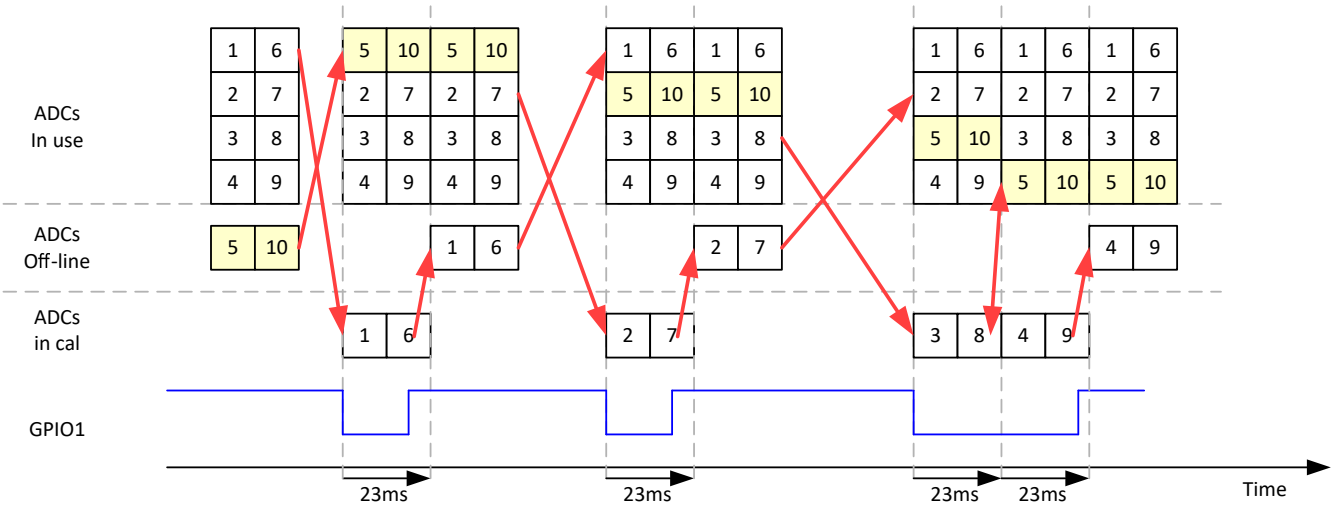

図 6-16. Timing diagram - calibration (2x AVG example)

図 6-17 shows the ADC switch happens approximate 120 ns after the logic level change on GPIO1 is detected.

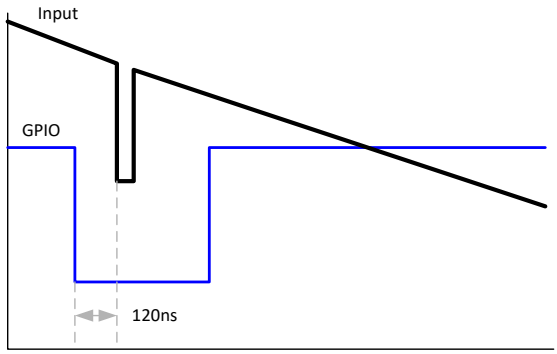

図 6-17. Timing diagram shows the ADC switch

6.3.3.2 ADC Switch

During the ADC transition, the amplitude drops for 1-2 samples as shown in 図 6-18. The gain variation from one ADC to the next is ~ < 0.05 dB while the phase change is less 0.01 deg as shown in 図 6-19.

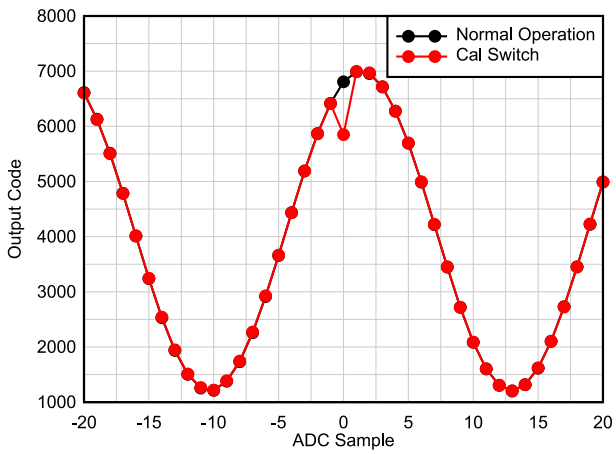

図 6-18. Output Code vs ADC Sample

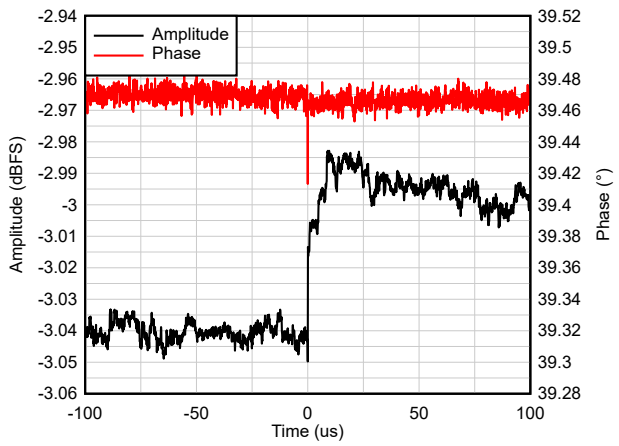

図 6-19. Amplitude and Phase vs Time

6.3.3.3 Calibration Configuration

The ADC34RF55 provides 3 different options to configure the internal foreground calibration:

- Calibrate all ADCs one time using SPI trigger (after initial power up or during operation) - see 表 6-8
- Continuous calibration - see 表 6-9
- Calibrate 2 ADCs at a time using GPIO trigger - see 表 6-10

The status of the calibration can be read back from register 0x298 (CALIBRATION page). Successful calibration reads back 0x0E on the 4 LSB of that register.

表 6-8. Register Writes for power up calibration or SINGLE calibration of all ADCs Using SPI

ADDR	DATA	DESCRIPTION
0x05	0x20	Select CALIBRATION page
0x46	0x02	
0x45	0x8A	Toggle calibration start
0x45	0x0A	
wait		1.3 seconds x 3 GSPS / F_S

表 6-9. Register Writes to Trigger CONTINOUS Calibration of all ADCs Using SPI

ADDR	DATA	DESCRIPTION
0x05	0x20	Select CALIBRATION page
0x46	0x03	
0x45	0x0A	

表 6-10. Register Writes to Trigger ADC Pair Calibration Using the GPIO Pin

ADDR	DATA	DESCRIPTION
0x05	0x20	Select CALIBRATION page
0x46	0x02	
0x45	0x4A	
0x05	0x02	Select DIGITAL page
0x234	0x04	Use GPIO1 pin to freeze calibration switch

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6.3.4 SYSREF

The SYSREF input signal is used to reset internal digital blocks and align them to the internal multi-frame clock to achieve deterministic latency subclass 1. The SYSREF input signal can be AC or DC coupled (selected via SPI register option) as shown in 図 6-20. The ADC34RF55 has internal 100-Ω termination for DC coupling and internal biasing when using AC coupling.

A register mask can be used to only give SYSREF to the NCO (see NCO section) in the decimation filter block. Leave all other blocks such as JESD interface unaffected.

When giving a periodic SYSREF signal, the frequency must be a sub-harmonic of the internal local multi-frame clock (LMFC). The LMFC frequency is determined by the selected decimation: frames per multi-frame setting (K), samples per frame (S), and the device sampling frequency (F_S).

表 6-11. LMFC and SYSREF settings for different operating modes

Operating Mode	LMFS Mode	LMFC Clock Frequency	SYSREF Frequency
DDC Bypass Mode	84810	FS / (20 x K)	FS / (N x 20 x K)
	8422	FS / (4 x K)	FS / (N x 4 x K)
Decimation	Various	FS / (D x S x K)	FS / (N x D x S x K)

Where N is an integer value (1, 2, 3...).

After enabling SYSREF input, the internal SYSREF input ignores any incoming SYSREF pulse after the first 16 pulses.

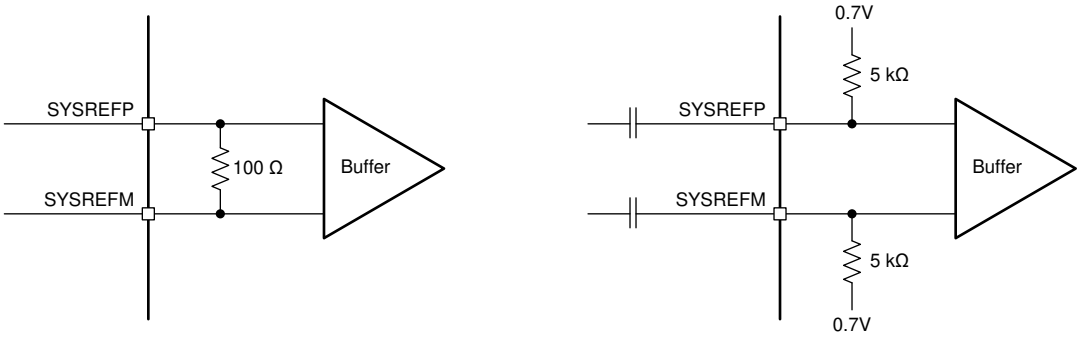

図 6-20. SYSREF Input Circuitry

The internal synchronization using the external SYSREF signal can be enabled with the following register writes.

表 6-12. Register Write Example for Enabling SYSREF Synchronization

ADDR	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x236	0x02	Enable internal SYSREF input and clear SYSREF pulse counter
0x236	0x03	Starts internal SYSREF counter

AC coupling with internal biasing of the SYSREF input can be enabled with the following SPI register writes.

表 6-13. Register Write Example for Enabling SYSREF AC Coupling

ADDR	DATA	DESCRIPTION
0x05	0x40	Select ANALOG page
0xB4	0x01	Enable external AC coupling with internal biasing on SYSREF

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6.3.4.1 SYSREF Capture Detection

The SYSREF input signal rising edge should be edge aligned with the rising edge of the sampling clock to maximize the setup and hold times. The ADC34RF5x includes an internal SYSREF monitoring circuitry to detect possible metastability resulting in a clock cycle slip and thus misalignment across devices.

The sampling clock gets delayed by approximately 160 ps and then captures the SYSREF signal. The SYSREF monitoring circuitry provides insights into SYSREF/clock misalignment by detecting whether SYSREF is leading the clock by up to 50 ps or lagging by up to 48 ps. This circuitry will detect and raise one of the SYSREF XOR flags corresponding to the matching SYSREF window below:

- Window XOR1: SYSREF leading sample clock by 25 to 50 ps
- Window XOR2: SYSREF leading sample clock by up to 25 ps
- Window XOR3: SYSREF lagging sample clock by up to 16 ps
- Window XOR4: SYSREF lagging sample clock by 16 to 32 ps
- Window XOR5: SYSREF lagging sample clock by 32 to 48 ps

The SYSREF monitor registers are not *sticky* registers. They get updated at every rising edge of SYSREF.

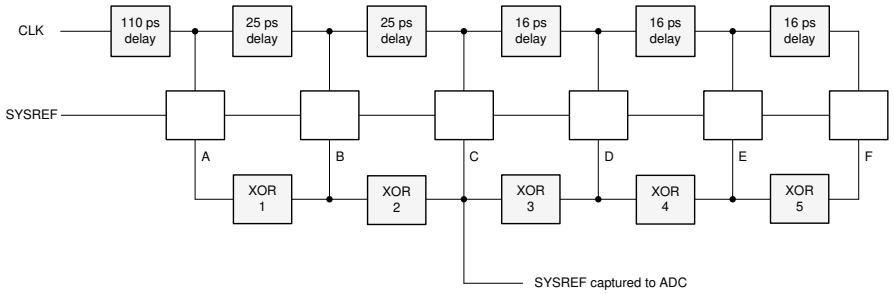

図 6-21. SYSREF Detection Circuitry

The example in 図 6-22 shows a misaligned SYSREF signal where the SYSREF signal arrives much later than the sampling clock rising edge. The SYSREF window feature checks if the SYSREF transition is within ±50 ps of the instant when the SYSREF signal gets captured by the sampling clock. In this example, the delayed SYSREF signal transitions between the "B" and "C" reverse which raises the XOR2 flag. The XOR flags is reported in register 0x22F in the digital page. Register 0x22F then reads back 0x8B, as shown in 表 6-14.

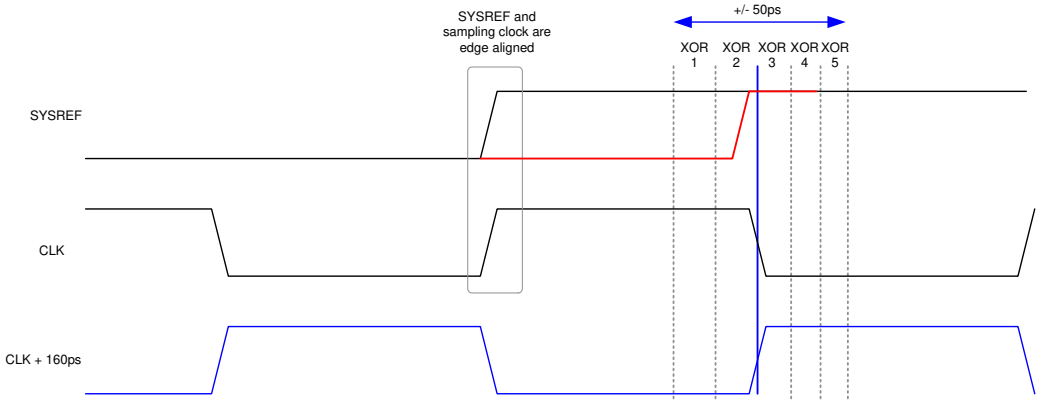

図 6-22. Detection of SYSREF Transition within Capture Window

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表 6-14. SYSREF Window Register Example (0x22F)

ADDR	D7	D6	D5	D4	D3	D2	D1	D0
0x22F	1	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1	SYSREF OR	1
	1	0	0	0	1	0	1	1

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6.3.5 Decimation Filter

The ADC34RF55 provides up to two digital down converters per ADC channel (see 図 6-23). The decimation filters provide a flexible option to cover a wide range of instantaneous bandwidths (IBW) as shown in 表 6-15. Single band decimation supports a wide bandwidth up to complex decimation by 4 while up to two narrow band channels with up to 128x complex decimation are supported in dual band decimation mode.

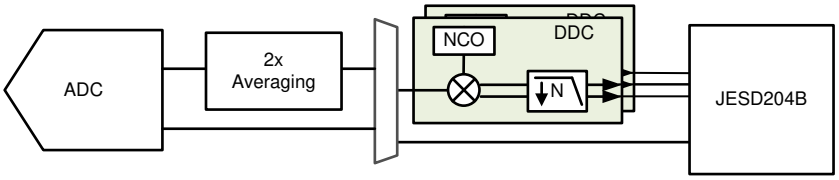

図 6-23. Digital Decimation Filter Options

表 6-15. Summary of Different Decimation Filter Band Options

No. of DDCs	Minimum Complex Decimation	Maximum Complex Decimation
1	4	128
2	8	128

The decimation filter can be configured to two different operating modes:

- Complex Decimation: This mode provides complex output with ~ 80% passband bandwidth using a 48-bit phase coherent NCO.

  During the complex mixing operation the digital output is reduced by 6-dB. This reduces the full scale from 0-dBFS to -6-dBFS. This 6-dB change applies to signals and noise and thus no dynamic range is lost.
- Real Decimation: In real decimation mode, the complex mixer is bypassed (NCO is set to 0 for lowest power consumption), and the digital filter acts as a low pass filter. There is no frequency shifting and the output passband bandwidth is approximately 40%.

Since the JESD204B interface is common across all ADC channels, the decimation ratio as well as the number of DDCs and ADC has to be the same across all ADC channels.

By default the output of values of the decimation filter are rounded to 16-bit resolution. To avoid quantization noise limitation when using high order of decimation (that is, /64 or /128), a special 32-bit output mode can be enabled (see セクション 6.3.5.3).

表 6-16 provides an overview of the available complex decimation settings and resulting complex and real output bandwidths. Note that some of the lower decimation settings requires a reduced sampling rate due to output bandwidth limitation of the JESD204B interface.

表 6-16. Decimation Setting vs Output Bandwidth

Decimation Factor N (complex)	Complex Output Bandwidth per DDC	F_S = 3 Gsps		Real Output Bandwidth per DDC	F_S = 3 Gsps	
		Complex Output Rate per DDC	Complex Output Bandwidth per DDC		Real Output Rate per DDC	Real Output Bandwidth per DDC
4(1)	0.8 x F_S / 4	650 Msps	520 MHz	0.4 x F_S / 4	750 Msps	300 MHz
8	0.8 x F_S / 8	375 Msps	300 MHz	0.4 x F_S / 8	375 Msps	150 MHz
16	0.8 x F_S / 16	187.5 Msps	150 MHz	0.4 x F_S / 16	187.5 Msps	75 MHz
32	0.8 x F_S / 32	93.75 Msps	75 MHz	0.4 x F_S / 32	93.75 Msps	37.5 MHz
64	0.8 x F_S / 64	46.875 Msps	37.5 MHz	0.4 x F_S / 64	46.875 Msps	18.75 MHz
128	0.8 x F_S / 128	23.4375 Msps	18.75 MHz	0.4 x F_S / 128	23.4375 Msps	9.375 MHz

(1) Limited to 2.6 GSPS in complex decimation.

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6.3.5.1 Decimation Filter Response

This section provides the different decimation filter responses with a normalized ADC sampling rate. The complex filter pass band is approximately 80% (-1 dB) with a minimum of 85 dB stop band rejection.

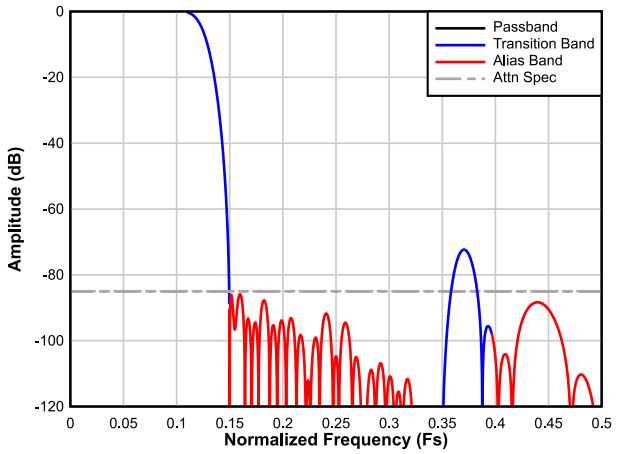

図 6-24. Complex Decimation by 4 Filter Response

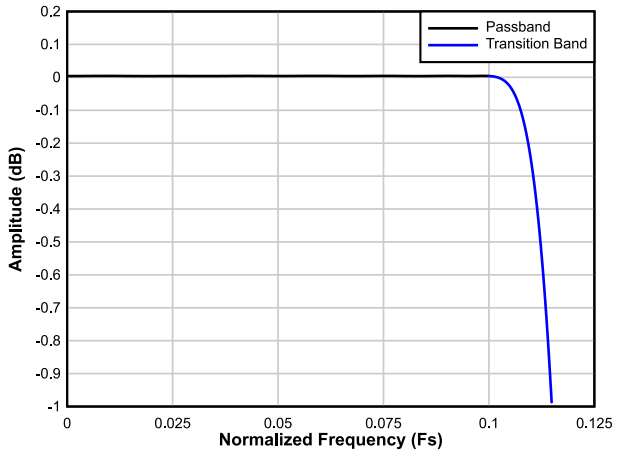

図 6-25. Decimation by 4 Passband Ripple Response

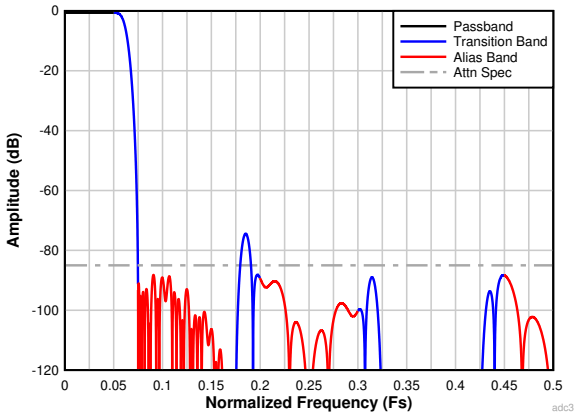

図 6-26. Complex Decimation by 8 Filter Response

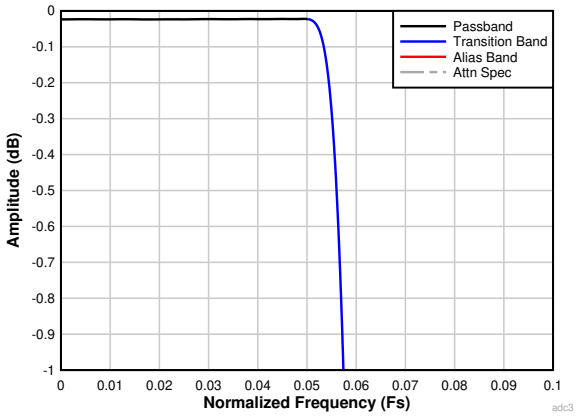

図 6-27. Decimation by 8 Passband Ripple Response

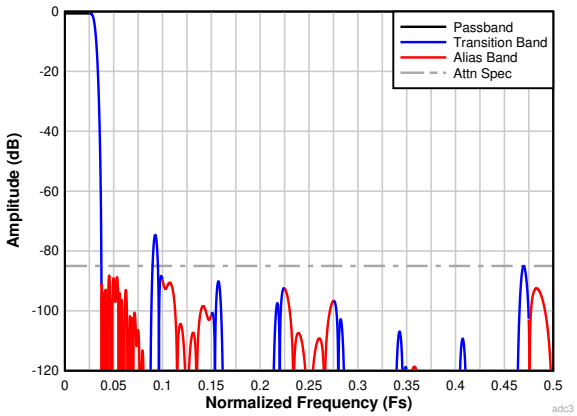

図 6-28. Complex Decimation by 16 Filter Response

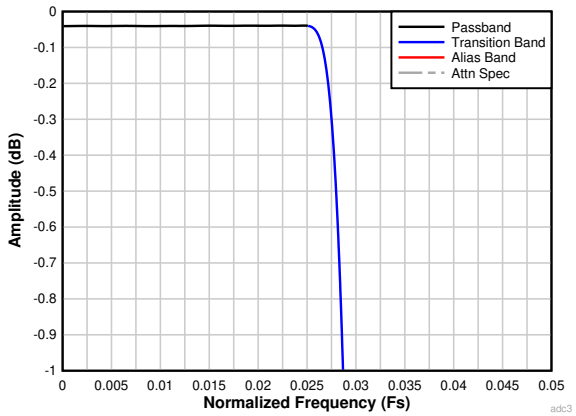

図 6-29. Decimation by 16 Passband Ripple Response

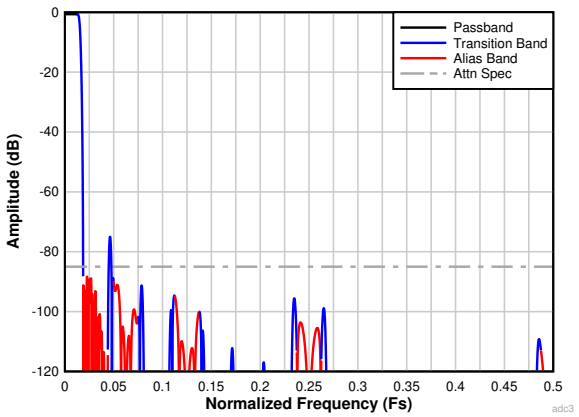

図 6-30. Complex Decimation by 32 Filter Response

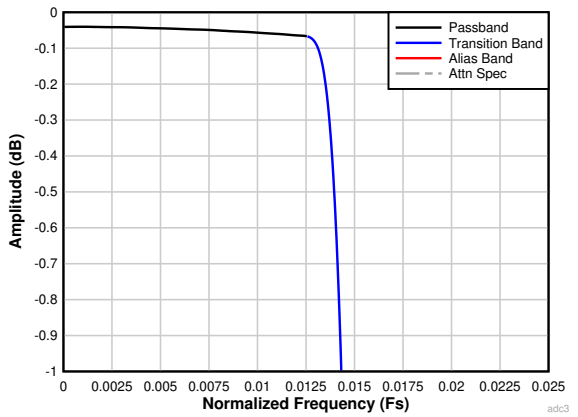

図 6-31. Decimation by 32 Passband Ripple Response

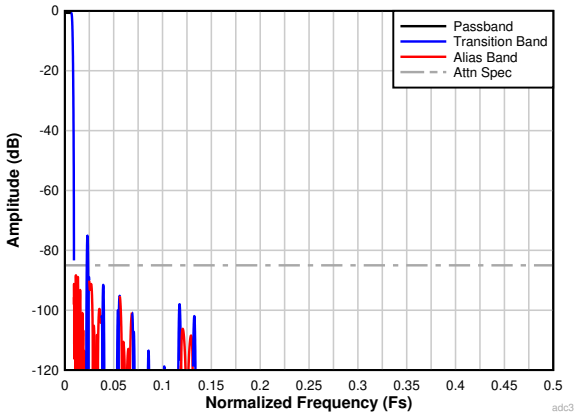

図 6-32. Complex Decimation by 64 Filter Response

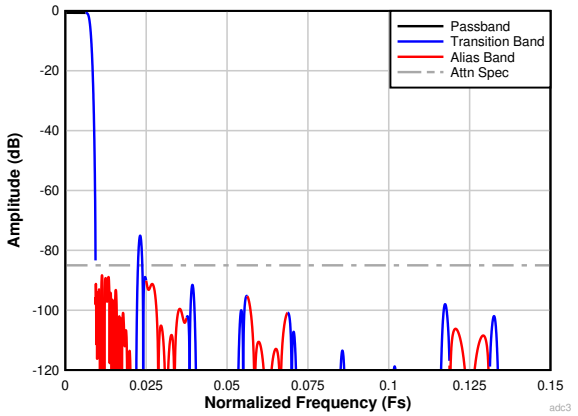

図 6-33. Complex Decimation by 64 Filter Response

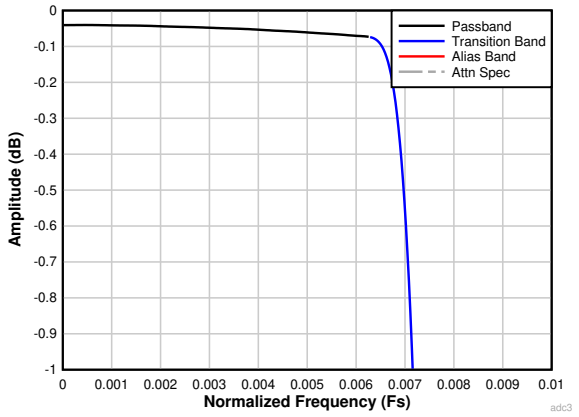

図 6-34. Decimation by 64 Passband Ripple Response

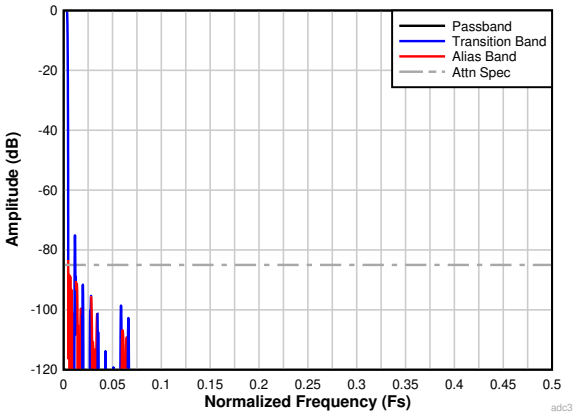

図 6-35. Complex Decimation by 128 Filter Response

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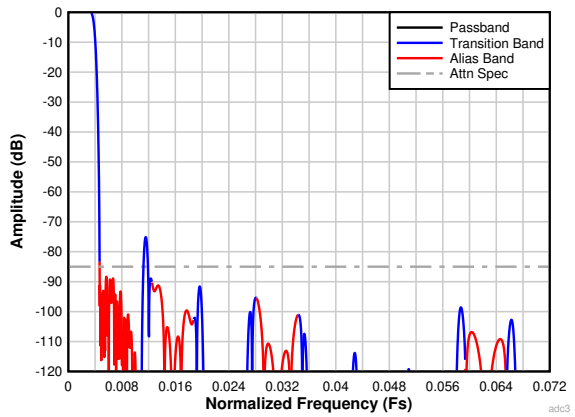

図 6-36. Complex Decimation by 128 Filter Response

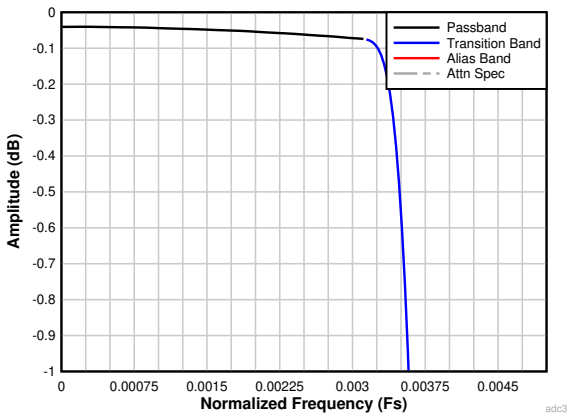

図 6-37. Decimation by 128 Passband Ripple Response

6.3.5.2 Decimation Filter Configuration

The decimation filter is configured with these register writes.

表 6-17. Register writes to enable the internal decimation filter

ADDR	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x2C		Select single/dual band
0x2D		Select decimation
0x05	0x04	Select JESD page
0x22		Select LMFS mode
0x24		Select DDC CLK setting
0x25		Select JESD TX CLK DIV setting
0x9F		Select JESD PLL1/2 settings
0xA0		Select JESD PLL INPUT1 setting
0xA1		Select JESD PLL INPUT2 settings

6.3.5.3 20-bit Output Mode

The device includes a 20-bit output resolution mode which can be used for high order decimation (such as: 64x, 128x) to avoid SNR degradation due to quantization noise limitation. In this mode, no additional JESD204B output lanes are added but the output data is transmitted at 2x the output rate and two consecutive 16-bit samples are filled with one 20-bit sample. So for example, a single band complex decimation would go from LMFS = 4841 (16-bit output mode) to LMFS = 4881 (20-bit output mode) as illustrated in 表 6-18.

The 20-bit output mode is enabled by setting D7 in 0x2C (DIGITAL page) and selecting viable decimation and LMFS mode.

表 6-18. JESD Frame Assembly Comparison between 16-bit and 20-bit Output Mode

LMFS = 4841					LMFS = 4881							
xI_0[15:8]	xI_0[7:0]	xQ_0[15:8]	xQ_0[7:0]		xI_0[31:24]	xI_0[23:16]	xI_0[15:8]	xI_0[7:0]	xQ_0[31:24]	xQ_0[23:16]	xQ_0[15:8]	xQ_0[7:0]
					20-bit sample I		0000 00000000		20-bit sample Q		0000 00000000	

6.3.5.4 Numerically Controlled Oscillator (NCO)

Each digital down-converter (DDC) uses a 48-bit numerically controlled oscillator (NCO) to fine tune the frequency placement prior to the digital filtering. Different NCO frequencies for each DDC are programmed using SPI register writes and the desired NCO frequency can be selected using SPI or the GPIO pins. When using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1 µs. The digital NCO is designed to have a SFDR of at least 100 dB. The number of available, programmable NCO frequencies depends on the number of DDC bands used as shown in 表 6-19.

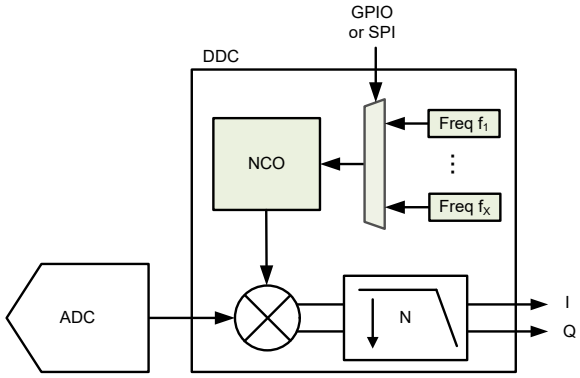

図 6-38. Phase Coherent NCO Block Diagram

表 6-19. Available No. of Frequencies per NCO depending on No. of DDCs used

No. of DDCs used	No. of Frequencies per NCO
1	4
2	4

There are two different NCO operating modes available. Phase continuous and infinite phase coherent.

1. **Phase Continuous NCO**: During a NCO frequency change, the NCO phase gradually adjusts to the new frequency as shown in 図 6-39. The *dashed line* shows the phase of original f_1 frequency.
2. **Infinite Phase Coherent NCO**: With a phase coherent NCO, all frequencies are synchronized to a single event using SYSREF. This enables an infinite amount of frequency hops without the need to reset the NCO as phase coherency is maintained between frequency hops. This is illustrated in 図 6-39 (right). When returning to the original frequency f_1, the NCO phase appears as if the NCO had never changed frequencies.

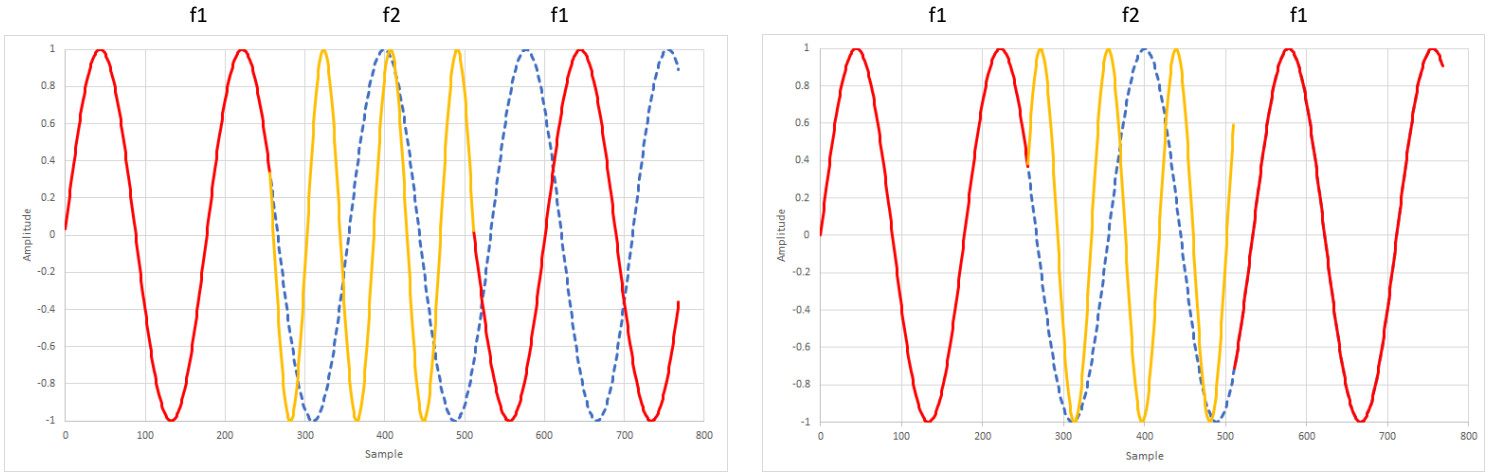

図 6-39. Phase Continuous (left) and Infinite Phase Coherent (right) NCO Frequency Switching

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The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \quad (1)$$

where: frequency (ω) is specified as a signed number by the 48-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to f_{IN} + f_{NCO}. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number.

The NCO frequency setting is set by the 48-bit register value given and calculated as:

$$\text{NCO frequency (0 to + } F_S/2\text{): NCO} = f_{NCO} \times 2^{48} / F_S \quad (2)$$

$$\text{NCO frequency (-}F_S/2 \text{ to 0): NCO} = (f_{NCO} + F_S) \times 2^{48} / F_S \quad (3)$$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is illustrated with this example:

- ADC sampling rate F_S = 3000 MSPS
- Desired NCO frequency = 920 MHz

$$\text{NCO frequency setting} = f_{NCO} \times 2^{48} / F_S = 920 \text{ MHz x } 2^{48} / 3000 \text{ MSPS} = 86{,}318{,}992{,}857{,}935 \quad (4)$$

表 6-20 shows the register writes to set frequency 1 of NCO1 of DDCA to that frequency:

表 6-20. Example register writes to change NCO frequency

ADDR	DATA	DESCRIPTION
0x05	0x08	Select DDCAB page
0x105	0x4E	Set frequency to 920 MHz (86,318,992,857,935) which is 0x4E81B4E81B4E starting MSB in 0x105.
0x104	0x81	
0x103	0xB4	
0x102	0xE8	
0x101	0x1B	
0x100	0x4E	
0x180	0x01	Select phase coherent NCO mode.
0x181	0x00	Load and update NCO1 with the new frequency.
0x181	0x30	

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6.3.5.5 NCO Frequency Programming Using the SPI Interface

There are 2 separate NCOs per channel - one for each band (that is, NCO1 = band 1) and 4 different frequencies can be programmed per NCO as shown in 図 6-40. The NCO frequencies are located in the DDCAB/CD pages (0x05 0x08 for channel A/B and 0x05 0x10 for channel C/D) in registers 0x100 to 0x17D. Depending on the number of bands used, the frequencies for each NCO are selected in registers 0x3B and 0x41 (DIGITAL page) as shown in 表 6-21. If the NCO frequencies are the same for channel A/B and channel C/D they can be written to both DDCAB and DDCCD pages simultaneously by selecting both pages (0x05 0x18).

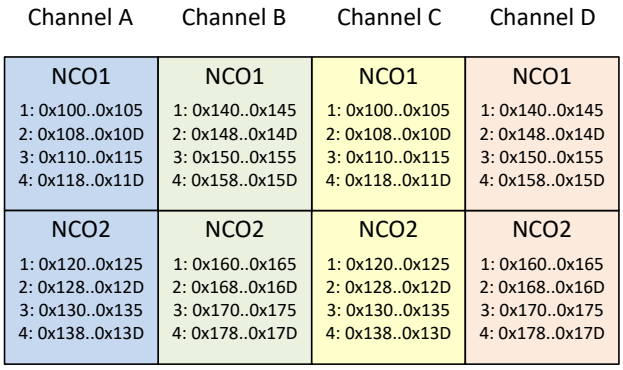

図 6-40. Multi-Band NCO

Single band DDC uses the frequencies of both NCO1 and NCO2 for a combined 8 different frequencies for NCO1 using 3 bit control (NCO2 CHx [1] and NCO1 CHx [1:0]). The NCO2 selection bit (D3) decides if frequencies from NCO1 or NCO2 are being used. In dual band DDC operating mode there are 4 frequencies per NCO available and selected using 2 register bits (NCOx CHx [1:0]).

表 6-21. NCO Frequency Selection SPI Interface Registers

NO. OF BANDS	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
SINGLE	0x3B	NCO2 CHB [1]	0	NCO1 CHB [1:0]		NCO2 CHA [1]	0	NCO1 CHA [1:0]	
	0x41	NCO2 CHD [1]	0	NCO1 CHD [1:0]		NCO2 CHC [1]	0	NCO1 CHC [1:0]	
DUAL	0x3B	NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	
	0x41	NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]	

To select a different frequency for the NCO, two registers (0x3B and 0x41) in the DIGITAL page have to be updated. Assuming a SPI clock frequency of 10 MHz (100 ns period), programming two registers (2x (16 bit address and 8 bit data) = 48 bit) means that the NCO frequency would be updated in approximately 5 µs.

When updating the NCO frequency being used to a new frequency, the following command must be written to load the new frequency into the NCO - 0x181 0x00/0x30 in each of the DDCAB/CD pages.

表 6-22. Example Register Writes

ADDR	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x3B	0x01	Select frequency 2 for NCO1 of channel A.
0x235	0xFF	Select NCO using SPI
0x05	0x08	Select DDCAB page
0x10D...0x108	0x..	Write new frequency in frequency 2 of NCO1 of channel A
0x181	0x00	Update NCO with current frequencies from the register map.
0x181	0x30	

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The NCO phase accumulators can be reset using the external SYSREF signal. A SYSREF mask can be setup such the SYSREF signal only goes to the NCO and the remaining device remains unaffected. The following register writes configure the SYSREF mask to only affect the NCO. After completion the SYSREF mask should be set back to default.

表 6-23. Example Register Writes to configure the SYSREF MASK

ADDR	DATA	DESCRIPTION
0x05	0x18	Select DDCAB/CD page
0x181	0x40	Reset NCO phases with SYSREF toggle
0x05	0x02	Select DIGITAL page
0x357	0xA2	SYSREF mask settings (0x00 is mask default)
0x358	0x02	SYSREF mask settings (0x00 is mask default)

6.3.5.6 Fast Frequency Hopping

The ADC34RF5x supports several different options to update the NCO frequencies. Fast frequency hopping can be achieved in one of the following ways:

- Using the GPIO1/2 pins to select the NCO frequency
- Using the GPIO1/2, SPISEL and SCLK/SDIO pins to select the NCO frequency
- Using the GPIO1/2 pins to program the NCO frequency selection (Fast SPI)

NCO CONTROL	SCLK	SDATA	SPISEL	GPIO1	GPIO2	NCO SEL MODE
Regular SPI (default)	SPI Interface		0	used for other purpose		00
GPIO1/2	SPI Interface		0	used for NCO control		00
GPIO1/2, SPISEL, SCLK/SDATA	NCO CONTROL		1	used for NCO control		00
FAST SPI	SPI Interface		1	SDATA	SCLK	10

The internal NCO is switched quickly. However, the switching time depends primarily on the time it takes to flush out the decimation filter as shown in 表 6-24.

表 6-24. NCO switching time (F_S = 3 GSPS) vs decimation setting

Decimation Setting	NCO Switching Time
/4	~ 250 ns
/8	~ 350 ns
/16	~ 600 ns
/32	~ 1 us
/64	~ 2 us
/128	~ 4 us

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6.3.5.6.1 Fast frequency hopping using the GPIO1/2 pins

The NCO frequency is selected as shown in 表 6-25. This mode is enabled with the following register writes:

1. Set 0x234 to 0x03 (NCO SEL MODE = 0, GPIO MODE = 3)

表 6-25. NCO Frequency Selection using GPIO1/2 Pins

NO. OF BANDS	GPIO2	GPIO1	GPIO2	GPIO1	GPIO2	GPIO1	GPIO2	GPIO1
SINGLE	0	0	NCO1 CHB [1:0]		0	0	NCO1 CHA [1:0]	
	0	0	NCO1 CHD [1:0]		0	0	NCO1 CHC [1:0]	
DUAL	NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	
	NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]	

6.3.5.6.2 Fast frequency hopping using GPIO1/2, SEN and SDATA pins

This mode is enabled by setting the SPISEL to logic high and using the following register writes:

1. NCO SEL MODE in address 0x234 needs to be set to 3

表 6-26. NCO Frequency Selection SPI Interface Registers

NO. OF BANDS	SDATA	SEN	GPIO2	GPIO1	SDATA	SEN	GPIO2	GPIO1
SINGLE	NCO1 CHB [2]	0	NCO1 CHB [1:0]		NCO1 CHA [2]	0	NCO1 CHA [1:0]	
	NCO1 CHD [2]	0	NCO1 CHD [1:0]		NCO1 CHC [2]	0	NCO1 CHC [1:0]	
DUAL	NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	
	NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]	

6.3.5.6.3 Fast frequency hopping using the fast SPI

In this mode, the GPIO1/2 pins are used as a *fast SPI* input which only updates the NCO selection registers. No register address information needs to be sent. GPIO1 pin is SDATA and GPIO2 pin is SCLK.

This mode is enabled by setting the SPISEL to logic high and using the following register writes:

1. Set 0x234 to 0x43 (NCO SEL MODE = 2, GPIO MODE = 3)

The NCO frequencies are selected as shown in 表 6-27.

表 6-27. NCO Frequency Programming using FAST SPI

NO. OF BANDS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SINGLE	NCO1 CHD [2]	0	NCO1 CHD [1:0]		NCO1 CHC [2]	0	NCO1 CHC [1:0]		NCO1 CHB [2]	0	NCO1 CHB [1:0]		NCO1 CHA [2]	0	NCO1 CHA [1:0]	
DUAL	NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]		NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	

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6.3.6 JESD204B Interface

The ADC34RF5x uses the JESD204B high-speed serial interface to transfer data from the ADC to the receiving logic device. ADC34RF5x serialized lanes are capable of operating up to 13 Gbps, slightly above the JESD204B max lane rate. A maximum of 8 lanes can be used to allow lower lane rates for interfacing with speed limited logic devices. 図 6-41 shows a simplified block diagram of the JESD204B interface.

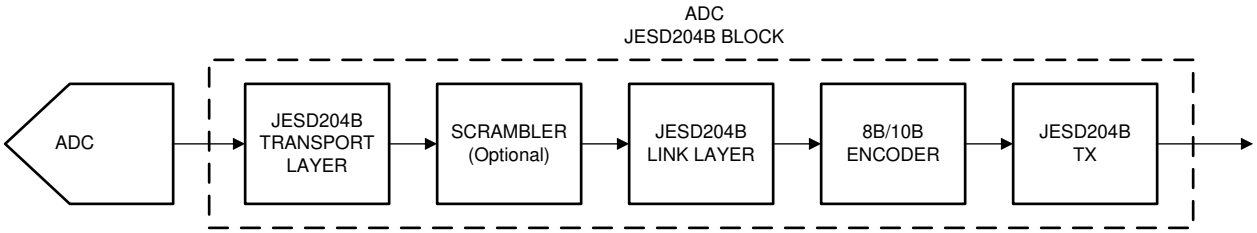

図 6-41. JESD204B Block Diagram

6.3.6.1 JESD204B Initial Lane Alignment (ILA)

The receiving device starts the initial lane alignment process by deasserting the $\overline{\text{SYNC}}$ signal. When a logic low state is detected on the $\overline{\text{SYNC}}$ input, the ADC starts transmitting comma characters (K28.5) to establish the code group synchronization, as shown in 図 6-42. When synchronization is completed, the receiving device reasserts the $\overline{\text{SYNC}}$ signal and the ADC starts the initial lane alignment sequence with the next local multi-frame clock (LMFC) boundary. The ADC transmits four multi-frames, each containing K frame (K is SPI programmable). Each of the multi-frames contains the frame start and frame end symbols. The second multi-frame also contains the JESD204B link configuration data.

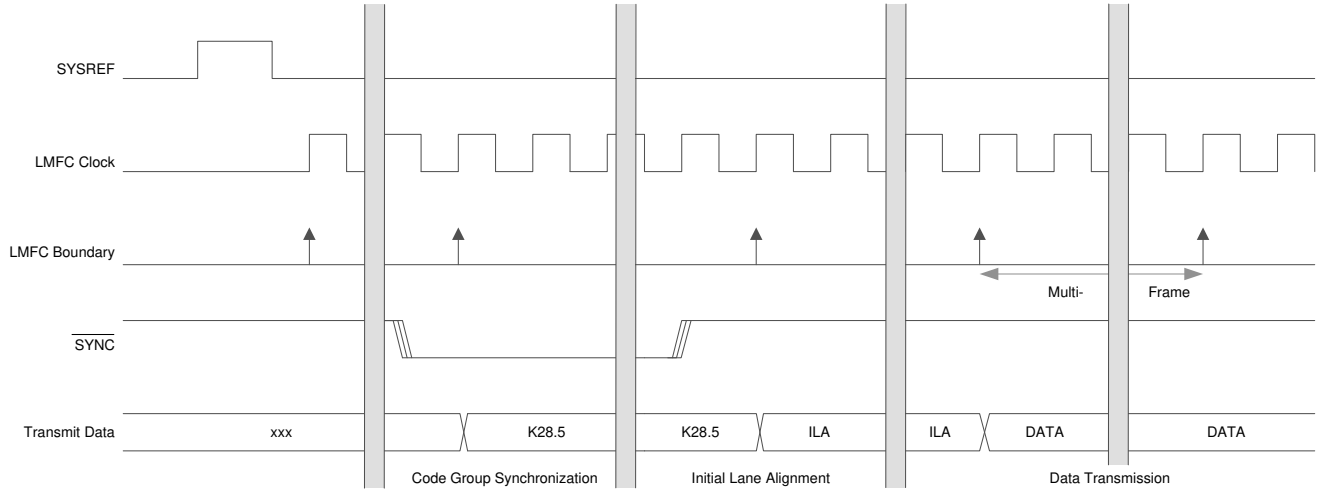

図 6-42. JESD204B Internal Timing Diagram

6.3.6.1.1 $\overline{\text{SYNC}}$ Signal

The $\overline{\text{SYNC}}$ signal can be issued using one of two different methods:

- One of the GPIO1/2 pins can be configured via SPI to become the $\overline{\text{SYNC}}$ input pin (address 0x234 in the digital page)
- The synchronization command can be issued via SPI register write (address 0x21 in the JESD page)

When using the GPIO1/2 pins for the $\overline{\text{SYNC}}$ signal input, the device also supports the option to invert the signal polarity (address 0x236 in the digital page).

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6.3.6.2 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L: number of lanes per link
- M: number of converters per device
- F: number of octets per frame clock period
- S: number of samples per frame

6.3.6.2.1 JESD204B Frame Assembly in Bypass Mode

表 6-28 lists the available JESD204B formats and corresponding valid sampling rate ranges for the ADC34RF5x. The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes is shown in 表 6-29.

表 6-28. JESD Mode Options: Bypass Mode

DECIMATION SETTING D (complex)	OUTPUT RESOLUTION (Bits)	L	M	F	S	MIN F_S (Gsps)	MAX F_S (Gsps)	RATIO [f_{SERDES}/F_S]
Bypass	12(1)	8	4	8	10	0.5	1.5	8
	14	8	4	2	2	0.5	1.3	10
	14	4	4	2	1	0.5	0.65	20

(1) In full rate output, the two LSBs are truncated to a 12-bit output.

表 6-29. JESD Sample Frame Assembly: Bypass Mode

OUTPUT LANE	LMFS = 84810								LMFS = 8422		LMFS = 4421	
DOUT0	A_0[11:4]	A_0[3:0], A_1[11:8]	A_1[7:0]	A_2[11:4]	A_2[3:0], A_3[11:8]	A_3[7:0]	A_4[11:4]	A_4[3:0], 0000	A_0[13:6]	A_0[5:0], 00	A_0[13:6]	A_0[5:0], 00
DOUT1	A_5[11:4]	A_5[3:0], A_6[11:8]	A_6[7:0]	A_7[11:4]	A_7[3:0], A_8[11:8]	A_8[7:0]	A_9[11:4]	A_9[3:0], 0000	A_1[13:6]	A_1[5:0], 00	B_0[13:6]	B_0[5:0], 00
DOUT2	B_0[11:4]	B_0[3:0], B_1[11:8]	B_1[7:0]	B_2[11:4]	B_2[3:0], B_3[11:8]	B_3[7:0]	B_4[11:4]	B_4[3:0], 0000	B_0[13:6]	B_0[5:0], 00	C_0[13:6]	C_0[5:0], 00
DOUT3	B_5[11:4]	B_5[3:0], B_6[11:8]	B_6[7:0]	B_7[11:4]	B_7[3:0], B_8[11:8]	B_8[7:0]	B_9[11:4]	B_9[3:0], 0000	B_1[13:6]	B_1[5:0], 00	D_0[13:6]	D_0[5:0], 00
DOUT4	C_0[11:4]	C_0[3:0], C_1[11:8]	C_1[7:0]	C_2[11:4]	C_2[3:0], C_3[11:8]	C_3[7:0]	C_4[11:4]	C_4[3:0], 0000	C_0[13:6]	C_0[5:0], 00		
DOUT5	C_5[11:4]	C_5[3:0], C_6[11:8]	C_6[7:0]	C_7[11:4]	C_7[3:0], C_8[11:8]	C_8[7:0]	C_9[11:4]	C_9[3:0], 0000	C_1[13:6]	C_1[5:0], 00		
DOUT6	D_0[11:4]	D_0[3:0], D_1[11:8]	D_1[7:0]	D_2[11:4]	D_2[3:0], D_3[11:8]	D_3[7:0]	D_4[11:4]	D_4[3:0], 0000	D_0[13:6]	D_0[5:0], 00		
DOUT7	D_5[11:4]	D_5[3:0], D_6[11:8]	D_6[7:0]	D_7[11:4]	D_7[3:0], D_8[11:8]	D_8[7:0]	D_9[11:4]	D_9[3:0], 0000	D_1[13:6]	D_1[5:0], 00		

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6.3.6.2.2 JESD204B Frame Assembly with Real Decimation - Single Band

表 6-30 lists the available JESD204B formats and corresponding valid sampling rate ranges for the ADC34RF55. The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes is shown in 表 6-31.

表 6-30. JESD Mode Options: Real Decimation

DECIMATION SETTING D (complex)	L	M	F	S	MIN F_S (Gsps)	MAX F_S (Gsps)	RATIO [$f_{SERDES}/(F_S/D)$]
/4	8	4	2	2	0.5	3.0	10
/8							
/16					0.8		
/4	4	4	2	1	0.5	2.6	20
/8						3.0	
/16							
/32					0.8		
/4	2	4	4	1	0.5	1.3	40
/8						2.6	
/16						3.0	
/32							
/64					0.8		
/8	1	4	8	1	0.5	1.3	80
/16						2.6	
/32						3.0	
/64							
/128					0.8		

表 6-31. JESD Sample Frame Assembly: Real Decimation - Single Band

OUTPUT LANE	LMFS = 8422		LMFS = 4421		LMFS = 2441				LMFS = 1481							
DOUT0	A_0 [15:8]	A_0 [7:0]	A_0 [15:8]	A_0 [7:0]	A_0 [15:8]	A_0 [7:0]	B_0 [15:8]	B_0 [7:0]	A_0 [15:8]	A_0 [7:0]	B_0 [15:8]	B_0 [7:0]	C_0 [15:8]	C_0 [7:0]	D_0 [15:8]	D_0 [7:0]
DOUT1	A_1 [15:8]	A_1 [7:0]	B_0 [15:8]	B_0 [7:0]	C_0 [15:8]	C_0 [7:0]	D_0 [15:8]	D_0 [7:0]								
DOUT2	B_0 [15:8]	B_0 [7:0]	C_0 [15:8]	C_0 [7:0]												
DOUT3	B_1 [15:8]	B_1 [7:0]	D_0 [15:8]	D_0 [7:0]												
DOUT4	C_0 [15:8]	C_0 [7:0]														
DOUT5	C_1 [15:8]	C_1 [7:0]														
DOUT6	D_0 [15:8]	D_0 [7:0]														
DOUT7	D_1 [15:8]	D_1 [7:0]														

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6.3.6.2.3 JESD204B Frame Assembly with Complex Decimation - Single Band

表 6-32 lists the available JESD204B interface formats and corresponding valid sampling rate ranges for the ADC34RF55 with complex decimation (single band). The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes are shown in 表 6-33 and 表 6-34.

表 6-32. JESD Mode Options: Decimation - Single Band

DECIMATION SETTING D (complex)	L	M	F	S	MIN F_S (Gsps)	MAX F_S (Gsps)	RATIO [$f_{SERDES}/(F_S/D)$]
/4	8	8	2	1	0.5	2.6	20
/8						3.0	
/16							
/32					0.75		
/64					1.5		
/4	4	8	4	1	0.5	1.3	40
/8						2.6	
/16						3.0	
/32							
/64					0.75		
/128					1.5		
/8	2	8	8	1	0.5	1.3	80
/16						2.6	
/32						3.0	
/64							
/128					0.75		
/16	1	8	16	1	0.5	1.3	160
/32						2.6	
/64						3.0	
/128							

表 6-33. JESD Sample Frame Assembly: Decimation - Single Band

OUTPUT LANE	LMFS = 8821		LMFS = 4841				LMFS = 2881							
DOUT0	AI_0 [15:8]	AI_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]
DOUT1	AQ_0 [15:8]	AQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	CI_0 [15:8]	CI_0 [7:0]	CQ_0 [15:8]	CQ_0 [7:0]	DI_0 [15:8]	DI_0 [7:0]	DQ_0 [15:8]	DQ_0 [7:0]
DOUT2	BI_0 [15:8]	BI_0 [7:0]	CI_0 [15:8]	CI_0 [7:0]	CQ_0 [15:8]	CQ_0 [7:0]								
DOUT3	BQ_0 [15:8]	BQ_0 [7:0]	DI_0 [15:8]	DI_0 [7:0]	DQ_0 [15:8]	DQ_0 [7:0]								
DOUT4	CI_0 [15:8]	CI_0 [7:0]												
DOUT5	CQ_0 [15:8]	CQ_0 [7:0]												
DOUT6	DI_0 [15:8]	DI_0 [7:0]												
DOUT7	DQ_0 [15:8]	DQ_0 [7:0]												

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表 6-34. JESD Sample Frame Assembly: Decimation - Single Band

OUTPUT LANE	LMFS = 1-8-16-1															
DOUT0	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	CI_0 [15:8]	CI_0 [7:0]	CQ_0 [15:8]	CQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	DI_0 [15:8]	DI_0 [7:0]	DQ_0 [15:8]	DQ_0 [7:0]
DOUT1																
DOUT2																
DOUT3																
DOUT4																
DOUT5																
DOUT6																
DOUT7																

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6.3.6.2.4 JESD204B Frame Assembly with Decimation - Dual Band

表 6-35 lists the available JESD204B interface formats and corresponding valid sampling rate ranges for the ADC34RF55 with complex decimation (dual band). The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes are shown in 表 6-36, 表 6-37 and 表 6-38.

表 6-35. JESD Mode Options: Decimation - Dual Band

DECIMATION SETTING D (complex)	L	M	F	S	MIN F_S (Gsps)	MAX F_S (Gsps)	RATIO [$f_{SERDES}/(F_S/D)$]
/8	8	16	4	1	0.5	2.6	40
/16						3.0	
/32							
/64					0.8		
/128					1.6		
/8	4	16	8	1	0.5	1.3	80
/16						2.6	
/32						3.0	
/64							
/128					0.8		
/16	2	16	16	1	0.5	1.3	160
/32						2.6	
/64						3.0	
/128							
/32	1	16	32	1	0.5	1.3	320
/64						2.6	
/128						3.0	

表 6-36. JESD Sample Frame Assembly: Decimation - Dual Band

OUTPUT LANE	LMFS = 8-16-4-1				LMFS = 4-16-8-1							
DOUT0	$A1I_0$ [15:8]	$A1I_0$ [7:0]	$A1Q_0$ [15:8]	$A1Q_0$ [7:0]	$A1I_0$ [15:8]	$A1I_0$ [7:0]	$A1Q_0$ [15:8]	$A1Q_0$ [7:0]	$A2I_0$ [15:8]	$A2I_0$ [7:0]	$A2Q_0$ [15:8]	$A2Q_0$ [7:0]
DOUT1	$A2I_0$ [15:8]	$A2I_0$ [7:0]	$A2Q_0$ [15:8]	$A2Q_0$ [7:0]	$B1I_0$ [15:8]	$B1I_0$ [7:0]	$B1Q_0$ [15:8]	$B1Q_0$ [7:0]	$B2I_0$ [15:8]	$B2I_0$ [7:0]	$B2Q_0$ [15:8]	$B2Q_0$ [7:0]
DOUT2	$B1I_0$ [15:8]	$B1I_0$ [7:0]	$B1Q_0$ [15:8]	$B1Q_0$ [7:0]	$C1I_0$ [15:8]	$C1I_0$ [7:0]	$C1Q_0$ [15:8]	$C1Q_0$ [7:0]	$C2I_0$ [15:8]	$C2I_0$ [7:0]	$C2Q_0$ [15:8]	$C2Q_0$ [7:0]
DOUT3	$B2I_0$ [15:8]	$B2I_0$ [7:0]	$B2Q_0$ [15:8]	$B2Q_0$ [7:0]	$D1I_0$ [15:8]	$D1I_0$ [7:0]	$D1Q_0$ [15:8]	$D1Q_0$ [7:0]	$D2I_0$ [15:8]	$D2I_0$ [7:0]	$D2Q_0$ [15:8]	$D2Q_0$ [7:0]
DOUT4	CI_0 [15:8]	$C1I_0$ [7:0]	$C1Q_0$ [15:8]	$C1Q_0$ [7:0]								
DOUT5	$C2I_0$ [15:8]	$C2I_0$ [7:0]	$C2Q_0$ [15:8]	$C2Q_0$ [7:0]								
DOUT6	$D1I_0$ [15:8]	$D1I_0$ [7:0]	$D1Q_0$ [15:8]	$D1Q_0$ [7:0]								
DOUT7	$D2I_0$ [15:8]	$D2I_0$ [7:0]	$D2Q_0$ [15:8]	$D2Q_0$ [7:0]								

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表 6-37. JESD Sample Frame Assembly: Decimation - Dual Band

OUTPUT LANE	LMFS = 2-16-16-1															
DOUT0	$A1I_0$ [15:8]	$A1I_0$ [7:0]	$A1Q_0$ [15:8]	$A1Q_0$ [7:0]	$A2I_0$ [15:8]	$A2I_0$ [7:0]	$A2Q_0$ [15:8]	$A2Q_0$ [7:0]	$B1I_0$ [15:8]	$B1I_0$ [7:0]	$B1Q_0$ [15:8]	$B1Q_0$ [7:0]	$B2I_0$ [15:8]	$B2I_0$ [7:0]	$B2Q_0$ [15:8]	$B2Q_0$ [7:0]
DOUT1	$C1I_0$ [15:8]	$C1I_0$ [7:0]	$C1Q_0$ [15:8]	$C1Q_0$ [7:0]	$C2I_0$ [15:8]	$C2I_0$ [7:0]	$C2Q_0$ [15:8]	$C2Q_0$ [7:0]	$D1I_0$ [15:8]	$D1I_0$ [7:0]	$D1Q_0$ [15:8]	$D1Q_0$ [7:0]	$D2I_0$ [15:8]	$D2I_0$ [7:0]	$D2Q_0$ [15:8]	$D2Q_0$ [7:0]
DOUT2																
DOUT3																
DOUT4																
DOUT5																
DOUT6																
DOUT7																

表 6-38. JESD Sample Frame Assembly: Decimation - Dual Band

OUTPUT LANE	LMFS = 1-16-32-1																
DOUT0	$A1I_0$ [15:8]	$A1I_0$ [7:0]	$A1Q_0$ [15:8]	$A1Q_0$ [7:0]	$A2I_0$ [15:8]	$A2I_0$ [7:0]	$A2Q_0$ [15:8]	$A2Q_0$ [7:0]	$B1I_0$ [15:8]	$B1I_0$ [7:0]	$B1Q_0$ [15:8]	$B1Q_0$ [7:0]	$B2I_0$ [15:8]	$B2I_0$ [7:0]	$B2Q_0$ [15:8]	$B2Q_0$ [7:0]	...
	...	$C1I_0$ [15:8]	$C1I_0$ [7:0]	$C1Q_0$ [15:8]	$C1Q_0$ [7:0]	$C2I_0$ [15:8]	$C2I_0$ [7:0]	$C2Q_0$ [15:8]	$C2Q_0$ [7:0]	$D1I_0$ [15:8]	$D1I_0$ [7:0]	$D1Q_0$ [15:8]	$D1Q_0$ [7:0]	$D2I_0$ [15:8]	$D2I_0$ [7:0]	$D2Q_0$ [15:8]	$D2Q_0$ [7:0]
DOUT1																	
DOUT2																	
DOUT3																	
DOUT4																	
DOUT5																	
DOUT6																	
DOUT7																	

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6.3.6.3 SERDES Output MUX

The SERDES output block contains one digital mux per SERDES output lane with a 3-bit register. This allows routing any of the 8 digital streams to any output serdes transmitter as shown in the example in 図 6-43.

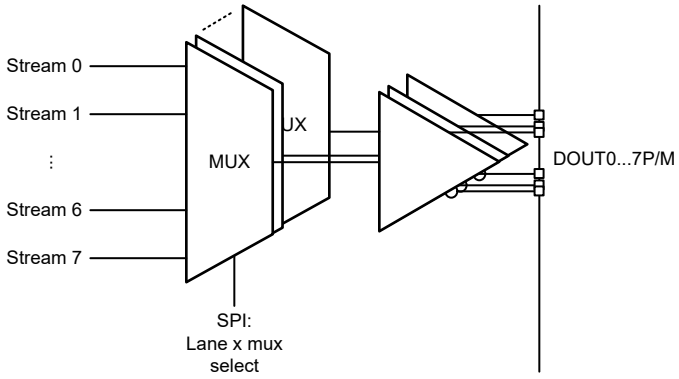

図 6-43. SERDES output mux for DOUT0

By default after power the active SERDES lanes start on lane DOUT0 as shown for the complex decimation single band example in 表 6-39. After power up the output is transmitted on lanes DOUT0..3. Using the digital output muxes, the output data for channel B is shifted from lanes DOUT2,3 to DOUT4,5. All SERDES transmitters are powered up and enabled by default. After configuring the output mux unused lanes can be powered down to save power consumption.

表 6-39. JESD Sample Frame Assembly: Complex Decimation - Single Band with LMFS = 4841

OUTPUT LANE	Default				Using MUX			
DOUT0	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]	AI_0 [15:8]	AI_0 [7:0]	AQ_0 [15:8]	AQ_0 [7:0]
DOUT1	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]	BI_0 [15:8]	BI_0 [7:0]	BQ_0 [15:8]	BQ_0 [7:0]
DOUT2	CI_0 [15:8]	CI_0 [7:0]	CQ_0 [15:8]	CQ_0 [7:0]				
DOUT3	DI_0 [15:8]	DI_0 [7:0]	DQ_0 [15:8]	DQ_0 [7:0]				
DOUT4					CI_0 [15:8]	CI_0 [7:0]	CQ_0 [15:8]	CQ_0 [7:0]
DOUT5					DI_0 [15:8]	DI_0 [7:0]	DQ_0 [15:8]	DQ_0 [7:0]
DOUT6								
DOUT7								

表 6-40 shows the register writes to shift the output lanes from default as illustrated in 表 6-39.

表 6-40. Example register writes to shift the output serdes lanes using the SERDES Output MUX

ADDR	DATA	DESCRIPTION
0x05	0x04	Select JESD page
0x81	0x54	Select internal JESD streams 4 and 5 to lanes DOUT2 and DOUT3
0x82	0x32	Select internal JESD streams 2 and 3 to lanes DOUT4 and DOUT5

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6.3.7 Test Pattern

The ADC34RF55 provides several different options to output test patterns instead of the actual output data of the ADC to simplify the serial interface and system debug of the JESD204B digital interface link. The output data path is shown in 図 6-44.

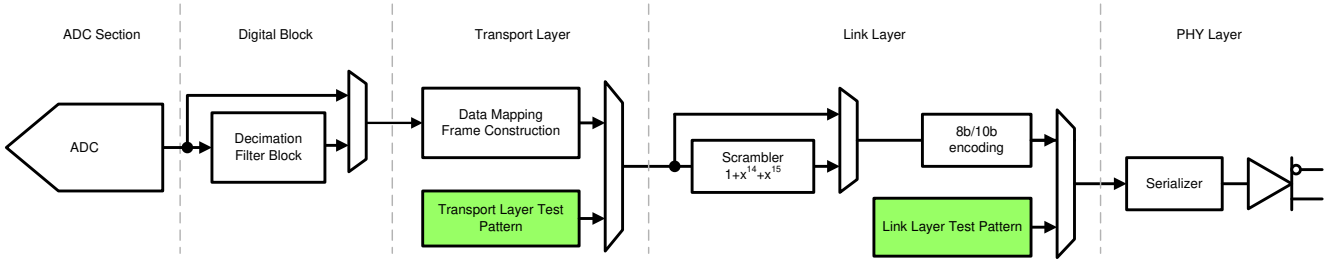

図 6-44. Test Pattern Options

The available test patterns in each block are described in 表 6-41. Both test pattern blocks replace output data from the digital block (and not from the ADC) and are available in decimation or decimation bypass mode.

表 6-41. Test Pattern Overview

TEST PATTERN LOCATION	TYPE	8b/10b encoded	REGISTER PAGE	REGISTER
TRANSPORT LAYER	CUSTOM PATTERN	Yes	JESD 0x05 0x04	0x2E, D0
	TOGGLE 1010 PATTERN	Yes		0x2E, D1
	RAMP PATTERN	Yes		0x2E, D2
LINK LAYER	JESD204B TEST PATTERNS	Depends		0x2D, D2-D0
	PRBS PATTERN (2^7.. 2^{31})	No		0x2F, D6-D4

The RAMP pattern provides two different output options. Internally each ADC data bus consists of parallel data streams. The RAMP pattern is generated for each stream and a different starting value can be set for each stream. By default all starting values are 0 and increment =1. For example, DDC bypass mode uses 2 internal data streams per ADC channel. Enabling a RAMP pattern would show a 'slow' ramp which increments once every 2 clock cycles with starting values set to 0 and ramp increment = 1.

On the other hand a RAMP pattern, which increments every clock cycle, can be set using different starting values (e.g. 0/1) for the 2 streams and setting the RAMP increment to 2. Table 表 6-42 shows the register addresses for the different digital streams being used for each operating mode.

表 6-42. Register address for RAMP starting values based on operating mode

Address (JESD Page)	Bypass Mode LMFS = 8-4-2-2	Complex Decimation Single Band	Complex Decimation Dual Band
0xA4/A5/A6	A_0	$A1I_0$	$A1I_0$
0xA8/A9/AA	A_1	$A1Q_0$	$A1Q_0$
0xAC/AD/AE			$A2I_0$
0xB0/B1/B2			$A2Q_0$
0xB4/B5/B6	B_0	$B1I_0$	$B1I_0$
0xB8/B9/BA	B_1	$B1Q_0$	$B2Q_0$
0xBC/BD/BE			$B2I_0$
0xC0/C1/C2			$B2Q_0$
0xC4/C5/C6	C_0	$C1I_0$	$C1I_0$
0xC8/C9/CA	C_1	$C1Q_0$	$C1Q_0$
0xCC/CD/CE			$C2I_0$
0xD0/D1/D2			$C2Q_0$

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表 6-42. Register address for RAMP starting values based on operating mode (続き)

Address (JESD Page)	Bypass Mode LMFS = 8-4-2-2	Complex Decimation Single Band	Complex Decimation Dual Band
0xD4/D5/D6	D_0	$D1I_0$	$D1I_0$
0xD8/D9/DA	D_1	$D1Q_0$	$D1Q_0$
0xDC/DD/DE			$D2I_0$
0xE0/E1/E2			$D2Q_0$

6.3.7.1 Transport Layer

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0's are added when needed. Alternatively, test patterns can be substituted instead of the ADC data with the JESD frame, as shown in 表 6-41.

6.3.7.2 Link Layer

The link layer contains the scrambler and the 8b/10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted. The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b/10b encoder and contain the options listed in 表 6-41.

6.3.7.3 Internal Capture Memory Buffer

The ADC includes a small internal capture memory buffer which can store up to 64 samples. Once a strobe is given to the memory using SPI register write, the memory stores the next continuous 64 samples of one ADC channel (selected via SPI register write) and stop. The samples are captured from the ADC cores (prior to averaging or decimation). These samples can be read back using the SPI interface without involving the JESD204B interface.

This mode allows debug of the analog front end during the initial bring-up phase even if the JESD204B interface is not yet operational.

表 6-43. Register writes to enable the internal sample capture buffer

ADDR	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x34		Select ADC channel (D5/D4) and give strobe (D6). The 64 samples are stored in 0x800 to 0x87F in the digital page

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6.4 Device Functional Modes

The device offers two different operating modes: bypass mode and digital averaging. Both operating modes use the same digital back end and JESD204B output configurations.

6.4.1 Bypass Mode

This default operating mode provides the lowest power consumption.

6.4.2 Digital Averaging

The ADC34RF55 provides a total of eight internal single core 3 Gsps ADCs. The normal operating mode uses only four ADC cores (one ADC per channel). The four additional ADC cores can be enabled to trade off additional noise density improvement against a small power increase. 図 6-45 shows the internal block diagram in digital averaging mode where one external input is connected to 2 ADC cores internally.

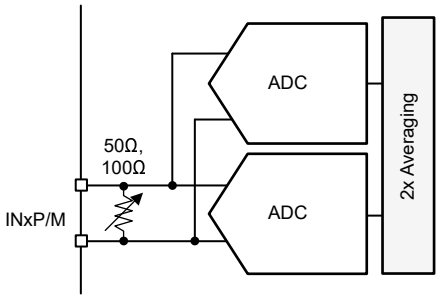

図 6-45. Internal Digital Averaging

表 6-44 provides a trade-off comparison of digital averaging mode vs the non-averaged mode (default).

表 6-44. Digital averaging vs full power input bandwidth (–3 dB)

No. of ADCs averaged	Input Bandwidth (-3 dB)	Effective input termination	Noise density	Power/ch (W)
Default	2.3 GHz	100 Ω	-156 dBFS/Hz	1.1
2	2.1 GHz	100 Ω	-159 dBFS/Hz	1.5

Digital averaging improves decorrelated noise contributions by 3 dB per 2x AVG (ideal) while correlated noise does not improve with averaging. Some of the dominant noise sources are correlated (that is, clock jitter (external or first clock input buffer) or power supply noise) while others (that is, ADC thermal noise, clock distribution buffers) are decorrelated.

SNR: When operating close to ADC fullscale, some of the SNR limitation is due to jitter and hence the SNR improvement won't reach 3 dB (2x AVG). As the input fullscale is reduced, the clock jitter contribution to SNR becomes less and the SNR improvement is approaching the ideal 3 dB per 2x AVG. The same phenomenon can be observed when using digital decimation. As the decimation factor increases, the close-in (correlated noise) becomes the more dominating noise unless the input signal amplitude is reduced.

SFDR: The amplitude of low order harmonics (HD2-HD5) and IMD3 typically is similar across ADCs and thus the improvement with averaging is very small.

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6.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI). However, it can operate in a default configuration without requiring the SPI interface. Also, the power down function and the internal and external reference configuration is possible via pin control (PDN/SYNC pin).

6.5.1 GPIO Pin Control

There are several commands which can be executed using SPI programming or GPIO pins. 表 6-45 provides an overview of the commands available using GPIO pins.

表 6-45. GPIO Pin Command Options

FEATURE	DESCRIPTION
JESD SYNC	Support for single ended CMOS or differential LVDS
NCO Control	Fast frequency hopping with 3 different control options
Fast Over Range	GPIO1 indicates over range for channel A and B and GPIO2 for channel C and D. In this mode the over range indication can be made 'sticky' where flag needs to be cleared using SPI commands.
Calibration Freeze	Freezes swapping of calibration ADC

6.5.2 Configuration using the SPI interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to approximately 1 MHz and also with a non-50% SCLK duty cycle.

6.5.2.1 Register Write

The internal registers can be programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

図 6-46 shows the timing requirements for the serial register write operation.

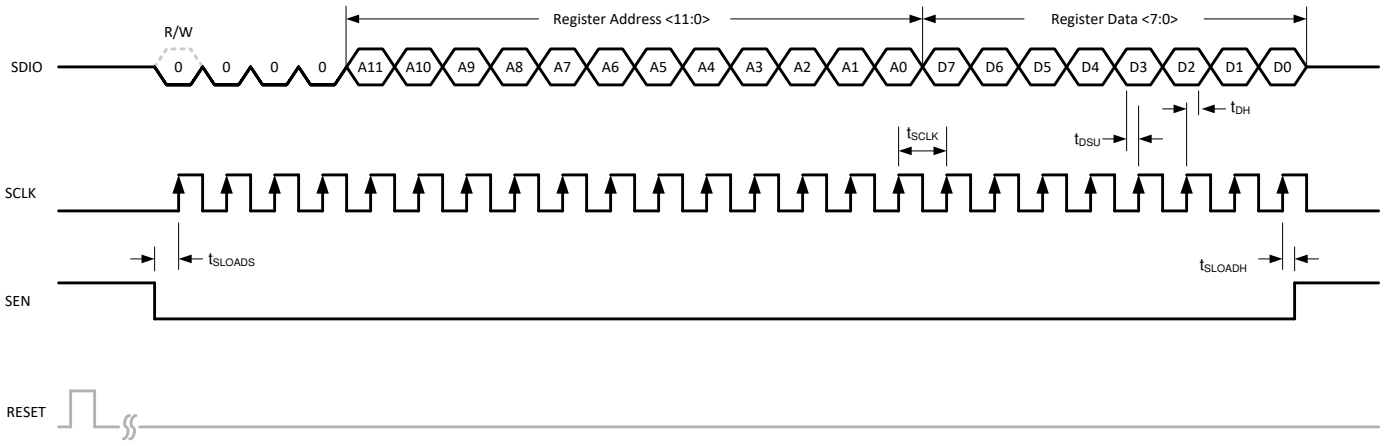

図 6-46. Serial Register Write Timing Diagram

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6.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device outputs the contents (D[7:0]) of the selected register on the SDIO pin
5. The external controller can latch the contents at the SCLK falling edge

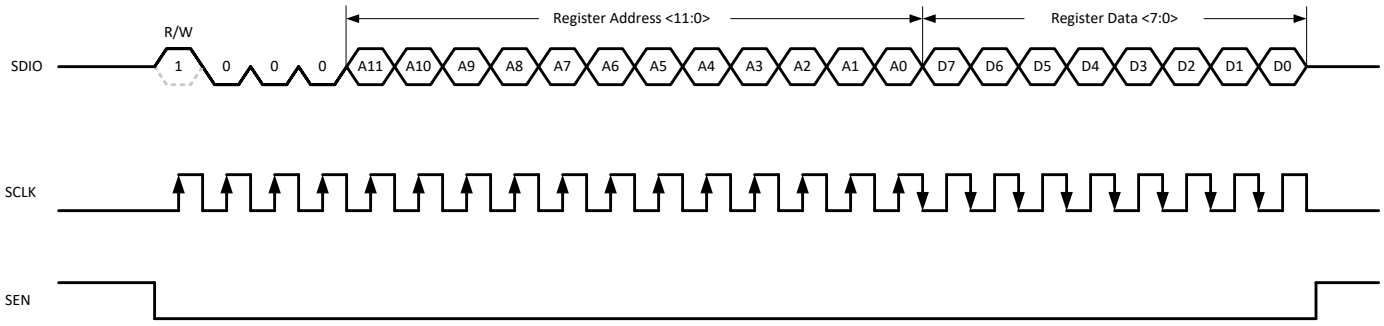

図 6-47. Serial Register Read Timing Diagram

6.6 Register Maps

表 6-46. Register Map Summary

PAGE	REGISTER ADDRESS	REGISTER DATA							
	A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL	0x00	0	0	0	0	0	0	0	RESET
	0x05	0	ANALOG PAGE	CALIB PAGE	DDCCD PAGE	DDCAB PAGE	JESD PAGE	DIGITAL PAGE	0
DIGITAL	0x2C	20-BIT OUT	DDC BAND SEL		0	0	0	DDC REAL	BYP EN
	0x2D	0	DECIMATION			0	0	0	0
	0x2E	0	0	0	0	AVG EN	AVG SEL(1)		OVR ON JESD
	0x33	0	0	0	1	FORMAT	0	GBL PDN	0
	0x34	0	MEM STROBE	MEM CH SEL		0	0	0	0
	0x3B	NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	
	0x41	NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]	
	0x22F	1	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1	SYSREF OR	1
	0x234	0	NCO SEL MODE		0	0	GPIO MODE		
	0X235	NCO SEL SOURCE							
	0x236	0	GPIO2 INV	GPIO1 INV	GPIO SWAP	0	0	SYSREF RESET	SYSREF EN
	0x238	OVR OUTPUT CFG				0	0	0	0
JESD	0x20	K							
	0x21	0	SYNC SPI EN	SYNC SPI	0	0	SYSREF MODE		
	0x22	LMFS MODE							
	0x24	DDC CLK DIV							
	0x25	JESD TX CLK DIV							
	0x27	0	0	DROP LSB	0	0	0	CLK BAL EN	0
	0x28	JESD TX LANE EN							
	0x2B	0	0	0	0	0	0	0	SYNC INV
	0x2D	0	0	0	0	0	TEST SEQ SEL		
	0x2E	RAMP INCR				0	RAMP EN	ALT PAT	0
	0x2F	0	PRBS PAT		PRBS EN	0	0	0	0
	0x53	SCR EN	0	0	0	0	0	0	0
	0x5C	F in ILA							
	0x5D	K in ILA							

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表 6-46. Register Map Summary (続き)

PAGE	REGISTER ADDRESS	REGISTER DATA							
	A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
JESD	0x7A	JESD LANE POL INV							
	0x80	0	LANE DOUT1 SEL			0	LANE DOUT0 SEL		
	0x81	0	LANE DOUT3 SEL			0	LANE DOUT2 SEL		
	0x82	0	LANE DOUT5 SEL			0	LANE DOUT4 SEL		
	0x83	0	LANE DOUT7 SEL			0	LANE DOUT6 SEL		
	0x84	0	0	0	0	0	0	JESD PLL FACTOR	
	0x89	TX EMPH DOUT1 [0]	TX EMPH DOUT0 [5:0]						0
	0x8A	0	0	0	TX EMPH DOUT1 [5:1]				
	0x8B	TX EMPH DOUT3 [0]	TX EMPH DOUT2 [5:0]						0
	0x8C	0	0	0	TX EMPH DOUT3 [5:1]				
	0x8D	TX EMPH DOUT5 [0]	TX EMPH DOUT4 [5:0]						0
	0x8E	0	0	0	TX EMPH DOUT5 [5:1]				
	0x8F	TX EMPH DOUT7 [0]	TX EMPH DOUT6 [5:0]						0
	0x90	0	0	0	TX EMPH DOUT7 [5:1]				
	0x9D	PD DOUT7 [0]	PD DOUT6 [0]	PD DOUT5 [0]	PD DOUT4 [0]	PD DOUT3 [0]	PD DOUT2 [0]	PD DOUT1 [0]	PD DOUT0 [0]
	0x9E	PD DOUT7 [1]	PD DOUT6 [1]	PD DOUT5 [1]	PD DOUT4 [1]	PD DOUT3 [1]	PD DOUT2 [1]	PD DOUT1 [1]	PD DOUT0 [1]
	0x9F	0	JESD PLL1			0	JESD PLL2		
	0xA0	0	JESD PLL INPUT1			0	0	0	0
	0xA1	0	JESD PLL INPUT2			0	0	0	0
	0xA2	0	0	0	0	JESD PLL INPUT3			0
	0xA4..A6	START VALUE JESD RAMP [19:0]							
	0xA8..AA	START VALUE JESD RAMP [19:0]							
	0xAC..AE	START VALUE JESD RAMP [19:0]							
	0xB0..B2	START VALUE JESD RAMP [19:0]							
	0xB4..B6	START VALUE JESD RAMP [19:0]							
	0xB8..BA	START VALUE JESD RAMP [19:0]							
	0xBC..BE	START VALUE JESD RAMP [19:0]							
	0xC0..C2	START VALUE JESD RAMP [19:0]							
	0xC4..C6	START VALUE JESD RAMP [19:0]							
	0xC8..CA	START VALUE JESD RAMP [19:0]							
	0xCC..CE	START VALUE JESD RAMP [19:0]							
	0xD0..D2	START VALUE JESD RAMP [19:0]							
	0xD4..D6	START VALUE JESD RAMP [19:0]							
	0xD8..DA	START VALUE JESD RAMP [19:0]							
	0xDC..DE	START VALUE JESD RAMP [19:0]							
	0xE0..E2	START VALUE JESD RAMP [19:0]							
	0xED	0	0	JESD DDC BYP		0	0	0	0

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表 6-46. Register Map Summary (続き)

PAGE	REGISTER ADDRESS	REGISTER DATA							
	A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
DDCAB/CD	0x100..0x105	NCO1 CHA/C FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x108..0x10D	NCO1 CHA/C FREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x110..0x115	NCO1 CHA/C FREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x118..0x11D	NCO1 CHA/C FREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x120..0x125	NCO2 CHA/C FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x128..0x12D	NCO2 CHA/C FREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x130..0x135	NCO2 CHA/C FREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x138..0x13D	NCO2 CHA/C FREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x140..0x145	NCO1 CHB/D FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x148..0x14D	NCO1 CHB/DFREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x150..0x155	NCO1 CHB/DFREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x158..0x15D	NCO1 CHB/DFREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x160..0x165	NCO2 CHB/DFREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x168..0x16D	NCO2 CHB/DFREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x170..0x175	NCO2 CHB/DFREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x178..0x17D	NCO2 CHB/DFREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
	0x180	0	0	DDC PDN	DDC DITH PDN	REAL DDC	SB/DB DDC	0	NCO MODE
	0x181	0	0	LOAD NCO		0	0	0	0
CALIBRATION	0x34	0	0	0	0	0	AVG SEL(2)		1
	0x45	CAL SPI	CAL GPIO	0	0	1	0	1	0
	0x298	0	0	0	0	CAL STATUS			
ANALOG	0x7B	0	0	TERM AB	0	0	0	0	TERM AB
	0x8B	0	0	TERM CD	0	0	0	0	TERM CD
	0xA8	0	DITHER AMP1				0	0	0
	0xAF	DITHER DIS	0	0	1	0	0	0	0
	0xB1	DITHER DIVIDER							
	0xB4	0	0	0	0	0	0	0	SYSREF AC EN
	0xCD	0	DITH AMP2			0	0	0	0
	0xE6	TX SWING [0]	0	0	0	0	0	0	0
	0xE7	0	0	0	0	0	0	TX SWING [2:1]	

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6.6.1 Detailed Register Description

図 6-48. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-47. Register 0x00 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	RESET	R/W	0	This bit resets all internal registers to the default values. Does not self clear to 0.

図 6-49. Register 0x05

7	6	5	4	3	2	1	0
0	ANALOG PAGE	CALIB PAGE	DDCCD PAGE	DDCAB PAGE	JESD PAGE	DIGITAL PAGE	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-48. Register 0x05 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	ANALOG PAGE	R/W	0	This bit enables access to the ANALOG page 0: ANALOG page access disabled 1: ANALOG page access enabled
5	CALIB PAGE	R/W	0	This bit enables access to the CALIBRATION page 0: CALIBRATION page access disabled 1: CALIBRATION page access enabled
4	DDCCD PAGE	R/W	0	This bit enables access to the DDCCD page. Contents can be written to DDCAB and DDCCD page simultaneously if it is identical. 0: DDCCD page access disabled 1: DDCCD page access enabled.
3	DDCAB PAGE	R/W	0	This bit enables access to the DDCAB page. Contents can be written to DDCAB and DDCCD page simultaneously if it is identical. 0: DDCAB page access disabled 1: DDCAB page access enabled
2	JESD PAGE	R/W	0	This bit enables access to the JESD page 0: JESD page access disabled 1: JESD page access enabled
1	DIGITAL PAGE	R/W	0	This bit enables access to the DIGITAL page 0: DIGITAL page access disabled 1: DIGITAL page access enabled
0	0	R/W	0	Must write 0

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図 6-50. Register 0x2C (DIGITAL page)

7	6	5	4	3	2	1	0
20-BIT OUT	DDC BAND SEL		0	0	0	DDC REAL	BYP EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-49. Register 0x2C Field Descriptions

Bit	Field	Type	Reset	Description
7	20-BIT OUT	R/W	0	This bit enables the 20-bit output mode. It carries the output sample with 20-bit output resolution from the DDC and the sample is filled to 32-bit with 12 trailing 0s. 0: Normal operation 1: 20-bit output mode
6-5	DDC BAND SEL	R/W	00	Selects 1 or 2 DDC per ADC when complex decimation is enabled 0: Single band 1: Dual band 2,3: not used
4-2	0	R	0	Must write 0
1	DDC REAL	R/W	0	This bit enables real decimation filter (NCO = 0). BYP EN (D0) must be set to 0. 0: Complex decimation 1: Real decimation
0	BYP EN	R/W	0	This bit enables DDC bypass mode 0: Decimation filter enabled. Complex decimation by default unless D1 is set 1: Decimation filter bypass

図 6-51. Register 0x2D (DIGITAL page)

7	6	5	4	3	2	1	0
0	DECIMATION			0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-50. Register 0x2D Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-4	DECIMATION	R/W	0	Selects decimation. 0,1: not used 2: Decimation by 4 3: Decimation by 8 4: Decimation by 16 5: Decimation by 32 6: Decimation by 64 7: Decimation by 128
3-0	0	R/W	0	Must write 0

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図 6-52. Register 0x2E (DIGITAL page)

7	6	5	4	3	2	1	0
0	0	0	0	AVG EN	AVG SEL (1)		OVR ON JESD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-51. Register 0x2E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3	AVG EN	R/W	0	This bit enables averaging 0: no average 1: ADC averaging enabled
2-1	AVG SEL (1)	R/W	00	Selects ADC averaging. Also AVG SEL (2) in CALIBRATION page needs to be set. 0: no average 1: 2 ADC average
0	OVR ON JESD	R/W	0	This bit enables to output OVR flag to replace the LSB in the JESD output stream 0: OVR on GPIO 1: OVR replaces LSB on JESD stream

図 6-53. Register 0x33 (DIGITAL page)

7	6	5	4	3	2	1	0
0	0	0	1	FORMAT	0	GBL PDN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-52. Register 0x33 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	1	R/W	0	Must write 1
3	FORMAT	R/W	0	This register bit determines the output data format in DDC bypass mode only. 0: Offset Binary 1: 2s Complement DDC mode only supports 2s complement output format.
2	0	R/W	0	Must write 0
1	GBL PDN	R/W	0	This register bit enables global power down mode 0: normal operation 1: global power down mode enabled
0	0	R/W	0	Must write 0

図 6-54. Register 0x34 (DIGITAL page)

7	6	5	4	3	2	1	0
0	MEM STROBE	MEM CH SEL		0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-53. Register 0x34 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	MEM STROBE	R/W	0	This register enables fast power down mode 0: normal operation 1: fast power down mode enabled

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表 6-53. Register 0x34 Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5-4	MEM CH SEL	R/W	0	This register selects which ADC channel is used to fill up the capture sample buffer. Only 1 channel can be selected at a time and the samples are captured from the ADC core without averaging or decimation. 00: capture memory is filled from chA input 01: capture memory is filled from chB input 10: capture memory is filled from chC input 11: capture memory is filled from chD input
0	0	R/W	0	Must write 0

図 6-55. Register 0x3B (DIGITAL page)

7	6	5	4	3	2	1	0
NCO2 CHB [1:0]		NCO1 CHB [1:0]		NCO2 CHA [1:0]		NCO1 CHA [1:0]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-54. Register 0x3B Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NCO2 CHB [1:0]	R/W	00	This register is used when selecting the NCO frequency for channel B, band 2 with the SPI interface in dual band DDC mode.
5-4	NCO1 CHB [1:0]	R/W	00	This register is used when selecting the NCO1 of channel B with the SPI interface.
3-2	NCO2 CHA [1:0]	R/W	00	This register is used when selecting the NCO frequency for channel A, band 2 with the SPI interface in dual band DDC mode.
1-0	NCO1 CHA [1:0]	R/W	00	This register is used when selecting the NCO1 of channel A with the SPI interface.

図 6-56. Register 0x41 (DIGITAL page)

7	6	5	4	3	2	1	0
NCO2 CHD [1:0]		NCO1 CHD [1:0]		NCO2 CHC [1:0]		NCO1 CHC [1:0]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-55. Register 0x41 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NCO2 CHD [1:0]	R/W	00	This register is used when selecting the NCO frequency for channel D, band 2 with the SPI interface in dual band DDC mode.
5-4	NCO1 CHD [1:0]	R/W	00	This register is used when selecting the NCO1 of channel D with the SPI interface.
3-2	NCO2 CHC [1:0]	R/W	00	This register is used when selecting the NCO frequency for channel C, band 2 with the SPI interface in dual band DDC mode.
1-0	NCO1 CHC [1:0]	R/W	00	This register is used when selecting the NCO1 of channel C with the SPI interface.

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図 6-57. Register 0x22F (DIGITAL page)

7	6	5	4	3	2	1	0
1	SYSREF X5	SYSREF X4	SYSREF X3	SYSREF X2	SYSREF X1	SYSREF OR	1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-56. Register 0x22F Field Descriptions

Bit	Field	Type	Reset	Description
7	1	R/W	1	Must write 1
6-2	SYSREF X1..5	R/W	0	These bits are the XOR flags from the SYSREF window monitoring circuitry. The sampling clock gets delayed internally by ~ 160 ps and used to capture the SYSREF signal. If a SYSREF signal transition happens within +/- 50 ps of the SYSREF capture the appropriate XOR flag gets raised. These bits are not sticky - they get overwritten with the next SYSREF rising edge. X1: Window from 110 ps to 135 ps after the rising sampling clock edge X2: Window from 135 ps to 160 ps after the rising sampling clock edge X3: Window from 160 ps to 176 ps after the rising sampling clock edge X4: Window from 176 ps to 192 ps after the rising sampling clock edge X5: Window from 192 ps to 208 ps after the rising sampling clock edge 0: No SYSREF transition detected 1: SYSREF transition detected within given window
1	SYSREF OR	R/W	0	This bit is the output of the five SYSREF XOR flags logically OR'ed together. 0: no SYSREF flag raised 1: one of the five SYSREF XOR flags is raised.
0	1	R/W	1	Must write 1

図 6-58. Register 0x234 (DIGITAL page)

7	6	5	4	3	2	1	0
0	NCO SEL MODE		0	0	GPIO MODE		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-57. Register 0x234 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-5	NCO SEL MODE	R/W	00	These bits select control of the NCO selection in complex decimation. 0: NCO selection using GPIO pins (GPIO MODE (D2-D0) needs to be set accordingly) 2: GPIO1/2 pins are used as a fast serial interface to only up NCO selection for each digital mixer others: not used
4-3	0	R/W	0	Must write 0
2-0	GPIO MODE	R/W	000	This register sets the functionality of the two GPIO pins 0: GPIO pins are used as SYNC input (LVDS), GPIO1 = SYNCP, GPIO2 = SYNCM 1: GPIO1 is used as SYNC input (CMOS) 3: Both GPIO pins are used to select NCOs for the decimation filters 4: GPIO1 is used to disable the calibration 5: GPIO1 is used as start of SYSREF counter others: not used

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図 6-59. Register 0x235 (DIGITAL page)

7	6	5	4	3	2	1	0
NCO SEL SOURCE							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-58. Register 0x235 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO SEL SOURCE	R/W	0	This register works in conjuction with NCO SEL MODE (0x234). 0x00: NCO selection other than regular SPI (GPIO, Fast SPI, and so on) 0xFF: NCO selection using regular SPI with addresses 0x3B/41.

図 6-60. Register 0x236 (DIGITAL page)

7	6	5	4	3	2	1	0
0	GPIO2 INV	GPIO1 INV	GPIO SWAP	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-59. Register 0x236 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	GPIO2 INV	R/W	0	This bit inverts polarity of the GPIO2 pin 0: Polarity as is 1: Polarity inverted
5	GPIO1 INV	R/W	0	This bit inverts polarity of the GPIO1 pin 0: Polarity as is 1: Polarity inverted
4	GPIO SWAP	R/W	0	This bit swaps GPIO1 and GPIO2 pins internally. 0: Normal operation 1: GPIO1 and GPIO2 are swapped
3-0	0	R/W	0	Must write 0

図 6-61. Register 0x238 (DIGITAL page)

7	6	5	4	3	2	1	0
OVR OUTPUT CFG				0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-60. Register 0x238 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OVR OUTPUT CFG	R/W	0000	This bit configures if the overrange indication (OVR) is output on JESD output stream or on GPIO pins 0000: OVR on JESD 1111: OVR on GPIO
3-0	0	R/W	0	Must write 0

図 6-62. Register 0x20 (JESD page)

7	6	5	4	3	2	1	0
K							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-61. Register 0x20 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	K	R/W	00000000	This is JESD204B parameter K which sets number of frames in a multi-frame. Bit value is set as K minus 1.

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図 6-63. Register 0x21 (JESD page)

7	6	5	4	3	2	1	0
0	SYNC SPI EN	SYNC SPI	0	0	SYSREF MODE		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-62. Register 0x21 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	SYNC SPI EN	R/W	0	This bit enables JESD SYNC control using SPI (ignoring SYNC using GPIO1/2 pins) using bit D5 (SYNC SPI). 0: SPI SYNC disabled 1: SPI SYNC (using register bit D5) enabled
5	SYNC SPI	R/W	0	This bit enables JESD SYNC. SYNC control via SPI must be enabled also (D6). 0: ADC outputs data (SYNC disabled) 1: SYNC enabled (ADC outputs K28.5 characters for JESD interface synchronization)
4-3	0	R/W	0	Must write 0
2-0	SYSREF MODE	R/W	000	This register controls how the ADC processes incoming SYSREF pulses. 0: Ignore all SYSREF pulses 1: Use all SYSREF pulses 2: Don't use SYSREF pulses 3: Skip one SYSREF pulse then use only the next one 4: Skip one SYSREF pulse then use all pulses 5: Skip two SYSREF pulses and then use one 6: Skip two SYSREF pulses and then use all

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図 6-64. Register 0x22 (JESD page)

7	6	5	4	3	2	1	0
JESD MODE							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-63. Register 0x22 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	JESD MODE	R/W	00000000	This register sets the LMFS configuration 2: LMFS = 8-4-8-10 (also bit DROP LSB in 0x27 needs to be set) 3: LMFS = 8-4-2-2 4: LMFS = 8-16-4-1 5: LMFS = 4-16-8-1 6: LMFS = 2-16-16-1 7: LMFS = 1-16-32-1 8: LMFS = 8-8-2-1 9: LMFS = 4-8-4-1 10: LMFS = 2-8-8-1 11: LMFS = 1-8-16-1 12: LMFS = 4-4-2-1 13: LMFS = 2-4-4-1 14: LMFS = 1-4-8-1 18: LMFS = 8-16-8-1 (20-bit output) 19: LMFS = 4-16-16-1 (20-bit output) 20: LMFS = 2-16-32-1 (20-bit output) 21: LMFS = 1-16-64-1 (20-bit output) 22: LMFS = 8-8-4-1 (20-bit output) 23: LMFS = 4-8-8-1 (20-bit output) 24: LMFS = 2-8-16-1 (20-bit output) 25: LMFS = 1-8-32-1 (20-bit output) 26: LMFS = 4-4-4-1 (20-bit output) 27: LMFS = 2-4-8-1 (20-bit output) 28: LMFS = 1-4-16-1 (20-bit output) others: not used

図 6-65. Register 0x24 (JESD page)

7	6	5	4	3	2	1	0
DDC CLK DIV							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-64. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DDC CLK DIV	R/W	00000000	This register sets the internal clock divider when using the decimation filter. See 表 6-66

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図 6-66. Register 0x25 (JESD page)

7	6	5	4	3	2	1	0
JESD TX CLK DIV							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-65. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD TX CLK DIV	R/W	0000000	This register sets the internal clock divider for the selected LMFS output mode. See 表 6-66 and 表 6-67

表 6-66. Register settings for 0x24/0x25 based on bypass/decimation and LMFS mode (16-bit output)

	0x24 (DDC CLK DIV)							0x25 (JESD TX CLK DIV)						
LMFS	BYP	/4	/8	/16	/32	/64	/128	BYP	/4	/8	/16	/32	/64	/128
8-4-8-10	1							4						
8-4-2-2	1	0	0					0	1	1				
4-4-2-1	3	0	0	0	0			0	0	0	0	0		
8-8-2-1		0	0	0	0	0			0	0	0	0	0	
8-16-4-1			1	1	1	1	1			0	0	0	0	0
4-8-4-1		1	1	1	1	1	1		0	0	0	0	0	0
4-16-8-1			3	3	3	3	3			0	0	0	0	0
2-4-4-1		1	1	1	1	1	1		0	0	0	0	0	0
2-8-8-1			3	3	3	3	3			0	0	0	0	0
2-16-16-1				7	7	7	7				0	0	0	0
1-4-8-1			3	3	3	3	3			0	0	0	0	0
1-8-16-1				7	7	7	7				0	0	0	0
1-16-32-1					15	15	15					0	0	0

表 6-67. Register settings for 0x24/0x25 based on decimation and LMFS mode (20-bit output)

	0x24 (DDC CLK DIV)						0x25 (JESD TX CLK DIV)					
LMFS	/4	/8	/16	/32	/64	/128	/4	/8	/16	/32	/64	/128
4-4-4-1	1	1	1	1			0	0	0	0		
8-8-4-1	1	1	1	1	1	1	0	0	0	0	0	0
8-16-8-1		3	3	3	3	3		0	0	0	0	0
4-8-8-1	3	3	3	3	3	3	0	0	0	0	0	0
4-16-16-1		7	7	7	7	7		0	0	0	0	0
2-4-8-1	3	3	3	3	3	3	0	0	0	0	0	0
2-8-16-1		7	7	7	7	7	0	0	0	0	0	0
2-16-32-1			15	15	15	15			0	0	0	0
1-4-16-1		7	7	7	7	7		0	0	0	0	0
1-8-32-1			15	15	15	15			0	0	0	0
1-16-64-1				31	31	31		0	0	0	0	0

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図 6-67. Register 0x27 (JESD page)

7	6	5	4	3	2	1	0
0	0	DROP LSB	0	0	0	CLK BAL EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-68. Register 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	DROP LSB	R/W	0	This register needs to be set when using the 12-bit output LMFS mode. 0: Drop LSB disabled 1: Drop LSB enabled when using LMFS = 8-4-8-10
4-2	0	R/W	0	Must write 0
1	CLK BAL EN	R/W	0	This register bit needs to be enabled in bypass mode LMFS = 8-4-2-2 only to improve internal clock balancing. 0: CLK BAL disabled 1: CLK BAL EN. Set for LMFS = 8-4-2-2
0	0	R/W	0	Must write 0

図 6-68. Register 0x28 (JESD page)

7	6	5	4	3	2	1	0
JESD LANE EN							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-69. Register 0x28 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD LANE EN	R/W	11111111	This register turns on individual output lanes 0: Lane powered down 1: Serdes lane enabled D0: Lane DOUT0 D1: Lane DOUT1 ... D7: Lane DOUT7

図 6-69. Register 0x2B (JESD page)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SYNC INV
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-70. Register 0x2B Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	SYNC INV	R/W	0	This register inverts the polarity from external SYNC pin 0: Polarity as is 1: Polarity inverted

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図 6-70. Register 0x2D (JESD page)

7	6	5	4	3	2	1	0
0	0	0	0	0	JESD SEQ SEL		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-71. Register 0x2D Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0
2-0	JESD SEQ SEL	R/W	000	This register selects the JESD test pattern sequence 0: Test sequence disabled 1: Repeat D21.5 high frequency pattern for random jitter (RJ) 2: Repeat K28.5 mixed frequency pattern for deterministic jitter (DJ) 3: Repeat initial lane alignment (ILA) sequence 4: Modified random pattern 5: Scrambled jitter pattern 6: Repeat K28.7 low frequency pattern 7: Short test pattern

図 6-71. Register 0x2E (JESD page)

7	6	5	4	3	2	1	0
RAMP INCR				0	RAMP EN	ALT PAT	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-72. Register 0x2E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RAMP INCR	R/W	0000	This register value sets the increment step size for the ramp pattern on 16-bit output. The step size is RAMP INCR plus 1.
3	0	R/W	0	Must write 0
2	RAMP EN	R/W	0	Enables RAMP output pattern in the TRANSPORT LAYER.
1	ALT PAT	R/W	0	Enables a toggle pattern switching between 0x0000 and 0xFFFF in the TRANSPORT LAYER
0	0	R/W	0	Must write 0

図 6-72. Register 0x2F (JESD page)

7	6	5	4	3	2	1	0
0	SERDES PRBS		SERDES PRBS EN	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-73. Register 0x2F Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-5	SERDES PRBS	R/W	0	This register selects the PRBS pattern in the LINK LAYER (no 8b/10b encoding). PRBS pattern must be enabled (D4). 0: PRBS 2^{7}-1 1: PRBS 2^{15}-1 2: PRBS 2^{23}-1 3: PRBS 2^{31}-1
4	SERDES PRBS EN	R/W	0	This register enables PRBS test pattern in the LINK LAYER 0: Test pattern mode disabled 1: PRBS test pattern mode enabled
3-0	0	R/W	0	Must write 0

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図 6-73. Register 0x53 (JESD page)

7	6	5	4	3	2	1	0
SCR EN	0	0	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-74. Register 0x53 Field Descriptions

Bit	Field	Type	Reset	Description
7	SCR EN	R/W	0	Enables scrambling of the JESD output data 0: Output scrambling disabled 1: Output scrambling enabled
6-0	0	R/W	0	Must write 0

図 6-74. Register 0x5C (JESD page)

7	6	5	4	3	2	1	0
F in ILA							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-75. Register 0x5C Field Descriptions

Bit	Field	Type	Reset	Description
7-0	F in ILA	R/W	0	These bits set F in the ILA sequence. Register value is actual F value -1 (0x01 = F(2)).

図 6-75. Register 0x5D (JESD page)

7	6	5	4	3	2	1	0
K in ILA							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-76. Register 0x5D Field Descriptions

Bit	Field	Type	Reset	Description
7-0	K in ILA	R/W	0	These bits set K in the ILA sequence. Register value is actual K value -1 (0x0F = K(15))

図 6-76. Register 0x7A (JESD page)

7	6	5	4	3	2	1	0
JESD LANE POL INV							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-77. Register 0x7A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD LANE POL INV	R/W	00000000	This register inverts the polarity of the individual SERDES output lanes. Register bit D0 corresponds to SERDES lane DOUT0, D1 to DOUT1, and so on 0: Output polarity as is 1: Output polarity inverted

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図 6-77. Register 0x80/81/82/83 (JESD page)

ADDR	7	6	5	4	3	2	1	0
0x80	0	LANE DOUT1 SEL			0	LANE DOUT0 SEL		
0x81	0	LANE DOUT3 SEL			0	LANE DOUT2 SEL		
0x82	0	LANE DOUT5 SEL			0	LANE DOUT4 SEL		
0x83	0	LANE DOUT7 SEL			0	LANE DOUT6 SEL		
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-78. Register 0x80/81/82/83 Field Descriptions

Bit	Field	Type	Reset	Description
7,3	0	R/W	0	Must write 0
6-4	LANE DOUT1/3/5/7 SEL	R/W	000	These register bits control the output mux. Any physical serdes output lane (DOUTx) can be connected to any JESD digital stream. By default, lane DOUT0 is connected to JESD stream 0, lane DOUT1 to JESD stream 1, and so on. 0: JESD stream 0 1: JESD stream 1 ... 7: JESD stream 7
2-0	LANE DOUT0/2/4/6 SEL	R/W	000	

図 6-78. Register 0x84 (JESD page)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	JESD PLL FACTOR	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-79. Register 0x84 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1-0	JESD PLL FACTOR	R/W	00	This register bit must be set for 12-bit output LMFS = 8-4-8-10 only. 0: all other JESD LMFS modes 1: Set for LMFS = 8-4-8-10

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図 6-79. Register 0x89/8A/8B/8C/8D/8E/8F/90 (JESD page)

7	6	5	4	3	2	1	0
TX EMPH DOUT1 [0]	TX EMPH DOUT0 [5:0]						0
0	0	0	TX EMPH DOUT1 [5:1]				
TX EMPH DOUT3 [0]	TX EMPH DOUT2 [5:0]						0
0	0	0	TX EMPH DOUT3 [5:1]				
TX EMPH DOUT5 [0]	TX EMPH DOUT4 [5:0]						0
0	0	0	TX EMPH DOUT5 [5:1]				
TX EMPH DOUT7 [0]	TX EMPH DOUT6 [5:0]						0
0	0	0	TX EMPH DOUT7 [5:1]				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-80. Register 0x89/8A/8B/8C/8D/8E/8F/90 Field Descriptions

Bit	Field	Type	Reset	Description
7-5,0	0	R/W	0	Must write 0
6-1	TX EMPH DOUT0/2/4/6 [5:0]	R/W	000000	These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0: 0 dB 1: –1 dB 3: –2 dB 7: –4.1 dB 15: –6.2 dB 31: –8.2 dB 63: –11.5 dB
4-0,7	TX EMPH DOUT1/3/5/7 [5:0]	R/W	000000	

図 6-80. Register 0x9D/9E (JESD page)

7	6	5	4	3	2	1	0
PD DOUT7 [0,1]	PD DOUT6 [0,1]	PD DOUT5 [0,1]	PD DOUT4 [0,1]	PD DOUT3 [0,1]	PD DOUT2 [0,1]	PD DOUT1 [0,1]	PD DOUT0 [0,1]
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-81. Register 0x9D/9E Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PD DOUTx [0,1]	R/W	0	Register 0x9D and 0x9E allow power down of individual serdes output lanes. Register 0x9D (PD DOUTx [0]) covers the output driver, 0x9E (PD DOUTx [1]) covers the associated internal high-speed data clock. 0: Output lane enabled 1: Output lane powered down

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図 6-81. Register 0x9F (JESD page)

7	6	5	4	3	2	1	0
0	JESD PLL1			0	JESD PLL2		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-82. Register 0x9F Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-4	JESD PLL1	R/W	000	Internal JESD PLL input divider setting. See 表 6-84 how to configure it for the different decimation and LMFS settings.
3	0	R/W	0	Must write 0
2-0	JESD PLL2	R/W	000	Internal JESD PLL input divider setting. See 表 6-85 how to configure it for the different decimation and LMFS settings.

図 6-82. Register 0xA0/A1/A2 (JESD page)

ADDR	7	6	5	4	3	2	1	0
0xA0	0	JESD PLL INPUT1			0	0	0	0
0xA1	0	JESD PLL INPUT2			0	0	0	0
0xA2	0	0	0	0	JESD PLL INPUT3			0
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-83. Register 0xA0/A1/A2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	0	R/W	0	Must write 0
6-4	JESD PLL INPUT1/2	R/W	000	Internal JESD PLL input divider setting. See 表 6-84 (16-bit output) and 表 6-85 (20-bit output) how to configure it for the different decimation and LMFS settings.
3-1	JESD PLL INPUT3	R/W	000	Internal JESD PLL input divider setting. See 表 6-84 (16-bit output) and 表 6-85 (20-bit output) how to configure it for the different decimation and LMFS settings.

表 6-84. Register settings for 0x9F/A0/A1/A2 based on bypass/decimation and LMFS mode and LMFS mode (16-bit output)

	JESD PLL1/2 (0x9F)							JESD PLL INPUT 1/2 (0xA0/A1)							JESD PLL INPUT 3 (0xA2)						
LMFS	BYP	/4	/8	/16	/32	/64	/128	BYP	/4	/8	/16	/32	/64	/128	BYP	/4	/8	/16	/32	/64	/128
8-4-8-10	0							0							1						
8-4-2-2	0	1	2					0	0	1					1	0	0				
4-4-2-1	0	0	1	2	3	4		0	0	1	2	3	4		3	0	0	0	0	0	0
8-8-2-1		0	1	2	3	4	5		0	1	2	3	4	5		0	0	0	0	0	0
8-16-4-1			0	1	2	3	4			0	1	2	3	4			0	0	0	0	0
4-8-4-1		0	0	1	2	3	4		0	0	1	2	3	4		1	0	0	0	0	0
4-16-8-1			0	0	1	2	3			0	0	1	2	3			1	0	0	0	0
2-8-8-1			0	0	1	2	3			0	0	1	2	3			1	0	0	0	0
2-4-4-1		0	0	1	2	3			0	0	1	2	3			1	0	0	0	0	
2-16-16-1				0	0	1	2				0	0	1	2				1	0	0	0
1-8-16-1				0	0	1	2				0	0	1	2				1	0	0	0
1-16-32-1					0	0	1					0	0	1					1	0	0
1-4-8-1			0	0	1	2	3			0	0	1	2	3			1	0	0	0	0

表 6-85. Register settings for 0x9F/A0/A1/A2 based on bypass/decimation and LMFS mode (20-bit output)

	JESD PLL1/2 (0x9F), JESD PLL INPUT 1/2 (0xA0/A1)						JESD PLL INPUT 3 (0xA2)					
LMFS	/4	/8	/16	/32	/64	/128	/4	/8	/16	/32	/64	/128
8-8-4-1	0	0	1	2	3		1	0	0	0	0	
8-16-8-1		0	0	1	2	3		1	0	0	0	0
4-4-4-1	0	0	1	2			1	0	0	0		
4-8-8-1	0	0	0	1	2	3	3	1	0	0	0	0
4-16-16-1		0	0	0	1	2		3	1	0	0	0
2-4-8-1	0	0	0	1	2		3	1	0	0	0	
2-8-16-1		0	0	0	1	2		3	1	0	0	0
2-16-32-1			0	0	0	1			3	1	0	0
1-4-16-1		0	0	0	1	2		3	1	0	0	0
1-8-32-1			0	0	0	1			3	1	0	0
1-16-64-1				0	0	0				3	1	0

図 6-83. Register 0xA4..0xE2 (JESD page)

7	6	5	4	3	2	1	0
START VALUE JESD RAMP [19:0]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-86. Register 0xA4..0xE2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	START VALUE JESD RAMP [19:0]	R/W	00000000	The JESD RAMP test pattern is designed to act as an individual RAMP pattern on each digital stream. See セクション 6.3.7 for detailed examples. Different registers are being used to set RAMP starting values for different operating modes.

図 6-84. Register 0xED (JESD page)

7	6	5	4	3	2	1	0
0	0	JESD DDC BYP		0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-87. Register 0xED Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5-4	JESD DDC BYP	R/W	00	This register needs to be set for the internal JESD frame assembly in DDC bypass output mode: 0: Any DDC mode 1: LMFS = 8-4-2-2 or 8-4-8-10 or 4-4-2-1
3-0	0	R/W	0	Must write 0

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図 6-85. Register 0x100..0x17D (DDCAB/CD page)

7	6	5	4	3	2	1	0
NCOx FREQUENCYx [7:0],[15:8],[23:16],[31:24],[39:32],[47:40]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-88. Register 0x100..0x17D Field Descriptions

Bit	Field	Type	Reset	Description
47:0	NCOx CHA/B/C/D FREQUENCYx	R/W	0	The frequencies for NCOs are located in addresses 0x100 to 0x17D. Each frequency is 48-bit and the MSB starts on the highest address.

図 6-86. Register 0x180 (DDCA/B page)

7	6	5	4	3	2	1	0
0	0	DDC PDN	DDC DITH PDN	REAL DDC	SB/DB DDC	0	NCO MODE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-89. Register 0x180 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	DDC PDN	R/W	0	This bit powers down the DDC mixer and NCO 0: DDC block enabled 1: DDC block powered down
4	DDC DITH PDN	R/W	0	This bit powers down the dither in the DDC digital block 0: DDC dither enabled 1: DDC dither powered down
3	REAL DDC	R/W	0	Set this bit to 1 in real decimation mode to disable the NCO. 0: Complex Decimation 1: Real Decimation
2	SB/DB DDC	R/W	0	This register splits the NCOs for dual band operation. 0: Single Band DDC 1: Dual Band DDC
1	0	R/W	0	Must write 0
0	NCO MODE	R/W	0	This register selects phase coherent or phase continuous operation of the NCO. 0: Phase continuous 1: Phase coherent

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図 6-87. Register 0x181 (DDCAB/CD page)

7	6	5	4	3	2	1	0
0	0	LOAD NCO		0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-90. Register 0x181 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5-4	LOAD NCO	R/W	00	This register loads all the NCO frequencies from the memory to the NCOs. To update the NCO this register has to be set to 3 and back to 0 as shown in 表 6-91
3-0	0	R/W	0	Must write 0

表 6-91. NCO frequency programming example

ADDR	DATA	DESCRIPTION
0x105	0x4E	NCO1 of DDCA: Set frequency to 920 MHz (86,318,992,857,935)which is 0x4E81B4E81B4E starting MSB in 0x105.
0x104	0x81	
0x103	0xB4	
0x102	0xE8	
0x101	0x1B	
0x100	0x4E	
0x180	0x01	Enable phase coherent NCO.
0x181	0x00	Load and update all NCO frequencies
0x181	0x30	

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図 6-88. Register 0x34 (CALIBRATION page)

7	6	5	4	3	2	1	0
0	0	0	0	0	AVG SEL (2)		1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-92. Register 0x34 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0
2-1	AVG SEL (2)	R/W	00	Selects ADC averaging. Also AVG SEL (1) in DIGITAL page needs to be set. 10: no average 11: 2 ADC average 00/01: not used
0	1	R/W	1	Must write 1

図 6-89. Register 0x45 (CALIBRATION page)

7	6	5	4	3	2	1	0
CAL SPI	CAL GPIO	0	0	1	0	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-93. Register 0x45 Field Descriptions

Bit	Field	Type	Reset	Description
7	CAL SPI	R/W	0	This register triggers the calibration using SPI write. It needs to be toggled (0=>1=>0).
6	CAL GPIO	R/W	0	This register triggers the calibration using the GPIO1 pin.
5-4	0	R/W	0	Must write 0
3	1	R/W	1	Must write 1
2	0	R/W	0	Must write 0
1	1	R/W	1	Must write 1
0	0	R/W	0	Must write 0

図 6-90. Register 0x298 (CALIBRATION page)

7	6	5	4	3	2	1	0
0	0	0	0	CAL STATUS			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-94. Register 0x298 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3-0	CAL STATUS	R/W	0000	This register can be used to check if calibration state machine has finished without any errors. A value of 0xE indicates successful calibration.

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図 6-91. Register 0x7B (ANALOG page)

7	6	5	4	3	2	1	0
0	0	TERM AB	0	0	0	0	TERM AB
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-95. Register 0x7B Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5,0	TERM AB	R/W	00	This register sets the internal termination resistor at the analog inputs for channel A and B. 0: 100 ohm differential termination 1: 50 ohm differential termination
4-1	0	R/W	0	Must write 0

図 6-92. Register 0x8B (ANALOG page)

7	6	5	4	3	2	1	0
0	0	TERM CD	0	0	0	0	TERM CD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-96. Register 0x8B Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5,0	TERM CD	R/W	00	This register sets the internal termination resistor at the analog inputs for channel C and D. 0: 100 ohm differential termination 1: 50 ohm differential termination
4-1	0	R/W	0	Must write 0

図 6-93. Register 0xA8 (ANALOG page)

7	6	5	4	3	2	1	0
0	DITH AMP1				0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-97. Register 0xA8 Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-3	DITH AMP1	R/W	0000	This register sets dither amplitude coarse gain. There are two recommended settings: 0000: Amplitude = 0 0011: Amplitude = 3 Here is a list of all the settings: 0000: Amplitude = 0 (smallest) 0001: Amplitude = 1 ... 1110: Amplitude = 14 1111: Amplitude = 15 (largest)
2-0	0	R/W	0	Must write 0

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図 6-94. Register 0xAF (ANALOG page)

7	6	5	4	3	2	1	0
DITHER DIS	0	0	1	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-98. Register 0xAF Field Descriptions

Bit	Field	Type	Reset	Description
7	DITHER DIS	R/W	0	This register disables internal dither. 0: Dither enabled 1: Dither disabled
6-5	0	R/W	0	Must write 0
4	1	R/W	0	Must write 1
3-0	0	R/W	0	Must write 0

図 6-95. Register 0xB1 (ANALOG page)

7	6	5	4	3	2	1	0
DITHER DIVIDER							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-99. Register 0xB1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DITHER DIVIDER	R/W	0	This register sets the dither divider frequency. SPI write is actual -1. For example a divider of 48 is 47 (0x2F). 0x00 (default) is a divide /50

図 6-96. Register 0xB4 (ANALOG page)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SYSREF AC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-100. Register 0xB4 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	SYSREF AC	R/W	0	This register enables external AC coupling of the SYSREF input with internal biasing. 0: External DC coupling with internal 100 Ω termination 1: External AC coupling with internal biasing

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図 6-97. Register 0xCD (ANALOG page)

7	6	5	4	3	2	1	0
0	DITH AMP2			0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-101. Register 0xCD Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6-4	DITH AMP2	R/W	0	This register sets dither amplitude fine gain. There are two recommended settings: 000: Amplitude = 0 100: Amplitude = -4 Here is a list of all the settings: 000: Amplitude = 0 001: Amplitude = 1 010: Amplitude = 2 011: Amplitude = 3 (largest) 100: Amplitude = -4 (smallest) 101: Amplitude = -3 110: Amplitude = -2 111: Amplitude = -1
5-0	0	R/W	0	Must write 0

図 6-98. Register 0xE6/E7 (ANALOG page)

ADDR	7	6	5	4	3	2	1	0
0xE6	TX SWING [0]	0	0	0	0	0	0	0
0xE7	0	0	0	0	0	0	TX SWING [2:1]	
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 6-102. Register 0xE6/E7 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	0	R/W	0	Must write 0
1,0,7	TX SWING [2:0]	R/W	000	This register adjusts the output amplitude on all 8 serdes lanes. 0: 850 mVpp 1: 825 mVpp 2: 800 mVpp 3: 775 mVpp 4: 950 mVpp 5: 925 mVpp 6: 900 mVpp 7: 875 mVpp

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7 Application Information Disclaimer

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7.1 Application Information

The ADC34RF55 can be used in a wide range of applications including radar, frequency domain digitizer and spectrum analyzer, test and communications equipment and software-defined radios (SDRs). The Typical Applications section describe one configuration that meets the needs of a number of these applications.

7.2 Typical Application

7.2.1 Wideband RF Sampling Receiver

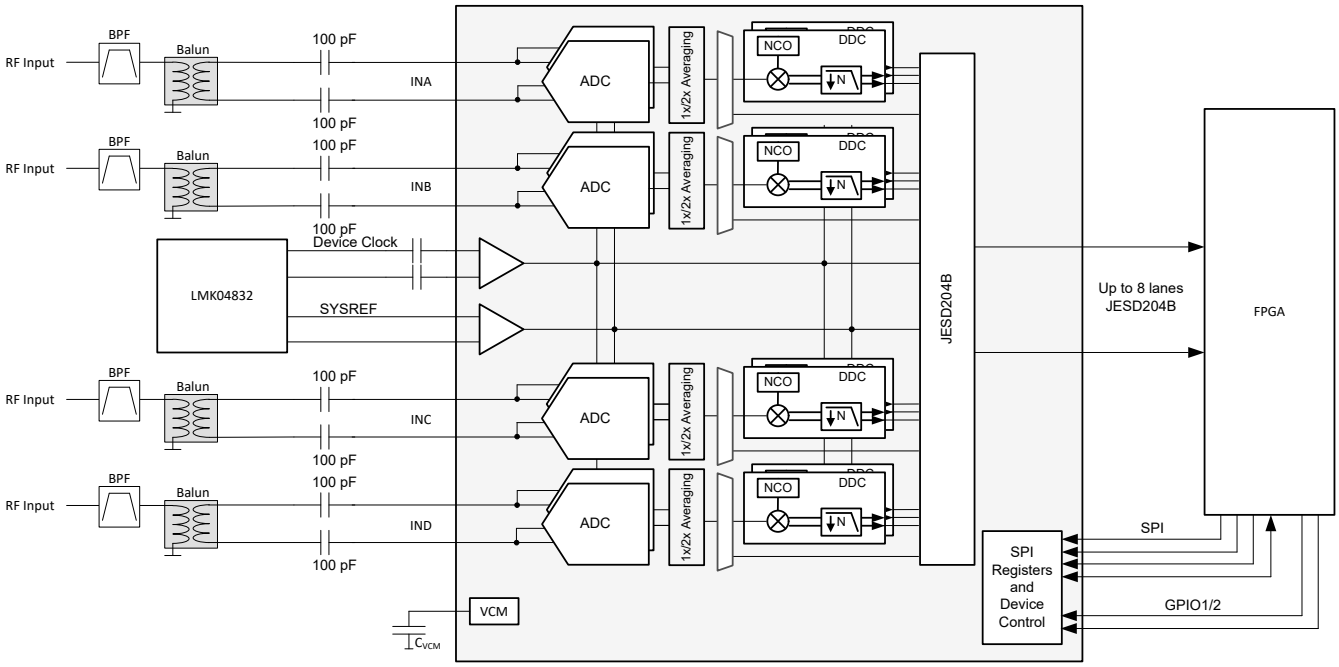

図 7-1. Typical Configuration for Wideband RF Sampling

7.2.2 Design Requirements

7.2.2.1 Input Signal Path

Appropriate band limiting filters must be used to reject unwanted frequencies in the receive signal path.

A 1:2 (for 100 Ω effective termination impedance) or a 1:1 (for 50 Ω effective termination impedance) balun transformer is needed to convert the single ended RF input to differential for input to the ADC. The balun outputs must be AC coupled with 100 pF capacitors. The balun must have good amplitude (< 2 dB) and phase balance (less than 2 deg) within the frequency range of interest. A back-to-back balun configuration often times gives better SFDR performance. 表 7-1 lists a number of recommended baluns for different impedance ratios and frequency ranges.

The S-parameters of the ADC input is used to design the front end matching network.

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表 7-1. Recommended Baluns

PART NUMBER	MANURACTURER(1)	IMPEDANCE RATIO	AMPLITUDE BALANCE (dB)	PHASE BALANCE (°)	FREQUENCY RANGE
BAL-0009SMG	Marki Microwave	1:2	0.6	5	0.5 MHz to 9 GHz
TCM2-43X+	Minicircuits	1:2	0.5	7	10 MHz to 4 GHz
TCM2-33WX+	Minicircuits	1:2	0.7	4	10 MHz to 3 GHz
TC1-1-13M+	Minicircuits	1:1	0.5	2-3	10 MHz to 3 GHz

(1) See the Third-Party Products Disclaimer.

7.2.2.2 Clocking

The ADC34RF55 clock inputs must be AC-coupled to the device to provide the rated performance. The clock source must have low jitter (integrated phase noise) for the ADC to meet the stated SNR performance, especially when operating at higher input frequencies. The clock signal needs to be filtered with a band pass filter to remove some of the broad band clock noise.

The JESD204B data converter system (ADC and FPGA) requires additional SYSREF and device clocks. The LMK04828 or LMK04832 devices are used to generate these clocks. Depending on the ADC clock frequency and jitter requirements, the device can also be used as a system clock synthesizer, or as a device clock and SYSREF distribution device when using multiple ADC34RF5x devices in a system.

7.2.3 Detailed Design Procedure

7.2.3.1 Sampling Clock

To maximize the SNR performance of the ADC a low jitter (< 50 fs) sampling clock is required. 図 7-2 shows the estimated SNR performance vs input frequency vs external clock jitter. The internal ADC aperture jitter also has some dependency to the clock amplitude (gets more sensitive with higher input frequency) as shown in 図 7-3.

When using averaging and/or decimation, the SNR for a single ADC core is estimated first before adding the SNR improvement from internal averaging and/or decimation.

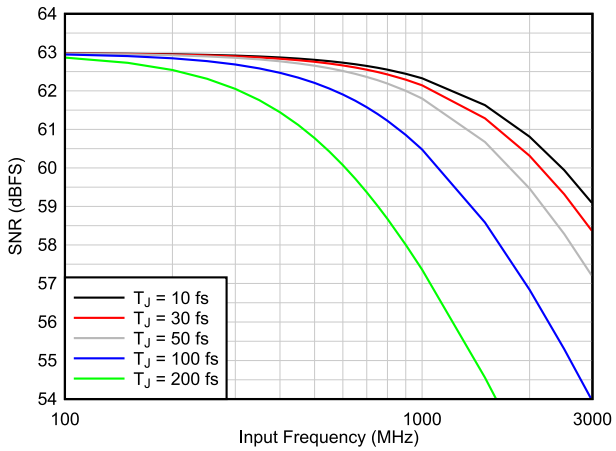

図 7-2. SNR vs T_{Jitter} vs F_{IN} (1x AVG)

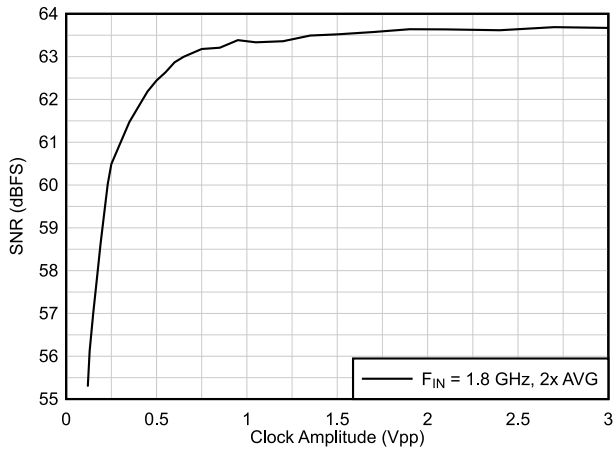

図 7-3. SNR vs Clock Amplitude

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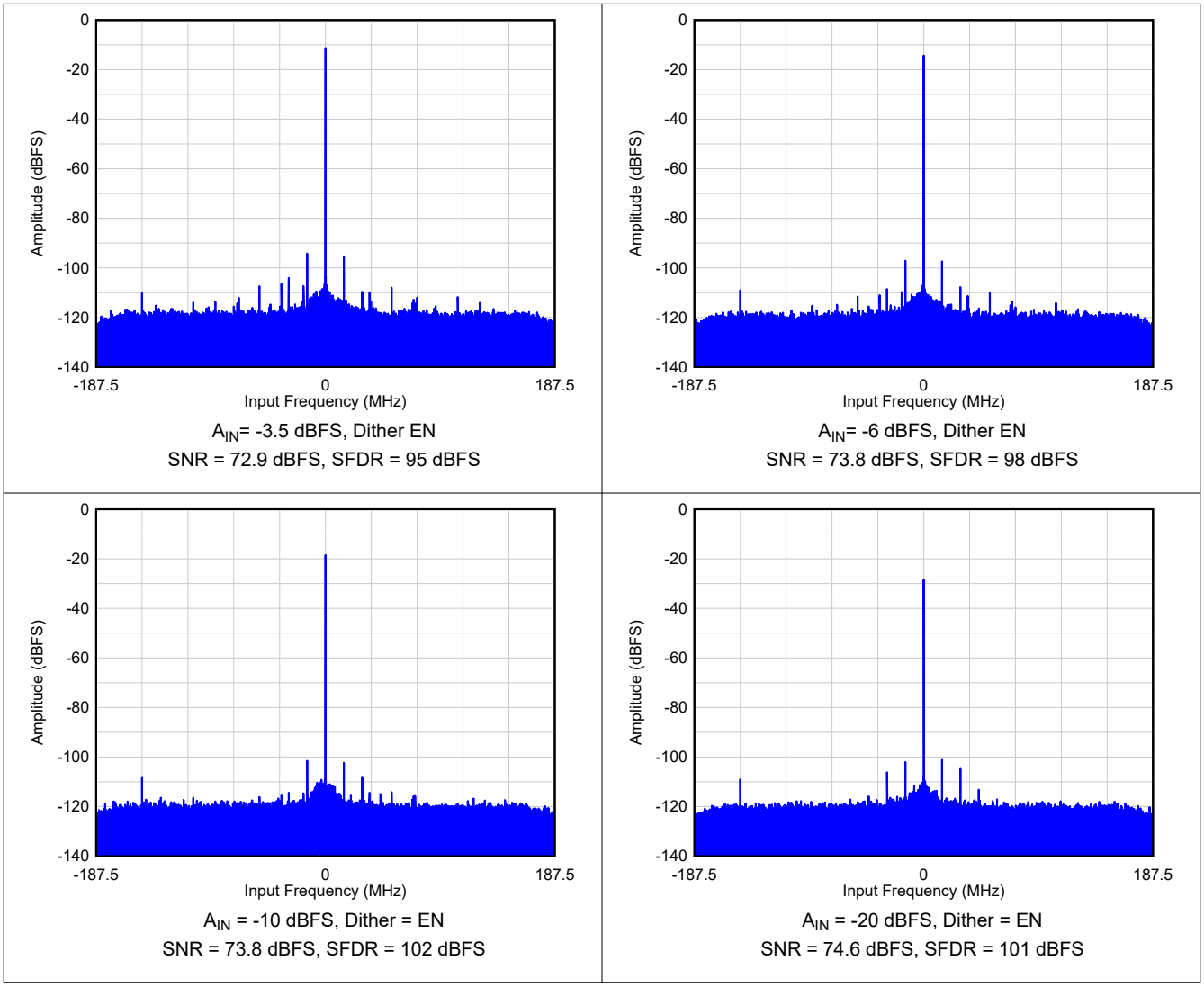
7.2.4 Application Curves

The following application curves demonstrate performance and results only of the ADC using a balun front end and configured to /8 complex decimation (NCO = 900 MHz) without internal averaging. The input frequency is 900 MHz (F_S = 3.0 GSPS) and input amplitudes of -3, -6, -10 and -20 dBFS are shown with dither enabled. The output spectrum is reduced by 6 dB as described in セクション 6.3.5.



A_{IN}= -3.5 dBFS, Dither EN
SNR = 72.9 dBFS, SFDR = 95 dBFS

A_{IN}= -6 dBFS, Dither EN
SNR = 73.8 dBFS, SFDR = 98 dBFS

A_{IN} = -10 dBFS, Dither = EN
SNR = 73.8 dBFS, SFDR = 102 dBFS

A_{IN} = -20 dBFS, Dither = EN
SNR = 74.6 dBFS, SFDR = 101 dBFS

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7.3 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a low pulse on the RESET pin, as shown in 図 7-4.

1. Apply 1.2 V DVDD digital power supply
2. Apply remaining 1.2 V power supplies (AVDD12, CLKVDD), in no specific order
3. Apply 1.8 V AVDD18 power supply
4. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses.
5. Begin programming the internal registers using the SPI interface.

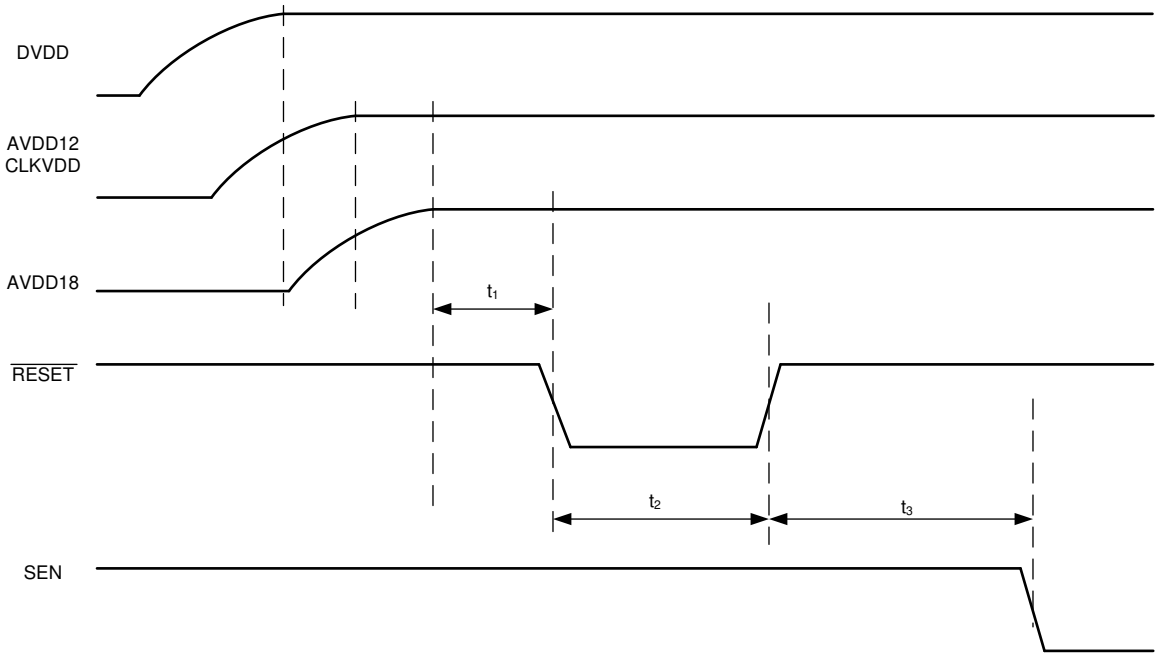

図 7-4. Initialization of serial registers after power up

表 7-2. Power-up timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to active high RESET pulse	1			ms
t_2	Reset pulse width: active low RESET pulse width	100			ns
t_3	Register write delay: delay from RESET disable to SEN active	45k			Clock cycles

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7.3.1 Initial Device Configuration After Power-Up

The following section outlines the sequence of register writes for the device configuration after initial power up.

表 7-3. Summary of programming steps after initial power up

Step	Section	Description
1	RESET	Hardware and software RESET to reset all registers to known state
2	DEVICE CONFIG	Configures the digital operating modes like averaging, test pattern output, input termination, internal dither and decimation.
3	JESD	Configures the JESD204B interface
4	SYSREF	Enables SYSREF input and resets internal circuits based on external SYSREF signal.
5	JESD	Clears and configures some of the JESD registers
6	TRIM	Set trim settings for best analog performance
7	CALIB CONFIG	Configure the calibration settings
8	SYSREF	Issue SYSREF for trim settings to go into effect
9	RUN CALIB	Run power up calibration
10	JESD	Synchronize the JESD interface with the receiver
11	NCO	NCO Configuration

The following section outlines the detailed register writes for the device configuration after initial power up. This includes all the register writes (fields in gray) which are not documented in the register summary table. The register examples are given for 1x internal averaging, Complex decimation /8 single band (LMFS = 8-8-2-1).

7.3.1.1 STEP 1: RESET

After the initial power up both hardware and software reset are required.

表 7-4. Register programming sequence for software RESET

ADDRESS	DATA	DESCRIPTION
0x00	0x01	Software set and reset
0x00	0x00	
0x01	0x00	
0x09	0x20	These two resets are staggered to minimize strain on external power supply.
0x09	0x80	
0x09	0x00	
0x08	0x01	Internal memory reset (set and reset)
0x08	0x00	
0x05	0x40	Select ANALOG page
0x47	0x80	Analog reset (set and reset)
0x47	0x00	

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7.3.1.2 STEP 2: Device Configuration

In this step, the operating mode and digital features (DDC, test pattern) are configured.

表 7-5. Register programming sequence for device configuration

ADDRESS	DATA	DESCRIPTION
0x05	0x20	Select CALIBRATION page
0x34	0x05	Select 2x averaging (1x AVG: 0x05, 2x AVG: 0x07)
0x05	0x02	Select DIGITAL page
0x2C	0x00	Select DDC enable
0x2D	0x30	No decimation, step can be skipped
0x2E	0x09	Select 1x averaging (1x: 0x0B), OVR on JESD
0x23C	0x07	
0x33	0x10	
0x2F	0x99	Select 1x averaging (1x: 0x99, 2x: 0xE1)
0x30	0x99	Select 1x averaging (1x: 0x99, 2x: 0xE1)
0x05	0x40	Select ANALOG page
0x7B/8B	0x00	Select internal input termination (0x00 = 100 ohm)
0xA8	0x00	DITHER AMP1: 3 = 0x80, 0 = 0x00
0xCD	0x00	DITHER AMP2: -4 = 0x40, 0 = 0x00
0x05	0x00	
0x04	0x01	
0x20	0x04	
0x91	0x40	
0xAF	0x10	
0xB1	0x00	Sets dither divider. 0x00 = /50
0xB2	0x00	
0xAF	0x18	
0xAF	0x10	0x10 = dither ENABLED, 0x90 = dither DISABLED
0x04	0x01	
0x20	0x00	
0x04	0x00	
0x05	0x02	
0x363	0x01	
0x05	0x18	Select DDCAB & DDCCD page, load non linearity correction (NLC) trims
0x21D	0x00	
0x21E	0x01	
0x205	0x03	
0x204	0xFF	
0x31D	0x00	
0x31E	0x01	
0x305	0x03	
0x304	0xFF	

Sampling Rate	640 - 2250 MSPS		2250 - 2800 MSPS		2800 - 3000 MSPS	
Nyquist Zone	1st	2nd	1st	2nd	1st	2nd
0x206	0x0E	0x0F	0x27	0x10	0x00	0x00
0x207	0x00	0x00	0x00	0x00	0x00	0x00
0x208	0x00	0x00	0xA6	0x52	0x00	0x00

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表 7-5. Register programming sequence for device configuration (続き)

ADDRESS	DATA	DESCRIPTION				
0x209	0x00	0x00	0x03	0x00	0x00	0x00
0x20A	0xF5	0xF4	0x8D	0x4D	0x00	0x00
0x20B	0x03	0x03	0x00	0x00	0x00	0x00
0x20C	0x27	0x28	0xBD	0xC2	0x00	0x00
0x20D	0x00	0x00	0x03	0x00	0x00	0x00
0x210	0xFC	0F9	0x00	0x00	0x00	0x00
0x211	0x03	0x03	0x00	0x00	0x00	0x00
0x212	0x5F	0xFD	0x00	0x00	0x00	0x00
0x213	0x03	0x03	0x00	0x00	0x00	0x00
0x21A	0x3C	0x3D	0x3C	0x3D	0x3C	0x3D
0x21C	0x00	0x00	0x00	0x00	0x00	0x02
0x223	0xFF	0xFF	0xFF	0xFF	0x00	0x00
0x224	0xFF	0xFF	0xFF	0xFF	0x00	0x00
0x225	0x00	Load NLC				
0x225	0x01					
0x225	0x00					
Sampling Rate	640 - 2250 MSPS		2250 - 2800 MSPS		2800 - 3000 MSPS	
Nyquist Zone	1st	2nd	1st	2nd	1st	2nd
0x306	0x0E	0x0F	0x27	0x10	0x00	0x00
0x307	0x00	0x00	0x00	0x00	0x00	0x00
0x308	0x00	0x00	0xA6	0x52	0x00	0x00
0x309	0x00	0x00	0x03	0x00	0x00	0x00
0x30A	0xF5	0xF4	0x8D	0x4D	0x00	0x00
0x30B	0x03	0x03	0x00	0x00	0x00	0x00
0x30C	0x27	0x28	0xBD	0xC2	0x00	0x00
0x30D	0x00	0x00	0x03	0x00	0x00	0x00
0x310	0xFC	0F9	0x00	0x00	0x00	0x00
0x311	0x03	0x03	0x00	0x00	0x00	0x00
0x312	0x5F	0xFD	0x00	0x00	0x00	0x00
0x313	0x03	0x03	0x00	0x00	0x00	0x00
0x31A	0x3C	0x3D	0x3C	0x3D	0x3C	0x3D
0x31C	0x00	0x00	0x00	0x00	0x00	0x02
0x323	0xFF	0xFF	0xFF	0xFF	0x00	0x00
0x324	0xFF	0xFF	0xFF	0xFF	0x00	0x00
0x325	0x00	Load NLC				
0x325	0x01					
0x325	0x00					
0x20	0x02	OVR MUX EN				
0x203	0x30					
0x303	0x30					
0x180	0x01	Enable coherent NCO mode				

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7.3.1.3 STEP 3: JESD Interface Configuration (1)

In this step, the JESD204B digital interface and parameters are configured.

表 7-6. Register programming sequence for JESD204B interface configuration

ADDRESS	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x81	0x00	
0x80	0xF0	
0x7F	0xFF	
0x7E	0xFF	
0x7D	0xFF	
0x7C	0xFF	
0x7B	0x3B	
0x7A	0x28	
0x79	0x51	
0x78	0x40	
0x05	0x04	Select JESD page
0x23	0x03	Set register to 0x03
0x29	0xFF	Set register to 0xFF
0x20	0x0F	Select K (0x0F: K=15)
0x21	0x01	SYSREF mode
0x22	0x08	Select LMFS configuration (LMFS = 8-8-2-1)
0x24	0x00	Select DDC CLK DIV
0x25	0x00	Select JESD TX CLK DIV
0x26	0x00	
0x27	0x00	
0x53	0x80	Output scrambler EN/DIS (SCR EN = 0x80, SCR DIS = 0x00)
0x5C	0x01	F-1 in ILA (F=2)
0x5D	0x0F	K-1 in ILA (K=15)
0x6E	0x11	
0xA0	0x10	Set JESD PLL INPUT1/2/3
0xA1	0x10	
0xA2	0x00	
0x9F	0x11	Select JESD PLL setting
0x2A	0x0C	
0x23	0x02	JESD INIT toggle
0x23	0x00	

7.3.1.4 STEP 4: SYSREF Synchronization

After device and JESD204B interface configuration, a synchronization using external SYSREF is necessary.

表 7-7. Device synchronization using external SYSREF

ADDRESS	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x236	0x02	Enable internal SYSREF input and clear SYSREF pulse counter
0x236	0x03	Starts SYSREF counter

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7.3.1.5 STEP 5: JESD Interface Configuration (2)

Some registers of the JESD204B interface must be set after the first SYSREF.

表 7-8. Register programming sequence for JESD204B interface configuration

ADDRESS	DATA	DESCRIPTION
0x05	0x04	Select JESD page
0x29	0x00	
0x84	0x00	JESD PLL factor

7.3.1.6 STEP 6: Analog Trim Settings

The following registers need to be set for best analog performance. The register write order is all writes in first 2 columns before moving to the next set of address/data in middle columns, and so on.

表 7-9. Analog Trim Setting Registers

ADDR	DATA	COMMENT	ADDR	DATA	COMMENT	ADDR	DATA	COMMENT
0x05	0x40		0xA8	1x AVG: 0x18 2x AVG: F_S<1.1 GSPS: 0x00 F_S=1.1-1.85 GSPS: 0x08 F_S=1.85-2.6 GSPS: 0x60 F_S=2.6-3.0 GSPS: 0x70		0x56	0x0F	
0xE8	0xF0					0x6E	0x08	
0xE9	0x01					0x102	0x02	
0x4B	0x1F					0x103	0xD9	
0x5B	0x01					0xA7	0x00	
0xEA	0x00		0xCD	0x00		0xA6	0x08	
0xEB	0x03		0xCE	0x00		0x05	0x20	
0x95	0x00		0x100	See 表 7-10 for sample rate dependent trim registers		0xC9	0x09	
0xFC	0x28		0x101			0x102	0xFE	
0xE0	0x8E		0x104			0x103	0x03	
0xE1	0x03		0x105			0x104	0xD4	
0x4C	0x40		0x107	0x10		0x105	0x03	
0x4E	0x01		0x05	0x20		0x106	0xFE	
0x4E	0x00		0x30	0xE8		0x107	0x03	
0xA1	0x01		0x31	0xFF		0x108	0xBC	
0xF8	0x00		0x30	0x08		0x109	0x1A	
0x31	0x20		0x31	0x80		0x101	0x01	
0xFD	0x1C		0x32	0x03		0x159	0x63	
0xAA	0x02		0x05	0x02		0x05	0x40	
0x4D	0x80		0x243	0x02		0x31	0x00	
0xB3	0x30		0x05	0x20		0x4D	0x00	
0x64	0x10		0x36	0x04		0x62	0x10	
0x62	0x12		0x1E8	0x00		0x56	0x0E	
0xFE	0x80		0x1E9	0x00		0x56	0x0C	
0xFC	0x28		0x1F8	0x01		0x56	0x08	
0xFF	0x14		0x1FC	0x0A		0x56	0x00	
0x106	0x00		0x1F0	0x20		0x6E	0x00	
0x107	0x00		0x1F1	0x0C		0xF8	0x06	
0x3D	0x06	Only for F_S> 2.9 GSPS	0x05	0x40		0x102	0x42	Only for F_S> 2.9 GSPS
0x104	0x60		0x39	0x40				
0xB0	0x00		0x56	0x01				
0xB1	0x03		0x56	0x03				

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表 7-9. Analog Trim Setting Registers (続き)

ADDR	DATA	COMMENT	ADDR	DATA	COMMENT	ADDR	DATA	COMMENT
0x3B	0x0C	Only for F_S < 2.9 GSPS	0x56	0x07				

表 7-10. Sample rate dependent trim registers

F_S (GSPS)	0x100	0x101	0x104	0x105
0.6-0.7	0x48	0x00	0x01	0x01
0.7-0.9	0xC8	0x01	0x81	0x00
0.9-1.1	0x48	0x01	0x81	0x00
1.1-1.3	0xC8	0x00	0x81	0x00
1.3-1.5	0x48	0x00	0x81	0x00
1.5-1.7	0xC8	0x01	0x01	0x00
1.7-1.9	0x48	0x01	0x01	0x00
1.9-2.1	0xC8	0x00	0x01	0x00
2.1-2.3	0x48	0x00	0x01	0x00
2.3-2.5	0xC8	0x01	0x81	0x03
2.5-2.7	0x48	0x01	0x81	0x03
2.7-2.9	0xC8	0x00	0x81	0x03
2.9-3.0	0x48	0x00	0xE1	0x03

7.3.1.7 STEP 7: Calibration Configuration

The following registers configure the internal foreground calibration. The register writes need to be written in the order indicated by *Write #*.

表 7-11. Calibration Register Settings

WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA
1	0x05	0x40	63	0xFC	0x13	125	0x47	0xC7
2	0x68	0xC0	64	0xFD	0x08	126	0x46	0x13
3	0x69	0xFF	65	0x36	0x04	127	0xFC	0x13
4	0x05	0x20	66	0x36	0x05	128	0xFD	0x00
5	0x46	0x03	67	0x36	0x04	129	0x36	0x04
6	0x47	0xC2	68	0xFC	0x13	130	0x36	0x05
7	0x46	0x13	69	0xFD	0x0A	131	0x36	0x04
8	0x1AE	0x00	70	0x36	0x04	132	0xFC	0x13
9	0x1E6	0x1C	71	0x36	0x05	133	0xFD	0x02
10	0x1AE	0x00	72	0x36	0x04	134	0x36	0x04
11	0x1E6	0x1C	73	0xFC	0x13	135	0x36	0x05
12	0x1E9	0x08	74	0xFD	0x0C	136	0x36	0x04
13	0x1E9	0xA8	75	0x36	0x04	137	0xFC	0x13
14	0x1E8	0x02	76	0x36	0x05	138	0xFD	0x04
15	0x1E8	0x06	77	0x36	0x04	139	0x36	0x04
16	0x1E8	0x04	78	0xFC	0x13	140	0x36	0x05
17	0x1E8	0x00	79	0xFD	0x0E	141	0x36	0x04
18	0x1E9	0xA0	80	0x36	0x04	142	0xFC	0x13
19	0x1F0	0x28	81	0x36	0x05	143	0xFD	0x06
20	0x1F1	0x0C	82	0x36	0x04	144	0x36	0x04
21	0x1F0	0x2A	83	0xFC	0x03	145	0x36	0x05
22	0x1F0	0x2E	84	0x36	0x04	146	0x36	0x04

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表 7-11. Calibration Register Settings (続き)

WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA
23	0x1F0	0x2C	85	0x46	0x03	147	0xFC	0x13
24	0x1F0	0x28	86	0x47	0xC0	148	0xFD	0x08
25	0x1F0	0x08	87	0x46	0x13	149	0x36	0x04
26	0x1F0	0x18	88	0x46	0x03	150	0x36	0x05
27	0x1F0	0x38	89	0x47	0xC7	151	0x36	0x04
28	0x1F1	0x0C	90	0x46	0x13	152	0xFC	0x13
29	0x1F0	0x3A	91	0x1AE	0x00	153	0xFD	0x0A
30	0x1F0	0x3E	92	0x1E6	0x1C	154	0x36	0x04
31	0x1F0	0x3C	93	0x1AE	0x00	155	0x36	0x05
32	0x1F0	0x38	94	0x1E6	0x1C	156	0x36	0x04
33	0x1F0	0x18	95	0x1E9	0xA8	157	0xFC	0x13
34	0x1F0	0x10	96	0x1E8	0x02	158	0xFD	0x0C
35	0x1AE	0x00	97	0x1E8	0x06	159	0x36	0x04
36	0x1E6	0x1C	98	0x1E8	0x04	160	0x36	0x05
37	0x1AE	0x00	99	0x1E8	0x00	161	0x36	0x04
38	0x1E6	0x1C	100	0x1E9	0xA0	162	0xFC	0x13
39	0x47	0xC0	101	0x1F0	0x18	163	0xFD	0x0E
40	0x46	0x03	102	0x1F0	0x08	164	0x36	0x04
41	0x47	0xC2	103	0x1F0	0x28	165	0x36	0x05
42	0x46	0x13	104	0x1F1	0x0C	166	0x36	0x04
43	0xFC	0x13	105	0x1F0	0x2A	167	0xFC	0x03
44	0xFD	0x00	106	0x1F0	0x2E	168	0x36	0x04
45	0x36	0x04	107	0x1F0	0x2C	169	0x46	0x03
46	0x36	0x05	108	0x1F0	0x28	170	0x47	0xC0
47	0x36	0x04	109	0x1F0	0x08	171	0x46	0x13
48	0xFC	0x13	110	0x1F0	0x18	172	0x05	0x40
49	0xFD	0x02	111	0x1F0	0x38	173	0x68	0x40
50	0x36	0x04	112	0x1F1	0x0C	174	0x69	0xFD
51	0x36	0x05	113	0x1F0	0x3A	175	0x69	0xF5
52	0x36	0x04	114	0x1F0	0x3E	176	0x69	0xD5
53	0xFC	0x13	115	0x1F0	0x3C	177	0x69	0x55
54	0xFD	0x04	116	0x1F0	0x38	178	0x68	0x00
55	0x36	0x04	117	0x1F0	0x18	179	0x69	0x54
56	0x36	0x05	118	0x1F0	0x10	180	0x69	0x50
57	0x36	0x04	119	0x1AE	0x00	181	0x69	0x40
58	0xFC	0x13	120	0x1E6	0x1C	182	0x69	0x00
59	0xFD	0x06	121	0x1AE	0x00	183	0x93	0x0E
60	0x36	0x04	122	0x1E6	0x1C	184	0x94	0x70
61	0x36	0x05	123	0x47	0xC0	185	0x94	0x77
62	0x36	0x04	124	0x46	0x03			

7.3.1.8 STEP 8: SYSREF Synchronization

After setting the analog trim registers, a synchronization using external SYSREF is necessary.

表 7-12. Device synchronization using external SYSREF

ADDRESS	DATA	DESCRIPTION
0x05	0x02	Select DIGITAL page
0x236	0x02	Enable internal SYSREF input and clear SYSREF pulse counter
0x236	0x03	Starts SYSREF counter

7.3.1.9 STEP 9: Run Power up Calibration

The following registers start the power up foreground calibration. The register writes need to be written in the order indicated by *Write #*.

表 7-13. Calibration Register Settings

WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA
1	0x05	0x20	62	0xC9	0x06	123	0xAA	0x80
2	0xE7	0x01	63	0x38	0x01	124	0xAC	0x80
3	0x174	0x02	64	0x110	0x10	125	0xAD	0x80
4	0x178	0x00	65	0x111	0x42	126	0xAD	0x90
5	0x17C	0x22	66	0x112	0xA6	127	0xAD	0xA0
6	0x3C	0x00	67	0x112	0xD6	128	0xAD	0xB0
7	0xFC	0x03	68	0x113	0xBB	129	0xAD	0xC0
8	0xFD	0x00	69	0x113	0xDB	130	0xAD	0xD0
9	0x154	0x1C	70	0x114	0xF4	131	0xAD	0xE0
10	0x155	0x03	71	0x114	0x64	132	0xA0	0x00
11	0xFC	0x03	72	0x115	0x0E	133	0xA2	0x00
12	0xEE	0x26	73	0x115	0xFE	134	0xA4	0x00
13	0xEF	0x02	74	0x116	0x0D	135	0xA6	0x00
14	0x18C	0x88	75	0x116	0xDD	136	0xA8	0x00
15	0xAE	0xC8	76	0x117	0x0D	137	0xAA	0x00
16	0xAF	0x00	77	0x117	0xDD	138	0xAC	0x00
17	0xB0	0x4C	78	0x46	0x03	139	0xAD	0x00
18	0xB1	0x3F	79	0x3D	0x00	140	0x9D	0x45
19	0x4F	0x46	80	0x45	0x0A	141	0x9D	0x05
20	0x50	0x2C	81	0x46	0x02	142	0x20	0x00
21	0x51	0x05	82	0x64	0x4A	143	0x04	0x00
22	0x154	0x7C	83	0x65	0x05	144	0x05	0x20
23	0x158	0x7C	84	0x68	0x28	145	0xFE	0x00
24	0x159	0x6F	85	0x69	0x5E	146	0xFF	0x00
25	0x15C	0x7C	86	0x6A	0x3D	147	0x89	0x00
26	0x15D	0x3F	87	0x6B	0x8F	148	0x95	0x00
27	0x160	0x7C	88	0x6C	0x44	149	0x96	0x00
28	0x161	0x3F	89	0x57	0xDA	150	0x97	0x00
29	0x164	0x7C	90	0x57	0x9A	151	0x9C	0x00
30	0x165	0x4F	91	0x57	0x1A	152	0x57	0x1A
31	0x16C	0x7C	92	0x58	0x3E	153	0x57	0x3A
32	0x1B0	0x1C	93	0x58	0x3C	154	0x57	0x7A
33	0x1B1	0x5F	94	0x58	0x38	155	0x57	0xFA
34	0x1D8	0x1C	95	0x58	0x30	156	0x58	0x01
35	0x1D9	0xAF	96	0x58	0x20	157	0x58	0x03

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表 7-13. Calibration Register Settings (続き)

WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA	WRITE #	ADDRESS	DATA
36	0xB2	0x1F	97	0x58	0x00	158	0x58	0x07
37	0xB5	0x7F	98	0x89	0x20	159	0x58	0x0F
38	0x165	0xFF	99	0x95	0x00	160	0x58	0x1F
39	0x38	0x01	100	0x96	0x00	161	0x58	0x3F
40	0xA4	0x30	101	0x97	0x10	162	0x45	0x8A
41	0xC5	0x7F	102	0x9C	0x00	163	0x45	0x0A
42	0xA8	0x00	103	0x57	0x1E	164	Delay 1.3 x 3 GSPS/ F_S seconds	
43	0xA2	0x63	104	0xFE	0x20	165	0x47	0xC0
44	0xA3	0x00	105	0xFF	0x19	166	0x46	0x03
45	0xAD	0x02	106	0x46	0x02	167	0x47	0xC0
46	0x05	0x80	107	0x45	0x8A	168	0x05	0x80
47	0x20	0x1F	108	0x45	0x0A	169	0x20	0x1F
48	0x93	0x20	109	Delay 1.3 x 3 GSPS/ F_S seconds		170	0x9D	0x05
49	0x20	0x00	110	0x05	0x80	171	0x9E	0x08
50	0x05	0x00	111	0x04	0x01	172	0x8B	0x40
51	0x04	0x01	112	0x20	0x1F	173	0x20	0x00
52	0x20	0x1F	113	0x82	0x00	174	0x05	0x00
53	0x93	0x20	114	0x9D	0x05	175	0x04	0x01
54	0x04	0x01	115	0x9E	0x08	176	0x20	0x1F
55	0x20	0x00	116	0x9D	0x45	177	0x9D	0x05
56	0x04	0x00	117	0x9D	0x05	178	0x9E	0x08
57	0x05	0x20	118	0xA0	0x80	179	0x8B	0x40
58	0xC0	0x7C	119	0xA2	0x80	180	0x20	0x00
59	0xBC	0x3C	120	0xA4	0x80	181	0x04	0x00
60	0xC9	0x01	121	0xA6	0x80			
61	0xC9	0x00	122	0xA8	0x80			

7.3.1.10 Step 10: JESD Interface Synchronization

The JESD interface can be synchronized using SPI writes or the GPIO1 pin (needs additional config).

表 7-14. JESD interface synchronization using SPI writes

ADDRESS	DATA	DESCRIPTION
0x05	0x04	Select JESD page
0x21	0x41	Configure ADC to control SYNC using SPI writes
0x21	0x61	Configure JESD interface to send K28.5 characters for receiver synchronization
0x21	0x41	Configure JESD interface to send normal ADC data

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7.3.1.11 Step 11: NCO Configuration

The NCO frequencies for the 4 DDCs are programmed with these steps.

表 7-15. Register programming sequence for device configuration

ADDRESS	DATA	DESCRIPTION
0x05	0x02	
0x235	0xFF	
0x05	0x08	Select DDCAB page
0x181	0x00	
0x100..0x105		Program NCO1 CHA
0x140..0x145		Program NCO1 CHB
0x181	0x30	Update NCO with current frequencies from the register map.
0x181	0x00	
0x05	0x08	Select DDCCD page
0x181	0x00	
0x100..0x105		Program NCO1 CHC
0x140..0x145		Program NCO1 CHD
0x181	0x30	Update NCO with current frequencies from the register map.
0x181	0x00	

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7.4 Power Supply Recommendations

The ADC34RF5x requires four different power-supplies. The AVDD18, AVDD12 and CLKVDD rail provides power for the internal analog and clocking circuits of the ADC while the DVDD rail powers the digital logic (including averaging and decimation filter) and the JESD204B digital interface.

Power sequencing is required as shown in Initialization Set Up. The AVDD18, AVDD12 and especially the CLKVDD power supply must be low noise to achieve data sheet performance. For applications operating near DC, the 1/f noise contribution of the power supply must also be considered.

Power supply decoupling capacitors (0.1 µF) must be as close as possible to the pins on the top layer.

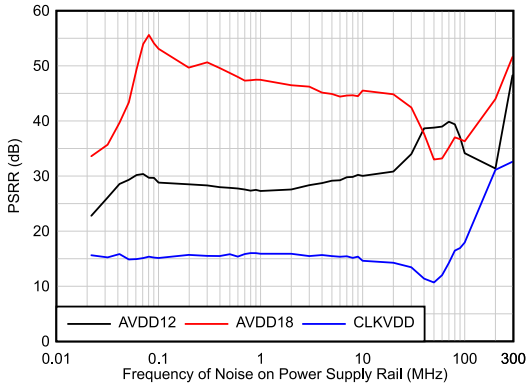

図 7-5. Power supply rejection ratio (PSRR) vs frequency

The recommended power supply architecture for a low noise design is to first use a high-efficiency step down switching regular, followed by a second stage of regulation using a low noise LDO for each power rail as shown in 図 7-6. This provides additional switching noise reduction and improved voltage accuracy.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements. Recommended switching regulators for the first stage include the LMS3635, and similar devices. Recommended low dropout (LDO) linear regulators include the TPS7A8400, and similar devices.

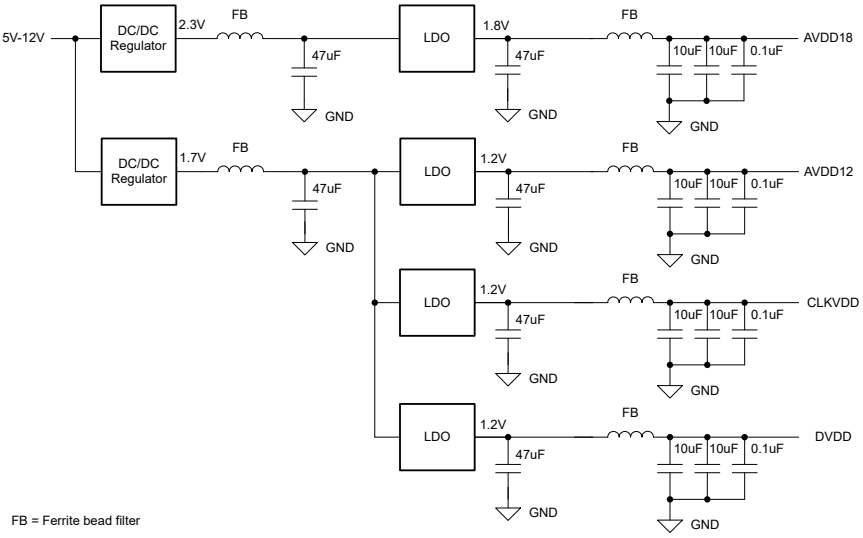

図 7-6. Power supply design example

AVDD12 or CLKVDD should not be shared with the DVDD to prevent digital switching noise from coupling into the analog domain.

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7.5 Layout

7.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100-Ω differential traces.
   - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital JESD204B output interface
   - Traces should be routed using tightly coupled 100-Ω differential traces.
3. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal, ground, power circuit board stack up to maximize coupling between the ground and power plane.

7.5.2 Layout Example

The following screen shot shows the top layer of the ADC34RF5x EVM.

- The input signal traces are routed as differential signals on the top layer avoiding vias. Care is taken to maintain symmetry between positive and negative input with matched trace length to minimize phase imbalance. 図 7-7 shows the layout example for 1x and 2x averaging configuration.
- JESD204B output interface lanes are routed differential and length matched.
- Bypass caps are close to the power pins on the top layer avoiding vias.

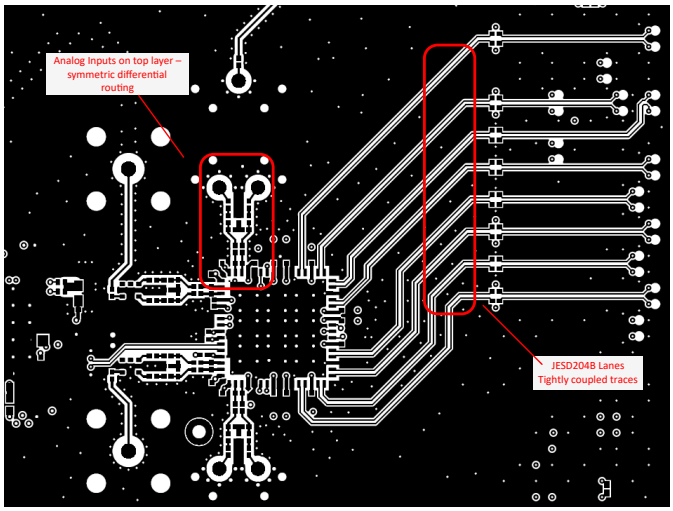

図 7-7. Layout example: top layer of ADC34RF5x EVM

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8 Device and Documentation Support

8.1 デバイスのサポート

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial release.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC34RF55IRTD	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ34RF55
ADC34RF55IRTD.A	Active	Production	VQFN (RTD) | 64	260 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34RF55
ADC34RF55IRTDT	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ34RF55
ADC34RF55IRTDT.A	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34RF55

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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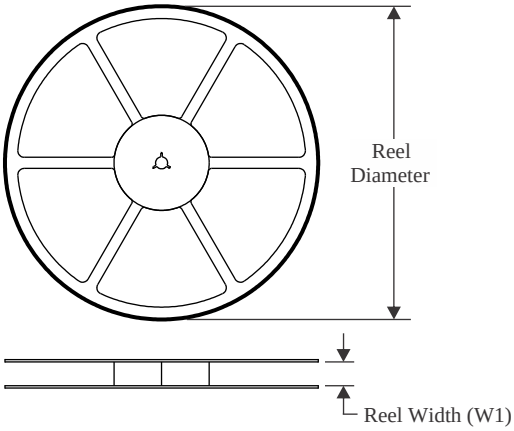
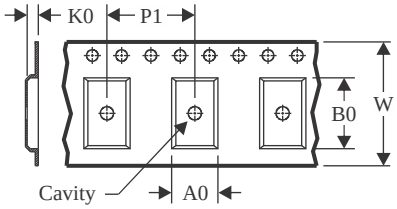
TAPE AND REEL INFORMATION

REEL DIMENSIONS

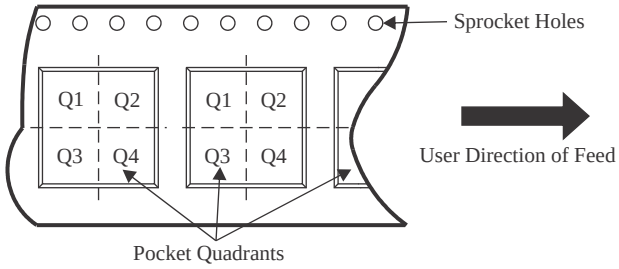


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

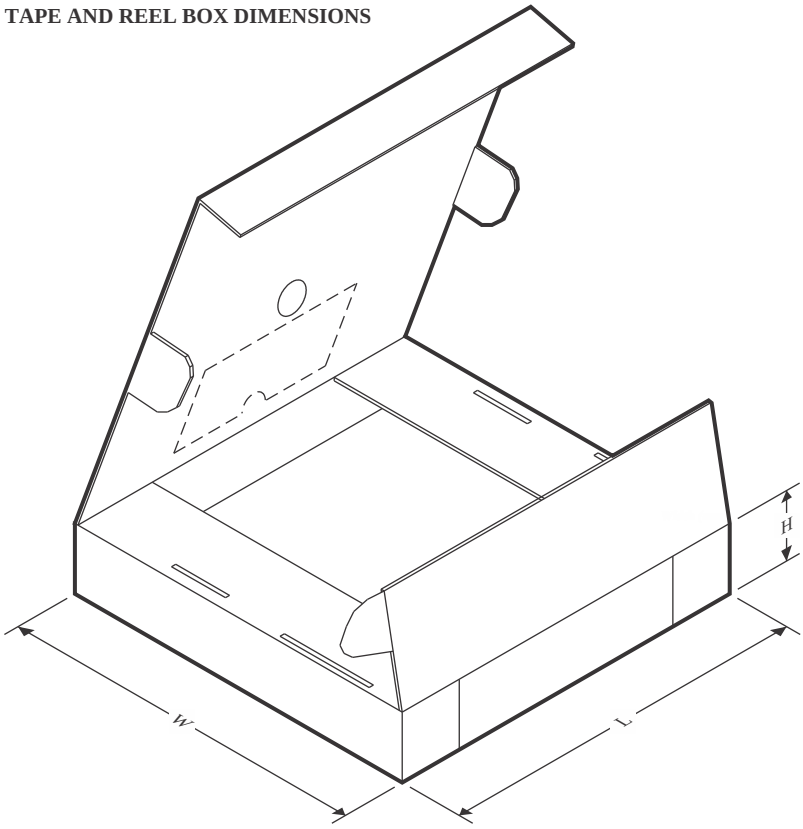
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC34RF55IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

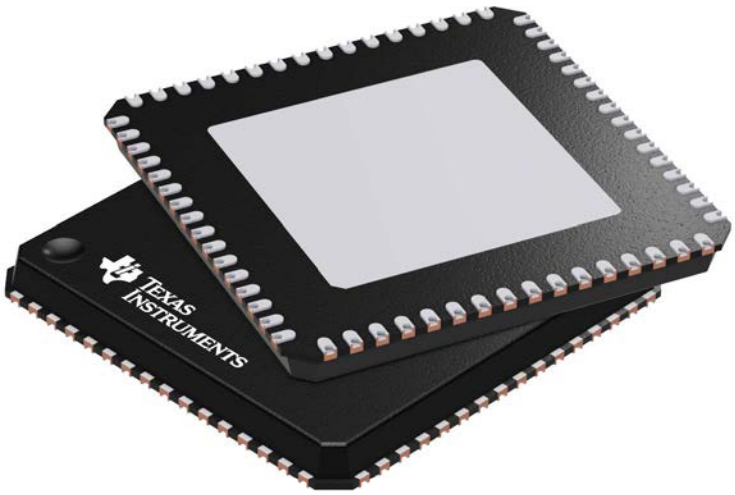
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC34RF55IRTDT	VQFN	RTD	64	250	213.0	191.0	55.0

GENERIC PACKAGE VIEW

RTD 64

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



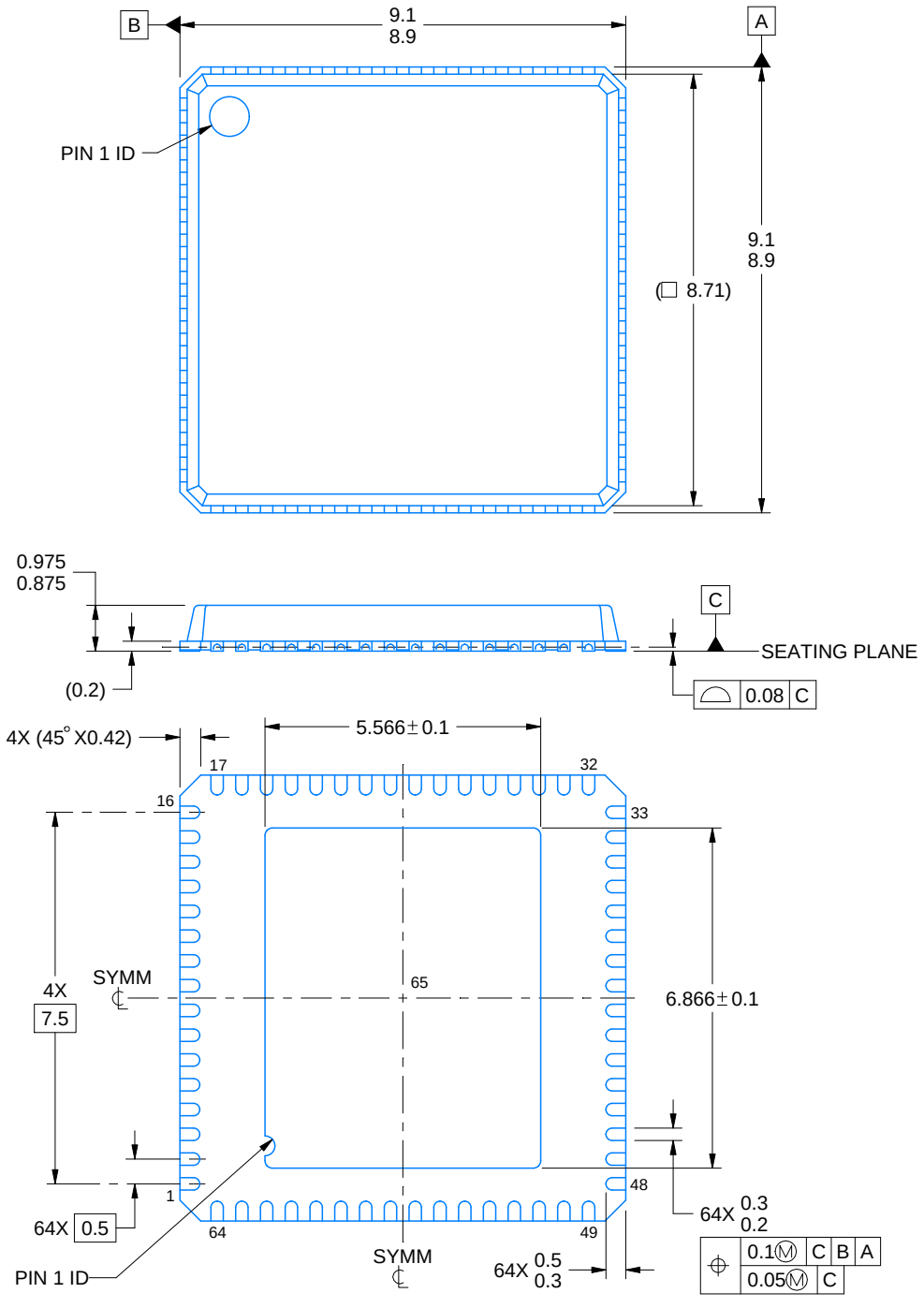
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RTD0064N

PACKAGE OUTLINE

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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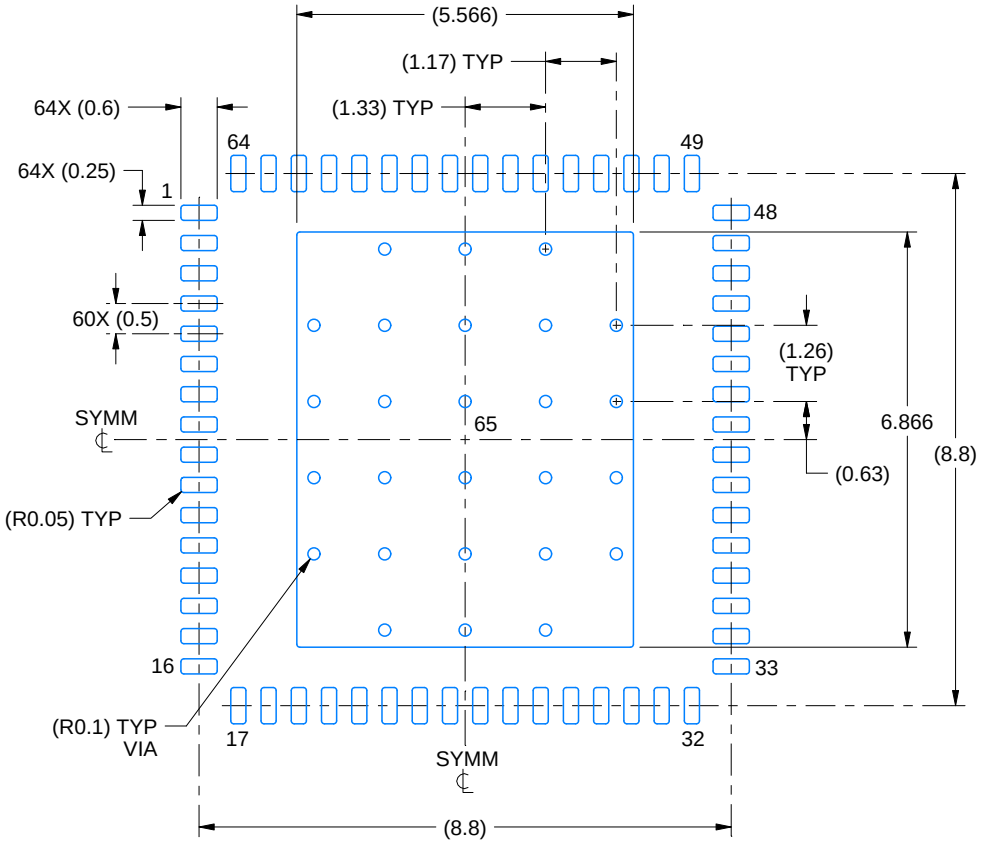
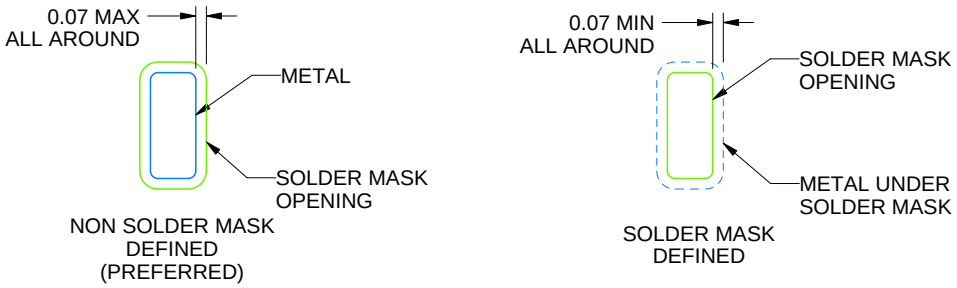
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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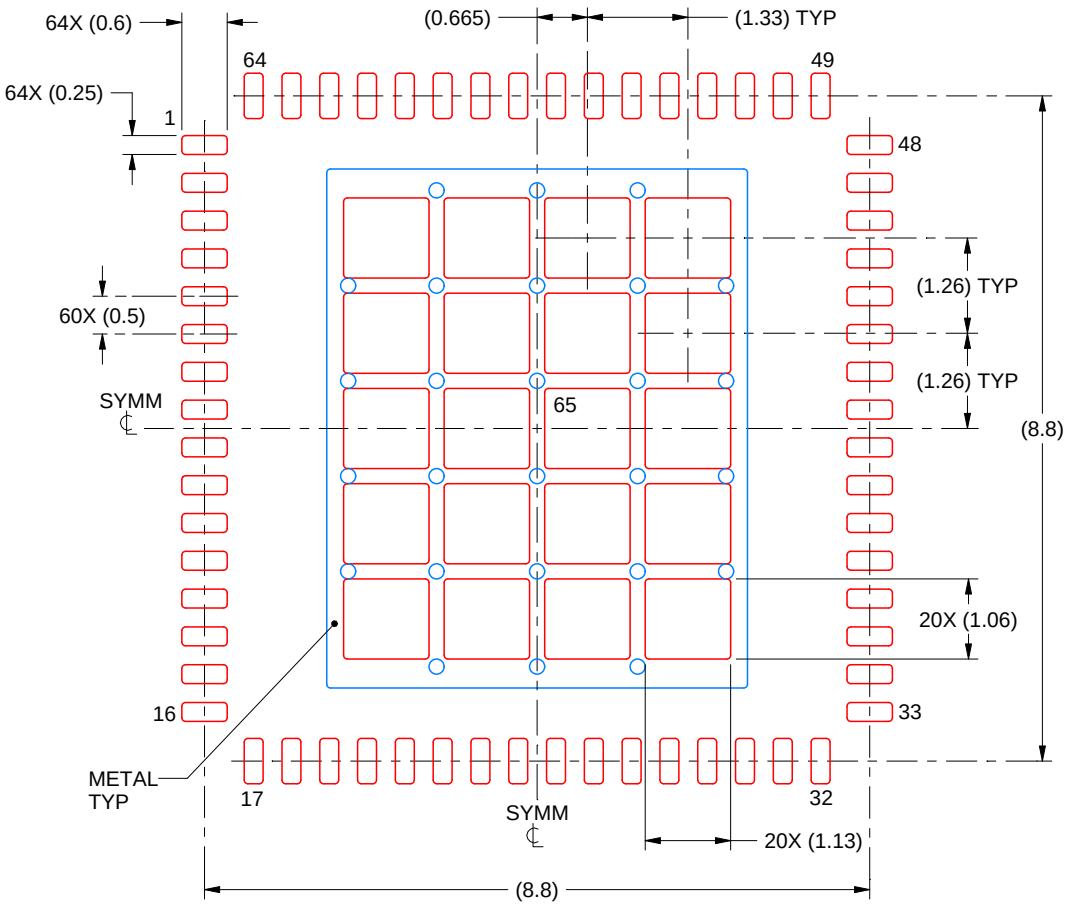
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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