

ADC3564 14 ビット、125MSPS、低ノイズ、超低消費電力の ADC

1 特長

- 14 ビット、125MSPS ADC
- ノイズ・フロア: -156dBFS/Hz
- 超低消費電力: 125MSPS で 137mW
- レイテンシ: 2 クロック・サイクル以下
- 14 ビット、ミッシング・コードなしを仕様規定
- INL: ± 1.5 LSB, DNL: ± 0.5 LSB
- リファレンス: 外部または内部
- 入力周波数帯: 1200MHz (3dB)
- 産業用温度範囲: -40°C ~ +105°C
- オンチップ・デジタル・フィルタ (オプション)
 - デシメーション比: 2、4、8、16、32
 - 32 ビット NCO
- シリアル LVDS デジタル・インターフェイス (2 線式、1 線式、1/2 線式)
- 小型サイズ: 40-WQFN (5mm × 5mm) パッケージ
- スペクトル性能 ($f_{IN} = 10$ MHz):
 - SNR: 77.5dBFS
 - SFDR: 80dBc HD2、HD3
 - SFDR: 95dBFS の最大スプリアス
- スペクトル性能 ($f_{IN} = 70$ MHz):
 - SNR: 75dBFS
 - SFDR: 75dBc HD2、HD3
 - SFDR: 90dBFS の最大スプリアス

2 アプリケーション

- 高速データ・アキュイジション
- 産業機器監視
- サーマル・イメージング
- 画像処理およびソナー
- ソフトウェア無線
- 電力品質分析器
- 通信インフラ
- 制御ループ
- 計測機器
- スマート・グリッド
- 分光器
- レーダー

3 概要

ADC3564 デバイスは、低ノイズ、超低消費電力、14 ビット、125MSPS の高速 A/D コンバータ (ADC) です。低消費電力を実現するように設計されており、ノイズ・スペクトル密度は -156dBFS/Hz で、優れた直線性とダイナミック・レンジを備えています。ADC3564 デバイスは IF サンプリングをサポートしており、広範なアプリケーションに最適です。待ち時間 (レイテンシ) がわずか 1 クロック・サイクルと短いため、高速な制御ループを実現できます。本 ADC の消費電力はわずか 137mW (125MSPS 時) であり、サンプリング・レートを下げることで、消費電力を良好に低減できます。

ADC3564 は、シリアル LVDS (SLVDS) インターフェイスを使用してデータを出力し、デジタル相互接続の数を最小限に抑えます。このデバイスは、2 レーン、1 レーン、およびハーフ・レーンのオプションをサポートしています。本デバイスは、各種速度グレードを持つピン互換ファミリであり、40 ピン VQFN パッケージで供給されます。このデバイスは、-40 ~ +105°C の拡張産業用温度範囲をサポートしています。

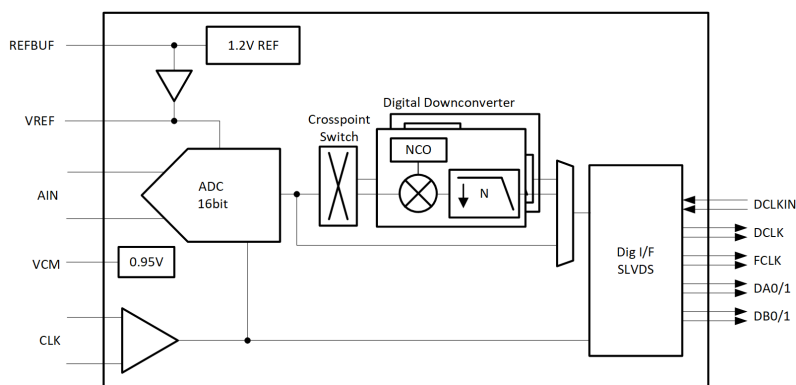
パッケージ情報

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|---------|-----------|---------------|
| ADC3564 | WQFN (40) | 5.00 × 5.00mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。

表 3-1. デバイスの比較

| 部品番号 | 分解能 | サンプリング・レート |
|---------|--------|------------|
| ADC3561 | 16 ビット | 10MSPS |
| ADC3562 | 16 ビット | 25MSPS |
| ADC3563 | 16 ビット | 65MSPS |
| ADC3564 | 14 ビット | 125MSPS |



概略ブロック図



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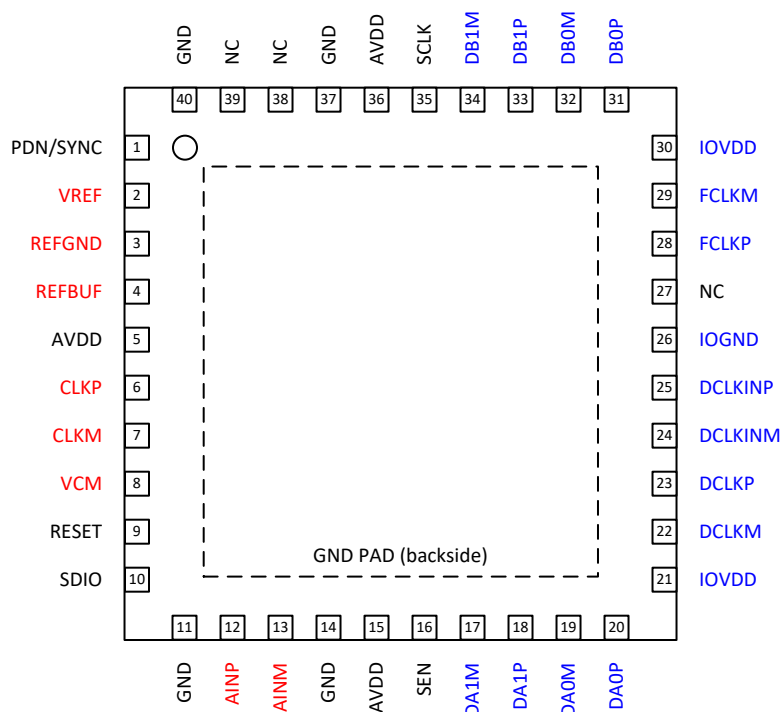
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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|-------------|----------|------------------|
| August 2022 | * | Initial release. |

5 Pin Configuration and Functions



**图 5-1. RSB (WQFN) Package, 40-Pin
(Top View)**

表 5-1. Pin Descriptions

| PIN | | I/O | DESCRIPTION |
|-----------------|-----|-----|---|
| NAME | NO. | | |
| INPUT/REFERENCE | | | |
| AINP | 12 | I | Positive analog input |
| AINM | 13 | I | Negative analog input |
| VCM | 8 | O | Common-mode voltage output for the analog inputs |
| VREF | 2 | I | External voltage reference input |
| REFBUF | 4 | I | 1.2 V external voltage reference input for use with internal reference buffer |
| REFGND | 3 | I | Reference ground input, 0 V |
| CLOCK | | | |
| CLKM | 7 | I | Negative differential sampling clock input for the ADC |
| CLKP | 6 | I | Positive differential sampling clock input for the ADC |
| CONFIGURATION | | | |
| PDN/SYNC | 1 | I | Power down/Synchronization input. This pin can be configured via the SPI interface. Active high. This pin has an internal 21 kΩ pull-down resistor. |
| RESET | 9 | I | Hardware reset. Active high. This pin has an internal 21 kΩ pull-down resistor. |
| SEN | 16 | I | Serial interface enable. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD. |
| SCLK | 35 | I | Serial interface clock input. This pin has an internal 21 kΩ pull-down resistor. |

表 5-1. Pin Descriptions (continued)

| PIN | | I/O | DESCRIPTION |
|--------------------------|--------------------------|-----|---|
| NAME | NO. | | |
| SDIO | 10 | I | Serial interface data input and output. This pin has an internal 21 kΩ pull-down resistor. |
| NC | 27,38,39 | - | Do not connect |
| DIGITAL INTERFACE | | | |
| DA0P | 20 | O | Positive differential serial LVDS output for lane 0, channel A |
| DA0M | 19 | O | Negative differential serial LVDS output for lane 0, channel A |
| DA1P | 18 | O | Positive differential serial LVDS output for lane 1, channel A |
| DA1M | 17 | O | Negative differential serial LVDS output for lane 1, channel A |
| DB0P | 31 | O | Positive differential serial LVDS output for lane 0, channel B. Used only in dual band complex decimation. Default is powered down. |
| DB0M | 32 | O | Negative differential serial LVDS output for lane 0, channel B. Used only in dual band complex decimation. Default is powered down. |
| DB1P | 33 | O | Positive differential serial LVDS output for lane 1, channel B. Used only in dual band complex decimation. Default is powered down. |
| DB1M | 34 | O | Negative differential serial LVDS output for lane 1, channel B. Used only in dual band complex decimation. Default is powered down. |
| DCLKP | 23 | O | Positive differential serial LVDS bit clock output. |
| DCLKM | 22 | O | Negative differential serial LVDS bit clock output. |
| FCLKP | 28 | O | Positive differential serial LVDS frame clock output. |
| FCLKM | 29 | O | Negative differential serial LVDS frame clock output. |
| DCLKINP | 25 | I | Positive differential serial LVDS bit clock input. |
| DCLKINM | 24 | I | Negative differential serial LVDS bit clock input. |
| POWER SUPPLY | | | |
| AVDD | 5,15,36 | I | Analog 1.8 V power supply |
| GND | 11,14,37,40, PowerPad | I | Ground, 0 V |
| IOGND | 26 | I | Ground, 0 V for digital interface |
| IOVDD | 21,30 | I | 1.8 V power supply for digital interface |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|---|------|--------------------|------|
| Supply voltage range, AVDD, IOVDD | | −0.3 | 2.1 | V |
| Supply voltage range, GND, IOGND, REFGND | | −0.3 | 0.3 | V |
| Voltage applied to input pins | AINP/M, CLKP/M, DCLKINP/M, VREF, REFBUF | −0.3 | MIN(2.1, AVDD+0.3) | V |
| | PDN/SYNC, RESET, SCLK, SEN, SDIO | −0.3 | MIN(2.1, AVDD+0.3) | |
| Junction temperature, T _J | | | 105 | °C |
| Storage temperature, T _{stg} | | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------------|--------------------------------|------|-----|--------------------|------|
| Supply voltage range | AVDD ⁽¹⁾ | 1.75 | 1.8 | 1.85 | V |
| | IOVDD ⁽¹⁾ | 1.75 | 1.8 | 1.85 | V |
| T _A | Operating free-air temperature | −40 | | 105 | °C |
| T _J | Operating junction temperature | | | 105 ⁽²⁾ | °C |

- (1) Measured to GND.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ADC3564 | UNIT |
|-------------------------------|--|-----------|------|
| | | RSB (QFN) | |
| | | 40 Pins | |
| R _{θJA} | Junction-to-ambient thermal resistance | 30.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 16.4 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 10.5 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 10.5 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 2.0 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics - Power Consumption

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, external 1.6V reference, and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--------------------------------------|-----|-----|-----|------|
| ADC3564: 125 MSPS | | | | | | |
| I _{AVDD} | Analog supply current | External reference | | 41 | 62 | mA |
| I _{IOVDD} | I/O supply current | SLVDS 2-wire | | 35 | 57 | |
| P _{DIS} | Power dissipation | External reference, SLVDS 2-wire | | 137 | | mW |
| I _{IOVDD} | I/O supply current | SLVDS 2-wire, 1/2-swing | | 27 | | mA |
| | | 4x real decimation, SLVDS 1-wire | | 41 | | |
| | | 16x real decimation, SLVDS 1-wire | | 36 | | |
| | | 4x complex decimation, SLVDS 1-wire | | 48 | | |
| | | 8x complex decimation, SLVDS 1-wire | | 45 | | |
| | | 16x complex decimation, SLVDS 1-wire | | 41 | | |
| | | 32x complex decimation, SLVDS 1-wire | | 40 | | |
| MISCELLANEOUS | | | | | | |
| I _{AVDD} | Internal reference, additional analog supply current | Enabled via SPI | | 4 | | mA |
| | External 1.2V reference (REFBUF), additional analog supply current | | | 0.5 | | |
| | Single ended clock input, reduces analog supply current by | | | 1 | | |
| P _{DIS} | Power consumption in global power down mode | Default mask settings | | 12 | | mW |

6.6 Electrical Characteristics - DC Specifications

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and -1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---------------------------------|-------|------------|------|-----------------------|
| DC ACCURACY | | | | | | |
| No missing codes | | | 14 | | | bits |
| PSRR | | $F_{\text{IN}} = 1 \text{ MHz}$ | | 35 | | dB |
| DNL | Differential nonlinearity | $F_{\text{IN}} = 5 \text{ MHz}$ | -0.97 | ± 0.9 | 0.97 | LSB |
| INL | Integral nonlinearity | $F_{\text{IN}} = 5 \text{ MHz}$ | -7.5 | ± 2.6 | 7.5 | LSB |
| V _{OS_ERR} | Offset error | | -55 | ± 30 | 55 | LSB |
| V _{OS_DRIFT} | Offset drift over temperature | | | ± 0.06 | | LSB/ $^\circ\text{C}$ |
| GAIN _{ERR} | Gain error | External 1.6V Reference | | ± 2 | | %FSR |
| GAIN _{DRIFT} | Gain drift over temperature | External 1.6V Reference | | ± 57 | | ppm/ $^\circ\text{C}$ |
| GAIN _{ERR} | Gain error | Internal Reference | | ± 3 | | %FSR |
| GAIN _{DRIFT} | Gain drift over temperature | Internal Reference | | 106 | | ppm/ $^\circ\text{C}$ |
| Transition Noise | | | | 0.7 | | LSB |
| ADC ANALOG INPUT (AINP/M) | | | | | | |
| FS | Input full scale | Differential | | 3.2 | | V _{pp} |
| V _{CM} | Input common mode voltage | | 0.9 | 0.95 | 1.0 | V |
| R _{IN} | Input resistance | Differential at DC | | 8 | | k Ω |
| C _{IN} | Input Capacitance | Differential at DC | | 5.4 | | pF |
| V _{OCM} | Output common mode voltage | | | 0.95 | | V |
| BW | Analog Input Bandwidth (-3dB) | | | 1.4 | | GHz |
| Internal Voltage Reference | | | | | | |
| V _{REF} | Internal reference voltage | | | 1.6 | | V |
| V _{REF} Output Impedance | | | | 8 | | Ω |
| Reference Input Buffer (REFBUF) | | | | | | |
| External reference voltage | | | | 1.2 | | V |
| External voltage reference (VREF) | | | | | | |
| V _{REF} | External voltage reference | | | 1.6 | | V |
| Input Current | | | | 1 | | mA |
| Input impedance | | | | 5.3 | | k Ω |
| Clock Input (CLKP/M) | | | | | | |
| Input clock frequency | | External reference | 10 | | 125 | MHz |
| | | Internal reference | 100 | | 125 | MHz |
| V _{ID} | Differential input voltage | | | 1 | 3.6 | V _{pp} |
| V _{CM} | Input common mode voltage | | | 0.9 | | V |
| R _{IN} | Single ended input resistance to common mode | | | 5 | | k Ω |
| C _{IN} | Single ended input capacitance | | | 1.5 | | pF |
| Clock duty cycle | | | 45 | 50 | 60 | % |

6.6 Electrical Characteristics - DC Specifications (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and -1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------|-------------------------------|----------------|-------|-----|------|
| Digital Inputs (RESET, PDN, SCLK, SEN, SDIO) | | | | | | |
| V _{IH} | High level input voltage | | 1.4 | | | V |
| V _{IL} | Low level input voltage | | | | 0.4 | |
| I _{IH} | High level input current | | | 90 | 150 | uA |
| I _{IL} | Low level input current | | -150 | -90 | | uA |
| C _I | Input capacitance | | | 1.5 | | pF |
| Digital Output (SDOUT) | | | | | | |
| V _{OH} | High level output voltage | I _{LOAD} = -400 uA | IOVDD – 0.1 | IOVDD | | V |
| V _{OL} | Low level output voltage | I _{LOAD} = 400 uA | | | 0.1 | |
| SLVDS Interface | | | | | | |
| V _{ID} | Differential input voltage | DCLKIN | 200 | 350 | 650 | mVpp |
| V _{CM} | Input common mode voltage | | 1 | 1.2 | 1.3 | V |
| Output data rate | | per differential SLVDS output | | | 1 | Gbps |
| V _{OD} | Differential output voltage | | 500 | 700 | 850 | mVpp |
| V _{CM} | Output common mode voltage | | | 1.0 | | V |

6.7 Electrical Characteristics - AC Specifications

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{IOVDD} = 1.8\text{ V}$, 1.6 V external reference, and -1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--|--|------|--------|-----|---------|
| NSD | Noise Spectral Density | $f_{\text{IN}} = 5\text{ MHz}$, $A_{\text{IN}} = -20\text{ dBFS}$ | | -156.9 | | dBFS/Hz |
| SNR | Signal to noise ratio | $f_{\text{IN}} = 5\text{ MHz}$ | 72 | 77.5 | | dBFS |
| | | $f_{\text{IN}} = 5\text{ MHz}$, $A_{\text{IN}} = -20\text{ dBFS}$ | | 78.9 | | dBFS |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 77.6 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 76.9 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 75.5 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 74.1 | | |
| SINAD | Signal to noise and distortion ratio | $f_{\text{IN}} = 5\text{ MHz}$ | | 75.7 | | dBFS |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 74.2 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 72.6 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 71.3 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 72.4 | | |
| ENOB | Effective number of bits | $f_{\text{IN}} = 5\text{ MHz}$ | | 12.6 | | bit |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 12.6 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 12.5 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 12.3 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 12.0 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{\text{IN}} = 5\text{ MHz}$ | 71.5 | 80 | | dBc |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 76 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 74 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 72 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 76 | | |
| HD2 | Second Harmonic Distortion | $f_{\text{IN}} = 5\text{ MHz}$ | 77 | 84 | | dBc |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 78 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 75 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 77 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 79 | | |
| HD3 | Third Harmonic Distortion | $f_{\text{IN}} = 5\text{ MHz}$ | 73.5 | 84 | | dBc |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 81 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 88 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 76 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 81 | | |
| Non HD2,3 | Spur free dynamic range (excluding HD2 and HD3) | $f_{\text{IN}} = 5\text{ MHz}$ | 84 | 92 | | dBFS |
| | | $f_{\text{IN}} = 10\text{ MHz}$ | | 93 | | |
| | | $f_{\text{IN}} = 40\text{ MHz}$ | | 89 | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 84 | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 86 | | |
| IMD3 | Two tone inter-modulation distortion | $f_1 = 10\text{ MHz}$, $f_2 = 12\text{ MHz}$, $A_{\text{IN}} = -7\text{ dBFS/ tone}$ | | 88 | | dBc |

6.8 Timing Requirements

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = IOVDD = 1.8\text{ V}$, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|--|--|-----|-----------------------|------|
| ADC Timing Specifications | | | | | | |
| t _{AD} | Aperture Delay | | 0.85 | | ns | |
| t _A | Aperture Jitter | square wave clock with fast edges | 250 | | fs | |
| t _J | Jitter on DCLKIN | | ± 50 | | ps pk-pk | |
| Recory time from +6 dB overload condition | | SNR within 1 dB of expected value | 1 | | Clock cycle | |
| t _{ACQ} | Signal acquisition period | referenced to sampling clock falling edge | -T _S /4 | | Sampling clock period | |
| t _{CONV} | Signal conversion period | | 6 | | ns | |
| Wake up time | Time to valid data after coming out of power down. Internal reference. | Bandgap reference enabled, single ended clock | 13 | | us | |
| | | Bandgap reference enabled, differential clock | 15 | | | |
| | | Bandgap reference disabled, single ended clock | 2.4 | | ms | |
| | | Bandgap reference disabled, differential clock | 2.3 | | | |
| | Time to valid data after coming out of power down. External 1.6V reference. | Bandgap reference enabled, single ended clock | 13 | | us | |
| | | Bandgap reference enabled, differential clock | 14 | | | |
| | | Bandgap reference disabled, single ended clock | 2.0 | | ms | |
| | | Bandgap reference disabled, differential clock | 2.2 | | | |
| t _{S,SYNC} | Setup time for SYNC input signal | Referenced to sampling clock rising edge | 500 | | ps | |
| t _{H,SYNC} | Hold time for SYNC input signal | | 600 | | | |
| ADC Latency | Signal input to data output | 1/2-wire SLVDS | 1 | | Clock cycles | |
| | | 1-wire SLVDS | 1 | | | |
| | | 2-wire SLVDS | 2 | | | |
| Add. Latency | Real decimation by 2 | | 21 | | Output clock cycles | |
| | Complex decimation by 2 | | 22 | | | |
| | Real or complex decimation by 4, 8, 16, 32 | | 23 | | | |
| Interface Timing: Serial LVDS Interface | | | | | | |
| t _{PD} | Propagation delay: sampling clock falling edge to DCLK rising edge | Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. T _{DCLK} = DCLK period t _{CDCLK} = Sampling clock falling edge to DCLKIN falling edge | 2 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ + 3 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ + 4 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ | | ns | |
| | | Delay between sampling clock falling edge to DCLKIN falling edge >= 2.5ns. T _{DCLK} = DCLK period t _{CDCLK} = Sampling clock falling edge to DCLKIN falling edge | 2 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ + 3 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ + 4 + $\frac{T_{\text{DCLK}}}{t_{\text{CDCLK}}}$ | | | |

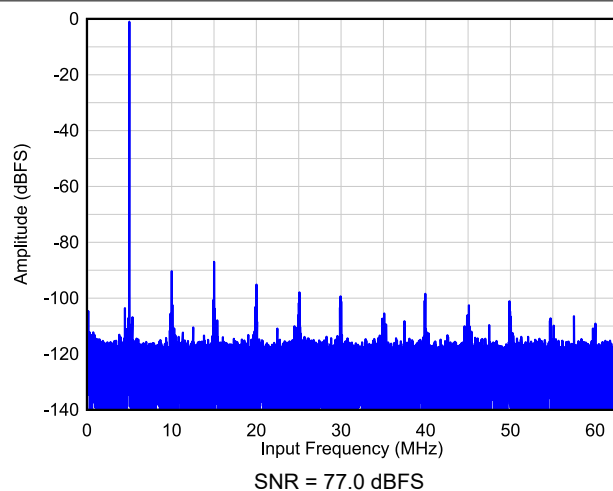
6.8 Timing Requirements (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 105^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{IOVDD} = 1.8\text{ V}$, 1.6 V external reference, and -1-dBFS differential input, unless otherwise noted

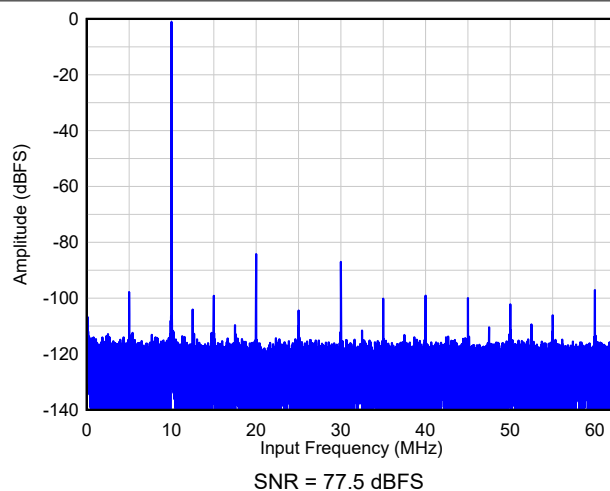
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--|---|-------------------------------------|------|-----|------|------|
| t _{CD} | DCLK rising edge to output data delay, 2-wire SLVDS, 14-bit | Fout = 65 MSPS, DA/B0,1 = 455 MBPS | 0 | 0.1 | | ns |
| | | Fout = 80 MSPS, DA/B0,1 = 560 MBPS | 0 | 0.1 | | |
| | | Fout = 125 MSPS, DA/B0,1 = 875 MBPS | -0.2 | 0.1 | | |
| | DCLK rising edge to output data delay, 1-wire SLVDS, 14-bit | Fout = 65 MSPS, DA/B0 = 910 MBPS | 0 | 0.1 | | |
| | DCLK rising edge to output data delay, 1-wire SLVDS, 16-bit | Fout = 10 MSPS, DA/B0 = 160 MBPS | 0 | 0.1 | | |
| | | Fout = 25 MSPS, DA/B0 = 400 MBPS | 0 | 0.1 | | |
| | | Fout = 62.5 MSPS, DA/B0= 1000 MBPS | -0.6 | 0.1 | | |
| | DCLK rising edge to output data delay, 1/2-wire SLVDS, 16-bit | Fout = 5 MSPS, DA0 = 160 MBPS | 0 | 0.1 | | |
| | | Fout = 10 MSPS, DA0 = 320 MBPS | 0 | 0.1 | | |
| | | Fout = 25 MSPS, DA0 = 800 MBPS | 0 | 0.1 | | |
| t _{DV} | Data valid, 2-wire SLVDS, 14-bit | Fout = 65 MSPS, DA/B0,1 = 455 MBPS | 1.8 | 1.9 | | ns |
| | | Fout = 80 MSPS, DA/B0,1 = 560 MBPS | 1.4 | 1.5 | | |
| | | Fout = 125 MSPS, DA/B0,1 = 875 MBPS | 0.6 | 0.8 | | |
| | Data valid, 1-wire SLVDS, 14-bit | Fout = 65 MSPS, DA/B0 = 910 MBPS | 0.6 | 0.8 | | |
| | Data valid, 1-wire SLVDS, 16-bit | Fout = 10 MSPS, DA/B0 = 160 MBPS | 5.7 | 5.8 | | |
| | | Fout = 25 MSPS, DA/B0 = 400 MBPS | 2.0 | 2.1 | | |
| | | Fout = 62.5 MSPS, DA/B0= 1000 MBPS | 0.5 | 0.6 | | |
| | Data valid, 1/2-wire SLVDS, 16-bit | Fout = 5 MSPS, DA0 = 160 MBPS | 5.7 | 5.8 | | |
| | | Fout = 10 MSPS, DA0 = 320 MBPS | 2.7 | 2.8 | | |
| | | Fout = 25 MSPS, DA0 = 800 MBPS | 0.8 | 0.9 | | |
| SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input | | | | | | |
| f _{CLK,SCLK} | Serial clock frequency | | | | 20 | MHz |
| t _{S,SEN} | SEN falling edge to SCLK rising edge | | 10 | | | ns |
| t _{H,SEN} | SCLK rising edge to SEN rising edge | | 9 | | | |
| t _{S,SDIO} | SDIO setup time from rising edge of SCLK | | 17 | | | |
| t _{H,SDIO} | SDIO hold time from rising edge of SCLK | | 9 | | | |
| SERIAL PROGRAMMING INTERFACE (SDIO) - Output | | | | | | |
| t _{OZD} | Delay from falling edge of 16th SCLK cycle during read operation for SDIO transition from tri-state to valid data | | 3.9 | | 10.8 | ns |
| t _{ODZ} | Delay from SEN rising edge for SDIO transition from valid data to tri-state | | 3.4 | | 14 | |
| t _{OD} | Delay from falling edge of 16th SCLK cycle during read operation to SDIO valid | | 3.9 | | 10.8 | |

6.9 Typical Characteristics

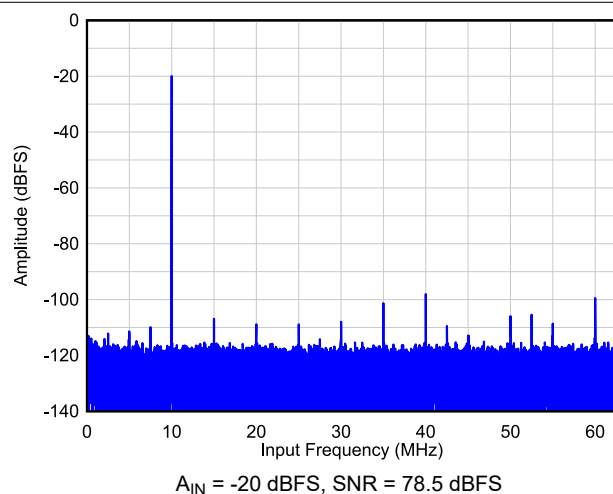
Typical values at $T_A = 25\text{ }^{\circ}\text{C}$, ADC sampling rate = 125 MSPS, $A_{IN} = -1\text{ dBFS}$ differential input, $AVDD = IOVDD = 1.8\text{ V}$, external voltage reference, unless otherwise noted.



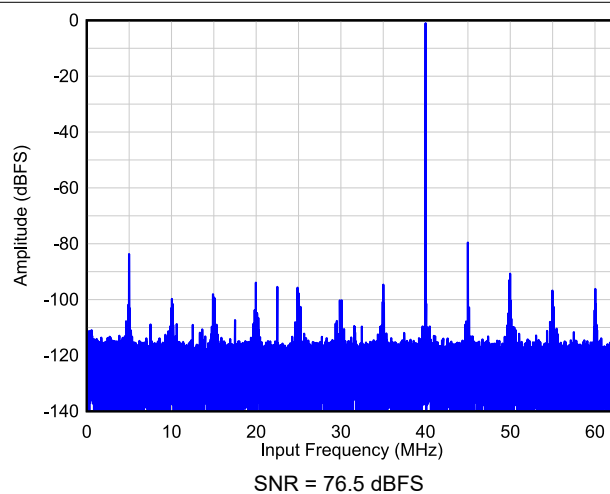
6-1. Single Tone FFT at $F_{IN} = 5\text{ MHz}$



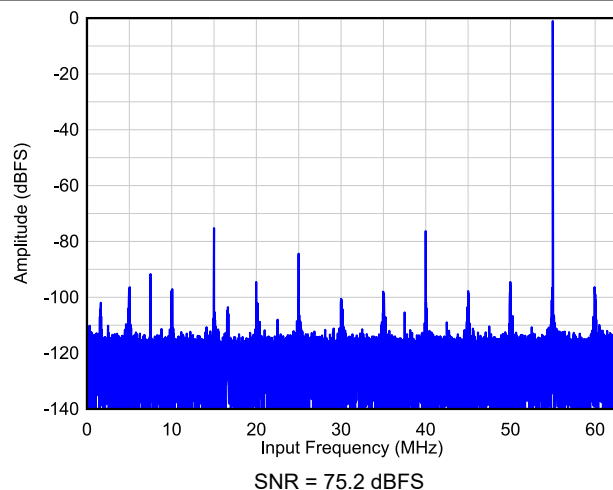
6-2. Single Tone FFT at $F_{IN} = 10\text{ MHz}$



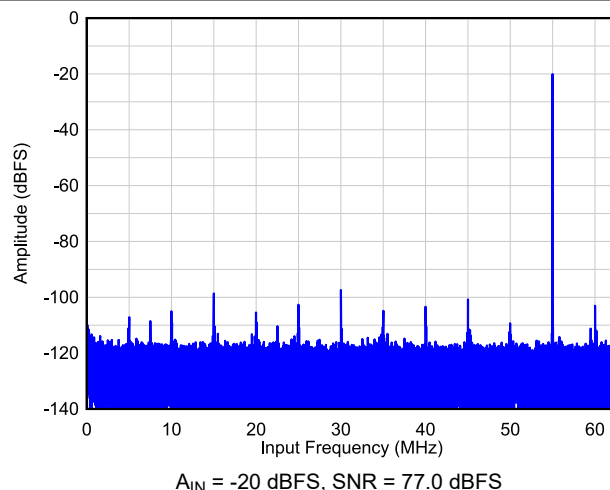
6-3. Single Tone FFT at $F_{IN} = 10\text{ MHz}$



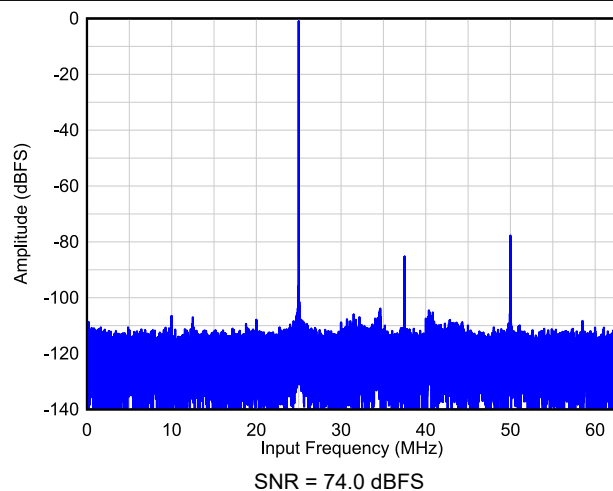
6-4. Single Tone FFT at $F_{IN} = 40\text{ MHz}$



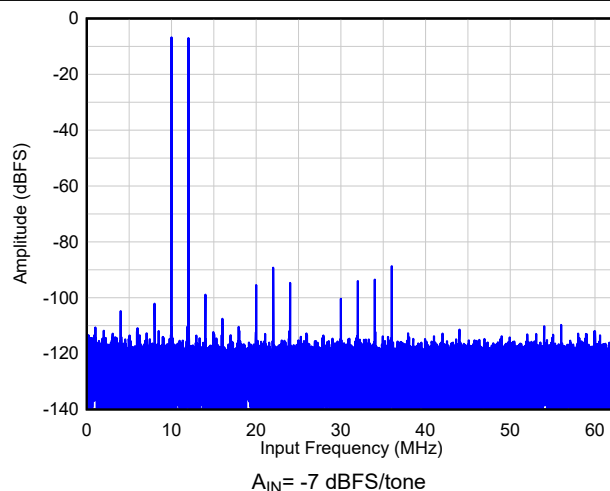
6-5. Single Tone FFT at $F_{IN} = 70$ MHz



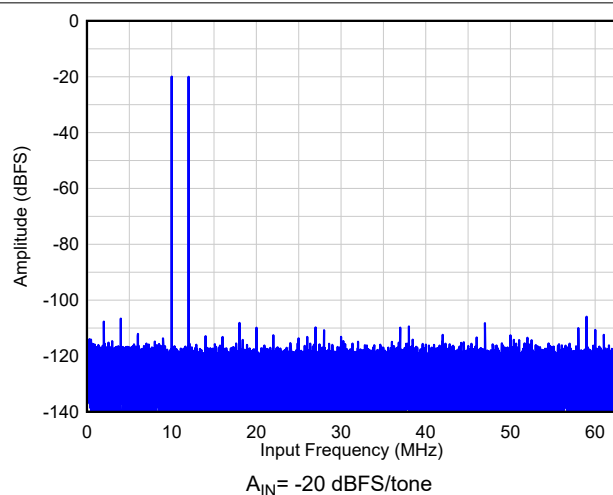
6-6. Single Tone FFT at $F_{IN} = 70$ MHz



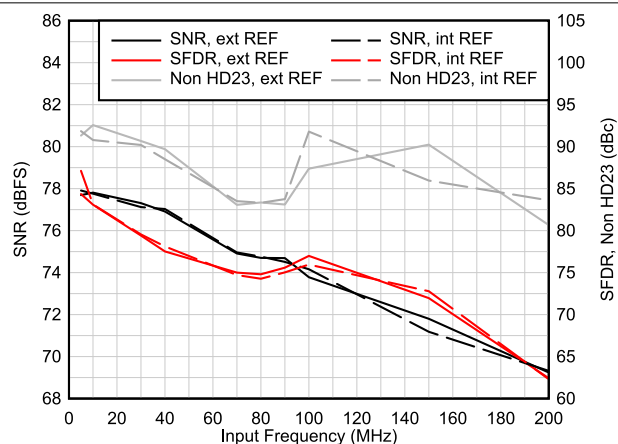
6-7. Single Tone FFT at $F_{IN} = 100$ MHz



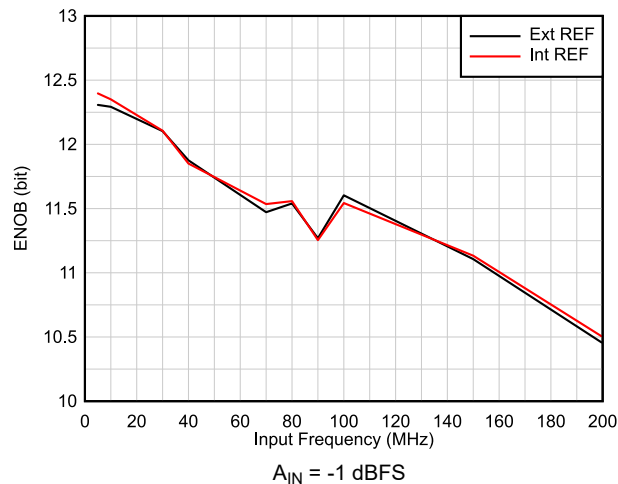
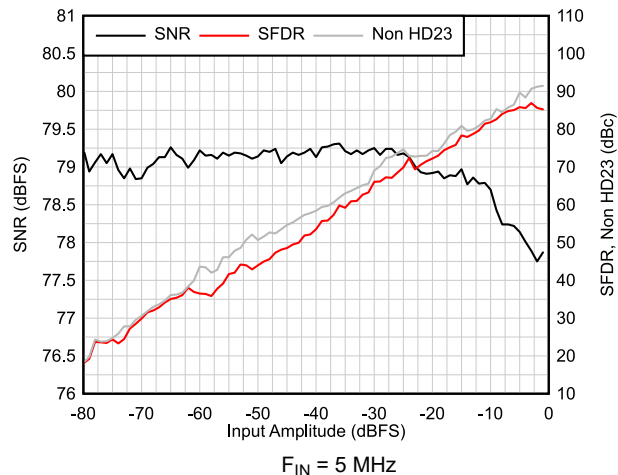
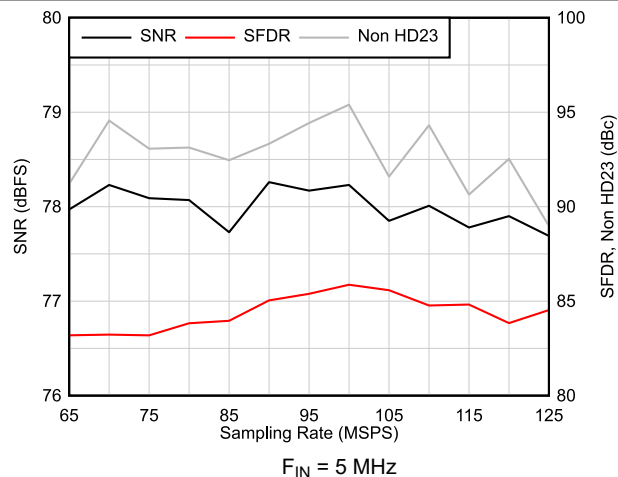
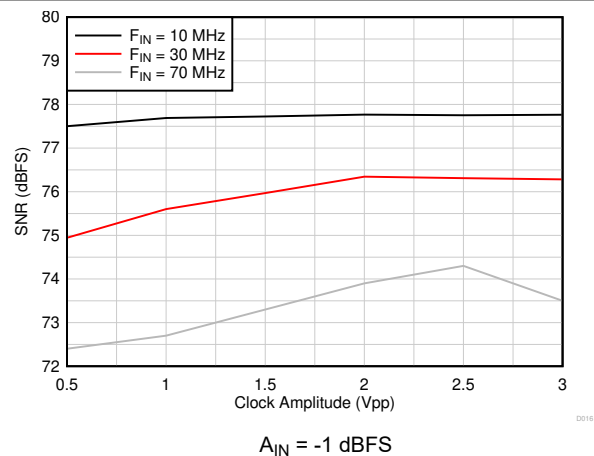
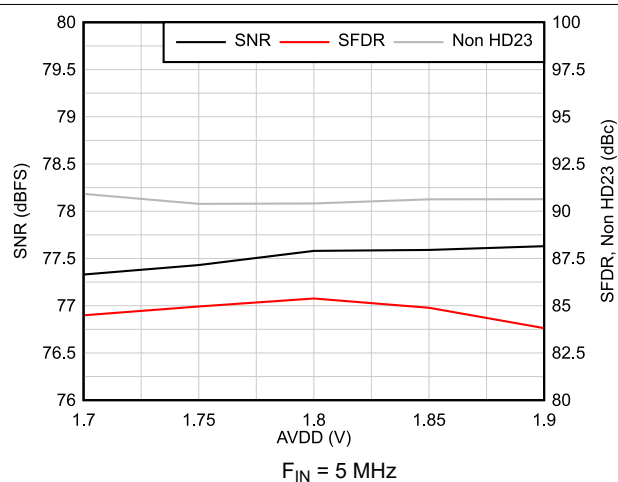
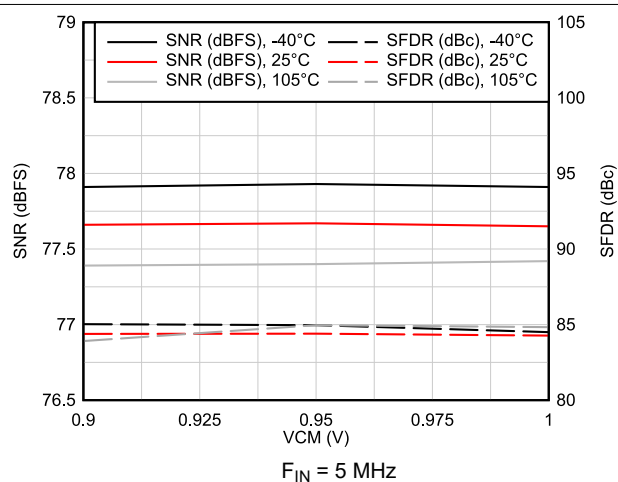
6-8. Two Tone FFT at $F_{IN} = 10/12$ MHz



6-9. Two Tone FFT at $F_{IN} = 10/12$ MHz



6-10. AC Performance vs Input Frequency


 **6-11. ENOB vs Input Frequency**

 **6-12. AC Performance vs Input Amplitude**

 **6-13. AC Performance vs Sampling Rate**

 **6-14. SNR vs Clock Amplitude**

 **6-15. AC Performance vs AVDD**

 **6-16. AC Performance vs VCM vs Temperature**

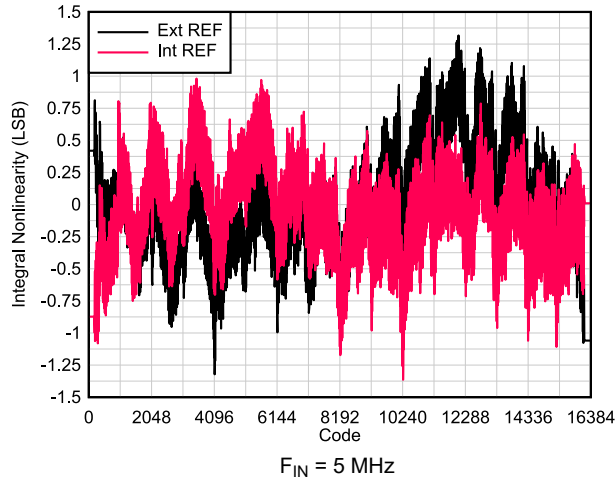


Figure 6-17. INL vs Code

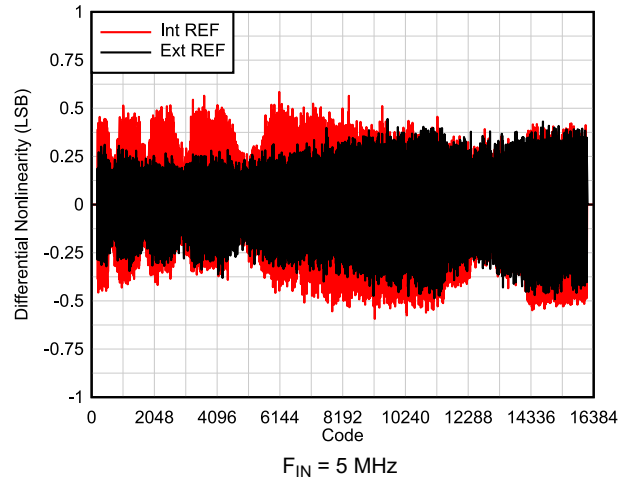


Figure 6-18. DNL vs Code

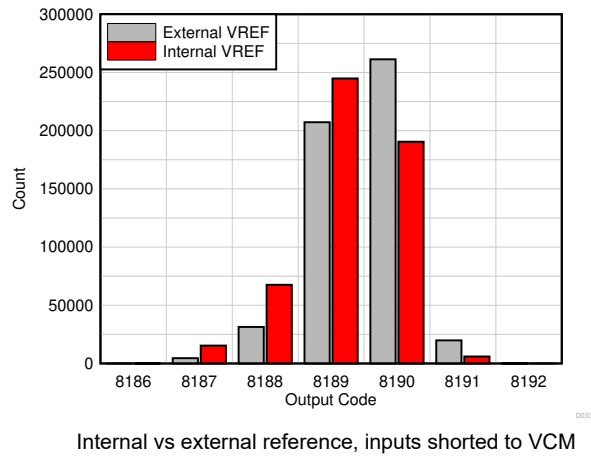


Figure 6-19. DC Histogram

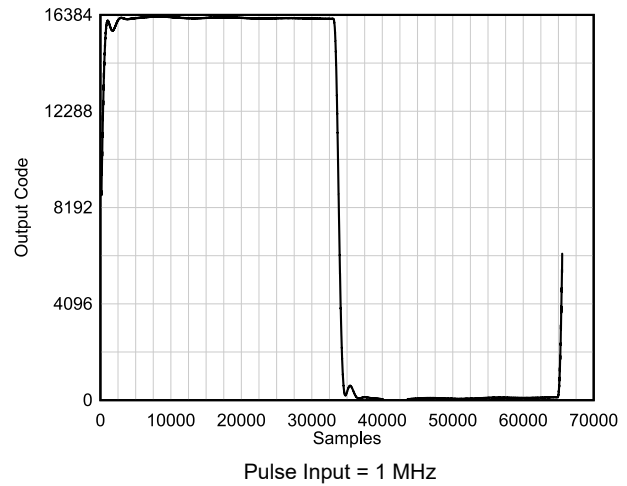


Figure 6-20. Pulse Response

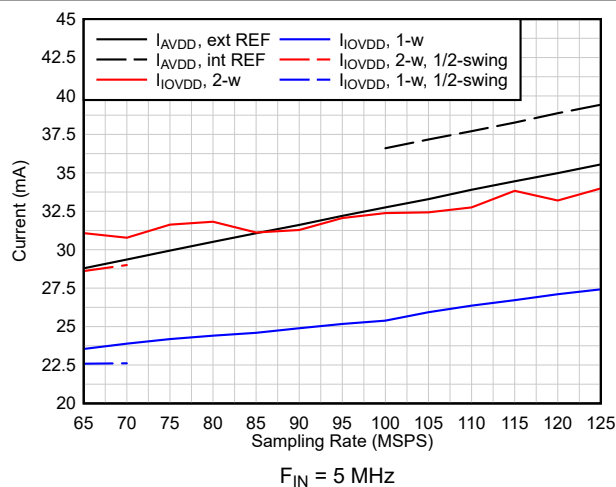


Figure 6-21. Current vs Sampling Rate

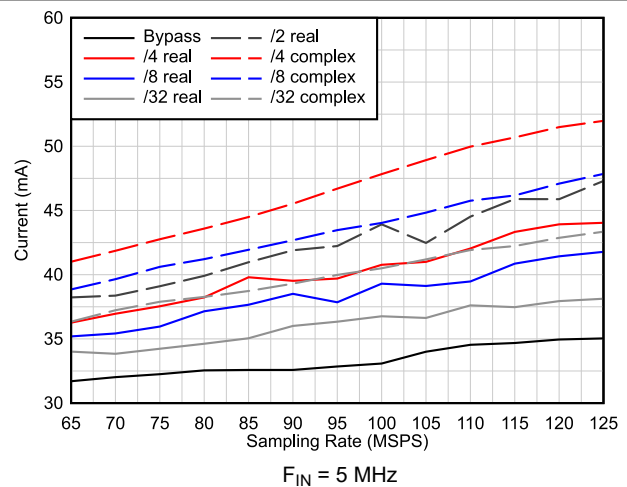
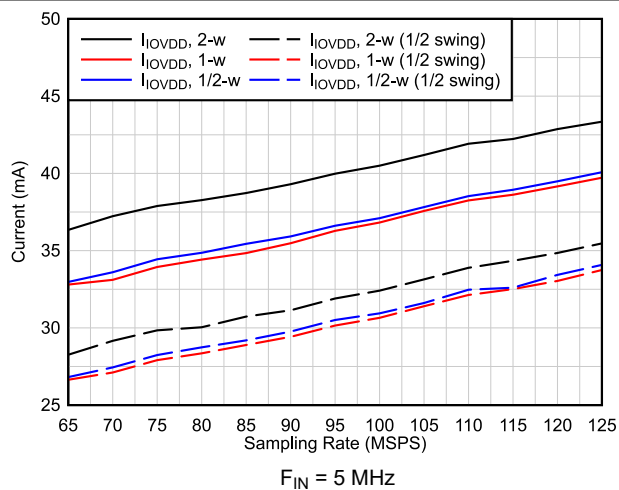
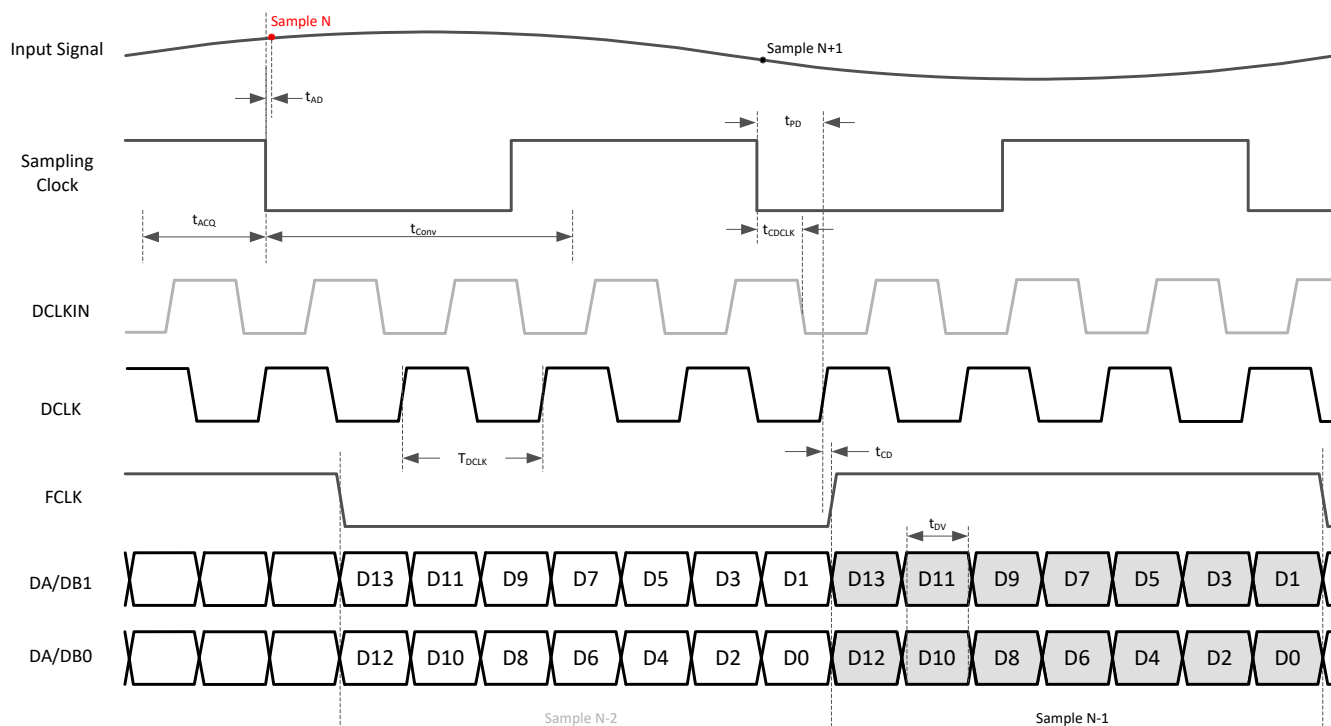


Figure 6-22. Current vs Decimation

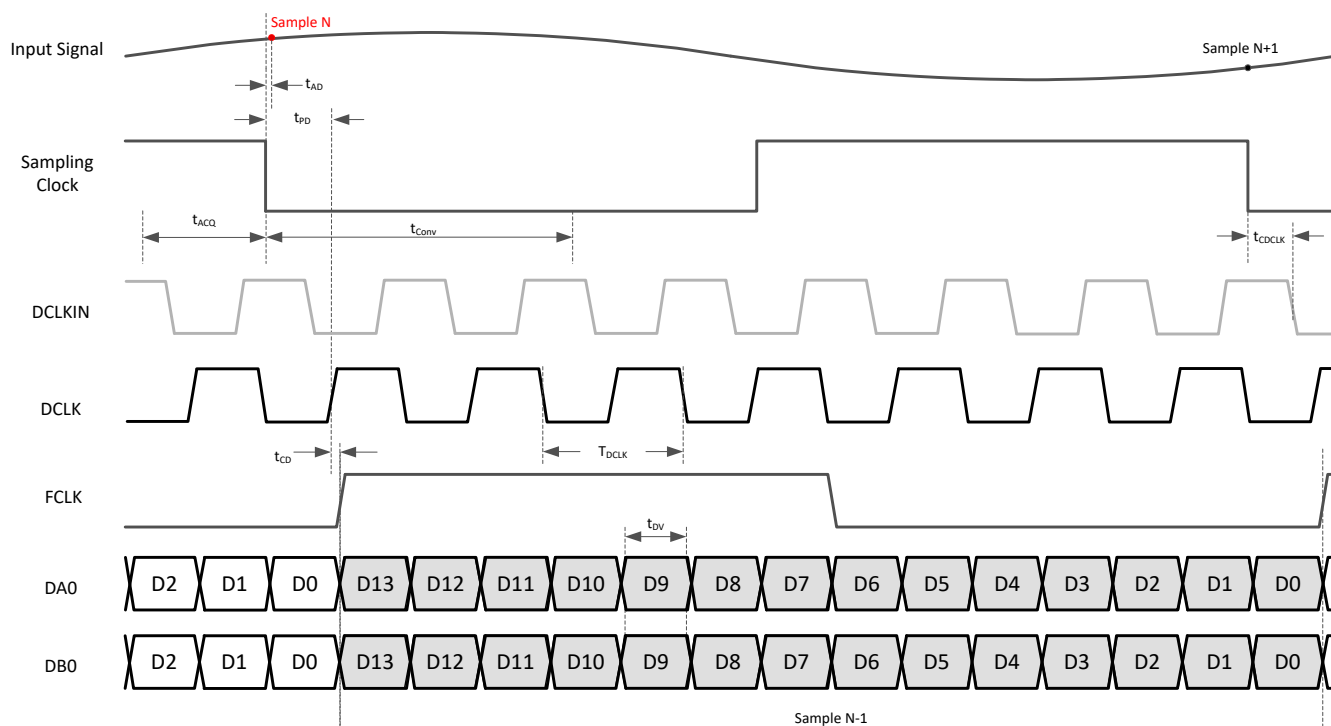


6-23. Current vs Interface

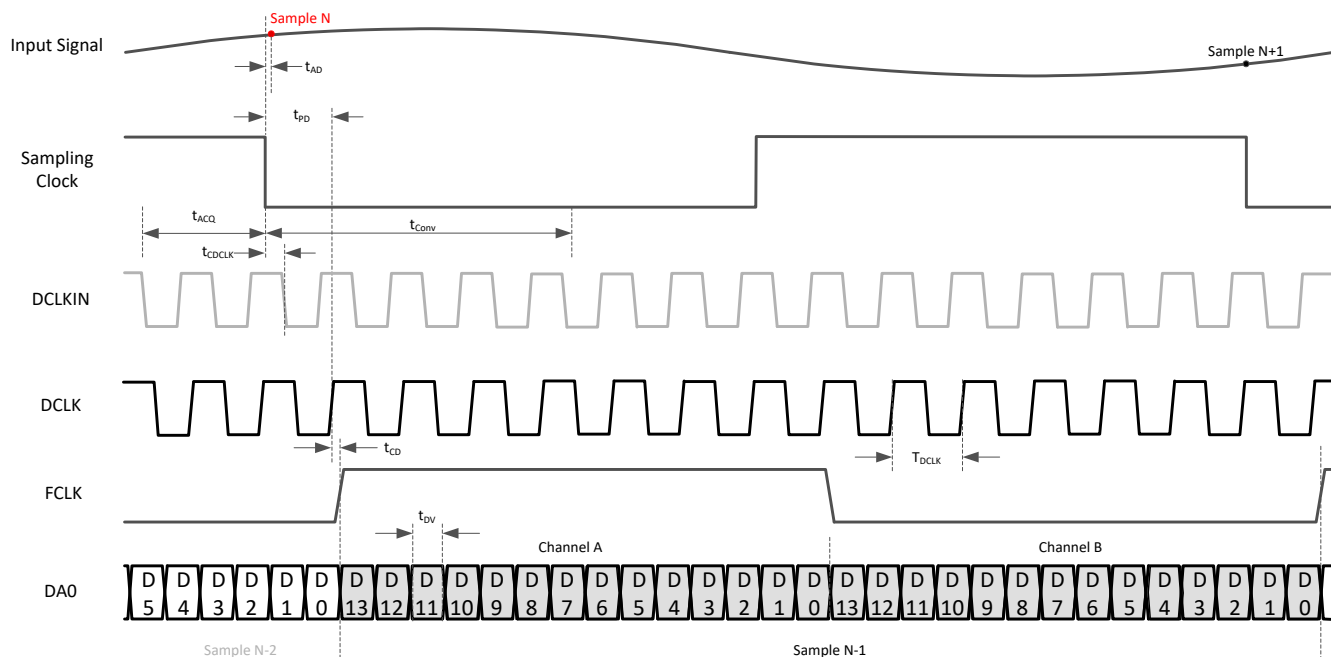
7 Parameter Measurement Information



7-1. Timing diagram: 2-wire SLVDS



7-2. Timing diagram: 1-wire SLVDS



✎ 7-3. Timing diagram: 1/2-wire SLVDS

8 Detailed Description

8.1 Overview

The ADC3564 is a low noise, ultra-low power 14-bit 125 MSPS high-speed ADC. It offers DC precision together with IF sampling support which makes it suited for a wide range of applications. The ADC3564 is equipped with an on-chip internal reference option but it also supports the use of an external, high precision 1.6 V voltage reference or an external 1.2 V reference which is buffered and gained up internally. Because of the inherent low latency architecture, the digital output result is available after only one clock cycle. Single ended as well as differential input signaling is supported.

注

The ADC3564 supports the following sampling rates:

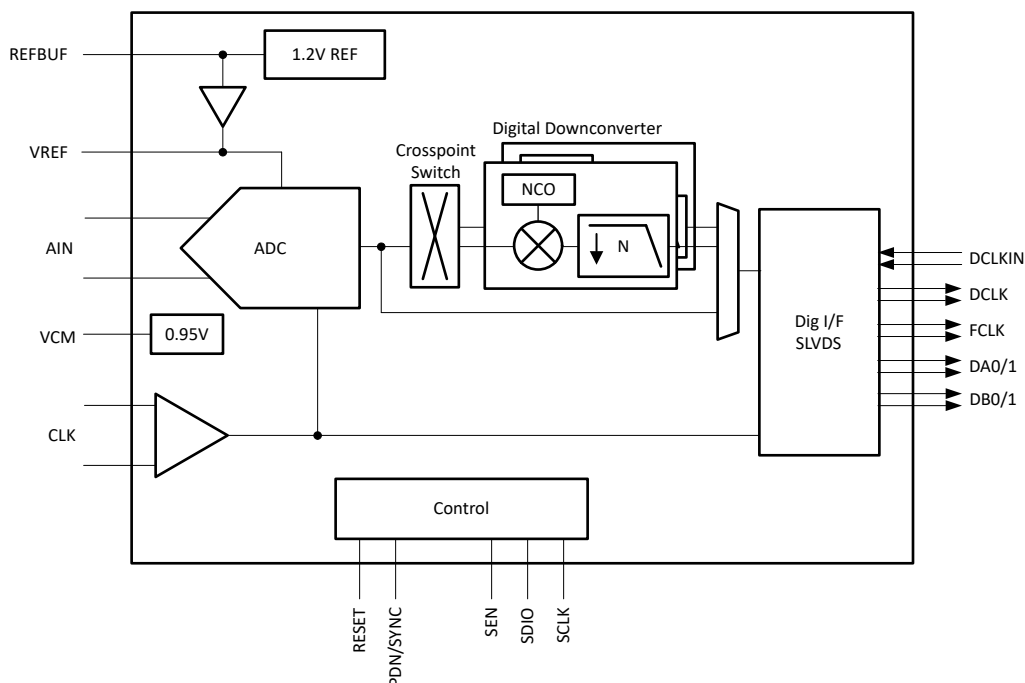
- External Reference: 10 to 125 MSPS
- Internal Reference: 100 to 125 MSPS

An optional, programmable digital down converter enables external anti-alias filter relaxation as well as output data rate reduction. The digital filter provides a 32-bit programmable NCO and supports both real or complex decimation.

The ADC3564 uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects. The device supports a two-lane (2-wire), a one-lane (1-wire) and a half-lane (1/2-wire) option. The ADC3564 includes a digital output formatter which supports output resolutions from 14 to 20-bit.

The device features and control options can be set up either through pin configurations or via SPI register writes.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The analog inputs of ADC3564 are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common mode voltage of 0.95 V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The equivalent input network diagram is shown in [Figure 8-1](#). All four sampling switches, on-resistance shown in red, are in same position (open or closed) simultaneously.

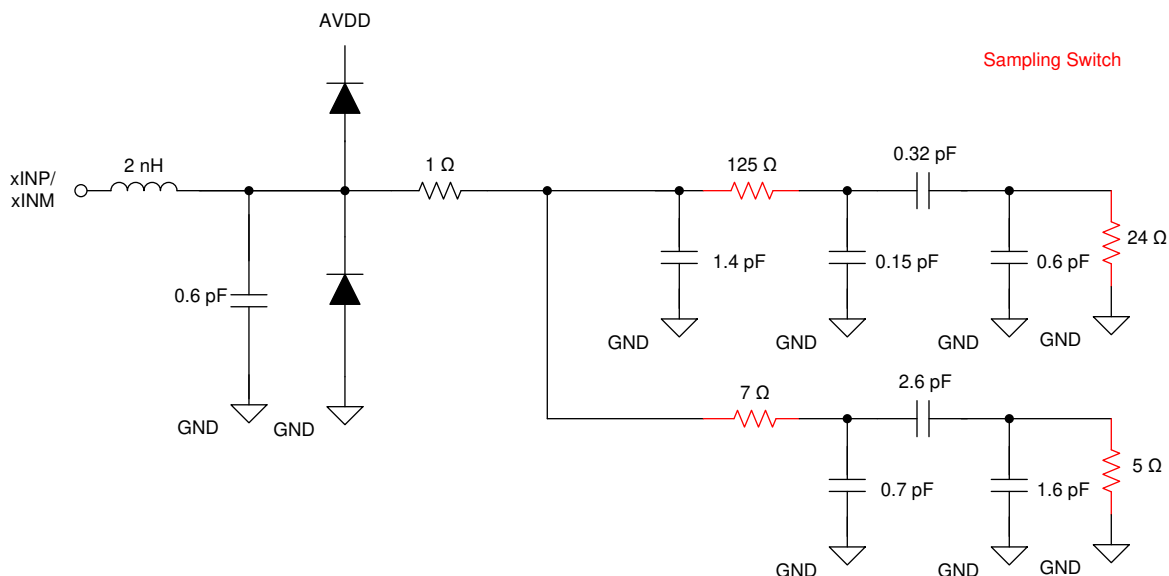


Figure 8-1. Equivalent Input Network

8.3.1.1 Analog Input Bandwidth

[Figure 8-2](#) shows the analog full power input bandwidth of the ADC3564 with a 50 Ω differential termination. The -3 dB bandwidth is approximately 1.4 GHz and the useful input bandwidth with good AC performance is approximately 200 MHz.

The equivalent differential input resistance R_{IN} and input capacitance C_{IN} vs frequency are shown in [Figure 8-3](#).

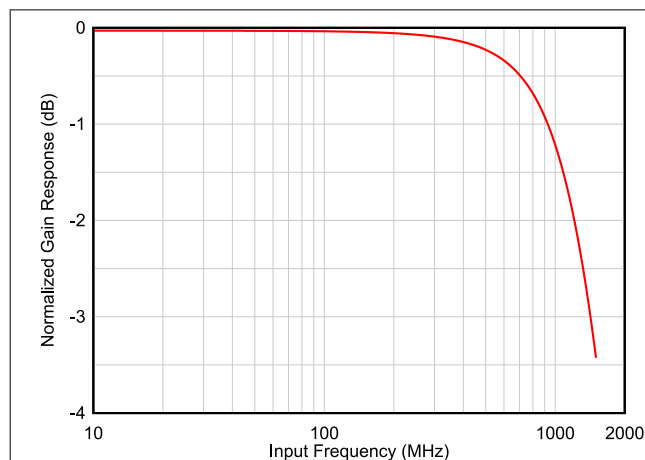


Figure 8-2. ADC Analog Input bandwidth response

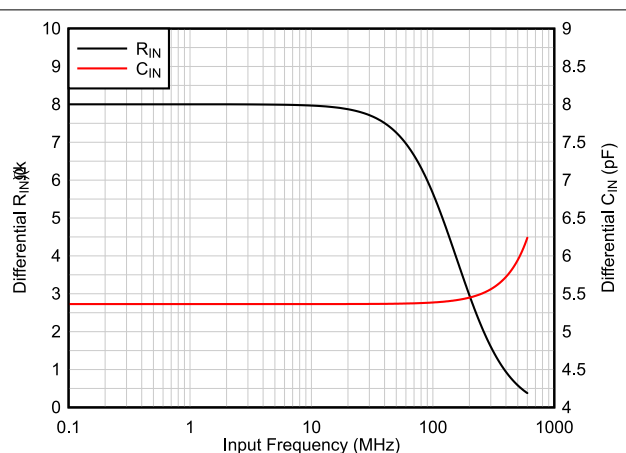


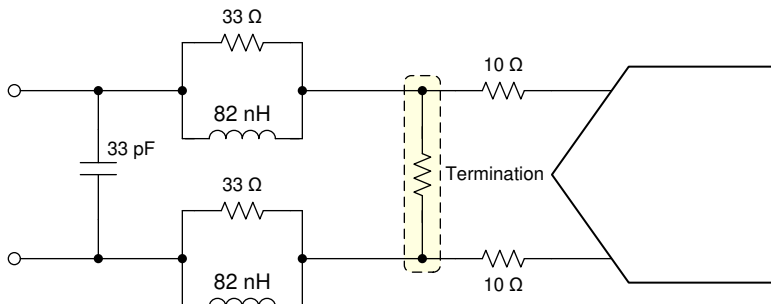
Figure 8-3. Equivalent R_{IN}/C_{IN} vs Input Frequency

8.3.1.2 Analog Front End Design

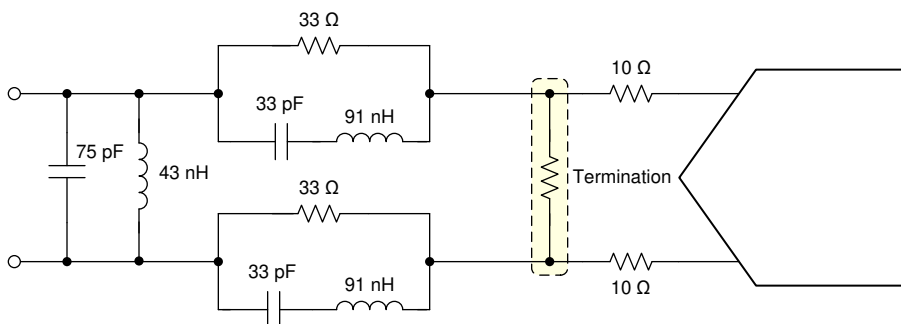
The ADC3564 is an unbuffered ADC and thus a passive kick-back filter is recommended to absorb the glitch from the sampling operation. Depending on if the input is driven by a balun or a differential amplifier with low output impedance, a termination network may be needed. Additionally a passive DC bias circuit is needed in AC-coupled applications which can be combined with the termination network.

8.3.1.2.1 Sampling Glitch Filter Design

The front end sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency and therefore the following filter designs are recommended for different input frequency ranges as shown in [8-4](#) and [8-5](#).



8-4. Sampling glitch filter example for input frequencies from DC to 60 MHz



8-5. Sampling glitch filter example for input frequencies from 60 to 120 MHz

8.3.1.2.2 Analog Input Termination and DC Bias

Depending on the input drive circuitry, a termination network and/or DC biasing needs to be provided.

8.3.1.2.2.1 AC-Coupling

The ADC3564 requires external DC bias using the common mode output voltage (VCM) of the ADC together with the termination network as shown in [Figure 8-6](#). The termination is located within the glitch filter network. When using a balun on the input, the termination impedance has to be adjusted to account for the turns ratio of the transformer. When using an amplifier, the termination impedance can be adjusted to optimize the amplifier performance.

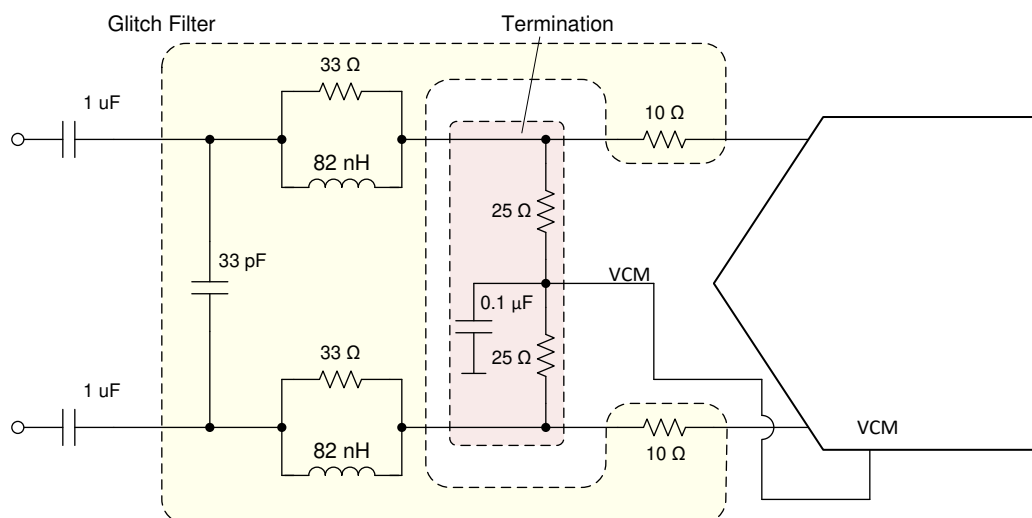


Figure 8-6. AC-Coupling: termination network provides DC bias (glitch filter example for up to 60 MHz)

8.3.1.2.2.2 DC-Coupling

In DC coupled applications the DC bias needs to be provided from the fully differential amplifier (FDA) using VCM output of the ADC as shown in [Figure 8-7](#). The glitch filter in this case is located between the anti-alias filter and the ADC. No termination may be needed if amplifier is located close to the ADC or if the termination is part of the anti-alias filter.

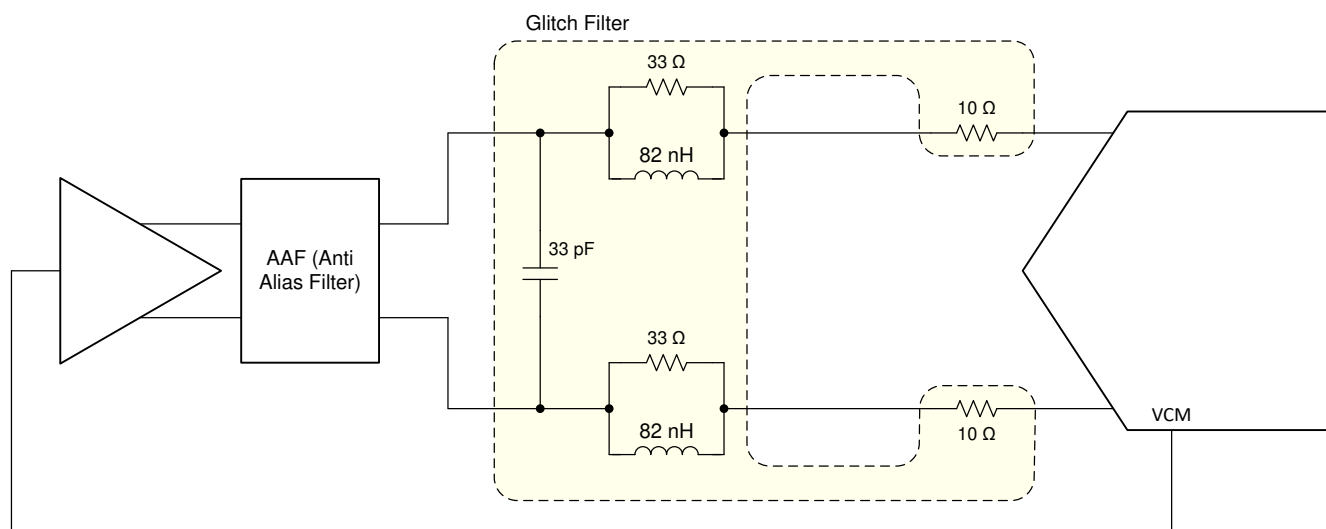


Figure 8-7. DC-Coupling: DC bias provided by FDA (glitch filter example for DC - 60 MHz)

8.3.2 Clock Input

In order to maximize the ADC SNR performance, the external sampling clock should be low jitter and differential signaling with a high slew rate. This is especially important in IF sampling applications. For less jitter sensitive applications, the ADC3564 provides the option to operate with single ended signaling which saves additional power consumption.

8.3.2.1 Single Ended vs Differential Clock Input

The ADC3564 can be operated using a differential or a single ended clock input where the single ended clock consumes less power consumption. However clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, a large clock signal with fast slew rates needs to be provided.

- **Differential Clock Input:** The clock input can be AC coupled externally. The ADC3564 provides internal biasing for that use case.
- **Single Ended Clock Input:** This mode needs to be configured using SPI register (0x0E, D2 and D0) or with the REFBUF pin. In this mode there is no internal clock biasing and thus the clock input needs to be DC coupled around a 0.9V center. The unused input needs to be AC coupled to ground.

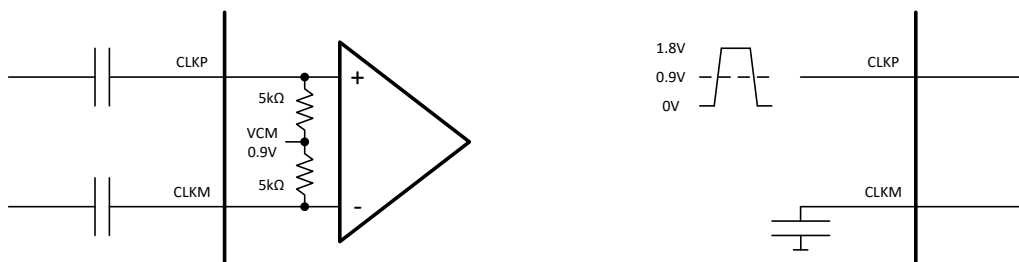


FIG 8-8. External and internal connection using differential (left) and single ended (right) clock input

8.3.3 Voltage Reference

The ADC3564 provides three different options for supplying the voltage reference to the ADC. An external 1.6 V reference can be directly connected to the VREF input; a voltage 1.2 V reference can be connected to the REFBUF input using the internal gain buffer or the internal 1.2V reference can be enabled to generate a 1.6 V reference voltage. For best performance, the reference noise should be filtered by connecting a 10 uF and a 0.1 uF ceramic bypass capacitor to the VREF pin. The internal reference circuitry of the ADC3564 is shown in [Figure 8-9](#).

注

The voltage reference mode can be selected using SPI writes or by using the REFBUF pin (default) as a control pin ([Section 8.5.1](#)). If the REFBUF pin is not used for configuration, the REFBUF pin should be connected to AVDD (even though the REFBUF pin has a weak internal pullup to AVDD) and the voltage reference option has to be selected using the SPI interface.

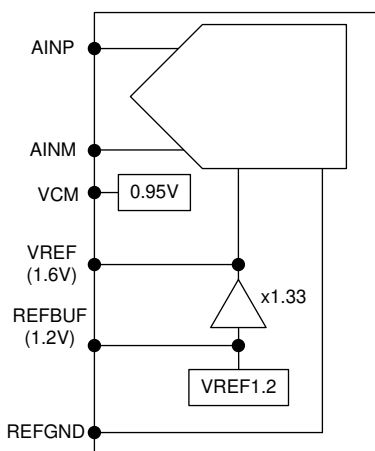


Figure 8-9. Different voltage reference options for ADC3564

8.3.3.1 Internal voltage reference

The 1.6V reference for the ADC can be generated internal using the on-chip 1.2 V reference along with the internal gain buffer. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) should be connected between the VREF and REFGND pins as close to the pins as possible.

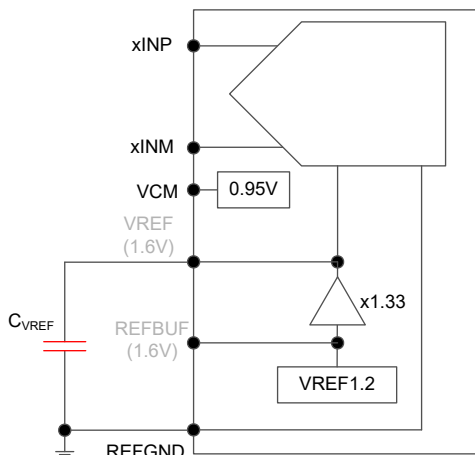


Figure 8-10. Internal reference

8.3.3.2 External voltage reference (VREF)

For highest accuracy and lowest temperature drift, the VREF input can be directly connected to an external 1.6 V reference. A 10 μ F and a 0.1 μ F ceramic bypass capacitor (C_{VREF}) connected between the VREF and REFGND pins and placed as close to the pins as possible is recommended. The load current from the external reference is about 1 mA.

注

The internal reference is also used for other functions inside the device, therefore the reference amplifier should only be powered down in power down state but not during normal operation.

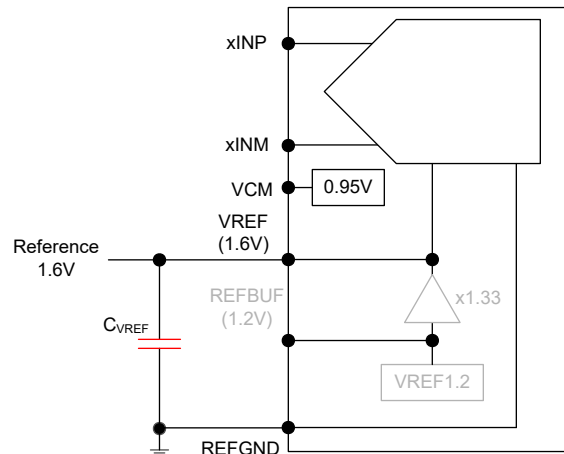


図 8-11. External 1.6V reference

8.3.3.3 External voltage reference with internal buffer (REFBUF)

The ADC3564 is equipped with an on-chip reference buffer that also includes gain to generate the 1.6 V reference voltage from an external 1.2V reference. A 10 μ F and a 0.1 μ F ceramic bypass capacitor (C_{VREF}) between the VREF and REFGND pins and a 10 μ F and a 0.1 μ F ceramic bypass capacitor between the REFBUF and REFGND pins are recommended. Both capacitors should be placed as close to the pins as possible. The load current from the external reference is less than 100 μ A.

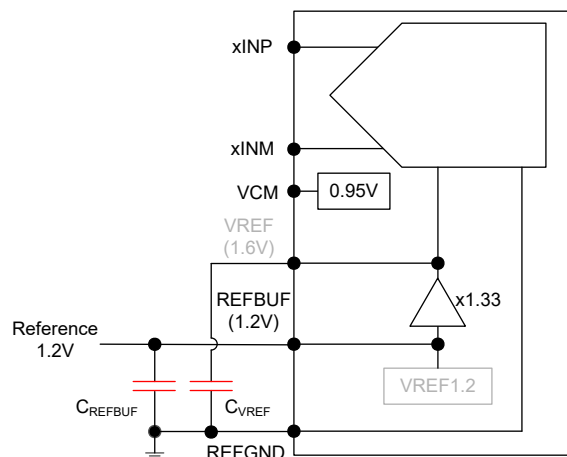


図 8-12. External 1.2V reference using internal reference buffer

8.3.4 Digital Down Converter

The ADC3564 includes an optional on-chip digital down conversion (DDC) decimation filter that can be enabled via SPI register setting. It supports complex decimation by 2, 4, 8, 16 and 32 using a digital mixer and a 32-bit numerically controlled oscillator (NCO) as shown in [Figure 8-13](#). Furthermore it supports a mode with real decimation where the complex mixer is bypassed (NCO should be set to 0 for lowest power consumption) and the digital filter acts as a low pass filter.

Internally the decimation filter calculations are performed with a 20-bit resolution in order to avoid any SNR degradation due to quantization noise. The [Section 8.3.5.1](#) truncates to the selected resolution prior to outputting the data on the digital interface.

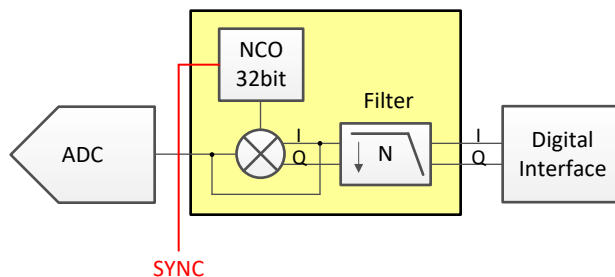


Figure 8-13. Internal Digital Decimation Filter

8.3.4.1 DDC MUX for Dual Band Decimation

The ADC3564 includes a MUX in front of the digital decimation filter which allows the ADC to be connected to two digital down converters (see [Figure 8-14](#)). This enables dual band complex decimation. The NCO of each digital down converter can be tuned to an independent frequency across the Nyquist zone as illustrated in the example in [Figure 8-15](#). The second DDC is output using the DB0/1 SLVDS interface.

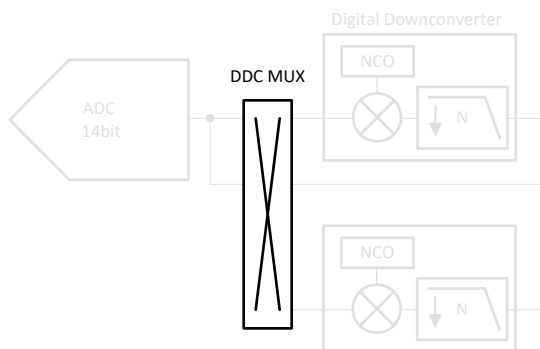


Figure 8-14. DDC MUX

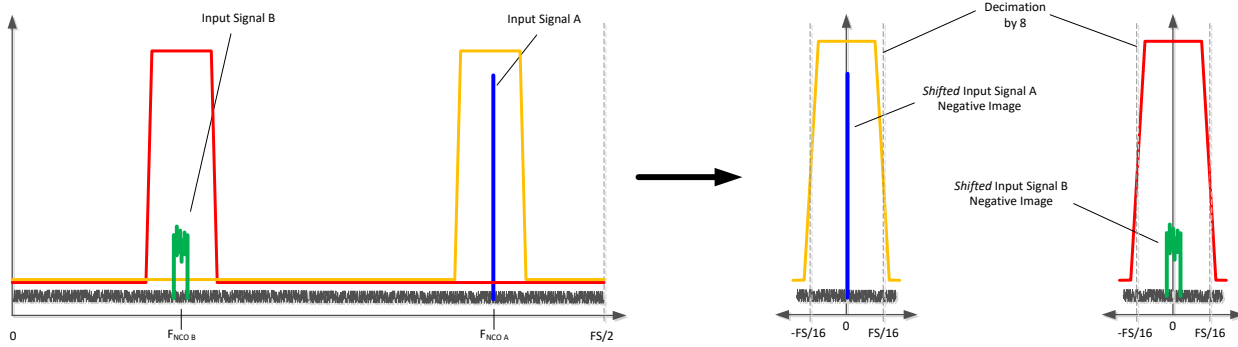


图 8-15. Complex Decimation (by 8) with dual band illustration

8.3.4.2 Digital Filter Operation

The complex decimation operation is illustrated with an example in [Figure 8-16](#). First the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left. Next a digital filter is applied (centered around 0 Hz) and the output data rate is decimated - in this example the output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$. During the complex mixing the spectrum (signal and noise) is split into real and complex parts and thus the amplitude is reduced by 6-dB. In order to compensate this loss, there is a 6-dB digital gain option in the decimation filter block that can be enabled via SPI write.

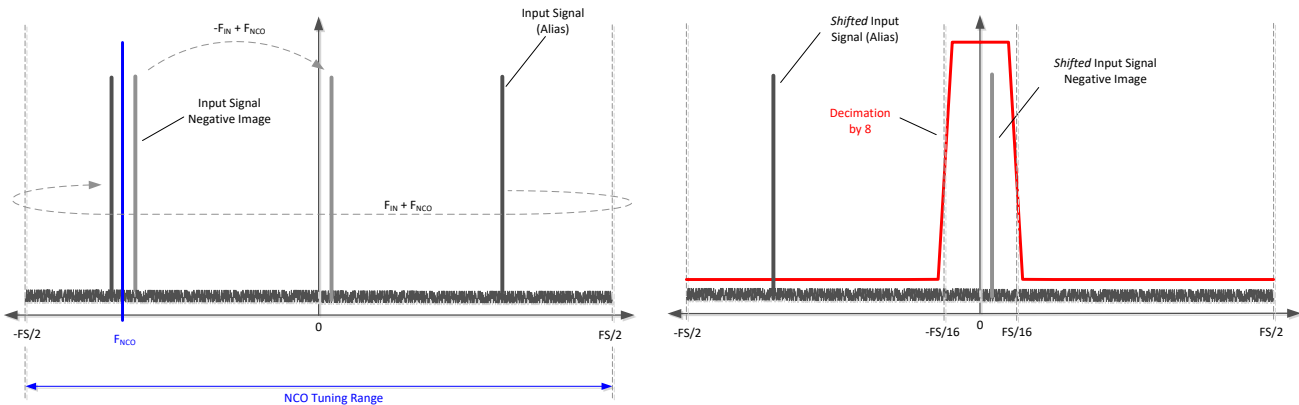


Figure 8-16. Complex decimation illustration

The real decimation operation is illustrated with an example in [Figure 8-17](#). There is no frequency shift happening and only the real portion of the complex digital filter is exercised. The output data rate is decimated - a decimation of 8 would result in an output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$.

During the real mixing the spectrum (signal and noise) amplitude is reduced by 3-dB. In order to compensate this loss, there is a 3-dB digital gain option in the decimation filter block that can be enabled via SPI write.

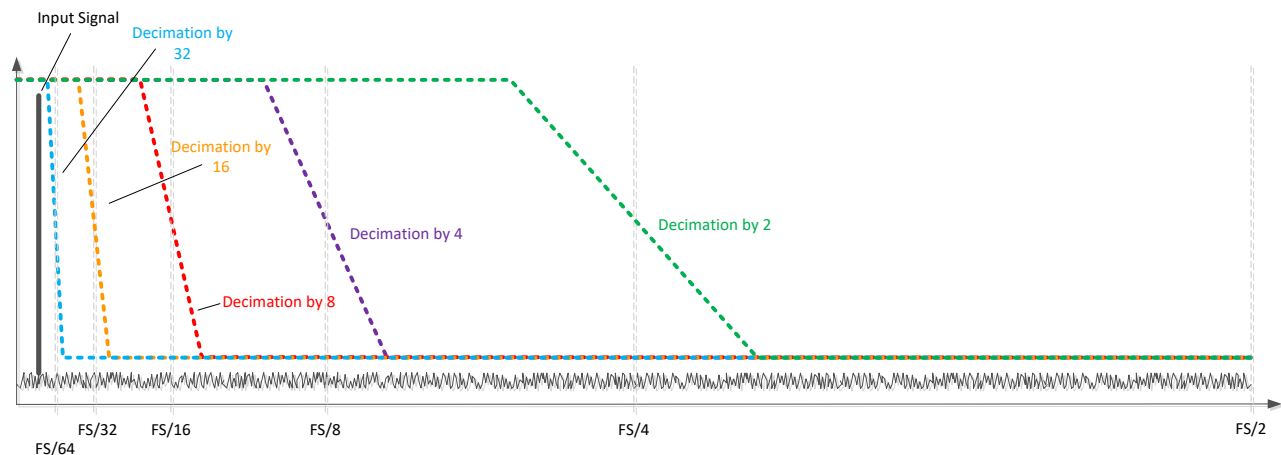


Figure 8-17. Real decimation illustration

8.3.4.3 FS/4 Mixing with Real Output

In this mode, the output after complex decimation gets mixed with FS/4 (FS = output data rate in this case). Instead of a complex output with the input signal centered around 0 Hz, the output is transmitted as a real output at twice the data rate and the signal is centered around FS/4 (Fout/4) as illustrated in 图 8-18.

In this example, complex decimation by 8 is used. The output data is transmitted as a real output with an output rate of Fout = FS'/4 (FS' = ADC sampling rate). The input signal is now centered around FS/4 (Fout/4) or FS'/16.

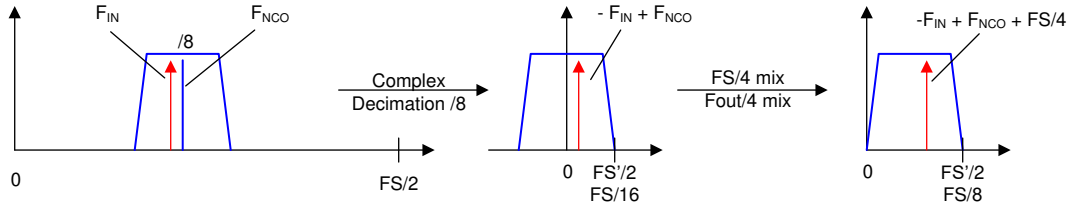


图 8-18. FS/4 Mixing with real output

8.3.4.4 Numerically Controlled Oscillator (NCO) and Digital Mixer

The decimation block is equipped with a 32-bit NCO and a digital mixer to fine tune the frequency placement prior to the digital filtering. The oscillator generates a complex exponential sequence of:

$e^{j\omega n}$ (default) or $e^{-j\omega n}$

where: frequency (ω) is specified as a signed number by the 32-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, the MIXER RESTART register bit or SYNC pin has to be toggled for the new frequency to get active. Additionally the ADC3564 provides the option via SPI to invert the mixer phase.

The NCO frequency setting is set by the 32-bit register value given and calculated as:

NCO frequency = 0 to $+F_S/2$: $NCO = f_{NCO} \times 2^{32} / F_S$

NCO frequency = $-F_S/2$ to 0: $NCO = (f_{NCO} + F_S) \times 2^{32} / F_S$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is further illustrated with this example:

- ADC sampling rate $F_S = 125$ MSPS
- Input signal $f_{IN} = 10$ MHz
- Desired output frequency $f_{OUT} = 0$ MHz

For this example there are actually four ways to program the NCO and achieve the desired output frequency as shown in 表 8-1.

表 8-1. NCO value calculations example

| Alias or negative image | f_{NCO} | NCO Value | Mixer Phase | Frequency translation for f_{OUT} |
|-------------------------|---------------------|-----------|-------------|--|
| $f_{IN} = -10$ MHz | $f_{NCO} = 10$ MHz | 343597384 | as is | $f_{OUT} = f_{IN} + f_{NCO} = -10 \text{ MHz} + 10 \text{ MHz} = 0 \text{ MHz}$ |
| $f_{IN} = 10$ MHz | $f_{NCO} = -10$ MHz | 373475417 | | $f_{OUT} = f_{IN} + f_{NCO} = 10 \text{ MHz} + (-10 \text{ MHz}) = 0 \text{ MHz}$ |
| $f_{IN} = 10$ MHz | $f_{NCO} = 10$ MHz | 343597384 | inverted | $f_{OUT} = f_{IN} - f_{NCO} = 10 \text{ MHz} - 10 \text{ MHz} = 0 \text{ MHz}$ |
| $f_{IN} = -10$ MHz | $f_{NCO} = -10$ MHz | 373475417 | | $f_{OUT} = f_{IN} - f_{NCO} = -10 \text{ MHz} - (-10 \text{ MHz}) = 0 \text{ MHz}$ |

8.3.4.5 Decimation Filter

The ADC3564 supports complex decimation by 2, 4, 8, 16 and 32 with a pass-band bandwidth of ~ 80% and a stopband rejection of at least 85 dB. 表 8-2 gives an overview of the pass-band bandwidth of the different decimation settings with respect to ADC sampling rate F_S . In real decimation mode the output bandwidth is half of the complex bandwidth.

表 8-2. Decimation Filter Summary and Maximum Available Output Bandwidth

| REAL/COMPLEX DECIMATION | DECIMATION SETTING N | OUTPUT RATE | OUTPUT BANDWIDTH | OUTPUT RATE ($F_S = 125$ MSPS) | OUTPUT BANDWIDTH ($F_S = 125$ MSPS) |
|-------------------------|----------------------|--------------------|-----------------------|---------------------------------|--------------------------------------|
| Complex | 2 | $F_S / 2$ complex | $0.8 \times F_S / 2$ | 62.5 MSPS complex | 50 MHz |
| | 4 | $F_S / 4$ complex | $0.8 \times F_S / 4$ | 31.25 MSPS complex | 25 MHz |
| | 8 | $F_S / 8$ complex | $0.8 \times F_S / 8$ | 15.625 MSPS complex | 12.5 MHz |
| | 16 | $F_S / 16$ complex | $0.8 \times F_S / 16$ | 7.8125 MSPS complex | 6.25 MHz |
| | 32 | $F_S / 32$ complex | $0.8 \times F_S / 32$ | 3.90625 MSPS complex | 3.125 MHz |
| Real | 2 | $F_S / 2$ real | $0.4 \times F_S / 2$ | 62.5 MSPS | 25 MHz |
| | 4 | $F_S / 4$ real | $0.4 \times F_S / 4$ | 31.25 MSPS | 12.5 MHz |
| | 8 | $F_S / 8$ real | $0.4 \times F_S / 8$ | 15.625 MSPS | 6.25 MHz |
| | 16 | $F_S / 16$ real | $0.4 \times F_S / 16$ | 7.8125 MSPS | 3.125 MHz |
| | 32 | $F_S / 32$ real | $0.4 \times F_S / 32$ | 3.90625 MSPS | 1.5625 MHz |

The decimation filter responses normalized to the ADC sampling clock frequency are illustrated in 图 8-20 to 图 8-29. They are interpreted as follows:

Each figure contains the filter pass-band, transition band(s) and alias or stop-band(s) as shown in 图 8-19. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate F_S .

For example, in the divide-by-4 complex setup, the output data rate is $F_S / 4$ complex with a Nyquist zone of $F_S / 8$ or $0.125 \times F_S$. The transition band (colored in blue) is centered around $0.125 \times F_S$ and the alias transition band is centered at $0.375 \times F_S$. The stop-bands (colored in red), which alias on top of the pass-band, are centered at $0.25 \times F_S$ and $0.5 \times F_S$. The stop-band attenuation is greater than 85 dB.

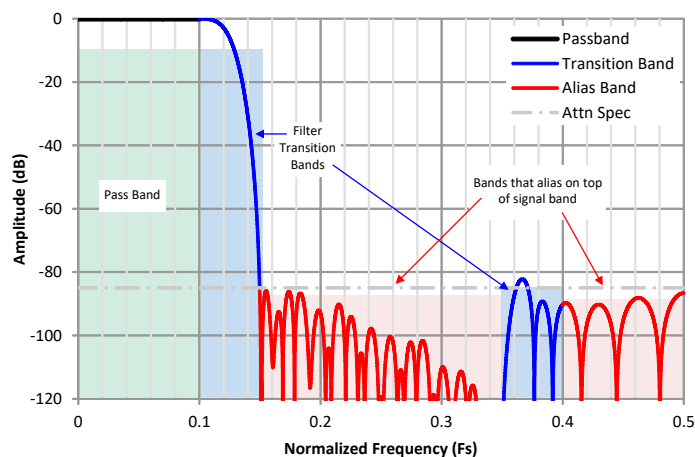
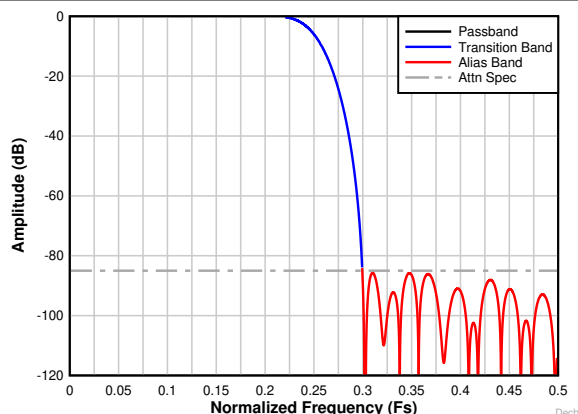
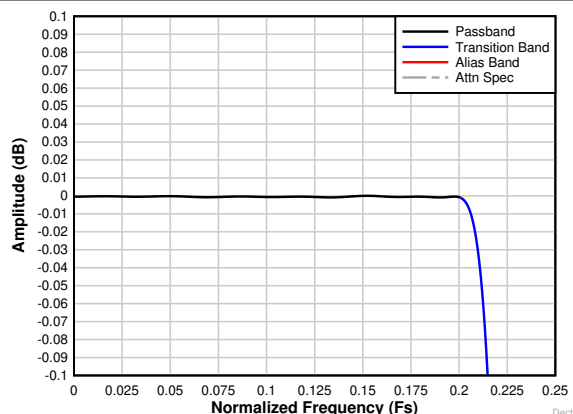


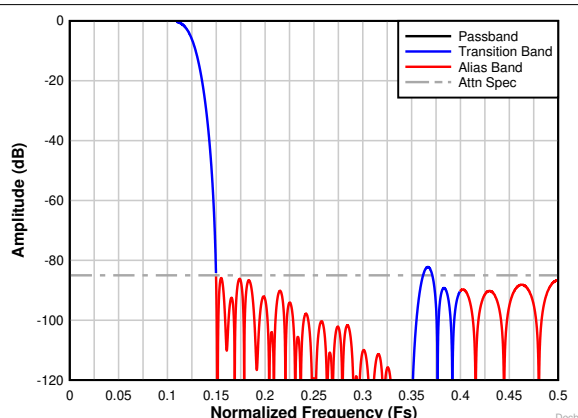
图 8-19. Interpretation of the Decimation Filter Plots



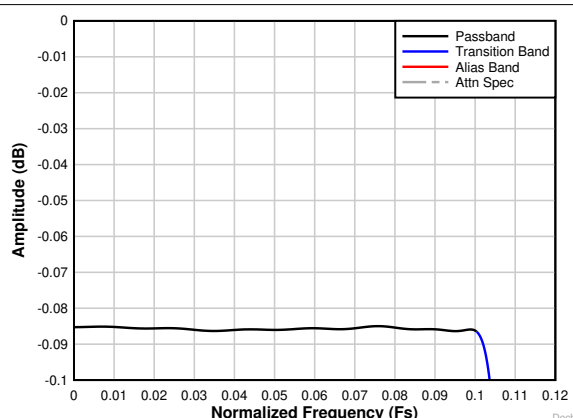
8-20. Decimation by 2 complex frequency response



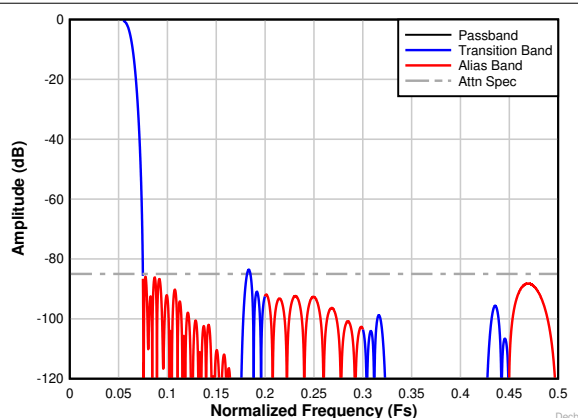
8-21. Decimation by 2 complex passband ripple response



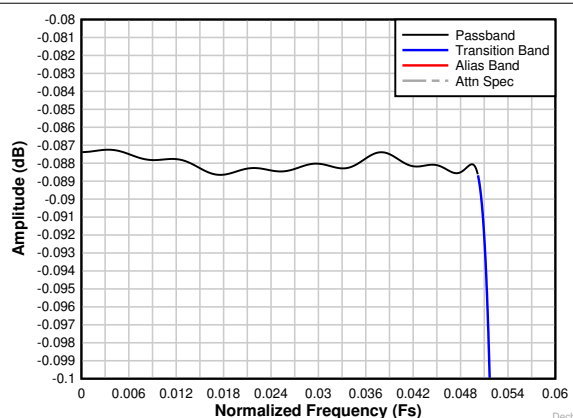
8-22. Decimation by 4 complex frequency response



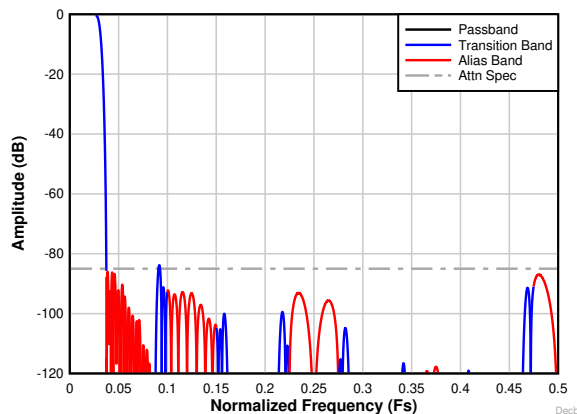
8-23. Decimation by 4 complex passband ripple response



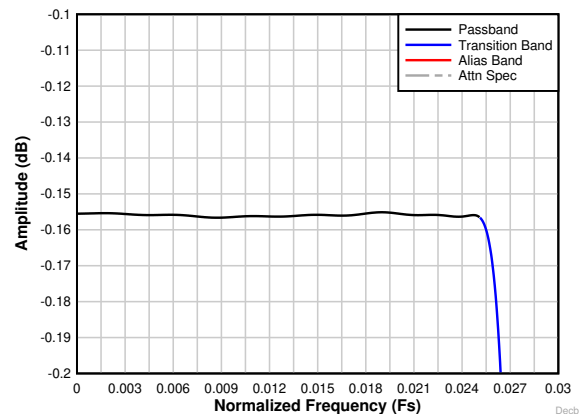
8-24. Decimation by 8 complex frequency response



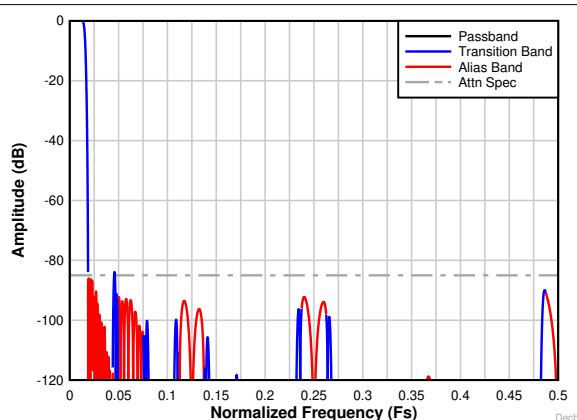
8-25. Decimation by 8 complex passband ripple response



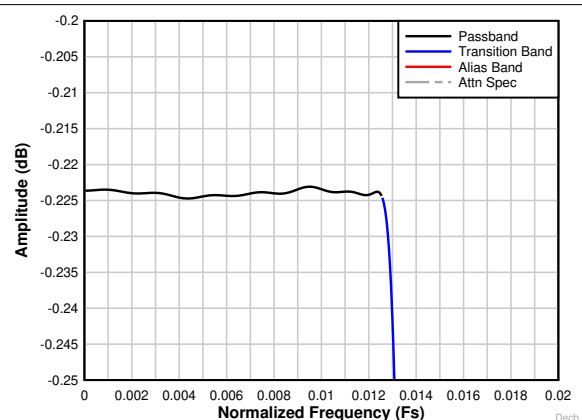
8-26. Decimation by 16 complex frequency response



8-27. Decimation by 16 complex passband ripple response



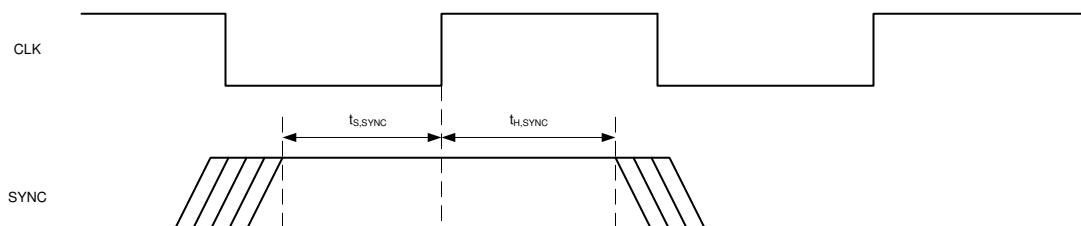
8-28. Decimation by 32 complex frequency response



8-29. Decimation by 32 complex passband ripple response

8.3.4.6 SYNC

The PDN/SYNC pin can be used to synchronize multiple devices using an external SYNC signal. The PDN/SYNC pin can be configured via SPI (SYNC EN bit) from power down to synchronization functionality and is latched in by the rising edge of the sampling clock as shown in 8-30.



8-30. External SYNC timing diagram

The synchronization signal is only required when using the decimation filter - either using the SPI SYNC register or the PDN/SYNC pin. It resets internal clock dividers used in the decimation filter and aligns the internal clocks as well as I and Q data within the same sample. If no SYNC signal is given, the internal clock dividers is not be synchronized, which can lead to a fractional delay across different devices. The SYNC signal also resets the NCO phase and loads the new NCO frequency (same as the MIXER RESTART bit).

When trying to resynchronize during operation, the SYNC toggle should occur at $64 \cdot K$ clock cycles, where K is an integer. This provides the phase continuity of the clock divider.

8.3.4.7 Output Formatting with Decimation

When using decimation, the digital output data is formatted as shown in [Figure 8-31](#) (complex decimation) and [Figure 8-32](#) (real decimation). The output format is illustrated for 16-bit output resolution.

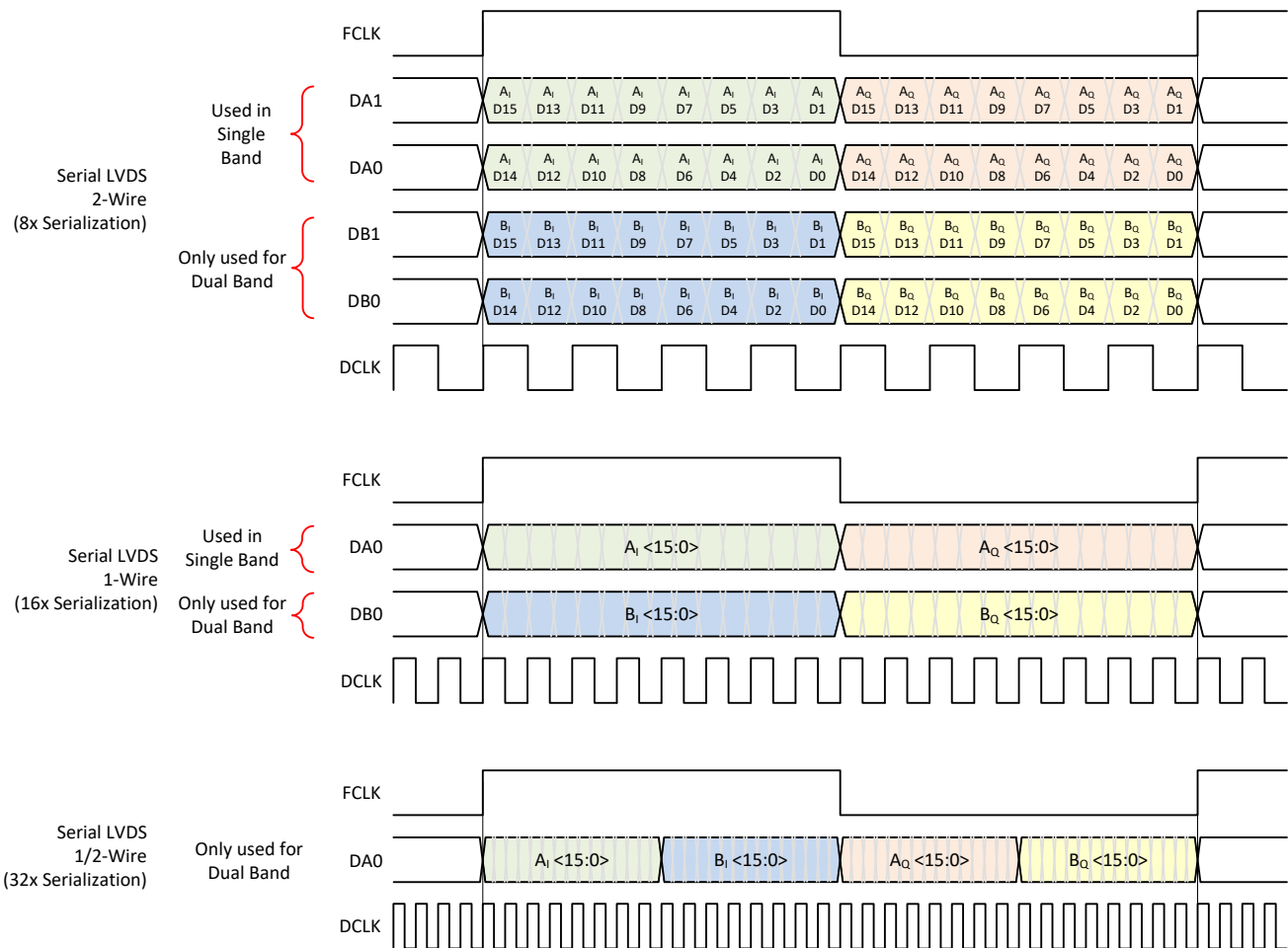


Figure 8-31. Output Data Format in Complex Decimation

[Table 8-3](#) illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and complex decimation setting (N).

Furthermore the table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 16-bit output resolution and complex decimation by 4.

Table 8-3. Serial LVDS Lane Rate Examples with Complex Decimation and 16-bit Output Resolution

| DECIMATION SETTING | ADC SAMPLING RATE | OUTPUT RESOLUTION | # of WIRES | FCLK | DCLKIN, DCLK | DA/B0,1 |
|--------------------|-------------------|-------------------|------------|------------|-----------------|---------------------------------|
| N | F_S | R | L | F_S / N | $[DA/B0,1] / 2$ | $F_S \times 2 \times R / L / N$ |
| 4 | 125 MSPS | 16 | 2 | 31.25 MHz | 250 MHz | 500 MHz |
| | | | 1 | | 500 MHz | 1000 MHz |
| | 55 MSPS | | 1/2 | 15.625 MHz | 500 MHz | 1000 MHz |

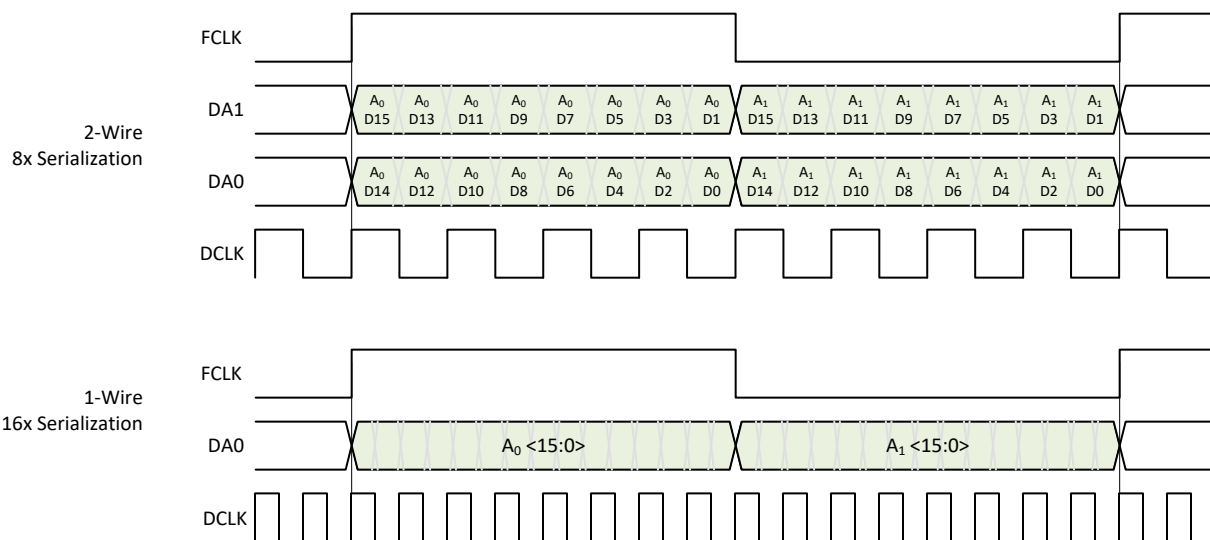


图 8-32. Output Data Format in Real Decimation

表 8-4 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and real decimation setting (M).

Furthermore the table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 16-bit output resolution and real decimation by 4.

表 8-4. Serial LVDS Lane Rate Examples with Real Decimation and 16-bit Output Resolution

| DECIMATION SETTING | ADC SAMPLING RATE | OUTPUT RESOLUTION | # of WIRES | FCLK | DCLKIN, DCLK | DA/B0,1 |
|--------------------|-------------------|-------------------|------------|---|-----------------|------------------------|
| M | F_S | R | L | $F_S / M / 2$ (L = 2) F_S / M (L = 1, 1/2) | $[DA/B0,1] / 2$ | $F_S \times R / L / M$ |
| 4 | 125 MSPS | 16 | 2 | 15.625 MHz | 125 MHz | 250 MHz |
| | | | 1 | 31.25 MHz | 250 MHz | 500 MHz |
| | | | 1/2 | | 500 MHz | 1000 MHz |

8.3.5 Digital Interface

The serial LVDS interface supports the data output with 2-wire, 1-wire and 1/2-wire operation. The actual data output rate depends on the output resolution and number of lanes used.

The ADC3564 requires an external serial LVDS clock input (DCLKIN), which is used to transmit the data out of the ADC along with the data clock (DCLK). The phase relationship between DCLKIN and the sampling clock is irrelevant but both clocks need to be frequency locked. The SLVDS interface is configured using SPI register writes.

8.3.5.1 Output Formatter

The digital output interface utilizes a flexible output bit mapper as shown in [Figure 8-33](#). The bit mapper takes the 14-bit output directly from the ADC or from digital filter block and reformats it to a resolution of 14, 16, 18 or 20-bit. The output serialization factor gets adjusted accordingly for 2-, 1- and 1/2-wire interface modes. The maximum SLVDS interface output data rate can not be exceeded independent of output resolution or serialization factor.

When using a higher resolution like 16-bit output for example in non-decimation mode, the 2 LSBs are set to 0.

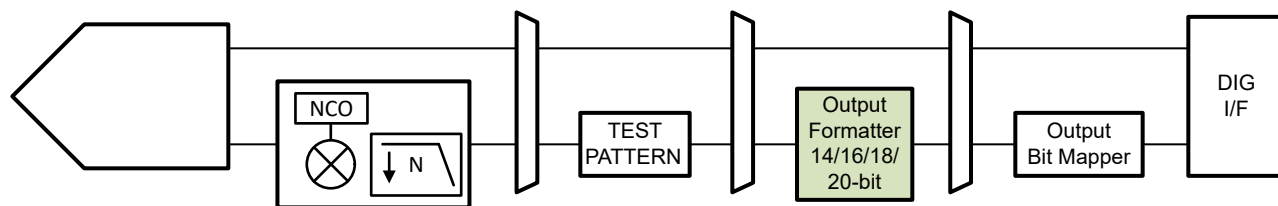


Figure 8-33. Interface output bit mapper

[Table 8-5](#) provides an overview for the resulting serialization factor depending on output resolution and output modes. Note that the DCLKIN frequency needs to be adjusted accordingly as well. Changing the output resolution to 16-bit, 2-wire mode for example would result in $DCLKIN = F_S * 4$ instead of $* 3.5$.

The output bit mapper can be used for bypass and decimation filter.

Table 8-5. Serialization factor vs output resolution for different output modes

| OUTPUT RESOLUTION | Interface | SERIALIZATION | FCLK | DCLKIN | DCLK | D0/D1 |
|-------------------|-----------|---------------|---------|-------------|-------------|------------|
| 14-bit (default) | 2-Wire | 7x | $F_S/2$ | $F_S * 3.5$ | $F_S * 3.5$ | $F_S * 7$ |
| | 1-Wire | 14x | F_S | $F_S * 7$ | $F_S * 7$ | $F_S * 14$ |
| | 1/2-Wire | 28x | F_S | $F_S * 14$ | $F_S * 14$ | $F_S * 28$ |
| 16-bit | 2-Wire | 8x | $F_S/2$ | $F_S * 4$ | $F_S * 4$ | $F_S * 8$ |
| | 1-Wire | 16x | F_S | $F_S * 8$ | $F_S * 8$ | $F_S * 16$ |
| | 1/2-Wire | 32x | F_S | $F_S * 16$ | $F_S * 16$ | $F_S * 32$ |
| 18-bit | 2-Wire | 9x | $F_S/2$ | $F_S * 4.5$ | $F_S * 4.5$ | $F_S * 9$ |
| | 1-Wire | 18x | F_S | $F_S * 9$ | $F_S * 9$ | $F_S * 18$ |
| | 1/2-Wire | 36x | F_S | $F_S * 18$ | $F_S * 18$ | $F_S * 36$ |
| 20-bit | 2-Wire | 10x | $F_S/2$ | $F_S * 5$ | $F_S * 5$ | $F_S * 10$ |
| | 1-Wire | 20x | F_S | $F_S * 10$ | $F_S * 10$ | $F_S * 20$ |
| | 1/2-Wire | 40x | F_S | $F_S * 20$ | $F_S * 20$ | $F_S * 40$ |

The programming sequence to change the output interface and/or resolution from default settings is shown in [Section 8.3.5.3](#).

8.3.5.2 Output Bit Mapper

The output bit mapper allows to change the output bit order for any selected interface mode.

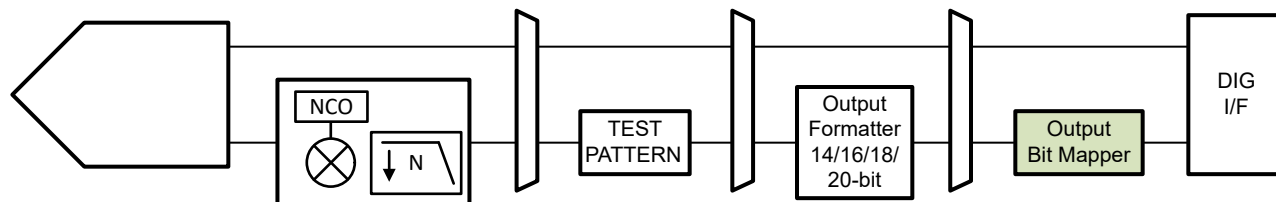


图 8-34. Output Bit Mapper

It is a two step process to change the output bit mapping and assemble the output data bus:

1. Both channel A and B can have up to 20-bit output. Each output bit of either channel has a unique identifier bit as shown in 表 8-6. The MSB starts with bit D19 – depending on output resolution chosen the LSB would be D6 (14-bit) to D0 (20-bit). The *previous sample* is only needed in 2-w mode.
2. The bit mapper is then used to assemble the output sample. The following sections detail how to remap the serial output format.

表 8-6. Unique identifier of each data bit

| Bit | Channel A | | Channel B | |
|-----------|---------------------------|----------------|---------------------------|----------------|
| | Previous sample (2w only) | Current sample | Previous sample (2w only) | Current sample |
| D19 (MSB) | 0x2D | 0x6D | 0x29 | 0x69 |
| D18 | 0x2C | 0x6C | 0x28 | 0x68 |
| D17 | 0x27 | 0x67 | 0x23 | 0x63 |
| D16 | 0x26 | 0x66 | 0x22 | 0x62 |
| D15 | 0x25 | 0x65 | 0x21 | 0x61 |
| D14 | 0x24 | 0x64 | 0x20 | 0x60 |
| D13 | 0x1F | 0x5F | 0x1B | 0x5B |
| D12 | 0x1E | 0x5E | 0x1A | 0x5A |
| D11 | 0x1D | 0x5D | 0x19 | 0x59 |
| D10 | 0x1C | 0x5C | 0x18 | 0x58 |
| D9 | 0x17 | 0x57 | 0x13 | 0x53 |
| D8 | 0x16 | 0x56 | 0x12 | 0x52 |
| D7 | 0x15 | 0x55 | 0x11 | 0x51 |
| D6 | 0x14 | 0x54 | 0x10 | 0x50 |
| D5 | 0x0F | 0x4F | 0x0B | 0x4B |
| D4 | 0x0E | 0x4E | 0x0A | 0x4A |
| D3 | 0x0D | 0x4D | 0x09 | 0x49 |
| D2 | 0x0C | 0x4C | 0x08 | 0x48 |
| D1 | 0x07 | 0x47 | 0x03 | 0x43 |
| D0 (LSB) | 0x06 | 0x46 | 0x02 | 0x42 |

In the serial output mode, a data bit (with unique identifier) needs to be assigned to each location within the serial output stream. There are a total of 40 addresses available per channel. Channel A spans from address 0x39 to 0x60 and channel B from address 0x61 to 0x88. When using complex decimation, the output bit mapper is applied to both the “I” and the “Q” sample.

2-wire mode: in this mode both the current and the previous sample have to be used in the address space as shown in [Figure 8-35](#). The address order is different for 14/18-bit and 16/20-bit. Note: there are unused addresses between samples for resolution less than 20-bit (grey back ground), which can be skipped if not used.

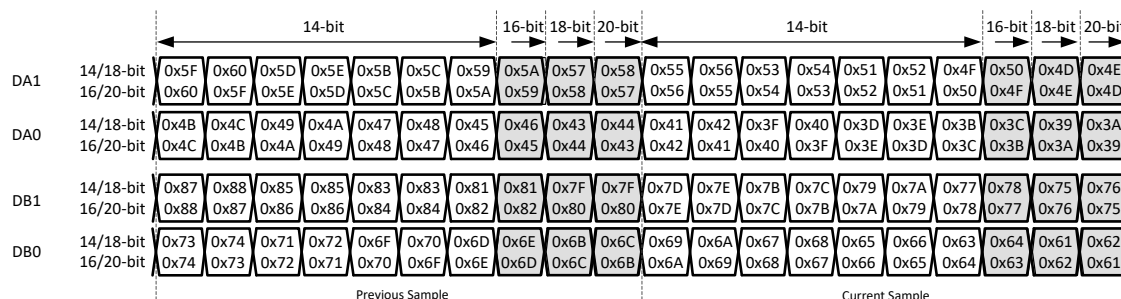


Figure 8-35. 2-wire output bit mapper

In the following example ([Figure 8-36](#)), the 16-bit 2-wire serial output is reordered to where lane DA1/DB1 carries the 8 MSB and lane DA0/DB0 carries 8 LSBs.

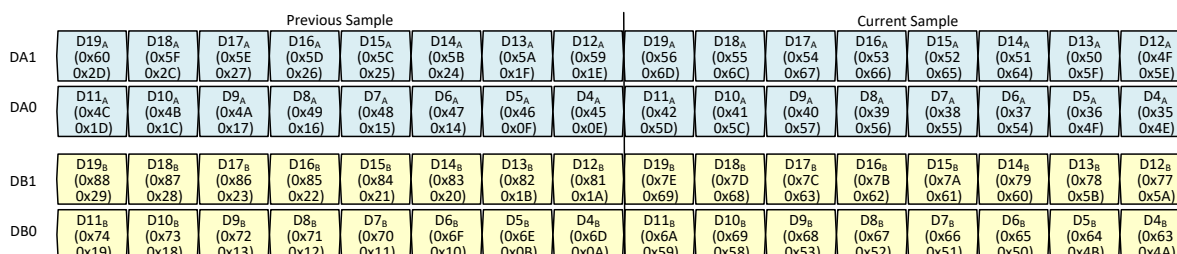


Figure 8-36. Example: 2-wire output bit mapping

1-wire mode: Only the *current* sample needs to be programmed in the address space. If desired, it can be duplicated on DA1/DB1 as well (using addresses shown below) in order to have a redundant output. Lane DA1/DB1 needs to be powered up in that case.



Figure 8-37. 1-wire output bit mapping

1/2-wire mode: The output is only lane DA0 and the sample order is programmed into the 40 addresses of chA (from 0x39 to 0x60). It covers 2 samples (one for chA, one for chB) as shown below. If desired it can be duplicated on DB0 as well (using addresses shown [Figure 8-38](#)) in order to have a redundant output. Lane DB0 needs to be powered up in that case.

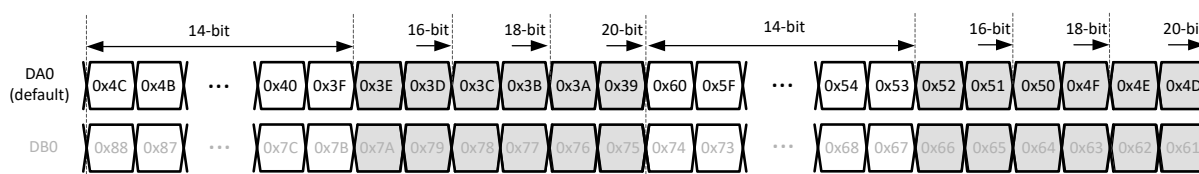


Figure 8-38. 1/2-wire output bit mapping

8.3.5.3 Output Interface/Mode Configuration

The following sequence summarizes all the relevant registers for changing the output interface and/or enabling the decimation filter. Steps 1 and 2 must come first since the E-Fuse load reset the SPI writes, the remaining steps can come in any order.

表 8-7. Configuration steps for changing interface or decimation

| STEP | FEATURE | ADDRESS | DESCRIPTION | | | | | |
|------|--------------------------|---|---|---------------|---|------------------------------|---------------|--|
| 1 | Output Interface | 0x07 | Select the output interface bit mapping depending on resolution and output interface. | | | | | |
| | | | Output Resolution | | 2-wire | 1-wire | 1/2-wire | |
| | | | 14-bit | | 0x2B | 0x6C | 0x8D | |
| | | | 16-bit | | 0x4B | | | |
| | | | 18-bit | | 0x2B | | | |
| | | | 20-bit | | 0x4B | | | |
| 2 | | 0x13 | Load the output interface bit mapping using the E-fuse loader (0x13, D0). Program register 0x13 to 0x01, wait ~ 1ms so that bit mapping is loaded properly followed by 0x13 0x00. | | | | | |
| 3 | | 0x19 | Configure the FCLK frequency based on bypass/decimation and number of lanes used. | | | | | |
| | | | Bypass/Dec | SLVDS | FCLK SRC (D7) | FCLK DIV (D4) | TOG FCLK (D0) | |
| | | | Bypass/ Real Decimation | 2-wire | 0 | 1 | 0 | |
| | | | | 1-wire | 0 | 0 | 0 | |
| | | | | 1/2-wire | 0 | 0 | 0 | |
| | | | Complex Decimation | 2-wire | 1 | 0 | 0 | |
| | | | | 1-wire | 1 | 0 | 0 | |
| | | | | 1/2-wire | 0 | 0 | 1 | |
| 4 | | 0x1B | Select the output interface resolution using the bit mapper (D5-D3). | | | | | |
| 5 | | 0x20 0x21 0x22 | Select the FCLK pattern for decimation for proper duty cycle output of the frame clock. | | | | | |
| | | | Output Resolution | 2-wire | 1-wire | 1/2-wire | | |
| | Real Decimation | | 14-bit | use default | 0xFE000 | use default | | |
| | | | 16-bit | | 0xFF000 | | | |
| | | | 18-bit | | 0xFF800 | | | |
| | | | 20-bit | | 0xFFC00 | | | |
| | Complex Decimation | | 14-bit | | 0xFFFFF | 0xFFFFF | | |
| | | | 16-bit | | | | | |
| | | | 18-bit | | | | | |
| | | | 20-bit | | | | | |
| | 6 | | 0x39..0x60 0x61..0x88 | | Change output bit mapping for chA and chB if desired. This works also with the default interface selection. | | | |
| | 7 | | Decimation Filter | | 0x24 | Enable the decimation filter | | |
| 8 | 0x25 | Configure the decimation filter | | | | | | |
| 9 | 0x2A/B/C/D 0x31/2/3/4 | Program the NCO frequency for complex decimation (can be skipped for real decimation) | | | | | | |
| 10 | 0x27 0x2E | Configure the complex output data stream (set both bits to 0 for real decimation) | | | | | | |
| | | SLVDS | | OP-Order (D4) | Q-Delay (D3) | | | |
| | | 2-wire | | 1 | 0 | | | |
| | | 1-wire | | 0 | 1 | | | |
| | | 1/2-wire | | 1 | 1 | | | |
| 11 | | 0x26 | Set the mixer gain and toggle the mixer reset bit to update the NCO frequency. | | | | | |

8.3.5.3.1 Configuration Example

The following is a step by step programming example to configure the ADC3564 to complex decimation by 8 with 1-wire SLVDS and 16-bit output.

1. 0x07 (address) 0x6C (load bit mapper configuration for 16-bit output with 1-wire SLVDS)
2. 0x13 0x01 (load e-fuse), wait 1 ms, 0x13 0x00
3. 0x19 0x80 (configure FCLK)
4. 0x1B 0x88 (select 16-bit output resolution)
5. 0x20 0xFF, 0x21 0xFF, 0x22 0x0F (configure FCLK pattern)
6. 0x24 0x06 (enable decimation filter)
7. 0x25 0x30 (configure complex decimation by 8)
8. 0x2A/B/C/D and 0x31/32/33/34 (program NCO frequency)
9. 0x27/0x2E 0x08 (configure Q-delay register bit)
10. 0x26 0xAA, 0x26 0x88 (set digital mixer gain to 6-dB and toggle the mixer update)

8.3.5.4 Output Data Format

The output data can be configured to two's complement (default) or offset binary formatting using SPI register writes (register 0x8F and 0x92). 表 8-8 provides an overview for minimum and maximum output codes for the two formatting options. The actual output resolution is set by the output bit mapper.

表 8-8. Overview of minimum and maximum output codes vs output resolution for different formatting

| RESOLUTION (BIT) | Two's Complement (default) | | Offset Binary | |
|------------------|----------------------------|--------|---------------|--------|
| | 14 | 16 | 14 | 16 |
| $V_{IN,MAX}$ | 0x1FFF | 0x7FFF | 0x3FFF | 0xFFFF |
| 0 | 0x0000 | | 0x2000 | 0x8000 |
| $V_{IN,MIN}$ | 0x2000 | 0x8000 | 0x0000 | |

8.3.6 Test Pattern

In order to enable in-circuit testing of the digital interface, the following test patterns are supported and enabled via SPI register writes (0x14/0x15/0x16). The test pattern generator is located after the decimation filter as shown in 图 8-39. In decimation mode (real and complex), the test patterns replace the output data of the DDC - however channel A controls the test patterns for both channels.

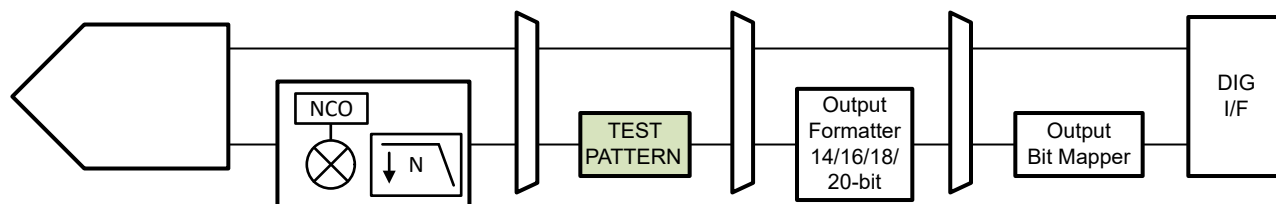


图 8-39. Test Pattern Generator

- RAMP Pattern: The step size needs to be configured in the CUSTOM PAT register according to the native resolution of the ADC. When selecting a higher output resolution then the additional LSBs will still be 0 in RAMP pattern mode.
 - 00001: 18-bit output resolution
 - 00100: 16-bit output resolution
 - 10000: 14-bit output resolution
- Custom Pattern: Configured in the CUSTOM PAT register

8.4 Device Functional Modes

8.4.1 Normal operation

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 14-bit resolution. The output is available in as little as 1 clock cycle with 1-wire SLVDS interface.

8.4.2 Power Down Options

A global power down mode can be enabled via SPI as well as using the power down pin (PDN/SYNC). There is an internal pull-down 21 kΩ resistor on the PDN/SYNC input pin and the pin is active high - so the pin needs to be pulled high externally to enter global power down mode.

The SPI register map provides the capability to enable/disable individual blocks directly or via PDN pin mask in order to trade off power consumption vs wake up time as shown in 表 8-9.

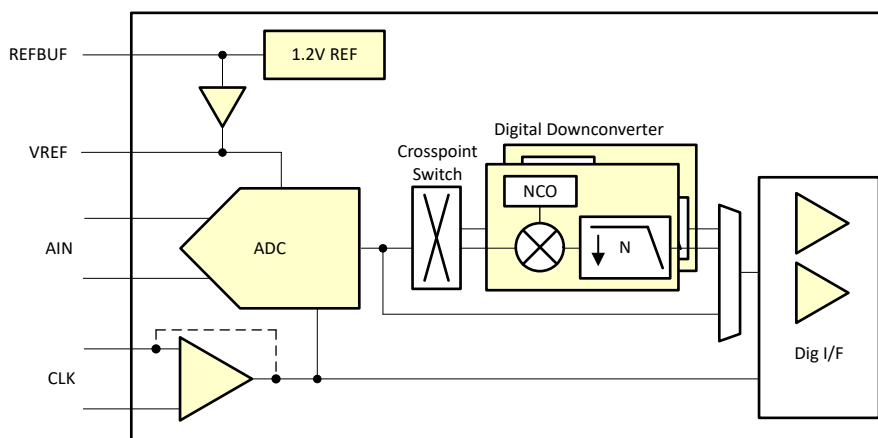


图 8-40. Power Down Configurations

表 8-9. Overview of Power Down Options

| Function/ Register | PDN via SPI | Mask for Global PDN | Feature - Default | Power Impact | Wake-up time | Comment |
|--------------------------|-------------|---------------------|--------------------|----------------------|--------------|--|
| ADC | Yes | - | Enabled | | | ADC is included in Global PDN automatically |
| Reference gain amplifier | Yes | Yes | Enabled | ~ 0.4 mA | ~3 us | Should only be powered down in power down state. |
| Internal 1.2V reference | Yes | | External ref | ~ 1-3.5 mA | ~3 ms | Internal/external reference selection is available through SPI and REFBUF pin. |
| Clock buffer | Yes | | Differential clock | ~ 1 mA | n/a | Single ended clock input saves ~ 1mA compared to differential. Some programmability is available through the REFBUF pin. |
| Output interface drivers | Yes | - | Enabled | varies | n/a | Depending on output interface mode, unused output drivers can be powered down for maximum power savings |
| Decimation filter | Yes | - | Disabled | see electrical table | n/a | |

8.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI) however it can operate in a default configuration without requiring the SPI interface. Furthermore the power down function as well as internal/external reference configuration is possible via pin control (PDN/SYNC and REFBUF pin).

注

The power down command (via PIN or SPI) only goes in effect with the ADC sampling clock present.

After initial power up, the default operating configuration is shown in 表 8-10.

表 8-10. Default device configuration after power up

| FEATURE | DEFAULT |
|---------------|---------------|
| Signal Input | Differential |
| Clock Input | Differential |
| Reference | External |
| Decimation | DDC bypass |
| Interface | 2-wire |
| Output Format | 2s complement |

8.5.1 Configuration using PINs only

The ADC voltage reference can be selected using the REFBUF pin. Even though there is an internal 100 kΩ pull-up resistor to AVDD, the REFBUF pin should be set to a voltage externally and not left floating.

When using a voltage divider to set the REFBUF voltage (R1 and R2 in 表 8-11), resistor values < 5 kΩ should be used.

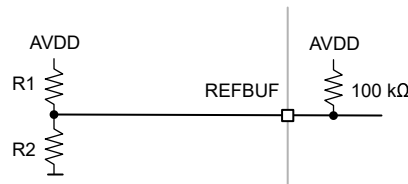


图 8-41. Configuration of external voltage on REFBUF pin

表 8-11. REFBUF voltage levels control voltage reference selection

| REFBUF VOLTAGE | VOLTAGE REFERENCE OPTION | CLOCKING OPTION |
|--------------------|--|--------------------------|
| > 1.7 V (Default) | External reference | Differential clock input |
| 1.2 V (1.15-1.25V) | External 1.2V input on REFBUF pin using internal gain buffer | Differential clock input |
| 0.5 - 0.7V | Internal reference | Differential clock input |
| < 0.1V | Internal reference | Single ended clock input |

8.5.2 Configuration using the SPI interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 12 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

8.5.2.1 Register Write

The internal registers can be programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 8-42 shows the timing requirements for the serial register write operation.

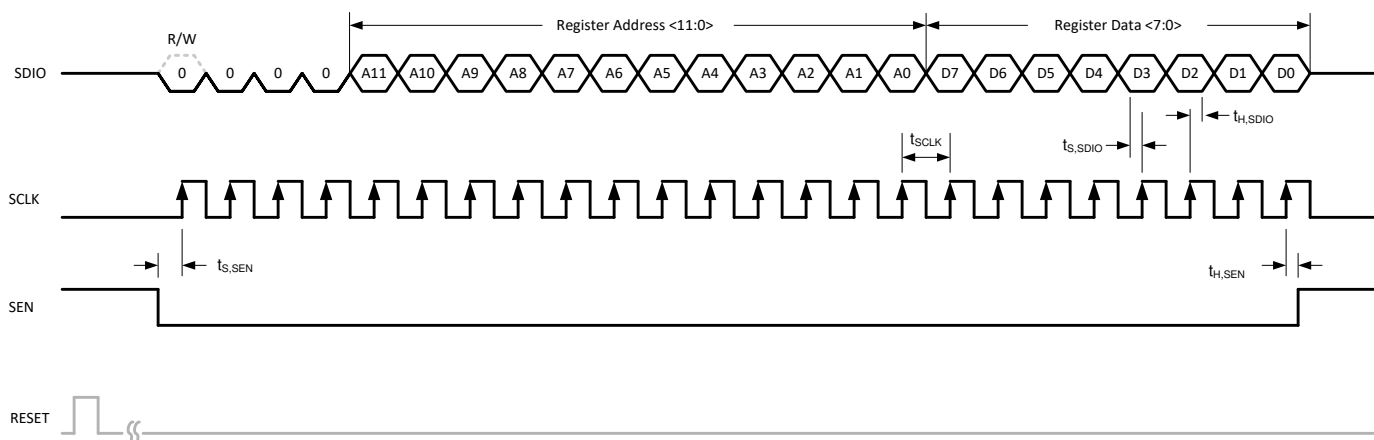


Figure 8-42. Serial Register Write Timing Diagram

8.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

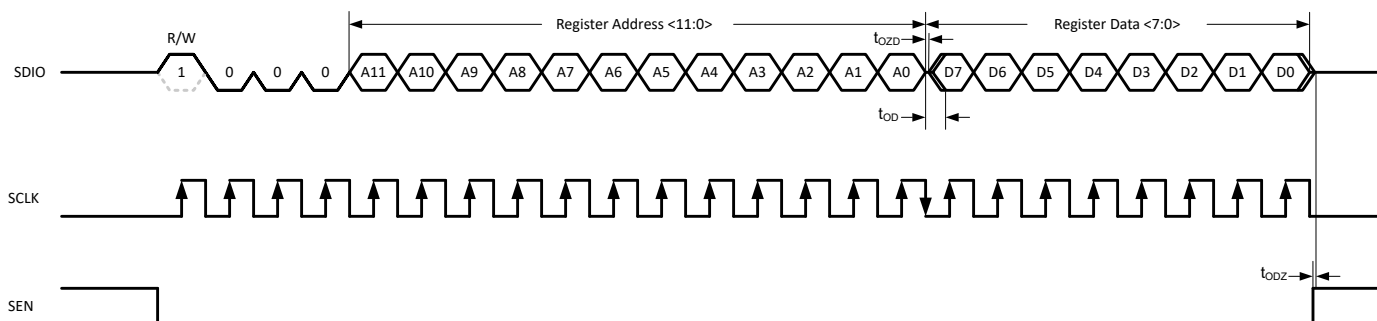


Figure 8-43. Serial Register Read Timing Diagram

8.6 Register Maps

表 8-12. Register Map Summary

| REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|------------------|-----------------------|------------|-----------------|-------------|------------------|----------------|--------------------|------------|
| A[11:0] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| 0x07 | OP IF MAPPER | | | 0 | OP IF EN | OP IF SEL | | |
| 0x08 | 0 | 0 | PDN CLKBUF | PDN REFAMP | 0 | PDN A | 1 | PDN GLOBAL |
| 0x09 | 0 | 0 | PDN FCLKOUT | PDN DCLKOUT | PDN DA1 | PDN DA0 | PDN DB1 | PDN DB0 |
| 0x0D | 0 | 0 | 0 | 0 | MASK CLKBUF | MASK REFAMP | MASK BG DIS | 0 |
| 0x0E | SYNC PIN EN | SPI SYNC | SPI SYNC EN | 0 | REF CTRL | REF SEL | | SE CLK EN |
| 0x11 | 0 | 0 | SE A | 0 | 0 | 0 | 0 | 0 |
| 0x13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | E-FUSE LD |
| 0x14 | CUSTOM PAT [7:0] | | | | | | | |
| 0x15 | CUSTOM PAT [15:8] | | | | | | | |
| 0x16 | TEST PAT B | | | TEST PAT A | | | CUSTOM PAT [17:16] | |
| 0x19 | FCLK SRC | 0 | 0 | FCLK DIV | 0 | 0 | 0 | TOG FCLK |
| 0x1A | 0 | 0 | LVDS SWING HIGH | | | LVDS SWING LOW | | |
| 0x1B | MAPPER EN | 20B EN | BIT MAPPER RES | | | 0 | 0 | 0 |
| 0x1E | 0 | 0 | 0 | 0 | LVDS DATA DEL | | LVDS DCLK DEL | |
| 0x20 | FCLK PAT [7:0] | | | | | | | |
| 0x21 | FCLK PAT [15:8] | | | | | | | |
| 0x22 | 0 | 0 | 0 | 0 | FCLK PAT [19:16] | | | |
| 0x24 | 0 | 0 | 0 | DDC MUX | | DIG BYP | DDC EN | 0 |
| 0x25 | DDC MUX EN | DECIMATION | | | REAL OUT | 0 | 0 | MIX PHASE |
| 0x26 | MIX GAIN A | | MIX RES A | FS/4 MIX A | MIX GAIN B | | MIX RES B | FS/4 MIX B |
| 0x27 | 0 | 0 | 0 | OP ORDER A | Q-DEL A | FS/4 MIX PH A | 0 | 0 |
| 0x2A | NCO A [7:0] | | | | | | | |
| 0x2B | NCO A [15:8] | | | | | | | |
| 0x2C | NCO A [23:16] | | | | | | | |
| 0x2D | NCO A [31:24] | | | | | | | |
| 0x2E | 0 | 0 | 0 | OP ORDER B | Q-DEL B | FS/4 MIX PH B | 0 | 0 |
| 0x31 | NCO B [7:0] | | | | | | | |
| 0x32 | NCO B [15:8] | | | | | | | |
| 0x33 | NCO B [23:16] | | | | | | | |
| 0x34 | NCO B [31:24] | | | | | | | |
| 0x39..0x60 | OUTPUT BIT MAPPER CHA | | | | | | | |
| 0x61..0x88 | OUTPUT BIT MAPPER CHB | | | | | | | |
| 0x8F | 0 | 0 | 0 | 0 | 0 | 0 | FORMAT A | 0 |
| 0x92 | 0 | 0 | 0 | 0 | 0 | 0 | FORMAT B | 0 |

8.6.1 Detailed Register Description

图 8-44. Register 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-13. Register 0x00 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 7-1 | 0 | R/W | 0 | Must write 0 |
| 0 | RESET | R/W | 0 | This bit resets all internal registers to the default values and self clears to 0. |

图 8-45. Register 0x07

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-------|-------|-------|----------|-----------|-------|-------|
| OP IF MAPPER | | | 0 | OP IF EN | OP IF SEL | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-14. Register 0x07 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-5 | OP IF MAPPER | R/W | 000 | Output interface mapper. This register contains the proper output interface bit mapping for the different interfaces. The interface bit mapping is internally loaded from e-fuses and also requires a fuse load command to go into effect (0x13, D0). Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. After initial reset the default output interface variant is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 001: 2-wire, 18 and 14-bit 010: 2-wire, 16-bit 011: 1-wire 100: 0.5-wire others: not used |
| 4 | 0 | R/W | 0 | Must write 0 |
| 3 | OP IF EN | R/W | 0 | Enables changing the default output interface mode (D2-D0). |
| 2-0 | OP IF SEL | R/W | 000 | Selection of the output interface mode. OP IF EN (D3) needs to be enabled also. After initial reset the default output interface is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 011: 2-wire 100: 1-wire 101: 0.5-wire others: not used |

✎ 8-46. Register 0x08

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|------------|------------|-------|-------|-------|------------|
| 0 | 0 | PDN CLKBUF | PDN REFAMP | 0 | 1 | PDN A | PDN GLOBAL |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-15. Register 0x08 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5 | PDN CLKBUF | R/W | 0 | Powers down sampling clock buffer 0: Clock buffer enabled 1: Clock buffer powered down |
| 4 | PDN REFAMP | R/W | 0 | Powers down internal reference gain amplifier 0: REFAMP enabled 1: REFAMP powered down |
| 3 | 0 | R/W | 0 | Must write 0 |
| 2 | PDN A | R/W | 0 | Powers down ADC channel A 0: ADC channel A enabled 1: ADC channel A powered down |
| 1 | 1 | R/W | 1 | Must write 1 |
| 0 | PDN GLOBAL | R/W | 0 | Global power down via SPI 0: Global power disabled 1: Global power down enabled. Power down mask (register 0x0D) determines which internal blocks are powered down. |

✎ 8-47. Register 0x09

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------------|-------------|---------|---------|----------|---------|
| 0 | 0 | PDN FCLKOUT | PDN DCLKOUT | PDN DA1 | PDN DA0 | PDN DBA1 | PDN DB0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-16. Register 0x09 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5 | PDN FCLKOUT | R/W | 0 | Powers down frame clock (FCLK) LVDS output buffer 0: FCLK output buffer enabled 1: FCLK output buffer powered down |
| 4 | PDN DCLKOUT | R/W | 0 | Powers down DCLK LVDS output buffer 0: DCLK output buffer enabled 1: DCLK output buffer powered down |
| 3 | PDN DA1 | R/W | 1 | Powers down LVDS output buffer for channel A, lane 1. Powered down automatically in 1-wire and 1/2-wire mode. 0: DA1 LVDS output buffer enabled 1: DA1 LVDS output buffer powered down |
| 2 | PDN DA0 | R/W | 1 | Powers down LVDS output buffer for channel A, lane 0. 0: DA0 LVDS output buffer enabled 1: DA0 LVDS output buffer powered down |
| 1 | PDN DB1 | R/W | 0 | Powers down LVDS output buffer for channel B, lane 1. Powered down automatically in 1-wire and 1/2-wire mode. Default is powered down. 0: DB1 LVDS output buffer enabled 1: DB1 LVDS output buffer powered down |
| 0 | PDN DB0 | R/W | 0 | Powers down LVDS output buffer for channel B, lane 0. Powered down automatically in 1/2-wire mode. Default is powered down. 0: DB0 LVDS output buffer enabled 1: DB0 LVDS output buffer powered down |

図 8-48. Register 0x0D (PDN GLOBAL MASK)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------------|-------------|-------------|-------|
| 0 | 0 | 0 | 0 | MASK CLKBUF | MASK REFAMP | MASK BG DIS | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-17. Register 0x0D Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7-4 | 0 | R/W | 0 | Must write 0 |
| 3 | MASK CLKBUF | R/W | 0 | Global power down mask control for sampling clock input buffer. 0: Clock buffer will get powered down when global power down is exercised. 1: Clock buffer will NOT get powered down when global power down is exercised. |
| 2 | MASK REFAMP | R/W | 0 | Global power down mask control for reference amplifier. 0: Reference amplifier will get powered down when global power down is exercised. 1: Reference amplifier will NOT get powered down when global power down is exercised. |
| 1 | MASK BG DIS | R/W | 0 | Global power down mask control for internal 1.2V bandgap voltage reference. Setting this bit reduces power consumption in global power down mode but increases the wake up time. See the power down option overview. 0: Internal 1.2V bandgap voltage reference will NOT get powered down when global power down is exercised. 1: Internal 1.2V bandgap voltage reference will get powered down when global power down is exercised. |
| 0 | 0 | R/W | 0 | Must write 0 |

图 8-49. Register 0x0E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------|-------------|-------|---------|---------|-------|-----------|
| SYNC PIN EN | SPI SYNC | SPI SYNC EN | 0 | REF CTL | REF SEL | | SE CLK EN |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-18. Register 0x0E Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | SYNC PIN EN | R/W | 0 | This bit controls the functionality of the SYNC/PDN pin. 0: SYNC/PDN pin exercises global power down mode when pin is pulled high. 1: SYNC/PDN pin issues the SYNC command when pin is pulled high. |
| 6 | SPI SYNC | R/W | 0 | Toggling this bit issues the SYNC command using the SPI register write. SYNC using SPI must be enabled as well (D5). This bit doesn't self reset to 0. 0: Normal operation 1: SYNC command issued. |
| 5 | SPI SYNC EN | R/W | 0 | This bit enables synchronization using SPI instead of the SYNC/PDN pin. 0: Synchronization using SPI register bit disabled. 1: Synchronization using SPI register bit enabled. |
| 4 | 0 | R/W | 0 | Must write 0 |
| 3 | REF CTL | R/W | 0 | This bit determines if the REFBUF pin controls the voltage reference selection or the SPI register (D2-D1). 0: The REFBUF pin selects the voltage reference option. 1: Voltage reference is selected using SPI (D2-D1) and single ended clock using D0. |
| 2-1 | REF SEL | R/W | 00 | Selects of the voltage reference option. REF CTRL (D3) must be set to 1. 00: Internal reference 01: External voltage reference (1.2V) using internal reference buffer (REFBUF) 10: External voltage reference 11: not used |
| 0 | SE CLK EN | R/W | 0 | Selects single ended clock input and powers down the differential sampling clock input buffer. REF CTRL (D3) must be set to 1. 0: Differential clock input 1: Single ended clock input |

图 8-50. Register 0x11

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | SE A | 0 | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-19. Register 0x11 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5 | SE A | R/W | 0 | This bit enables single ended analog input, channel A. This mode reduces the SNR by 3-dB. 0: Differential input 1: Single ended input |
| 4-0 | 0 | R/W | 0 | Must write 0 |

图 8-51. Register 0x13

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | | E-FUSE LD |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-20. Register 0x13 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-1 | 0 | R/W | 0 | Must write 0 |
| 0 | E-FUSE LD | R/W | 0 | This register bit loads the internal bit mapping for different interfaces. After setting the interface in register 0x07, this E-FUSE LD bit needs to be set to 1 and reset to 0 for loading to go into effect. Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. 0: E-FUSE LOAD set 1: E-FUSE LOAD reset |

图 8-52. Register 0x14/15/16

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|-------|-------|------------|-------|-------|--------------------|-------|
| CUSTOM PAT [7:0] | | | | | | | |
| CUSTOM PAT [15:8] | | | | | | | |
| TEST PAT B | | | TEST PAT A | | | CUSTOM PAT [17:16] | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-21. Register 0x14/15/16 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|----------|--|
| 7-0 | CUSTOM PAT [17:0] | R/W | 00000000 | This register is used for two purposes: <ul style="list-style-type: none"> It sets the constant custom pattern starting from MSB It sets the RAMP pattern increment step size. 00001: Ramp pattern for 18-bit ADC 00100: Ramp pattern for 16-bit ADC 10000: Ramp pattern for 14-bit ADC |
| 7-5 | TEST PAT B | R/W | 000 | Enables test pattern output mode for channel B (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format. 000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used |
| 4-2 | TEST PAT A | R/W | 000 | Enables test pattern output mode for channel A (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format. 000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used |

图 8-53. Register 0x19

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------|-------|----------|-------|-------|-------|----------|
| FCLK SRC | 0 | 0 | FCLK DIV | 0 | 0 | 0 | TOG FCLK |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-22. Register 0x19 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | FCLK SRC | R/W | 0 | User has to select if FCLK signal comes from ADC or from DDC block. Here real decimation is treated same as bypass mode 0: FCLK generated from ADC. FCLK SRC set to 0 for DDC bypass, real decimation mode and 1/2-w complex decimation mode. 1: FCLK generated from DDC block. In complex decimation mode only this bit needs to be set for 2-w and 1-w output interface mode but NOT for 1/2-w mode. |
| 6-5 | 0 | R/W | 0 | Must write 0 |
| 4 | FCLK DIV | R/W | 0 | This bit needs to be set to 1 for 2-w output mode in bypass/real decimation mode only . 0: All output interface modes except 2-w decimation bypass and real decimation mode. 1: 2-w output interface mode for decimation bypass and real decimation. |
| 3-1 | 0 | R/W | 0 | Must write 0 |
| 0 | TOG FCLK | R/W | 0 | This bit adjusts the FCLK signal appropriately for 1/2-wire mode where FCLK is stretched to cover channel A and channel B. This bit ONLY needs to be set in 1/2-wire mode with complex decimation mode. 0: all other modes. 1: FCLK for 1/2-wire complex decimation mode. |

表 8-23. Configuration of FCLK SRC and FCLK DIV Register Bits vs Serial Interface

| BYPASS/DECIMATION | SERIAL INTERFACE | FCLK SRC | FCLK DIV | TOG FCLK |
|------------------------------------|------------------|----------|----------|----------|
| Decimation Bypass/ Real Decimation | 2-wire | 0 | 1 | 0 |
| | 1-wire | 0 | 0 | 0 |
| | 1/2-wire | 0 | 0 | 0 |
| Complex Decimation | 2-wire | 1 | 0 | 0 |
| | 1-wire | 1 | 0 | 0 |
| | 1/2-wire | 0 | 0 | 1 |

图 8-54. Register 0x1A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-----------------|-------|-------|----------------|-------|-------|
| 0 | 0 | LVDS SWING HIGH | | | LVDS SWING LOW | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-24. Register 0x1A Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5-3 | LVDS SWING HIGH | R/W | 000 | These bits adjust the SLVDS interface output high side amplitude in 25mV steps. By using SLVDS SWING HIGH/LOW the differential amplitude and common mode can be adjusted. 000: 1250 mV 001: 1275 mV 010: 1300 mV 011: 1325 mV 100: 1350 mV 101: 1325 mV 110: 1350 mV 111: 1375 mV |
| 2-0 | LVDS SWING LOW | R/W | 000 | These bits adjust the SLVDS interface output low side amplitude in 25mV steps. By using SLVDS SWING HIGH/LOW the differential amplitude and common mode can be adjusted. 000: 575 mV 001: 600 mV 010: 625 mV 011: 650 mV 100: 675 mV 101: 700 mV 110: 725 mV 111: 750 mV |

图 8-55. Register 0x1B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|--------|----------------|-------|-------|-------|-------|-------|
| MAPPER EN | 20B EN | BIT MAPPER RES | | | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-25. Register 0x1B Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | MAPPER EN | R/W | 0 | This bit enables changing the resolution of the output (including output serialization factor) in bypass mode only. This bit is not needed for 20-bit resolution output. 0: Output bit mapper disabled. 1: Output bit mapper enabled. |
| 6 | 20B EN | R/W | 0 | This bit enables 20-bit output resolution which can be useful for very high decimation settings so that quantization noise doesn't impact the ADC performance. 0: 20-bit output resolution disabled. 1: 20-bit output resolution enabled. |
| 5-3 | BIT MAPPER RES | R/W | 000 | Sets the output resolution using the bit mapper. MAPPER EN bit (D6) needs to be enabled when operating in bypass mode.. 000: 18 bit 001: 16 bit 010: 14 bit all others, n/a |
| 2-0 | 0 | R/W | 0 | Must write 0 |

表 8-26. Register Settings for Output Bit Mapper vs Operating Mode

| BYPASS/ DECIMATION | OUTPUT RESOLUTION | MAPPER EN (D7) | BIT MAPPER RES (D5-D3) |
|-----------------------|------------------------------------|----------------|---|
| Decimation Bypass | Resolution Change | 1 | 000: 18-bit 001: 16-bit 010: 14-bit |
| Real Decimation | Resolution Change (default 18-bit) | 0 | |
| Complex Decimation | | 0 | |

图 8-56. Register 0x1E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|---------------|-------|---------------|-------|
| 0 | 0 | 0 | 0 | LVDS DATA DEL | | LVDS DCLK DEL | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-27. Register 0x1E Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7-4 | 0 | R/W | 0 | Must write 0 |
| 3-2 | LVDS DATA DEL | R/W | 00 | These bits adjust the output timing of the SLVDS output data. 00: no delay 01: Data advanced by 50 ps 10: Data delayed by 50 ps 11: Data delayed by 100 ps |
| 1-0 | LVDS DCLK DEL | R/W | 00 | These bits adjust the output timing of the SLVDS DCLK output. 00: no delay 01: DCLK advanced by 50 ps 10: DCLK delayed by 50 ps 11: DCLK delayed by 100 ps |

图 8-57. Register 0x20/21/22

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------|-------|-------|------------------|-------|-------|-------|
| FCLK PAT [7:0] | | | | | | | |
| FCLK PAT [15:8] | | | | | | | |
| 0 | 0 | 0 | 0 | FCLK PAT [19:16] | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-28. Register 0x20/21/22 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|---------|--|
| 7-0 | FCLK PAT [19:0] | R/W | 0xFFC00 | These bits can adjust the duty cycle of the FCLK. In decimation bypass mode the FCLK pattern gets adjusted automatically for the different output resolutions. 表 8-29 shows the proper FCLK pattern values for 1-wire and 1/2-wire in real/complex decimation. |

表 8-29. FCLK Pattern for different resolution based on interface

| DECIMATION | OUTPUT RESOLUTION | 2-WIRE | 1-WIRE | 1/2-WIRE |
|--------------------|-------------------|-------------|---------|-------------|
| REAL DECIMATION | 14-bit | Use Default | 0xFE000 | Use Default |
| | 16-bit | | 0xFF000 | |
| | 18-bit | | 0xFF800 | |
| | 20-bit | | 0xFFC00 | |
| COMPLEX DECIMATION | 14-bit | | 0xFFFFF | 0xFFFFF |
| | 16-bit | | | |
| | 18-bit | | | |
| | 20-bit | | | |

图 8-58. Register 0x24

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|---------|-------|---------|--------|-------|
| 0 | 0 | 0 | DDC MUX | | DIG BYP | DDC EN | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-30. Register 0x24 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7-5 | 0 | R/W | 0 | Must write 0 |
| 4-3 | DDC MUX | R/W | 0 | Configures DDC MUX in front of the decimation filter. 00: ADC channel A connected to DDC A; 01: ADC channel A connected to DDC A and DDC B. others: not used |
| 2 | DIG BYP | R/W | 0 | This bit needs to be set to enable digital features block which includes decimation and scrambling. 0: Digital feature block bypassed - lowest latency 1: Data path includes digital features |
| 1 | DDC EN | R/W | 0 | Enables internal decimation filter for both channels 0: DDC disabled. 1: DDC enabled. |
| 0 | 0 | R/W | 0 | Must write 0 |

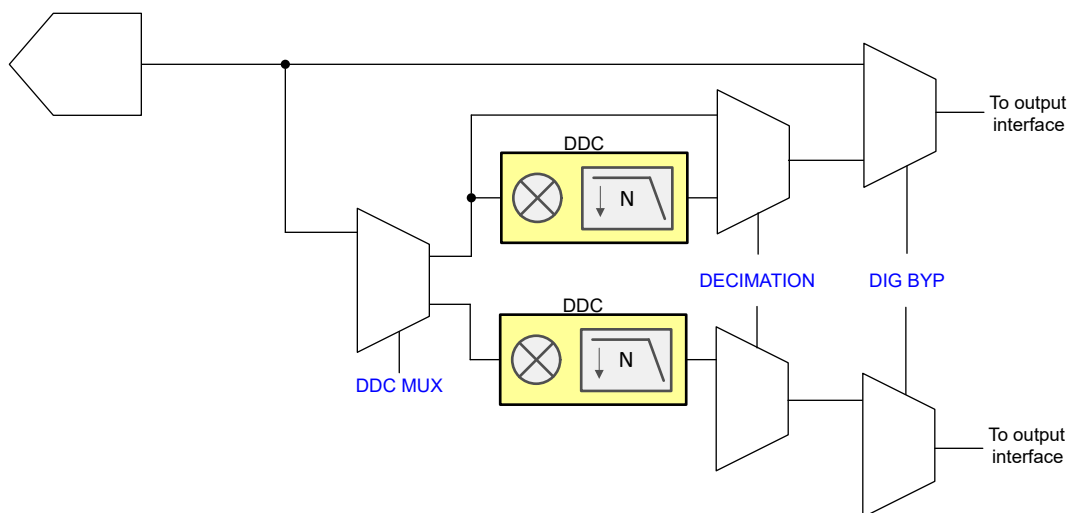


图 8-59. Register control for digital features

 **8-60. Register 0x25**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|-------|-------|----------|-------|-------|-----------|
| DDC MUX EN | DECIMATION | | | REAL OUT | 0 | 0 | MIX PHASE |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-31. Register 0x25 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7 | DDC MUX EN | R/W | 0 | Enables the digital mux between ADCs and decimation filters. This bit is required for DDC mux settings in register 0x024 (D4, D3) to go into effect. 0: DDC mux disabled 1: DDC mux enabled |
| 6-4 | DECIMATION | R/W | 000 | Complex decimation setting. This applies to both channels. 000: Bypass mode (no decimation) 001: Decimation by 2 010: Decimation by 4 011: Decimation by 8 100: Decimation by 16 101: Decimation by 32 others: not used |
| 3 | REAL OUT | R/W | 0 | This bit selects real output decimation. This mode applies to both channels. In this mode, the decimation filter is a low pass filter and no complex mixing is performed to reduce power consumption. For maximum power savings the NCO in this case should be set to 0. 0: Complex decimation 1: Real decimation |
| 2-1 | 0 | R/W | 0 | Must write 0 |
| 0 | MIX PHASE | R/W | 0 | This bit used to invert the NCO phase 0: NCO phase as is. 1: NCO phase inverted. |

 **8-61. Register 0x26**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-------|-----------|------------|------------|-------|-----------|------------|
| MIX GAIN A | | MIX RES A | FS/4 MIX A | MIX GAIN B | | MIX RES B | FS/4 MIX B |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-32. Register 0x26 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7-6 | MIX GAIN A | R/W | 00 | This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel A. 00: no digital gain added 01: 3-dB digital gain added 10: 6-dB digital gain added 11: not used |
| 5 | MIX RES A | R/W | 0 | Toggling this bit resets the NCO phase of channel A and loads the new NCO frequency. This bit does not self reset. |
| 4 | FS/4 MIX A | R/W | 0 | Enables FS/4 mixing for DDC A (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled. |
| 3-2 | MIX GAIN B | R/W | 00 | This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel B. 00: no digital gain added 01: 3-dB digital gain added 10: 6-dB digital gain added 11: not used |
| 1 | MIX RES B | R/W | 0 | Toggling this bit resets the NCO phase of channel B and loads the new NCO frequency. This bit does not self reset. |

表 8-32. Register 0x26 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 0 | FS/4 MIX B | R/W | 0 | Enables FS/4 mixing for DDC B (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled. |

図 8-62. Register 0x27

| | | | | | | | |
|-------|-------|-------|------------|---------|---------------|-------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | OP ORDER A | Q-DEL A | FS/4 MIX PH A | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-33. Register 0x27 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-5 | 0 | R/W | 0 | Must write 0 |
| 4 | OP ORDER A | R/W | 0 | Swaps the I and Q output order for channel A 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n] |
| 3 | Q-DEL A | R/W | 0 | This delays the Q-sample output of channel A by one. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2] |
| 2 | FS/4 MIX PH A | R/W | 0 | Inverts the mixer phase for channel A when using FS/4 mixer 0: Mixer phase is non-inverted 1: Mixer phase is inverted |
| 1-0 | 0 | R/W | 0 | Must write 0 |

図 8-63. Register 0x2A/B/C/D

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO A [7:0] | | | | | | | |
| NCO A [15:8] | | | | | | | |
| NCO A [23:16] | | | | | | | |
| NCO A [31:24] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-34. Register 0x2A/2B/2C/2D Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | NCO A [31:0] | R/W | 0 | Sets the 32 bit NCO value for decimation filter channel A. The NCO value is $f_{NCO} \times 2^{32}/FS$ In real decimation mode these registers are automatically set to 0. |

図 8-64. Register 0x2E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|------------|---------|---------------|-------|-------|
| 0 | 0 | 0 | OP ORDER B | Q-DEL B | FS/4 MIX PH B | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-35. Register 0x2E/2F/30 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-5 | 0 | R/W | 0 | Must write 0 |
| 4 | OP ORDER B | R/W | 0 | Swaps the I and Q output order for channel B 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n] |
| 3 | Q-DEL B | R/W | 0 | This delays the Q-sample output of channel B by one. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2] |
| 2 | FS/4 MIX PH B | R/W | 0 | Inverts the mixer phase for channel B when using FS/4 mixer 0: Mixer phase is non-inverted 1: Mixer phase is inverted |
| 1-0 | 0 | R/W | 0 | Must write 0 |

図 8-65. Register 0x31/32/33/34

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| NCO B [7:0] | | | | | | | |
| NCO B [15:8] | | | | | | | |
| NCO B [23:16] | | | | | | | |
| NCO B [31:24] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-36. Register 0x31/32/33/34 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | NCO B [31:0] | R/W | 0 | Sets the 32 bit NCO value for decimation filter channel B. The NCO value is $f_{NCO} \times 2^{32}/FS$ In real decimation mode these registers are automatically set to 0. |

図 8-66. Register 0x39..0x60

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| OUTPUT BIT MAPPER CHA | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-37. Register 0x39..0x60 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7-0 | OUTPUT BIT MAPPER CHA | R/W | 0 | These registers are used to reorder the output data bus. See the セクション 8.3.5.2 on how to program it. |

図 8-67. Register 0x61..0x88

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| OUTPUT BIT MAPPER CHB | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-38. Register 0x61..0x88 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 7-0 | OUTPUT BIT MAPPER CHB | R/W | 0 | These registers are used to reorder the output data bus. See the セクション 8.3.5.2 on how to program it. |

図 8-68. Register 0x8F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|----------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | FORMAT A | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-39. Register 0x8F Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-2 | 0 | R/W | 0 | Must write 0 |
| 1 | FORMAT A | R/W | 0 | This bit sets the output data format for channel A. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary |
| 0 | 0 | R/W | 0 | Must write 0 |

図 8-69. Register 0x92

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|----------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | FORMAT B | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

表 8-40. Register 0x92 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-2 | 0 | R/W | 0 | Must write 0 |
| 1 | FORMAT B | R/W | 0 | This bit sets the output data format for channel B. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary |
| 0 | 0 | R/W | 0 | Must write 0 |

9 Application Information Disclaimer

注

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9.1 Typical Application

A spectrum analyzer is a typical frequency domain application for the ADC3564 and its front end circuitry is very similar to several other systems such as software defined radio (SDR), radar or communications. Some applications require frequency coverage including DC or near DC so it's included in this example.

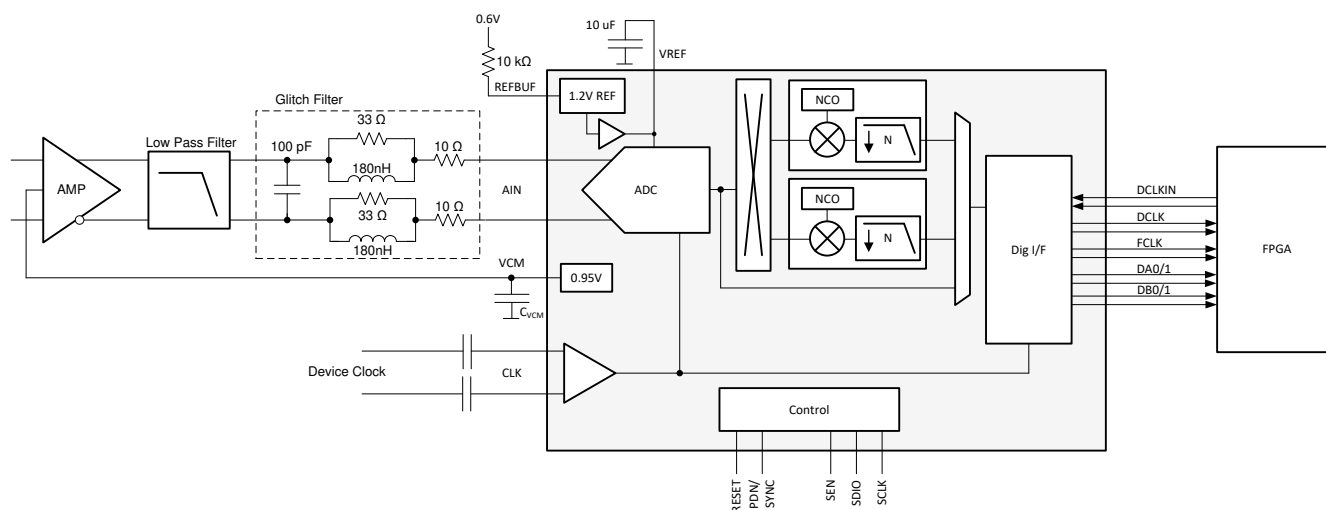


図 9-1. Typical configuration for a spectrum analyzer with DC support

9.1.1 Design Requirements

Frequency domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone to undersampling in higher Nyquist zones. If very low input frequency is supported then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA). If low frequency support is not needed then AC coupling and use of a balun may be more suitable.

The internal reference is used since DC precision is not needed. However the ADC AC performance is highly dependent on the quality of the external clock source. If in-band interferers can be present then the ADC SFDR performance will be a key care about as well. A higher ADC sampling rate is desirable in order to relax the external anti-aliasing filter – an internal decimation filter can be used to reduce the digital output rate afterwards.

表 9-1. Design key care-about

| FEATURE | DESCRIPTION |
|------------------|--|
| Signal Bandwidth | DC to 30 MHz |
| Input Driver | Single ended to differential signal conversion and DC coupling |
| Clock Source | External clock with low jitter |

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3564 input full-scale is 3.2Vpp. When factoring in ~ 1 dB for insertion loss of the filter, then the amplifier needs to deliver close to 3.6Vpp. The amplifier distortion performance will degrade with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The ADC3564 provides an output common mode voltage of 0.95V and the THS4541 for

example can only swing within 250 mV of its negative supply. A unipolar 3.3 V amplifier power supply will thus limit the maximum voltage swing to ~ 2.8Vpp. Hence if a larger output swing is required (factoring in filter insertion loss) then a negative supply for the amplifier is needed in order to eliminate that limitation. Additionally input voltage protection diodes may be needed to protect the ADC from over-voltage events.

表 9-2. Output voltage swing of THS4541 vs power supply

| DEVICE | MIN OUTPUT VOLTAGE | MAX SWING WITH 3.3 V/ 0 V SUPPLY | MAX SWING WITH 3.3 V/ -1.0 V SUPPLY |
|---------|--------------------|----------------------------------|-------------------------------------|
| THS4541 | VS- + 250 mV | 2.8 Vpp | 6.8 Vpp |

9.1.2 Detailed Design Procedure

9.1.2.1 Input Signal Path

The THS4541 provides a very good low power option to drive the ADC inputs. [表 9-3](#)

provides an overview of the THS4541 with power consumption and usable frequency.

表 9-3. Fully Differential Amplifier Options

| DEVICE | CURRENT (IQ) PER CHANNEL | USABLE FREQUENCY RANGE |
|---------|--------------------------|------------------------|
| THS4541 | 10 mA | < 70 MHz |

The low pass filter design (topology, filter order) is driven by the application itself. However, when designing the low pass filter, the optimum load impedance for the amplifier should be taken into consideration as well. Between the low pass filter and the ADC input the sampling glitch filter needs to added as well as shown in [セクション 8.3.1.2.1](#). In this example the DC - 30 MHz glitch filter is selected.

9.1.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 30 MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (i.e. square wave vs sine wave). [表 9-4](#) provides an overview of the estimated SNR performance of the ADC3564 based on different amounts of jitter of the external clock source. The SNR is estimated based on ADC3564 thermal noise of 77 dBFS and input signal at -1dBFS.

表 9-4. ADC SNR performance across vs input frequency for different amounts of external clock jitter

| INPUT FREQUENCY | T _{J,EXT} = 100 fs | T _{J,EXT} = 250 fs | T _{J,EXT} = 500 fs | T _{J,EXT} = 1 ps |
|-----------------|-----------------------------|-----------------------------|-----------------------------|---------------------------|
| 10 MHz | 76.5 | 76.4 | 76.3 | 75.9 |
| 20 MHz | 76.3 | 76.2 | 75.8 | 74.5 |
| 30 MHz | 76.2 | 75.9 | 75.1 | 72.8 |

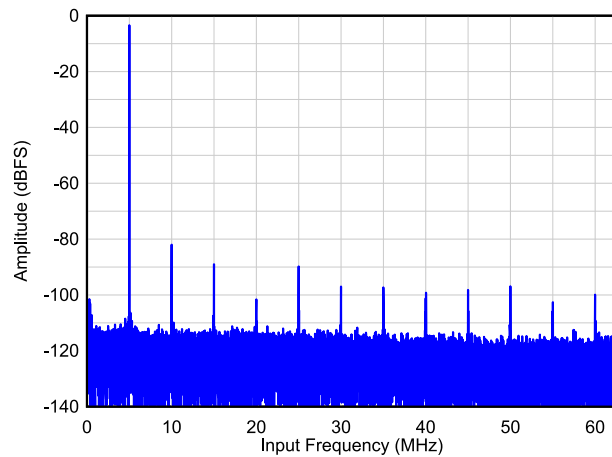
Termination of the clock input should be considered for long clock traces.

9.1.2.3 Voltage Reference

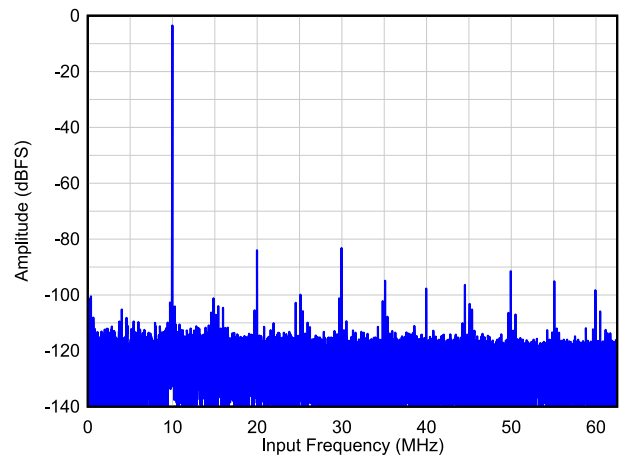
The ADC3564 is configured to internal reference operation by applying 0.6 V to the REFBUF pin.

9.1.3 Application Curves

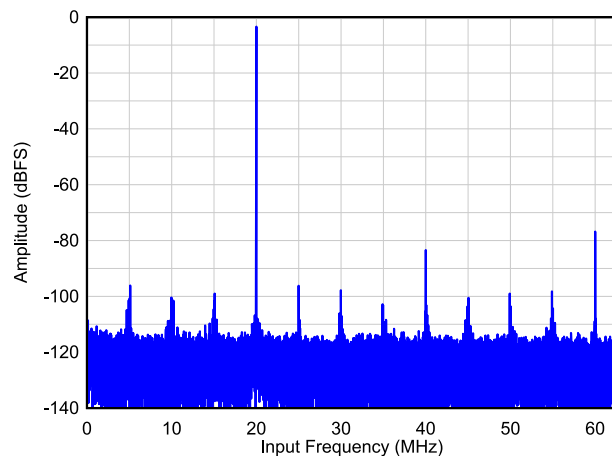
The following FFT plots show the performance of THS4541 driving the ADC3564 operated at 125 MSPS with a full-scale input at -1 dBFS with input frequencies at 5, 10 and 20 MHz.



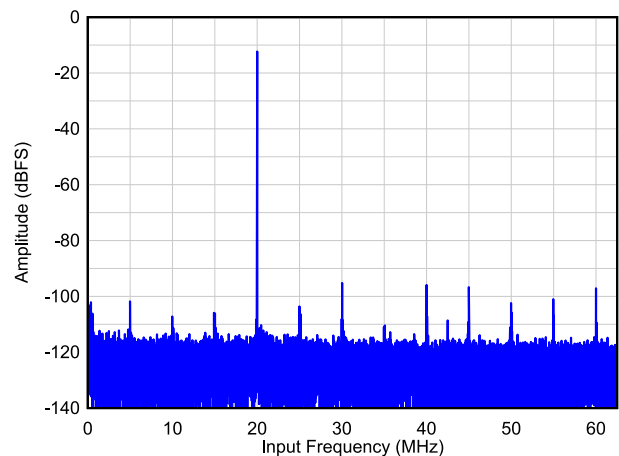
📐 9-2. Single Tone FFT at $F_{IN} = 5$ MHz



📐 9-3. Single Tone FFT at $F_{IN} = 10$ MHz



📐 9-4. Single Tone FFT at $F_{IN} = 20$ MHz

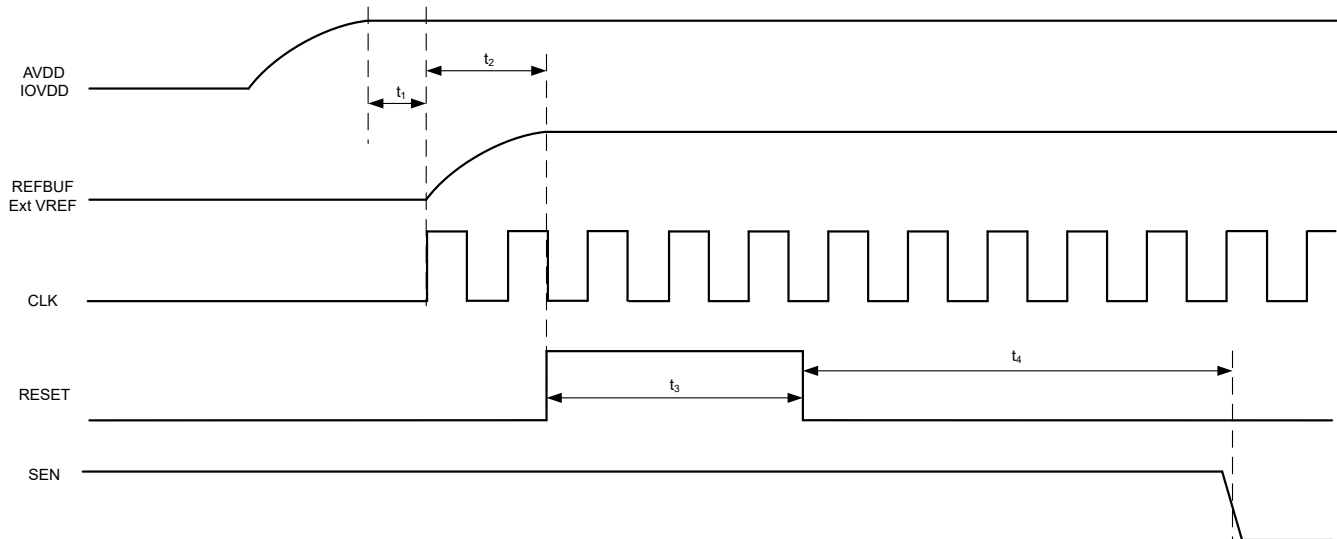


📐 9-5. Single Tone FFT at $F_{IN} = 20$ MHz

9.2 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in 9-6.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal bandgap reference will power up and settle out in ~ 2ms.
2. Configure REFBUF pin (pull high or low even if configured via SPI later on) and apply the sampling clock.
3. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up capacitor calibration is initiated. The calibration takes approximately 200000 clock cycles.
4. Begin programming using SPI interface.



9-6. Initialization of serial registers after power up

表 9-5. Power-up timing

| | | MIN | TYP | MAX | UNIT |
|-------|--|----------|-----|-----|--------------|
| t_1 | Power-on delay: delay from power up to logic level of REFBUF pin | 2 | | | ms |
| t_2 | Delay from REFBUF pin logic level to RESET rising edge | 100 | | | ns |
| t_3 | RESET pulse width | 1 | | | us |
| t_4 | Delay from RESET disable to SEN active | ~ 200000 | | | clock cycles |

9.2.1 Register Initialization During Operation

If required, the serial interface registers can be cleared and reset to default settings during operation either:

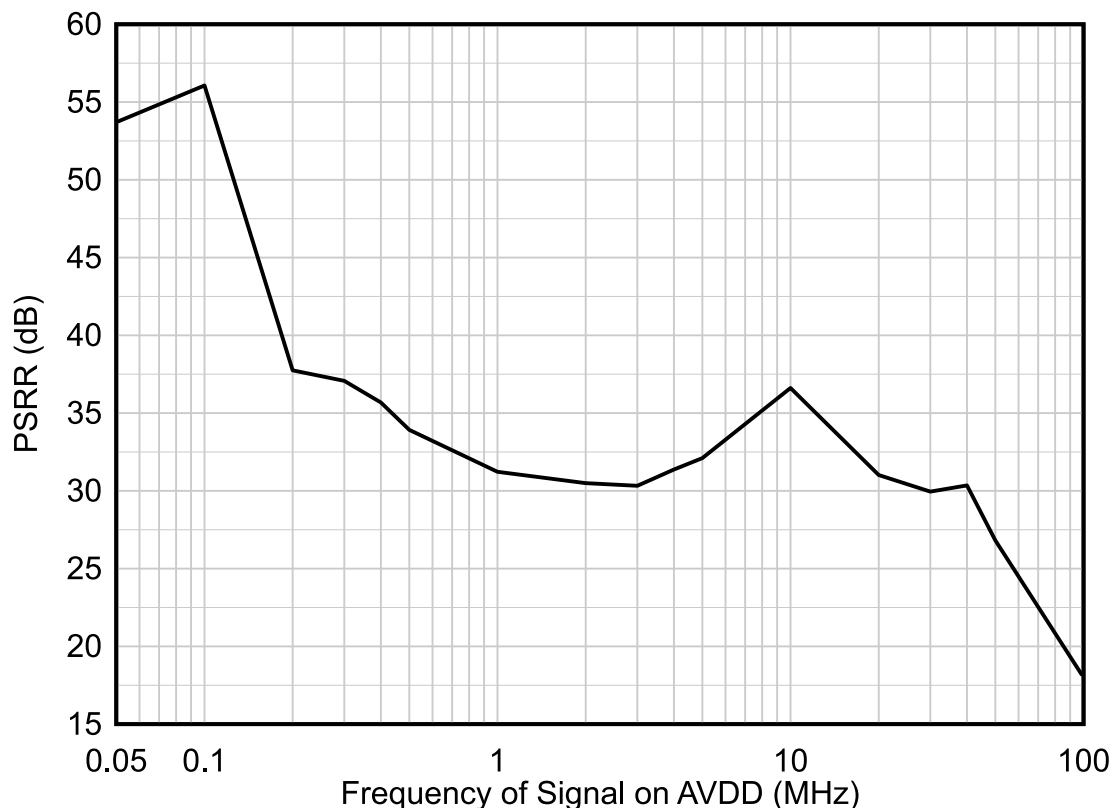
- through a hardware reset or
- by applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 0x00) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

After hardware or software reset the wait time is also ~ 200000 clock cycles before the SPI registers can be programmed.

9.3 Power Supply Recommendations

The ADC3564 requires two different power-supplies. The AVDD rail provides power for the internal analog circuits and the ADC itself while the IOVDD rail powers the digital interface and the internal digital circuits like decimation filter or output interface mapper. Power sequencing is not required.

The AVDD power supply must be low noise to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply must also be considered. The ADC is designed for good PSRR which aides with the power supply filter design.



✎ 9-7. Power Supply Rejection Ratio (PSRR) vs Frequency

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to make sure the switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. ✎ 9-8 and ✎ 9-9 illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared in order to prevent digital switching noise from coupling into the analog signal chain.

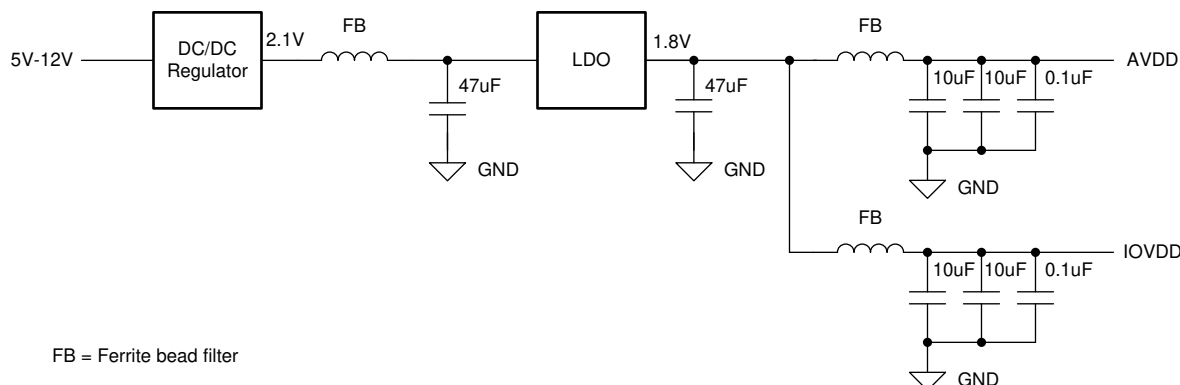


Figure 9-8. Example: LDO Linear Regulator Approach

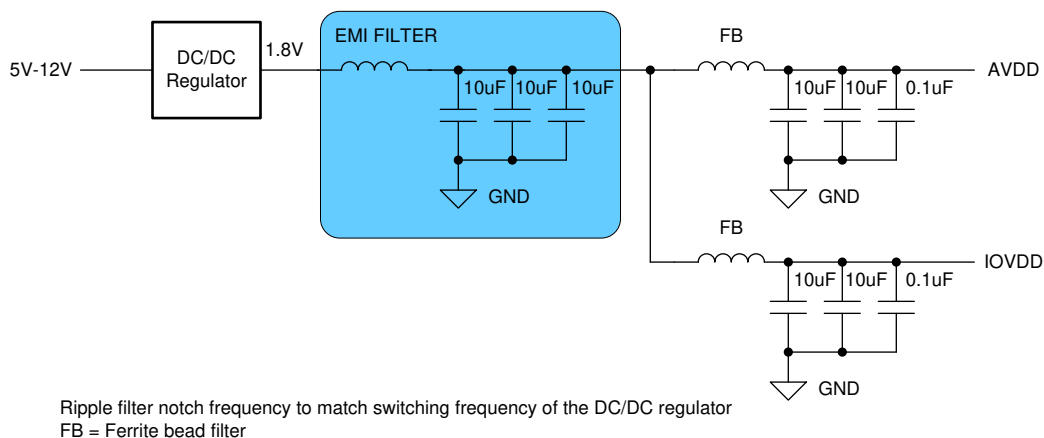


Figure 9-9. Example Switcher-Only Approach

9.4 Layout

9.4.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
 - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
 - Traces should be routed using loosely coupled 100-Ω differential traces.
 - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital output interface
 - Traces should be routed using tightly coupled 100-Ω differential traces.
3. Voltage reference
 - The bypass capacitor should be placed as close to the device pins as possible and connected between VREF and REFGND – on top layer avoiding vias.
 - Depending on configuration an additional bypass capacitor between REFBUF and REFGND may be recommended and should also be placed as close to pins as possible on top layer.
4. Power and ground connections
 - Provide low resistance connection paths to all power and ground pins.
 - Use power and ground planes instead of traces.
 - Avoid narrow, isolated paths which increase the connection resistance.

- Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

9.4.2 Layout Example

The following screen shot shows the top layer of the ADC3564/3664 EVM.

- Signal and clock inputs are routed as differential signals on the top layer avoiding vias.
- SLVDS output interface lanes are routed differential and length matched
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

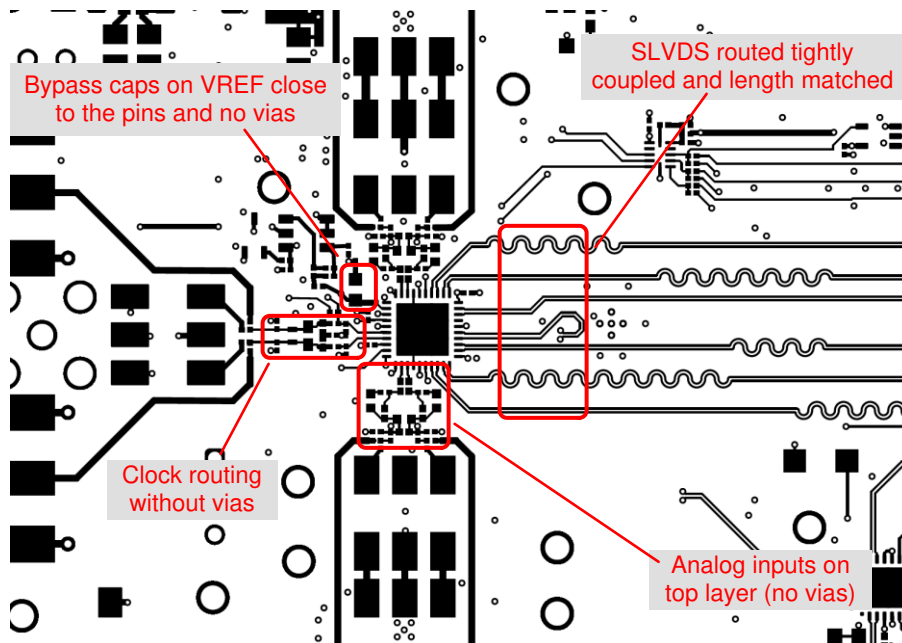


图 9-10. Layout example: top layer of ADC3564 EVM

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Support

10.2 Documentation Support

10.2.1 Related Documentation

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 サポート・リソース

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10.5 商標

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADC3564IRSB | Active | Production | WQFN (RSB) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | AZ3564 |
| ADC3564IRSB.R.A | Active | Production | WQFN (RSB) 40 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | AZ3564 |
| ADC3564IRSB | Active | Production | WQFN (RSB) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | AZ3564 |
| ADC3564IRSB.T.A | Active | Production | WQFN (RSB) 40 | 250 SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | AZ3564 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

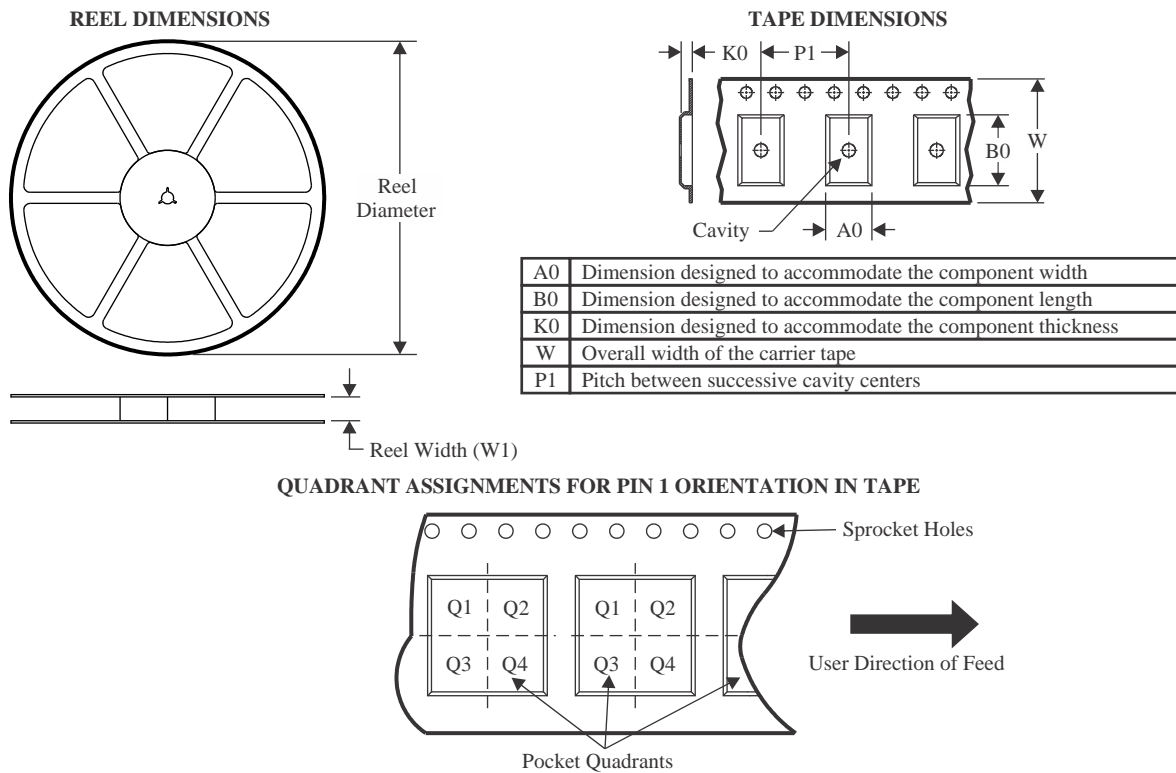
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

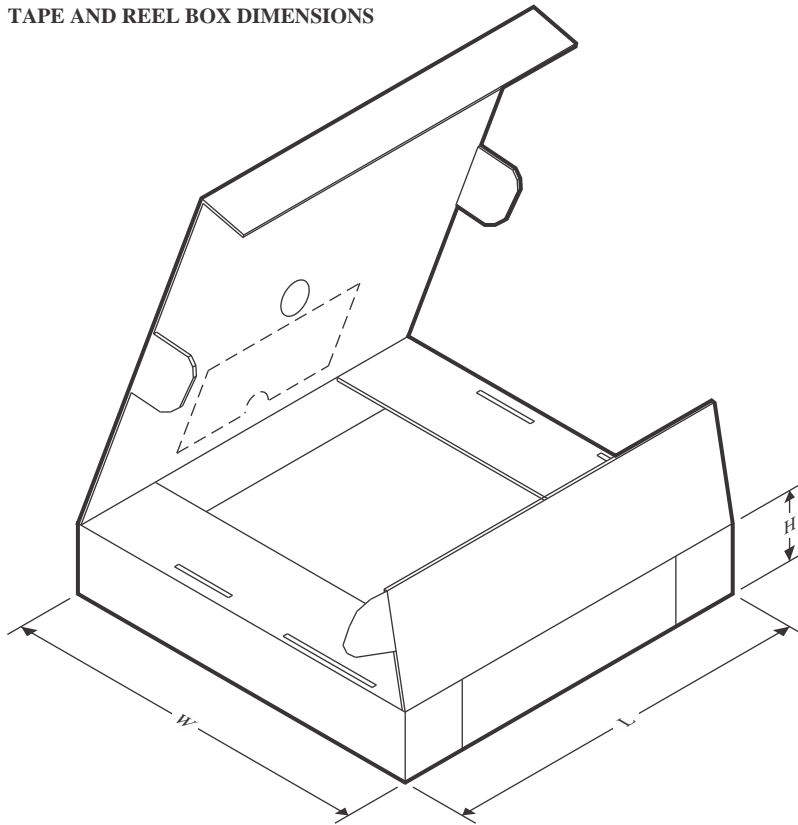
TAPE AND REEL INFORMATION



*All dimensions are nominal

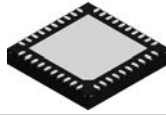
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADC3564IRSBR | WQFN | RSB | 40 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| ADC3564IRSBT | WQFN | RSB | 40 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

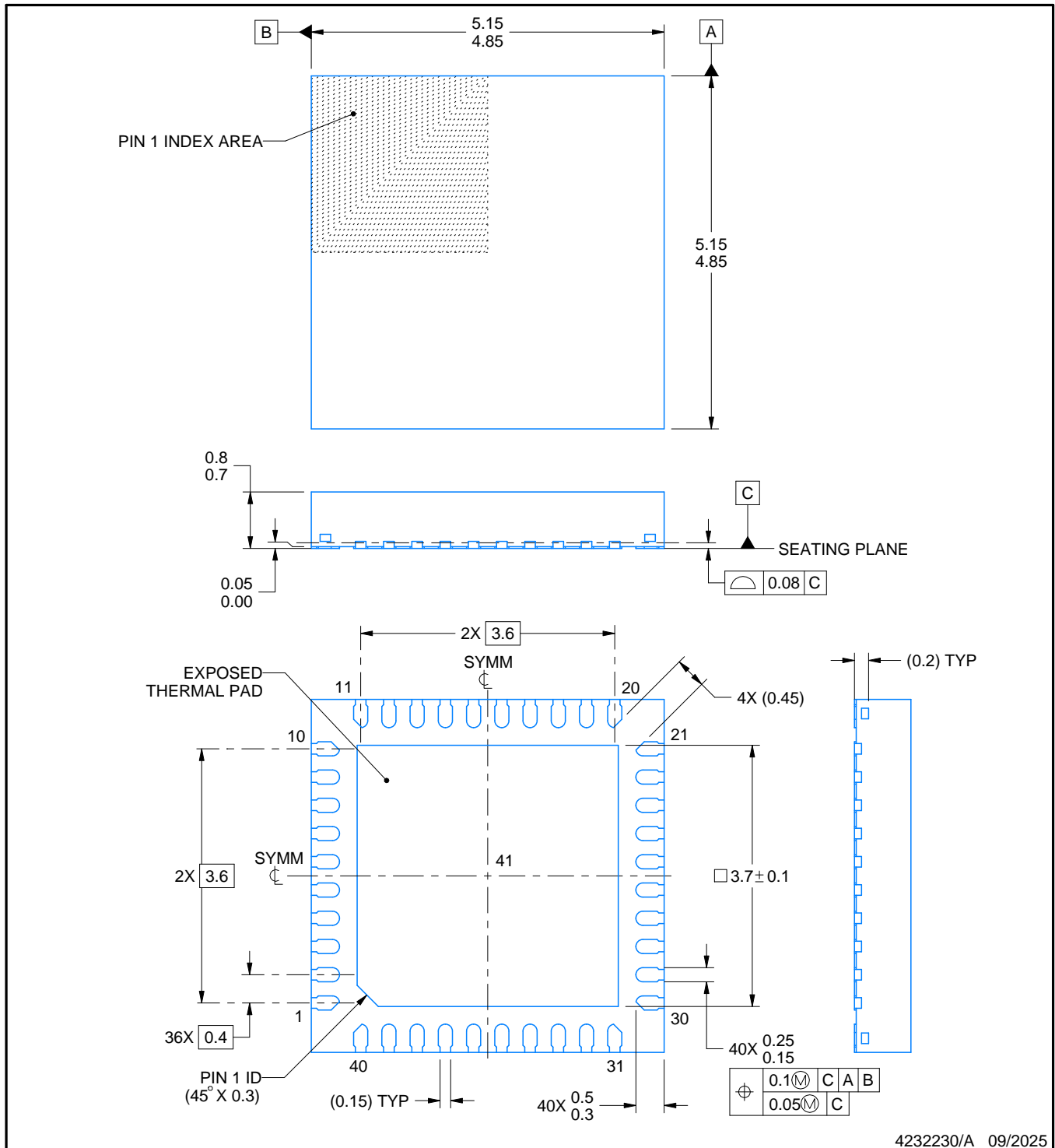


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADC3564IRSBR | WQFN | RSB | 40 | 3000 | 350.0 | 350.0 | 43.0 |
| ADC3564IRSBT | WQFN | RSB | 40 | 250 | 210.0 | 185.0 | 35.0 |

RSB0040F**PACKAGE OUTLINE****WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4232230/A 09/2025

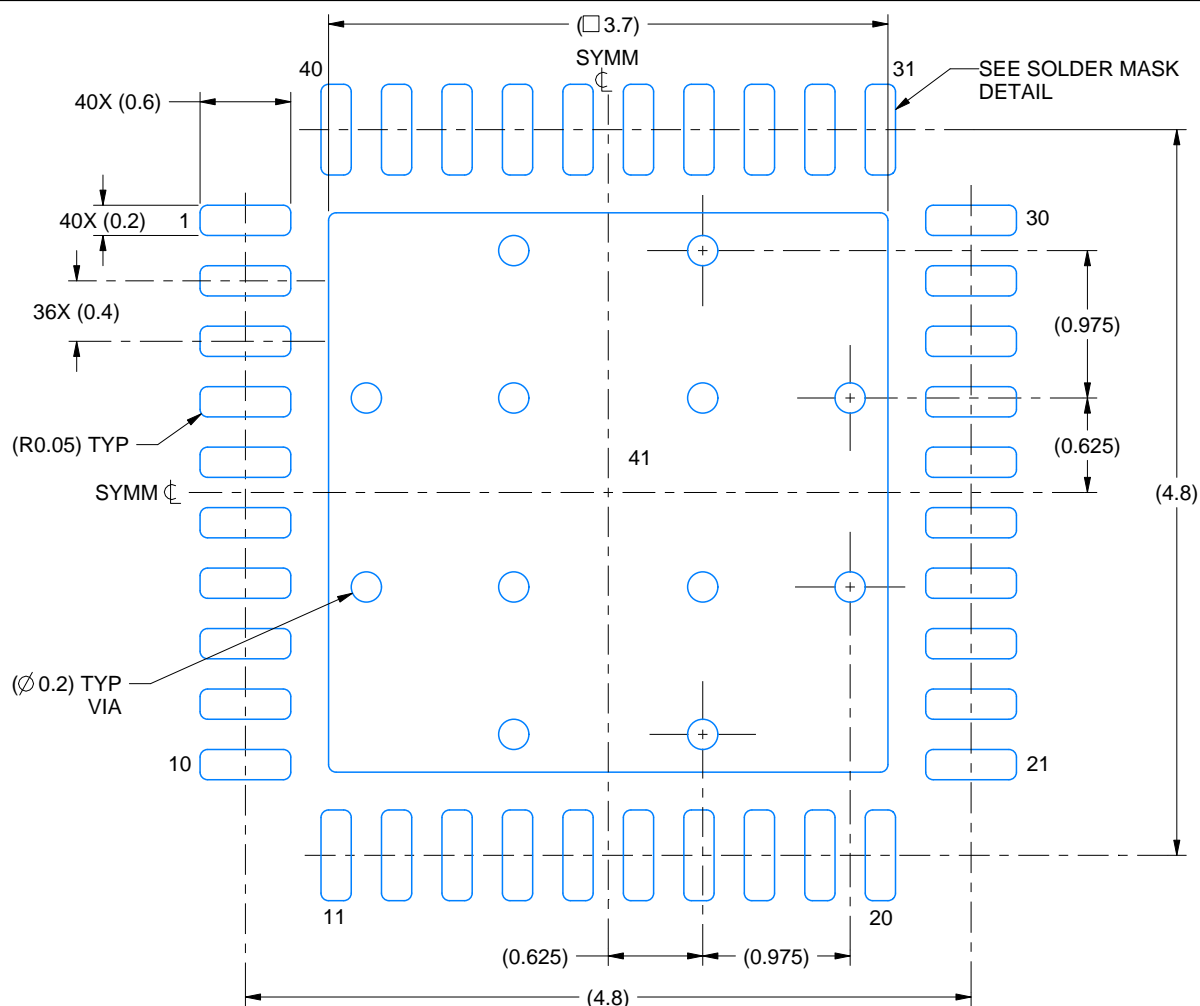
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

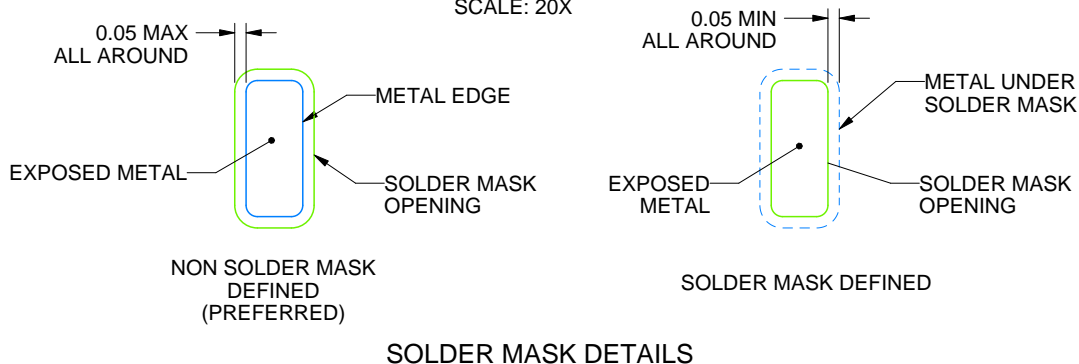
RSB0040F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4232230/A 09/2025

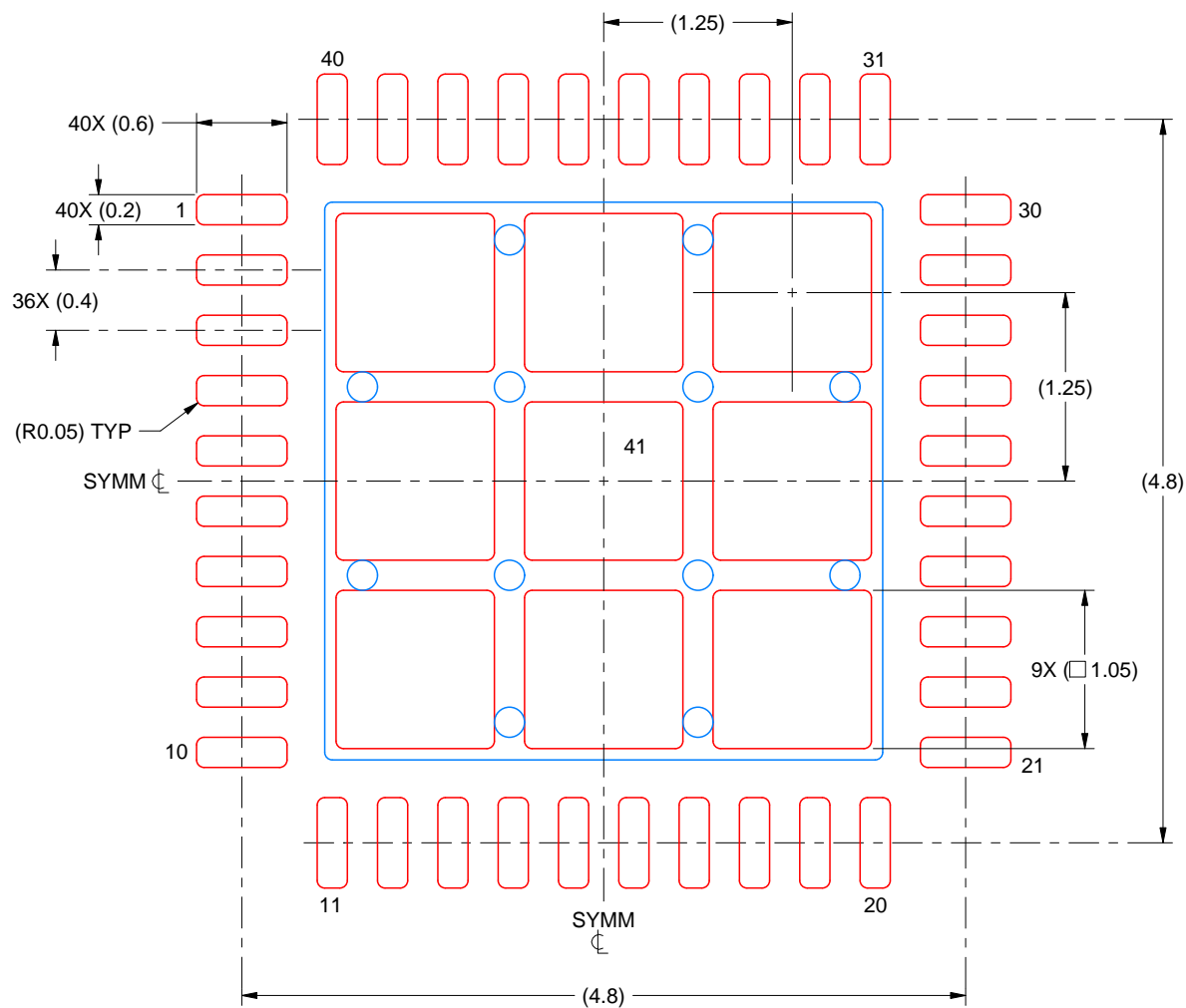
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RSB0040F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



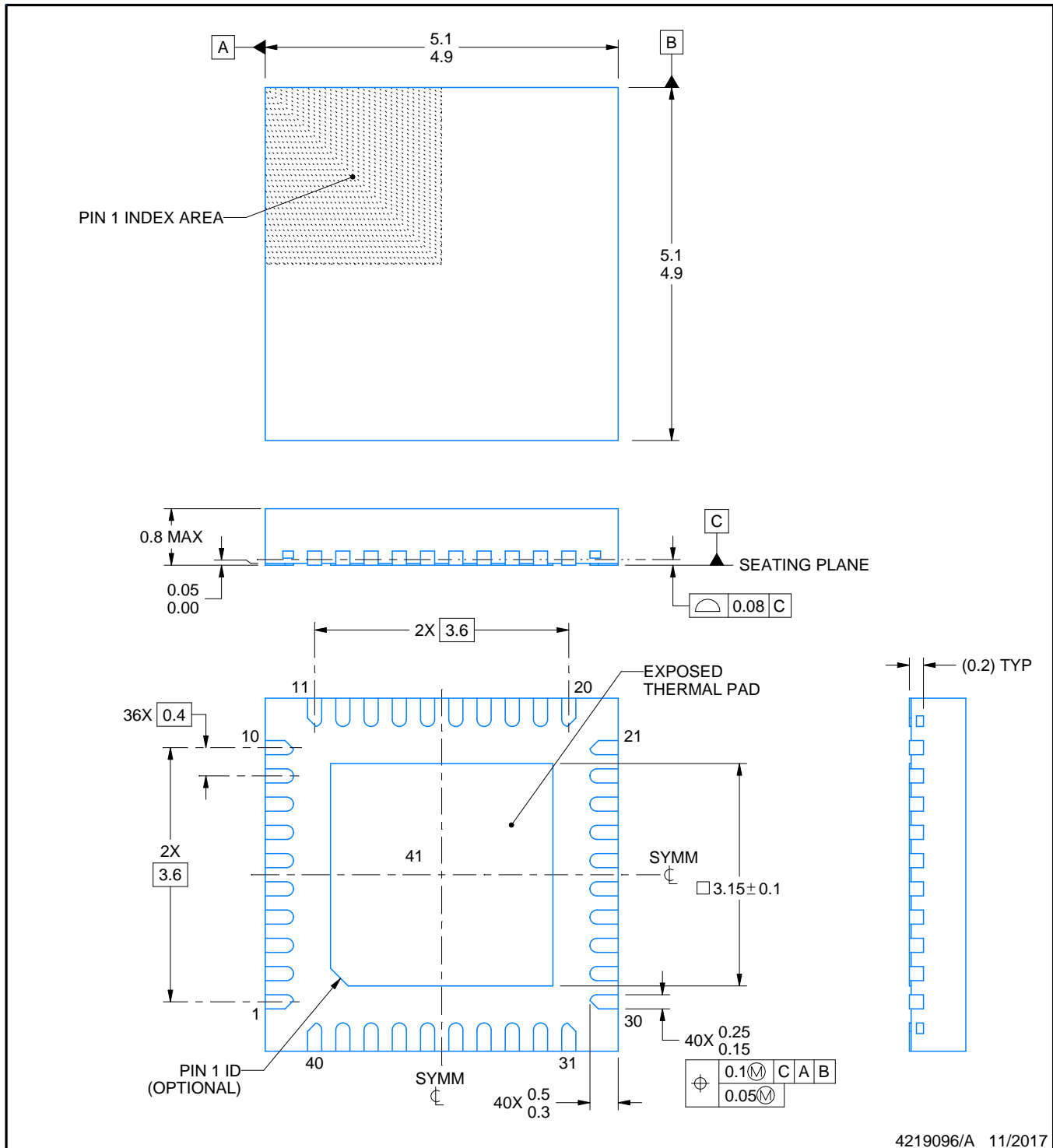
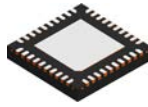
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 41
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4232230/A 09/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

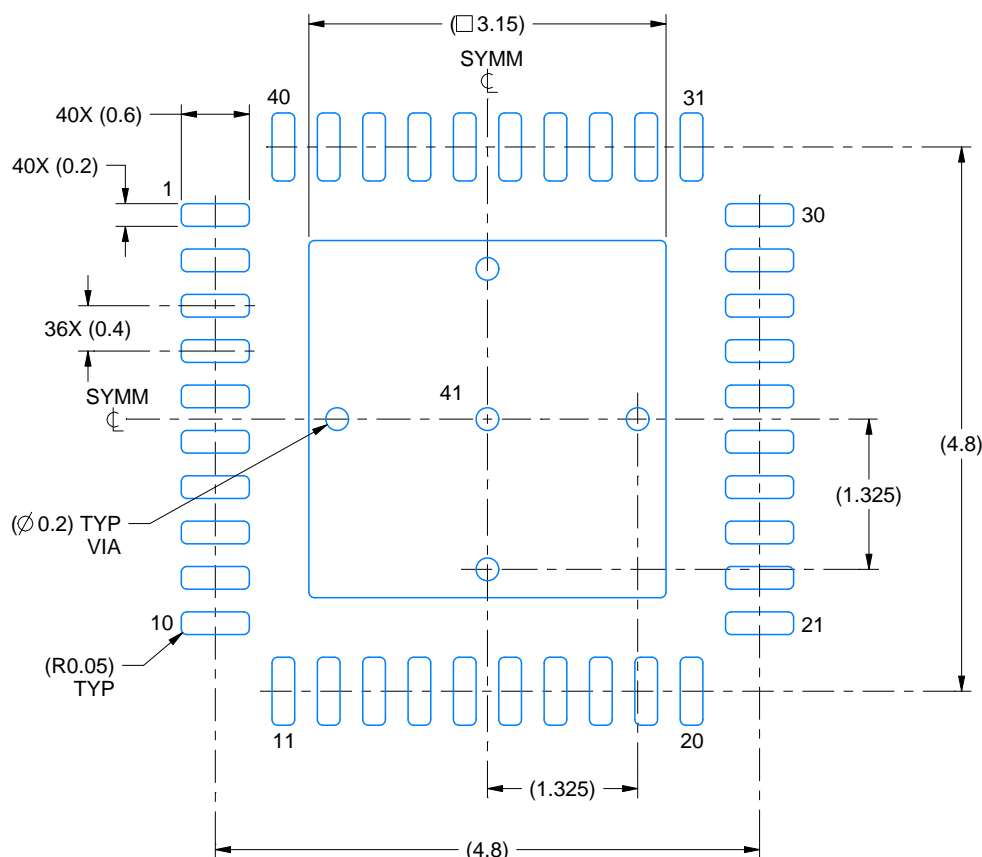
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

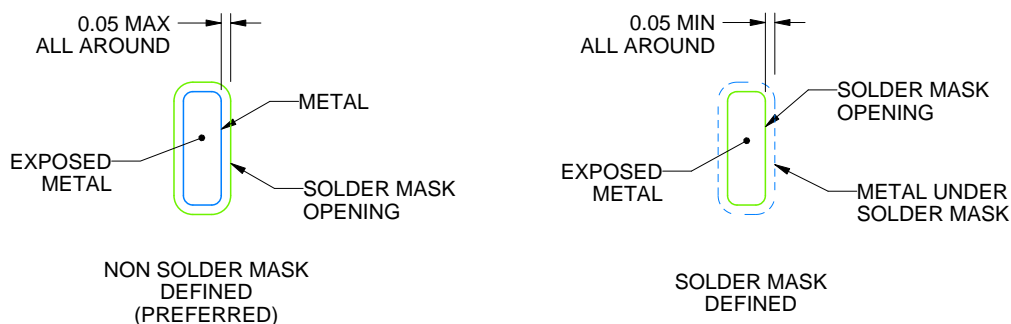
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219096/A 11/2017

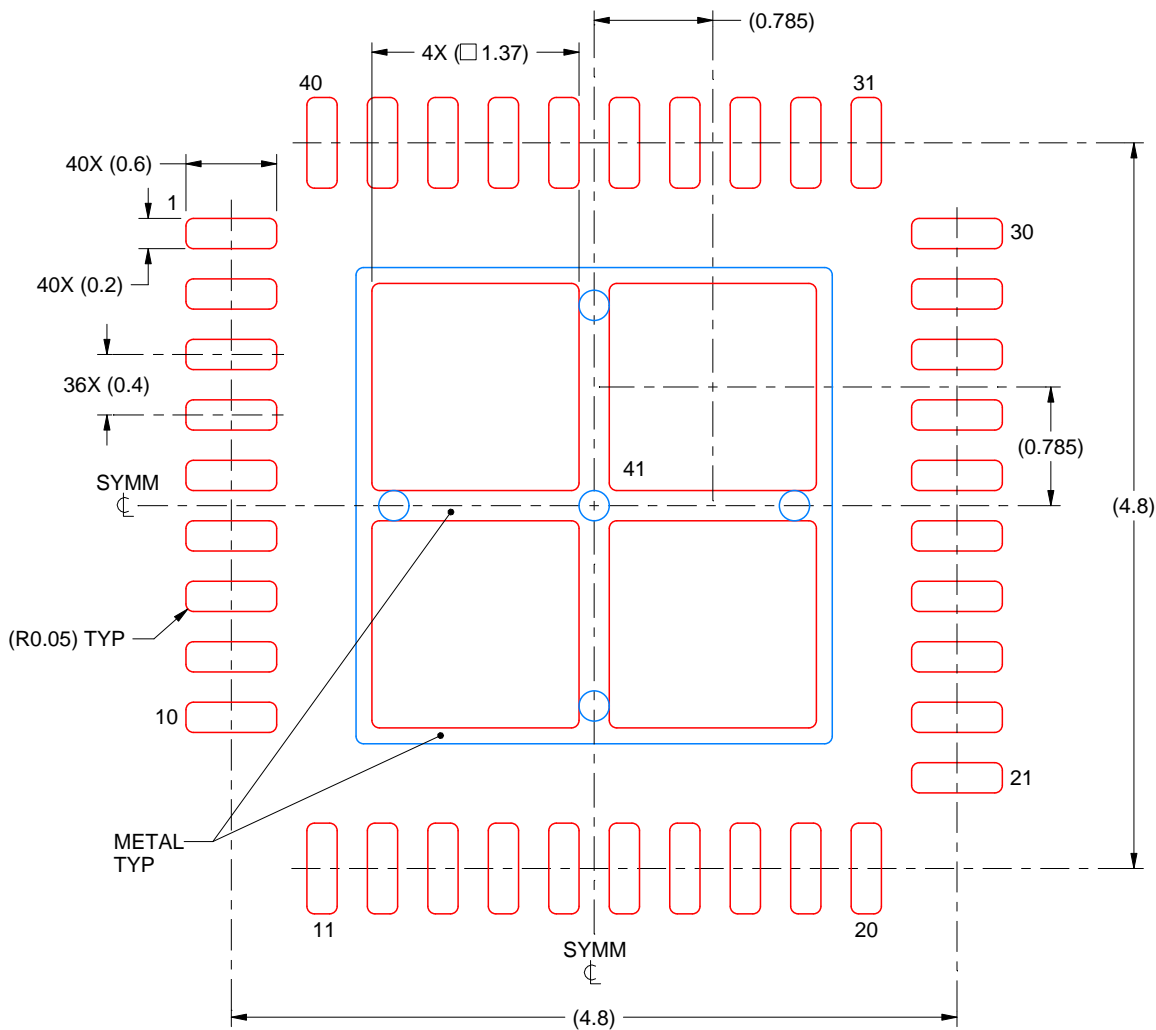
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

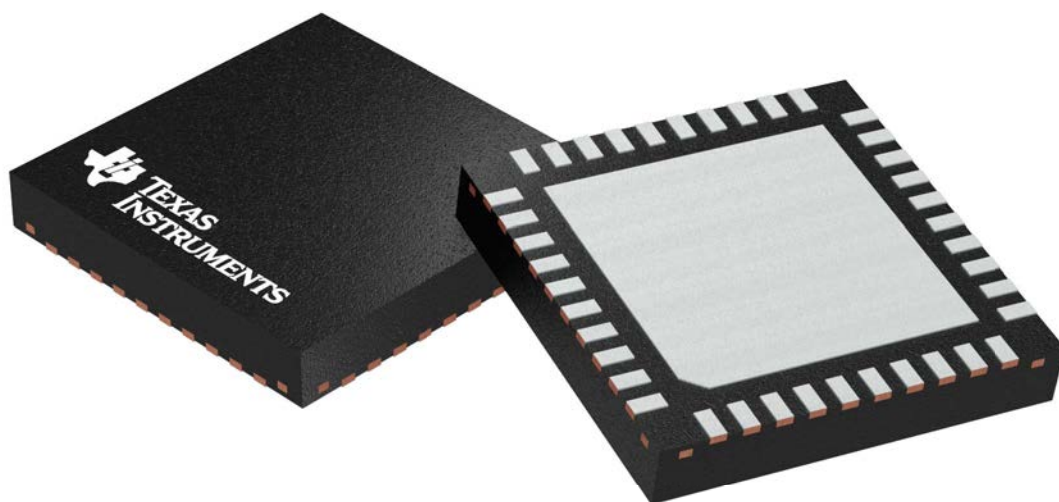
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

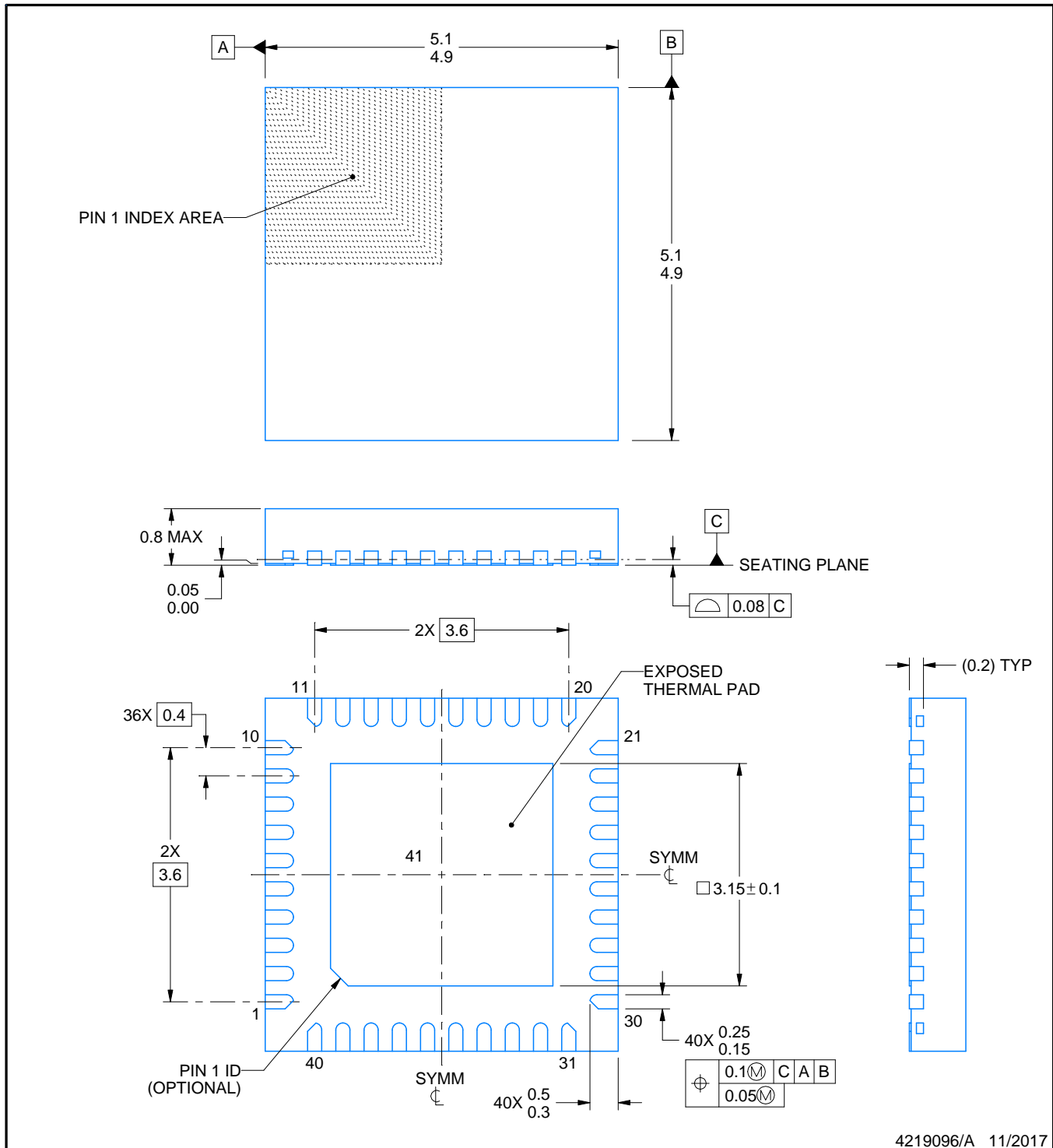
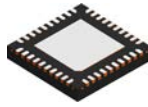
5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207182/D



NOTES:

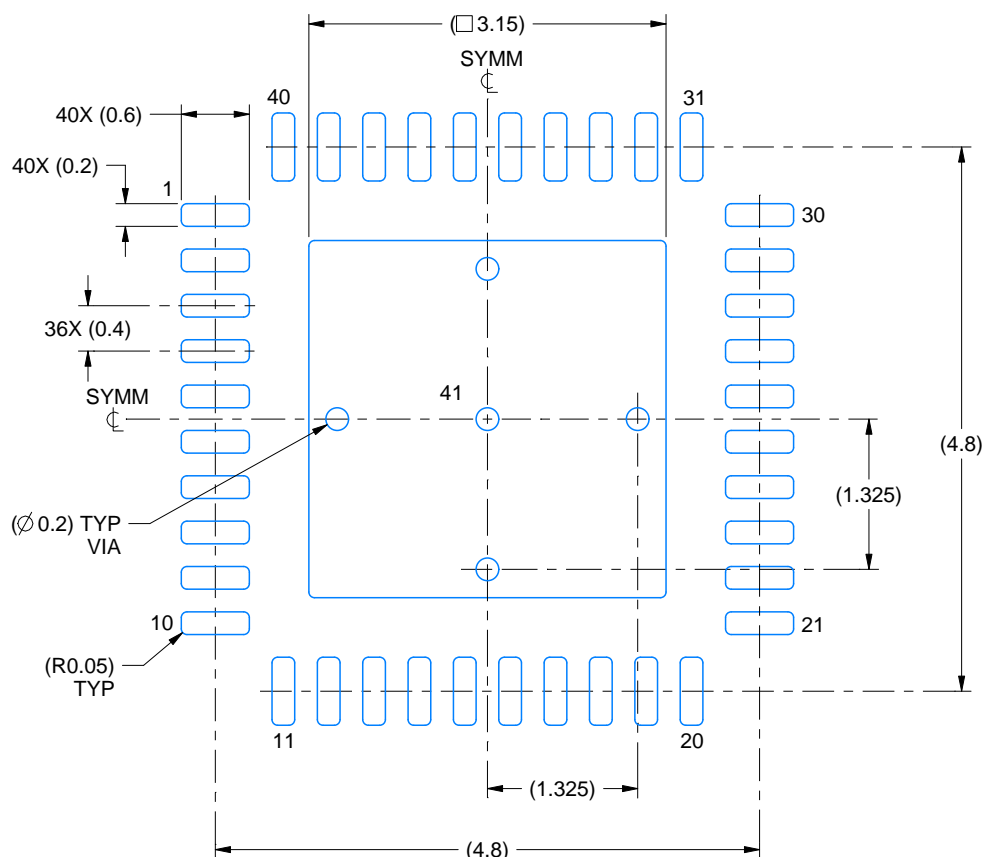
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

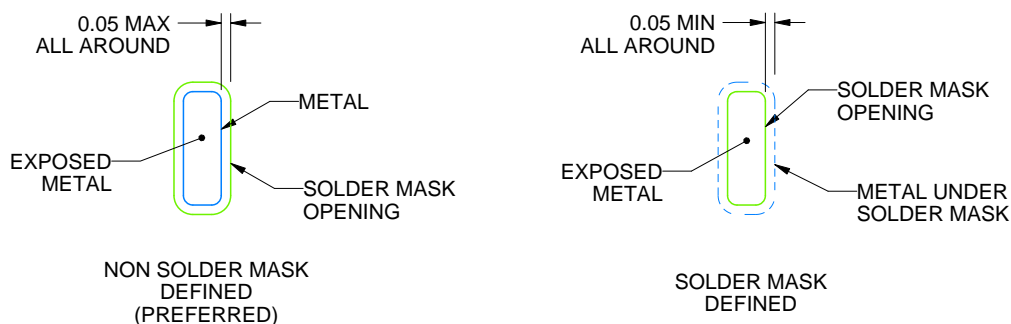
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219096/A 11/2017

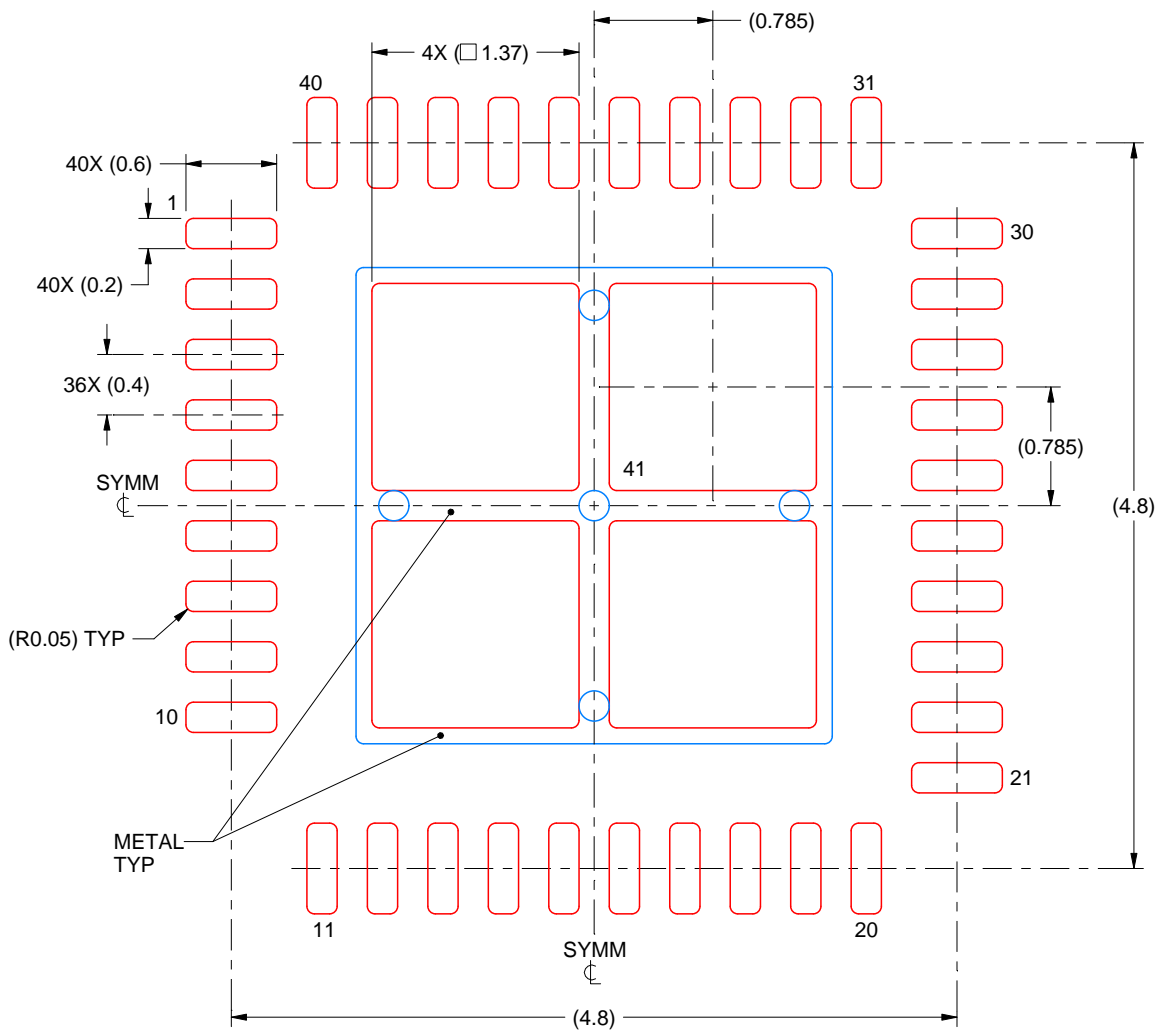
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月