# AM437x Sitara™プロセッサ

## 1 デバイスの概要

### 1.1 特長

- ハイライト
  - Sitara™ ARM® Cortex®-A9 32ビットRISCプロセッサで、最高1000MHz
    - NEON™SIMDコプロセッサ およびベクトル浮動小数点(VFPv3)コプロセッサ
    - 32KBのL1命令およびデータ・キャッシュ
    - 256KBのL2キャッシュまたはL3 RAM
  - 32ビットのLPDDR2、DDR3、DDR3Lをサポート
  - 汎用メモリのサポート(NAND、NOR、SRAM): 最大16ビットのECCをサポート
  - SGX530グラフィック・エンジン
  - ディスプレイ・サブシステム
  - プログラマブル・リアルタイム・ユニット・サブシステムおよび産業用通信サブシステム（PRU-ICSS）
  - リアルタイム・クロック(RTC)
  - 最大2つのUSB 2.0 High-Speed、デュアル・ロール(ホストまたはデバイス)ポート、PHY搭載
  - 10、100、1000イーサネット・スイッチ、最大2ポートをサポート
  - シリアル・インターフェイス
    - 2つのCAN (Controller Area Network)ポート
    - 6つのUART、2つのMcASP、5つのMcSPI、3つのI$^2$Cポート、1つのQSPI、1つのHDQまたは1線式
  - セキュリティ
    - 暗号化ハードウェア・アクセラレータ(AES、SHA、RNG、DES、3DES)
    - セキュア・ブート(AM437x高度セキュリティ[AM437xHS]デバイスでのみ利用可能)
  - 2つの12ビット逐次比較型(SAR) ADC
  - 最大3つの32ビット拡張キャプチャ(eCAP)モジュール
  - 最大3つの拡張直交エンコーダ・パルス(eQEP)モジュール
  - 最大6つの拡張高分解能PWM (eHRPWM)モジュール
- MPUサブシステム
  - 最高1000MHzの処理速度を持つARM Cortex-A9 32ビットRISCマイクロプロセッサ
  - 32KBのL1命令およびデータ・キャッシュ
  - 256KBのL2キャッシュ(L3 RAMとしても構成可能)
  - 256KBのオンチップ・ブートROM
  - 64KBのオンチップRAM
  - セキュア制御モジュール(SCM) (AM437xHSデバイスでのみ利用可能)
  - エミュレーションおよびデバッグ
    - JTAG
    - 組み込みトレース・バッファ
  - 割り込みハンドラ
- オンチップ・メモリ（共有L3 RAM）
  - 256KBの汎用オンチップ・メモリ・コントローラ(OCMC) RAM
  - すべてのマスタからアクセス可能
  - 高速ウェークアップ用の保持をサポート
  - 最大512KBの合計内部RAM
    (L3 RAMとして構成された256KBのARMメモリ + 256KBのOCMC RAM)
- 外部メモリ・インターフェイス(EMIF)
  - DDRコントローラ
    - LPDDR2: 266MHzクロック(データ速度LPDDR2-533)
    - DDR3およびDDR3L: 400MHzクロック(データ速度DDR-800)
    - 32ビット・データ・バス
    - 合計2GBのアドレッシング可能領域
    - 1つのx32、2つのx16、または4つのx8メモリ・デバイス構成をサポート
- 汎用メモリ・コントローラ(GPMC)
  - 柔軟な8および16ビットの非同期メモリ・インターフェイスと、最大7つのチップ・セレクト(NAND、NOR、Muxed-NOR、SRAM)
  - BCHコードを使用して4、8、または16ビットECCをサポート
  - ハミング・コードを使用して1ビットECCをサポート
- エラー特定モジュール(ELM)
  - GPMCと組み合わせて使用すると、BCHアルゴリズムで生成されたシンドローム多項式により、データ・エラーのアドレスを特定可能
  - BCHアルゴリズムに基づいて、512バイトのブロックごとに4、8、または16ビットのエラーを特定可能
- プログラマブル・リアルタイム・ユニット・サブシステムおよび産業用通信サブシステム（PRU-ICSS）
  - 各種のプロトコルをサポート: EtherCAT®、PROFIBUS®、PROFINET®、EtherNet/IP™、EnDat 2.2など
  - 2つのプログラム可能なリアルタイム・ユニット(PRU)サブシステム、それぞれに2つのPRUコアが付属
    - 各コアは32ビットのロード・アンド・ストアRISCプロセッサで、200MHzで実行可能

  - 単一エラーの検出機能(パリティ)付きの、12KB (PRU-ICSS1)または4KB (PRU-ICSS0)の命令RAM
  - 単一エラーの検出機能(パリティ)付きの、8KB (PRU-ICSS1)または4KB (PRU-ICSS0)のデータRAM
  - 64ビット・アキュムレータを備えたシングル・サイクル32ビット乗算器
  - 拡張GPIOモジュールにより、シフトイン/シフトアウトおよび外部信号の並列ラッチをサポート
- 単一エラーの検出機能(パリティ)付きの、12KB (PRU-ICSS1のみ)の共有RAM
- 各PRUからアクセス可能な3つの120バイト・レジスタ・バンク
- システム入力イベント処理用の、割り込みコントローラ(INTC)モジュール
- 内部および外部マスタをPRU-ICSS内部のリソースに接続する、ローカル相互接続バス
- PRU-ICSS内部のペリフェラル
  - 最大12Mbpsをサポートする、1つのフロー制御ピン付きUARTポート
  - 1つのeCAPモジュール
  - EtherCATなどの産業用イーサネットをサポートする、2つのMIIイーサネット・ポート
  - 1つのMDIOポート
- 2つのPRU-ICSSサブシステムにより産業用通信をサポート

- 電源、リセット、クロック管理(PRCM)モジュール
  - ディープ・スリープ・モードの開始と終了を制御
  - スリープ・シーケンス、電力ドメインのスイッチオフ・シーケンス、ウェークアップ・シーケンス、電力ドメインのスイッチオン・シーケンスを制御
  - クロック
    - 高周波発振器を搭載し、各種のシステムおよびペリフェラル・クロック用のリファレンス・クロック(19.2、24、25、26MHz)を生成
    - 個別のクロックのイネーブル/ディセーブル制御をサポートしているため、サブシステムおよびペリフェラルでの消費電力低減を促進
    - 5つのADPLLによりシステム・クロック(MPUサブシステム、DDRインターフェイス、USB、ペリフェラル [MMCおよびSD、UART、SPI、$I^2C$]、L3、L4、イーサネット、GFX [SGX530]、LCDピクセル・クロック)を生成
  - 電源
    - 2つの切り替え不可電力ドメイン(RTCおよびウェークアップ・ロジック[WAKE-UP])
    - 3つの切り替え可能電力ドメイン(MPUサブシステム、SGX530 [GFX]、ペリフェラルとインフラストラクチャ[PER])
    - 動的電圧周波数スケーリング(DVFS)
- リアルタイム・クロック(RTC)
  - リアルタイムの日付(日、月、年、曜日)および時刻(時、分、秒)情報
  - 32.768kHz発振器、RTCロジック、1.1V内部LDOを内蔵
  - 独立のパワー・オン・リセット(RTC_PWRONRSTn)入力
  - 外部ウェーク・イベント用の専用入力ピン(RTC_WAKEUP)
  - プログラム可能なアラームを使用して、ウェークアップ用にPRCMへ、またはイベント通知用にCortex-A9への内部割り込みを生成可能
  - プログラム可能なアラームと外部出力(RTC_PMIC_EN)を使用して、電力管理ICをイネーブルし、RTC以外の電力ドメインを復元可能
- ペリフェラル
  - 最大2つのUSB 2.0 High-Speed、デュアル・ロール(ホストまたはデバイス)ポート、PHY搭載
  - 最大2つの産業用ギガビット・イーサネットMAC (10、100、1000Mbps)
    - 内蔵スイッチ
    - 各MACはMII、RMII、RGMII、MDIOインターフェイスをサポート
    - イーサネットのMACおよびスイッチは他の機能と独立して動作可能
    - IEEE 1588v2高精度時刻プロトコル(PTP)
  - 最大2つのCANポート
    - CANバージョン2パートAおよびBをサポート
  - 最大2つのマルチチャネル・オーディオ・シリアル・ポート(McASP)
    - 最高50MHzの送信および受信クロック
    - McASPポートごとに最大4つのシリアル・データ・ピン、個々に独立したTXおよびRXクロック
    - 時分割多重化(TDM)、IC間サウンド(I2S)、および類似のフォーマットをサポート
    - デジタル・オーディオ・インターフェイス送信(SPDIF、IEC60958-1、AES-3フォーマット)をサポート
    - 送受信用FIFOバッファ(256バイト)
  - 最大6つのUART
    - すべてのUARTがIrDAおよびCIRモードをサポート
    - すべてのUARTがRTSおよびCTSフロー制御をサポート
    - UART1は完全なモデム制御をサポート
  - 最大5つのマスタおよびスレーブMcSPI
    - McSPI0～McSPI2は最大4つのチップ・セレクトをサポート

  - McSPI3およびMcSPI4は最大2つのチップ・セレクトをサポート
  - 最高48MHz
- 1つのクワッドSPI
  - シリアルNOR FLASHからのXIP (eXecute In Place)をサポート
- 1つのDallas 1-Wire®およびHDQシリアル・インターフェイス
- 最大3つのMMC、SD、SDIOポート
  - 1、4、8ビットMMC、SD、SDIOモード
  - すべてのポートが1.8～3.3Vで動作
  - 最高48MHzのクロック
  - カード検出と書き込み保護をサポート
  - MMC4.3とSDおよびSDIO 2.0仕様に準拠
- 最大3つのI²Cマスタおよびスレーブ・インターフェイス
  - 標準モード(最高100kHz)
  - ファースト・モード(最高400kHz)
- 最大6バンクの汎用I/O (GPIO)
  - バンクごとに32のGPIO (他の機能ピンと多重化)
  - GPIOは割り込み入力として使用可能(バンクごとに最大2つの割り込み入力)
- 最大3つの外部DMAイベント入力、割り込み入力としても使用可能
- 12個の32ビット汎用タイマ
  - DMTIMER1は1msタイマで、オペレーティング・システム(OS)のティックに使用
  - DMTIMER4～DMTIMER7はピン出力
- 1つのパブリック・ウォッチドッグ・タイマ
- 1つのフリーランニング高分解能32kHzカウンタ(synctimer32K)
- 1つのセキュア・ウォッチドッグ・タイマ(AM437xHSデバイスでのみ使用可能)
- SGX530 3Dグラフィック・エンジン
  - タイル・ベースのアーキテクチャにより最大20Mポリゴン/秒を実現
  - ユニバーサル・スケーラブル・シェーダー・エンジンはマルチスレッドのエンジンで、ピクセルおよび頂点シェーダー機能を搭載
  - Microsoft VS3.0、PS3.0、OGL2.0を超える高度なシェーダー機能セット
  - 業界標準APIのDirect3D Mobileと、OGL-ES 1.1および2.0をサポート
  - 粒度の細かいタスク切り替え、負荷分散、電力管理
  - 高度なジオメトリDMAベースの動作により、CPUとの連携は最小限
  - プログラム可能な高品質の画像アンチ・エイリアシング
  - メモリ・アドレッシングの完全な仮想化により、統一メモリ・アーキテクチャでOSが動作可能
- ディスプレイ・サブシステム
  - 表示モード
    - ピクセル・メモリ形式をプログラム可能(ピクセルごとに1、2、4、8ビットのパレット化ピクセル、RGB 16および24ビット、およびYUV 4:2:2)
    - 256×24ビットのRGBエントリ・パレット
    - 最大解像度2048×2048
  - ディスプレイのサポート
    - パッシブおよびアクティブ・カラー、パッシブおよびアクティブ・モノクロームの4種類のディスプレイに対応
    - 4および8ビットのモノクローム・パッシブ・パネル・インターフェイスをサポート(ディザリング・ブロックにより15のグレイスケール・レベルをサポート)
    - RGB 8ビット・カラーのパッシブ・パネル・インターフェイスをサポート(ディザリング・ブロックによりカラー・パネルで3,375色をサポート)
    - RGB 12、16、18、24ビットのアクティブ・パネル・インターフェイスをサポート(複製またはディザリングされたエンコード・ピクセル値)
    - RFBIモジュールにより、リモート・フレーム・バッファ(LCDパネルに組み込まれたもの)に対応
    - RFBIモジュールにより、リモート・フレーム・バッファを部分的リフレッシュ
    - 部分的表示
    - 8、9、12、16ビット・インターフェイス(TDM)での複数サイクル出力フォーマット
  - 信号処理
    - 1つのグラフィック・レイヤ(RGBまたはCLUT)と2つのビデオ・レイヤ(YUV 4:2:2、RGB16、RGB24)のオーバーレイおよびウィンドウ表示のサポート
    - ディスプレイ・インターフェイスでRGB 24ビットをサポート、オプションとしてディザリングによりRGB 18ビット・ピクセル出力と6ビット・フレーム・レート制御(空間的または時間的)に対応
    - 透明カラー・キー(ソースおよびデスティネーション)
    - バッファ更新の同期
    - ガンマ曲線のサポート
    - 複数のバッファのサポート
    - クロッピングのサポート
    - カラー・フェーズの回転
- 2つの12ビットSAR ADC (ADC0、ADC1)
  - 毎秒867Kサンプル
  - 入力は、8:1アナログ・スイッチにより多重化された8つのアナログ入力のどれからでも選択可能
  - ADC0は4、5、8線式の抵抗性タッチ・スクリーン・コントローラ(TSC)で動作するよう構成可能
- 最大3つの32ビットeCAPモジュール
  - 3つのキャプチャ入力、または3つの補助PWM出力として構成可能
- 最大6つの拡張eHRPWMモジュール
  - 専用の16ビットの時間ベース・カウンタ、時間お

  - よび周波数の制御機能付き
  - 6つのシングル・エンド、6つのデュアル・エッジ対称型、または3つのデュアル・エッジ非対称型出力として構成可能
  - 最大3つの32ビットeQEPモジュール
- デバイス識別情報
  - 電気ヒューズ・ファーム(FuseFarm)を出荷時にプログラム可能
  - 製造ID
  - デバイス部品番号(固有のJTAG ID)
  - デバイスのリビジョン(ホストのARMから読み取り可能)
  - セキュリティ・キー(AM437xHSデバイスでのみ使用可能)
  - 機能識別情報
- デバッグ・インターフェイスのサポート
  - ARM (Cortex-A9およびPRCM)およびPRU-ICSSデバッグ用のJTAGおよびcJTAG
  - リアルタイム・トレース・ピンのサポート(Cortex-A9用)
  - 64KBの組み込みトレース・バッファ(ETB)
  - デバイスの境界スキャンをサポート
  - IEEE 1500をサポート
- DMA
  - オンチップの拡張DMAコントローラ(EDMA)に、3つのサードパーティー転送コントローラ(TPTC)および1つのサードパーティー・チャネル・コントローラ(TPCC)を搭載し、最大64のプログラム可能な論理チャネルおよび8つのQDMAチャネルをサポート
  - EDMAは次の目的に使用
    - オンチップ・メモリとの間の転送
    - 外部ストレージ(EMIF、GPMC、スレーブ・ペリフェラル)との間の転送
- プロセッサ間通信(IPC)
  - Cortex-A9、PRCM、およびPRU-ICSS間のプロセス同期のため、IPCおよびスピンロック用のハードウェア・ベースのメールボックスを内蔵
- ブート・モード
  - ブート・モードは、PWRONRSTnリセット入力ピンの立ち上がりエッジでラッチされるブート構成ピンにより選択
- カメラ
  - デュアル・ポートの8および10ビットBT656インターフェイス
  - デュアル・ポートの8および10ビット、外部同期を含む
  - シングル・ポートの12ビット
  - YUV422/RGB422およびBT656入力フォーマット
  - RAWフォーマット
  - 最高75MHzのピクセル・クロック速度
- パッケージ
  - 491ピンのBGAパッケージ(17mm×17mm) (ZDN接尾辞)、ボール・ピッチ0.65mm、チャネル・アレイ・テクノロジにより低コストの配線が可能

## 1.2 アプリケーション

- メディカル・モニタ
- ナビゲーション機器
- 産業用オートメーション
- ポータブル・データ端末
- バーコード・スキャナ
- サービス時点管理（POS）
- 携帯用モバイル・ラジオ
- 試験/測定機器

## 1.3 概要

TI AM437x 高性能プロセッサは、ARM Cortex-A9コアを基礎としています。

プロセッサを3Dグラフィック・アクセラレーションで拡張し、豊富なグラフィック・ユーザー・インターフェイスを実現するとともに、EtherCAT、PROFIBUS、EnDatなどの工業用通信プロトコルを含む、決定論的なリアルタイム処理用のコプロセッサが搭載されています。これらのデバイスは、高レベルのオペレーティング・システム(HLOS)をサポートしています。 Linux®は、TIから無料で入手できます。他のHLOSは、TIのDesign Networkおよびエコシステム・パートナーから入手できます。

これらのデバイスは、性能の低いARMコアをベースにするシステムをアップグレードするため使用でき、QSPI-NORやLPDDR2などのメモリ・オプションも含めて、ペリフェラルも更新されています。

これらのプロセッサには、機能ブロック図に示すサブシステムが含まれています。以下で簡単に説明します。

プロセッサ・サブシステムはARM Cortex-A9コアをベースとしており、 PowerVR SGX™グラフィック・アクセラレータ・サブシステムをベースとして、3Dグラフィック・アクセラレーションにより、ディスプレイと高度なユーザー・インターフェイスをサポートします。

プログラム可能なリアルタイム・ユニット・サブシステムと、工業用通信サブシステム(PRU-ICSS)はARMコアと分離されており、独立に動作およびクロック供給を行えるため、効率性と柔軟性が向上しています。PRU-ICSSにより、EtherCAT、PROFINET、EtherNet/IP、PROFIBUS、Ethernet Powerlink、Sercos、EnDat、その他の追加ペリフェラル・インターフェイスやリアルタイム・プロトコルが利用可能になります。PRU-ICSSにより、EnDatや他の工業用通信プロトコルが並列に動作できます。さらに、PRU-ICSSのプログラム可能な性質と、ピン、イベント、およびすべてのシステム・オン・チップ(SoC)リソースにアクセスできることから、高速でリアルタイムの応答、特化したデータ処理操作、カスタム・ペリフェラル・インターフェイスを柔軟に実装でき、SoCの他のプロセッサ・コアをタスクの負荷から解放できます。

高性能の相互接続により、複数のイニシエータから内部および外部のメモリ・コントローラやオンチップ・ペリフェラルへ、高帯域のデータ転送を行えます。また、このデバイスには包括的なクロック管理方式も用意されています。

オンチップのアナログ/デジタル・コンバータ(ADC0)があり、ディスプレイ・サブシステムとの組み合わせにより、統合されたタッチ・スクリーン・ソリューションを実現できます。もう1つのADC (ADC1)は、パルス幅モジュールとの組み合わせにより、閉ループのモータ制御ソリューションを作成できます。

RTCは、別の電力ドメインに基準クロックを供給でき、バッテリでバックアップされた基準クロックを実現可能です。

カメラ・インターフェイスは、シングルまたはデュアル・カメラのパラレル・ポート用に構成できます。

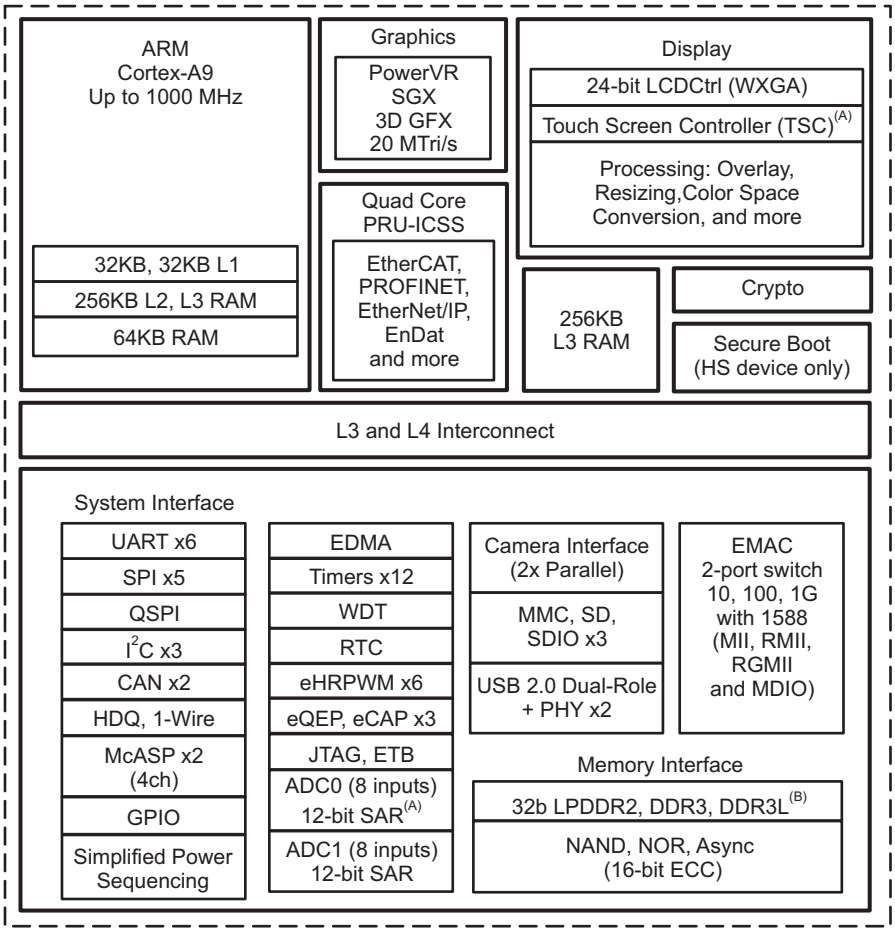
すべてのデバイスで、暗号化アクセラレーションが使用可能です。セキュアなブートのサポート、デバッグ・セキュリティ、信頼される実行環境のサポートなど、サポートされる他のセキュリティ機能はすべて、高セキュリティ(HS)デバイスで使用可能です。HSデバイスの詳細については、TI販売代理店にお問い合わせください。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ |
|---|---|---|
| AM4372ZDN | NFBGA (491) | 17.0mm×17.0mm |
| AM4376ZDN | NFBGA (491) | 17.0mm×17.0mm |
| AM4377ZDN | NFBGA (491) | 17.0mm×17.0mm |
| AM4378ZDN | NFBGA (491) | 17.0mm×17.0mm |
| AM4379ZDN | NFBGA (491) | 17.0mm×17.0mm |

(1) 詳細については、7、「*メカニカル、パッケージ、および注文情報*」を参照してください。

## 1.4 機能ブロック図






A. TSCを使用すると、利用可能なADC0入力が制限されます。
B. 最大クロック: LPDDR2 = 266MHz、DDR3/DDR3L = 400MHz

**図 1-1. 機能ブロック図**

# Table of Contents

## 2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**2016年8月15日発行分から2019年01月15日発行分への変更 (from D Revision (August 2016) to E Revision)** **Page**

# 3 Device Comparison

表 3-1 shows the features supported across different AM437x devices.

**表 3-1. Device Features Comparison**

| FUNCTION | AM4372 | AM4376 | AM4377 | AM4378 | AM4379 |
|---|---|---|---|---|---|
| ARM Cortex-A9 | Yes | Yes | Yes | Yes | Yes |
| Frequency | 600 MHz<br>800 MHz | 300 MHz<br>800 MHz<br>1000 MHz | 800 MHz<br>1000 MHz | 800 MHz<br>1000 MHz | 800 MHz<br>1000 MHz |
| MIPS | 1500<br>2000 | 750<br>2000<br>2500 | 2000<br>2500 | 2000<br>2500 | 2000<br>2500 |
| On-chip L1 cache | 64KB | 64KB | 64KB | 64KB | 64KB |
| On-chip L2 cache | 256KB | 256KB | 256KB | 256KB | 256KB |
| Graphics accelerator (SGX530) | — | — | — | 3D | 3D |
| Hardware acceleration | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator | Crypto accelerator |
| Programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) | — | Features including basic Industrial protocols | Features including all Industrial protocols | Features including basic Industrial protocols | Features including all Industrial protocols |
| On-chip memory | 256KB | 256KB | 256KB | 256KB | 256KB |
| Display options | DSS | DSS | DSS | DSS | DSS |
| General-purpose memory | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) | 1 16-bit (GPMC, NAND flash, NOR flash, SRAM) |
| DRAM(1) | 1 32-bit (DDR3-800, DDR3L-800, LPDDR2-532) | 1 32-bit (DDR3-800, DDR3L-800, LPDDR2-532) | 1 32-bit (DDR3-800, DDR3L-800, LPDDR2-532) | 1 32-bit (DDR3-800, DDR3L-800, LPDDR2-532) | 1 32-bit (DDR3-800, DDR3L-800, LPDDR2-532) |
| Universal serial bus (USB) | 2 ports | 2 ports | 2 ports | 2 ports | 2 ports |
| Ethernet media access controller (EMAC) with 2-port switch | 10/100/1000<br>2 ports | 10/100/1000<br>2 ports | 10/100/1000<br>2 ports | 10/100/1000<br>2 ports | 10/100/1000<br>2 ports |
| Multimedia card (MMC) | 3 | 3 | 3 | 3 | 3 |
| Controller-area network (CAN) | 2 | 2 | 2 | 2 | 2 |
| Universal asynchronous receiver and transmitter (UART) | 6 | 6 | 6 | 6 | 6 |
| Analog-to-digital converter (ADC) | 2 8-ch 12-bit | 2 8-ch 12-bit | 2 8-ch 12-bit | 2 8-ch 12-bit | 2 8-ch 12-bit |
| Enhanced high-resolution PWM modules (eHRPWM) | 6 | 6 | 6 | 6 | 6 |
| Enhanced capture modules (eCAP) | 3 | 3 | 3 | 3 | 3 |
| Enhanced quadrature encoder pulse (eQEP) | 3 | 3 | 3 | 3 | 3 |
| Real-time clock (RTC) | 1 | 1 | 1 | 1 | 1 |
| Inter-integrated circuit ($I^2C$) | 3 | 3 | 3 | 3 | 3 |
| Multichannel audio serial port (McASP) | 2 | 2 | 2 | 2 | 2 |
| Multichannel serial port interface (McSPI) | 5 | 5 | 5 | 5 | 5 |
| Enhanced direct memory access (EDMA) | 64-Ch | 64-Ch | 64-Ch | 64-Ch | 64-Ch |
| Camera (VPFE) | 12-bit | 12-bit | 12-bit | 12-bit | 12-bit |
| Sync timer (32K) | 1 | 1 | 1 | 1 | 1 |
| HDQ/1-Wire | 1 | 1 | 1 | 1 | 1 |
| QSPI | 1 | 1 | 1 | 1 | 1 |

表 3-1. Device Features Comparison (continued)

| FUNCTION | AM4372 | AM4376 | AM4377 | AM4378 | AM4379 |
|---|---|---|---|---|---|
| Timers | 12 | 12 | 12 | 12 | 12 |
| DEV_FEATURE register value(2) | 0x02FC20FE | 0x02FD20FF | 0x02FF20FF | 0x22FD20FF | 0x22FF20FF |
| Input/output (I/O) supply | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V | 1.8 V, 3.3 V |
| Operating temperature range | 0 to 90°C<br>–40 to 105°C | 0 to 90°C<br>–40 to 105°C<br>–40 to 90°C | –40 to 105°C<br>–40 to 90°C | 0 to 90°C<br>–40 to 105°C<br>–40 to 90°C | –40 to 105°C |

(1) DRAM speeds listed are data rates.

(2) For more details about the DEV_FEATURE register, see the *AM437x Sitara Processors Technical Reference Manual*.

## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links:

**Sitara Processors** Scalable processors based on ARM Cortex-A cores with flexible peripherals, connectivity and unified software support – perfect for sensors to servers.

**Sitara AM437x Processors** Scalable ARM Cortex-A9 from 300 MHz up to 1 GHz. 3D graphics option for enhanced user interface. Quad core PRU-ICSS for industrial Ethernet protocols and position feedback control. Dual camera support for barcode scanning, preview and still pictures. Customer programmable secure boot option.

**Companion Products for AM437x Devices** Review products that are frequently used in conjunction with this product.

**Reference Designs for AM437x Devices** TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

# 4 Terminal Configuration and Functions

## 4.1 Pin Diagrams

注: The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

## Table 4-1. ZDN Ball Map [Section Top Left - Top View]

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 25 | VSS | XTALOUT | XTALIN | gpio5_8 | gpio5_12 | USB1_DRVVBUS | EXTINTn | uart3_rxd |
| 24 | dss_ac_bias_en | VSS_OSC | xdma_event_intr1 | xdma_event_intr0 | gpio5_13 | gpio5_9 | eCAP0_in_PWM0_out | uart3_txd |
| 23 | dss_hsync | dss_vsync | VDDS_OSC | | VDDS_CLKOUT | gpio5_11 | | mcasp0_axr0 |
| 22 | dss_pclk | dss_data0 | | | | VDDSHV5 | WARMRSTn | uart3_ctsn |
| 21 | dss_data1 | dss_data2 | dss_data3 | | | | USB0_DRVVBUS | Reserved |
| 20 | dss_data4 | dss_data5 | dss_data6 | vdd_mpu_mon | | VDDS | gpio5_10 | clkreq |
| 19 | dss_data8 | dss_data9 | dss_data12 | dss_data13 | dss_data7 | CAP_VBB_MPU | | Reserved |
| 18 | dss_data10 | dss_data11 | | | | | | VSS |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-2. ZDN Ball Map [Section Top Middle - Top View]

| | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|
| 25 | uart0_rtsn | uart0_rxd | uart0_ctsn | mcasp0_axr1 | spi4_cs0 | spi4_sclk | spi0_cs1 | USB1_VBUS |
| 24 | uart0_txd | uart3_rtsn | mcasp0_ahclkx | mcasp0_ahclkr | mcasp0_aclkx | spi4_d1 | spi4_d0 | EMU1 |
| 23 | | mcasp0_fsr | mcasp0_aclkr | | EMU0 | spi0_sclk | | spi2_cs0 |
| 22 | | uart1_ctsn | uart1_rtsn | | mcasp0_fsx | spi2_d0 | | spi0_d0 |
| 21 | | uart1_rxd | uart1_txd | | VDDS_PLL_CORE_LCD | VPP | | spi0_d1 |
| 20 | | VDD_MPU | VDD_MPU | | spi2_sclk | spi2_d1 | | spi0_cs0 |
| 19 | | VDD_MPU | VDD_MPU | | VDDSHV3 | VDDS | | VDD_CORE |
| 18 | VDDSHV3 | VDDSHV3 | VSS | VDD_MPU | VDDSHV3 | VDDSHV3 | VSS | VDD_CORE |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-3. ZDN Ball Map [Section Top Right - Top View]

| | U | V | W | Y | AA | AB | AC | AD | AE |
|---|---|---|---|---|---|---|---|---|---|
| 25 | USB1_ID | USB1_DM | USB0_DP | nTRST | TCK | cam1_wen | cam1_field | cam1_hd | VSS |
| 24 | USB0_ID | USB1_DP | USB0_DM | TMS | TDO | I2C0_SDA | cam1_data9 | cam1_data8 | cam1_data7 |
| 23 | USB0_VBUS | | VSSA_USB | PWRONRSTn | VSS | | cam1_vd | cam1_data6 | cam1_data5 |
| 22 | USB1_CE | | USB0_CE | I2C0_SCL | | | | cam1_data4 | cam1_data3 |
| 21 | VDDA1P8V_USB1 | | VDDA1P8V_USB0 | | | | cam1_data1 | cam1_data2 | cam1_pclk |
| 20 | VDDA3P3V_USB1 | | VDDA3P3V_USB0 | TDI | | cam1_data0 | cam0_pclk | cam0_data7 | cam0_data6 |
| 19 | VSS | | | VDDS | cam0_data9 | cam0_data8 | | cam0_data5 | cam0_data4 |
| 18 | VSS | VSS | VDDSHV3 | cam0_data2 | cam0_data3 | cam0_data1 | cam0_field | cam0_vd | cam0_data0 |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-4. ZDN Ball Map [Section Middle Left - Top View]

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 17 | mdio_data | mdio_clk | dss_data14 | dss_data15 | VDDS_PLL_MPU | mii1_rxd0 | VDDSHV6 | VDDSHV6 |
| 16 | rmii1_ref_clk | mii1_rxd1 | mii1_txd3 | mii1_col | mii1_rxd2 | VDDSHV7 | VDDSHV6 | VDD_MPU |
| 15 | mii1_rx_dv | mii1_txd0 | | | | | | VSS |
| 14 | mii1_txd1 | mii1_crs | mii1_rxd3 | mii1_tx_clk | CAP_VDD_SRAM_MPU | VDDS_SRAM_MPU_BB | VDDSHV8 | VDD_MPU |
| 13 | mii1_tx_en | mii1_rx_er | mii1_txd2 | mii1_rx_clk | CAP_VDD_SRAM_CORE | VDDS_SRAM_CORE_BG | VDDSHV8 | VDD_MPU |
| 12 | gpmc_clk | gpmc_csn3 | | | | | | VDDS |
| 11 | gpmc_ad15 | gpmc_ad14 | gpmc_ad13 | gpmc_ad11 | gpmc_ad12 | gpmc_ad10 | VDDSHV9 | VDDSHV9 |
| 10 | gpmc_ad9 | gpmc_ad8 | gpmc_be0n_cle | gpmc_wen | gpmc_oen_ren | gpmc_csn2 | VDDSHV10 | VDDSHV10 |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

**Table 4-5. ZDN Ball Map [Section Middle Middle - Top View]**

| | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|
| 17 | VSS | VDDSHV3 | VSS | VDD_MPU | VDD_CORE | VDD_CORE | VSS | VSS |
| 16 | VDD_MPU | | | VSS | VDD_CORE | VDD_CORE | | |
| 15 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS |
| 14 | VDD_MPU | VSS | VDD_CORE | VDD_CORE | VSS | VSS | VDD_CORE | VDD_CORE |
| 13 | VDD_MPU | | | VSS | VSS | VSS | | |
| 12 | VSS | VSS | VDD_CORE | VDD_CORE | VSS | VSS | VSS | VSS |
| 11 | VDD_CORE | VSS | VSS | VSS | VSS | VSS | VDD_CORE | VDD_CORE |
| 10 | VDD_CORE | | | VSS | VSS | VSS | | |

**Ball Map Position**

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-6. ZDN Ball Map [Section Middle Right - Top View]

| | U | V | W | Y | AA | AB | AC | AD | AE |
|---|---|---|---|---|---|---|---|---|---|
| 17 | VSS | VDDSHV2 | | | | | | cam0_wen | cam0_hd |
| 16 | VSS | VDDSHV2 | VDDSHV2 | VDDA_ADC1 | ADC1_AIN2 | ADC1_AIN1 | ADC1_AIN0 | ADC1_AIN7 | ADC1_AIN6 |
| 15 | VDD_CORE | VDD_CORE | VDDS | ADC1_AIN5 | ADC1_AIN4 | ADC1_AIN3 | VSSA_ADC | ADC1_VREFN | ADC1_VREFP |
| 14 | VSS | VSS | | | | | | ADC0_VREFP | ADC0_VREFN |
| 13 | VSS | VSS | VDD_CORE | ADC0_AIN2 | ADC0_AIN3 | ADC0_AIN4 | ADC0_AIN5 | ADC0_AIN6 | ADC0_AIN7 |
| 12 | VSS | VSS | VDD_CORE | ADC0_AIN1 | ADC0_AIN0 | VDDA_ADC0 | Reserved | VDDS | Reserved |
| 11 | VSS | VSS | | | | | | Reserved | Reserved |
| 10 | VSS | VSS | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | VSS |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-7. ZDN Ball Map [Section Bottom Left - Top View]

| | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 9 | gpmc_advn_ale | gpmc_csn1 | | | | | | VDDSHV11 |
| 8 | gpmc_csn0 | gpmc_ad7 | gpmc_ad6 | gpmc_a11 | gpmc_a6 | VDDS3P3V_IOLDO | gpmc_a10 | VDDSHV11 |
| 7 | gpmc_ad5 | gpmc_ad4 | | gpmc_a4 | gpmc_a5 | gpmc_a8 | | |
| 6 | gpmc_ad3 | gpmc_ad2 | gpmc_a2 | CAP_VDDS1P8V_IOLDO | | gpmc_a7 | VDDS | |
| 5 | gpmc_ad1 | gpmc_ad0 | gpmc_a1 | | | | VDDS_PLL_DDR | |
| 4 | gpmc_a3 | gpmc_a9 | | | | ddr_dqm0 | ddr_d4 | |
| 3 | gpmc_be1n | gpmc_wpn | gpmc_a0 | | ddr_d0 | ddr_d3 | ddr_d5 | |
| 2 | gpmc_wait0 | mmc0_dat2 | mmc0_dat1 | mmc0_cmd | ddr_d1 | ddr_dqs0 | ddr_d6 | ddr_dqm1 |
| 1 | VSS | mmc0_dat3 | mmc0_dat0 | mmc0_clk | ddr_d2 | ddr_dqsn0 | ddr_d7 | ddr_d8 |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

**Table 4-8. ZDN Ball Map [Section Bottom Middle - Top View]**

| | J | K | L | M | N | P | R | T |
|---|---|---|---|---|---|---|---|---|
| 9 | VSS | VSS | VSS | VDD_CORE | VDD_CORE | VSS | VDD_CORE | VDD_CORE |
| 8 | VDDSHV1 | VDDS_DDR | VSS | VDDS_DDR | VDDS_DDR | VSS | VDDS_DDR | VDDS_DDR |
| 7 | VDDSHV1 | VDDS_DDR | | VDDS_DDR | VDDS_DDR | | VDDS_DDR | VDDS_DDR |
| 6 | ddr_d9 | ddr_d13 | | ddr_a10 | ddr_cke1 | | VDDS_DDR | ddr_vref |
| 5 | ddr_d10 | ddr_d14 | | ddr_csn0 | ddr_a13 | | ddr_a5 | ddr_a11 |
| 4 | ddr_d11 | ddr_d15 | | ddr_csn1 | ddr_wen | | ddr_a6 | ddr_a12 |
| 3 | ddr_d12 | ddr_ba2 | | ddr_cke0 | ddr_casn | | ddr_a7 | ddr_a14 |
| 2 | ddr_dqs1 | ddr_ba1 | ddr_a2 | ddr_ck | ddr_rasn | ddr_a3 | ddr_a8 | ddr_a15 |
| 1 | ddr_dqsn1 | ddr_ba0 | ddr_a1 | ddr_nck | ddr_a0 | ddr_a4 | ddr_a9 | ddr_resetn |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## Table 4-9. ZDN Ball Map [Section Bottom Right - Top View]

| | U | V | W | Y | AA | AB | AC | AD | AE |
|---|---|---|---|---|---|---|---|---|---|
| 9 | VSS | VSS | | | Reserved | Reserved | Reserved | VDD_CORE | Reserved |
| 8 | VSS | VDDS_DDR | | | | | | VDDS | VSS |
| 7 | | VDDS_DDR | | Reserved | Reserved | Reserved | Reserved | Reserved | VSS |
| 6 | | ddr_dqm2 | ddr_d23 | Reserved | | Reserved | Reserved | RTC_PMIC_EN | RTC_PWRONRSTn |
| 5 | | ddr_d16 | ddr_d22 | | | | Reserved | VDDS_RTC | RTC_XTALIN |
| 4 | | ddr_d17 | ddr_d21 | ddr_d26 | | | | VSS_RTC | RTC_XTALOUT |
| 3 | | ddr_d18 | | ddr_d25 | ddr_d27 | | ddr_vtp | CAP_VDD_RTC | RTC_WAKEUP |
| 2 | ddr_odt1 | ddr_d19 | ddr_dqsn2 | ddr_d24 | ddr_dqsn3 | ddr_d28 | ddr_d31 | Reserved | RTC_KALDO_ENn |
| 1 | ddr_odt0 | ddr_d20 | ddr_dqs2 | ddr_dqm3 | ddr_dqs3 | ddr_d29 | ddr_d30 | Reserved | VSS |

### Ball Map Position

| | | |
|---|---|---|
| 1 | 2 | 3 |
| 4 | 5 | 6 |
| 7 | 8 | 9 |

## 4.2 Pin Attributes

1. **BALL NUMBER:** Package ball numbers associated with each signals.
2. **PIN NAME:** The name of the package pin.
   **Note**: The table does not take into account subsystem terminal multiplexing options.
3. **SIGNAL NAME**: The signal name for that pin in the mode being used.
4. **MODE:** Multiplexing mode number.
   a. Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the terminal corresponds to the name of the terminal. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.

      **Note:** The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.

   b. Modes 1 to 7 are possible modes for alternate functions. On each terminal, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
5. **TYPE:** Signal direction
   – I = Input
   – O = Output
   – IO = Input and Output
   – D = Open drain
   – DS = Differential
   – A = Analog
   – PWR = Power
   – GND = Ground

   **Note**: In the safe_mode, the buffer is configured in high-impedance.
6. **BALL RESET STATE:** State of the terminal while the active low PWRONRSTn terminal is low.
   – 0: The buffer drives $V_{OL}$ (pulldown or pullup resistor not activated)
     0(PD): The buffer drives $V_{OL}$ with an active pulldown resistor
   – 1: The buffer drives $V_{OH}$ (pulldown or pullup resistor not activated)
     1(PU): The buffer drives $V_{OH}$ with an active pullup resistor
   – Z or OFF: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
7. **BALL RESET REL. STATE:** State of the terminal after the active low PWRONRSTn terminal transitions from low to high.
   – 0: The buffer drives $V_{OL}$ (pulldown or pullup resistor not activated)
     0(PD): The buffer drives $V_{OL}$ with an active pulldown resistor
   – 1: The buffer drives $V_{OH}$ (pulldown or pullup resistor not activated)
     1(PU): The buffer drives $V_{OH}$ with an active pullup resistor
   – Z or OFF: High-impedance.
   – L: High-impedance with an active pulldown resistor
   – H : High-impedance with an active pullup resistor
8. **RESET REL. MODE:** The mode is automatically configured after the active low PWRONRSTn terminal transitions from low to high.
9. **POWER:** The voltage supply that powers the terminal's IO buffers.
10. **HYS:** Indicates if the input buffer is with hysteresis.
11. **BUFFER STRENGTH:** Drive strength of the associated output buffer.
12. **PULLUP OR PULLDOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
13. **IO CELL:** IO cell information.

**Note**: Configuring two terminals to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

## Table 4-10. Pin Attributes (ZDN Package)

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE14 | ADC0_VREFN | ADC0_VREFN | 0x0 | AP | Z | Z | Mode0 | VDDA_ADC0 | NA | NA | NA | Analog |
| AD14 | ADC0_VREFP | ADC0_VREFP | 0x0 | AP | Z | Z | Mode0 | VDDA_ADC0 | NA | NA | NA | Analog |
| AD15 | ADC1_VREFN | ADC1_VREFN | 0x0 | AP | Z | Z | Mode0 | VDDA_ADC1 | NA | NA | NA | Analog |
| AE15 | ADC1_VREFP | ADC1_VREFP | 0x0 | AP | Z | Z | Mode0 | VDDA_ADC1 | NA | NA | NA | Analog |
| AA12 | ADC0_AIN0 | ADC0_AIN0 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| Y12 | ADC0_AIN1 | ADC0_AIN1 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| Y13 | ADC0_AIN2 | ADC0_AIN2 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AA13 | ADC0_AIN3 | ADC0_AIN3 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AB13 | ADC0_AIN4 | ADC0_AIN4 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AC13 | ADC0_AIN5 | ADC0_AIN5 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AD13 | ADC0_AIN6 | ADC0_AIN6 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AE13 | ADC0_AIN7 | ADC0_AIN7 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC0 | NA | 25 | NA | Analog |
| AC16 | ADC1_AIN0 | ADC1_AIN0 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AB16 | ADC1_AIN1 | ADC1_AIN1 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AA16 | ADC1_AIN2 | ADC1_AIN2 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AB15 | ADC1_AIN3 | ADC1_AIN3 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AA15 | ADC1_AIN4 | ADC1_AIN4 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| Y15 | ADC1_AIN5 | ADC1_AIN5 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AE16 | ADC1_AIN6 | ADC1_AIN6 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AD16 | ADC1_AIN7 | ADC1_AIN7 | 0x0 | A | Z | Z | Mode0 | VDDA_ADC1 | NA | 25 | NA | Analog |
| AC18 | cam0_field | cam0_field | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data21 | 0x2 | O | | | | | | | | |
| | | cam0_data10 | 0x3 | I | | | | | | | | |
| | | spi2_sclk | 0x4 | IO | | | | | | | | |
| | | cam1_data10 | 0x5 | I | | | | | | | | |
| | | EMU4 | 0x6 | IO | | | | | | | | |
| | | gpio4_2 | 0x7 | IO | | | | | | | | |
| AE17 | cam0_hd | cam0_hd | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data23 | 0x2 | O | | | | | | | | |
| | | pr1_edio_sof | 0x3 | O | | | | | | | | |
| | | spi2_cs1 | 0x4 | IO | | | | | | | | |
| | | EMU10 | 0x5 | IO | | | | | | | | |
| | | EMU2 | 0x6 | IO | | | | | | | | |
| | | gpio4_0 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AC20 | cam0_pclk | cam0_pclk | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data19 | 0x2 | O | | | | | | | | |
| | | pr0_pru0_gpo14 | 0x3 | O | | | | | | | | |
| | | spi2_cs0 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpi14 | 0x5 | I | | | | | | | | |
| | | EMU6 | 0x6 | IO | | | | | | | | |
| | | gpio4_4 | 0x7 | IO | | | | | | | | |
| | | I2C2_SDA | 0x8 | IOD | | | | | | | | |
| AD18 | cam0_vd | cam0_vd | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data22 | 0x2 | O | | | | | | | | |
| | | pr1_edio_outvalid | 0x3 | O | | | | | | | | |
| | | spi2_d1 | 0x4 | IO | | | | | | | | |
| | | EMU11 | 0x5 | IO | | | | | | | | |
| | | EMU3 | 0x6 | IO | | | | | | | | |
| | | gpio4_1 | 0x7 | IO | | | | | | | | |
| AD17 | cam0_wen | cam0_wen | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data20 | 0x2 | O | | | | | | | | |
| | | cam0_data11 | 0x3 | I | | | | | | | | |
| | | spi2_d0 | 0x4 | IO | | | | | | | | |
| | | cam1_data11 | 0x5 | I | | | | | | | | |
| | | EMU5 | 0x6 | IO | | | | | | | | |
| | | gpio4_3 | 0x7 | IO | | | | | | | | |
| AC25 | cam1_field | cam1_field | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr7 | 0x1 | I | | | | | | | | |
| | | ext_hw_trigger | 0x2 | I | | | | | | | | |
| | | cam0_data10 | 0x3 | I | | | | | | | | |
| | | spi2_cs1 | 0x4 | IO | | | | | | | | |
| | | cam1_data10 | 0x5 | I | | | | | | | | |
| | | ehrpwm1B | 0x6 | O | | | | | | | | |
| | | gpio4_12 | 0x7 | IO | | | | | | | | |
| | | ehrpwm3A | 0x8 | O | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD25 | cam1_hd | cam1_hd | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr4 | 0x1 | I | | | | | | | | |
| | | spi0_cs3 | 0x2 | IO | | | | | | | | |
| | | pr0_pru1_gpo1 | 0x3 | O | | | | | | | | |
| | | spi2_cs0 | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpi1 | 0x5 | I | | | | | | | | |
| | | ehrpwm0A | 0x6 | O | | | | | | | | |
| | | gpio4_9 | 0x7 | IO | | | | | | | | |
| AE21 | cam1_pclk | cam1_pclk | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr6 | 0x1 | I | | | | | | | | |
| | | spi1_cs3 | 0x2 | IO | | | | | | | | |
| | | pr0_pru1_gpo3 | 0x3 | O | | | | | | | | |
| | | spi2_sclk | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpi3 | 0x5 | I | | | | | | | | |
| | | ehrpwm1A | 0x6 | O | | | | | | | | |
| | | gpio4_11 | 0x7 | IO | | | | | | | | |
| AC23 | cam1_vd | cam1_vd | 0x0 | IO | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr5 | 0x1 | I | | | | | | | | |
| | | spi1_cs2 | 0x2 | IO | | | | | | | | |
| | | pr0_pru1_gpo2 | 0x3 | O | | | | | | | | |
| | | spi2_cs2 | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpi2 | 0x5 | I | | | | | | | | |
| | | ehrpwm0B | 0x6 | O | | | | | | | | |
| | | gpio4_10 | 0x7 | IO | | | | | | | | |
| AB25 | cam1_wen | cam1_wen | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr8 | 0x1 | I | | | | | | | | |
| | | pr1_edio_sof | 0x2 | O | | | | | | | | |
| | | cam0_data11 | 0x3 | I | | | | | | | | |
| | | spi2_d1 | 0x4 | IO | | | | | | | | |
| | | cam1_data11 | 0x5 | I | | | | | | | | |
| | | EMU11 | 0x6 | IO | | | | | | | | |
| | | gpio4_13 | 0x7 | IO | | | | | | | | |
| | | ehrpwm3B | 0x8 | O | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE18 | cam0_data0 | cam0_data0 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | cam1_data9 | 0x2 | I | | | | | | | | |
| | | I2C1_SDA | 0x3 | IOD | | | | | | | | |
| | | pr0_pru1_gpo16 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi16 | 0x5 | I | | | | | | | | |
| | | ehrpwm0_synco | 0x6 | O | | | | | | | | |
| | | gpio5_19 | 0x7 | IO | | | | | | | | |
| AB18 | cam0_data1 | cam0_data1 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | cam1_data8 | 0x2 | I | | | | | | | | |
| | | I2C1_SCL | 0x3 | IOD | | | | | | | | |
| | | pr0_pru1_gpo17 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi17 | 0x5 | I | | | | | | | | |
| | | ehrpwm3_synco | 0x6 | O | | | | | | | | |
| | | gpio5_20 | 0x7 | IO | | | | | | | | |
| Y18 | cam0_data2 | cam0_data2 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_clk | 0x1 | IO | | | | | | | | |
| | | cam1_data10 | 0x2 | I | | | | | | | | |
| | | qspi_clk | 0x3 | IO | | | | | | | | |
| | | gpio4_24 | 0x7 | IO | | | | | | | | |
| AA18 | cam0_data3 | cam0_data3 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_cmd | 0x1 | IO | | | | | | | | |
| | | cam1_data11 | 0x2 | I | | | | | | | | |
| | | qspi_csn | 0x3 | O | | | | | | | | |
| | | gpio4_25 | 0x7 | IO | | | | | | | | |
| AE19 | cam0_data4 | cam0_data4 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat0 | 0x1 | IO | | | | | | | | |
| | | cam1_wen | 0x2 | I | | | | | | | | |
| | | qspi_d0 | 0x3 | IO | | | | | | | | |
| | | ehrpwm3A | 0x6 | O | | | | | | | | |
| | | gpio4_26 | 0x7 | IO | | | | | | | | |
| AD19 | cam0_data5 | cam0_data5 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat1 | 0x1 | IO | | | | | | | | |
| | | qspi_d1 | 0x3 | I | | | | | | | | |
| | | ehrpwm3B | 0x6 | O | | | | | | | | |
| | | gpio4_27 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AE20 | cam0_data6 | cam0_data6 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat2 | 0x1 | IO | | | | | | | | |
| | | qspi_d2 | 0x3 | I | | | | | | | | |
| | | ehrpwm1A | 0x6 | O | | | | | | | | |
| | | gpio4_28 | 0x7 | IO | | | | | | | | |
| AD20 | cam0_data7 | cam0_data7 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat3 | 0x1 | IO | | | | | | | | |
| | | qspi_d3 | 0x3 | I | | | | | | | | |
| | | ehrpwm1B | 0x6 | O | | | | | | | | |
| | | gpio4_29 | 0x7 | IO | | | | | | | | |
| AB19 | cam0_data8 | cam0_data8 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data18 | 0x2 | O | | | | | | | | |
| | | pr0_pru0_gpo15 | 0x3 | O | | | | | | | | |
| | | spi2_cs2 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpi15 | 0x5 | I | | | | | | | | |
| | | EMU7 | 0x6 | IO | | | | | | | | |
| | | gpio4_5 | 0x7 | IO | | | | | | | | |
| | | I2C2_SCL | 0x8 | IOD | | | | | | | | |
| AA19 | cam0_data9 | cam0_data9 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data17 | 0x2 | O | | | | | | | | |
| | | pr0_pru0_gpo16 | 0x3 | O | | | | | | | | |
| | | spi2_cs3 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpi16 | 0x5 | I | | | | | | | | |
| | | EMU8 | 0x6 | IO | | | | | | | | |
| | | gpio4_6 | 0x7 | IO | | | | | | | | |
| AB20 | cam1_data0 | cam1_data0 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_rxd | 0x1 | IO | | | | | | | | |
| | | spi3_d0 | 0x2 | IO | | | | | | | | |
| | | I2C2_SDA | 0x3 | IOD | | | | | | | | |
| | | ehrpwm0_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio4_14 | 0x7 | IO | | | | | | | | |
| AC21 | cam1_data1 | cam1_data1 | 0x0 | I | H | H | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_txd | 0x1 | IO | | | | | | | | |
| | | spi3_d1 | 0x2 | IO | | | | | | | | |
| | | I2C2_SCL | 0x3 | IOD | | | | | | | | |
| | | ehrpwm0_synci | 0x6 | I | | | | | | | | |
| | | gpio4_15 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD21 | cam1_data2 | cam1_data2 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_ctsn | 0x1 | IO | | | | | | | | |
| | | spi3_cs0 | 0x2 | IO | | | | | | | | |
| | | mmc2_clk | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo10 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi10 | 0x5 | I | | | | | | | | |
| | | ehrpwm1_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio4_16 | 0x7 | IO | | | | | | | | |
| AE22 | cam1_data3 | cam1_data3 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_rtsn | 0x1 | O | | | | | | | | |
| | | spi3_sclk | 0x2 | IO | | | | | | | | |
| | | mmc2_cmd | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo11 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi11 | 0x5 | I | | | | | | | | |
| | | pr1_edc_latch0_in | 0x6 | I | | | | | | | | |
| | | gpio4_17 | 0x7 | IO | | | | | | | | |
| AD22 | cam1_data4 | cam1_data4 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_rin | 0x1 | I | | | | | | | | |
| | | uart2_rxd | 0x2 | IO | | | | | | | | |
| | | mmc2_dat0 | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo12 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi12 | 0x5 | I | | | | | | | | |
| | | pr1_edc_latch1_in | 0x6 | I | | | | | | | | |
| | | gpio4_18 | 0x7 | IO | | | | | | | | |
| | | uart0_dcdn | 0x8 | I | | | | | | | | |
| AE23 | cam1_data5 | cam1_data5 | 0x0 | I | H | H | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_dsrn | 0x1 | I | | | | | | | | |
| | | uart2_txd | 0x2 | IO | | | | | | | | |
| | | mmc2_dat1 | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo13 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi13 | 0x5 | I | | | | | | | | |
| | | pr1_edio_latch_in | 0x6 | I | | | | | | | | |
| | | gpio4_19 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD23 | cam1_data6 | cam1_data6 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_dcdn | 0x1 | I | | | | | | | | |
| | | uart2_ctsn | 0x2 | IO | | | | | | | | |
| | | mmc2_dat2 | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo14 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi14 | 0x5 | I | | | | | | | | |
| | | pr1_edio_data_in0 | 0x6 | I | | | | | | | | |
| | | gpio4_20 | 0x7 | IO | | | | | | | | |
| AE24 | cam1_data7 | cam1_data7 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | uart1_dtrn | 0x1 | O | | | | | | | | |
| | | uart2_rtsn | 0x2 | O | | | | | | | | |
| | | mmc2_dat3 | 0x3 | IO | | | | | | | | |
| | | pr0_pru1_gpo15 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi15 | 0x5 | I | | | | | | | | |
| | | pr1_edio_data_in1 | 0x6 | I | | | | | | | | |
| | | gpio4_21 | 0x7 | IO | | | | | | | | |
| AD24 | cam1_data8 | cam1_data8 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr3 | 0x1 | I | | | | | | | | |
| | | spi0_cs2 | 0x2 | IO | | | | | | | | |
| | | pr0_pru1_gpo0 | 0x3 | O | | | | | | | | |
| | | spi2_d0 | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpi0 | 0x5 | I | | | | | | | | |
| | | EMU10 | 0x6 | IO | | | | | | | | |
| | | gpio4_8 | 0x7 | IO | | | | | | | | |
| | | uart0_rtsn | 0x8 | O | | | | | | | | |
| AC24 | cam1_data9 | cam1_data9 | 0x0 | I | L | L | Mode7 | VDDSHV2 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data16 | 0x2 | O | | | | | | | | |
| | | pr0_pru0_gpo17 | 0x3 | O | | | | | | | | |
| | | spi2_cs3 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpi17 | 0x5 | I | | | | | | | | |
| | | EMU9 | 0x6 | IO | | | | | | | | |
| | | gpio4_7 | 0x7 | IO | | | | | | | | |
| | | uart0_ctsn | 0x8 | I | | | | | | | | |
| F19 | CAP_VBB_MPU | CAP_VBB_MPU | NA | A | NA | NA | NA | NA | NA | NA | NA | NA |
| D6 | CAP_VDDS1P8V_IOLDO | CAP_VDDS1P8V_IOLDO | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| AD3 | CAP_VDD_RTC | CAP_VDD_RTC | NA | A | NA | NA | NA | NA | NA | NA | NA | NA |
| E13 | CAP_VDD_SRAM_CORE | CAP_VDD_SRAM_CORE | NA | A | NA | NA | NA | NA | NA | NA | NA | NA |
| E14 | CAP_VDD_SRAM_MPU | CAP_VDD_SRAM_MPU | NA | A | NA | NA | NA | NA | NA | NA | NA | NA |

## Table 4-10. Pin Attributes (ZDN Package) (continued)

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H20 | clkreq | clkreq | 0x0 | O | OFF | H | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio0_24 | 0x7 | IO | | | | | | | | |
| N1 | ddr_a0 | ddr_a0 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| L1 | ddr_a1 | ddr_a1 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| L2 | ddr_a2 | ddr_a2 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| P2 | ddr_a3 | ddr_a3 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| P1 | ddr_a4 | ddr_a4 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| R5 | ddr_a5 | ddr_a5 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| R4 | ddr_a6 | ddr_a6 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| R3 | ddr_a7 | ddr_a7 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| R2 | ddr_a8 | ddr_a8 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| R1 | ddr_a9 | ddr_a9 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M6 | ddr_a10 | ddr_a10 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| T5 | ddr_a11 | ddr_a11 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| T4 | ddr_a12 | ddr_a12 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| N5 | ddr_a13 | ddr_a13 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| T3 | ddr_a14 | ddr_a14 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| T2 | ddr_a15 | ddr_a15 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K1 | ddr_ba0 | ddr_ba0 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K2 | ddr_ba1 | ddr_ba1 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K3 | ddr_ba2 | ddr_ba2 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| N3 | ddr_casn | ddr_casn | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M2 | ddr_ck | ddr_ck | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M3 | ddr_cke0 | ddr_cke0 | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N6 | ddr_cke1 | ddr_cke1 | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M5 | ddr_csn0 | ddr_csn0 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M4 | ddr_csn1 | ddr_csn1 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| E3 | ddr_d0 | ddr_d0 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| E2 | ddr_d1 | ddr_d1 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| E1 | ddr_d2 | ddr_d2 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| F3 | ddr_d3 | ddr_d3 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| G4 | ddr_d4 | ddr_d4 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| G3 | ddr_d5 | ddr_d5 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| G2 | ddr_d6 | ddr_d6 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| G1 | ddr_d7 | ddr_d7 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| H1 | ddr_d8 | ddr_d8 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J6 | ddr_d9 | ddr_d9 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J5 | ddr_d10 | ddr_d10 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J4 | ddr_d11 | ddr_d11 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J3 | ddr_d12 | ddr_d12 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K6 | ddr_d13 | ddr_d13 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K5 | ddr_d14 | ddr_d14 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| K4 | ddr_d15 | ddr_d15 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| V5 | ddr_d16 | ddr_d16 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| V4 | ddr_d17 | ddr_d17 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| V3 | ddr_d18 | ddr_d18 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| V2 | ddr_d19 | ddr_d19 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V1 | ddr_d20 | ddr_d20 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| W4 | ddr_d21 | ddr_d21 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| W5 | ddr_d22 | ddr_d22 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| W6 | ddr_d23 | ddr_d23 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| Y2 | ddr_d24 | ddr_d24 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| Y3 | ddr_d25 | ddr_d25 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| Y4 | ddr_d26 | ddr_d26 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AA3 | ddr_d27 | ddr_d27 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AB2 | ddr_d28 | ddr_d28 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AB1 | ddr_d29 | ddr_d29 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AC1 | ddr_d30 | ddr_d30 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AC2 | ddr_d31 | ddr_d31 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| F4 | ddr_dqm0 | ddr_dqm0 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| H2 | ddr_dqm1 | ddr_dqm1 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| V6 | ddr_dqm2 | ddr_dqm2 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| Y1 | ddr_dqm3 | ddr_dqm3 | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| F2 | ddr_dqs0 | ddr_dqs0 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J2 | ddr_dqs1 | ddr_dqs1 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| W1 | ddr_dqs2 | ddr_dqs2 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| AA1 | ddr_dqs3 | ddr_dqs3 | 0x0 | IO | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| F1 | ddr_dqsn0 | ddr_dqsn0 | 0x0 | IO | H | | Mode0 | VDDS_DDR | Yes | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| J1 | ddr_dqsn1 | ddr_dqsn1 | 0x0 | IO | H | | Mode0 | VDDS_DDR | Yes | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| W2 | ddr_dqsn2 | ddr_dqsn2 | 0x0 | IO | H | | Mode0 | VDDS_DDR | Yes | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AA2 | ddr_dqsn3 | ddr_dqsn3 | 0x0 | IO | H | | Mode0 | VDDS_DDR | Yes | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| M1 | ddr_nck | ddr_nck | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| U1 | ddr_odt0 | ddr_odt0 | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| U2 | ddr_odt1 | ddr_odt1 | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| N2 | ddr_rasn | ddr_rasn | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| T1 | ddr_resetn | ddr_resetn | 0x0 | O | L | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS |
| T6 | ddr_vref | ddr_vref | 0x0 | AP (24) | NA | NA | Mode0 | VDDS_DDR | NA | NA | NA | Analog |
| AC3 | ddr_vtp | ddr_vtp | 0x0 | I (25) | NA | NA | Mode0 | VDDS_DDR | NA | NA | NA | Analog |
| N4 | ddr_wen | ddr_wen | 0x0 | O | H | | Mode0 | VDDS_DDR | YES | 8 (4) | PU/PD | LVCMOS/HSTL/HSUL_12 |
| A24 | dss_ac_bias_en | dss_ac_bias_en | 0x0 | O | OFF | OFF (5) | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a11 | 0x1 | O | | | | | | | | |
| | | gpmc_a4 | 0x2 | O | | | | | | | | |
| | | pr1_edio_data_in5 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out5 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpo9 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi9 | 0x6 | I | | | | | | | | |
| | | gpio2_25 | 0x7 | IO | | | | | | | | |
| B22 | dss_data0 (6) | dss_data0 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a0 | 0x1 | O | | | | | | | | |
| | | pr1_mii_mt0_clk | 0x2 | I | | | | | | | | |
| | | ehrpwm2A | 0x3 | O | | | | | | | | |
| | | pr1_pru0_gpo0 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi0 | 0x6 | I | | | | | | | | |
| | | gpio2_6 | 0x7 | IO | | | | | | | | |
| A21 | dss_data1 (6) | dss_data1 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a1 | 0x1 | O | | | | | | | | |
| | | pr1_mii0_txen | 0x2 | O | | | | | | | | |
| | | ehrpwm2B | 0x3 | O | | | | | | | | |
| | | pr1_pru0_gpo1 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi1 | 0x6 | I | | | | | | | | |
| | | gpio2_7 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B21 | dss_data2 (6) | dss_data2 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a2 | 0x1 | O | | | | | | | | |
| | | pr1_mii0_txd3 | 0x2 | O | | | | | | | | |
| | | ehrpwm2_tripzone_input | 0x3 | I | | | | | | | | |
| | | pr1_pru0_gpo2 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi2 | 0x6 | I | | | | | | | | |
| | | gpio2_8 | 0x7 | IO | | | | | | | | |
| C21 | dss_data3 (6) | dss_data3 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a3 | 0x1 | O | | | | | | | | |
| | | pr1_mii0_txd2 | 0x2 | O | | | | | | | | |
| | | ehrpwm0_synco | 0x3 | O | | | | | | | | |
| | | pr1_pru0_gpo3 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi3 | 0x6 | I | | | | | | | | |
| | | gpio2_9 | 0x7 | IO | | | | | | | | |
| A20 | dss_data4 (6) | dss_data4 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a4 | 0x1 | O | | | | | | | | |
| | | pr1_mii0_txd1 | 0x2 | O | | | | | | | | |
| | | eQEP2A_in | 0x3 | I | | | | | | | | |
| | | pr1_pru0_gpo4 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi4 | 0x6 | I | | | | | | | | |
| | | gpio2_10 | 0x7 | IO | | | | | | | | |
| B20 | dss_data5 (6) | dss_data5 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a5 | 0x1 | O | | | | | | | | |
| | | pr1_mii0_txd0 | 0x2 | O | | | | | | | | |
| | | eQEP2B_in | 0x3 | I | | | | | | | | |
| | | pr1_pru0_gpo5 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi5 | 0x6 | I | | | | | | | | |
| | | gpio2_11 | 0x7 | IO | | | | | | | | |
| C20 | dss_data6 (6) | dss_data6 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a6 | 0x1 | O | | | | | | | | |
| | | pr1_edio_data_in6 | 0x2 | I | | | | | | | | |
| | | eQEP2_index | 0x3 | IO | | | | | | | | |
| | | pr1_edio_data_out6 | 0x4 | O | | | | | | | | |
| | | pr1_pru0_gpo6 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi6 | 0x6 | I | | | | | | | | |
| | | gpio2_12 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E19 | dss_data7 (6) | dss_data7 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a7 | 0x1 | O | | | | | | | | |
| | | pr1_edio_data_in7 | 0x2 | I | | | | | | | | |
| | | eQEP2_strobe | 0x3 | IO | | | | | | | | |
| | | pr1_edio_data_out7 | 0x4 | O | | | | | | | | |
| | | pr1_pru0_gpo7 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi7 | 0x6 | I | | | | | | | | |
| | | gpio2_13 | 0x7 | IO | | | | | | | | |
| A19 | dss_data8 (6) | dss_data8 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a12 | 0x1 | O | | | | | | | | |
| | | ehrpwm1_tripzone_input | 0x2 | I | | | | | | | | |
| | | mcasp0_aclkx | 0x3 | IO | | | | | | | | |
| | | uart5_txd | 0x4 | O | | | | | | | | |
| | | pr1_mii0_rxd3 | 0x5 | I | | | | | | | | |
| | | uart2_ctsn | 0x6 | IO | | | | | | | | |
| | | gpio2_14 | 0x7 | IO | | | | | | | | |
| B19 | dss_data9 (6) | dss_data9 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a13 | 0x1 | O | | | | | | | | |
| | | ehrpwm0_synco | 0x2 | O | | | | | | | | |
| | | mcasp0_fsx | 0x3 | IO | | | | | | | | |
| | | uart5_rxd | 0x4 | I | | | | | | | | |
| | | pr1_mii0_rxd2 | 0x5 | I | | | | | | | | |
| | | uart2_rtsn | 0x6 | O | | | | | | | | |
| | | gpio2_15 | 0x7 | IO | | | | | | | | |
| A18 | dss_data10 (6) | dss_data10 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a14 | 0x1 | O | | | | | | | | |
| | | ehrpwm1A | 0x2 | O | | | | | | | | |
| | | mcasp0_axr0 | 0x3 | IO | | | | | | | | |
| | | pr1_mii0_rxd1 | 0x5 | I | | | | | | | | |
| | | uart3_ctsn | 0x6 | IO | | | | | | | | |
| | | gpio2_16 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B18 | dss_data11 (6) | dss_data11 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a15 | 0x1 | O | | | | | | | | |
| | | ehrpwm1B | 0x2 | O | | | | | | | | |
| | | mcasp0_ahclkr | 0x3 | IO | | | | | | | | |
| | | mcasp0_axr2 | 0x4 | IO | | | | | | | | |
| | | pr1_mii0_rxd0 | 0x5 | I | | | | | | | | |
| | | uart3_rtsn | 0x6 | O | | | | | | | | |
| | | gpio2_17 | 0x7 | IO | | | | | | | | |
| | | spi3_cs1 | 0x8 | IO | | | | | | | | |
| C19 | dss_data12 (6) | dss_data12 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a16 | 0x1 | O | | | | | | | | |
| | | eQEP1A_in | 0x2 | I | | | | | | | | |
| | | mcasp0_aclkr | 0x3 | IO | | | | | | | | |
| | | mcasp0_axr2 | 0x4 | IO | | | | | | | | |
| | | pr1_mii0_rxlink | 0x5 | I | | | | | | | | |
| | | uart4_ctsn | 0x6 | I | | | | | | | | |
| | | gpio0_8 | 0x7 | IO | | | | | | | | |
| | | spi3_sclk | 0x8 | IO | | | | | | | | |
| D19 | dss_data13 (6) | dss_data13 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a17 | 0x1 | O | | | | | | | | |
| | | eQEP1B_in | 0x2 | I | | | | | | | | |
| | | mcasp0_fsr | 0x3 | IO | | | | | | | | |
| | | mcasp0_axr3 | 0x4 | IO | | | | | | | | |
| | | pr1_mii0_rxer | 0x5 | I | | | | | | | | |
| | | uart4_rtsn | 0x6 | O | | | | | | | | |
| | | gpio0_9 | 0x7 | IO | | | | | | | | |
| | | spi3_d0 | 0x8 | IO | | | | | | | | |
| C17 | dss_data14 (6) | dss_data14 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a18 | 0x1 | O | | | | | | | | |
| | | eQEP1_index | 0x2 | IO | | | | | | | | |
| | | mcasp0_axr1 | 0x3 | IO | | | | | | | | |
| | | uart5_rxd | 0x4 | I | | | | | | | | |
| | | pr1_mii_mr0_clk | 0x5 | I | | | | | | | | |
| | | uart5_ctsn | 0x6 | I | | | | | | | | |
| | | gpio0_10 | 0x7 | IO | | | | | | | | |
| | | spi3_d1 | 0x8 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D17 | dss_data15 (6) | dss_data15 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a19 | 0x1 | O | | | | | | | | |
| | | eQEP1_strobe | 0x2 | IO | | | | | | | | |
| | | mcasp0_ahclkx | 0x3 | IO | | | | | | | | |
| | | mcasp0_axr3 | 0x4 | IO | | | | | | | | |
| | | pr1_mii0_rxdv | 0x5 | I | | | | | | | | |
| | | uart5_rtsn | 0x6 | O | | | | | | | | |
| | | gpio0_11 | 0x7 | IO | | | | | | | | |
| | | spi3_cs0 | 0x8 | IO | | | | | | | | |
| A23 | dss_hsync (7) | dss_hsync | 0x0 | O | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a9 | 0x1 | O | | | | | | | | |
| | | gpmc_a2 | 0x2 | O | | | | | | | | |
| | | pr1_edio_data_in3 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out3 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpo7 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi7 | 0x6 | I | | | | | | | | |
| | | gpio2_23 | 0x7 | IO | | | | | | | | |
| A22 | dss_pclk | dss_pclk | 0x0 | O | OFF | L | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a10 | 0x1 | O | | | | | | | | |
| | | gpmc_a3 | 0x2 | O | | | | | | | | |
| | | pr1_edio_data_in4 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out4 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpo8 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi8 | 0x6 | I | | | | | | | | |
| | | gpio2_24 | 0x7 | IO | | | | | | | | |
| B23 | dss_vsync (8) | dss_vsync | 0x0 | O | OFF | OFF | Mode7 | VDDSHV6 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a8 | 0x1 | O | | | | | | | | |
| | | gpmc_a1 | 0x2 | O | | | | | | | | |
| | | pr1_edio_data_in2 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out2 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpo6 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi6 | 0x6 | I | | | | | | | | |
| | | gpio2_22 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G24 | eCAP0_in_PWM0_out | eCAP0_in_PWM0_out | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart3_txd | 0x1 | IO | | | | | | | | |
| | | spi1_cs1 | 0x2 | IO | | | | | | | | |
| | | pr1_ecap0_ecap_capin_apwm_o | 0x3 | IO | | | | | | | | |
| | | spi1_sclk | 0x4 | IO | | | | | | | | |
| | | mmc0_sdwp | 0x5 | I | | | | | | | | |
| | | xdma_event_intr2 | 0x6 | I | | | | | | | | |
| | | gpio0_7 | 0x7 | IO | | | | | | | | |
| | | ehrpwm2B | 0x8 | O | | | | | | | | |
| | | timer1 | 0x9 | IO | | | | | | | | |
| N23 | EMU0 | EMU0 | 0x0 | IO | H | H | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio3_7 | 0x7 | IO | | | | | | | | |
| T24 | EMU1 | EMU1 | 0x0 | IO | H | H | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio3_8 | 0x7 | IO | | | | | | | | |
| G25 | EXTINTn | nNMI | 0x0 | I | OFF | H | Mode0 | VDDSHV3 | Yes | NA | PU/PD | LVCMOS |
| D25 | gpio5_8 | pr1_mii0_col | 0x5 | I | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio5_8 | 0x7 | IO | | | | | | | | |
| F24 | gpio5_9 | pr1_mii1_col | 0x5 | I | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio5_9 | 0x7 | IO | | | | | | | | |
| G20 | gpio5_10 | I2C1_SCL | 0x1 | IOD | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | pr1_mii0_crs | 0x5 | I | | | | | | | | |
| | | gpio5_10 | 0x7 | IO | | | | | | | | |
| F23 | gpio5_11 | pr1_mii1_crs | 0x5 | I | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio5_11 | 0x7 | IO | | | | | | | | |
| E25 | gpio5_12 | I2C1_SDA | 0x1 | IOD | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | pr1_mii0_rxlink | 0x5 | I | | | | | | | | |
| | | gpio5_12 | 0x7 | IO | | | | | | | | |
| E24 | gpio5_13 | pr1_mii1_rxlink | 0x5 | I | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio5_13 | 0x7 | IO | | | | | | | | |
| C3 | gpmc_a0 | gpmc_a0 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txen | 0x1 | O | | | | | | | | |
| | | rgmii2_tctl | 0x2 | O | | | | | | | | |
| | | rmii2_txen | 0x3 | O | | | | | | | | |
| | | gpmc_a16 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_txen | 0x5 | O | | | | | | | | |
| | | ehrpwm1_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio1_16 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C5 | gpmc_a1 | gpmc_a1 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxdv | 0x1 | I | | | | | | | | |
| | | rgmii2_rctl | 0x2 | I | | | | | | | | |
| | | mmc2_dat0 | 0x3 | IO | | | | | | | | |
| | | gpmc_a17 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_rxdv | 0x5 | I | | | | | | | | |
| | | ehrpwm0_synco | 0x6 | O | | | | | | | | |
| | | gpio1_17 | 0x7 | IO | | | | | | | | |
| C6 | gpmc_a2 | gpmc_a2 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txd3 | 0x1 | O | | | | | | | | |
| | | rgmii2_td3 | 0x2 | O | | | | | | | | |
| | | mmc2_dat1 | 0x3 | IO | | | | | | | | |
| | | gpmc_a18 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_txd3 | 0x5 | O | | | | | | | | |
| | | ehrpwm1A | 0x6 | O | | | | | | | | |
| | | gpio1_18 | 0x7 | IO | | | | | | | | |
| A4 | gpmc_a3 | gpmc_a3 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txd2 | 0x1 | O | | | | | | | | |
| | | rgmii2_td2 | 0x2 | O | | | | | | | | |
| | | mmc2_dat2 | 0x3 | IO | | | | | | | | |
| | | gpmc_a19 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_txd2 | 0x5 | O | | | | | | | | |
| | | ehrpwm1B | 0x6 | O | | | | | | | | |
| | | gpio1_19 | 0x7 | IO | | | | | | | | |
| D7 | gpmc_a4 | gpmc_a4 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txd1 | 0x1 | O | | | | | | | | |
| | | rgmii2_td1 | 0x2 | O | | | | | | | | |
| | | rmii2_txd1 | 0x3 | O | | | | | | | | |
| | | gpmc_a20 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_txd1 | 0x5 | O | | | | | | | | |
| | | eQEP1A_in | 0x6 | I | | | | | | | | |
| | | gpio1_20 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E7 | gpmc_a5 | gpmc_a5 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txd0 | 0x1 | O | | | | | | | | |
| | | rgmii2_td0 | 0x2 | O | | | | | | | | |
| | | rmii2_txd0 | 0x3 | O | | | | | | | | |
| | | gpmc_a21 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_txd0 | 0x5 | O | | | | | | | | |
| | | eQEP1B_in | 0x6 | I | | | | | | | | |
| | | gpio1_21 | 0x7 | IO | | | | | | | | |
| E8 | gpmc_a6 | gpmc_a6 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_txclk | 0x1 | I | | | | | | | | |
| | | rgmii2_tclk | 0x2 | O | | | | | | | | |
| | | mmc2_dat4 | 0x3 | IO | | | | | | | | |
| | | gpmc_a22 | 0x4 | O | | | | | | | | |
| | | pr1_mii_mt1_clk | 0x5 | I | | | | | | | | |
| | | eQEP1_index | 0x6 | IO | | | | | | | | |
| | | gpio1_22 | 0x7 | IO | | | | | | | | |
| F6 | gpmc_a7 | gpmc_a7 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxclk | 0x1 | I | | | | | | | | |
| | | rgmii2_rclk | 0x2 | I | | | | | | | | |
| | | mmc2_dat5 | 0x3 | IO | | | | | | | | |
| | | gpmc_a23 | 0x4 | O | | | | | | | | |
| | | pr1_mii_mr1_clk | 0x5 | I | | | | | | | | |
| | | eQEP1_strobe | 0x6 | IO | | | | | | | | |
| | | gpio1_23 | 0x7 | IO | | | | | | | | |
| F7 | gpmc_a8 | gpmc_a8 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxd3 | 0x1 | I | | | | | | | | |
| | | rgmii2_rd3 | 0x2 | I | | | | | | | | |
| | | mmc2_dat6 | 0x3 | IO | | | | | | | | |
| | | gpmc_a24 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_rxd3 | 0x5 | I | | | | | | | | |
| | | mcasp0_aclkx | 0x6 | IO | | | | | | | | |
| | | gpio1_24 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B4 | gpmc_a9 | gpmc_a9 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxd2 | 0x1 | I | | | | | | | | |
| | | rgmii2_rd2 | 0x2 | I | | | | | | | | |
| | | mmc2_dat7 | 0x3 | IO | | | | | | | | |
| | | gpmc_a25 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_rxd2 | 0x5 | I | | | | | | | | |
| | | mcasp0_fsx | 0x6 | IO | | | | | | | | |
| | | gpio1_25 | 0x7 | IO | | | | | | | | |
| | | rmii2_crs_dv | 0x8 | I | | | | | | | | |
| G8 | gpmc_a10 | gpmc_a10 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxd1 | 0x1 | I | | | | | | | | |
| | | rgmii2_rd1 | 0x2 | I | | | | | | | | |
| | | rmii2_rxd1 | 0x3 | I | | | | | | | | |
| | | gpmc_a26 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_rxd1 | 0x5 | I | | | | | | | | |
| | | mcasp0_axr0 | 0x6 | IO | | | | | | | | |
| | | gpio1_26 | 0x7 | IO | | | | | | | | |
| D8 | gpmc_a11 | gpmc_a11 | 0x0 | O | L | L | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxd0 | 0x1 | I | | | | | | | | |
| | | rgmii2_rd0 | 0x2 | I | | | | | | | | |
| | | rmii2_rxd0 | 0x3 | I | | | | | | | | |
| | | gpmc_a27 | 0x4 | O | | | | | | | | |
| | | pr1_mii1_rxd0 | 0x5 | I | | | | | | | | |
| | | mcasp0_axr1 | 0x6 | IO | | | | | | | | |
| | | gpio1_27 | 0x7 | IO | | | | | | | | |
| B5 | gpmc_ad0 | gpmc_ad0 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat0 | 0x1 | IO | | | | | | | | |
| | | gpio1_0 | 0x7 | IO | | | | | | | | |
| A5 | gpmc_ad1 | gpmc_ad1 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat1 | 0x1 | IO | | | | | | | | |
| | | gpio1_1 | 0x7 | IO | | | | | | | | |
| B6 | gpmc_ad2 | gpmc_ad2 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat2 | 0x1 | IO | | | | | | | | |
| | | gpio1_2 | 0x7 | IO | | | | | | | | |
| A6 | gpmc_ad3 | gpmc_ad3 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat3 | 0x1 | IO | | | | | | | | |
| | | gpio1_3 | 0x7 | IO | | | | | | | | |

## Table 4-10. Pin Attributes (ZDN Package) (continued)

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | gpmc_ad4 | gpmc_ad4 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat4 | 0x1 | IO | | | | | | | | |
| | | gpio1_4 | 0x7 | IO | | | | | | | | |
| A7 | gpmc_ad5 | gpmc_ad5 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat5 | 0x1 | IO | | | | | | | | |
| | | gpio1_5 | 0x7 | IO | | | | | | | | |
| C8 | gpmc_ad6 | gpmc_ad6 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat6 | 0x1 | IO | | | | | | | | |
| | | gpio1_6 | 0x7 | IO | | | | | | | | |
| B8 | gpmc_ad7 | gpmc_ad7 | 0x0 | IO | L | L | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_dat7 | 0x1 | IO | | | | | | | | |
| | | gpio1_7 | 0x7 | IO | | | | | | | | |
| B10 | gpmc_ad8 | gpmc_ad8 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data23 | 0x1 | O | | | | | | | | |
| | | mmc1_dat0 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat4 | 0x3 | IO | | | | | | | | |
| | | ehrpwm2A | 0x4 | O | | | | | | | | |
| | | pr1_mii_mt0_clk | 0x5 | I | | | | | | | | |
| | | spi3_sclk | 0x6 | IO | | | | | | | | |
| | | gpio0_22 | 0x7 | IO | | | | | | | | |
| | | spi3_cs1 | 0x8 | IO | | | | | | | | |
| | | gpio5_26 | 0x9 | IO | | | | | | | | |
| A10 | gpmc_ad9 | gpmc_ad9 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data22 | 0x1 | O | | | | | | | | |
| | | mmc1_dat1 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat5 | 0x3 | IO | | | | | | | | |
| | | ehrpwm2B | 0x4 | O | | | | | | | | |
| | | pr1_mii0_col | 0x5 | I | | | | | | | | |
| | | spi3_d0 | 0x6 | IO | | | | | | | | |
| | | gpio0_23 | 0x7 | IO | | | | | | | | |
| | | gpio5_25 | 0x9 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F11 | gpmc_ad10 | gpmc_ad10 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data21 | 0x1 | O | | | | | | | | |
| | | mmc1_dat2 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat6 | 0x3 | IO | | | | | | | | |
| | | ehrpwm2_tripzone_input | 0x4 | I | | | | | | | | |
| | | pr1_mii0_txen | 0x5 | O | | | | | | | | |
| | | spi3_d1 | 0x6 | IO | | | | | | | | |
| | | gpio0_26 | 0x7 | IO | | | | | | | | |
| | | gpio5_24 | 0x9 | IO | | | | | | | | |
| D11 | gpmc_ad11 | gpmc_ad11 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data20 | 0x1 | O | | | | | | | | |
| | | mmc1_dat3 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat7 | 0x3 | IO | | | | | | | | |
| | | ehrpwm0_synco | 0x4 | O | | | | | | | | |
| | | pr1_mii0_txd3 | 0x5 | O | | | | | | | | |
| | | spi3_cs0 | 0x6 | IO | | | | | | | | |
| | | gpio0_27 | 0x7 | IO | | | | | | | | |
| | | gpio5_23 | 0x9 | IO | | | | | | | | |
| E11 | gpmc_ad12 | gpmc_ad12 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data19 | 0x1 | O | | | | | | | | |
| | | mmc1_dat4 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat0 | 0x3 | IO | | | | | | | | |
| | | eQEP2A_in | 0x4 | I | | | | | | | | |
| | | pr1_mii0_txd2 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi10 | 0x6 | I | | | | | | | | |
| | | gpio1_12 | 0x7 | IO | | | | | | | | |
| | | mcasp0_aclkx | 0x8 | IO | | | | | | | | |
| | | pr1_pru0_gpo10 | 0x9 | O | | | | | | | | |
| C11 | gpmc_ad13 | gpmc_ad13 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data18 | 0x1 | O | | | | | | | | |
| | | mmc1_dat5 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat1 | 0x3 | IO | | | | | | | | |
| | | eQEP2B_in | 0x4 | I | | | | | | | | |
| | | pr1_mii0_txd1 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi11 | 0x6 | I | | | | | | | | |
| | | gpio1_13 | 0x7 | IO | | | | | | | | |
| | | mcasp0_fsx | 0x8 | IO | | | | | | | | |
| | | pr1_pru0_gpo11 | 0x9 | O | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B11 | gpmc_ad14 | gpmc_ad14 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data17 | 0x1 | O | | | | | | | | |
| | | mmc1_dat6 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat2 | 0x3 | IO | | | | | | | | |
| | | eQEP2_index | 0x4 | IO | | | | | | | | |
| | | pr1_mii0_txd0 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi16 | 0x6 | I | | | | | | | | |
| | | gpio1_14 | 0x7 | IO | | | | | | | | |
| | | mcasp0_axr0 | 0x8 | IO | | | | | | | | |
| A11 | gpmc_ad15 | gpmc_ad15 | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | dss_data16 | 0x1 | O | | | | | | | | |
| | | mmc1_dat7 | 0x2 | IO | | | | | | | | |
| | | mmc2_dat3 | 0x3 | IO | | | | | | | | |
| | | eQEP2_strobe | 0x4 | IO | | | | | | | | |
| | | pr1_ecap0_ecap_capin_apwm_o | 0x5 | IO | | | | | | | | |
| | | gpio1_15 | 0x7 | IO | | | | | | | | |
| | | mcasp0_axr1 | 0x8 | IO | | | | | | | | |
| | | spi3_cs1 | 0x9 | IO | | | | | | | | |
| A9 | gpmc_advn_ale | gpmc_advn_ale | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | spi0_cs3 | 0x1 | IO | | | | | | | | |
| | | timer4 | 0x2 | IO | | | | | | | | |
| | | qspi_d0 | 0x3 | IO | | | | | | | | |
| | | gpio2_2 | 0x7 | IO | | | | | | | | |
| C10 | gpmc_be0n_cle | gpmc_be0n_cle | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | spi1_cs3 | 0x1 | IO | | | | | | | | |
| | | timer5 | 0x2 | IO | | | | | | | | |
| | | qspi_d3 | 0x3 | I | | | | | | | | |
| | | pr1_mii1_rxlink | 0x4 | I | | | | | | | | |
| | | gpmc_a5 | 0x5 | O | | | | | | | | |
| | | spi3_cs1 | 0x6 | IO | | | | | | | | |
| | | gpio2_5 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | gpmc_be1n | gpmc_be1n | 0x0 | O | H | H | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_col | 0x1 | I | | | | | | | | |
| | | gpmc_csn6 | 0x2 | O | | | | | | | | |
| | | mmc2_dat3 | 0x3 | IO | | | | | | | | |
| | | gpmc_dir | 0x4 | O | | | | | | | | |
| | | pr1_mii1_col | 0x5 | I | | | | | | | | |
| | | mcasp0_aclkr | 0x6 | IO | | | | | | | | |
| | | gpio1_28 | 0x7 | IO | | | | | | | | |
| A12 | gpmc_clk | gpmc_clk | 0x0 | IO | L | L | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_wait1 | 0x2 | I | | | | | | | | |
| | | mmc2_clk | 0x3 | IO | | | | | | | | |
| | | pr1_mii1_crs | 0x4 | I | | | | | | | | |
| | | pr1_mdio_mdclk | 0x5 | O | | | | | | | | |
| | | mcasp0_fsr | 0x6 | IO | | | | | | | | |
| | | gpio2_1 | 0x7 | IO | | | | | | | | |
| | | gpio0_4 | 0x9 | IO | | | | | | | | |
| A8 | gpmc_csn0 | gpmc_csn0 | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | qspi_csn | 0x3 | O | | | | | | | | |
| | | gpio1_29 | 0x7 | IO | | | | | | | | |
| B9 | gpmc_csn1 | gpmc_csn1 | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_clk | 0x1 | IO | | | | | | | | |
| | | mmc1_clk | 0x2 | IO | | | | | | | | |
| | | pr1_edio_data_in6 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out6 | 0x4 | O | | | | | | | | |
| | | pr1_pru0_gpo8 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi8 | 0x6 | I | | | | | | | | |
| | | gpio1_30 | 0x7 | IO | | | | | | | | |
| F10 | gpmc_csn2 | gpmc_csn2 | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_be1n | 0x1 | O | | | | | | | | |
| | | mmc1_cmd | 0x2 | IO | | | | | | | | |
| | | pr1_edio_data_in7 | 0x3 | I | | | | | | | | |
| | | pr1_edio_data_out7 | 0x4 | O | | | | | | | | |
| | | pr1_pru0_gpo9 | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi9 | 0x6 | I | | | | | | | | |
| | | gpio1_31 | 0x7 | IO | | | | | | | | |
| | | gmii2_crs | 0x8 | I | | | | | | | | |
| | | rmii2_crs_dv | 0x9 | I | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B12 | gpmc_csn3 | gpmc_csn3 | 0x0 | O | H | H | Mode7 | VDDSHV9 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_wait0 | 0x1 | I | | | | | | | | |
| | | qspi_clk | 0x2 | IO | | | | | | | | |
| | | mmc2_cmd | 0x3 | IO | | | | | | | | |
| | | pr1_mii0_crs | 0x4 | I | | | | | | | | |
| | | pr1_mdio_data | 0x5 | IO | | | | | | | | |
| | | EMU4 | 0x6 | IO | | | | | | | | |
| | | gpio2_0 | 0x7 | IO | | | | | | | | |
| | | gmii2_crs | 0x8 | I | | | | | | | | |
| | | rmii2_crs_dv | 0x9 | I | | | | | | | | |
| E10 | gpmc_oen_ren | gpmc_oen_ren | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | spi0_cs2 | 0x1 | IO | | | | | | | | |
| | | timer7 | 0x2 | IO | | | | | | | | |
| | | qspi_d1 | 0x3 | I | | | | | | | | |
| | | gpio2_3 | 0x7 | IO | | | | | | | | |
| A2 | gpmc_wait0 | gpmc_wait0 | 0x0 | I | H | H | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_crs | 0x1 | I | | | | | | | | |
| | | gpmc_csn4 | 0x2 | O | | | | | | | | |
| | | rmii2_crs_dv | 0x3 | I | | | | | | | | |
| | | mmc1_sdcd | 0x4 | I | | | | | | | | |
| | | pr1_mii1_crs | 0x5 | I | | | | | | | | |
| | | uart4_rxd | 0x6 | I | | | | | | | | |
| | | gpio0_30 | 0x7 | IO | | | | | | | | |
| | | gpio5_30 | 0x9 | IO | | | | | | | | |
| D10 | gpmc_wen | gpmc_wen | 0x0 | O | H | H | Mode7 | VDDSHV10 | Yes | 6 | PU/PD | LVCMOS |
| | | spi1_cs2 | 0x1 | IO | | | | | | | | |
| | | timer6 | 0x2 | IO | | | | | | | | |
| | | qspi_d2 | 0x3 | I | | | | | | | | |
| | | gpio2_4 | 0x7 | IO | | | | | | | | |
| B3 | gpmc_wpn | gpmc_wpn | 0x0 | O | H | H | Mode7 | VDDSHV11 | Yes | 6 | PU/PD | LVCMOS |
| | | gmii2_rxer | 0x1 | I | | | | | | | | |
| | | gpmc_csn5 | 0x2 | O | | | | | | | | |
| | | rmii2_rxer | 0x3 | I | | | | | | | | |
| | | mmc2_sdcd | 0x4 | I | | | | | | | | |
| | | pr1_mii1_rxer | 0x5 | I | | | | | | | | |
| | | uart4_txd | 0x6 | O | | | | | | | | |
| | | gpio0_31 | 0x7 | IO | | | | | | | | |
| | | gpio5_31 | 0x9 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y22 | I2C0_SCL | I2C0_SCL | 0x0 | IOD | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | timer7 | 0x1 | IO | | | | | | | | |
| | | uart2_rtsn | 0x2 | O | | | | | | | | |
| | | eCAP1_in_PWM1_out | 0x3 | IO | | | | | | | | |
| | | gpio3_6 | 0x7 | IO | | | | | | | | |
| AB24 | I2C0_SDA | I2C0_SDA | 0x0 | IOD | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | timer4 | 0x1 | IO | | | | | | | | |
| | | uart2_ctsn | 0x2 | IO | | | | | | | | |
| | | eCAP2_in_PWM2_out | 0x3 | IO | | | | | | | | |
| | | gpio3_5 | 0x7 | IO | | | | | | | | |
| L23 | mcasp0_aclkr | mcasp0_aclkr | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | eQEP0A_in | 0x1 | I | | | | | | | | |
| | | mcasp0_axr2 | 0x2 | IO | | | | | | | | |
| | | mcasp1_aclkx | 0x3 | IO | | | | | | | | |
| | | mmc0_sdwp | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo4 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi4 | 0x6 | I | | | | | | | | |
| | | gpio3_18 | 0x7 | IO | | | | | | | | |
| | | gpio0_18 | 0x9 | IO | | | | | | | | |
| N24 | mcasp0_aclkx | mcasp0_aclkx | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0A | 0x1 | O | | | | | | | | |
| | | spi0_cs3 | 0x2 | IO | | | | | | | | |
| | | spi1_sclk | 0x3 | IO | | | | | | | | |
| | | mmc0_sdcd | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo0 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi0 | 0x6 | I | | | | | | | | |
| | | gpio3_14 | 0x7 | IO | | | | | | | | |
| M24 | mcasp0_ahclkr | mcasp0_ahclkr | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0_synci | 0x1 | I | | | | | | | | |
| | | mcasp0_axr2 | 0x2 | IO | | | | | | | | |
| | | spi1_cs0 | 0x3 | IO | | | | | | | | |
| | | eCAP2_in_PWM2_out | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpo3 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi3 | 0x6 | I | | | | | | | | |
| | | gpio3_17 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L24 | mcasp0_ahclkx | mcasp0_ahclkx | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | eQEP0_strobe | 0x1 | IO | | | | | | | | |
| | | mcasp0_axr3 | 0x2 | IO | | | | | | | | |
| | | mcasp1_axr1 | 0x3 | IO | | | | | | | | |
| | | EMU4 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpo7 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi7 | 0x6 | I | | | | | | | | |
| | | gpio3_21 | 0x7 | IO | | | | | | | | |
| | | gpio0_3 | 0x9 | IO | | | | | | | | |
| K23 | mcasp0_fsr | mcasp0_fsr | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | eQEP0B_in | 0x1 | I | | | | | | | | |
| | | mcasp0_axr3 | 0x2 | IO | | | | | | | | |
| | | mcasp1_fsx | 0x3 | IO | | | | | | | | |
| | | EMU2 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpo5 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi5 | 0x6 | I | | | | | | | | |
| | | gpio3_19 | 0x7 | IO | | | | | | | | |
| | | gpio0_19 | 0x9 | IO | | | | | | | | |
| N22 | mcasp0_fsx | mcasp0_fsx | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0B | 0x1 | O | | | | | | | | |
| | | spi1_cs2 | 0x2 | IO | | | | | | | | |
| | | spi1_d0 | 0x3 | IO | | | | | | | | |
| | | mmc1_sdcd | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo1 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi1 | 0x6 | I | | | | | | | | |
| | | gpio3_15 | 0x7 | IO | | | | | | | | |
| H23 | mcasp0_axr0 | mcasp0_axr0 | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0_tripzone_input | 0x1 | I | | | | | | | | |
| | | spi1_cs3 | 0x2 | IO | | | | | | | | |
| | | spi1_d1 | 0x3 | IO | | | | | | | | |
| | | mmc2_sdcd | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo2 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi2 | 0x6 | I | | | | | | | | |
| | | gpio3_16 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M25 | mcasp0_axr1 | mcasp0_axr1 | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | eQEP0_index | 0x1 | IO | | | | | | | | |
| | | mcasp1_axr0 | 0x3 | IO | | | | | | | | |
| | | EMU3 | 0x4 | IO | | | | | | | | |
| | | pr0_pru0_gpo6 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi6 | 0x6 | I | | | | | | | | |
| | | gpio3_20 | 0x7 | IO | | | | | | | | |
| | | gpio0_2 | 0x9 | IO | | | | | | | | |
| B17 | mdio_clk | mdio_clk | 0x0 | O | H | H | Mode7 | VDDSHV7 | Yes | 6 | PU/PD | LVCMOS |
| | | timer5 | 0x1 | IO | | | | | | | | |
| | | uart5_txd | 0x2 | O | | | | | | | | |
| | | uart3_rtsn | 0x3 | O | | | | | | | | |
| | | mmc0_sdwp | 0x4 | I | | | | | | | | |
| | | mmc1_clk | 0x5 | IO | | | | | | | | |
| | | mmc2_clk | 0x6 | IO | | | | | | | | |
| | | gpio0_1 | 0x7 | IO | | | | | | | | |
| | | pr1_mdio_mdclk | 0x8 | O | | | | | | | | |
| A17 | mdio_data | mdio_data | 0x0 | IO | H | H | Mode7 | VDDSHV7 | Yes | 6 | PU/PD | LVCMOS |
| | | timer6 | 0x1 | IO | | | | | | | | |
| | | uart5_rxd | 0x2 | I | | | | | | | | |
| | | uart3_ctsn | 0x3 | IO | | | | | | | | |
| | | mmc0_sdcd | 0x4 | I | | | | | | | | |
| | | mmc1_cmd | 0x5 | IO | | | | | | | | |
| | | mmc2_cmd | 0x6 | IO | | | | | | | | |
| | | gpio0_0 | 0x7 | IO | | | | | | | | |
| | | pr1_mdio_data | 0x8 | IO | | | | | | | | |
| D16 | mii1_col | gmii1_col | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii2_refclk | 0x1 | IO | | | | | | | | |
| | | spi1_sclk | 0x2 | IO | | | | | | | | |
| | | uart5_rxd | 0x3 | I | | | | | | | | |
| | | mcasp1_axr2 | 0x4 | IO | | | | | | | | |
| | | mmc2_dat3 | 0x5 | IO | | | | | | | | |
| | | mcasp0_axr2 | 0x6 | IO | | | | | | | | |
| | | gpio3_0 | 0x7 | IO | | | | | | | | |
| | | gpio0_0 | 0x9 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B14 | mii1_crs | gmii1_crs | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_crs_dv | 0x1 | I | | | | | | | | |
| | | spi1_d0 | 0x2 | IO | | | | | | | | |
| | | I2C1_SDA | 0x3 | IOD | | | | | | | | |
| | | mcasp1_aclkx | 0x4 | IO | | | | | | | | |
| | | uart5_ctsn | 0x5 | I | | | | | | | | |
| | | uart2_rxd | 0x6 | IO | | | | | | | | |
| | | gpio3_1 | 0x7 | IO | | | | | | | | |
| D13 | mii1_rx_clk | gmii1_rxclk | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | uart2_txd | 0x1 | IO | | | | | | | | |
| | | rgmii1_rclk | 0x2 | I | | | | | | | | |
| | | mmc0_dat6 | 0x3 | IO | | | | | | | | |
| | | mmc1_dat1 | 0x4 | IO | | | | | | | | |
| | | uart1_dsrn | 0x5 | I | | | | | | | | |
| | | mcasp0_fsx | 0x6 | IO | | | | | | | | |
| | | gpio3_10 | 0x7 | IO | | | | | | | | |
| | | gpio0_9 | 0x9 | IO | | | | | | | | |
| A15 | mii1_rx_dv | gmii1_rxdv | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rgmii1_rctl | 0x2 | I | | | | | | | | |
| | | uart5_txd | 0x3 | O | | | | | | | | |
| | | mcasp1_aclkx | 0x4 | IO | | | | | | | | |
| | | mmc2_dat0 | 0x5 | IO | | | | | | | | |
| | | mcasp0_aclkr | 0x6 | IO | | | | | | | | |
| | | gpio3_4 | 0x7 | IO | | | | | | | | |
| | | gpio0_1 | 0x9 | IO | | | | | | | | |
| B13 | mii1_rx_er | gmii1_rxer | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_rxer | 0x1 | I | | | | | | | | |
| | | spi1_d1 | 0x2 | IO | | | | | | | | |
| | | I2C1_SCL | 0x3 | IOD | | | | | | | | |
| | | mcasp1_fsx | 0x4 | IO | | | | | | | | |
| | | uart5_rtsn | 0x5 | O | | | | | | | | |
| | | uart2_txd | 0x6 | IO | | | | | | | | |
| | | gpio3_2 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D14 | mii1_tx_clk | gmii1_txclk | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | uart2_rxd | 0x1 | IO | | | | | | | | |
| | | rgmii1_tclk | 0x2 | O | | | | | | | | |
| | | mmc0_dat7 | 0x3 | IO | | | | | | | | |
| | | mmc1_dat0 | 0x4 | IO | | | | | | | | |
| | | uart1_dcdn | 0x5 | I | | | | | | | | |
| | | mcasp0_aclkx | 0x6 | IO | | | | | | | | |
| | | gpio3_9 | 0x7 | IO | | | | | | | | |
| | | gpio0_8 | 0x9 | IO | | | | | | | | |
| A13 | mii1_tx_en | gmii1_txen | 0x0 | O | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_txen | 0x1 | O | | | | | | | | |
| | | rgmii1_tctl | 0x2 | O | | | | | | | | |
| | | timer4 | 0x3 | IO | | | | | | | | |
| | | mcasp1_axr0 | 0x4 | IO | | | | | | | | |
| | | eQEP0_index | 0x5 | IO | | | | | | | | |
| | | mmc2_cmd | 0x6 | IO | | | | | | | | |
| | | gpio3_3 | 0x7 | IO | | | | | | | | |
| F17 | mii1_rxd0 | gmii1_rxd0 | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_rxd0 | 0x1 | I | | | | | | | | |
| | | rgmii1_rd0 | 0x2 | I | | | | | | | | |
| | | mcasp1_ahclkx | 0x3 | IO | | | | | | | | |
| | | mcasp1_ahclkr | 0x4 | IO | | | | | | | | |
| | | mcasp1_aclkr | 0x5 | IO | | | | | | | | |
| | | mcasp0_axr3 | 0x6 | IO | | | | | | | | |
| | | gpio2_21 | 0x7 | IO | | | | | | | | |
| B16 | mii1_rxd1 | gmii1_rxd1 | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_rxd1 | 0x1 | I | | | | | | | | |
| | | rgmii1_rd1 | 0x2 | I | | | | | | | | |
| | | mcasp1_axr3 | 0x3 | IO | | | | | | | | |
| | | mcasp1_fsr | 0x4 | IO | | | | | | | | |
| | | eQEP0_strobe | 0x5 | IO | | | | | | | | |
| | | mmc2_clk | 0x6 | IO | | | | | | | | |
| | | gpio2_20 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E16 | mii1_rxd2 | gmii1_rxd2 | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | uart3_txd | 0x1 | IO | | | | | | | | |
| | | rgmii1_rd2 | 0x2 | I | | | | | | | | |
| | | mmc0_dat4 | 0x3 | IO | | | | | | | | |
| | | mmc1_dat3 | 0x4 | IO | | | | | | | | |
| | | uart1_rin | 0x5 | I | | | | | | | | |
| | | mcasp0_axr1 | 0x6 | IO | | | | | | | | |
| | | gpio2_19 | 0x7 | IO | | | | | | | | |
| | | gpio0_11 | 0x9 | IO | | | | | | | | |
| C14 | mii1_rxd3 | gmii1_rxd3 | 0x0 | I | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | uart3_rxd | 0x1 | IO | | | | | | | | |
| | | rgmii1_rd3 | 0x2 | I | | | | | | | | |
| | | mmc0_dat5 | 0x3 | IO | | | | | | | | |
| | | mmc1_dat2 | 0x4 | IO | | | | | | | | |
| | | uart1_dtrn | 0x5 | O | | | | | | | | |
| | | mcasp0_axr0 | 0x6 | IO | | | | | | | | |
| | | gpio2_18 | 0x7 | IO | | | | | | | | |
| | | gpio0_10 | 0x9 | IO | | | | | | | | |
| B15 | mii1_txd0 | gmii1_txd0 | 0x0 | O | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_txd0 | 0x1 | O | | | | | | | | |
| | | rgmii1_td0 | 0x2 | O | | | | | | | | |
| | | mcasp1_axr2 | 0x3 | IO | | | | | | | | |
| | | mcasp1_aclkr | 0x4 | IO | | | | | | | | |
| | | eQEP0B_in | 0x5 | I | | | | | | | | |
| | | mmc1_clk | 0x6 | IO | | | | | | | | |
| | | gpio0_28 | 0x7 | IO | | | | | | | | |
| A14 | mii1_txd1 | gmii1_txd1 | 0x0 | O | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | rmii1_txd1 | 0x1 | O | | | | | | | | |
| | | rgmii1_td1 | 0x2 | O | | | | | | | | |
| | | mcasp1_fsr | 0x3 | IO | | | | | | | | |
| | | mcasp1_axr1 | 0x4 | IO | | | | | | | | |
| | | eQEP0A_in | 0x5 | I | | | | | | | | |
| | | mmc1_cmd | 0x6 | IO | | | | | | | | |
| | | gpio0_21 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C13 | mii1_txd2 | gmii1_txd2 | 0x0 | O | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | dcan0_rx | 0x1 | I | | | | | | | | |
| | | rgmii1_td2 | 0x2 | O | | | | | | | | |
| | | uart4_txd | 0x3 | O | | | | | | | | |
| | | mcasp1_axr0 | 0x4 | IO | | | | | | | | |
| | | mmc2_dat2 | 0x5 | IO | | | | | | | | |
| | | mcasp0_ahclkx | 0x6 | IO | | | | | | | | |
| | | gpio0_17 | 0x7 | IO | | | | | | | | |
| | | gpio3_12 | 0x9 | IO | | | | | | | | |
| C16 | mii1_txd3 | gmii1_txd3 | 0x0 | O | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | dcan0_tx | 0x1 | O | | | | | | | | |
| | | rgmii1_td3 | 0x2 | O | | | | | | | | |
| | | uart4_rxd | 0x3 | I | | | | | | | | |
| | | mcasp1_fsx | 0x4 | IO | | | | | | | | |
| | | mmc2_dat1 | 0x5 | IO | | | | | | | | |
| | | mcasp0_fsr | 0x6 | IO | | | | | | | | |
| | | gpio0_16 | 0x7 | IO | | | | | | | | |
| | | gpio3_11 | 0x9 | IO | | | | | | | | |
| D1 | mmc0_clk | mmc0_clk | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a24 | 0x1 | O | | | | | | | | |
| | | uart3_ctsn | 0x2 | IO | | | | | | | | |
| | | uart2_rxd | 0x3 | IO | | | | | | | | |
| | | dcan1_tx | 0x4 | O | | | | | | | | |
| | | pr0_pru0_gpo12 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi12 | 0x6 | I | | | | | | | | |
| | | gpio2_30 | 0x7 | IO | | | | | | | | |
| D2 | mmc0_cmd | mmc0_cmd | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a25 | 0x1 | O | | | | | | | | |
| | | uart3_rtsn | 0x2 | O | | | | | | | | |
| | | uart2_txd | 0x3 | IO | | | | | | | | |
| | | dcan1_rx | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo13 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi13 | 0x6 | I | | | | | | | | |
| | | gpio2_31 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1 | mmc0_dat0 | mmc0_dat0 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a23 | 0x1 | O | | | | | | | | |
| | | uart5_rtsn | 0x2 | O | | | | | | | | |
| | | uart3_txd | 0x3 | IO | | | | | | | | |
| | | uart1_rin | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo11 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi11 | 0x6 | I | | | | | | | | |
| | | gpio2_29 | 0x7 | IO | | | | | | | | |
| C2 | mmc0_dat1 | mmc0_dat1 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a22 | 0x1 | O | | | | | | | | |
| | | uart5_ctsn | 0x2 | I | | | | | | | | |
| | | uart3_rxd | 0x3 | IO | | | | | | | | |
| | | uart1_dtrn | 0x4 | O | | | | | | | | |
| | | pr0_pru0_gpo10 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi10 | 0x6 | I | | | | | | | | |
| | | gpio2_28 | 0x7 | IO | | | | | | | | |
| B2 | mmc0_dat2 | mmc0_dat2 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a21 | 0x1 | O | | | | | | | | |
| | | uart4_rtsn | 0x2 | O | | | | | | | | |
| | | timer6 | 0x3 | IO | | | | | | | | |
| | | uart1_dsrn | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo9 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi9 | 0x6 | I | | | | | | | | |
| | | gpio2_27 | 0x7 | IO | | | | | | | | |
| B1 | mmc0_dat3 | mmc0_dat3 | 0x0 | IO | OFF | OFF | Mode7 | VDDSHV1 | Yes | 6 | PU/PD | LVCMOS |
| | | gpmc_a20 | 0x1 | O | | | | | | | | |
| | | uart4_ctsn | 0x2 | I | | | | | | | | |
| | | timer5 | 0x3 | IO | | | | | | | | |
| | | uart1_dcdn | 0x4 | I | | | | | | | | |
| | | pr0_pru0_gpo8 | 0x5 | O | | | | | | | | |
| | | pr0_pru0_gpi8 | 0x6 | I | | | | | | | | |
| | | gpio2_26 | 0x7 | IO | | | | | | | | |
| Y25 | nTRST | nTRST | 0x0 | I | L | L | Mode0 | VDDSHV3 | Yes | NA | PU/PD | LVCMOS |
| Y23 | PWRONRSTn | porz | 0x0 | I | Z | Z | Mode0 | VDDSHV3 (18) | Yes | NA | NA | LVCMOS |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AA10, AA7, AA9, AB10, AB6, AB7, AB9, AC10, AC12, AC5, AC6, AC7, AC9, AD1, AD10, AD11, AD2, AD7, AE11, AE12, AE9, H19, H21, W10, Y10, Y6, Y7 | Reserved | Reserved (9) | NA | NA | NA | NA | NA | NA | NA | NA | NA | NA |
| A16 | rmii1_ref_clk | rmii1_refclk | 0x0 | IO | L | L | Mode7 | VDDSHV8 | Yes | 6 | PU/PD | LVCMOS |
| | | xdma_event_intr2 | 0x1 | I | | | | | | | | |
| | | spi1_cs0 | 0x2 | IO | | | | | | | | |
| | | uart5_txd | 0x3 | O | | | | | | | | |
| | | mcasp1_axr3 | 0x4 | IO | | | | | | | | |
| | | mmc0_pow | 0x5 | O | | | | | | | | |
| | | mcasp1_ahclkx | 0x6 | IO | | | | | | | | |
| | | gpio0_29 | 0x7 | IO | | | | | | | | |
| AE2 | RTC_KALDO_ENn | RTC_KALDO_ENn | 0x0 | I | Z | Z | Mode0 | VDDS_RTC | NA | NA | NA | Analog |
| AD6 | RTC_PMIC_EN | RTC_PMIC_EN | 0x0 | O | H | 1 | Mode0 | VDDS_RTC | NA | 6 | NA | LVCMOS |
| AE6 | RTC_PWRONRSTn | RTC_PORz | 0x0 | I | Z | Z | Mode0 | VDDS_RTC | Yes | NA | NA | LVCMOS |
| AE3 | RTC_WAKEUP | RTC_WAKEUP | 0x0 | I | L | Z | Mode0 | VDDS_RTC | Yes | NA | NA | LVCMOS |
| AE5 | RTC_XTALIN | OSC1_IN | 0x0 | I | H | H | Mode0 | VDDS_RTC | Yes | NA | PU (2) | LVCMOS |
| AE4 | RTC_XTALOUT | OSC1_OUT | 0x0 | O | Z | Z (29) | Mode0 | VDDS_RTC | NA | NA (19) | NA | LVCMOS |
| P23 | spi0_sclk | spi0_sclk | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart2_rxd | 0x1 | IO | | | | | | | | |
| | | I2C2_SDA | 0x2 | IOD | | | | | | | | |
| | | ehrpwm0A | 0x3 | O | | | | | | | | |
| | | pr1_uart0_cts_n | 0x4 | I | | | | | | | | |
| | | pr0_uart0_cts_n | 0x5 | I | | | | | | | | |
| | | EMU2 | 0x6 | IO | | | | | | | | |
| | | gpio0_2 | 0x7 | IO | | | | | | | | |
| N20 | spi2_sclk | spi2_sclk | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | I2C1_SCL | 0x1 | IOD | | | | | | | | |
| | | ehrpwm4_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio3_24 | 0x7 | IO | | | | | | | | |
| | | gpio0_22 | 0x9 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P25 | spi4_sclk | spi4_sclk | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0_synci | 0x6 | I | | | | | | | | |
| | | gpio5_4 | 0x7 | IO | | | | | | | | |
| T20 | spi0_cs0 | spi0_cs0 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc2_sdwp | 0x1 | I | | | | | | | | |
| | | I2C1_SCL | 0x2 | IOD | | | | | | | | |
| | | ehrpwm0_synci | 0x3 | I | | | | | | | | |
| | | pr1_uart0_txd | 0x4 | O | | | | | | | | |
| | | pr0_uart0_txd | 0x5 | O | | | | | | | | |
| | | pr1_edio_data_out1 | 0x6 | O | | | | | | | | |
| | | gpio0_5 | 0x7 | IO | | | | | | | | |
| | | ehrpwm1B | 0x8 | O | | | | | | | | |
| R25 | spi0_cs1 | spi0_cs1 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart3_rxd | 0x1 | IO | | | | | | | | |
| | | eCAP1_in_PWM1_out | 0x2 | IO | | | | | | | | |
| | | mmc0_pow | 0x3 | O | | | | | | | | |
| | | xdma_event_intr2 | 0x4 | I | | | | | | | | |
| | | mmc0_sdcd | 0x5 | I | | | | | | | | |
| | | EMU4 | 0x6 | IO | | | | | | | | |
| | | gpio0_6 | 0x7 | IO | | | | | | | | |
| | | ehrpwm2A | 0x8 | O | | | | | | | | |
| | | timer0 | 0x9 | IO | | | | | | | | |
| T22 | spi0_d0 | spi0_d0 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart2_txd | 0x1 | IO | | | | | | | | |
| | | I2C2_SCL | 0x2 | IOD | | | | | | | | |
| | | ehrpwm0B | 0x3 | O | | | | | | | | |
| | | pr1_uart0_rts_n | 0x4 | O | | | | | | | | |
| | | pr0_uart0_rts_n | 0x5 | O | | | | | | | | |
| | | EMU3 | 0x6 | IO | | | | | | | | |
| | | gpio0_3 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T21 | spi0_d1 | spi0_d1 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_sdwp | 0x1 | I | | | | | | | | |
| | | I2C1_SDA | 0x2 | IOD | | | | | | | | |
| | | ehrpwm0_tripzone_input | 0x3 | I | | | | | | | | |
| | | pr1_uart0_rxd | 0x4 | I | | | | | | | | |
| | | pr0_uart0_rxd | 0x5 | I | | | | | | | | |
| | | pr1_edio_data_out0 | 0x6 | O | | | | | | | | |
| | | gpio0_4 | 0x7 | IO | | | | | | | | |
| | | ehrpwm1A | 0x8 | O | | | | | | | | |
| T23 | spi2_cs0 | spi2_cs0 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | I2C1_SDA | 0x1 | IOD | | | | | | | | |
| | | ehrpwm2_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio3_25 | 0x7 | IO | | | | | | | | |
| | | gpio0_23 | 0x9 | IO | | | | | | | | |
| P22 | spi2_d0 | spi2_d0 | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm5_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio3_22 | 0x7 | IO | | | | | | | | |
| | | gpio0_20 | 0x9 | IO | | | | | | | | |
| P20 | spi2_d1 | spi2_d1 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm1_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio3_23 | 0x7 | IO | | | | | | | | |
| | | gpio0_21 | 0x9 | IO | | | | | | | | |
| N25 | spi4_cs0 | spi4_cs0 | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm3_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio5_7 | 0x7 | IO | | | | | | | | |
| R24 | spi4_d0 | spi4_d0 | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm3_synci | 0x6 | I | | | | | | | | |
| | | gpio5_5 | 0x7 | IO | | | | | | | | |
| P24 | spi4_d1 | spi4_d1 | 0x0 | IO | OFF | L | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | ehrpwm0_tripzone_input | 0x6 | I | | | | | | | | |
| | | gpio5_6 | 0x7 | IO | | | | | | | | |
| AA25 | TCK | TCK | 0x0 | I | H | H | Mode0 | VDDSHV3 | Yes | NA | PU/PD | LVCMOS |
| Y20 | TDI | TDI | 0x0 | I | H | H | Mode0 | VDDSHV3 | Yes | NA | PU/PD | LVCMOS |
| AA24 | TDO | TDO | 0x0 | O | H | H | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| Y24 | TMS | TMS | 0x0 | I | H | H | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L25 | uart0_ctsn | uart0_ctsn | 0x0 | I | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart4_rxd | 0x1 | I | | | | | | | | |
| | | dcan1_tx | 0x2 | O | | | | | | | | |
| | | I2C1_SDA | 0x3 | IOD | | | | | | | | |
| | | spi1_d0 | 0x4 | IO | | | | | | | | |
| | | timer7 | 0x5 | IO | | | | | | | | |
| | | pr1_edc_sync0_out | 0x6 | O | | | | | | | | |
| | | gpio1_8 | 0x7 | IO | | | | | | | | |
| J25 | uart0_rtsn | uart0_rtsn | 0x0 | O | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | uart4_txd | 0x1 | O | | | | | | | | |
| | | dcan1_rx | 0x2 | I | | | | | | | | |
| | | I2C1_SCL | 0x3 | IOD | | | | | | | | |
| | | spi1_d1 | 0x4 | IO | | | | | | | | |
| | | spi1_cs0 | 0x5 | IO | | | | | | | | |
| | | pr1_edc_sync1_out | 0x6 | O | | | | | | | | |
| | | gpio1_9 | 0x7 | IO | | | | | | | | |
| K25 | uart0_rxd | uart0_rxd | 0x0 | I | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | spi1_cs0 | 0x1 | IO | | | | | | | | |
| | | dcan0_tx | 0x2 | O | | | | | | | | |
| | | I2C2_SDA | 0x3 | IOD | | | | | | | | |
| | | eCAP2_in_PWM2_out | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpo4 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi4 | 0x6 | I | | | | | | | | |
| | | gpio1_10 | 0x7 | IO | | | | | | | | |
| J24 | uart0_txd | uart0_txd | 0x0 | O | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | spi1_cs1 | 0x1 | IO | | | | | | | | |
| | | dcan0_rx | 0x2 | I | | | | | | | | |
| | | I2C2_SCL | 0x3 | IOD | | | | | | | | |
| | | eCAP1_in_PWM1_out | 0x4 | IO | | | | | | | | |
| | | pr0_pru1_gpo5 | 0x5 | O | | | | | | | | |
| | | pr0_pru1_gpi5 | 0x6 | I | | | | | | | | |
| | | gpio1_11 | 0x7 | IO | | | | | | | | |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K22 | uart1_ctsn | uart1_ctsn | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | timer6 | 0x1 | IO | | | | | | | | |
| | | dcan0_tx | 0x2 | O | | | | | | | | |
| | | I2C2_SDA | 0x3 | IOD | | | | | | | | |
| | | spi1_cs0 | 0x4 | IO | | | | | | | | |
| | | pr1_uart0_cts_n | 0x5 | I | | | | | | | | |
| | | pr1_edc_latch0_in | 0x6 | I | | | | | | | | |
| | | gpio0_12 | 0x7 | IO | | | | | | | | |
| L22 | uart1_rtsn | uart1_rtsn | 0x0 | O | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | timer5 | 0x1 | IO | | | | | | | | |
| | | dcan0_rx | 0x2 | I | | | | | | | | |
| | | I2C2_SCL | 0x3 | IOD | | | | | | | | |
| | | spi1_cs1 | 0x4 | IO | | | | | | | | |
| | | pr1_uart0_rts_n | 0x5 | O | | | | | | | | |
| | | pr1_edc_latch1_in | 0x6 | I | | | | | | | | |
| | | gpio0_13 | 0x7 | IO | | | | | | | | |
| K21 | uart1_rxd | uart1_rxd | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc1_sdwp | 0x1 | I | | | | | | | | |
| | | dcan1_tx | 0x2 | O | | | | | | | | |
| | | I2C1_SDA | 0x3 | IOD | | | | | | | | |
| | | pr1_uart0_rxd | 0x5 | I | | | | | | | | |
| | | pr1_pru0_gpi16 | 0x6 | I | | | | | | | | |
| | | gpio0_14 | 0x7 | IO | | | | | | | | |
| L21 | uart1_txd | uart1_txd | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | mmc2_sdwp | 0x1 | I | | | | | | | | |
| | | dcan1_rx | 0x2 | I | | | | | | | | |
| | | I2C1_SCL | 0x3 | IOD | | | | | | | | |
| | | pr1_uart0_txd | 0x5 | O | | | | | | | | |
| | | pr1_pru0_gpi16 | 0x6 | I | | | | | | | | |
| | | gpio0_15 | 0x7 | IO | | | | | | | | |
| H22 | uart3_ctsn | uart3_ctsn | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | spi4_cs1 | 0x2 | IO | | | | | | | | |
| | | pr0_pru1_gpo18 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi18 | 0x5 | I | | | | | | | | |
| | | ehrpwm5A | 0x6 | O | | | | | | | | |
| | | gpio5_0 | 0x7 | IO | | | | | | | | |

## Table 4-10. Pin Attributes (ZDN Package) (continued)

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| K24 | uart3_rtsn | uart3_rtsn | 0x0 | O | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | hdq_sio | 0x1 | IOD | | | | | | | | |
| | | pr0_pru1_gpo19 | 0x4 | O | | | | | | | | |
| | | pr0_pru1_gpi19 | 0x5 | I | | | | | | | | |
| | | ehrpwm5B | 0x6 | O | | | | | | | | |
| | | gpio5_1 | 0x7 | IO | | | | | | | | |
| H25 | uart3_rxd | uart3_rxd | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | pr0_pru0_gpo18 | 0x4 | O | | | | | | | | |
| | | pr0_pru0_gpi18 | 0x5 | I | | | | | | | | |
| | | ehrpwm4A | 0x6 | O | | | | | | | | |
| | | gpio5_2 | 0x7 | IO | | | | | | | | |
| H24 | uart3_txd | uart3_txd | 0x0 | IO | OFF | H | Mode7 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | pr0_pru0_gpo19 | 0x4 | O | | | | | | | | |
| | | pr0_pru0_gpi19 | 0x5 | I | | | | | | | | |
| | | ehrpwm4B | 0x6 | O | | | | | | | | |
| | | gpio5_3 | 0x7 | IO | | | | | | | | |
| W22 | USB0_CE | USB0_CE | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB0/VDDA1P8V_USB0 | NA | NA | NA | Analog |
| W24 | USB0_DM | USB0_DM | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB0/VDDA1P8V_USB0 | NA (20) | 8 (20) | NA | Analog |
| W25 | USB0_DP | USB0_DP | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB0/VDDA1P8V_USB0 | NA (20) | 8 (20) | NA | Analog |
| G21 | USB0_DRVVBUS | USB0_DRVVBUS | 0x0 | O | L | L | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio0_18 | 0x7 | IO | | | | | | | | |
| | | gpio5_27 | 0x9 | IO | | | | | | | | |
| U24 | USB0_ID | USB0_ID | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB0/VDDA1P8V_USB0 | NA | NA | NA | Analog |
| U23 | USB0_VBUS | USB0_VBUS | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB0/VDDA1P8V_USB0 | NA | NA | NA | Analog |
| U22 | USB1_CE | USB1_CE | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB1/VDDA1P8V_USB1 | NA | NA | NA | Analog |
| V25 | USB1_DM | USB1_DM | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB1/VDDA1P8V_USB1 | NA (21) | 8 (21) | NA | Analog |
| V24 | USB1_DP | USB1_DP | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB1/VDDA1P8V_USB1 | NA (21) | 8 (21) | NA | Analog |
| F25 | USB1_DRVVBUS | USB1_DRVVBUS | 0x0 | O | L | L | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |
| | | gpio3_13 | 0x7 | IO | | | | | | | | |
| | | gpio0_25 | 0x9 | IO | | | | | | | | |
| U25 | USB1_ID | USB1_ID | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB1/VDDA1P8V_USB1 | NA | NA | NA | Analog |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T25 | USB1_VBUS | USB1_VBUS | 0x0 | A | Z | Z | Mode0 | VDDA3P3V_USB1/VDDA1P8V_USB1 | NA | NA | NA | Analog |
| W21 | VDDA1P8V_USB0 | VDDA1P8V_USB0 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| U21 | VDDA1P8V_USB1 | VDDA1P8V_USB1 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| W20 | VDDA3P3V_USB0 | VDDA3P3V_USB0 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| U20 | VDDA3P3V_USB1 | VDDA3P3V_USB1 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| AB12 | VDDA_ADC0 | VDDA_ADC0 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| Y16 | VDDA_ADC1 | VDDA_ADC1 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| AD12, AD8, F20, G6, H12, P19, W15, Y19 | VDDS | VDDS (1) | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| F8 | VDDS3P3V_IOLDO | VDDS3P3V_IOLDO | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| J7, J8 | VDDSHV1 | VDDSHV1 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| V16, V17, W16 | VDDSHV2 | VDDSHV2 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| J18, K17, K18, N18, N19, P18, W18 | VDDSHV3 | VDDSHV3 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| F22 | VDDSHV5 | VDDSHV5 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| G16, G17, H17 | VDDSHV6 | VDDSHV6 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| F16 | VDDSHV7 | VDDSHV7 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| G13, G14 | VDDSHV8 | VDDSHV8 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| G11, H11 | VDDSHV9 | VDDSHV9 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| G10, H10 | VDDSHV10 | VDDSHV10 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| H8, H9 | VDDSHV11 | VDDSHV11 | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| E23 | VDDS_CLKOUT | VDDS_CLKOUT | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| K7, K8, M7, M8, N7, N8, R6, R7, R8, T7, T8, V7, V8 | VDDS_DDR | VDDS_DDR | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| C23 | VDDS_OSC | VDDS_OSC | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| N21 | VDDS_PLL_CORE_LCD | VDDS_PLL_CORE_LCD | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| G5 | VDDS_PLL_DDR | VDDS_PLL_DDR | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| E17 | VDDS_PLL_MPU | VDDS_PLL_MPU | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| AD5 | VDDS_RTC | VDDS_RTC | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| F13 | VDDS_SRAM_CORE_BG | VDDS_SRAM_CORE_BG | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| F14 | VDDS_SRAM_MPU_BB | VDDS_SRAM_MPU_BB | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AD9, J10, J11, L12, L14, M12, M14, M9, N16, N17, N9, P16, P17, R11, R14, R9, T11, T14, T18, T19, T9, U15, V15, W12, W13 | VDD_CORE | VDD_CORE (15) | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| H13, H14, H16, J13, J14, J16, K19, K20, L19, L20, M17, M18 | VDD_MPU | VDD_MPU | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| D20 | vdd_mpu_mon | vdd_mpu_mon (30) | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| P21 | VPP | VPP (23) | NA | POWER | NA | NA | NA | NA | NA | NA | NA | NA |
| A1, A25, AA23, AE1, AE10, AE25, AE7, AE8, H15, H18, J12, J15, J17, J9, K11, K12, K14, K15, K9, L11, L15, L17, L18, L8, L9, M10, M11, M13, M15, M16, N10, N11, N12, N13, N14, N15, P10, P11, P12, P13, P14, P15, P8, P9, R12, R15, R17, R18, T12, T15, T17, U10, U11, U12, U13, U14, U16, U17, U18, U19, U8, U9, V10, V11, V12, V13, V14, V18, V9 | VSS | VSS (16) | NA | GROUND | NA | NA | NA | NA | NA | NA | NA | NA |
| AC15 | VSSA_ADC | VSSA_ADC | NA | GROUND | NA | NA | NA | NA | NA | NA | NA | NA |
| W23 | VSSA_USB | VSSA_USB | NA | GROUND | NA | NA | NA | NA | NA | NA | NA | NA |
| B24 | VSS_OSC | VSS_OSC (31) | NA | GROUND | NA | NA | NA | NA | NA | NA | NA | NA |
| AD4 | VSS_RTC | VSS_RTC (32) | NA | GROUND | NA | NA | NA | NA | NA | NA | NA | NA |
| G22 | WARMRSTn | nRESETIN_OUT | 0x0 | IOD (12) | OFF | H (22) | Mode0 | VDDSHV3 | Yes | 6 | PU/PD | LVCMOS |

**Table 4-10. Pin Attributes (ZDN Package) (continued)**

| BALL NUMBER [1] | PIN NAME [2] | SIGNAL NAME [3] | MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. STATE [7] | BALL RESET REL. MODE [8] | POWER [9] | HYS [10] | BUFFER STRENGTH (mA) [11] | PULL UP/DOWN TYPE [12] | IO CELL [13] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D24 | xdma_event_intr0 | xdma_event_intr0 | 0x0 | I | OFF | L (10) | Mode7 (13) | VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | ext_hw_trigger | 0x1 | I | | | | | | | | |
| | | timer4 | 0x2 | IO | | | | | | | | |
| | | clkout1 | 0x3 | O | | | | | | | | |
| | | spi1_cs1 | 0x4 | IO | | | | | | | | |
| | | pr1_pru0_gpi16 | 0x5 | I | | | | | | | | |
| | | EMU2 | 0x6 | IO | | | | | | | | |
| | | gpio0_19 | 0x7 | IO | | | | | | | | |
| | | pr1_mdio_data | 0x8 | IO | | | | | | | | |
| | | gpio5_28 | 0x9 | IO | | | | | | | | |
| C24 | xdma_event_intr1 | xdma_event_intr1 | 0x0 | I | OFF | L (11) | Mode7 (14) | VDDSHV5 | Yes | 6 | PU/PD | LVCMOS |
| | | spi0_cs2 | 0x1 | IO | | | | | | | | |
| | | tclkin | 0x2 | I | | | | | | | | |
| | | clkout2 | 0x3 | O | | | | | | | | |
| | | timer7 | 0x4 | IO | | | | | | | | |
| | | pr1_pru0_gpi16 | 0x5 | I | | | | | | | | |
| | | EMU3 | 0x6 | IO | | | | | | | | |
| | | gpio0_20 | 0x7 | IO | | | | | | | | |
| | | pr1_mdio_mdclk | 0x8 | O | | | | | | | | |
| | | gpio5_29 | 0x9 | IO | | | | | | | | |
| C25 | XTALIN | OSC0_IN | 0x0 (3) | I | Z | Z | Mode0 | VDDS_OSC | Yes | NA | PD | LVCMOS |
| B25 | XTALOUT | OSC0_OUT | 0x0 | O | Z | Z | Mode0 | VDDS_OSC | NA | NA (19) | NA | LVCMOS |

(1) AD12 and AD8 are not connected to VDDS in the device, but they are required to be connected to 1.8V VDDS on the board

(2) An internal 10 kohm pull up is turned on when the oscillator is disabled. The oscillator is disabled by default after power is applied.

(3) An internal 15 kohm pull down is turned on when the oscillator is disabled. The oscillator is enabled by default after power is applied.

(4) Buffer strength of 8mA is for 50ohms. Can be programmed to have a drive of 5-12mA. See TRM (Control Module) for details.

(5) DSS_AC_BIAS_EN terminal is SYSBOOT[18] input, latched on the rising edge of PWRONRSTn

(6) DSS_DATA[15:0] terminals are respectively SYSBOOT[15:0] inputs, latched on the rising edge of PWRONRSTn.

(7) DSS_HSYNC terminal is SYSBOOT[17] input, latched on the rising edge of PWRONRSTn.

(8) DSS_VSYNC terminal is SYSBOOT[16] input, latched on the rising edge of PWRONRSTn.

(9) Do not connect any signal, test point, or board trace to reserved signals.

(10) If sysboot[17] is low on the rising edge of PWRONRSTn, this terminal has an internal pull-down turned on after reset is released. If sysboot[17] is high on the rising edge or PWRONRSTn, this terminal will initially be driven low after reset is released then it begins to toggle at the same frequency of the OSC0_IN terminal.

(11) If sysboot[18] is low on the rising edge of PWRONRSTn, this terminal has an internal pull-down turned on after reset is released. If sysboot[18] is high on the rising edge or PWRONRSTn, this terminal will initially be driven low after reset is released then it begins to toggle at either 25MHz or 50MHz, depending on the value of SYSBOOT[5].

(12) Refer to the External Warm Reset section of the Technical Reference Manual for more information related to the operation of this terminal.

(13) Reset Release Mode = 7 if sysboot[17] is low. Mode = 3 if sysboot[17] is high.

(14) Reset Release Mode = 7 if sysboot[18] is low. Mode = 3 if sysboot[18] is high.

(15) Terminal AD9 is not connected to VDD_CORE in the device, but it is required to be connected to VDD_CORE on the board

(16) Terminals AA23, AE10, AE7, AE8 are not connected to VSS in the device, but they are required to be connected to board ground

(17) The default Pull controls for after reset are set by Control Module Registers (DDR IO Ctrl). Please refer to TRM (Control Module) for details.

(18) The input voltage thresholds for this input are not a function of VDDSHV3. Please refer to the DC Electrical Characteristics section for details related to electrical parameters associated with this input terminal

(19) This output should only be used to source the recommended crystal circuit.

(20) This parameter only applies when this USB PHY terminal is operating in UART2 mode.

(21) This parameter only applies when this USB PHY terminal is operating in UART3 mode.

(22) This pin is configured as Open-drain and hence is expected to have an external Pull-up resistor. However there is also an internal PU resistor by default enabled after reset is deasserted.

(23) This signal is only valid for High Security (AM437xHS) devices. For more details, please refer to the VPP Specification for One-Time Programmable (OTP) eFUSEs section. This signal is reserved for AM437x devices, and thus do not connect any signal, test point, or board trace to this signal for AM437x devices

(24) This terminal is an analog input used to set the switching threshold of the DDR input buffers to (VDDS_DDR / 2).

(25) This terminal is an analog passive signal that connects to an external 49.9 ohm 1%, 20mW reference resistor which is used to calibrate the DDR input/output buffers.

(26) This terminal is analog input that may also be configured as an open-drain output.

(27) This terminal is analog input that may also be configured as an open-source or open-drain output.

(28) This terminal is analog input that may also be configured as an open-source output.

(29) This terminal is high-Z when the oscillator is disabled. This terminal is driven high if RTC_XTALIN is less than VIL, driven low if RTC_XTALIN is greater than VIH, and driven to a unknown value if RTC_XTALIN is between VIL and VIH when the oscillator is enabled. The oscillator is disabled by default after power is applied.

(30) This terminal provides a Kelvin connection to VDD_MPU. It can be connected to the power supply feedback input to provide remote sensing which compensates for voltage drop in the PCB power distribution network and package. When the Kelvin connection is not used it should be connected to the same power source as VDD_MPU.

(31) This terminal provides a Kelvin ground reference for the external crystal components. If a crystal circuit is connected to the OSC0_IN/OSC0_OUT terminals, the crystal circuit component grounds should be connected to this terminal and also be connected to the PCB ground plane close to this terminal. If an external LVCMOS clock source is connected to the OSC0_IN terminal, this terminal should be connected to VSS.

(32) This terminal provides a Kelvin ground reference for the external crystal components. If a crystal circuit is connected to the OSC1_IN/OSC1_OUT terminals, the crystal circuit component grounds should be connected to this terminal and also should be connected to the PCB ground plane close to this terminal. If an external LVCMOS clock source is connected to the OSC1_IN terminal, this terminal should be connected to VSS

## 4.3 Signal Descriptions

The device contains many peripheral interfaces. In order to reduce package size and lower overall system cost while maintaining maximum functionality, many of the terminals can multiplex up to eight signal functions. Although there are many combinations of pin multiplexing that are possible, only a certain number of sets, called IO Sets, are valid due to timing limitations. These valid IO Sets were carefully chosen to provide many possible application scenarios for the user.

TI has developed a Windows-based application called Pin Mux Utility that helps a system designer select the appropriate pin-multiplexing configuration for their device-based product design. The Pin Mux Utility provides a way to select valid IO Sets of specific peripheral interfaces to ensure the pin-multiplexing configuration selected for a design only uses valid IO Sets supported by the device.

(1) **SIGNAL NAME:** The signal name

(2) **DESCRIPTION:** Description of the signal.

(3) **TYPE:** Ball type for this specific function:

- I = Input
- O = Output
- I/O = Input/Output
- D = Open drain
- DS = Differential
- A = Analog

(4) **BALL:** Package ball location.

### *4.3.1 ADC Interfaces*

**Table 4-11. ADC0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ADC0_VREFN | Analog Negative Reference Input | AP | AE14 |
| ADC0_VREFP | Analog Positive Reference Input | AP | AD14 |
| ADC0_AIN0 | Analog Input/Output | A | AA12 |
| ADC0_AIN1 | Analog Input/Output | A | Y12 |
| ADC0_AIN2 | Analog Input/Output | A | Y13 |
| ADC0_AIN3 | Analog Input/Output | A | AA13 |
| ADC0_AIN4 | Analog Input/Output | A | AB13 |
| ADC0_AIN5 | Analog Input/Output | A | AC13 |
| ADC0_AIN6 | Analog Input/Output | A | AD13 |
| ADC0_AIN7 | Analog Input/Output | A | AE13 |

**Table 4-12. ADC0/1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ext_hw_trigger | External Hardware Trigger for ADC conversion | I | AC25, D24 |

**Table 4-13. ADC1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ADC1_VREFN | Analog Negative Reference Input | AP | AD15 |
| ADC1_VREFP | Analog Positive Reference Input | AP | AE15 |
| ADC1_AIN0 | Analog Input/Output | A | AC16 |
| ADC1_AIN1 | Analog Input/Output | A | AB16 |
| ADC1_AIN2 | Analog Input/Output | A | AA16 |
| ADC1_AIN3 | Analog Input/Output | A | AB15 |
| ADC1_AIN4 | Analog Input/Output | A | AA15 |
| ADC1_AIN5 | Analog Input/Output | A | Y15 |
| ADC1_AIN6 | Analog Input/Output | A | AE16 |

**Table 4-13. ADC1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ADC1_AIN7 | Analog Input/Output | A | AD16 |

### 4.3.2 CAN Interfaces

**Table 4-14. DCAN0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| dcan0_rx | DCAN0 Receive Data | I | C13, J24, L22 |
| dcan0_tx | DCAN0 Transmit Data | O | C16, K22, K25 |

**Table 4-15. DCAN1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| dcan1_rx | DCAN1 Receive Data | I | D2, J25, L21 |
| dcan1_tx | DCAN1 Transmit Data | O | D1, K21, L25 |

### 4.3.3 Camera (VPFE) Interfaces

**Table 4-16. Camera0 Input Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| cam0_field | CCD Data Field Indicator | IO | AC18 |
| cam0_hd | CCD Data Horizontal Detect | IO | AE17 |
| cam0_pclk | CCD Data Pixel Clock | I | AC20 |
| cam0_vd | CCD Data Vertical Detect | IO | AD18 |
| cam0_wen | CCD Data Write Enable | I | AD17 |
| cam0_data0 | Camera data | I | AE18 |
| cam0_data1 | Camera data | I | AB18 |
| cam0_data2 | Camera data | I | Y18 |
| cam0_data3 | Camera data | I | AA18 |
| cam0_data4 | Camera data | I | AE19 |
| cam0_data5 | Camera data | I | AD19 |
| cam0_data6 | Camera data | I | AE20 |
| cam0_data7 | Camera data | I | AD20 |
| cam0_data8 | Camera data | I | AB19 |
| cam0_data9 | Camera data | I | AA19 |
| cam0_data10 | Camera data | I | AC18, AC25 |
| cam0_data11 | Camera data | I | AB25, AD17 |

**Table 4-17. Camera1 Input Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| cam1_field | CCD Data Field Indicator | IO | AC25 |
| cam1_hd | CCD Data Horizontal Detect | IO | AD25 |
| cam1_pclk | CCD Data Pixel Clock | I | AE21 |
| cam1_vd | CCD Data Vertical Detect | IO | AC23 |
| cam1_wen | CCD Data Write Enable | I | AB25, AE19 |
| cam1_data0 | Camera data | I | AB20 |
| cam1_data1 | Camera data | I | AC21 |
| cam1_data2 | Camera data | I | AD21 |
| cam1_data3 | Camera data | I | AE22 |
| cam1_data4 | Camera data | I | AD22 |
| cam1_data5 | Camera data | I | AE23 |
| cam1_data6 | Camera data | I | AD23 |
| cam1_data7 | Camera data | I | AE24 |
| cam1_data8 | Camera data | I | AB18, AD24 |
| cam1_data9 | Camera data | I | AC24, AE18 |
| cam1_data10 | Camera data | I | AC18, AC25, Y18 |
| cam1_data11 | Camera data | I | AA18, AB25, AD17 |

### 4.3.4 Debug Subsystem Interface

**Table 4-18. Debug Subsystem Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| EMU0 | MISC EMULATION PIN | IO | N23 |
| EMU1 | MISC EMULATION PIN | IO | T24 |
| EMU2 | MISC EMULATION PIN | IO | AE17, D24, K23, P23 |
| EMU3 | MISC EMULATION PIN | IO | AD18, C24, M25, T22 |
| EMU4 | MISC EMULATION PIN | IO | AC18, B12, L24, R25 |
| EMU5 | MISC EMULATION PIN | IO | AD17 |
| EMU6 | MISC EMULATION PIN | IO | AC20 |
| EMU7 | MISC EMULATION PIN | IO | AB19 |
| EMU8 | MISC EMULATION PIN | IO | AA19 |
| EMU9 | MISC EMULATION PIN | IO | AC24 |
| EMU10 | MISC EMULATION PIN | IO | AD24, AE17 |
| EMU11 | MISC EMULATION PIN | IO | AB25, AD18 |
| nTRST | JTAG TEST RESET (ACTIVE LOW) | I | Y25 |
| TCK | JTAG TEST CLOCK | I | AA25 |
| TDI | JTAG TEST DATA INPUT | I | Y20 |
| TDO | JTAG TEST DATA OUTPUT | O | AA24 |
| TMS | JTAG TEST MODE SELECT | I | Y24 |

### 4.3.5 Display Subsystem (DSS) Interface

**Table 4-19. Display Subsystem (DSS) Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| dss_ac_bias_en | DSS data | O | A24 |
| dss_data0 | DSS data | IO | B22 |
| dss_data1 | DSS data | IO | A21 |
| dss_data2 | DSS data | IO | B21 |
| dss_data3 | DSS data | IO | C21 |
| dss_data4 | DSS data | IO | A20 |
| dss_data5 | DSS data | IO | B20 |
| dss_data6 | DSS data | IO | C20 |
| dss_data7 | DSS data | IO | E19 |
| dss_data8 | DSS data | IO | A19 |
| dss_data9 | DSS data | IO | B19 |
| dss_data10 | DSS data | IO | A18 |
| dss_data11 | DSS data | IO | B18 |
| dss_data12 | DSS data | IO | C19 |
| dss_data13 | DSS data | IO | D19 |
| dss_data14 | DSS data | IO | C17 |
| dss_data15 | DSS data | IO | D17 |
| dss_data16 | DSS data | O | A11, AC24 |
| dss_data17 | DSS data | O | AA19, B11 |
| dss_data18 | DSS data | O | AB19, C11 |
| dss_data19 | DSS data | O | AC20, E11 |
| dss_data20 | DSS data | O | AD17, D11 |
| dss_data21 | DSS data | O | AC18, F11 |
| dss_data22 | DSS data | O | A10, AD18 |
| dss_data23 | DSS data | O | AE17, B10 |
| dss_hsync | DSS Horizontal Sync | O | A23 |
| dss_pclk | DSS Pixel Clock | O | A22 |
| dss_vsync | DSS Vertical Sync | O | B23 |

### 4.3.6 Ethernet (GEMAC_CPSW) Interfaces

**Table 4-20. MDIO Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mdio_clk | MDIO Clk | O | B17 |
| mdio_data | MDIO Data | IO | A17 |

**Table 4-21. MII1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gmii1_col | MII Colision | I | D16 |
| gmii1_crs | MII Carrier Sense | I | B14 |
| gmii1_rxclk | MII Receive Clock | I | D13 |
| gmii1_rxdv | MII Receive Data Valid | I | A15 |
| gmii1_rxer | MII Receive Data Error | I | B13 |
| gmii1_txclk | MII Transmit Clock | I | D14 |
| gmii1_txen | MII Transmit Enable | O | A13 |
| gmii1_rxd0 | MII Receive Data bit 0 | I | F17 |
| gmii1_rxd1 | MII Receive Data bit 1 | I | B16 |
| gmii1_rxd2 | MII Receive Data bit 2 | I | E16 |
| gmii1_rxd3 | MII Receive Data bit 3 | I | C14 |
| gmii1_txd0 | MII Transmit Data bit 0 | O | B15 |
| gmii1_txd1 | MII Transmit Data bit 1 | O | A14 |
| gmii1_txd2 | MII Transmit Data bit 2 | O | C13 |
| gmii1_txd3 | MII Transmit Data bit 3 | O | C16 |

**Table 4-22. MII2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gmii2_col | MII Colision | I | A3 |
| gmii2_crs | MII Carrier Sense | I | A2, B12, F10 |
| gmii2_rxclk | MII Receive Clock | I | F6 |
| gmii2_rxdv | MII Receive Data Valid | I | C5 |
| gmii2_rxer | MII Receive Data Error | I | B3 |
| gmii2_txclk | MII Transmit Clock | I | E8 |
| gmii2_txen | MII Transmit Enable | O | C3 |
| gmii2_rxd0 | MII Receive Data bit 0 | I | D8 |
| gmii2_rxd1 | MII Receive Data bit 1 | I | G8 |
| gmii2_rxd2 | MII Receive Data bit 2 | I | B4 |
| gmii2_rxd3 | MII Receive Data bit 3 | I | F7 |
| gmii2_txd0 | MII Transmit Data bit 0 | O | E7 |
| gmii2_txd1 | MII Transmit Data bit 1 | O | D7 |
| gmii2_txd2 | MII Transmit Data bit 2 | O | A4 |
| gmii2_txd3 | MII Transmit Data bit 3 | O | C6 |

**Table 4-23. RGMII1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| rgmii1_rclk | RGMII Receive Clock | I | D13 |
| rgmii1_rctl | RGMII Receive Control | I | A15 |
| rgmii1_tclk | RGMII Transmit Clock | O | D14 |

**Table 4-23. RGMII1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| rgmii1_tctl | RGMII Transmit Control | O | A13 |
| rgmii1_rd0 | RGMII Receive Data bit 0 | I | F17 |
| rgmii1_rd1 | RGMII Receive Data bit 1 | I | B16 |
| rgmii1_rd2 | RGMII Receive Data bit 2 | I | E16 |
| rgmii1_rd3 | RGMII Receive Data bit 3 | I | C14 |
| rgmii1_td0 | RGMII Transmit Data bit 0 | O | B15 |
| rgmii1_td1 | RGMII Transmit Data bit 1 | O | A14 |
| rgmii1_td2 | RGMII Transmit Data bit 2 | O | C13 |
| rgmii1_td3 | RGMII Transmit Data bit 3 | O | C16 |

**Table 4-24. RGMII2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| rgmii2_rclk | RGMII Receive Clock | I | F6 |
| rgmii2_rctl | RGMII Receive Control | I | C5 |
| rgmii2_tclk | RGMII Transmit Clock | O | E8 |
| rgmii2_tctl | RGMII Transmit Control | O | C3 |
| rgmii2_rd0 | RGMII Receive Data bit 0 | I | D8 |
| rgmii2_rd1 | RGMII Receive Data bit 1 | I | G8 |
| rgmii2_rd2 | RGMII Receive Data bit 2 | I | B4 |
| rgmii2_rd3 | RGMII Receive Data bit 3 | I | F7 |
| rgmii2_td0 | RGMII Transmit Data bit 0 | O | E7 |
| rgmii2_td1 | RGMII Transmit Data bit 1 | O | D7 |
| rgmii2_td2 | RGMII Transmit Data bit 2 | O | A4 |
| rgmii2_td3 | RGMII Transmit Data bit 3 | O | C6 |

**Table 4-25. RMII1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| rmii1_crs_dv | RMII Carrier Sense / Data Valid | I | B14 |
| rmii1_refclk | RMII Reference Clock | IO | A16 |
| rmii1_rxer | RMII Receive Data Error | I | B13 |
| rmii1_txen | RMII Transmit Enable | O | A13 |
| rmii1_rxd0 | RMII Receive Data bit 0 | I | F17 |
| rmii1_rxd1 | RMII Receive Data bit 1 | I | B16 |
| rmii1_txd0 | RMII Transmit Data bit 0 | O | B15 |
| rmii1_txd1 | RMII Transmit Data bit 1 | O | A14 |

**Table 4-26. RMII2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| rmii2_crs_dv | RMII Carrier Sense / Data Valid | I | A2, B12, B4, F10 |
| rmii2_refclk | RMII Reference Clock | IO | D16 |
| rmii2_rxer | RMII Receive Data Error | I | B3 |
| rmii2_txen | RMII Transmit Enable | O | C3 |
| rmii2_rxd0 | RMII Receive Data bit 0 | I | D8 |
| rmii2_rxd1 | RMII Receive Data bit 1 | I | G8 |
| rmii2_txd0 | RMII Transmit Data bit 0 | O | E7 |
| rmii2_txd1 | RMII Transmit Data bit 1 | O | D7 |

### 4.3.7 External Memory Interfaces

**Table 4-27. DDR Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ddr_a0 | DDR SDRAM ROW/COLUMN ADDRESS | O | N1 |
| ddr_a1 | DDR SDRAM ROW/COLUMN ADDRESS | O | L1 |
| ddr_a2 | DDR SDRAM ROW/COLUMN ADDRESS | O | L2 |
| ddr_a3 | DDR SDRAM ROW/COLUMN ADDRESS | O | P2 |
| ddr_a4 | DDR SDRAM ROW/COLUMN ADDRESS | O | P1 |
| ddr_a5 | DDR SDRAM ROW/COLUMN ADDRESS | O | R5 |
| ddr_a6 | DDR SDRAM ROW/COLUMN ADDRESS | O | R4 |
| ddr_a7 | DDR SDRAM ROW/COLUMN ADDRESS | O | R3 |
| ddr_a8 | DDR SDRAM ROW/COLUMN ADDRESS | O | R2 |
| ddr_a9 | DDR SDRAM ROW/COLUMN ADDRESS | O | R1 |
| ddr_a10 | DDR SDRAM ROW/COLUMN ADDRESS | O | M6 |
| ddr_a11 | DDR SDRAM ROW/COLUMN ADDRESS | O | T5 |
| ddr_a12 | DDR SDRAM ROW/COLUMN ADDRESS | O | T4 |
| ddr_a13 | DDR SDRAM ROW/COLUMN ADDRESS | O | N5 |
| ddr_a14 | DDR SDRAM ROW/COLUMN ADDRESS | O | T3 |
| ddr_a15 | DDR SDRAM ROW/COLUMN ADDRESS | O | T2 |
| ddr_ba0 | DDR SDRAM BANK ADDRESS | O | K1 |
| ddr_ba1 | DDR SDRAM BANK ADDRESS | O | K2 |
| ddr_ba2 | DDR SDRAM BANK ADDRESS | O | K3 |
| ddr_casn | DDR SDRAM COLUMN ADDRESS STROBE. (ACTIVE LOW) | O | N3 |
| ddr_ck | DDR SDRAM CLOCK (Differential+) | O | M2 |
| ddr_cke0 | DDR SDRAM CLOCK ENABLE | O | M3 |
| ddr_cke1 | DDR SDRAM CLOCK ENABLE1 | O | N6 |
| ddr_csn0 | DDR SDRAM CHIP SELECT0 | O | M5 |
| ddr_csn1 | DDR SDRAM CHIP SELECT1 | O | M4 |
| ddr_d0 | DDR SDRAM DATA | IO | E3 |
| ddr_d1 | DDR SDRAM DATA | IO | E2 |
| ddr_d2 | DDR SDRAM DATA | IO | E1 |
| ddr_d3 | DDR SDRAM DATA | IO | F3 |
| ddr_d4 | DDR SDRAM DATA | IO | G4 |
| ddr_d5 | DDR SDRAM DATA | IO | G3 |
| ddr_d6 | DDR SDRAM DATA | IO | G2 |
| ddr_d7 | DDR SDRAM DATA | IO | G1 |
| ddr_d8 | DDR SDRAM DATA | IO | H1 |
| ddr_d9 | DDR SDRAM DATA | IO | J6 |
| ddr_d10 | DDR SDRAM DATA | IO | J5 |
| ddr_d11 | DDR SDRAM DATA | IO | J4 |
| ddr_d12 | DDR SDRAM DATA | IO | J3 |
| ddr_d13 | DDR SDRAM DATA | IO | K6 |
| ddr_d14 | DDR SDRAM DATA | IO | K5 |
| ddr_d15 | DDR SDRAM DATA | IO | K4 |
| ddr_d16 | DDR SDRAM DATA | IO | V5 |
| ddr_d17 | DDR SDRAM DATA | IO | V4 |
| ddr_d18 | DDR SDRAM DATA | IO | V3 |
| ddr_d19 | DDR SDRAM DATA | IO | V2 |

**Table 4-27. DDR Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ddr_d20 | DDR SDRAM DATA | IO | V1 |
| ddr_d21 | DDR SDRAM DATA | IO | W4 |
| ddr_d22 | DDR SDRAM DATA | IO | W5 |
| ddr_d23 | DDR SDRAM DATA | IO | W6 |
| ddr_d24 | DDR SDRAM DATA | IO | Y2 |
| ddr_d25 | DDR SDRAM DATA | IO | Y3 |
| ddr_d26 | DDR SDRAM DATA | IO | Y4 |
| ddr_d27 | DDR SDRAM DATA | IO | AA3 |
| ddr_d28 | DDR SDRAM DATA | IO | AB2 |
| ddr_d29 | DDR SDRAM DATA | IO | AB1 |
| ddr_d30 | DDR SDRAM DATA | IO | AC1 |
| ddr_d31 | DDR SDRAM DATA | IO | AC2 |
| ddr_dqm0 | DDR WRITE ENABLE / DATA MASK FOR DATA[7:0] | O | F4 |
| ddr_dqm1 | DDR WRITE ENABLE / DATA MASK FOR DATA[15:8] | O | H2 |
| ddr_dqm2 | DDR WRITE ENABLE / DATA MASK FOR DATA[23:16] | O | V6 |
| ddr_dqm3 | DDR WRITE ENABLE / DATA MASK FOR DATA[31:24] | O | Y1 |
| ddr_dqs0 | DDR DATA STROBE FOR DATA[7:0] (Differential+) | IO | F2 |
| ddr_dqs1 | DDR DATA STROBE FOR DATA[15:8] (Differential+) | IO | J2 |
| ddr_dqs2 | DDR DATA STROBE FOR DATA[23:16] (Differential+) | IO | W1 |
| ddr_dqs3 | DDR DATA STROBE FOR DATA[31:24] (Differential+) | IO | AA1 |
| ddr_dqsn0 | DDR DATA STROBE FOR DATA[7:0] (Differential-) | IO | F1 |
| ddr_dqsn1 | DDR DATA STROBE FOR DATA[15:8] (Differential-) | IO | J1 |
| ddr_dqsn2 | DDR DATA STROBE FOR DATA[23:16] (Differential-) | IO | W2 |
| ddr_dqsn3 | DDR DATA STROBE FOR DATA[31:24] (Differential-) | IO | AA2 |
| ddr_nck | DDR SDRAM CLOCK (Differential-) | O | M1 |
| ddr_odt0 | DDR SDRAM ODT0 | O | U1 |
| ddr_odt1 | DDR SDRAM ODT1 | O | U2 |
| ddr_rasn | DDR SDRAM ROW ADDRESS STROBE (ACTIVE LOW) | O | N2 |
| ddr_resetn | DDR SDRAM RESET (only for DDR3) | O | T1 |
| ddr_vref | Voltage Reference | AP (1) | T6 |
| ddr_vtp | External Resistor for Impedance Training | I (2) | AC3 |
| ddr_wen | DDR SDRAM WRITE ENABLE (ACTIVE LOW) | O | N4 |

(1) This terminal is an analog input used to set the switching threshold of the DDR input buffers to (VDDS_DDR / 2).

(2) This terminal is an analog passive signal that connects to an external 49.9 ohm 1%, 20mW reference resistor which is used to calibrate the DDR input/output buffers.

**Table 4-28. General Purpose Memory Controller (GPMC) Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpmc_a0 | GPMC Address | O | B22, C3 |
| gpmc_a1 | GPMC Address | O | A21, B23, C5 |
| gpmc_a2 | GPMC Address | O | A23, B21, C6 |
| gpmc_a3 | GPMC Address | O | A22, A4, C21 |
| gpmc_a4 | GPMC Address | O | A20, A24, D7 |
| gpmc_a5 | GPMC Address | O | B20, C10, E7 |
| gpmc_a6 | GPMC Address | O | C20, E8 |
| gpmc_a7 | GPMC Address | O | E19, F6 |
| gpmc_a8 | GPMC Address | O | B23, F7 |

**Table 4-28. General Purpose Memory Controller (GPMC) Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpmc_a9 | GPMC Address | O | A23, B4 |
| gpmc_a10 | GPMC Address | O | A22, G8 |
| gpmc_a11 | GPMC Address | O | A24, D8 |
| gpmc_a12 | GPMC Address | O | A19 |
| gpmc_a13 | GPMC Address | O | B19 |
| gpmc_a14 | GPMC Address | O | A18 |
| gpmc_a15 | GPMC Address | O | B18 |
| gpmc_a16 | GPMC Address | O | C19, C3 |
| gpmc_a17 | GPMC Address | O | C5, D19 |
| gpmc_a18 | GPMC Address | O | C17, C6 |
| gpmc_a19 | GPMC Address | O | A4, D17 |
| gpmc_a20 | GPMC Address | O | B1, D7 |
| gpmc_a21 | GPMC Address | O | B2, E7 |
| gpmc_a22 | GPMC Address | O | C2, E8 |
| gpmc_a23 | GPMC Address | O | C1, F6 |
| gpmc_a24 | GPMC Address | O | D1, F7 |
| gpmc_a25 | GPMC Address | O | B4, D2 |
| gpmc_a26 | GPMC Address | O | G8 |
| gpmc_a27 | GPMC Address | O | D8 |
| gpmc_ad0 | GPMC Address and Data | IO | B5 |
| gpmc_ad1 | GPMC Address and Data | IO | A5 |
| gpmc_ad2 | GPMC Address and Data | IO | B6 |
| gpmc_ad3 | GPMC Address and Data | IO | A6 |
| gpmc_ad4 | GPMC Address and Data | IO | B7 |
| gpmc_ad5 | GPMC Address and Data | IO | A7 |
| gpmc_ad6 | GPMC Address and Data | IO | C8 |
| gpmc_ad7 | GPMC Address and Data | IO | B8 |
| gpmc_ad8 | GPMC Address and Data | IO | B10 |
| gpmc_ad9 | GPMC Address and Data | IO | A10 |
| gpmc_ad10 | GPMC Address and Data | IO | F11 |
| gpmc_ad11 | GPMC Address and Data | IO | D11 |
| gpmc_ad12 | GPMC Address and Data | IO | E11 |
| gpmc_ad13 | GPMC Address and Data | IO | C11 |
| gpmc_ad14 | GPMC Address and Data | IO | B11 |
| gpmc_ad15 | GPMC Address and Data | IO | A11 |
| gpmc_advn_ale | GPMC Address Valid / Address Latch Enable | O | A9 |
| gpmc_be0n_cle | GPMC Byte Enable 0 / Command Latch Enable | O | C10 |
| gpmc_be1n | GPMC Byte Enable 1 | O | A3, F10 |
| gpmc_clk | GPMC Clock | IO | A12, B9 |
| gpmc_csn0 | GPMC Chip Select | O | A8 |
| gpmc_csn1 | GPMC Chip Select | O | B9 |
| gpmc_csn2 | GPMC Chip Select | O | F10 |
| gpmc_csn3 | GPMC Chip Select | O | B12 |
| gpmc_csn4 | GPMC Chip Select | O | A2 |
| gpmc_csn5 | GPMC Chip Select | O | B3 |
| gpmc_csn6 | GPMC Chip Select | O | A3 |
| gpmc_dir | GPMC Data Direction | O | A3 |

**Table 4-28. General Purpose Memory Controller (GPMC) Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpmc_oen_ren | GPMC Output / Read Enable | O | E10 |
| gpmc_wait0 | GPMC Wait 0 | I | A2, B12 |
| gpmc_wait1 | GPMC Wait 1 | I | A12 |
| gpmc_wen | GPMC Write Enable | O | D10 |
| gpmc_wpn | GPMC Write Protect | O | B3 |

### 4.3.8 General Purpose IOs

**Table 4-29. GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio0_0 | GPIO | IO | A17, D16 |
| gpio0_1 | GPIO | IO | A15, B17 |
| gpio0_2 | GPIO | IO | M25, P23 |
| gpio0_3 | GPIO | IO | L24, T22 |
| gpio0_4 | GPIO | IO | A12, T21 |
| gpio0_5 | GPIO | IO | T20 |
| gpio0_6 | GPIO | IO | R25 |
| gpio0_7 | GPIO | IO | G24 |
| gpio0_8 | GPIO | IO | C19, D14 |
| gpio0_9 | GPIO | IO | D13, D19 |
| gpio0_10 | GPIO | IO | C14, C17 |
| gpio0_11 | GPIO | IO | D17, E16 |
| gpio0_12 | GPIO | IO | K22 |
| gpio0_13 | GPIO | IO | L22 |
| gpio0_14 | GPIO | IO | K21 |
| gpio0_15 | GPIO | IO | L21 |
| gpio0_16 | GPIO | IO | C16 |
| gpio0_17 | GPIO | IO | C13 |
| gpio0_18 | GPIO | IO | G21, L23 |
| gpio0_19 | GPIO | IO | D24, K23 |
| gpio0_20 | GPIO | IO | C24, P22 |
| gpio0_21 | GPIO | IO | A14, P20 |
| gpio0_22 | GPIO | IO | B10, N20 |
| gpio0_23 | GPIO | IO | A10, T23 |
| gpio0_24 | GPIO | IO | H20 |
| gpio0_25 | GPIO | IO | F25 |
| gpio0_26 | GPIO | IO | F11 |
| gpio0_27 | GPIO | IO | D11 |
| gpio0_28 | GPIO | IO | B15 |
| gpio0_29 | GPIO | IO | A16 |
| gpio0_30 | GPIO | IO | A2 |
| gpio0_31 | GPIO | IO | B3 |

**Table 4-30. GPIO1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio1_0 | GPIO | IO | B5 |
| gpio1_1 | GPIO | IO | A5 |
| gpio1_2 | GPIO | IO | B6 |
| gpio1_3 | GPIO | IO | A6 |
| gpio1_4 | GPIO | IO | B7 |
| gpio1_5 | GPIO | IO | A7 |
| gpio1_6 | GPIO | IO | C8 |
| gpio1_7 | GPIO | IO | B8 |
| gpio1_8 | GPIO | IO | L25 |
| gpio1_9 | GPIO | IO | J25 |

**Table 4-30. GPIO1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio1_10 | GPIO | IO | K25 |
| gpio1_11 | GPIO | IO | J24 |
| gpio1_12 | GPIO | IO | E11 |
| gpio1_13 | GPIO | IO | C11 |
| gpio1_14 | GPIO | IO | B11 |
| gpio1_15 | GPIO | IO | A11 |
| gpio1_16 | GPIO | IO | C3 |
| gpio1_17 | GPIO | IO | C5 |
| gpio1_18 | GPIO | IO | C6 |
| gpio1_19 | GPIO | IO | A4 |
| gpio1_20 | GPIO | IO | D7 |
| gpio1_21 | GPIO | IO | E7 |
| gpio1_22 | GPIO | IO | E8 |
| gpio1_23 | GPIO | IO | F6 |
| gpio1_24 | GPIO | IO | F7 |
| gpio1_25 | GPIO | IO | B4 |
| gpio1_26 | GPIO | IO | G8 |
| gpio1_27 | GPIO | IO | D8 |
| gpio1_28 | GPIO | IO | A3 |
| gpio1_29 | GPIO | IO | A8 |
| gpio1_30 | GPIO | IO | B9 |
| gpio1_31 | GPIO | IO | F10 |

**Table 4-31. GPIO2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio2_0 | GPIO | IO | B12 |
| gpio2_1 | GPIO | IO | A12 |
| gpio2_2 | GPIO | IO | A9 |
| gpio2_3 | GPIO | IO | E10 |
| gpio2_4 | GPIO | IO | D10 |
| gpio2_5 | GPIO | IO | C10 |
| gpio2_6 | GPIO | IO | B22 |
| gpio2_7 | GPIO | IO | A21 |
| gpio2_8 | GPIO | IO | B21 |
| gpio2_9 | GPIO | IO | C21 |
| gpio2_10 | GPIO | IO | A20 |
| gpio2_11 | GPIO | IO | B20 |
| gpio2_12 | GPIO | IO | C20 |
| gpio2_13 | GPIO | IO | E19 |
| gpio2_14 | GPIO | IO | A19 |
| gpio2_15 | GPIO | IO | B19 |
| gpio2_16 | GPIO | IO | A18 |
| gpio2_17 | GPIO | IO | B18 |
| gpio2_18 | GPIO | IO | C14 |
| gpio2_19 | GPIO | IO | E16 |
| gpio2_20 | GPIO | IO | B16 |
| gpio2_21 | GPIO | IO | F17 |

**Table 4-31. GPIO2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio2_22 | GPIO | IO | B23 |
| gpio2_23 | GPIO | IO | A23 |
| gpio2_24 | GPIO | IO | A22 |
| gpio2_25 | GPIO | IO | A24 |
| gpio2_26 | GPIO | IO | B1 |
| gpio2_27 | GPIO | IO | B2 |
| gpio2_28 | GPIO | IO | C2 |
| gpio2_29 | GPIO | IO | C1 |
| gpio2_30 | GPIO | IO | D1 |
| gpio2_31 | GPIO | IO | D2 |

**Table 4-32. GPIO3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio3_0 | GPIO | IO | D16 |
| gpio3_1 | GPIO | IO | B14 |
| gpio3_2 | GPIO | IO | B13 |
| gpio3_3 | GPIO | IO | A13 |
| gpio3_4 | GPIO | IO | A15 |
| gpio3_5 | GPIO | IO | AB24 |
| gpio3_6 | GPIO | IO | Y22 |
| gpio3_7 | GPIO | IO | N23 |
| gpio3_8 | GPIO | IO | T24 |
| gpio3_9 | GPIO | IO | D14 |
| gpio3_10 | GPIO | IO | D13 |
| gpio3_11 | GPIO | IO | C16 |
| gpio3_12 | GPIO | IO | C13 |
| gpio3_13 | GPIO | IO | F25 |
| gpio3_14 | GPIO | IO | N24 |
| gpio3_15 | GPIO | IO | N22 |
| gpio3_16 | GPIO | IO | H23 |
| gpio3_17 | GPIO | IO | M24 |
| gpio3_18 | GPIO | IO | L23 |
| gpio3_19 | GPIO | IO | K23 |
| gpio3_20 | GPIO | IO | M25 |
| gpio3_21 | GPIO | IO | L24 |
| gpio3_22 | GPIO | IO | P22 |
| gpio3_23 | GPIO | IO | P20 |
| gpio3_24 | GPIO | IO | N20 |
| gpio3_25 | GPIO | IO | T23 |

**Table 4-33. GPIO4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio4_0 | GPIO | IO | AE17 |
| gpio4_1 | GPIO | IO | AD18 |
| gpio4_2 | GPIO | IO | AC18 |
| gpio4_3 | GPIO | IO | AD17 |
| gpio4_4 | GPIO | IO | AC20 |

**Table 4-33. GPIO4 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio4_5 | GPIO | IO | AB19 |
| gpio4_6 | GPIO | IO | AA19 |
| gpio4_7 | GPIO | IO | AC24 |
| gpio4_8 | GPIO | IO | AD24 |
| gpio4_9 | GPIO | IO | AD25 |
| gpio4_10 | GPIO | IO | AC23 |
| gpio4_11 | GPIO | IO | AE21 |
| gpio4_12 | GPIO | IO | AC25 |
| gpio4_13 | GPIO | IO | AB25 |
| gpio4_14 | GPIO | IO | AB20 |
| gpio4_15 | GPIO | IO | AC21 |
| gpio4_16 | GPIO | IO | AD21 |
| gpio4_17 | GPIO | IO | AE22 |
| gpio4_18 | GPIO | IO | AD22 |
| gpio4_19 | GPIO | IO | AE23 |
| gpio4_20 | GPIO | IO | AD23 |
| gpio4_21 | GPIO | IO | AE24 |
| gpio4_24 | GPIO | IO | Y18 |
| gpio4_25 | GPIO | IO | AA18 |
| gpio4_26 | GPIO | IO | AE19 |
| gpio4_27 | GPIO | IO | AD19 |
| gpio4_28 | GPIO | IO | AE20 |
| gpio4_29 | GPIO | IO | AD20 |

**Table 4-34. GPIO5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio5_0 | GPIO | IO | H22 |
| gpio5_1 | GPIO | IO | K24 |
| gpio5_2 | GPIO | IO | H25 |
| gpio5_3 | GPIO | IO | H24 |
| gpio5_4 | GPIO | IO | P25 |
| gpio5_5 | GPIO | IO | R24 |
| gpio5_6 | GPIO | IO | P24 |
| gpio5_7 | GPIO | IO | N25 |
| gpio5_8 | GPIO | IO | D25 |
| gpio5_9 | GPIO | IO | F24 |
| gpio5_10 | GPIO | IO | G20 |
| gpio5_11 | GPIO | IO | F23 |
| gpio5_12 | GPIO | IO | E25 |
| gpio5_13 | GPIO | IO | E24 |
| gpio5_19 | GPIO | IO | AE18 |
| gpio5_20 | GPIO | IO | AB18 |
| gpio5_23 | GPIO | IO | D11 |
| gpio5_24 | GPIO | IO | F11 |
| gpio5_25 | GPIO | IO | A10 |
| gpio5_26 | GPIO | IO | B10 |
| gpio5_27 | GPIO | IO | G21 |

**Table 4-34. GPIO5 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| gpio5_28 | GPIO | IO | D24 |
| gpio5_29 | GPIO | IO | C24 |
| gpio5_30 | GPIO | IO | A2 |
| gpio5_31 | GPIO | IO | B3 |

### 4.3.9 HDQ Interface

**Table 4-35. HDQ Signal Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| hdq_sio | HDQ 1W Data IO | IOD | K24 |

### 4.3.10 I2C Interfaces

**Table 4-36. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| I2C0_SCL | I2C0 Clock | IOD | Y22 |
| I2C0_SDA | I2C0 Data | IOD | AB24 |

**Table 4-37. I2C1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| I2C1_SCL | I2C1 Clock | IOD | AB18, B13, G20, J25, L21, N20, T20 |
| I2C1_SDA | I2C1 Data | IOD | AE18, B14, E25, K21, L25, T21, T23 |

**Table 4-38. I2C2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| I2C2_SCL | I2C2 Clock | IOD | AB19, AC21, J24, L22, T22 |
| I2C2_SDA | I2C2 Data | IOD | AB20, AC20, K22, K25, P23 |

### 4.3.11 McASP Interfaces

**Table 4-39. McASP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mcasp0_aclkr | McASP0 Receive Bit Clock | IO | A15, A3, C19, L23 |
| mcasp0_aclkx | McASP0 Transmit Bit Clock | IO | A19, D14, E11, F7, N24 |
| mcasp0_ahclkr | McASP0 Receive Master Clock | IO | B18, M24 |
| mcasp0_ahclkx | McASP0 Transmit Master Clock | IO | C13, D17, L24 |
| mcasp0_fsr | McASP0 Receive Frame Sync | IO | A12, C16, D19, K23 |
| mcasp0_fsx | McASP0 Transmit Frame Sync | IO | B19, B4, C11, D13, N22 |
| mcasp0_axr0 | McASP0 Serial Data (IN/OUT) | IO | A18, B11, C14, G8, H23 |
| mcasp0_axr1 | McASP0 Serial Data (IN/OUT) | IO | A11, C17, D8, E16, M25 |
| mcasp0_axr2 | McASP0 Serial Data (IN/OUT) | IO | B18, C19, D16, L23, M24 |
| mcasp0_axr3 | McASP0 Serial Data (IN/OUT) | IO | D17, D19, F17, K23, L24 |

**Table 4-40. McASP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mcasp1_aclkr | McASP1 Receive Bit Clock | IO | B15, F17 |
| mcasp1_aclkx | McASP1 Transmit Bit Clock | IO | A15, B14, L23 |
| mcasp1_ahclkr | McASP1 Receive Master Clock | IO | F17 |
| mcasp1_ahclkx | McASP1 Transmit Master Clock | IO | A16, F17 |
| mcasp1_fsr | McASP1 Receive Frame Sync | IO | A14, B16 |
| mcasp1_fsx | McASP1 Transmit Frame Sync | IO | B13, C16, K23 |
| mcasp1_axr0 | McASP1 Serial Data (IN/OUT) | IO | A13, C13, M25 |
| mcasp1_axr1 | McASP1 Serial Data (IN/OUT) | IO | A14, L24 |
| mcasp1_axr2 | McASP1 Serial Data (IN/OUT) | IO | B15, D16 |
| mcasp1_axr3 | McASP1 Serial Data (IN/OUT) | IO | A16, B16 |

### 4.3.12 Miscellaneous

**Table 4-41. Miscellaneous Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| clkout1 | Clock out1 | O | D24 |
| clkout2 | Clock out2 | O | C24 |
| clkreq | Clock Request Control | O | H20 |
| nNMI | External Interrupt to ARM Cortex A9 core | I | G25 |
| nRESETIN_OUT | Warm Reset Input/Output | IOD (1) | G22 |
| OSC0_IN | High frequency oscillator input | I | C25 |
| OSC0_OUT | High frequency oscillator output | O | B25 |
| OSC1_IN | Low frequency (32.768 KHz) Real Time Clock oscillator input | I | AE5 |
| OSC1_OUT | Low frequency (32.768 KHz) Real Time Clock oscillator output | O | AE4 |
| porz | Power on Reset | I | Y23 |
| RTC_PORz | RTC active low reset input | I | AE6 |
| tclkin | Timer Clock In | I | C24 |
| xdma_event_intr0 | External DMA Event or Interrupt 0 | I | D24 |
| xdma_event_intr1 | External DMA Event or Interrupt 1 | I | C24 |
| xdma_event_intr2 | External DMA Event or Interrupt 2 | I | A16, G24, R25 |
| xdma_event_intr3 | External DMA Event or Interrupt 3 | I | AD24 |
| xdma_event_intr4 | External DMA Event or Interrupt 4 | I | AD25 |
| xdma_event_intr5 | External DMA Event or Interrupt 5 | I | AC23 |
| xdma_event_intr6 | External DMA Event or Interrupt 6 | I | AE21 |
| xdma_event_intr7 | External DMA Event or Interrupt 7 | I | AC25 |
| xdma_event_intr8 | External DMA Event or Interrupt 8 | I | AB25 |

(1) Refer to the External Warm Reset section of the Technical Reference Manual for more information related to the operation of this terminal.

**Table 4-42. Reserved Signals**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| Reserved | | NA | AA10, AA7, AA9, AB10, AB6, AB7, AB9, AC10, AC12, AC5, AC6, AC7, AC9, AD1, AD10, AD11, AD2, AD7, AE11, AE12, AE9, H19, H21, W10, Y10, Y6, Y7 |

### 4.3.13 PRU-ICSS0 Interface

**Table 4-43. PRU-ICSS0-PRU0/General Purpose Inputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr0_pru0_gpi0 | PRU-ICSS0 PRU0 Data In | I | N24 |
| pr0_pru0_gpi1 | PRU-ICSS0 PRU0 Data In | I | N22 |
| pr0_pru0_gpi2 | PRU-ICSS0 PRU0 Data In | I | H23 |
| pr0_pru0_gpi3 | PRU-ICSS0 PRU0 Data In | I | M24 |
| pr0_pru0_gpi4 | PRU-ICSS0 PRU0 Data In | I | L23 |
| pr0_pru0_gpi5 | PRU-ICSS0 PRU0 Data In | I | K23 |
| pr0_pru0_gpi6 | PRU-ICSS0 PRU0 Data In | I | M25 |
| pr0_pru0_gpi7 | PRU-ICSS0 PRU0 Data In | I | L24 |
| pr0_pru0_gpi8 | PRU-ICSS0 PRU0 Data In | I | B1 |
| pr0_pru0_gpi9 | PRU-ICSS0 PRU0 Data In | I | B2 |
| pr0_pru0_gpi10 | PRU-ICSS0 PRU0 Data In | I | C2 |
| pr0_pru0_gpi11 | PRU-ICSS0 PRU0 Data In | I | C1 |
| pr0_pru0_gpi12 | PRU-ICSS0 PRU0 Data In | I | D1 |
| pr0_pru0_gpi13 | PRU-ICSS0 PRU0 Data In | I | D2 |
| pr0_pru0_gpi14 | PRU-ICSS0 PRU0 Data In | I | AC20 |
| pr0_pru0_gpi15 | PRU-ICSS0 PRU0 Data In | I | AB19 |
| pr0_pru0_gpi16 | PRU-ICSS0 PRU0 Data In Capture Enable | I | AA19 |
| pr0_pru0_gpi17 | PRU-ICSS0 PRU0 Data In | I | AC24 |
| pr0_pru0_gpi18 | PRU-ICSS0 PRU0 Data In | I | H25 |
| pr0_pru0_gpi19 | PRU-ICSS0 PRU0 Data In | I | H24 |

**Table 4-44. PRU-ICSS0-PRU0/General Purpose Outputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr0_pru0_gpo0 | PRU-ICSS0 PRU0 Data Out | O | N24 |
| pr0_pru0_gpo1 | PRU-ICSS0 PRU0 Data Out | O | N22 |
| pr0_pru0_gpo2 | PRU-ICSS0 PRU0 Data Out | O | H23 |
| pr0_pru0_gpo3 | PRU-ICSS0 PRU0 Data Out | O | M24 |
| pr0_pru0_gpo4 | PRU-ICSS0 PRU0 Data Out | O | L23 |
| pr0_pru0_gpo5 | PRU-ICSS0 PRU0 Data Out | O | K23 |
| pr0_pru0_gpo6 | PRU-ICSS0 PRU0 Data Out | O | M25 |
| pr0_pru0_gpo7 | PRU-ICSS0 PRU0 Data Out | O | L24 |
| pr0_pru0_gpo8 | PRU-ICSS0 PRU0 Data Out | O | B1 |
| pr0_pru0_gpo9 | PRU-ICSS0 PRU0 Data Out | O | B2 |
| pr0_pru0_gpo10 | PRU-ICSS0 PRU0 Data Out | O | C2 |
| pr0_pru0_gpo11 | PRU-ICSS0 PRU0 Data Out | O | C1 |
| pr0_pru0_gpo12 | PRU-ICSS0 PRU0 Data Out | O | D1 |
| pr0_pru0_gpo13 | PRU-ICSS0 PRU0 Data Out | O | D2 |
| pr0_pru0_gpo14 | PRU-ICSS0 PRU0 Data Out | O | AC20 |
| pr0_pru0_gpo15 | PRU-ICSS0 PRU0 Data Out | O | AB19 |
| pr0_pru0_gpo16 | PRU-ICSS0 PRU0 Data Out | O | AA19 |
| pr0_pru0_gpo17 | PRU-ICSS0 PRU0 Data Out | O | AC24 |
| pr0_pru0_gpo18 | PRU-ICSS0 PRU0 Data Out | O | H25 |
| pr0_pru0_gpo19 | PRU-ICSS0 PRU0 Data Out | O | H24 |

**Table 4-45. PRU-ICSS0-PRU1/General Purpose Inputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr0_pru1_gpi0 | PRU-ICSS0 PRU1 Data In | I | AD24 |
| pr0_pru1_gpi1 | PRU-ICSS0 PRU1 Data In | I | AD25 |
| pr0_pru1_gpi2 | PRU-ICSS0 PRU1 Data In | I | AC23 |
| pr0_pru1_gpi3 | PRU-ICSS0 PRU1 Data In | I | AE21 |
| pr0_pru1_gpi4 | PRU-ICSS0 PRU1 Data In | I | K25 |
| pr0_pru1_gpi5 | PRU-ICSS0 PRU1 Data In | I | J24 |
| pr0_pru1_gpi6 | PRU-ICSS0 PRU1 Data In | I | B23 |
| pr0_pru1_gpi7 | PRU-ICSS0 PRU1 Data In | I | A23 |
| pr0_pru1_gpi8 | PRU-ICSS0 PRU1 Data In | I | A22 |
| pr0_pru1_gpi9 | PRU-ICSS0 PRU1 Data In | I | A24 |
| pr0_pru1_gpi10 | PRU-ICSS0 PRU1 Data In | I | AD21 |
| pr0_pru1_gpi11 | PRU-ICSS0 PRU1 Data In | I | AE22 |
| pr0_pru1_gpi12 | PRU-ICSS0 PRU1 Data In | I | AD22 |
| pr0_pru1_gpi13 | PRU-ICSS0 PRU1 Data In | I | AE23 |
| pr0_pru1_gpi14 | PRU-ICSS0 PRU1 Data In | I | AD23 |
| pr0_pru1_gpi15 | PRU-ICSS0 PRU1 Data In | I | AE24 |
| pr0_pru1_gpi16 | PRU-ICSS0 PRU1 Data In Capture Enable | I | AE18 |
| pr0_pru1_gpi17 | PRU-ICSS0 PRU1 Data In | I | AB18 |
| pr0_pru1_gpi18 | PRU-ICSS0 PRU1 Data In | I | H22 |
| pr0_pru1_gpi19 | PRU-ICSS0 PRU1 Data In | I | K24 |

**Table 4-46. PRU-ICSS0-PRU1/General Purpose Outputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr0_pru1_gpo0 | PRU-ICSS0 PRU1 Data Out | O | AD24 |
| pr0_pru1_gpo1 | PRU-ICSS0 PRU1 Data Out | O | AD25 |
| pr0_pru1_gpo2 | PRU-ICSS0 PRU1 Data Out | O | AC23 |
| pr0_pru1_gpo3 | PRU-ICSS0 PRU1 Data Out | O | AE21 |
| pr0_pru1_gpo4 | PRU-ICSS0 PRU1 Data Out | O | K25 |
| pr0_pru1_gpo5 | PRU-ICSS0 PRU1 Data Out | O | J24 |
| pr0_pru1_gpo6 | PRU-ICSS0 PRU1 Data Out | O | B23 |
| pr0_pru1_gpo7 | PRU-ICSS0 PRU1 Data Out | O | A23 |
| pr0_pru1_gpo8 | PRU-ICSS0 PRU1 Data Out | O | A22 |
| pr0_pru1_gpo9 | PRU-ICSS0 PRU1 Data Out | O | A24 |
| pr0_pru1_gpo10 | PRU-ICSS0 PRU1 Data Out | O | AD21 |
| pr0_pru1_gpo11 | PRU-ICSS0 PRU1 Data Out | O | AE22 |
| pr0_pru1_gpo12 | PRU-ICSS0 PRU1 Data Out | O | AD22 |
| pr0_pru1_gpo13 | PRU-ICSS0 PRU1 Data Out | O | AE23 |
| pr0_pru1_gpo14 | PRU-ICSS0 PRU1 Data Out | O | AD23 |
| pr0_pru1_gpo15 | PRU-ICSS0 PRU1 Data Out | O | AE24 |
| pr0_pru1_gpo16 | PRU-ICSS0 PRU1 Data Out | O | AE18 |
| pr0_pru1_gpo17 | PRU-ICSS0 PRU1 Data Out | O | AB18 |
| pr0_pru1_gpo18 | PRU-ICSS0 PRU1 Data Out | O | H22 |
| pr0_pru1_gpo19 | PRU-ICSS0 PRU1 Data Out | O | K24 |

**Table 4-47. PRU-ICSS0/UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr0_uart0_cts_n | UART Clear to Send | I | P23 |
| pr0_uart0_rts_n | UART Request to Send | O | T22 |
| pr0_uart0_rxd | UART Receive Data | I | T21 |
| pr0_uart0_txd | UART Transmit Data | O | T20 |

### 4.3.14 PRU-ICSS1 Interface

**Table 4-48. PRU-ICSS1-PRU0/General Purpose Inputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_pru0_gpi0 | PRU-ICSS1 PRU0 Data In | I | B22 |
| pr1_pru0_gpi1 | PRU-ICSS1 PRU0 Data In | I | A21 |
| pr1_pru0_gpi2 | PRU-ICSS1 PRU0 Data In | I | B21 |
| pr1_pru0_gpi3 | PRU-ICSS1 PRU0 Data In | I | C21 |
| pr1_pru0_gpi4 | PRU-ICSS1 PRU0 Data In | I | A20 |
| pr1_pru0_gpi5 | PRU-ICSS1 PRU0 Data In | I | B20 |
| pr1_pru0_gpi6 | PRU-ICSS1 PRU0 Data In | I | C20 |
| pr1_pru0_gpi7 | PRU-ICSS1 PRU0 Data In | I | E19 |
| pr1_pru0_gpi8 | PRU-ICSS1 PRU0 Data In | I | B9 |
| pr1_pru0_gpi9 | PRU-ICSS1 PRU0 Data In | I | F10 |
| pr1_pru0_gpi10 | PRU-ICSS1 PRU0 Data In | I | E11 |
| pr1_pru0_gpi11 | PRU-ICSS1 PRU0 Data In | I | C11 |
| pr1_pru0_gpi16 | PRU-ICSS1 PRU0 Data In Capture Enable | I | B11, C24, D24, K21, L21 |

**Table 4-49. PRU-ICSS1-PRU0/General Purpose Outputs Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_pru0_gpo0 | PRU-ICSS1 PRU0 Data Out | O | B22 |
| pr1_pru0_gpo1 | PRU-ICSS1 PRU0 Data Out | O | A21 |
| pr1_pru0_gpo2 | PRU-ICSS1 PRU0 Data Out | O | B21 |
| pr1_pru0_gpo3 | PRU-ICSS1 PRU0 Data Out | O | C21 |
| pr1_pru0_gpo4 | PRU-ICSS1 PRU0 Data Out | O | A20 |
| pr1_pru0_gpo5 | PRU-ICSS1 PRU0 Data Out | O | B20 |
| pr1_pru0_gpo6 | PRU-ICSS1 PRU0 Data Out | O | C20 |
| pr1_pru0_gpo7 | PRU-ICSS1 PRU0 Data Out | O | E19 |
| pr1_pru0_gpo8 | PRU-ICSS1 PRU0 Data Out | O | B9 |
| pr1_pru0_gpo9 | PRU-ICSS1 PRU0 Data Out | O | F10 |
| pr1_pru0_gpo10 | PRU-ICSS1 PRU0 Data Out | O | E11 |
| pr1_pru0_gpo11 | PRU-ICSS1 PRU0 Data Out | O | C11 |

**Table 4-50. PRU-ICSS1/ECAT Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_edio_latch_in | Latch In | I | AE23 |
| pr1_edio_outvalid | Data Out Valid | O | AD18 |
| pr1_edio_sof | Start of Frame | O | AB25, AE17 |
| pr1_edc_latch0_in | Data In | I | AE22, K22 |
| pr1_edc_latch1_in | Data In | I | AD22, L22 |
| pr1_edc_sync0_out | Data Out | O | L25 |
| pr1_edc_sync1_out | Data Out | O | J25 |
| pr1_edio_data_in0 | Data In | I | AD23 |
| pr1_edio_data_in1 | Data In | I | AE24 |
| pr1_edio_data_in2 | Data In | I | B23 |
| pr1_edio_data_in3 | Data In | I | A23 |
| pr1_edio_data_in4 | Data In | I | A22 |
| pr1_edio_data_in5 | Data In | I | A24 |

**Table 4-50. PRU-ICSS1/ECAT Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_edio_data_in6 | Data In | I | B9, C20 |
| pr1_edio_data_in7 | Data In | I | E19, F10 |
| pr1_edio_data_out0 | Data Out | O | T21 |
| pr1_edio_data_out1 | Data Out | O | T20 |
| pr1_edio_data_out2 | Data Out | O | B23 |
| pr1_edio_data_out3 | Data Out | O | A23 |
| pr1_edio_data_out4 | Data Out | O | A22 |
| pr1_edio_data_out5 | Data Out | O | A24 |
| pr1_edio_data_out6 | Data Out | O | B9, C20 |
| pr1_edio_data_out7 | Data Out | O | E19, F10 |

**Table 4-51. PRU-ICSS1/MDIO Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_mdio_data | MDIO Data | IO | A17, B12, D24 |
| pr1_mdio_mdclk | MDIO Clk | O | A12, B17, C24 |

**Table 4-52. PRU-ICSS1/MII0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_mii0_col | MII Collision Detect | I | A10, D25 |
| pr1_mii0_crs | MII Carrier Sense | I | B12, G20 |
| pr1_mii0_rxdv | MII Receive Data Valid | I | D17 |
| pr1_mii0_rxer | MII Receive Data Error | I | D19 |
| pr1_mii0_rxlink | MII Receive Link | I | C19, E25 |
| pr1_mii0_txen | MII Transmit Enable | O | A21, F11 |
| pr1_mii0_rxd0 | MII Receive Data bit 0 | I | B18 |
| pr1_mii0_rxd1 | MII Receive Data bit 1 | I | A18 |
| pr1_mii0_rxd2 | MII Receive Data bit 2 | I | B19 |
| pr1_mii0_rxd3 | MII Receive Data bit 3 | I | A19 |
| pr1_mii0_txd0 | MII Transmit Data bit 0 | O | B11, B20 |
| pr1_mii0_txd1 | MII Transmit Data bit 1 | O | A20, C11 |
| pr1_mii0_txd2 | MII Transmit Data bit 2 | O | C21, E11 |
| pr1_mii0_txd3 | MII Transmit Data bit 3 | O | B21, D11 |
| pr1_mii_mr0_clk | MII Receive Clock | I | C17 |
| pr1_mii_mt0_clk | MII Transmit Clock | I | B10, B22 |

**Table 4-53. PRU-ICSS1/MII1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_mii1_col | MII Collision Detect | I | A3, F24 |
| pr1_mii1_crs | MII Carrier Sense | I | A12, A2, F23 |
| pr1_mii1_rxdv | MII Receive Data Valid | I | C5 |
| pr1_mii1_rxer | MII Receive Data Error | I | B3 |
| pr1_mii1_rxlink | MII Receive Link | I | C10, E24 |
| pr1_mii1_txen | MII Transmit Enable | O | C3 |
| pr1_mii1_rxd0 | MII Receive Data bit 0 | I | D8 |
| pr1_mii1_rxd1 | MII Receive Data bit 1 | I | G8 |
| pr1_mii1_rxd2 | MII Receive Data bit 2 | I | B4 |

**Table 4-53. PRU-ICSS1/MII1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_mii1_rxd3 | MII Receive Data bit 3 | I | F7 |
| pr1_mii1_txd0 | MII Transmit Data bit 0 | O | E7 |
| pr1_mii1_txd1 | MII Transmit Data bit 1 | O | D7 |
| pr1_mii1_txd2 | MII Transmit Data bit 2 | O | A4 |
| pr1_mii1_txd3 | MII Transmit Data bit 3 | O | C6 |
| pr1_mii_mr1_clk | MII Receive Clock | I | F6 |
| pr1_mii_mt1_clk | MII Transmit Clock | I | E8 |

**Table 4-54. PRU-ICSS1/UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_uart0_cts_n | UART Clear to Send | I | K22, P23 |
| pr1_uart0_rts_n | UART Request to Send | O | L22, T22 |
| pr1_uart0_rxd | UART Receive Data | I | K21, T21 |
| pr1_uart0_txd | UART Transmit Data | O | L21, T20 |

**Table 4-55. PRU-ICSS1/eCAP Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| pr1_ecap0_ecap_capin_apwm_o | Enhanced capture input or Auxiliary PWM out | IO | A11, G24 |

### 4.3.15 QSPI Interface

**Table 4-56. QSPI Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| qspi_clk | QSPI Clock | IO | B12, Y18 |
| qspi_csn | QSPI Chip Select | O | A8, AA18 |
| qspi_d0 | QSPI Data | IO | A9, AE19 |
| qspi_d1 | QSPI Data | I | AD19, E10 |
| qspi_d2 | QSPI Data | I | AE20, D10 |
| qspi_d3 | QSPI Data | I | AD20, C10 |

### 4.3.16 RTC Subsystem Interface

**Table 4-57. RTC Subsystem Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| RTC_KALDO_ENn | Active low enable input for internal CAP_VDD_RTC voltage regulator | I | AE2 |
| RTC_PMIC_EN | PMIC Power Enable output generated from Generic RTCSS | O | AD6 |
| RTC_WAKEUP | External Wakeup Pin when Generic RTC is used | I | AE3 |

### 4.3.17 Removable Media Interfaces

**Table 4-58. MMC0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mmc0_clk | MMC/SD/SDIO Clock | IO | D1 |
| mmc0_cmd | MMC/SD/SDIO Command | IO | D2 |
| mmc0_pow | MMC/SD Power Switch Control | O | A16, R25 |
| mmc0_sdcd | SD Card Detect | I | A17, N24, R25 |
| mmc0_sdwp | SD Write Protect | I | B17, G24, L23 |
| mmc0_dat0 | MMC/SD/SDIO Data Bus | IO | C1 |
| mmc0_dat1 | MMC/SD/SDIO Data Bus | IO | C2 |
| mmc0_dat2 | MMC/SD/SDIO Data Bus | IO | B2 |
| mmc0_dat3 | MMC/SD/SDIO Data Bus | IO | B1 |
| mmc0_dat4 | MMC/SD/SDIO Data Bus | IO | E16 |
| mmc0_dat5 | MMC/SD/SDIO Data Bus | IO | C14 |
| mmc0_dat6 | MMC/SD/SDIO Data Bus | IO | D13 |
| mmc0_dat7 | MMC/SD/SDIO Data Bus | IO | D14 |

**Table 4-59. MMC1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mmc1_clk | MMC/SD/SDIO Clock | IO | B15, B17, B9, Y18 |
| mmc1_cmd | MMC/SD/SDIO Command | IO | A14, A17, AA18, F10 |
| mmc1_sdcd | SD Card Detect | I | A2, N22 |
| mmc1_sdwp | SD Write Protect | I | K21, T21 |
| mmc1_dat0 | MMC/SD/SDIO Data Bus | IO | AE19, B10, B5, D14 |
| mmc1_dat1 | MMC/SD/SDIO Data Bus | IO | A10, A5, AD19, D13 |
| mmc1_dat2 | MMC/SD/SDIO Data Bus | IO | AE20, B6, C14, F11 |
| mmc1_dat3 | MMC/SD/SDIO Data Bus | IO | A6, AD20, D11, E16 |
| mmc1_dat4 | MMC/SD/SDIO Data Bus | IO | B7, E11 |
| mmc1_dat5 | MMC/SD/SDIO Data Bus | IO | A7, C11 |
| mmc1_dat6 | MMC/SD/SDIO Data Bus | IO | B11, C8 |
| mmc1_dat7 | MMC/SD/SDIO Data Bus | IO | A11, B8 |

**Table 4-60. MMC2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| mmc2_clk | MMC/SD/SDIO Clock | IO | A12, AD21, B16, B17 |
| mmc2_cmd | MMC/SD/SDIO Command | IO | A13, A17, AE22, B12 |
| mmc2_sdcd | SD Card Detect | I | B3, H23 |
| mmc2_sdwp | SD Write Protect | I | L21, T20 |
| mmc2_dat0 | MMC/SD/SDIO Data Bus | IO | A15, AD22, C5, E11 |
| mmc2_dat1 | MMC/SD/SDIO Data Bus | IO | AE23, C11, C16, C6 |
| mmc2_dat2 | MMC/SD/SDIO Data Bus | IO | A4, AD23, B11, C13 |
| mmc2_dat3 | MMC/SD/SDIO Data Bus | IO | A11, A3, AE24, D16 |
| mmc2_dat4 | MMC/SD/SDIO Data Bus | IO | B10, E8 |
| mmc2_dat5 | MMC/SD/SDIO Data Bus | IO | A10, F6 |
| mmc2_dat6 | MMC/SD/SDIO Data Bus | IO | F11, F7 |
| mmc2_dat7 | MMC/SD/SDIO Data Bus | IO | B4, D11 |

### 4.3.18 SPI Interfaces

**Table 4-61. SPI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| spi0_sclk | SPI Clock | IO | P23 |
| spi0_cs0 | SPI Chip Select | IO | T20 |
| spi0_cs1 | SPI Chip Select | IO | R25 |
| spi0_cs2 | SPI Chip Select | IO | AD24, C24, E10 |
| spi0_cs3 | SPI Chip Select | IO | A9, AD25, N24 |
| spi0_d0 | SPI Data | IO | T22 |
| spi0_d1 | SPI Data | IO | T21 |

**Table 4-62. SPI1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| spi1_sclk | SPI Clock | IO | D16, G24, N24 |
| spi1_cs0 | SPI Chip Select | IO | A16, J25, K22, K25, M24 |
| spi1_cs1 | SPI Chip Select | IO | D24, G24, J24, L22 |
| spi1_cs2 | SPI Chip Select | IO | AC23, D10, N22 |
| spi1_cs3 | SPI Chip Select | IO | AE21, C10, H23 |
| spi1_d0 | SPI Data | IO | B14, L25, N22 |
| spi1_d1 | SPI Data | IO | B13, H23, J25 |

**Table 4-63. SPI2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| spi2_sclk | SPI Clock | IO | AC18, AE21, N20 |
| spi2_cs0 | SPI Chip Select | IO | AC20, AD25, T23 |
| spi2_cs1 | SPI Chip Select | IO | AC25, AE17 |
| spi2_cs2 | SPI Chip Select | IO | AB19, AC23 |
| spi2_cs3 | SPI Chip Select | IO | AA19, AC24 |
| spi2_d0 | SPI Data | IO | AD17, AD24, P22 |
| spi2_d1 | SPI Data | IO | AB25, AD18, P20 |

**Table 4-64. SPI3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| spi3_sclk | SPI Clock | IO | AE22, B10, C19 |
| spi3_cs0 | SPI Chip Select | IO | AD21, D11, D17 |
| spi3_cs1 | SPI Chip Select | IO | A11, B10, B18, C10 |
| spi3_d0 | SPI Data | IO | A10, AB20, D19 |
| spi3_d1 | SPI Data | IO | AC21, C17, F11 |

**Table 4-65. SPI4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| spi4_sclk | SPI Clock | IO | P25 |
| spi4_cs0 | SPI Chip Select | IO | N25 |
| spi4_cs1 | SPI Chip Select | IO | H22 |
| spi4_d0 | SPI Data | IO | R24 |
| spi4_d1 | SPI Data | IO | P24 |

### 4.3.19 Timer Interfaces

**Table 4-66. Timer0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer0 | Timer trigger event / PWM out | IO | R25 |

**Table 4-67. Timer1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer1 | Timer trigger event / PWM out | IO | G24 |

**Table 4-68. Timer4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer4 | Timer trigger event / PWM out | IO | A13, A9, AB24, D24 |

**Table 4-69. Timer5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer5 | Timer trigger event / PWM out | IO | B1, B17, C10, L22 |

**Table 4-70. Timer6 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer6 | Timer trigger event / PWM out | IO | A17, B2, D10, K22 |

**Table 4-71. Timer7 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| timer7 | Timer trigger event / PWM out | IO | C24, E10, L25, Y22 |

### 4.3.20 UART Interfaces

**Table 4-72. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart0_ctsn | UART Clear to Send | I | AC24, L25 |
| uart0_dcdn | UART Data Carrier Detect | I | AD22 |
| uart0_rtsn | UART Request to Send | O | AD24, J25 |
| uart0_rxd | UART Receive Data | I | K25 |
| uart0_txd | UART Transmit Data | O | J24 |

**Table 4-73. UART1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart1_ctsn | UART Clear to Send | IO | AD21, K22 |
| uart1_dcdn | UART Clear to Send | I | AD23, B1, D14 |
| uart1_dsrn | UART Request to Send | I | AE23, B2, D13 |
| uart1_dtrn | UART Receive Data | O | AE24, C14, C2 |
| uart1_rin | UART Transmit Data | I | AD22, C1, E16 |
| uart1_rtsn | UART Request to Send | O | AE22, L22 |
| uart1_rxd | UART Receive Data | IO | AB20, K21 |
| uart1_txd | UART Transmit Data | IO | AC21, L21 |

**Table 4-74. UART2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart2_ctsn | UART Clear to Send | IO | A19, AB24, AD23 |
| uart2_rtsn | UART Request to Send | O | AE24, B19, Y22 |
| uart2_rxd | UART Receive Data | IO | AD22, B14, D1, D14, P23 |
| uart2_txd | UART Transmit Data | IO | AE23, B13, D13, D2, T22 |

**Table 4-75. UART3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart3_ctsn | UART Clear to Send | IO | A17, A18, D1, H22 |
| uart3_rtsn | UART Request to Send | O | B17, B18, D2, K24 |
| uart3_rxd | UART Receive Data | IO | C14, C2, H25, R25 |
| uart3_txd | UART Transmit Data | IO | C1, E16, G24, H24 |

**Table 4-76. UART4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart4_ctsn | UART Clear to Send | I | B1, C19 |
| uart4_rtsn | UART Request to Send | O | B2, D19 |
| uart4_rxd | UART Receive Data | I | A2, C16, L25 |
| uart4_txd | UART Transmit Data | O | B3, C13, J25 |

**Table 4-77. UART5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart5_ctsn | UART Clear to Send | I | B14, C17, C2 |
| uart5_rtsn | UART Request to Send | O | B13, C1, D17 |

**Table 4-77. UART5 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| uart5_rxd | UART Receive Data | I | A17, B19, C17, D16 |
| uart5_txd | UART Transmit Data | O | A15, A16, A19, B17 |

### 4.3.21 USB Interfaces

**Table 4-78. USB0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| USB0_CE | USB0 Active high Charger Enable output | A | W22 |
| USB0_DM | USB0 Data minus | A | W24 |
| USB0_DP | USB0 Data plus | A | W25 |
| USB0_DRVVBUS | USB0 Active high VBUS control output | O | G21 |
| USB0_ID | USB0 ID | A | U24 |
| USB0_VBUS | USB0 VBUS | A | U23 |

**Table 4-79. USB1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| USB1_CE | USB1 Active high Charger Enable output | A | U22 |
| USB1_DM | USB1 Data minus | A | V25 |
| USB1_DP | USB1 Data plus | A | V24 |
| USB1_DRVVBUS | USB1 Active high VBUS control output | O | F25 |
| USB1_ID | USB1 ID | A | U25 |
| USB1_VBUS | USB1 VBUS | A | T25 |

### 4.3.22 eCAP Interfaces

**Table 4-80. eCAP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eCAP0_in_PWM0_out | Enhanced Capture 0 input or Auxiliary PWM0 output | IO | G24 |

**Table 4-81. eCAP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eCAP1_in_PWM1_out | Enhanced Capture 1 input or Auxiliary PWM1 output | IO | J24, R25, Y22 |

**Table 4-82. eCAP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eCAP2_in_PWM2_out | Enhanced Capture 2 input or Auxiliary PWM2 output | IO | AB24, K25, M24 |

### 4.3.23 eHRPWM Interfaces

**Table 4-83. eHRPWM0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm0_synci | Sync input to eHRPWM0 module from an external pin | I | AC21, M24, P25, T20 |
| ehrpwm0_synco | Sync Output from eHRPWM0 module to an external pin | O | AE18, B19, C21, C5, D11 |
| ehrpwm0_tripzone_input | eHRPWM0 trip zone input | I | AB20, H23, P24, T21 |
| ehrpwm0A | eHRPWM0 A output. | O | AD25, N24, P23 |
| ehrpwm0B | eHRPWM0 B output. | O | AC23, N22, T22 |

**Table 4-84. eHRPWM1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm1_tripzone_input | eHRPWM1 trip zone input | I | A19, AD21, C3, P20 |
| ehrpwm1A | eHRPWM1 A output. | O | A18, AE20, AE21, C6, T21 |
| ehrpwm1B | eHRPWM1 B output. | O | A4, AC25, AD20, B18, T20 |

**Table 4-85. eHRPWM2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm2_tripzone_input | eHRPWM2 trip zone input | I | B21, F11, T23 |
| ehrpwm2A | eHRPWM2 A output. | O | B10, B22, R25 |
| ehrpwm2B | eHRPWM2 B output. | O | A10, A21, G24 |

**Table 4-86. eHRPWM3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm3_synci | Sync input to eHRPWM3 module or sync output to external PWM | I | R24 |
| ehrpwm3_synco | Sync input to eHRPWM3 module or sync output to external PWM | O | AB18 |
| ehrpwm3_tripzone_input | eHRPWM3 trip zone input | I | N25 |
| ehrpwm3A | eHRPWM3 A output. | O | AC25, AE19 |
| ehrpwm3B | eHRPWM3 B output. | O | AB25, AD19 |

**Table 4-87. eHRPWM4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm4_tripzone_input | eHRPWM4 trip zone input | I | N20 |
| ehrpwm4A | eHRPWM4 A output. | O | H25 |
| ehrpwm4B | eHRPWM4 B output. | O | H24 |

**Table 4-88. eHRPWM5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| ehrpwm5_tripzone_input | eHRPWM5 trip zone input | I | P22 |
| ehrpwm5A | eHRPWM5 A output. | O | H22 |
| ehrpwm5B | eHRPWM5 B output. | O | K24 |

### 4.3.24 eQEP Interfaces

**Table 4-89. eQEP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eQEP0_index | eQEP0 index. | IO | A13, M25 |
| eQEP0_strobe | eQEP0 strobe. | IO | B16, L24 |
| eQEP0A_in | eQEP0A quadrature input | I | A14, L23 |
| eQEP0B_in | eQEP0B quadrature input | I | B15, K23 |

**Table 4-90. eQEP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eQEP1_index | eQEP1 index. | IO | C17, E8 |
| eQEP1_strobe | eQEP1 strobe. | IO | D17, F6 |
| eQEP1A_in | eQEP1A quadrature input | I | C19, D7 |
| eQEP1B_in | eQEP1B quadrature input | I | D19, E7 |

**Table 4-91. eQEP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZDN [4] |
|---|---|---|---|
| eQEP2_index | eQEP2 index. | IO | B11, C20 |
| eQEP2_strobe | eQEP2 strobe. | IO | A11, E19 |
| eQEP2A_in | eQEP2A quadrature input | I | A20, E11 |
| eQEP2B_in | eQEP2B quadrature input | I | B20, C11 |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)[1][2]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VDD_MPU | Supply voltage for the MPU domain | | –0.5 | 1.5 | V |
| VDD_CORE | Supply voltage range for the CORE domain | | –0.5 | 1.5 | V |
| CAP_VDD_RTC[3] | Supply voltage range for the RTC domain | | –0.5 | 1.5 | V |
| VDDS_RTC | Supply voltage range for the RTC domain | | –0.5 | 2.1 | V |
| VDDS_OSC | Supply voltage range for the System oscillator | | –0.5 | 2.1 | V |
| VDDS_SRAM_CORE_BG | Supply voltage range for the Core SRAM and Bandgap LDOs | | –0.5 | 2.1 | V |
| VDDS_SRAM_MPU_BB | Supply voltage range for the MPU SRAM and BB LDOs | | –0.5 | 2.1 | V |
| VDDS_PLL_DDR | Supply voltage range for the DPLL DDR | | –0.5 | 2.1 | V |
| VDDS_PLL_CORE_LCD | Supply voltage range for the DPLL CORE, EXTDEV, and LCD | | –0.5 | 2.1 | V |
| VDDS_PLL_MPU | Supply voltage range for the DPLL MPU | | –0.5 | 2.1 | V |
| VDDS_DDR | Supply voltage range for the DDR IO domain | | –0.5 | 2.1 | V |
| VDDS | Supply voltage range for all dual-voltage IO domains | | –0.5 | 2.1 | V |
| VDDA1P8V_USB0 | Supply voltage range for USBPHY and DPLL PER | | –0.5 | 2.1 | V |
| VDDA1P8V_USB1 | Supply voltage range for USBPHY | | –0.5 | 2.1 | V |
| VDDA_ADC0 | Supply voltage range for ADC0 | | –0.5 | 2.1 | V |
| VDDA_ADC1 | Supply voltage range for ADC1 | | –0.5 | 2.1 | V |
| VDDSHV1 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV2 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV3 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV5 | Supply voltage range for the CLKOUT voltage domain | | –0.5 | 3.8 | V |
| VDDSHV6 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV7 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV8 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV9 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV10 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDSHV11 | Supply voltage range for the dual-voltage IO domain | | –0.5 | 3.8 | V |
| VDDA3P3V_USB0 | Supply voltage range for USBPHY | | –0.5 | 4 | V |
| VDDA3P3V_USB1 | Supply voltage range for USBPHY | | –0.5 | 4 | V |
| VDDS3P3V_IOLDO | Supply voltage range for the dual-voltage IO LDO | | –0.5 | 3.8 | V |
| VDDS_CLKOUT | Supply voltage range for CLKOUT domain | | –0.5 | 2.1 | V |
| USB0_VBUS[4] | Supply voltage range for USB VBUS comparator input | | –0.5 | 5.25 | V |
| USB1_VBUS[4] | Supply voltage range for USB VBUS comparator input | | –0.5 | 5.25 | V |
| DDR_VREF | Supply voltage range for the DDR3/DDR3L HSTL, LPDDR2 HSUL_12 reference voltage | | –0.3 | 1.1 | V |
| Steady State Max. Voltage at all IO pins[5] | | | –0.5 V to IO supply voltage + 0.3 V | | |
| USB0_ID[6] | Steady state maximum voltage range for the USB ID input | | –0.5 | 2.1 | V |
| USB1_ID[6] | Steady state maximum voltage range for the USB ID input | | –0.5 | 2.1 | V |
| Transient Overshoot and Undershoot specification at IO terminal | | | 20% of corresponding IO supply voltage for up to 20% of signal period (see Figure 5-1) | | |
| Latch-up Performance[7] | Class II (105°C) | Latch-up I-test performance current-pulse injection on each IO pin | ±100 | | mA |
| | | Latch-up overvoltage performance voltage injection on each IO pin | ±100 | | |
| $T_{stg}$[8] | Storage temperature | | –55 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to their associated VSS or VSSA_x.

## Absolute Maximum Ratings *(continued)*

over junction temperature range (unless otherwise noted)(1)(2)

(3) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.

(4) This terminal is connected to a fail-safe IO and does not have a dependence on any IO supply voltage.

(5) This parameter applies to all IO terminals which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.5 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.

(6) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

(7) For current pulse injection:
Pins stressed per JEDEC JESD78D (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For overvoltage performance:
Supplies stressed per JEDEC JESD78D (Class II) and passed specified voltage injection.

(8) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The USB0_VBUS, USB1_VBUS, and DDR_RESETn are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in Section 5.1.

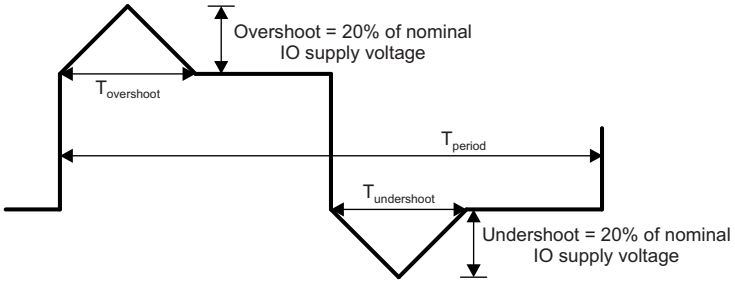



**Figure 5-1. $T_{overshoot}$ + $T_{undershoot}$ < 20% of $T_{period}$**

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge (ESD) | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged device model (CDM), per JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Power-On Hours (POH)(1)(2)(3)(4)

| OPERATING CONDITION | COMMERCIAL | | INDUSTRIAL | | EXTENDED | |
|---|---|---|---|---|---|---|
| | JUNCTION TEMP ($T_j$) | LIFETIME (POH)(5) | JUNCTION TEMP ($T_j$) | LIFETIME (POH)(5) | JUNCTION TEMP ($T_j$) | LIFETIME (POH)(5) |
| Nitro | 0°C to 90°C | 100K | –40°C to 90°C | 100K | –40°C to 105°C | 84.4K |
| Turbo | 0°C to 90°C | 100K | –40°C to 90°C | 100K | –40°C to 105°C | 100K |
| OPP120 | 0°C to 90°C | 100K | –40°C to 90°C | 100K | –40°C to 105°C | 100K |
| OPP100 | 0°C to 90°C | 100K | –40°C to 90°C | 100K | –40°C to 105°C | 100K |
| OPP50 | 0°C to 90°C | 100K | –40°C to 90°C | 100K | –40°C to 105°C | 100K |

(1) The POH information in this table is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) To avoid significant degradation, the device POH must be limited as described in this table.

(3) Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

(4) The previous notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.

(5) POH = Power-on hours when the device is fully functional.

## 5.4 Operating Performance Points

Device operating performance points (OPPs) are defined in 表 5-1, 表 5-2, and 表 5-3.

**表 5-1. VDD_CORE OPPs(1)**

| VDD_CORE OPP | VDD_CORE | | | DDR3/DDR3L(2) | LPDDR2(2) | L3 and L4 |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | | | |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 400 MHz | 266 MHz | 200 MHz and 100 MHz |
| OPP50 | 0.912 V | 0.950 V | 1 V | Not supported | 133 MHz | 100 MHz and 50 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) This parameter represents the maximum memory clock frequency. Because data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

**表 5-2. VDD_MPU OPPs(1)**

| VDD_MPU OPP | VDD_MPU | | | ARM (A9) |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Nitro | 1.272 V | 1.325 V | 1.378 V | 1 GHz |
| Turbo | 1.210 V | 1.260 V | 1.326 V | 800 MHz |
| OPP120 | 1.152 V | 1.200 V | 1.248 V | 720 MHz |
| OPP100 | 1.056 V | 1.100 V | 1.144 V | 600 MHz |
| OPP50 | 0.912 V | 0.950 V | 1.000 V | 300 MHz |

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

**表 5-3. Valid Combinations of VDD_CORE and VDD_MPU OPPs(1)**

| VDD_CORE | VDD_MPU |
|---|---|
| OPP50 | OPP50 |
| OPP100 | OPP50 |
| OPP100 | OPP100 |
| OPP100 | OPP120 |
| OPP100 | Turbo |
| OPP100 | Nitro |

(1) OPP combinations listed in this table have been tested. Other OPP combinations are not supported.

## 5.5 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

| SUPPLY NAME | DESCRIPTION | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDD_CORE | Supply voltage range for core domain; OPP100 | | 1.056 | 1.100 | 1.144 | V |
| | Supply voltage range for core domain; OPP50 | | 0.912 | 0.950 | 1.000 | |
| VDD_MPU | Supply voltage range for MPU domain, Nitro | | 1.272 | 1.325 | 1.378 | V |
| | Supply voltage range for MPU domain; Turbo | | 1.210 | 1.260 | 1.326 | |
| | Supply voltage range for MPU domain; OPP120 | | 1.152 | 1.200 | 1.248 | |
| | Supply voltage range for MPU domain; OPP100 | | 1.056 | 1.100 | 1.144 | |
| | Supply voltage range for MPU domain; OPP50 | | 0.912 | 0.950 | 1.000 | |
| CAP_VDD_RTC(1) | Supply voltage range for RTC core domain | | 0.900 | 1.100 | 1.250 | V |
| VDDS_RTC | Supply voltage range for RTC domain | | 1.710 | 1.800 | 1.890 | V |
| VDDS_DDR | Supply voltage range for DDR IO domain (DDR3) | | 1.425 | 1.500 | 1.575 | V |
| | Supply voltage range for DDR IO domain (DDR3L) | | 1.283 | 1.350 | 1.418 | |
| | Supply voltage range for DDR IO domain (LPDDR2) | | 1.140 | 1.200 | 1.260 | |
| VDDS(2) | Supply voltage range for all dual-voltage IO domains | | 1.710 | 1.800 | 1.890 | V |
| VDDS_SRAM_CORE_BG | Supply voltage range for Core SRAM LDOs, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDS_SRAM_MPU_BB | Supply voltage range for MPU SRAM LDOs, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_DDR(3) | Supply voltage range for DPLL DDR, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_CORE_LCD(3) | Supply voltage range for DPLL CORE, EXTDEV, and LCD, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDS_PLL_MPU(3) | Supply voltage range for DPLL MPU, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDS_OSC | Supply voltage range for system oscillator, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDA1P8V_USB0(3) | Supply voltage range for USBPHY and DPLL PER, Analog, 1.8 V | | 1.710 | 1.800 | 1.890 | V |
| VDDA1P8V_USB1 | Supply voltage range for USBPHY, Analog, 1.8 V | | 1.710 | 1.800 | 1.890 | V |
| VDDA3P3V_USB0 | Supply voltage range for USBPHY, Analog, 3.3 V | | 3.135 | 3.300 | 3.465 | V |
| VDDA3P3V_USB1 | Supply voltage range for USBPHY, Analog, 3.3 V | | 3.135 | 3.300 | 3.465 | V |
| VDDA_ADC0 | Supply voltage range for ADC0, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDA_ADC1 | Supply voltage range for ADC1, Analog | | 1.710 | 1.800 | 1.890 | V |
| VDDSHV1 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV2 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV3 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV5 | Supply voltage range for CLKOUT voltage domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV6 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV7 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV8 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV9 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV10 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| VDDSHV11 | Supply voltage range for dual-voltage IO domain | 1.8-V operation | 1.710 | 1.800 | 1.890 | V |
| | | 3.3-V operation | 3.135 | 3.300 | 3.465 | |
| DDR_VREF | Supply voltage range for the DDR3/DDR3L HSTL, LPDDR2 HSUL_12 reference input | | 0.49 × VDDS_DDR | 0.50 × VDDS_DDR | 0.51 × VDDS_DDR | V |
| VDDS3P3V_IOLDO | Supply voltage range for the dual-voltage IO LDO | | 3.135 | 3.3 | 3.465 | V |
| VDDS_CLKOUT | Supply voltage range for CLKOUT domain | | 1.71 | 1.8 | 1.89 | V |

## Recommended Operating Conditions *(continued)*

over junction temperature range (unless otherwise noted)

| SUPPLY NAME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| USB0_VBUS | Voltage range for USB VBUS comparator input | 0.000 | 5.000 | 5.250 | V |
| USB1_VBUS | Voltage range for USB VBUS comparator input | 0.000 | 5.000 | 5.250 | V |
| USB0_ID | Voltage range for the USB ID input | | (4) | | V |
| USB1_ID | Voltage range for the USB ID input | | (4) | | V |
| Operating Temperature Range, $T_j$ | Commercial Temperature | 0 | | 90 | °C |
| | Industrial Temperature | –40 | | 90 | |
| | Extended Temperature | –40 | | 105 | |

(1) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.

(2) VDDS should be supplied irrespective of 1.8-V or 3.3-V mode of operation of the dual-voltage IOs.

(3) For more details on power supply requirements, see 5.12.2.1.1.

(4) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

## 5.6 Power Consumption Summary

表 5-4 summarizes the maximum power consumption at each power terminal.

**Note:** Data in the Maximum Current Ratings table (表 5-4) represents worst-case power consumption based on various applications of the device using practical operating conditions. The data primarily benefits the power supply designer trying to understand the worst-case power consumption expected from each power rail.

**表 5-4. Maximum Current Ratings at Power Terminals(1)**

| PARAMETER | | | MAX | UNIT |
|---|---|---|---|---|
| SUPPLY NAME | DESCRIPTION | | | |
| VDD_CORE | Maximum current rating for the core domain; OPP100 | | 600 | mA |
| | Maximum current rating for the core domain; OPP50 | | 400 | mA |
| VDD_MPU | Maximum current rating for the MPU domain; Nitro | at 1 GHz | 1000 | mA |
| | Maximum current rating for the MPU domain; Turbo | at 800 MHz | 800 | |
| | Maximum current rating for the MPU domain; OPP120 | at 720 MHz | 720 | |
| | Maximum current rating for the MPU domain; OPP100 | at 600 MHz | 600 | |
| | Maximum current rating for the MPU domain; OPP50 | at 300 MHz | 350 | |
| CAP_VDD_RTC(2) | Maximum current rating for RTC domain and LDO output | | 2 | mA |
| VDDS_RTC | Maximum current rating for the RTC domain | | 5 | mA |
| VDDS_DDR | Maximum current rating for DDR IO domain; DDR3/DDR3L | | 300 | mA |
| | Maximum current rating for DDR IO domain; LPDDR2 | | 150 | |
| VDDS | Maximum current rating for all dual-voltage IO domains | | 70 | mA |
| VDDS_SRAM_CORE_BG | Maximum current rating for core SRAM LDOs | | 10 | mA |
| VDDS_SRAM_MPU_BB | Maximum current rating for MPU SRAM LDOs | | 10 | mA |
| VDDS_PLL_DDR | Maximum current rating for the DPLL DDR | | 10 | mA |
| VDDS_PLL_CORE_LCD | Maximum current rating for the DPLL CORE, EXTDEV, and LCD | | 20 | mA |
| VDDS_PLL_MPU | Maximum current rating for the DPLL MPU | | 10 | mA |
| VDDS_OSC | Maximum current rating for the system oscillator | | 5 | mA |
| VDDA1P8V_USB0 | Maximum current rating for USBPHY 1.8 V and DPLL PER | | 25 | mA |
| VDDA1P8V_USB1 | Maximum current rating for USBPHY 1.8 V | | 25 | mA |
| VDDA3P3V_USB0 | Maximum current rating for USBPHY 3.3 V | | 40 | mA |
| VDDA3P3V_USB1 | Maximum current rating for USBPHY 3.3 V | | 40 | mA |
| VDDS3P3V_IOLDO | Maximum current rating for the dual-voltage IO LDO | | 30 | mA |
| VDDA_ADC0 | Maximum current rating for ADC0 | | 10 | mA |
| VDDA_ADC1 | Maximum current rating for ADC1 | | 10 | mA |
| VDDSHV1 | Maximum current rating for dual-voltage IO domain | | 30 | mA |
| VDDSHV2 | Maximum current rating for dual-voltage IO domain | | 80 | mA |
| VDDSHV3 | Maximum current rating for dual-voltage IO domain | | 100 | mA |
| VDDSHV5 | Maximum current rating for dual-voltage IO domain | | 10 | mA |
| VDDSHV6 | Maximum current rating for dual-voltage IO domain | | 50 | mA |
| VDDSHV7 | Maximum current rating for dual-voltage IO domain | | 10 | mA |
| VDDSHV8 | Maximum current rating for dual-voltage IO domain | | 50 | mA |
| VDDSHV9 | Maximum current rating for dual-voltage IO domain | | 50 | mA |
| VDDSHV10 | Maximum current rating for dual-voltage IO domain | | 50 | mA |
| VDDSHV11 | Maximum current rating for dual-voltage IO domain | | 50 | mA |
| VDDS_CLKOUT | Maximum current rating for CLKOUT domain | | 10 | mA |

(1) Current ratings specified in this table are worst-case estimates. Actual application power supply estimates could be lower. For more information, see *AM43xx Power Consumption Summary*.
(2) This supply is sourced from an internal LDO when RTC_KALDO_ENn is low. If RTC_KALDO_ENn is high, this supply must be sourced from an external power supply.

## 5.7 DC Electrical Characteristics

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)[1]

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DDR_CSn[1:0], DDR_CKE[1:0], DDR_CK, DDR_CKn, DDR_CASn, DDR_RASn, DDR_WEn, DDR_BA[2:0], DDR_A[15:0], DDR_ODT[1:0], DDR_D[31:0], DDR_DQM[3:0], DDR_DQS[3:0], DDR_DQSn[3:0] pins (DDR3/DDR3L - HSTL mode)** | | | | | | |
| $V_{IH}$ | High-level input voltage | VDDS_DDR = 1.5 V | DDR_VREF + 0.1 | | | V |
| | | VDDS_DDR = 1.35 V | DDR_VREF + 0.09 | | | |
| $V_{IL}$ | Low-level input voltage | VDDS_DDR = 1.5 V | | | DDR_VREF – 0.1 | V |
| | | VDDS_DDR = 1.35 V | | | DDR_VREF – 0.09 | |
| $V_{HYS}$ | Hysteresis voltage at an input | | | NA | | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 8 mA | VDDS_DDR – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –10 | | 10 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 40 | | 240 | |
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –10 | | 10 | µA |
| **DDR_CSn[1:0], DDR_CKE[1:0], DDR_CK, DDR_CKn, DDR_CASn, DDR_RASn, DDR_WEn, DDR_BA[2:0], DDR_A[15:0], DDR_D[31:0], DDR_DQM[3:0], DDR_DQS[3:0], DDR_DQSn[3:0] pins (LPDDR2 - HSUL_12 mode)[2]** | | | | | | |
| $V_{IH}$ | High-level input voltage | VDDS_DDR = 1.2 V | DDR_VREF + 0.13 | | | V |
| $V_{IL}$ | Low-level input voltage | VDDS_DDR = 1.2 V | | | DDR_VREF – 0.13 | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | | NA | | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 8 mA | VDDS_DDR – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –10 | | 10 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 40 | | 240 | |
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –10 | | 10 | µA |
| **DDR_RESETn[3]** | | | | | | |
| $V_{IH}$ | High-level input voltage | | | NA | | |
| $V_{IL}$ | Low-level input voltage | | | NA | | |
| $V_{HYS}$ | Hysteresis voltage at an input | | | NA | | |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 8 mA | VDDS_DDR – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –10 | | 10 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –240 | | –24 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 24 | | 240 | |

## DC Electrical Characteristics *(continued)*

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)[1]

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –10 | | 10 | µA |
| **RTC_PWRONRSTn** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.65 × VDDS_RTC | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 × VDDS_RTC | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.065 | | | V |
| $I_I$ | Input leakage current | | –1 | | 1 | µA |
| **RTC_PMIC_EN** | | | | | | |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 6 mA | VDDS_RTC – 0.45 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 6 mA | | | 0.45 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –1 | | 1 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –200 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 40 | | 200 | |
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –1 | | 1 | µA |
| **RTC_WAKEUP** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.65 × VDDS_RTC | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 × VDDS_RTC | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.15 | | | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –1 | | 1 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –200 | | –40 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 40 | | 200 | |
| **TCK (VDDSHV3 = 1.8 V)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 1.45 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.46 | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.4 | | | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –8 | | 8 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –161 | –100 | –52 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 52 | 100 | 170 | |
| **TCK (VDDSHV3 = 3.3 V)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2.15 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.46 | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.4 | | | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –18 | | 18 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –243 | –100 | –19 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 51 | 110 | 210 | |
| **PWRONRSTn (VDDSHV3 = 1.8 V or 3.3 V)[4]** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 1.35 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.5 | V |

## DC Electrical Characteristics *(continued)*

over recommended ranges of supply voltage and operating temperature (unless otherwise noted)(1)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.07 | | | V |
| $I_I$ | Input leakage current | $V_I$ = 1.8 V | | | 0.1 | µA |
| | | $V_I$ = 3.3 V | | | 2 | |
| **All other LVCMOS pins (VDDSHVx = 1.8 V; x=1–11)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.65 × VDDSHVx | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 × VDDSHVx | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.18 | | 0.305 | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 6 mA | VDDSHVx – 0.45 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 6 mA | | | 0.45 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –8.4 | | 8.4 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –161 | –100 | –52 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 52 | 100 | 170 | |
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –8.4 | | 8.4 | µA |
| **All other LVCMOS pins (VDDSHVx = 3.3 V; x=1–11)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{HYS}$ | Hysteresis voltage at an input | | 0.265 | | 0.44 | V |
| $V_{OH}$ | High-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OH}$ = 6 mA | VDDSHVx – 0.45 | | | V |
| $V_{OL}$ | Low-level output voltage, driver enabled, pullup or pulldown disabled | $I_{OL}$ = 6 mA | | | 0.45 | V |
| $I_I$ | Input leakage current, Receiver disabled, pullup or pulldown inhibited | | –18 | | 18 | µA |
| | Input leakage current, Receiver disabled, pullup enabled | | –243 | –100 | –19 | |
| | Input leakage current, Receiver disabled, pulldown enabled | | 51 | 110 | 210 | |
| $I_{OZ}$ | Total leakage current through the terminal connection of a driver-receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited. | | –18 | | 18 | µA |
| **XTALIN (OSC0)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.65 × VDDS_OSC | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 × VDDS_OSC | V |
| **RTC_XTALIN (OSC1)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.65 × VDDS_RTC | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 × VDDS_RTC | V |

(1) The interfaces or signals described in this table correspond to the interfaces or signals available in multiplexing mode 0. All interfaces or signals multiplexed on the terminals described in this table have the same DC electrical characteristics.

(2) For mapping to the LPDDR2 interface terminal name, see the *AM437x Sitara Processors Technical Reference Manual*.

(3) The DDR_RESETn terminal supports fail-safe operation.

(4) The input voltage thresholds for this input are not a function of VDDSHV3.

## 5.8 ADC0: Touch Screen Controller and Analog-to-Digital Subsystem Electrical Parameters

The touch screen controller (TSC) and analog-to-digital converter (ADC) subsystem (ADC0) contains a single-channel ADC connected to an 8:1 analog multiplexer which operates as a general-purpose ADC with optional support for interleaving TSC conversions for 4-wire, 5-wire, or 8-wire resistive panels. The ADC0 subsystem can be configured for use in one of the following applications:

- 8 general-purpose ADC channels
- 4-wire TSC with 4 general-purpose ADC channels
- 5-wire TSC with 3 general-purpose ADC channels
- 8-wire TSC

表 5-5 summarizes the ADC0 subsystem electrical parameters.

**表 5-5. ADC0 Electrical Parameters**

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | |
| ADC0_VREFP[1] | | (0.5 × VDDA_ADC0) + 0.25 | | VDDA_ADC0 | V |
| ADC0_VREFN[1] | | 0 | | (0.5 × VDDA_ADC0) – 0.25 | V |
| ADC0_VREFP + ADC0_VREFN | | | VDDA_ADC0 | | V |
| Full-scale Input Range | Internal Voltage Reference | 0 | | VDDA_ADC0 | V |
| | External Voltage Reference | ADC0_VREFN | | ADC0_VREFP | |
| Differential Nonlinearity (DNL) | Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V | –1 | 0.5 | 1 | LSB |
| Integral Nonlinearity (INL) | Source impedance = 50 Ω Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V | –2 | ±1 | 2 | LSB |
| | Source Impedance = 1 kΩ Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V | | ±1 | | |
| Gain Error | Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V | | ±2 | | LSB |
| Offset Error | Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V | | ±2 | | LSB |
| Input Sampling Capacitance | | | 5.5 | | pF |
| Signal-to-Noise Ratio (SNR) | Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V Input Signal: 30 kHz sine wave at –0.5 dB Full Scale | | 70 | | dB |
| Total Harmonic Distortion (THD) | Internal Voltage Reference: VDDA_ADC0 = 1.8 V External Voltage Reference: VREFP – VREFN = 1.8 V Input Signal: 30 kHz sine wave at –0.5 dB Full Scale | | 75 | | dB |

表 5-5. ADC0 Electrical Parameters (continued)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Spurious Free Dynamic Range | Internal Voltage Reference: VDDA_ADC0 = 1.8 V<br>External Voltage Reference: VREFP – VREFN = 1.8 V<br>Input Signal: 30 kHz sine wave at –0.5 dB Full Scale | | 80 | | dB |
| Signal-to-Noise Plus Distortion | Internal Voltage Reference: VDDA_ADC0 = 1.8 V<br>External Voltage Reference: VREFP – VREFN = 1.8 V<br>Input Signal: 30 kHz sine wave at –0.5 dB Full Scale | | 69 | | dB |
| VREFP and VREFN Input Impedance | | | 20 | | kΩ |
| Input Impedance of AIN[7:0](2) | f = input frequency | | [1/((65.97 × $10^{-12}$) × f)] | | Ω |
| **SAMPLING DYNAMICS** | | | | | |
| ADC Clock Frequency | | | | 13 | MHz |
| Conversion Time | | | 13 | | ADC0 clock cycles |
| Acquisition Time | | 2 | | 257 | ADC0 clock cycles |
| Sampling Rate(3) | ADC0 Clock = 13 MHz | | | 867 | kSPS |
| Channel-to-Channel Isolation | | | 100 | | dB |
| **TOUCH SCREEN SWITCH DRIVERS** | | | | | |
| Pullup and Pulldown Switch ON-Resistance (Ron) | | | 2 | | Ω |
| Pullup and Pulldown Switch Current Leakage Ileak | Source impedance = 500 Ω | | | 0.5 | uA |
| Drive Current | | | | 25 | mA |
| Touch Screen Resistance | | | | 6 | kΩ |
| Pen Touch Detect | | | | 2 | kΩ |

(1) The ADC0_VREFP and ADC0_VREFN terminals should not be allowed to float to prevent noise from coupling into the ADC. If ADC0_VREFN is not used to connect an external negative voltage reference to the ADC, connect it to VSSA_ADC. If ADC0_VREFP is not used to connect an external positive voltage reference to the ADC, connect it to VSSA_ADC or VDDA_ADC0. Connecting ADC0_VREFP to VSSA_ADC in this use case is the preferred option because VDDA_ADC0 may couple more noise into the ADC than VSSA_ADC.

(2) This parameter is valid when the respective AIN terminal is configured to operate as a general-purpose ADC input.

(3) The maximum sample rate assumes a conversion time of 13 ADC clock cycles with the acquisition time configured for the minimum of 2 ADC clock cycles, where it takes a total of 15 ADC clock cycles to sample the analog input and convert it to a positive binary weighted digital value.

## 5.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for high-security (AM437xHS) devices.

**表 5-6. Recommended Operating Conditions for OTP eFuse Programming**

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD_CORE | Supply voltage range for the core domain during OTP operation; OPP100 | 1.056 | 1.1 | 1.144 | V |
| VPP | Supply voltage range for the eFuse ROM domain during normal operation | | NC | | |
| | Supply voltage range for the eFuse ROM domain during OTP programming (1) (2) | 1.65 | 1.7 | 1.75 | V |
| I(VPP) | | | | 50 | mA |
| Temperature (ambient) | | 0 | 30 | 50 | ºC |

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions TLV70717 from the TLV707x family meet the supply voltage range needed for VPP.
(2) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the regulator attached to the VPP terminal. For more details, see *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*.

### 5.9.1 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see 5.12.1.2).

### 5.9.2 Programming Sequence

Programming sequence for OTP eFuses:

1. Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
2. Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
3. Apply the voltage on the VPP terminal according to the specification in 表 5-6.
4. Run the software that programs the OTP registers.
5. After validating the content of the OTP registers, remove the voltage from the VPP terminal.

### 5.9.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY FOR ANY TI DEVICES THAT HAVE BEEN eFUSED.

## 5.10 Thermal Resistance Characteristics

Failure to maintain a junction temperature within the range specified in Section 5.5 reduces operating lifetime, reliability, and performance—and may cause irreversible damage to the system. Therefore, the product design cycle should include thermal analysis to verify the maximum operating junction temperature of the device. It is important this thermal analysis is performed using specific system use cases and conditions. TI provides an application report to aid users in overcoming some of the existing challenges of producing a good thermal design. For more information, see AM43xx Thermal Considerations.

表 5-7 provides thermal characteristics for the packages used on this device.

注

This table provides simulation data and may not represent actual use-case values.

**表 5-7. Thermal Resistance Characteristics (NFBGA Package) [ZDN]**

over operating free-air temperature range (unless otherwise noted)

| NAME | DESCRIPTION | ZDN (°C/W)(1) (2) | AIR FLOW (m/s)(1) (3) |
|---|---|---|---|
| $R\Theta_{JC}$ | Junction-to-case | 7.07 | NA |
| $R\Theta_{JB}$ | Junction-to-board | 11.11 | NA |
| $R\Theta_{JA}$ | Junction-to-free air | 23.0 | 0.0 |
| | | 19.5 | 0.5 |
| | | 18.5 | 1.0 |
| | | 17.5 | 2.0 |
| | | 16.9 | 3.0 |
| $Psi_{JT}$ | Junction-to-package top | 2.10 | 0.0 |
| | | 2.16 | 0.5 |
| | | 2.20 | 1.0 |
| | | 2.27 | 2.0 |
| | | 2.31 | 3.0 |
| $Psi_{JB}$ | Junction-to-board | 11.59 | 0.0 |
| | | 11.18 | 0.5 |
| | | 11.05 | 1.0 |
| | | 10.91 | 2.0 |
| | | 10.80 | 3.0 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(2) °C/W = degrees Celsius per watt.
(3) m/s = meters per second.

## 5.11 External Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

### *5.11.1 Voltage Decoupling Capacitors*

表 5-8 summarizes the Core voltage decoupling characteristics.

#### 5.11.1.1 Core Voltage Decoupling Capacitors

To improve module performance, decoupling capacitors are required to suppress high-frequency switching noise and to stabilize the supply voltage. A decoupling capacitor is most effective when located close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

**表 5-8. Core Voltage Decoupling Characteristics**

| PARAMETER | TYP | UNIT |
|---|---|---|
| $C_{VDD\_CORE}$ (1) | 10.08 | µF |
| $C_{VDD\_MPU}$ (2) | 10.05 | µF |

(1) The typical value corresponds to 1 capacitor of 10 µF and 8 capacitors of 10 nF.

(2) The typical value corresponds to 1 capacitor of 10 µF and 5 capacitors of 10 nF.

#### 5.11.1.2 IO and Analog Voltage Decoupling Capacitors

表 5-9 summarizes the power-supply decoupling capacitor recommendations.

**表 5-9. Power-Supply Decoupling Capacitor Characteristics**

| PARAMETER | TYP | UNIT |
|---|---|---|
| $C_{VDDA\_ADC0}$ | 10 | nF |
| $C_{VDDA\_ADC1}$ | 10 | nF |
| $C_{VDDA1P8V\_USB0}$ (1) | 2.21 | µF |
| $C_{CVDDA3P3V\_USB0}$ | 10 | nF |
| $C_{VDDA1P8V\_USB1}$ | 10 | nF |
| $C_{VDDA3P3V\_USB1}$ | 10 | nF |
| $C_{VDDS}$ (2) | 10.04 | µF |
| $C_{VDDS\_DDR}$ | (3) | |
| $C_{VDDS\_OSC}$ | 10 | nF |
| $C_{VDDS\_PLL\_DDR}$ | 10 | nF |
| $C_{VDDS\_PLL\_CORE\_LCD}$ | 10 | nF |
| $C_{VDDS\_SRAM\_CORE\_BG}$ (4) | 10.01 | µF |
| $C_{VDDS\_SRAM\_MPU\_BB}$ (5) | 10.01 | µF |
| $C_{VDDS\_PLL\_MPU}$ | 10 | nF |
| $C_{VDDS\_RTC}$ | 10 | nF |
| $C_{VDDS\_CLKOUT}$ | 10 | nF |
| $C_{VDDS3P3V\_IOLDO}$ | 10 | nF |
| $C_{VDDSHV1}$ (6) | 10.02 | µF |
| $C_{VDDSHV2}$ (7) | 10.06 | µF |
| $C_{VDDSHV3}$ (7) | 10.06 | µF |
| $C_{VDDSHV5}$ (6) | 10.02 | µF |
| $C_{VDDSHV6}$ (7) | 10.06 | µF |
| $C_{VDDSHV7}$ (6) | 10.02 | µF |

表 5-9. Power-Supply Decoupling Capacitor Characteristics (continued)

| PARAMETER | TYP | UNIT |
|---|---|---|
| $C_{VDDSHV8}$ (6) | 10.02 | µF |
| $C_{VDDSHV9}$ (6) | 10.02 | µF |
| $C_{VDDSHV10}$ (6) | 10.02 | µF |
| $C_{VDDSHV11}$ (6) | 10.02 | µF |

(1) Typical values consist of 1 capacitor of 2.2 µF and 1 capacitor of 10 nF.

(2) Typical values consist of 1 capacitor of 10 µF and 4 capacitors of 10 nF.

(3) For more details on decoupling capacitor requirements for the DDR3 and DDR3L memory interface, see 5.12.8.2.1.3.6 and 5.12.8.2.1.3.7 when using DDR3 and DDR3L memory devices.

(4) VDDS_SRAM_CORE_BG supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_CORE_BG supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_CORE_BG terminals. TI recommends placing a 10-µF capacitor close to the terminal and routing it with the widest traces possible to minimize the voltage drop on VDDS_SRAM_CORE_BG terminals.

(5) VDDS_SRAM_MPU_BB supply powers an internal LDO for SRAM supplies. Inrush currents could cause voltage drop on the VDDS_SRAM_MPU_BB supplies when the SRAM LDO is enabled after powering up VDDS_SRAM_MPU_BB terminals. TI recommends placing a 10-µF capacitor close to the terminal and routing it with the widest traces possible to minimize the voltage drop on VDDS_SRAM_MPU_BB terminals.

(6) Typical values consist of 1 capacitor of 10 µF and 2 capacitors of 10 nF.

(7) Typical values consist of 1 capacitor of 10 µF and 6 capacitors of 10 nF.

### 5.11.2 Output Capacitors

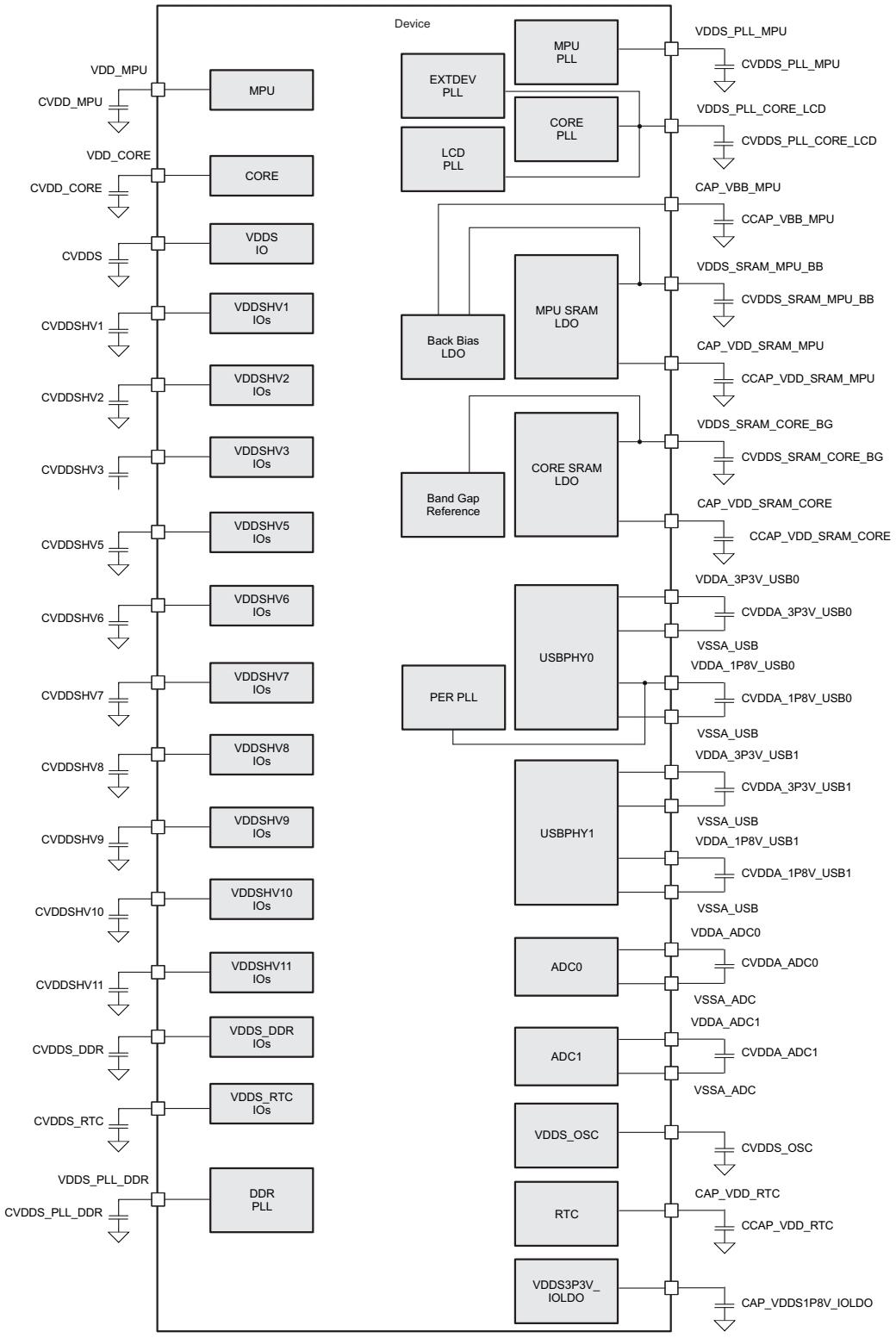
Internal low dropout output (LDO) regulators require external capacitors to stabilize their outputs. These capacitors should be placed as close as possible to the respective terminals of the device. 表 5-10 summarizes the LDO output capacitor recommendations.

表 5-10. Output Capacitor Characteristics

| PARAMETER | TYP | UNIT |
|---|---|---|
| $C_{CAP\_VDD\_SRAM\_CORE}$ (1) | 1 | µF |
| $C_{CAP\_VDD\_RTC}$ (1) (2) | 1 | µF |
| $C_{CAP\_VDD\_SRAM\_MPU}$ (1) | 1 | µF |
| $C_{CAP\_VBB\_MPU}$ (1) | 1 | µF |
| $C_{CAP\_VDDS1P8V\_IOLDO}$ (1) (3) | 2.2 | µF |

(1) LDO regulator outputs should not be used as a power source for any external components.
(2) The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the RTC_KALDO_ENn terminal is high.
(3) The CAP_VDDS1P8V_IOLDO terminal is the output of the IO LDO and required for simplified power sequencing. For more details, see 図 5-8. If simplified power sequencing is not used, this terminal can be left floating.

図 5-2 shows an example of the external capacitors.




A. Decoupling capacitors must be placed as closed as possible to the power terminal. Choose the ground closest to the power pin for each decoupling capacitor. In case of interconnecting powers, first insert the decoupling capacitor and then interconnect the powers.

B. The decoupling capacitor value depends on the board characteristics.

**図 5-2. External Capacitors**

## 5.12 Timing and Switching Characteristics

The data provided in the following timing requirements and switching characteristics tables assumes the device is operating within the recommended operating conditions defined in Section 5.5, unless otherwise noted.

### *5.12.1 Power Supply Sequencing*

#### 5.12.1.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 1.0E + 5 V/s. For instance, as shown in 図 5-3, TI recommends having the supply ramp slew for a 1.8-V supply of more than 18 µs.

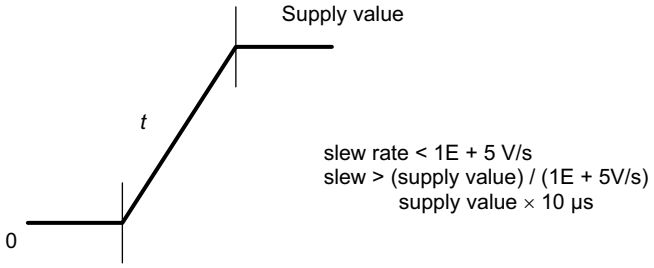
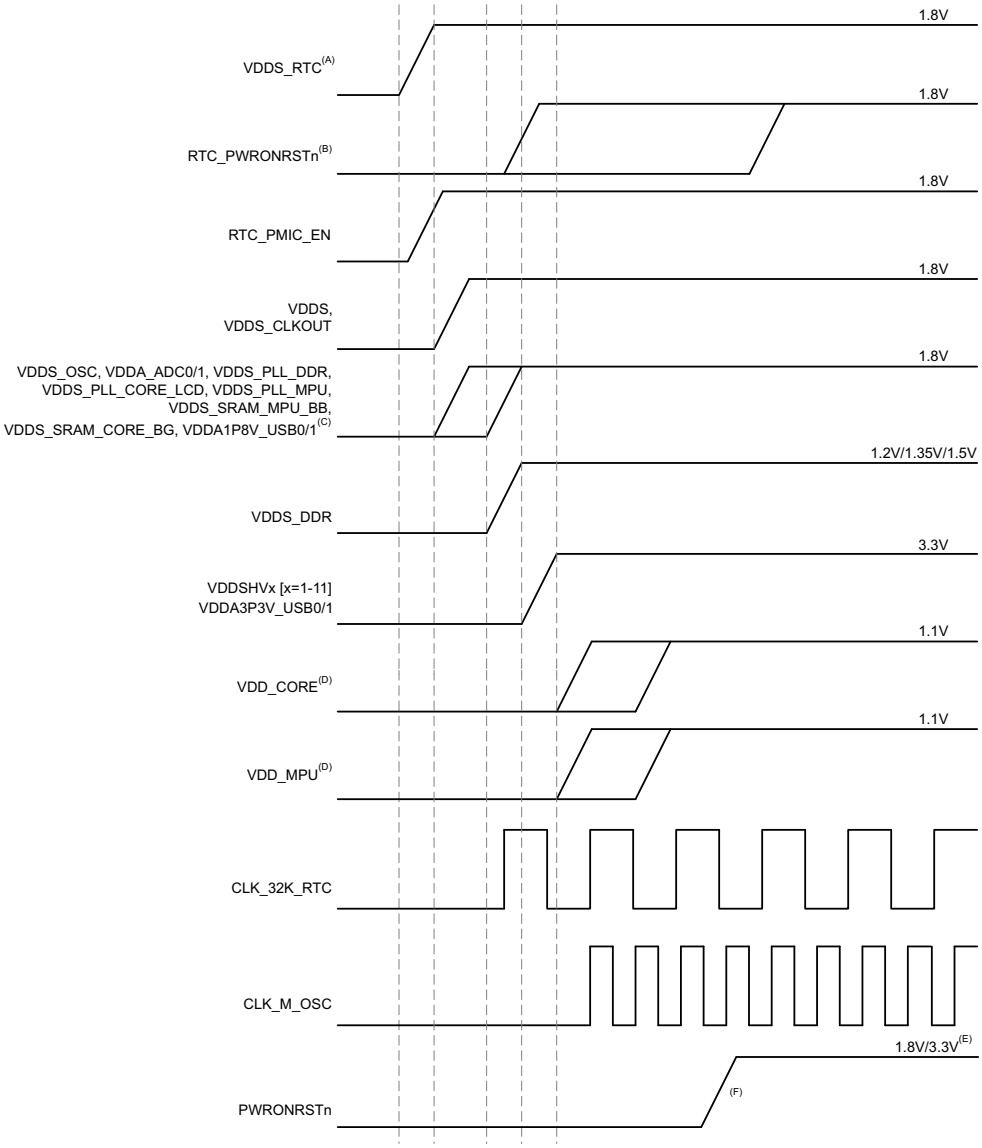



**図 5-3. Power Supply Slew and Slew Rate**

### 5.12.1.2 Power-Up Sequencing




A. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.
VDDS_RTC can be ramped independent of other supplies if RTC_PMIC_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE when internal RTC LDO is enabled, there might be a small amount of leakage current on VDD_CORE.

B. RTC_PWRONRSTn should be asserted for at least 1 ms and can be released before the 32-kHz clock is stable.

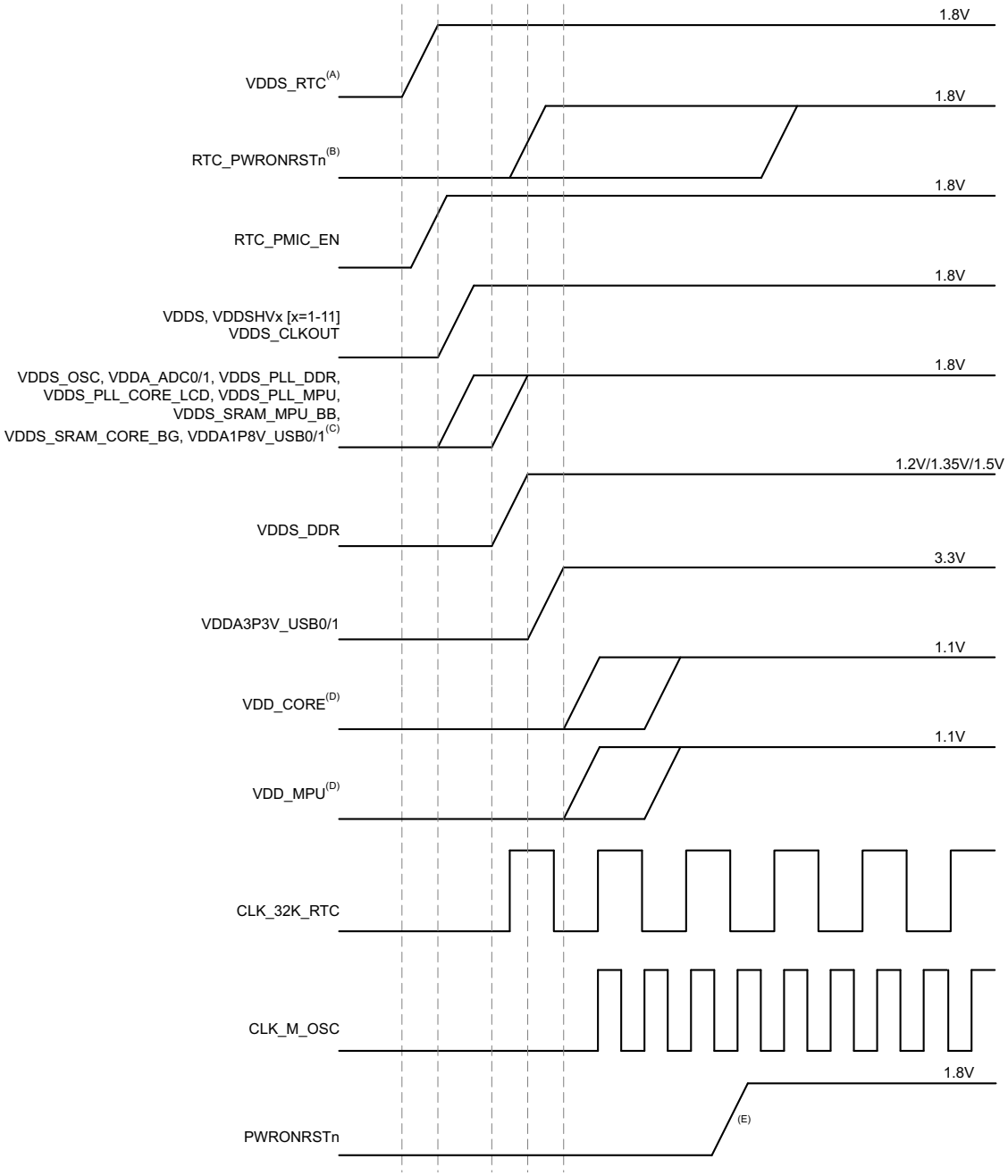
C. These supplies can be ramped together with VDDS, VDDS_CLKOUT supplies if powered from the same source only. If a USB port is not used, the respective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

D. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

E. PWRONRSTn input voltage thresholds are not dependent on VDDSHV3 voltage and the terminal is not fail-safe. PWRONRSTn can accept 1.8-V or 3.3-V input levels when VDDSHV3 is configured as 3.3 V. However, PWRONRSTn can only accept 1.8 V input levels when VDDSHV3 is configured as 1.8 V. For details on this input terminal, see Section 5.7.

F. It is required to hold the PWRONRSTn terminal low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**図 5-4. Power Sequencing With RTC Feature Enabled, All Dual-Voltage IOs Configured as 3.3 V**




A. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.

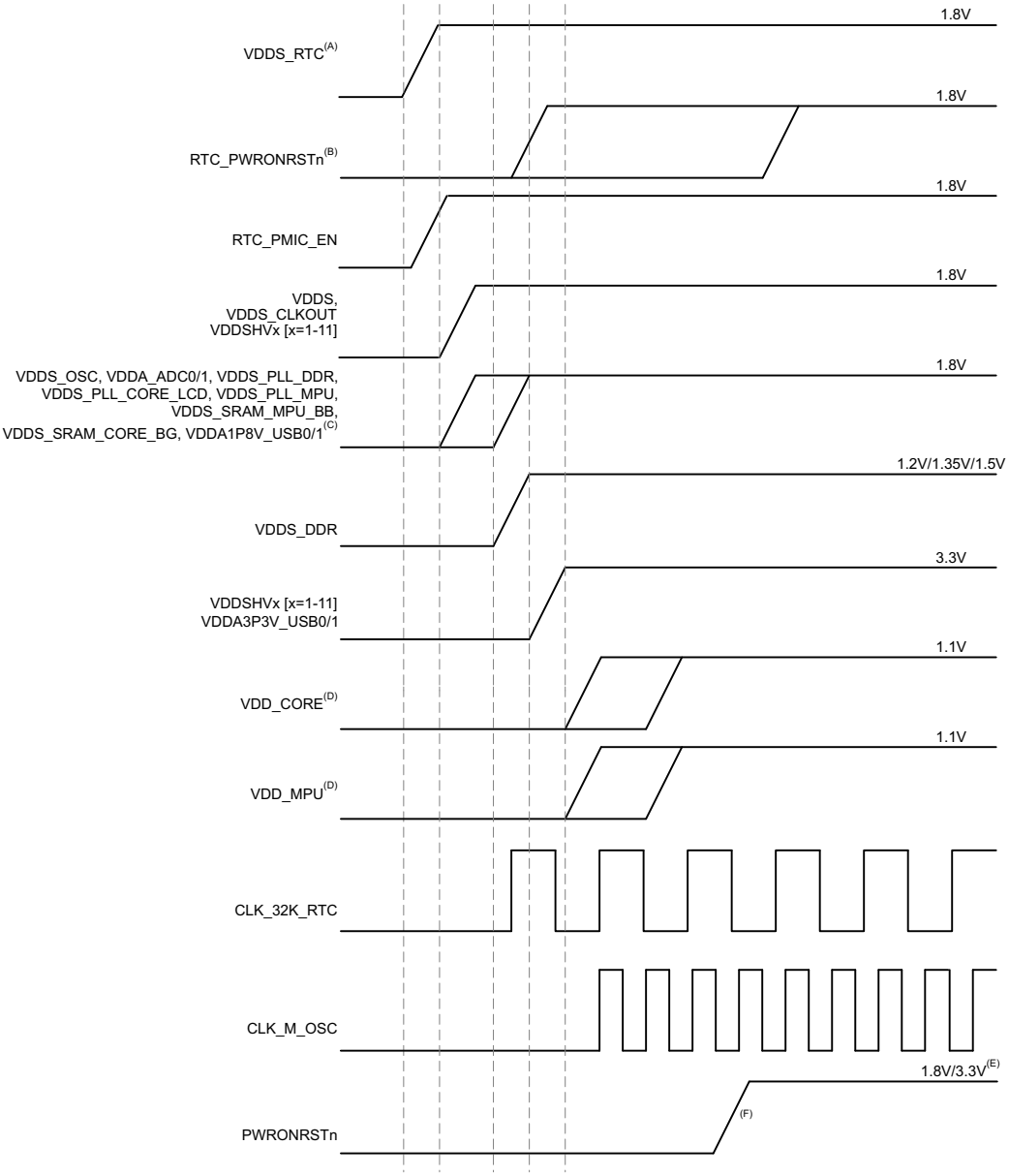
B. RTC_PWRONRSTn should be asserted for at least 1 ms and can be released before the 32-kHz clock is stable.

C. These supplies can be ramped together with the VDDS, VDDSHVx [x=1-11], VDDS_CLKOUT supplies if powered from the same source.
If a USB port is not used, the respective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

D. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

E. It is required to hold the PWRONRSTn terminal low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**図 5-5. Power Sequencing With RTC Feature Enabled, All Dual-Voltage IOs Configured as 1.8 V**




A. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.

B. RTC_PWRONRSTn should be asserted for at least 1 ms and can be released before the 32-kHz clock is stable.

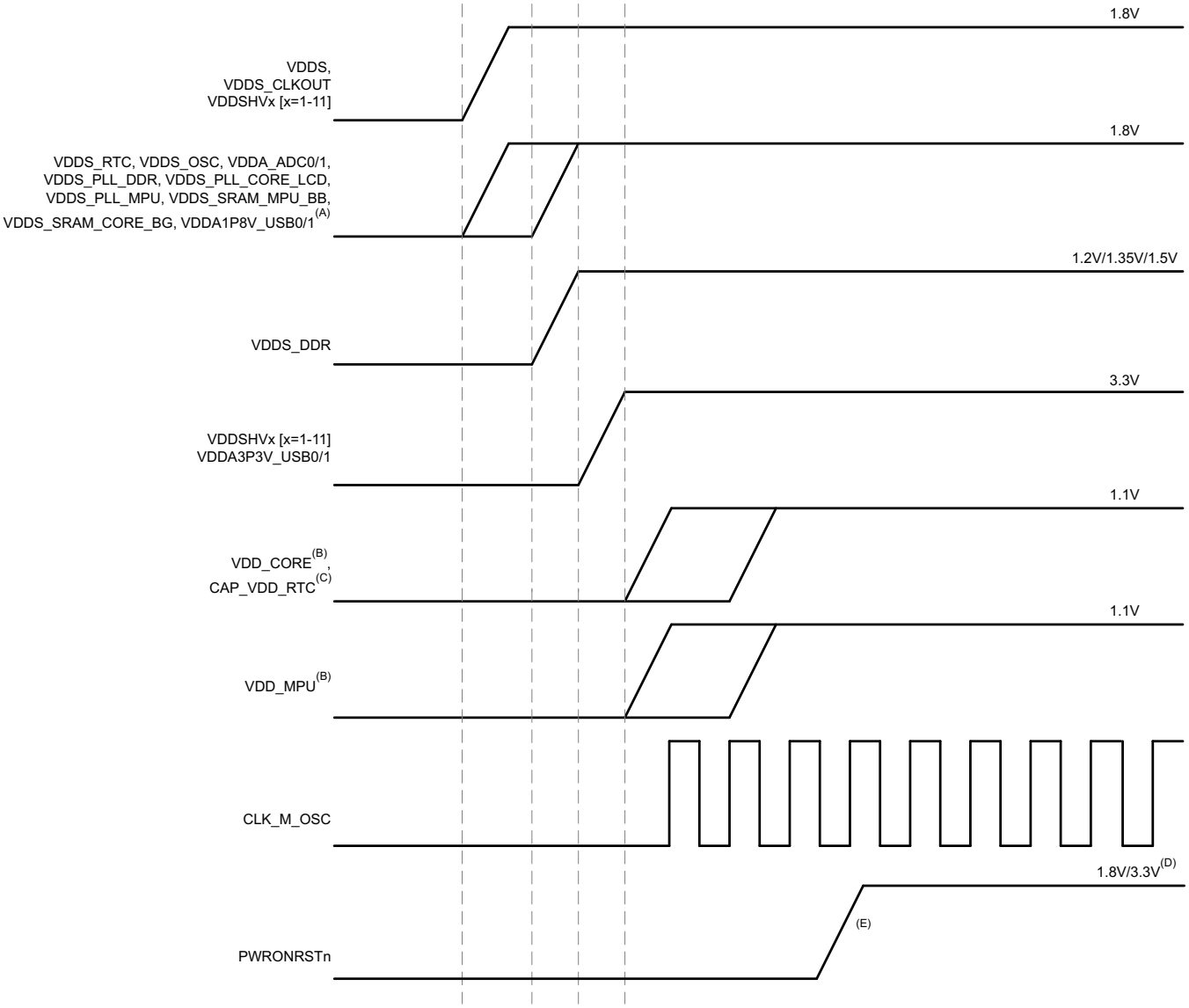
C. These supplies can be ramped together with the VDDS, VDDSHVx [x=1-11], VDDS_CLKOUT supplies if powered from the same source.
If a USB port is not used, the respective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

D. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

E. PWRONRSTn input voltage thresholds are not dependent on VDDSHV3 voltage and the terminal is not fail-safe. PWRONRSTn can accept 1.8-V or 3.3-V input levels when VDDSHV3 is configured as 3.3 V. However, PWRONRSTn can only accept 1.8 V input levels when VDDSHV3 is configured as 1.8 V. For details on this input terminal, see Section 5.7.

F. It is required to hold the PWRONRSTn terminal low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**図 5-6. Power Sequencing With RTC Feature Enabled, Dual-Voltage IOs Configured as 1.8 V, 3.3 V**




A. These supplies can be ramped together with the VDDS, VDDSHVx [x=1-11], VDDS_CLKOUT supplies if powered from the same source.
If a USB port is not used, the repsective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

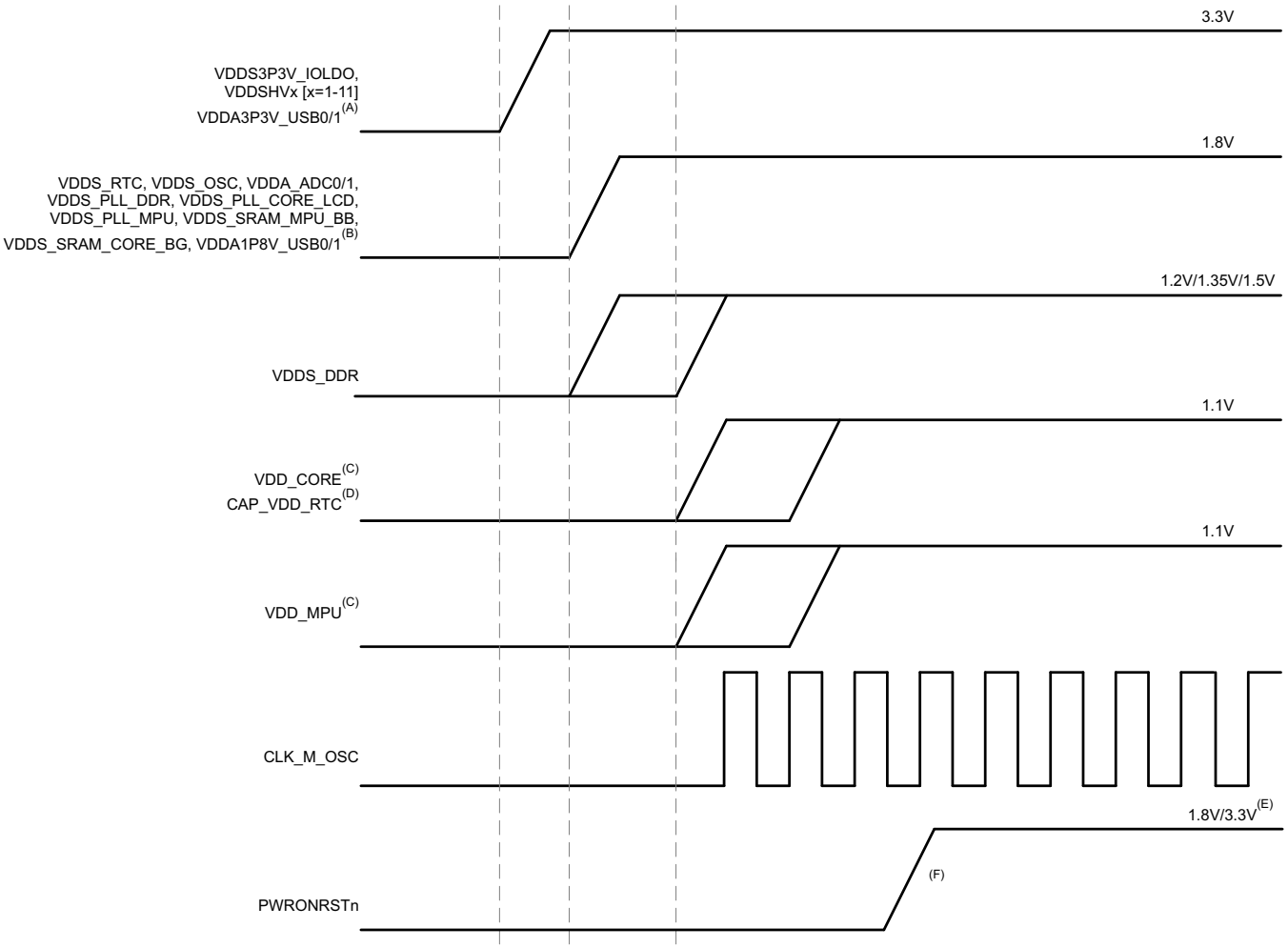
B. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

C. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.
VDDS_RTC can be ramped independent of other supplies if RTC_PMIC_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE when internal RTC LDO is enabled, there might be a small amount of leakage current on VDD_CORE.

D. PWRONRSTn input voltage thresholds are not dependent on VDDSHV3 voltage and the terminal is not fail-safe. PWRONRSTn can accept 1.8-V or 3.3-V input levels when VDDSHV3 is configured as 3.3 V. However, PWRONRSTn can only accept 1.8 V input levels when VDDSHV3 is configured as 1.8 V. For details on this input terminal, see Section 5.7.

E. It is required to hold the PWRONRSTn terminal low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**図 5-7. Power Sequencing With RTC Feature Disabled, Dual-Voltage IOs Configured as 1.8 V, 3.3 V**




A. Power source supplying VDDS3P3V_IOLDO should have a supply slew of >100us.
CAP_VDDS1P8V_IOLDO is the 1.8-V output of VDDA3P3V_IOLDO. VDDS, VDDS_CLKOUT terminals are powered by shorting them to CAP_VDDS1P8V_IOLDO on the board.

B. If a USB port is not used, the repsective VDDA1P8V_USB may be connected to any 1.8-V power supply and the respective VDDA3P3V_USB terminal may be connected to any 3.3-V power supply. If a system does not have a 3.3-V supply, the VDDA3P3V_USB may be connected to ground.

C. VDD_MPU and VDD_CORE can be supplied from the same power source if OPPs higher than OPP100 are not used.

D. The CAP_VDD_RTC terminal operates as an input to the RTC core voltage domain when the internal RTC LDO is disabled by connecting the RTC_KALDO_ENn terminal to VDDS_RTC.
If the internal RTC LDO is disabled, CAP_VDD_RTC should be sourced from an external 1.1-V power supply. If CAP_VDD_RTC is ramped after VDD_CORE, there might be a small amount of additional leakage current on VDD_CORE.
VDDS_RTC can be ramped independent of other supplies if RTC_PMIC_EN functionality is not required. If VDDS_RTC is ramped after VDD_CORE when internal RTC LDO is enabled, there might be a small amount of leakage current on VDD_CORE.

E. PWRONRSTn input voltage thresholds are not dependent on VDDSHV3 voltage and the terminal is not fail-safe. PWRONRSTn can accept 1.8-V or 3.3-V input levels when VDDSHV3 is configured as 3.3 V. However, PWRONRSTn can only accept 1.8 V input levels when VDDSHV3 is configured as 1.8 V. For details on this input terminal, see Section 5.7.

F. The PWRONRSTn terminal must be held low until all the supplies have ramped and the input clock CLK_M_OSC is stable.

**図 5-8. Simplified Power Sequencing With RTC Feature Disabled, Dual-Voltage IOs Configured as 3.3 V**

#### 5.12.1.3 Power-Down Sequencing

PWRONRSTn input terminal should be taken low, which stops all internal clocks before power supplies are turned off. All other external clocks to the device should be shut off.

The preferred way to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that is ramped down. This ensures there would be no spurious current paths during the power-down sequence. The VDDS, VDDS_CLKOUT power supply must ramp down after all 3.3-V VDDSHVx [x=1-11] power supplies.

If it is desired to ramp down VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] simultaneously, it should always be ensured that the difference between VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] during the entire power-down sequence is <2 V. Any violation of this could cause reliability risks for the device. Further, it is recommended to maintain VDDS, VDDS_CLKOUT ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

If none of the VDDSHVx [x=1-11] power supplies are configured as 3.3 V, the VDDS, VDDS_CLKOUT power supply may ramp down along with the VDDSHVx [x=1-11] supplies or after all the VDDSHVx [x=1-11] supplies have ramped down. TI recommends maintaining VDDS, VDDS_CLKOUT ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

When using simplified power-down sequence, there are no power-down requirements between the VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] supplies and are ramped down together without any reliability concerns.

## 5.12.2 Clock

### 5.12.2.1 PLLs

#### 5.12.2.1.1 Digital Phase-Locked Loop Power Supply Requirements

The digital phase-locked loop (DPLL) provides all interface clocks and functional clocks to the processor of the device. The device integrates six different DPLLs:

- Core DPLL
- Per DPLL
- Display DPLL
- DDR DPLL
- MPU DPLL
- EXTDEV DPLL

図 5-9 shows the power supply connectivity implemented in the device. 表 5-11 provides the power supply requirements for the DPLL.

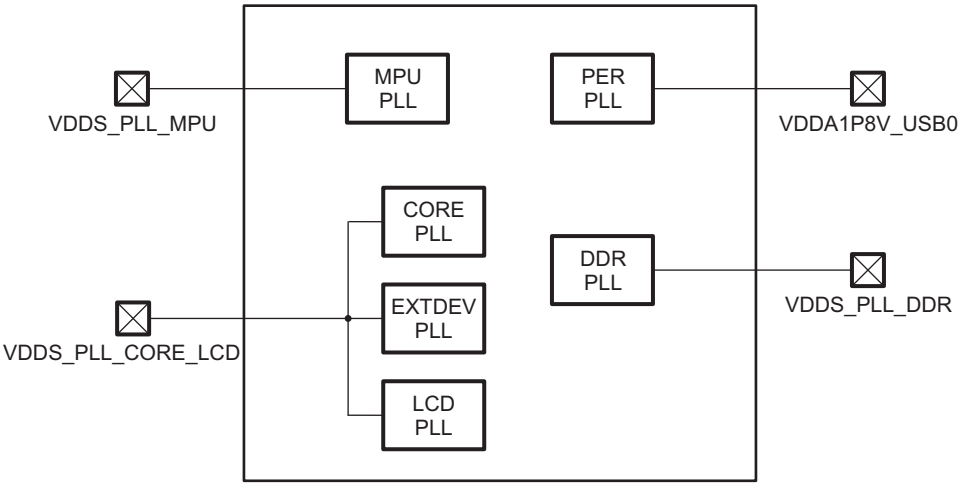



**図 5-9. DPLL Power Supply Connectivity**

**表 5-11. DPLL Power Supply Requirements**

| SUPPLY NAME | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDDA1P8V_USB0 | Supply voltage range for USBPHY and PER DPLL, Analog, 1.8V | 1.71 | 1.8 | 1.89 | V |
| | Max. peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_MPU | Supply voltage range for DPLL MPU, Analog | 1.71 | 1.8 | 1.89 | V |
| | Max. peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_CORE_LCD | Supply voltage range for DPLL CORE, EXTDEV, and LCD, Analog | 1.71 | 1.8 | 1.89 | V |
| | Max. peak-to-peak supply noise | | | 50 | mV (p-p) |
| VDDS_PLL_DDR | Supply voltage range for DPLL DDR, Analog | 1.71 | 1.8 | 1.89 | V |
| | Max. peak-to-peak supply noise | | | 50 | mV (p-p) |

#### 5.12.2.2 Input Clock Specifications

The device has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal circuit (oscillator mode) or external LVCMOS square-wave digital clock source (bypass mode). The oscillators automatically operate in bypass mode when their input is connected to an external LVCMOS square-wave digital clock source. The oscillator associated with a specific clock input must be enabled when the clock input is being used in either oscillator mode or bypass mode.

The OSC1 oscillator provides a 32.768-kHz reference clock to the real-time clock (RTC) and is connected to the RTC_XTALIN and RTC_XTALOUT terminals. This clock source is referred to as the 32K oscillator (CLK_32K_RTC) in the device-specific technical reference manual. OSC1 is disabled by default after power is applied. This clock input is optional and may not be required if the RTC is configured to receive a clock from the internal 32k RC oscillator (CLK_RC32K) or peripheral PLL (CLK_32KHZ) which receives a reference clock from the OSC0 input.

The OSC0 oscillator provides a 19.2-MHz, 24-MHz, 25-MHz, or 26-MHz reference clock which is used to clock all non-RTC functions and is connected to the XTALIN and XTALOUT terminals. This clock source is referred to as the master oscillator (CLK_M_OSC) in the device-specific technical reference manual. OSC0 is enabled by default after power is applied.

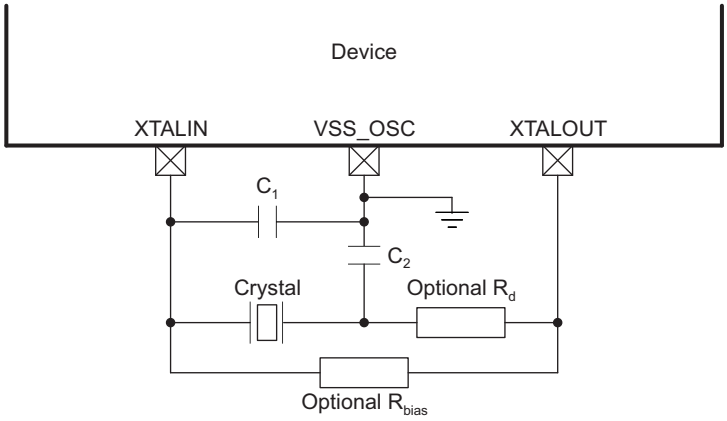
For more information related to recommended circuit topologies and crystal oscillator circuit requirements for these clock inputs, see 5.12.2.3.

### 5.12.2.3 Input Clock Requirements

#### *5.12.2.3.1 OSC0 Internal Oscillator Clock Source*

図 5-10 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors $R_{bias}$ and $R_d$ in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, $R_{bias}$ is not required and $R_d$ is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

The XTALIN terminal has a 15-kΩ to 40-kΩ internal pulldown resistor which is enabled when OSC0 is disabled. This internal resistor prevents the XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.






A. Oscillator components (Crystal, $C_1$, $C_2$, optional $R_{bias}$ and $R_d$) must be located close to the package. Parasitic capacitance to the printed circuit board (PCB) ground and other signals should be minimized to reduce noise coupled into the oscillator. The external crystal component grounds should be connected to the VSS_OSC terminal. The VSS_OSC terminal should be connected to the PCB ground plane as close as possible to the device.

B. $C_1$ and $C_2$ represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors $C_1$ and $C_2$ should be selected to provide the total load capacitance, $C_L$, specified by the crystal manufacturer. The total load capacitance is $C_L = [(C_1 \times C_2)/(C_1+C_2)] + C_{shunt}$, where $C_{shunt}$ is the crystal shunt capacitance ($C_0$) specified by the crystal manufacturer plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the XTALIN and XTALOUT signals. For recommended values of crystal circuit components, see 表 5-12.

**図 5-10. OSC0 Crystal Circuit Schematic**

**表 5-12. OSC0 Crystal Circuit Requirements**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | Crystal parallel resonance frequency | Fundamental mode oscillation only | | 19.2, 24.0, 25.0, or 26.0 | | MHz |
| | Crystal frequency stability and tolerance | | –50.0 | | 50.0 | ppm |
| $C_{C1}$ | $C_1$ capacitance | | 12.0 | | 24.0 | pF |
| $C_{C2}$ | $C_2$ capacitance | | 12.0 | | 24.0 | pF |
| $C_{shunt}$ | Shunt capacitance | | | | 5.0 | pF |
| ESR | Crystal effective series resistance | $f_{xtal}$ = 19.2 MHz, oscillator has nominal negative resistance of 272 Ω and worst-case negative resistance of 163 Ω | | | 54.4 | Ω |
| | | $f_{xtal}$ = 24.0 MHz, oscillator has nominal negative resistance of 240 Ω and worst-case negative resistance of 144 Ω | | | 48.0 | |
| | | $f_{xtal}$ = 25.0 MHz, oscillator has nominal negative resistance of 233 Ω and worst-case negative resistance of 140 Ω | | | 46.6 | |
| | | $f_{xtal}$ = 26.0 MHz, oscillator has nominal negative resistance of 227 Ω and worst-case negative resistance of 137 Ω | | | 45.3 | |

**表 5-13. OSC0 Crystal Circuit Characteristics**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{pkg}$ | Shunt capacitance of package | ZDN package | | 0.01 | | pF |
| $P_{xtal}$ | The actual values of the ESR, $f_{xtal}$, and $C_L$ should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, $f_{xtal}$, and $C_L$ parameters yields a maximum power dissipation value. | | | $P_{xtal}$ = 0.5 ESR (2 π $f_{xtal}$ $C_L$ VDDS_OSC)$^2$ | | |
| $t_{sX}$ | Start-up time | | | 1.5 | | ms |

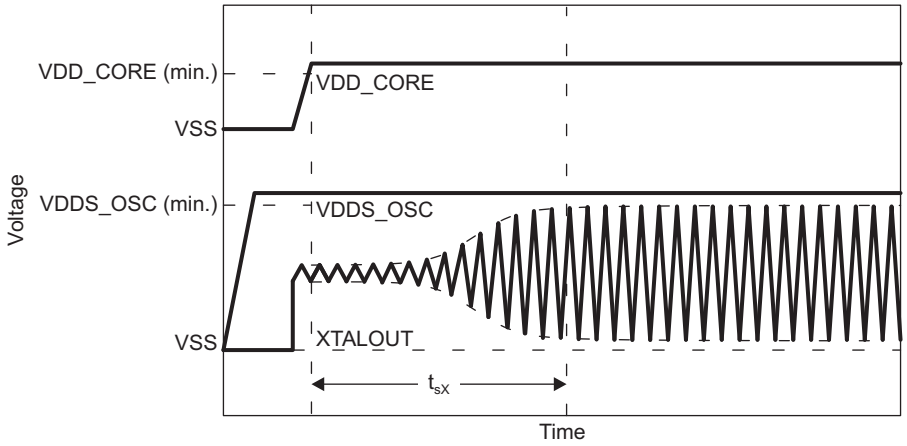



**図 5-11. OSC0 Start-up Time**

#### 5.12.2.3.2 OSC0 LVCMOS Digital Clock Source

図 5-12 shows the recommended oscillator connections when OSC0 is connected to an LVCMOS square-wave digital clock source. The LVCMOS clock source is connected to the XTALIN terminal. In this mode of operation, the XTALOUT terminal should not be used to source any external components. The printed circuit board design should provide a mechanism to disconnect the XTALOUT terminal from any external components or signal traces that may couple noise into OSC0 via the XTALOUT terminal.

The XTALIN terminal has a 15-kΩ to 40-kΩ internal pulldown resistor which is enabled when OSC0 is disabled. This internal resistor prevents the XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.

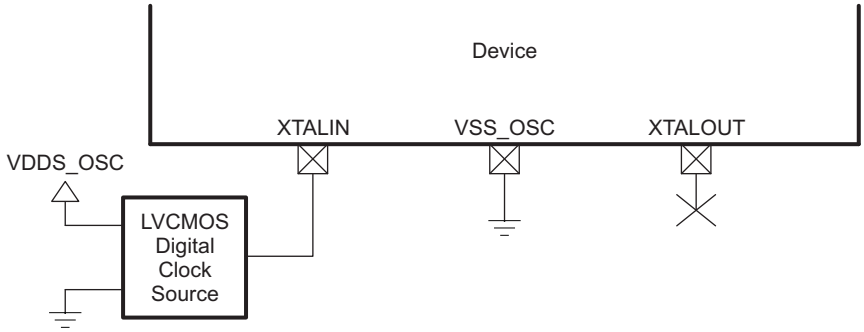





**図 5-12. OSC0 LVCMOS Circuit Schematic**

**表 5-14. OSC0 LVCMOS Reference Clock Requirements**

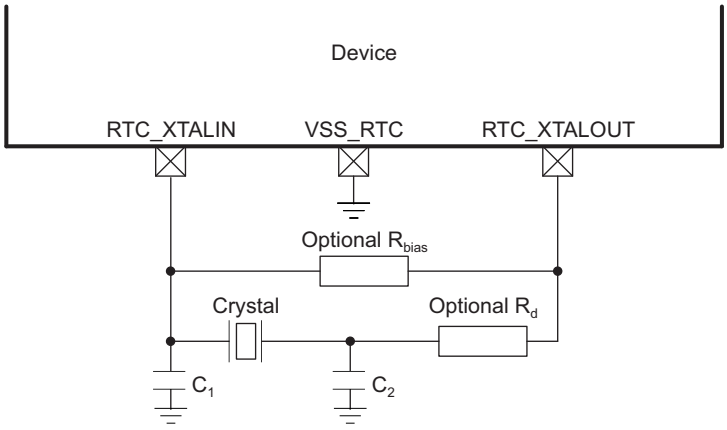
| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(XTALIN)}$ | Frequency, LVCMOS reference clock | | 19.2, 24, 25, or 26 | | MHz |
| | Frequency, LVCMOS reference clock stability and tolerance (1) | –50 | | 50 | ppm |
| $t_{dc(XTALIN)}$ | Duty cycle, LVCMOS reference clock period | 45% | | 55% | |
| $t_{jpp(XTALIN)}$ | Jitter peak-to-peak, LVCMOS reference clock period | –1% | | 1% | |
| $t_{R(XTALIN)}$ | Time, LVCMOS reference clock rise | | | 5 | ns |
| $t_{F(XTALIN)}$ | Time, LVCMOS reference clock fall | | | 5 | ns |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

#### 5.12.2.3.3 OSC1 Internal Oscillator Clock Source

図 5-13 shows the recommended crystal circuit for OSC1 of the package. It is recommended that pre-production printed circuit board (PCB) designs include the two optional resistors $R_{bias}$ and $R_d$ in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, $R_{bias}$ is not required and $R_d$ is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

The RTC_XTALIN terminal has a 10-kΩ to 40-kΩ internal pullup resistor which is enabled when OSC1 is disabled. This internal resistor prevents the RTC_XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.






A. Oscillator components (Crystal, $C_1$, $C_2$, optional $R_{bias}$ and $R_d$) must be located close to the package. Parasitic capacitance to the printed circuit board (PCB) ground and other signals should be minimized to reduce noise coupled into the oscillator.

B. $C_1$ and $C_2$ represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors $C_1$ and $C_2$ should be selected to provide the total load capacitance, $C_L$, specified by the crystal manufacturer. The total load capacitance is $C_L = [(C_1 \times C_2)/(C_1+C_2)] + C_{shunt}$, where $C_{shunt}$ is the crystal shunt capacitance ($C_0$) specified by the crystal manufacturer plus any mutual capacitance ($C_{pkg}$ + $C_{PCB}$) seen across the RTC_XTALIN and RTC_XTALOUT signals. For recommended values of crystal circuit components, see 表 5-15.

**図 5-13. OSC1 Crystal Circuit Schematic**

**表 5-15. OSC1 Crystal Circuit Requirements**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | Crystal parallel resonance frequency | Fundamental mode oscillation only | | 32.768 | | kHz |
| | Crystal frequency stability and tolerance | Maximum RTC error = 10.512 minutes per year | –20.0 | | 20.0 | ppm |
| | | Maximum RTC error = 26.28 minutes per year | –50.0 | | 50.0 | ppm |
| $C_{C1}$ | $C_1$ capacitance | | 12.0 | | 24.0 | pF |
| $C_{C2}$ | $C_2$ capacitance | | 12.0 | | 24.0 | pF |
| $C_{shunt}$ | Shunt capacitance | | | | 1.5 | pF |
| ESR | Crystal effective series resistance | $f_{xtal}$ = 32.768 kHz, oscillator has nominal negative resistance of 725 kΩ and worst-case negative resistance of 250 kΩ | | | 80 | kΩ |

**表 5-16. OSC1 Crystal Circuit Characteristics**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{pkg}$ | Shunt capacitance of package | ZDN package | | 0.17 | | pF |

表 5-16. OSC1 Crystal Circuit Characteristics (continued)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $P_{xtal}$ | The actual values of the ESR, $f_{xtal}$, and $C_L$ should be used to yield a typical crystal power dissipation value. Using the maximum values specified for ESR, $f_{xtal}$, and $C_L$ parameters yields a maximum power dissipation value. | | $P_{xtal}$ = 0.5 ESR (2 π $f_{xtal}$ $C_L$ VDDS_RTC)$^2$ | | |
| $t_{sX}$ | Start-up time | | 2 | | s |

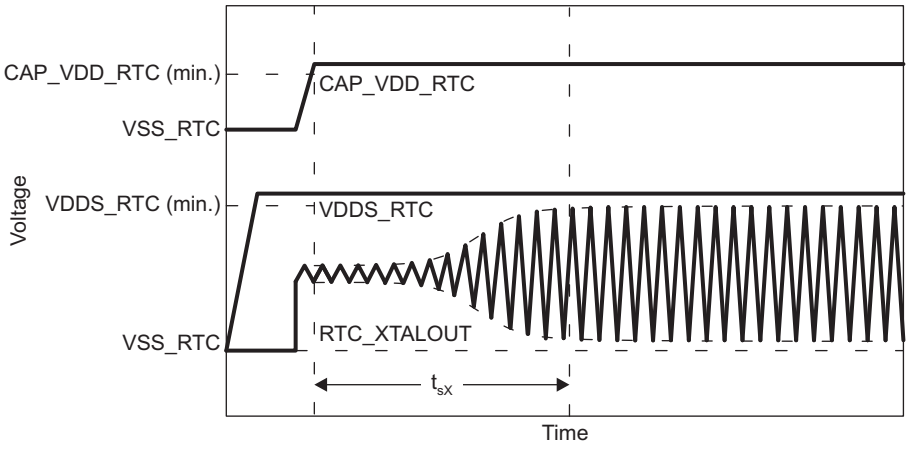



図 5-14. OSC1 Start-up Time

#### 5.12.2.3.4 OSC1 LVCMOS Digital Clock Source

図 5-15 shows the recommended oscillator connections when OSC1 of the package is connected to an LVCMOS square-wave digital clock source. The LVCMOS clock source is connected to the RTC_XTALIN terminal. In this mode of operation, the RTC_XTALOUT terminal should not be used to source any external components. The printed circuit board design should provide a mechanism to disconnect the RTC_XTALOUT terminal from any external components or signal traces that may couple noise into OSC1 via the RTC_XTALOUT terminal.

The RTC_XTALIN terminal has a 10-kΩ to 40-kΩ internal pullup resistor which is enabled when OSC1 is disabled. This internal resistor prevents the RTC_XTALIN terminal from floating to an invalid logic level which may increase leakage current through the oscillator input buffer.

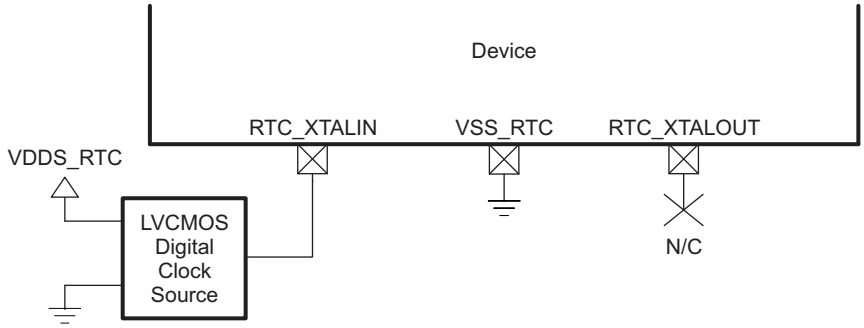





**図 5-15. OSC1 LVCMOS Circuit Schematic**

**表 5-17. OSC1 LVCMOS Reference Clock Requirements**

| NAME | DESCRIPTION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(RTC\_XTALIN)}$ | Frequency, LVCMOS reference clock | | | 32.768 | | kHz |
| | Frequency, LVCMOS reference clock stability and tolerance(1) | Maximum RTC error = 10.512 minutes/year | –20 | | 20 | ppm |
| | | Maximum RTC error = 26.28 minutes/year | –50 | | 50 | ppm |
| $t_{dc(RTC\_XTALIN)}$ | Duty cycle, LVCMOS reference clock period | | 45% | | 55% | |
| $t_{jpp(RTC\_XTALIN)}$ | Jitter peak-to-peak, LVCMOS reference clock period | | –1% | | 1% | |
| $t_{R(RTC\_XTALIN)}$ | Time, LVCMOS reference clock rise | | | | 5 | ns |
| $t_{F(RTC\_XTALIN)}$ | Time, LVCMOS reference clock fall | | | | 5 | ns |

(1) Initial accuracy, temperature drift, and aging effects should be combined when evaluating a reference clock for this requirement.

#### 5.12.2.3.5 OSC1 Not Used

図 5-16 shows the recommended oscillator connections when OSC1 is not used. An internal 10-kΩ pullup on the RTC_XTALIN terminal is turned on when OSC1 is disabled to prevent this input from floating to an invalid logic level which may increase leakage current through the oscillator input buffer. OSC1 is disabled by default after power is applied. Therefore, both RTC_XTALIN and RTC_XTALOUT terminals should be a no connect (NC) when OSC1 is not used.

For more information on disabling OSC1, see the device-specific technical reference manual.

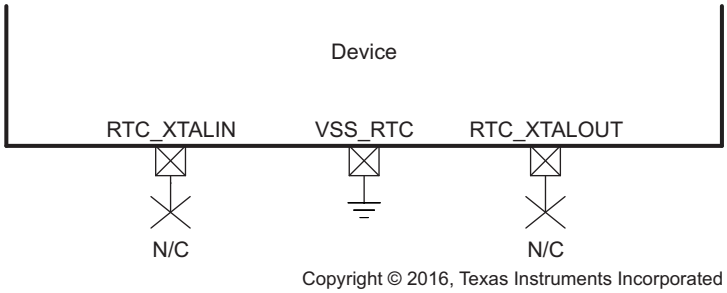



**図 5-16. OSC1 Not Used Schematic**

#### 5.12.2.4 Output Clock Specifications

The device has two clock output signals. The CLKOUT1 signal can be configured to output the master oscillator (CLK_M_OSC), EXTDEV_PLL, 32-kHz, or several other internal clocks. See the device-specific TRM for more details. The CLKOUT2 signal can be configured to output the OSC1 input clock, which is referred to as the 32K oscillator (CLK_32K_RTC) in the device-specific technical reference manual, or four other internal clocks. For more information related to configuring these clock output signals, see the *CLKOUT Signals* section of the device-specific technical reference manual.

#### 5.12.2.5 Output Clock Characteristics

##### *5.12.2.5.1 CLKOUT1*

The CLKOUT1 signal can be output on the XDMA_EVENT_INTR0 terminal. This terminal connects to one of seven internal signals through configurable multiplexers. The XDMA_EVENT_INTR0 multiplexer must be configured for Mode 3 to connect the CLKOUT1 signal to the XDMA_EVENT_INTR0 terminal.

The default reset configuration of the XDMA_EVENT_INTR0 multiplexer is selected by the logic level applied to the DSS_HSYNC terminal on the rising edge of PWRONRSTn. The XDMA_EVENT_INTR0 multiplexer is configured to Mode 7 if the DSS_HSYNC terminal is low on the rising edge of PWRONRSTn or Mode 3 if the DSS_HSYNC terminal is high on the rising edge of PWRONRSTn. This allows the CLKOUT1 signal to be output on the XDMA_EVENT_INTR0 terminal without software intervention. In this mode, the output is held low while PWRONRSTn is active and begins to toggle after PWRONRSTn is released.

##### *5.12.2.5.2 CLKOUT2*

The CLKOUT2 signal can be output on the XDMA_EVENT_INTR1 terminal. This terminal connects to one of seven internal signals through configurable multiplexers. The XDMA_EVENT_INTR1 multiplexer must be configured for Mode 3 to connect the CLKOUT2 signal to the XDMA_EVENT_INTR1 terminal.

The default reset configuration of the XDMA_EVENT_INTR1 multiplexer is always Mode 7. Software must configure the XDMA_EVENT_INTR1 multiplexer to Mode 3 for the CLKOUT2 signal to be output on the XDMA_EVENT_INTR1 terminal.

### *5.12.3 Timing Parameters and Board Routing Analysis*

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing or decreasing such delays. TI recommends using the available IO buffer information specification (IBIS) models to analyze the timing characteristics correctly. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

The timing parameter values specified in this data manual assume the SLEWCTRL bit in each pad control register is configured for fast mode (0b).

For the LPDDR2, DDR3, and DDR3L memory interfaces, it is *not* necessary to use the IBIS models to analyze timing characteristics. TI provides a PCB routing rules solution that describes the routing rules to ensure the memory interface timings are met.

### 5.12.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.

### 5.12.5 Controller Area Network (CAN)

For more information, see the Controller Area Network (CAN) section of the *AM437x Sitara Processors Technical Reference Manual*.

#### 5.12.5.1 DCAN Electrical Data and Timing

**表 5-18. Timing Requirements for DCANx Receive**

(see 図 5-17)

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $f_{baud(baud)}$ | Maximum programmable baud rate | | 1 | | 1 | Mbps |
| 1 | $t_{w(RX)}$ | Pulse duration, receive data bit | H - 2(1) | H + 2(1) | H + 2(1) | H + 2(1) | ns |

(1) H = period of baud rate, 1/programmed baud rate.

**表 5-19. Switching Characteristics for DCANx Transmit**

(see 図 5-17)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $f_{baud(baud)}$ | Maximum programmable baud rate | | 1 | | 1 | Mbps |
| 2 | $t_{w(TX)}$ | Pulse duration, transmit data bit | H - 2(1) | H + 2(1) | H - 2(1) | H + 2(1) | ns |

(1) H = period of baud rate, 1/programmed baud rate.

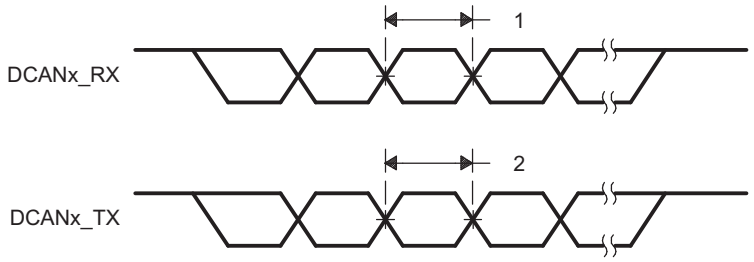



**図 5-17. DCANx Timings**

## 5.12.6 DMTimer

### 5.12.6.1 DMTimer Electrical Data and Timing

**表 5-20. Timing Requirements for DMTimer [1-11]**

(see 図 5-18)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(TCLKIN)}$ | Cycle time, TCLKIN | 4P+1 (1) | | ns |

(1) P = period of PICLKOCP (interface clock).

**表 5-21. Switching Characteristics for DMTimer [4-7]**

(see 図 5-18)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 2 | $t_{w(TIMERxH)}$ | Pulse duration, high | 4P-3 (1) | | ns |
| 3 | $t_{w(TIMERxL)}$ | Pulse duration, low | 4P-3 (1) | | ns |

(1) P = period of PICLKTIMER (functional clock).

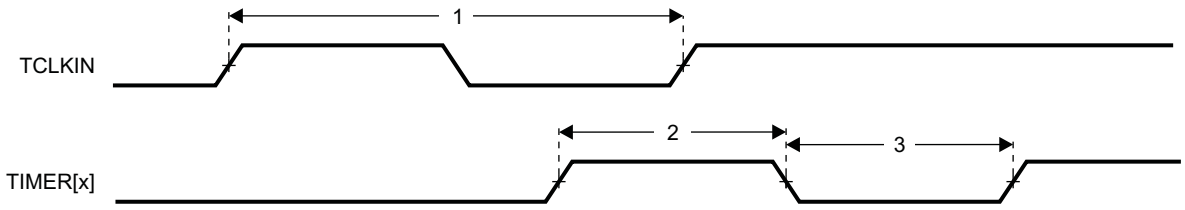



**図 5-18. Timer Timing**

## 5.12.7 Ethernet Media Access Controller (EMAC) and Switch

### 5.12.7.1 Ethernet MAC and Switch Electrical Data and Timing

The Ethernet MAC and Switch implemented in the device supports GMII mode, but the design does not pin out 9 of the 24 GMII signals. This was done to reduce the total number of package terminals. Therefore, the device does not support GMII mode. MII mode is supported with the remaining GMII signals.

The *AM437x Sitara Processors Technical Reference Manual* and this document may reference internal signal names when discussing peripheral input and output signals because many of the package terminals can be multiplexed to one of several peripheral signals. For example, the terminal names for port 1 of the Ethernet MAC and switch have been changed from GMII to MII to indicate their Mode 0 function, but the internal signal is named GMII. However, documents that describe the Ethernet switch reference these signals by their internal signal name. For a cross-reference of internal signal names to terminal names, see Table 4-10.

Operation of the Ethernet MAC and switch in RGMII mode is not supported for OPP50.

**表 5-22. Ethernet MAC and Switch Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_R$ | Input signal rise time | 1(1) | | 5(1) | ns |
| $t_F$ | Input signal fall time | 1(1) | | 5(1) | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | 3 | | 30 | pF |

(1) Except when specified otherwise.

#### 5.12.7.1.1 Ethernet MAC/Switch MDIO Electrical Data and Timing

**表 5-23. Timing Requirements for MDIO_DATA**

(see 図 5-19)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{su(MDIO-MDC)}$ | Setup time, MDIO valid before MDC high | 90 | | | ns |
| 2 | $t_{h(MDIO-MDC)}$ | Hold time, MDIO valid from MDC high | 0 | | | ns |

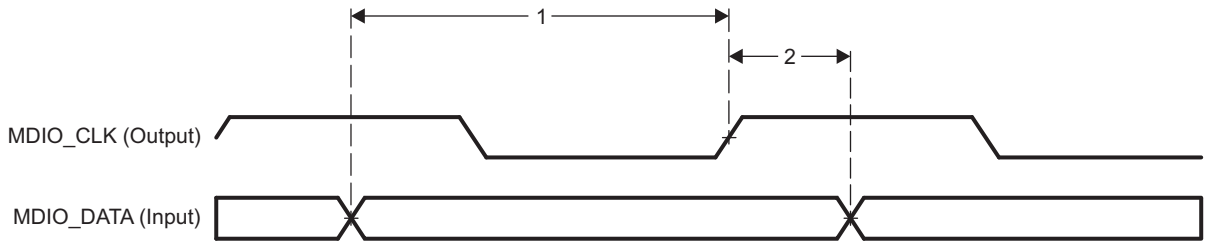



**図 5-19. MDIO_DATA Timing - Input Mode**

**表 5-24. Switching Characteristics for MDIO_CLK**

(see 図 5-20)

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(MDC)}$ | Cycle time, MDC | 400 | | | ns |
| 2 | $t_{w(MDCH)}$ | Pulse duration, MDC high | 160 | | | ns |
| 3 | $t_{w(MDCL)}$ | Pulse duration, MDC low | 160 | | | ns |
| 4 | $t_{t(MDC)}$ | Transition time, MDC | | | 5 | ns |

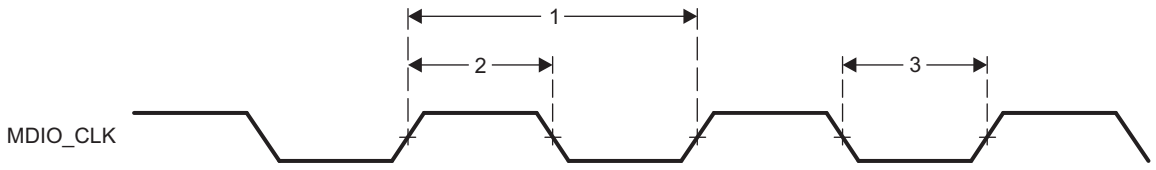



**図 5-20. MDIO_CLK Timing**

**表 5-25. MDIO Switching Characteristics - MDIO_DATA**

(see 図 5-21)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{d(MDC-MDIO)}$ | Delay time, MDC high to MDIO valid | 10 | | (P*0.5)–10 (1) | ns |

(1) P = MDIO_CLK period

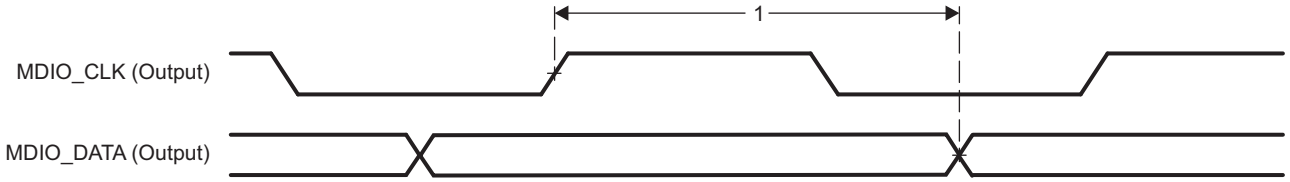



**図 5-21. MDIO_DATA Timing - Output Mode**

### *5.12.7.1.2 Ethernet MAC and Switch MII Electrical Data and Timing*

**表 5-26. Timing Requirements for GMII[x]_RXCLK - MII Mode**

(see 図 5-22)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(RX\_CLK)}$ | Cycle time, RX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_{w(RX\_CLKH)}$ | Pulse Duration, RX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_{w(RX\_CLKL)}$ | Pulse Duration, RX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_{t(RX\_CLK)}$ | Transition time, RX_CLK | | | 5 | | | 5 | ns |

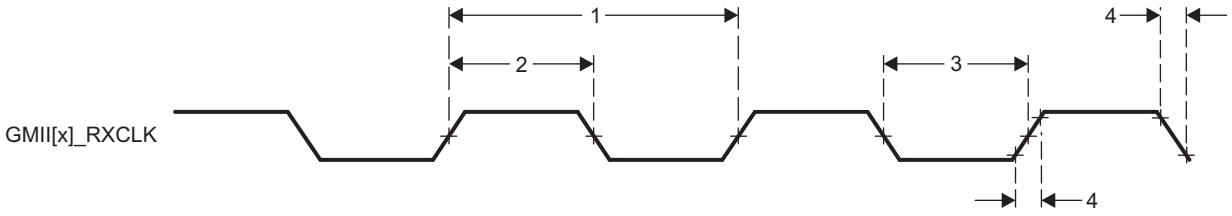



**図 5-22. GMII[x]_RXCLK Timing - MII Mode**

**表 5-27. Timing Requirements for GMII[x]_TXCLK - MII Mode**

(see 図 5-23)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(TX\_CLK)}$ | Cycle time, TX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_{w(TX\_CLKH)}$ | Pulse Duration, TX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_{w(TX\_CLKL)}$ | Pulse Duration, TX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_{t(TX\_CLK)}$ | Transition time, TX_CLK | | | 5 | | | 5 | ns |

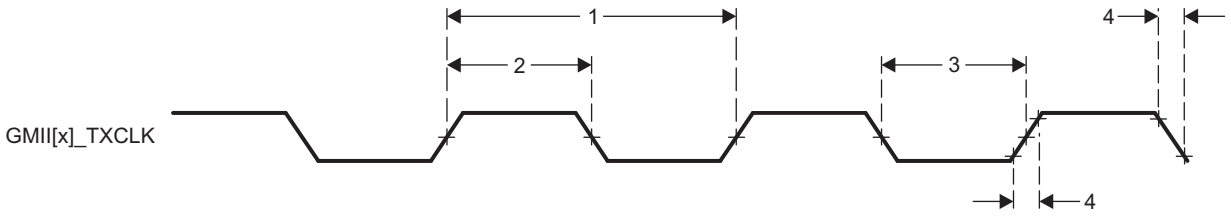



**図 5-23. GMII[x]_TXCLK Timing - MII Mode**

**表 5-28. Timing Requirements for GMII[x]_RXD[3:0], GMII[x]_RXDV, and GMII[x]_RXER - MII Mode**

(see 図 5-24)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(RXD\text{-}RX\_CLK)}$ | Setup time, RXD[3:0] valid before RX_CLK | 8 | | | 8 | | | ns |
| | $t_{su(RX\_DV\text{-}RX\_CLK)}$ | Setup time, RX_DV valid before RX_CLK | | | | | | | |
| | $t_{su(RX\_ER\text{-}RX\_CLK)}$ | Setup time, RX_ER valid before RX_CLK | | | | | | | |
| 2 | $t_{h(RX\_CLK\text{-}RXD)}$ | Hold time RXD[3:0] valid after RX_CLK | 8 | | | 8 | | | ns |
| | $t_{h(RX\_CLK\text{-}RX\_DV)}$ | Hold time RX_DV valid after RX_CLK | | | | | | | |
| | $t_{h(RX\_CLK\text{-}RX\_ER)}$ | Hold time RX_ER valid after RX_CLK | | | | | | | |

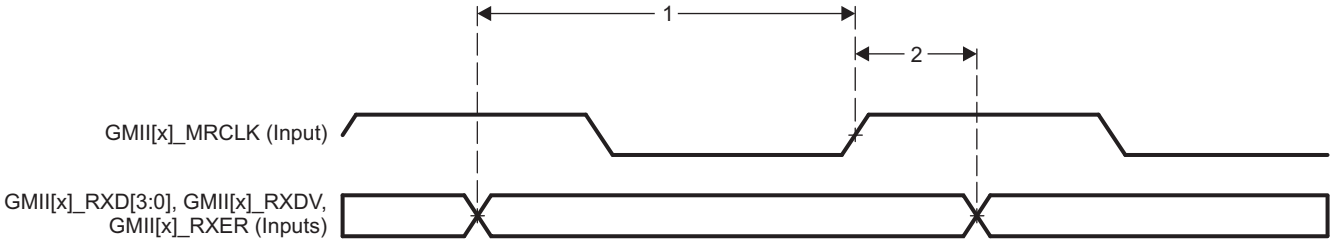



**図 5-24. GMII[x]_RXD[3:0], GMII[x]_RXDV, GMII[x]_RXER Timing - MII Mode**

### 表 5-29. Switching Characteristics for GMII[x]_TXD[3:0], and GMII[x]_TXEN - MII Mode

(see 図 5-25)

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{d(TX\_CLK-TXD)}$ | Delay time, TX_CLK high to TXD[3:0] valid | 5 | | 25 | 5 | | 25 | ns |
| | $t_{d(TX\_CLK-TX\_EN)}$ | Delay time, TX_CLK to TX_EN valid | | | | | | | |

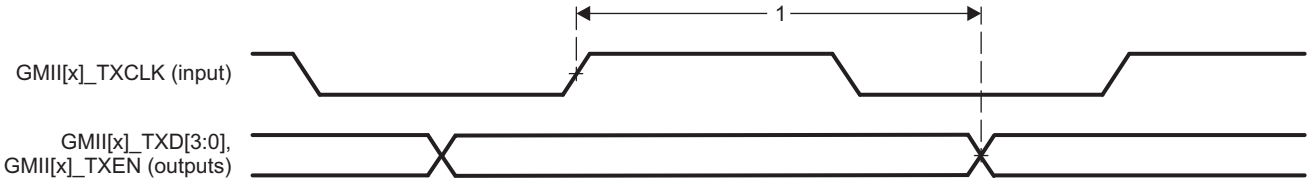



**図 5-25. GMII[x]_TXD[3:0], GMII[x]_TXEN Timing - MII Mode**

#### 5.12.7.1.3 Ethernet MAC and Switch RMII Electrical Data and Timing

**表 5-30. Timing Requirements for RMII[x]_REFCLK - RMII Mode**

(see 図 5-26)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(REF\_CLK)}$ | Cycle time, REF_CLK | 19.999 | | 20.001 | ns |
| 2 | $t_{w(REF\_CLKH)}$ | Pulse Duration, REF_CLK high | 7 | | 13 | ns |
| 3 | $t_{w(REF\_CLKL)}$ | Pulse Duration, REF_CLK low | 7 | | 13 | ns |

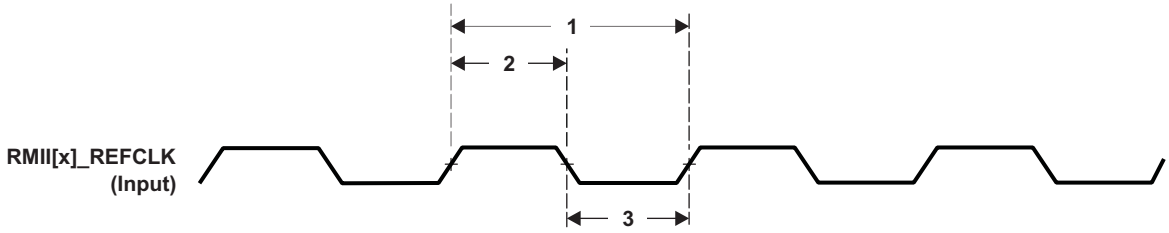



**図 5-26. RMII[x]_REFCLK Timing - RMII Mode**

**表 5-31. Timing Requirements for RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER - RMII Mode**

(see 図 5-27)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{su(RXD-REF\_CLK)}$ | Setup time, RXD[1:0] valid before REF_CLK | 4 | | | ns |
| | $t_{su(CRS\_DV-REF\_CLK)}$ | Setup time, CRS_DV valid before REF_CLK | | | | |
| | $t_{su(RX\_ER-REF\_CLK)}$ | Setup time, RX_ER valid before REF_CLK | | | | |
| 2 | $t_{h(REF\_CLK-RXD)}$ | Hold time RXD[1:0] valid after REF_CLK | 2 | | | ns |
| | $t_{h(REF\_CLK-CRS\_DV)}$ | Hold time, CRS_DV valid after REF_CLK | | | | |
| | $t_{h(REF\_CLK-RX\_ER)}$ | Hold time, RX_ER valid after REF_CLK | | | | |

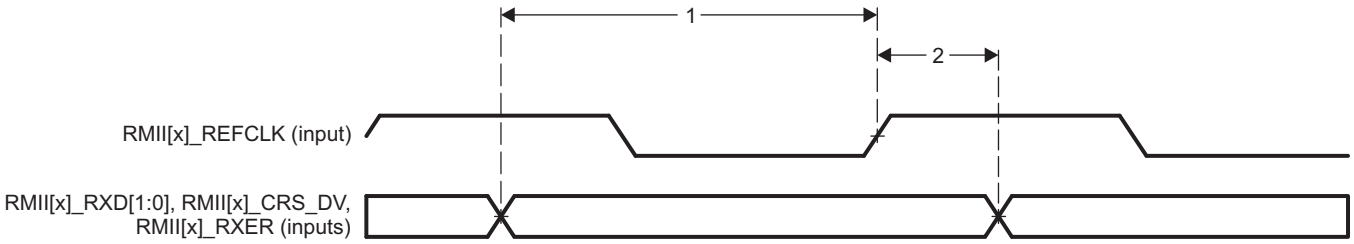



**図 5-27. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing - RMII Mode**

**表 5-32. Switching Characteristics for RMII[x]_TXD[1:0], and RMII[x]_TXEN - RMII Mode**

(see 図 5-28)

| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{d(REF\_CLK-TXD)}$ | Delay time, REF_CLK high to TXD[1:0] valid | 2 | | 14.2 | ns |
| | $t_{d(REF\_CLK-TXEN)}$ | Delay time, REF_CLK to TXEN valid | | | | |

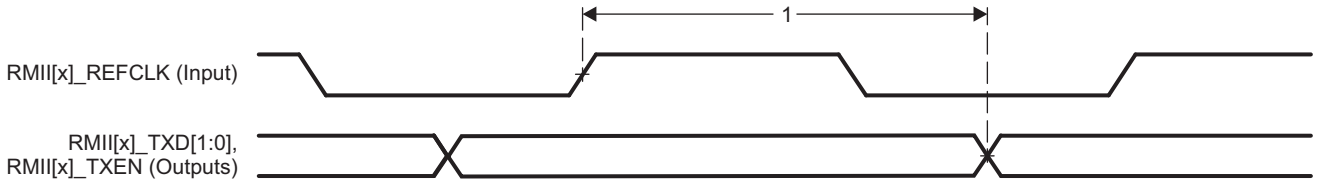



**図 5-28. RMII[x]_TXD[1:0], RMII[x]_TXEN Timing - RMII Mode**

#### 5.12.7.1.4 Ethernet MAC and Switch RGMII Electrical Data and Timing

**表 5-33. Timing Requirements for RGMII[x]_RCLK - RGMII Mode**

(see 図 5-29)

| NO. | | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(RXC)}$ | Cycle time, RXC | 360 | | 440 | 36 | | 44 | 7.2 | | 8.8 | ns |
| 2 | $t_{w(RXCH)}$ | Pulse duration, RXC high | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 3 | $t_{w(RXCL)}$ | Pulse duration, RXC low | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 4 | $t_{t(RXC)}$ | Transition time, RXC | | | 0.75 | | | 0.75 | | | 0.75 | ns |

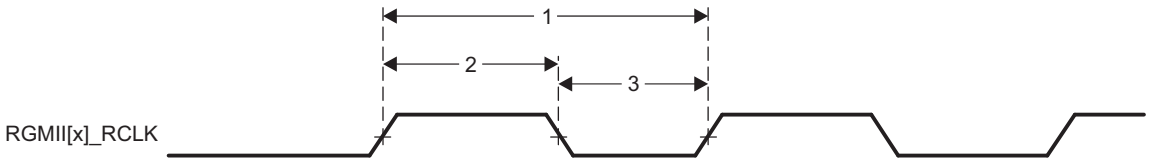
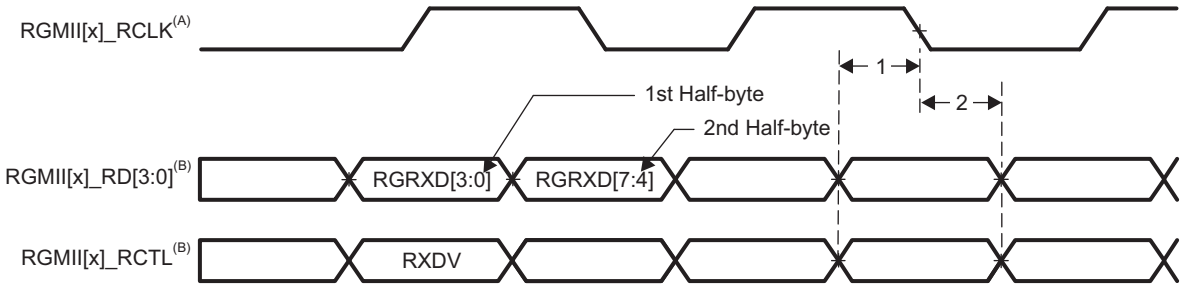



**図 5-29. RGMII[x]_RCLK Timing - RGMII Mode**

**表 5-34. Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL - RGMII Mode**

(see 図 5-30)

| NO. | | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(RD-RXC)}$ | Setup time, RD[3:0] valid before RXC high or low | 1 | | | 1 | | | 1 | | | ns |
| | $t_{su(RX\_CTL-RXC)}$ | Setup time, RX_CTL valid before RXC high or low | 1 | | | 1 | | | 1 | | | |
| 2 | $t_{h(RXC-RD)}$ | Hold time, RD[3:0] valid after RXC high or low | 1 | | | 1 | | | 1 | | | ns |
| | $t_{h(RXC-RX\_CTL)}$ | Hold time, RX_CTL valid after RXC high or low | 1 | | | 1 | | | 1 | | | |
| 3 | $t_{t(RD)}$ | Transition time, RD | | | 0.75 | | | 0.75 | | | 0.75 | ns |
| | $t_{t(RX\_CTL)}$ | Transition time, RX_CTL | | | 0.75 | | | 0.75 | | | 0.75 | |




A. RGMII[x]_RCLK must be externally delayed relative to the RGMII[x]_RD[3:0] and RGMII[x]_RCTL signals to meet the respective timing requirements.

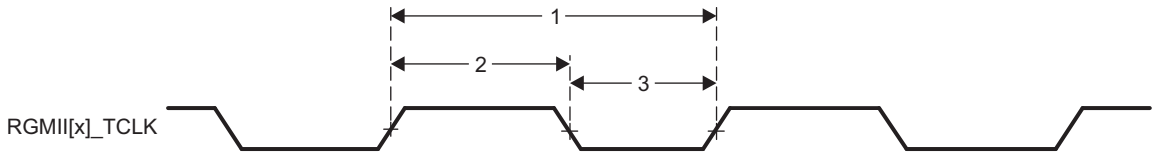
B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RCLK and data bits 7-4 on the falling edge of RGMII[x]_RCLK. Similarly, RGMII[x]_RCTL carries RXDV on rising edge of RGMII[x]_RCLK and RXERR on falling edge of RGMII[x]_RCLK.

**図 5-30. RGMII[x]_RD[3:0], RGMII[x]_RCTL Timing - RGMII Mode**

### 表 5-35. Switching Characteristics for RGMII[x]_TCLK - RGMII Mode

(see 図 5-31)

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(TXC)}$ | Cycle time, TXC | 360 | | 440 | 36 | | 44 | 7.2 | | 8.8 | ns |
| 2 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |
| 3 | $t_{w(TXCL)}$ | Pulse duration, TXC low | 160 | | 240 | 16 | | 24 | 3.6 | | 4.4 | ns |

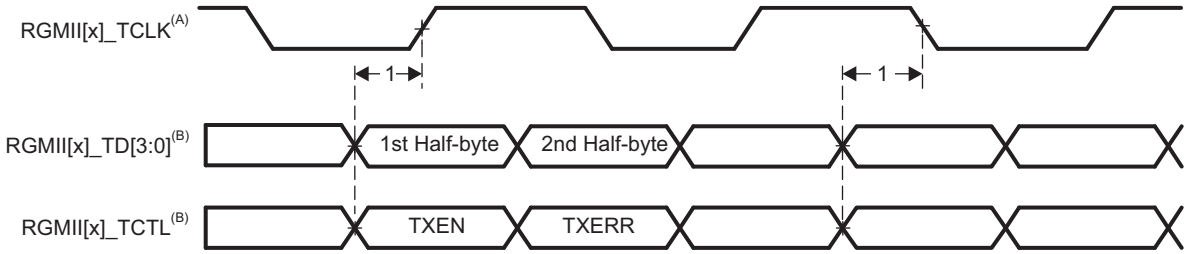



### 図 5-31. RGMII[x]_TCLK Timing - RGMII Mode

### 表 5-36. Switching Characteristics for RGMII[x]_TD[3:0], and RGMII[x]_TCTL - RGMII Mode

(see 図 5-32)

| NO. | PARAMETER | | 10 Mbps | | | 100 Mbps | | | 1000 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{sk(TD-TXC)}$ | TD to TXC output skew | -0.5 | | 0.5 | -0.5 | | 0.5 | -0.5 | | 0.5 | ns |
| | $t_{sk(TX\_CTL-TXC)}$ | TX_CTL to TXC output skew | -0.5 | | 0.5 | -0.5 | | 0.5 | -0.5 | | 0.5 | |




A. The Ethernet MAC and switch implemented in the device supports internal TX delay mode.

B. Data and control information is transmitted using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TCLK and data bits 7-4 on the falling edge of RGMII[x]_TCLK. Similarly, RGMII[x]_TCTL carries TXEN on rising edge of RGMII[x]_TCLK and TXERR of falling edge of RGMII[x]_TCLK.

### 図 5-32. RGMII[x]_TD[3:0], RGMII[x]_TCTL Timing - RGMII Mode

### 5.12.8 External Memory Interfaces

The device includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- LPDDR2, DDR3, and DDR3L Memory Interface (EMIF)

#### 5.12.8.1 General-Purpose Memory Controller (GPMC)

注

For more information, see the Memory Subsystem and General-Purpose Memory Controller section of the *AM437x Sitara Processors Technical Reference Manual*.

The GPMC is the unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

##### 5.12.8.1.1 GPMC and NOR Flash—Synchronous Mode

表 5-38 and 表 5-39 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-33 through 図 5-37).

**表 5-37. GPMC and NOR Flash Timing Conditions—Synchronous Mode**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_R$ | Input signal rise time | 0.3 | | 1.8 | ns |
| $t_F$ | Input signal fall time | 0.3 | | 1.8 | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | 3 | | 30 | pF |

**表 5-38. GPMC and NOR Flash Timing Requirements—Synchronous Mode**

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| F12 | $t_{su(dV-clkH)}$ | Setup time, input data gpmc_ad[15:0] valid before output clock gpmc_clk high | 3.5 | | 13.2 | | ns |
| F13 | $t_{h(clkH-dV)}$ | Hold time, input data gpmc_ad[15:0] valid after output clock gpmc_clk high | 2.5 | | 2.75 | | ns |
| F21 | $t_{su(waitV-clkH)}$ | Setup time, input wait gpmc_wait[x](1) valid before output clock gpmc_clk high | 3.5 | | 13.2 | | ns |
| F22 | $t_{h(clkH-waitV)}$ | Hold time, input wait gpmc_wait[x](1) valid after output clock gpmc_clk high | 2.5 | | 2.5 | | ns |

(1) In gpmc_wait[x], x is equal to 0 or 1.

## 表 5-39. GPMC and NOR Flash Switching Characteristics—Synchronous Mode

| NO. | PARAMETER | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| F0 | $1 / t_{c(clk)}$ | Frequency[1], output clock gpmc_clk | | | 100 | | 50 | MHz |
| F1 | $t_{w(clkH)}$ | Typical pulse duration, output clock gpmc_clk high | | 0.5P[2] | 0.5P[2] | 0.5P[2] | 0.5P[2] | ns |
| F1 | $t_{w(clkL)}$ | Typical pulse duration, output clock gpmc_clk low | | 0.5P[2] | 0.5P[2] | 0.5P[2] | 0.5P[2] | ns |
| | $t_{dc(clk)}$ | Duty cycle error, output clock gpmc_clk | | –500 | 500 | –500 | 500 | ps |
| | $t_{J(clk)}$ | Jitter standard deviation[3], output clock gpmc_clk | | | 33.33 | | 33.33 | ps |
| F2 | $t_{d(clkH-csnV)}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x][4] transition | | F[5] – 2.2 | F[5] + 4.5 | F[5] – 3.2 | F[5] + 9.5 | ns |
| F3 | $t_{d(clkH-csnIV)}$ | Delay time, output clock gpmc_clk rising edge to output chip select gpmc_csn[x][4] invalid | | E[6] – 2.2 | E[6] + 4.5 | E[6] – 3.2 | E[6] + 9.5 | ns |
| F4 | $t_{d(aV-clk)}$ | Delay time, output address gpmc_a[27:1] valid to output clock gpmc_clk first edge | | B[7] – 4.5 | B[7] + 3.1 | B[7] – 5.5 | B[7] + 13.1 | ns |
| F5 | $t_{d(clkH-aIV)}$ | Delay time, output clock gpmc_clk rising edge to output address gpmc_a[27:1] invalid | | -2.3 | 4.5 | -3.3 | 15.3 | ns |
| F6 | $t_{d(be[x]nV-clk)}$ | Delay time, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n valid to output clock gpmc_clk first edge | | B[7] - 1.9 | B[7] + 2.3 | B[7] – 2.9 | B[7] + 12.3 | ns |
| F7 | $t_{d(clkH-be[x]nIV)}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n invalid[8] | | D[9] – 2.3 | D[9] + 1.9 | D[9] – 3.3 | D[9] + 6.9 | ns |
| F7 | $t_{d(clkL-be[x]nIV)}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 invalid[10] | | D[9] – 2.3 | D[9] + 1.9 | D[9] – 3.3 | D[9] + 6.9 | ns |
| F7 | $t_{d(clkL-be[x]nIV)}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 invalid[11] | | D[9] – 2.3 | D[9] + 1.9 | D[9] – 3.3 | D[9] + 11.9 | ns |
| F8 | $t_{d(clkH-advn)}$ | Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale transition | | G[12] – 2.3 | G[12] + 4.5 | G[12] – 3.3 | G[12] + 9.5 | ns |
| F9 | $t_{d(clkH-advnIV)}$ | Delay time, output clock gpmc_clk rising edge to output address valid and address latch enable gpmc_advn_ale invalid | | D[9] – 2.3 | D[9] + 4.5 | D[9] – 3.3 | D[9] + 9.5 | ns |
| F10 | $t_{d(clkH-oen)}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen transition | | H[13] – 2.3 | H[13] + 3.5 | H[13] – 3.3 | H[13] + 8.5 | ns |
| F11 | $t_{d(clkH-oenIV)}$ | Delay time, output clock gpmc_clk rising edge to output enable gpmc_oen invalid | | H[13] – 2.3 | H[13] + 3.5 | H[13] – 3.3 | H[13] + 8.5 | ns |
| F14 | $t_{d(clkH-wen)}$ | Delay time, output clock gpmc_clk rising edge to output write enable gpmc_wen transition | | I[14] – 2.3 | I[14] + 4.5 | I[14] – 3.3 | I[14] + 9.5 | ns |
| F15 | $t_{d(clkH-do)}$ | Delay time, output clock gpmc_clk rising edge to output data gpmc_ad[15:0] transition[8] | | J[15] – 2.3 | J[15] + 2.7 | J[15] – 3.3 | J[15] + 7.7 | ns |
| F15 | $t_{d(clkL-do)}$ | Delay time, gpmc_clk falling edge to gpmc_ad[15:0] data bus transition[10] | | J[15] – 2.3 | J[15] + 2.7 | J[15] – 3.3 | J[15] + 7.7 | ns |
| F15 | $t_{d(clkL-do)}$ | Delay time, gpmc_clk falling edge to gpmc_ad[15:0] data bus transition[11] | | J[15] – 2.3 | J[15] + 2.7 | J[15] – 3.3 | J[15] + 12.7 | ns |
| F17 | $t_{d(clkH-be[x]n)}$ | Delay time, output clock gpmc_clk rising edge to output lower byte enable and command latch enable gpmc_be0n_cle transition[8] | | J[15] – 2.3 | J[15] + 1.9 | J[15] – 3.3 | J[15] + 6.9 | ns |
| F17 | $t_{d(clkL-be[x]n)}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 transition[10] | | J[15] – 2.3 | J[15] + 1.9 | J[15] – 3.3 | J[15] + 6.9 | ns |
| F17 | $t_{d(clkL-be[x]n)}$ | Delay time, gpmc_clk falling edge to gpmc_nbe0_cle, gpmc_nbe1 transition[11] | | J[15] – 2.3 | J[15] + 1.9 | J[15] – 3.3 | J[15] + 11.9 | ns |
| F18 | $t_{w(csnV)}$ | Pulse duration, output chip select gpmc_csn[x][4] low | Read | A[16] | | A[16] | | ns |
| | | | Write | A[16] | | A[16] | | ns |
| F19 | $t_{w(be[x]nV)}$ | Pulse duration, output lower byte enable and command latch enable gpmc_be0n_cle, output upper byte enable gpmc_be1n low | Read | C[17] | | C[17] | | ns |
| | | | Write | C[17] | | C[17] | | ns |

表 5-39. GPMC and NOR Flash Switching Characteristics—Synchronous Mode (continued)

| NO. | PARAMETER | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| F20 | $t_{w(advnV)}$ | Pulse duration, output address valid and address latch enable gpmc_advn_ale low | Read | K(18) | | K(18) | | ns |
| | | | Write | K(18) | | K(18) | | ns |

(1) Related to the gpmc_clk output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.

(2) P = gpmc_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

(5) For csn falling edge (CS activated):
- Case GpmcFCLKDivider = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(19)
- Case GpmcFCLKDivider = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(19) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(19) otherwise
- Case GpmcFCLKDivider = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(19) if ((CSOnTime – ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(19) if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(19) if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(6) For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)
For burst write: E = (CSWrOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)

(7) B = ClkActivationTime × GPMC_FCLK(19)

(8) First transfer only for CLK DIV 1 mode.

(9) For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)
For burst write: D = (WrCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(19)

(10) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(11) Half cycle of GPMC_CLK_OUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLK_OUT divide down from GPMC_FCLK.

(12) For ADV falling edge (ADV activated):
- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GpmcFCLKDivider = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19)
- Case GpmcFCLKDivider = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(19) otherwise
- Case GpmcFCLKDivider = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(19) if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)

- G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[19] if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK[19] if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(13) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GpmcFCLKDivider = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19]
- Case GpmcFCLKDivider = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19] if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] otherwise
- Case GpmcFCLKDivider = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19] if ((OEOnTime – ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GpmcFCLKDivider = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19]
- Case GpmcFCLKDivider = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19] if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] otherwise
- Case GpmcFCLKDivider = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[19] if ((OEOffTime – ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK[19] if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(14) For WE falling edge (WE activated):

- Case GpmcFCLKDivider = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[19]
- Case GpmcFCLKDivider = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[19] if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[19] if ((WEOnTime – ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GpmcFCLKDivider = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK [19]
- Case GpmcFCLKDivider = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[19] if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] otherwise
- Case GpmcFCLKDivider = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[19] if ((WEOffTime – ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[19] if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

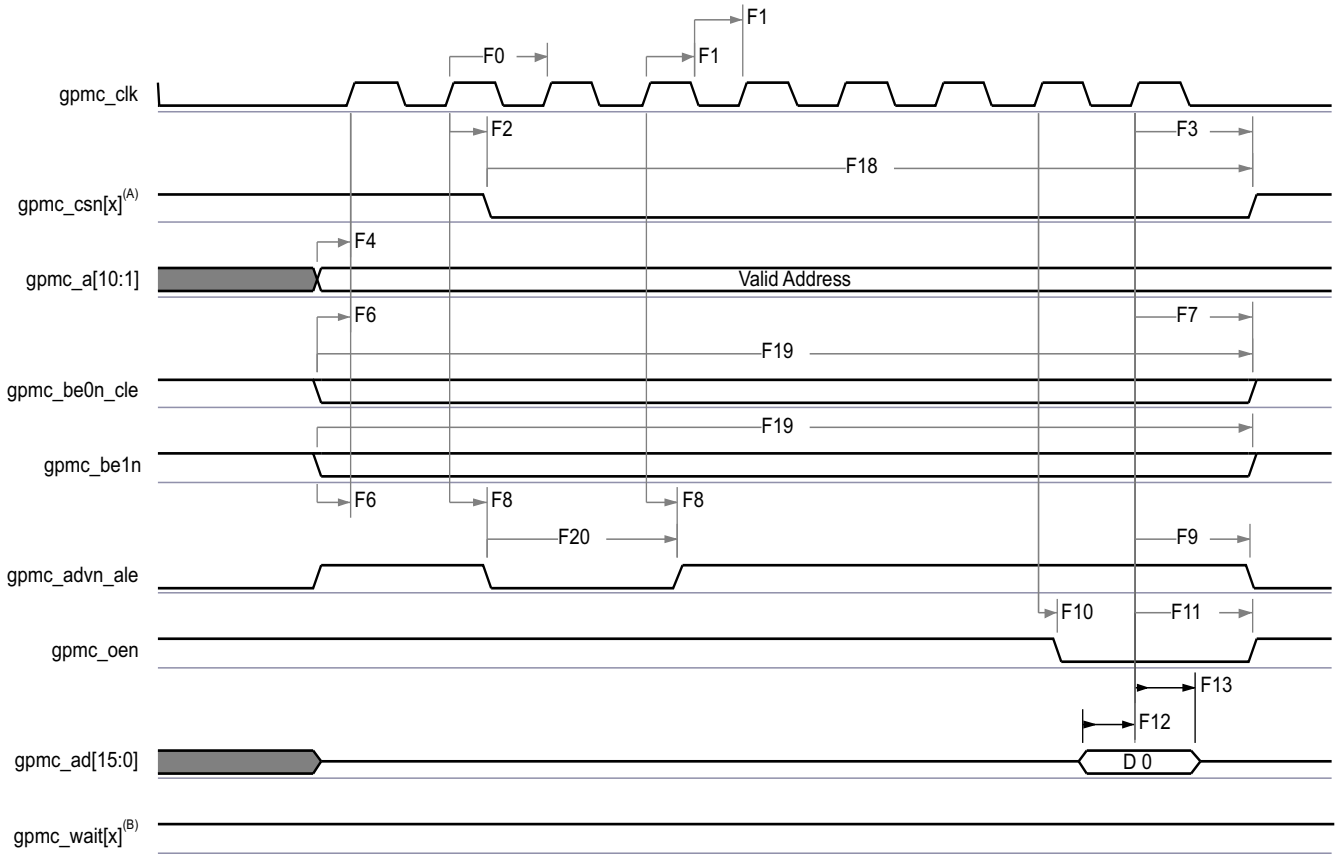
(15) J = GPMC_FCLK[19]

(16) For single read: A = (CSRdOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
With n being the page burst access number.

(17) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[19]
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
For burst write: C = (WrCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
With n being the page burst access number.

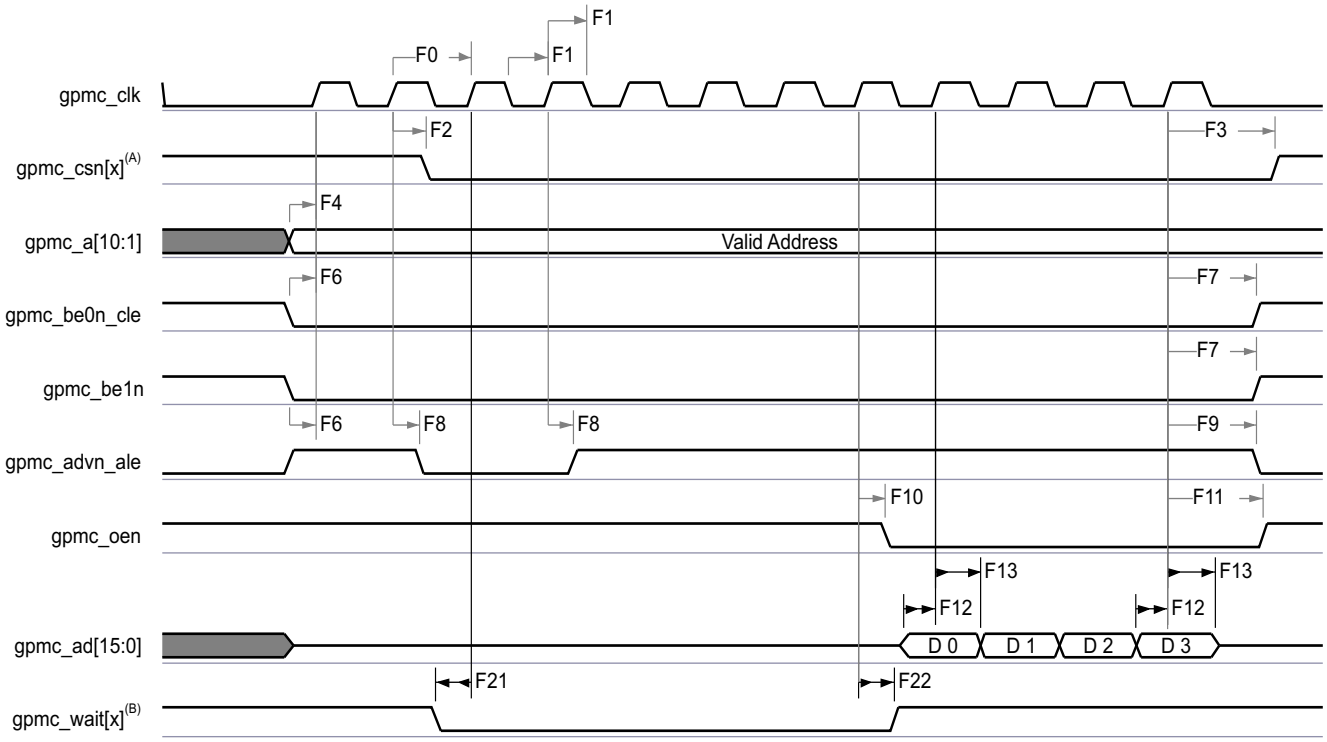
(18) For read: K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]
For write: K = (ADVWrOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[19]

(19) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.



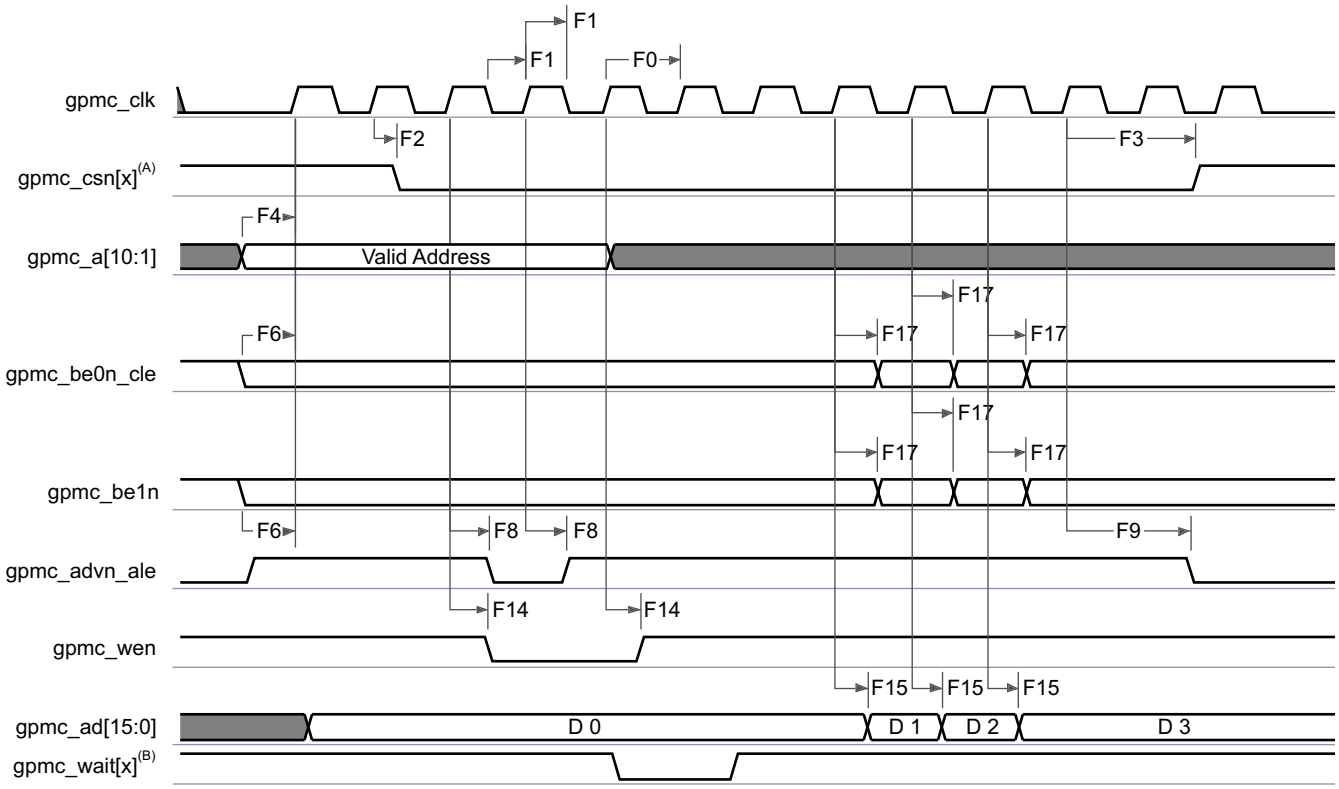

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.
B. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-33. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)**



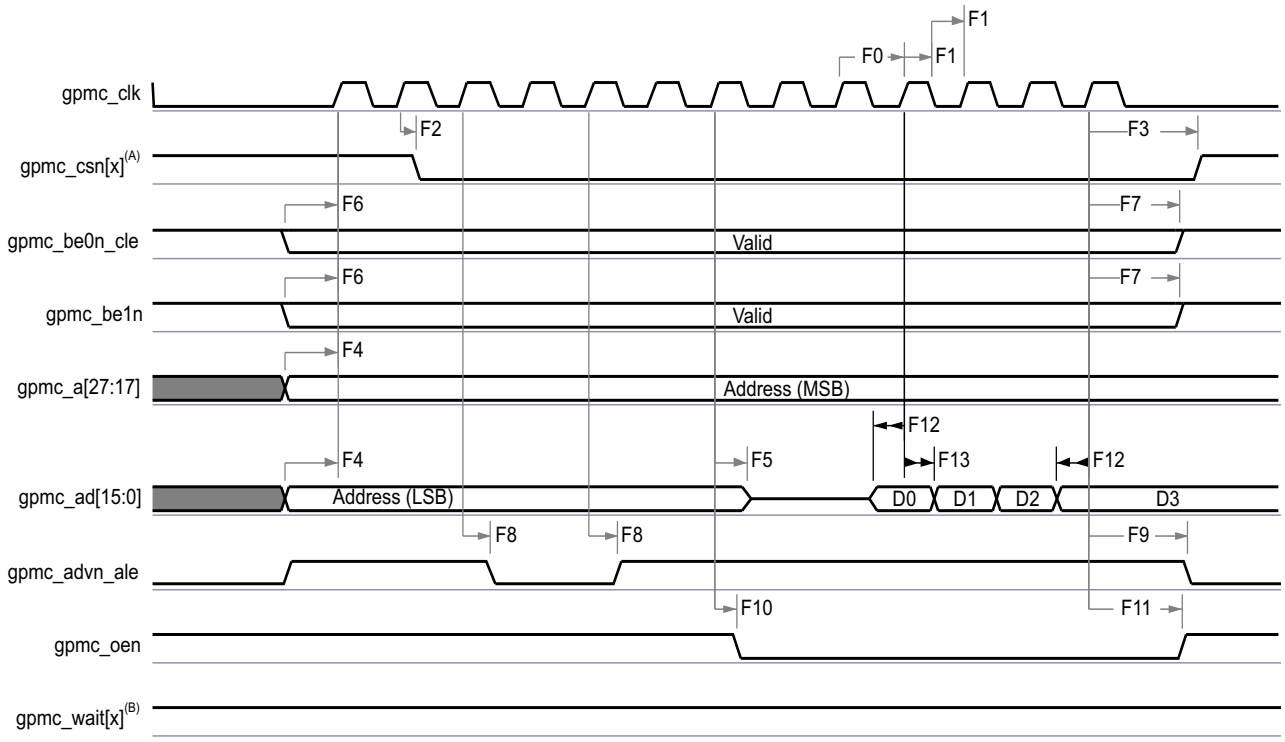

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.
B. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-34. GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0)**



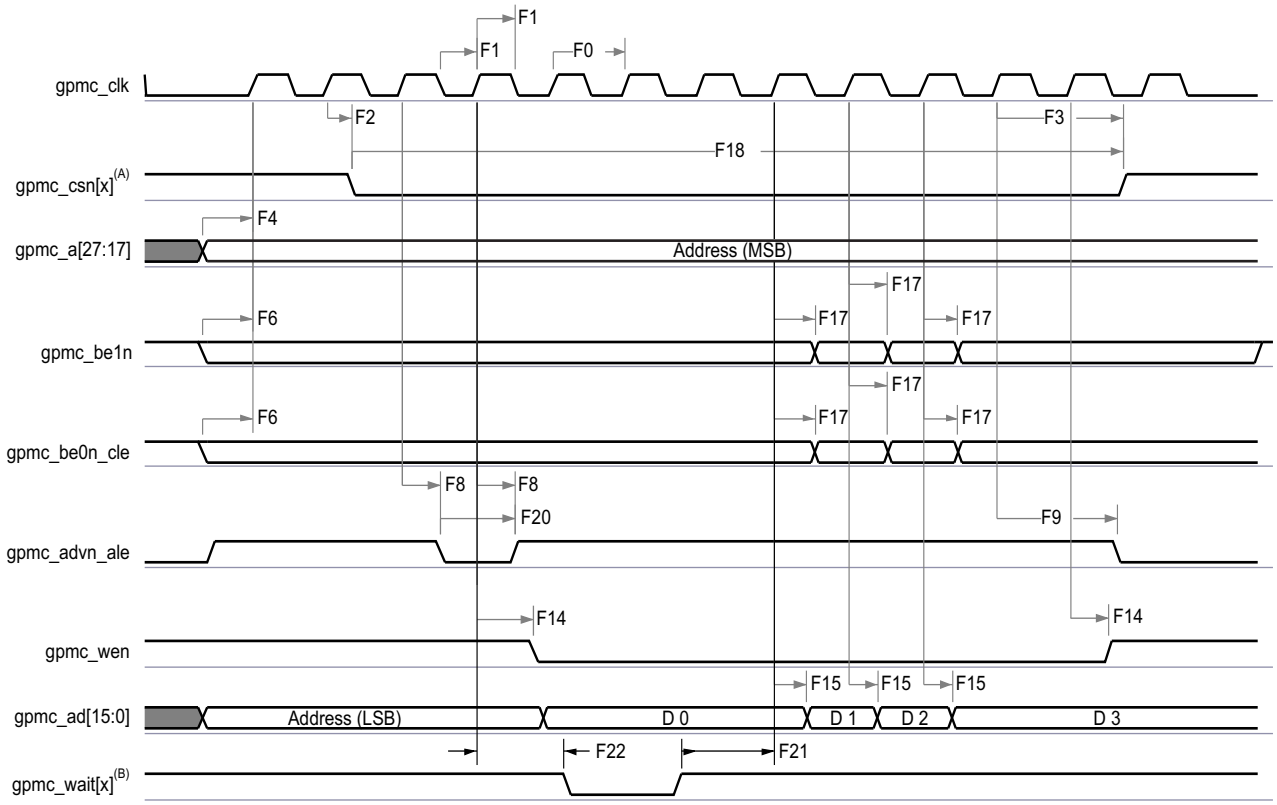

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.
B. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-35. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)**




A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.
B. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-36. GPMC and Multiplexed NOR Flash—Synchronous Burst Read**




A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.
B. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-37. GPMC and Multiplexed NOR Flash—Synchronous Burst Write**

#### 5.12.8.1.2 GPMC and NOR Flash—Asynchronous Mode

表 5-41 and 表 5-42 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-38 through 図 5-43).

**表 5-40. GPMC and NOR Flash Timing Conditions—Asynchronous Mode**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_R$ | Input signal rise time | 0.3 | | 1.8 | ns |
| $t_F$ | Input signal fall time | 0.3 | | 1.8 | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | 3 | | 30 | pF |

**表 5-41. GPMC and NOR Flash Internal Timing Parameters—Asynchronous Mode(1)(2)**

| NO. | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| FI1 | Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI2 | Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK(3) | | 4 | | 4 | ns |
| FI3 | Delay time, output chip select gpmc_csn[x] generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI4 | Delay time, output address gpmc_a[27:1] generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI5 | Delay time, output address gpmc_a[27:1] valid from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI6 | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI7 | Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI8 | Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK(3) | | 6.5 | | 6.5 | ns |
| FI9 | Skew, internal functional clock GPMC_FCLK(3) | | 100 | | 100 | ps |

(1) The internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

### 表 5-42. GPMC and NOR Flash Timing Requirements—Asynchronous Mode

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FA5[1] | $t_{acc(d)}$ | Data access time | | H[4] | | H[4] | ns |
| FA20[2] | $t_{acc1\text{-}pgmode(d)}$ | Page mode successive data access time | | P[5] | | P[5] | ns |
| FA21[3] | $t_{acc2\text{-}pgmode(d)}$ | Page mode first data access time | | H[4] | | H[4] | ns |

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.

(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

(3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

(4) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]

(5) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]

(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

### 表 5-43. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode

| NO. | PARAMETER | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| FA0 | $t_{w(be[x]nV)}$ | Pulse duration, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid time | Read | | N[1] | | N[1] | ns |
| | | | Write | | N[1] | | N[1] | |
| FA1 | $t_{w(csnV)}$ | Pulse duration, output chip select gpmc_csn[x][2] low | Read | | A[3] | | A[3] | ns |
| | | | Write | | A[3] | | A[3] | |
| FA3 | $t_{d(csnV\text{-}advnIV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output address valid and address latch enable gpmc_advn_ale invalid | Read | B[4] – 0.2 | B[4] + 2.0 | B[4] – 0.2 | B[4] + 2.0 | ns |
| | | | Write | B[4] – 0.2 | B[4] + 2.0 | B[4] – 0.2 | B[4] + 2.0 | |
| FA4 | $t_{d(csnV\text{-}oenIV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output enable gpmc_oen invalid (Single read) | | C[5] – 0.2 | C[5] + 2.0 | C[5] – 0.2 | C[5] + 2.0 | ns |
| FA9 | $t_{d(aV\text{-}csnV)}$ | Delay time, output address gpmc_a[27:1] valid to output chip select gpmc_csn[x][2] valid | | J[6] – 0.2 | J[6] + 2.0 | J[6] – 0.2 | J[6] + 2.0 | ns |
| FA10 | $t_{d(be[x]nV\text{-}csnV)}$ | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle, output upper-byte enable gpmc_be1n valid to output chip select gpmc_csn[x][2] valid | | J[6] – 0.2 | J[6] + 2.0 | J[6] – 0.2 | J[6] + 2.0 | ns |
| FA12 | $t_{d(csnV\text{-}advnV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output address valid and address latch enable gpmc_advn_ale valid | | K[7] – 0.2 | K[7] + 2.0 | K[7] – 0.2 | K[7] + 2.0 | ns |
| FA13 | $t_{d(csnV\text{-}oenV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output enable gpmc_oen valid | | L[8] – 0.2 | L[8] + 2.0 | L [8] – 0.2 | L[8] + 2.0 | ns |
| FA16 | $t_{w(aIV)}$ | Pulse durationm output address gpmc_a[26:1] invalid between 2 successive read and write accesses | | G[9] | | G[9] | | ns |
| FA18 | $t_{d(csnV\text{-}oenIV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output enable gpmc_oen invalid (Burst read) | | I[10] – 0.2 | I[10] + 2.0 | I[10] – 0.2 | I[10] + 2.0 | ns |
| FA20 | $t_{w(aV)}$ | Pulse duration, output address gpmc_a[27:1] valid — 2nd, 3rd, and 4th accesses | | D[11] | | D[11] | | ns |
| FA25 | $t_{d(csnV\text{-}wenV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output write enable gpmc_wen valid | | E[12] – 0.2 | E[12] + 2.0 | E[12] – 0.2 | E[12] + 2.0 | ns |
| FA27 | $t_{d(csnV\text{-}wenIV)}$ | Delay time, output chip select gpmc_csn[x][2] valid to output write enable gpmc_wen invalid | | F[13] – 0.2 | F[13] + 2.0 | F[13] – 0.2 | F[13] + 2.0 | ns |

表 5-43. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| FA28 | $t_{d(wenV-dV)}$ | Delay time, output write enable gpmc_ wen valid to output data gpmc_ad[15:0] valid | | 2.8 | | 5 | ns |
| FA29 | $t_{d(dV-csnV)}$ | Delay time, output data gpmc_ad[15:0] valid to output chip select gpmc_csn[x](2) valid | J(6) – 0.2 | J(6) + 2.8 | J(6) – 0.2 | J(6) + 2.8 | ns |
| FA37 | $t_{d(oenV-aIV)}$ | Delay time, output enable gpmc_oen valid to output address gpmc_ad[15:0] phase end | | 2.8 | | 2.8 | ns |

(1) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: N = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: N = (WrCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(2) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.

(3) For single read: A = (CSRdOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: A = (CSWrOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
with n being the page burst access number

(4) For reading: B = ((ADVRdOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)
For writing: B = ((ADVWrOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(5) C = ((OEOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(6) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK(14)

(7) K = ((ADVOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(8) L = ((OEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(9) G = Cycle2CycleDelay × GPMC_FCLK(14)

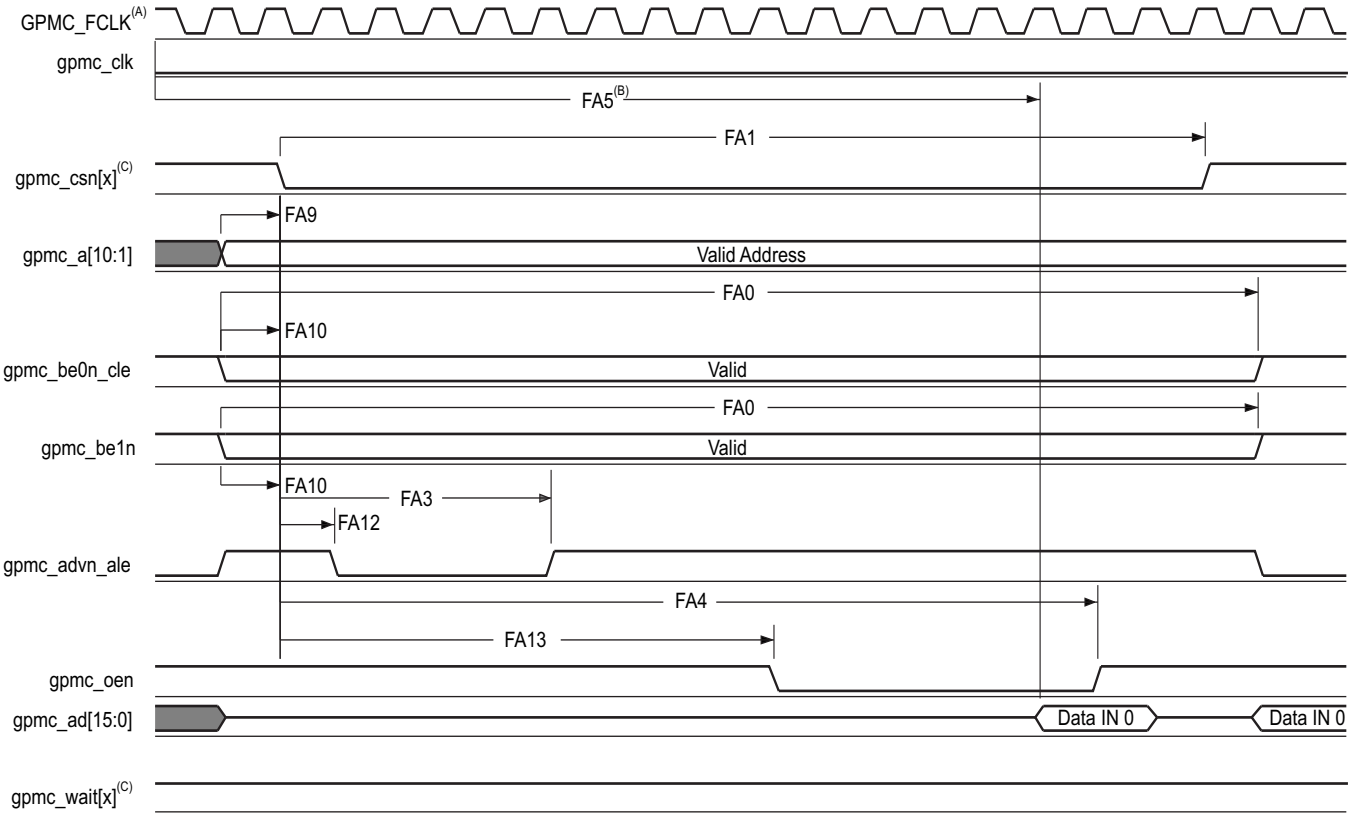
(10) I = ((OEOffTime + (n – 1) × PageBurstAccessTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(11) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(12) E = ((WEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(13) F = ((WEOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK(14)

(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

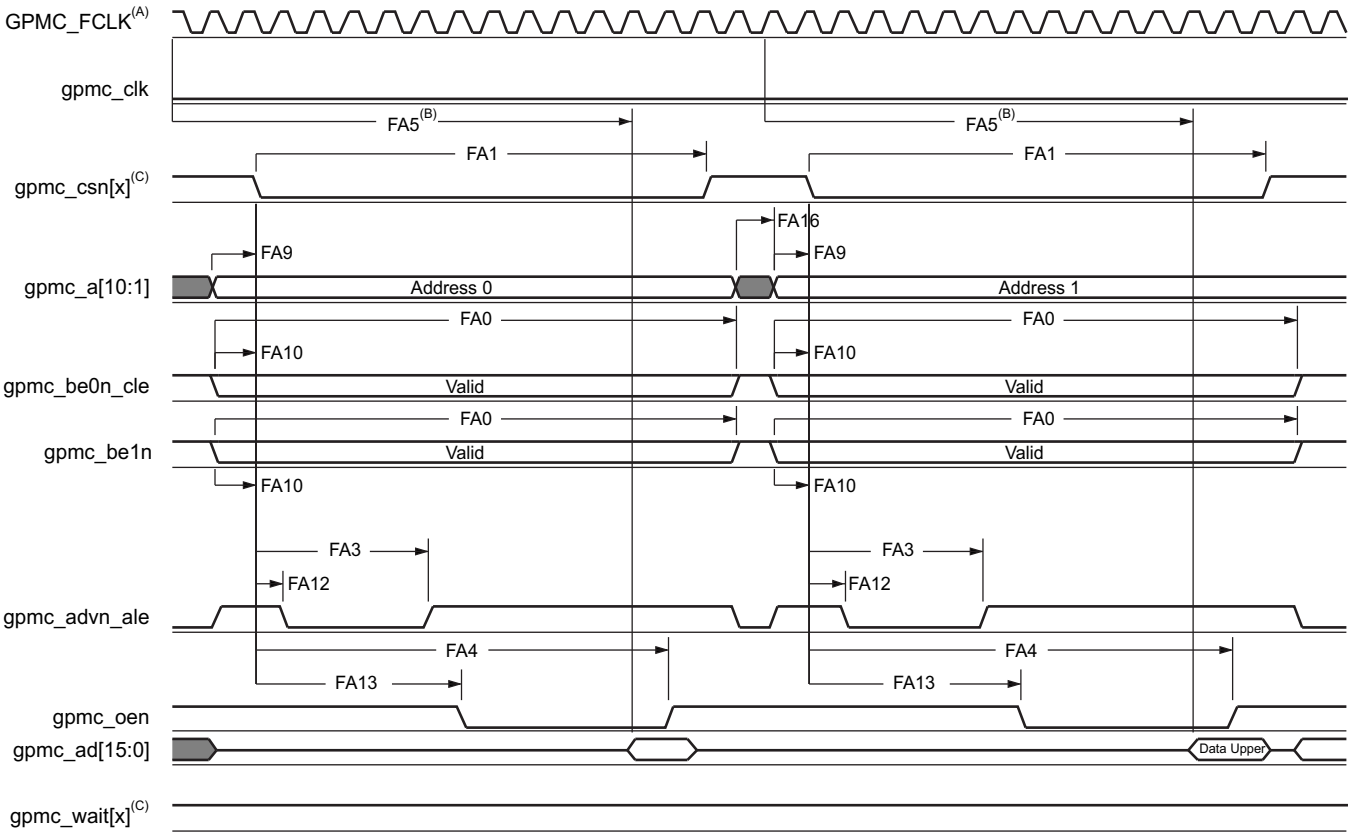



A. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-38. GPMC and NOR Flash—Asynchronous Read—Single Word**

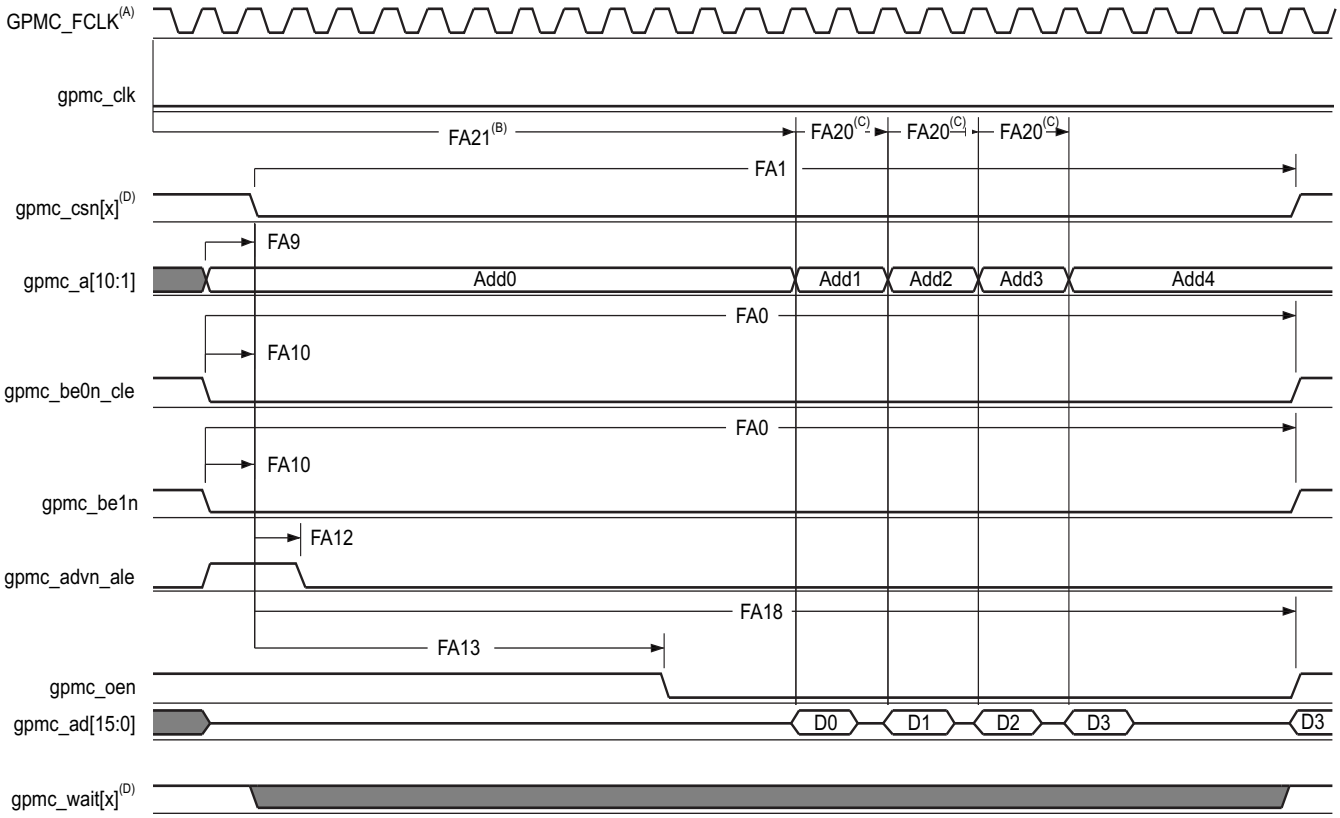



A. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-39. GPMC and NOR Flash—Asynchronous Read—32-Bit**



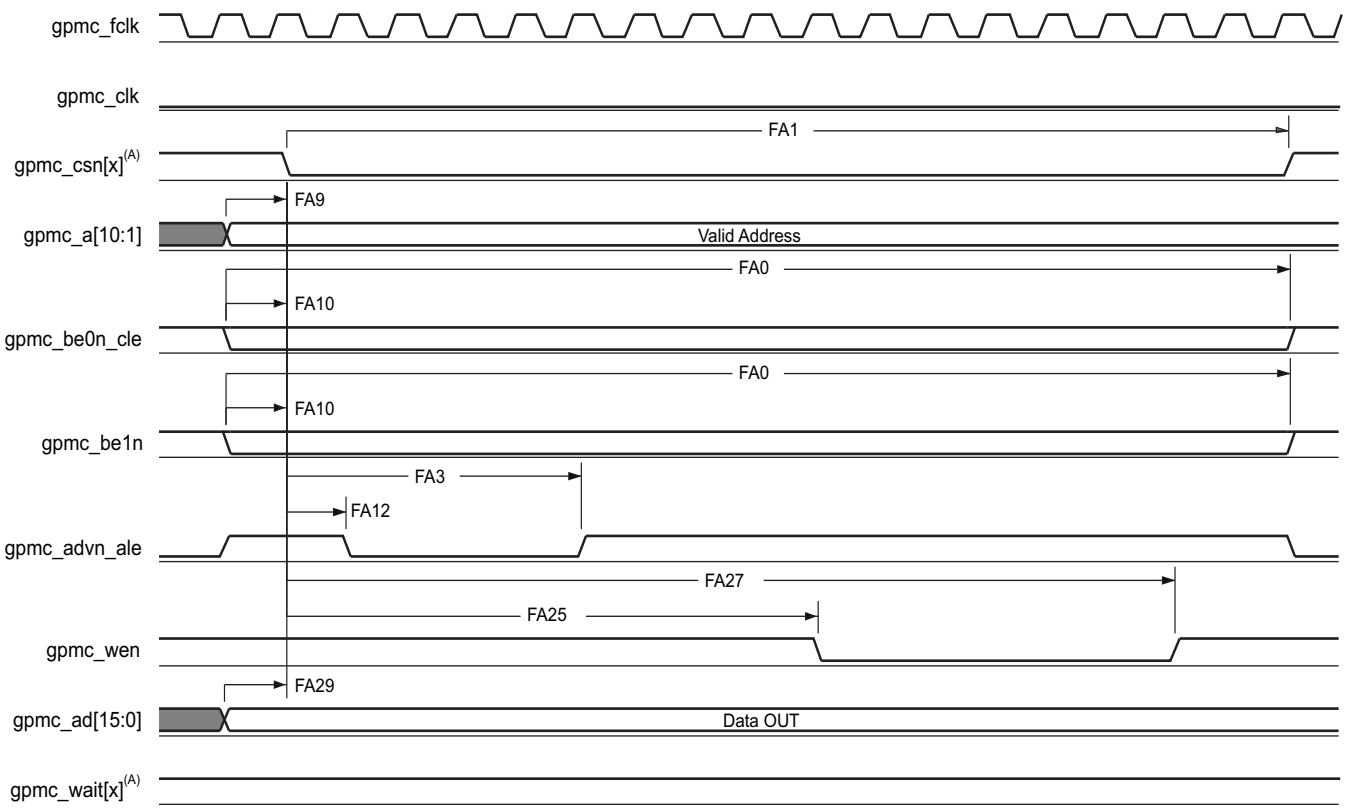

A. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

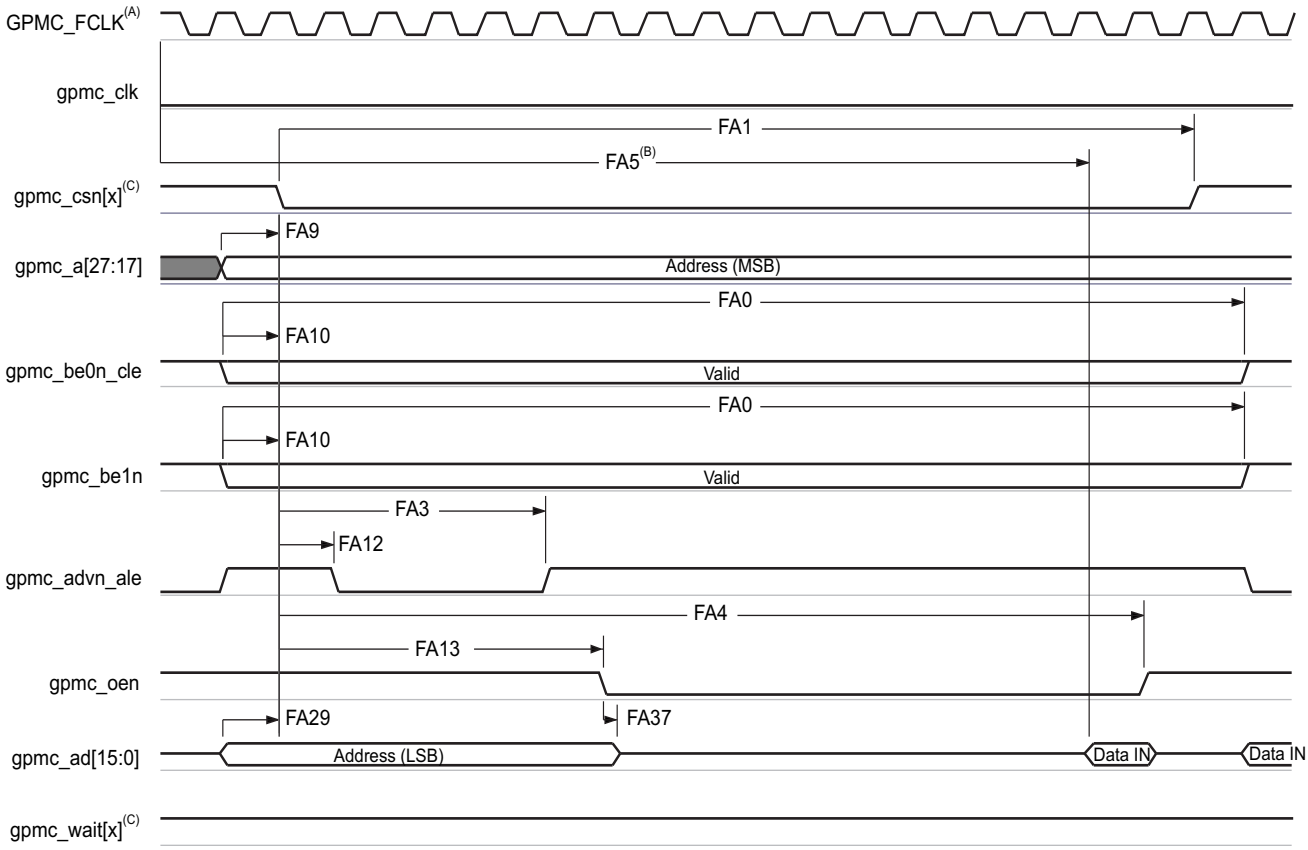
D. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-40. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-Bit**




A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-41. GPMC and NOR Flash—Asynchronous Write—Single Word**

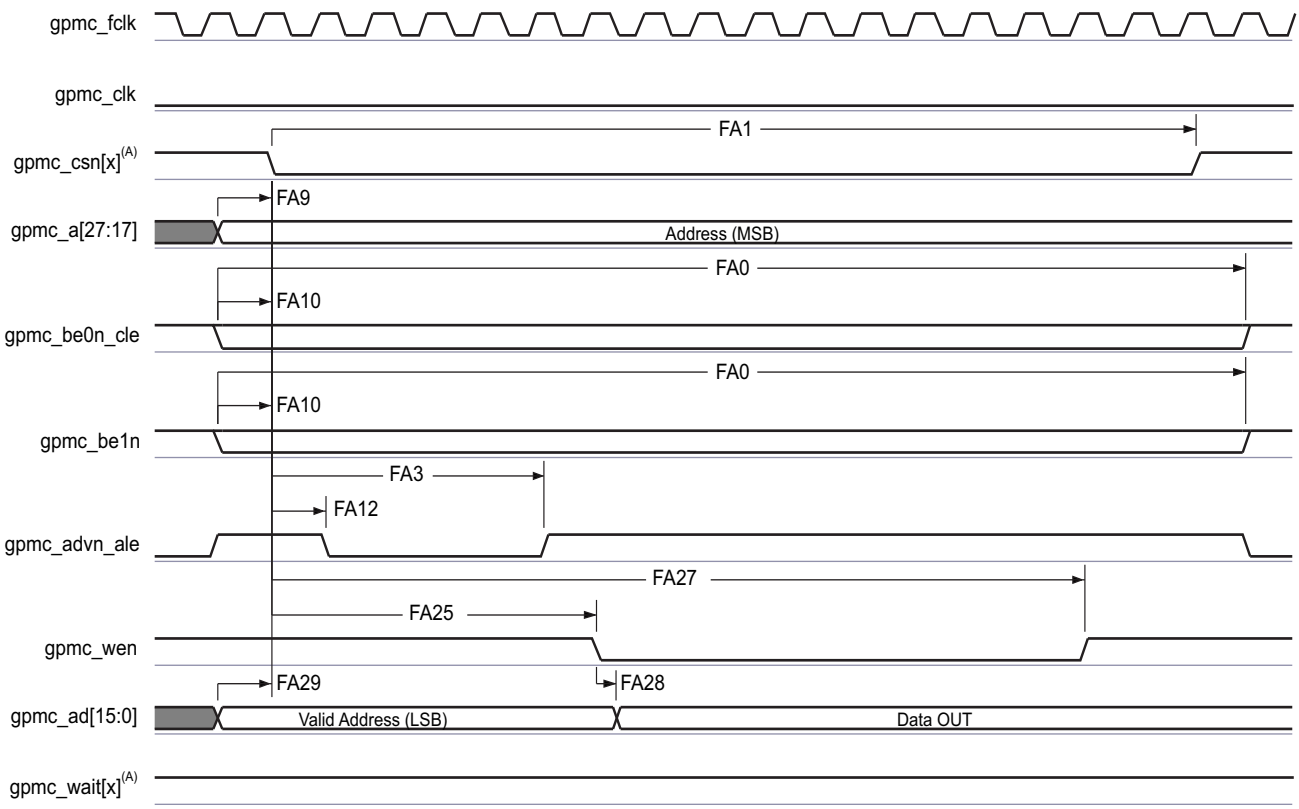



A. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-42. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word**




A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-43. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word**

#### 5.12.8.1.3 GPMC and NAND Flash—Asynchronous Mode

表 5-45 and 表 5-46 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-44 through 図 5-47).

**表 5-44. GPMC and NAND Flash Timing Conditions—Asynchronous Mode**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_R$ | Input signal rise time | 0.3 | | 1.8 | ns |
| $t_F$ | Input signal fall time | 0.3 | | 1.8 | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | 3 | | 30 | pF |

**表 5-45. GPMC and NAND Flash Internal Timing Parameters—Asynchronous Mode[1][2]**

| NO. | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| GNFI1 | Delay time, output data gpmc_ad[15:0] generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI2 | Delay time, input data gpmc_ad[15:0] capture from internal functional clock GPMC_FCLK[3] | | 4.0 | | 4.0 | ns |
| GNFI3 | Delay time, output chip select gpmc_csn[x] generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI4 | Delay time, output address valid and address latch enable gpmc_advn_ale generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI5 | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI6 | Delay time, output enable gpmc_oen generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI7 | Delay time, output write enable gpmc_wen generation from internal functional clock GPMC_FCLK[3] | | 6.5 | | 6.5 | ns |
| GNFI8 | Skew, functional clock GPMC_FCLK[3] | | 100 | | 100 | ps |

(1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

(3) GPMC_FCLK is general-purpose memory controller internal functional clock.

**表 5-46. GPMC and NAND Flash Timing Requirements—Asynchronous Mode**

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| GNF12[1] | $t_{acc(d)}$ | Access time, input data gpmc_ad[15:0] | | J[2] | | J[2] | ns |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]

(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

### 表 5-47. GPMC and NAND Flash Switching Characteristics—Asynchronous Mode

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| GNF0 | $t_{w(wenV)}$ | Pulse duration, output write enable gpmc_wen valid | A(1) | | A(1) | | ns |
| GNF1 | $t_{d(csnV-wenV)}$ | Delay time, output chip select gpmc_csn[x](2) valid to output write enable gpmc_wen valid | B(3) - 0.2 | B(3) + 2.0 | B(3) - 0.2 | B(3) + 2.0 | ns |
| GNF2 | $t_{w(cleH-wenV)}$ | Delay time, output lower-byte enable and command latch enable gpmc_be0n_cle high to output write enable gpmc_wen valid | C(4) - 0.2 | C(4) + 2.0 | C(4) - 0.2 | C(4) + 2.0 | ns |
| GNF3 | $t_{w(wenV-dV)}$ | Delay time, output data gpmc_ad[15:0] valid to output write enable gpmc_wen valid | D(5) - 0.2 | D(5) + 2.8 | D(5) - 0.2 | D(5) + 2.0 | ns |
| GNF4 | $t_{w(wenIV-dIV)}$ | Delay time, output write enable gpmc_wen invalid to output data gpmc_ad[15:0] invalid | E(6) - 0.2 | E(6) + 2.8 | E(6) - 0.2 | E(6) + 2.0 | ns |
| GNF5 | $t_{w(wenIV-cleIV)}$ | Delay time, output write enable gpmc_wen invalid to output lower-byte enable and command latch enable gpmc_be0n_cle invalid | F(7) - 0.2 | F(7) + 2.0 | F(7) - 0.2 | F(7) + 2.0 | ns |
| GNF6 | $t_{w(wenIV-csnIV)}$ | Delay time, output write enable gpmc_wen invalid to output chip select gpmc_csn[x](2) invalid | G(8) - 0.2 | G(8) + 2.0 | G(8) - 0.2 | G(8) + 2.0 | ns |
| GNF7 | $t_{w(aleH-wenV)}$ | Delay time, output address valid and address latch enable gpmc_advn_ale high to output write enable gpmc_wen valid | C(4) - 0.2 | C(4) + 2.0 | C(4) - 0.2 | C(4) + 2.0 | ns |
| GNF8 | $t_{w(wenIV-aleIV)}$ | Delay time, output write enable gpmc_wen invalid to output address valid and address latch enable gpmc_advn_ale invalid | F(7) - 0.2 | F(7) + 2.0 | F(7) - 0.2 | F(7) + 2.0 | ns |
| GNF9 | $t_{c(wen)}$ | Cycle time, write | | H(9) | | H(9) | ns |
| GNF10 | $t_{d(csnV-oenV)}$ | Delay time, output chip select gpmc_csn[x](2) valid to output enable gpmc_oen valid | I(10) - 0.2 | I(10) + 2.0 | I(10) - 0.2 | I(10) + 2.0 | ns |
| GNF13 | $t_{w(oenV)}$ | Pulse duration, output enable gpmc_oen valid | | K(11) | | K(11) | ns |
| GNF14 | $t_{c(oen)}$ | Cycle time, read | L(12) | | L(12) | | ns |
| GNF15 | $t_{w(oenIV-csnIV)}$ | Delay time, output enable gpmc_oen invalid to output chip select gpmc_csn[x](2) invalid | M(13) - 0.2 | M(13) + 2.0 | M(13) - 0.2 | M(13) + 2.0 | ns |

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(2) In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.

(3) B = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(4) C = ((WEOnTime - ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - ADVExtraDelay)) × GPMC_FCLK(14)

(5) D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK(14)

(6) E = ((WrCycleTime - WEOffTime) × (TimeParaGranularity + 1) - 0.5 × WEExtraDelay) × GPMC_FCLK(14)

(7) F = ((ADVWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - WEExtraDelay)) × GPMC_FCLK(14)

(8) G = ((CSWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - WEExtraDelay)) × GPMC_FCLK(14)

(9) H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK(14)

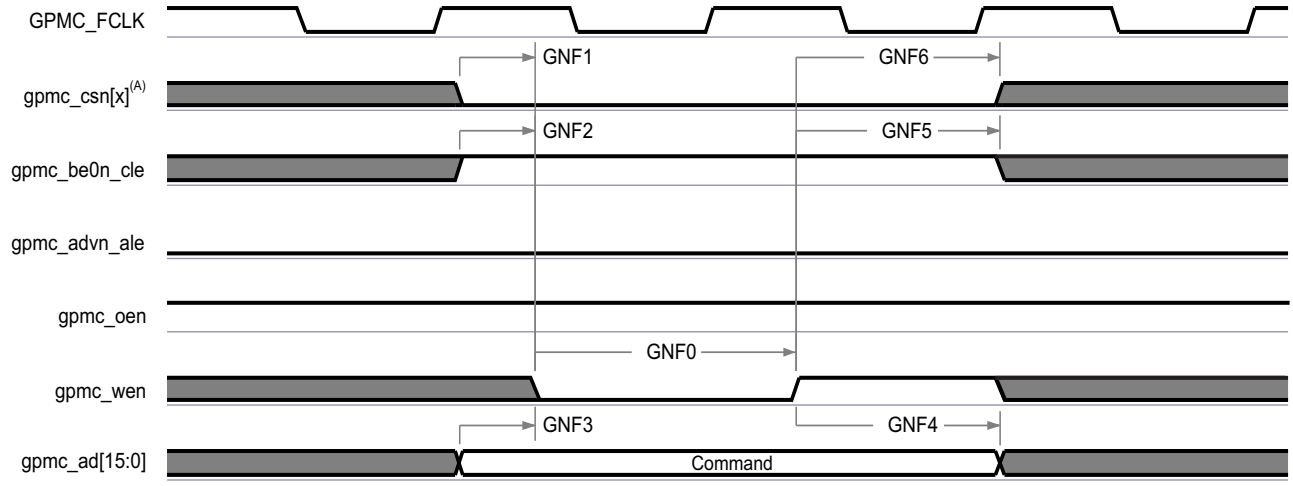
(10) I = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(11) K = (OEOffTime - OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK(14)

(12) L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK(14)

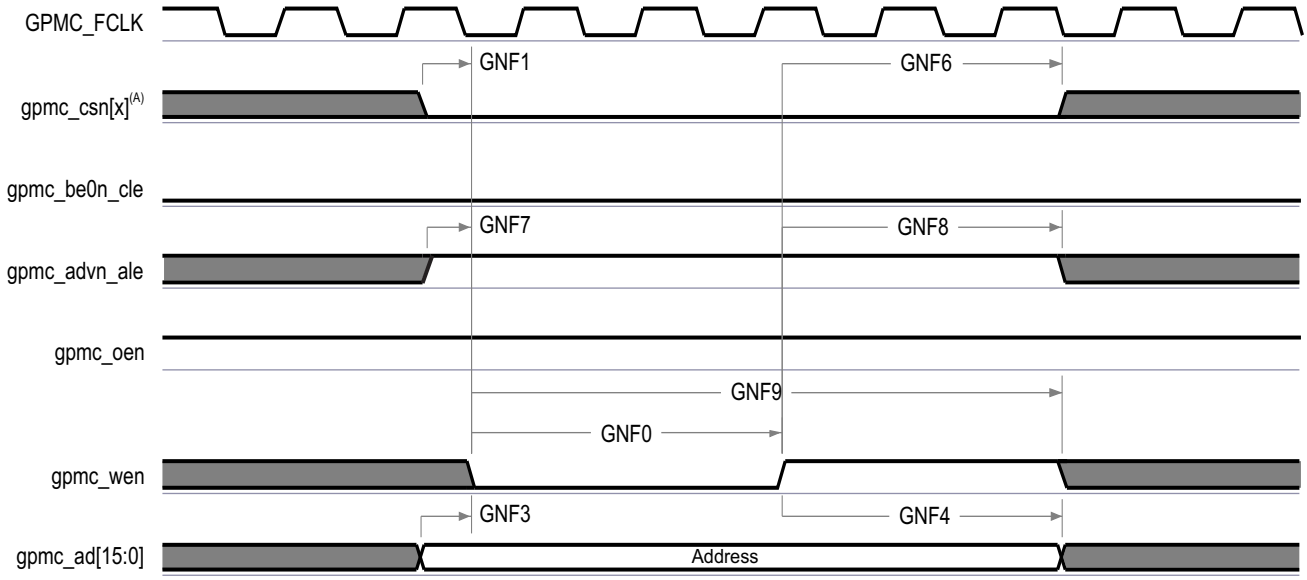
(13) M = ((CSRdOffTime - OEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - OEExtraDelay)) × GPMC_FCLK(14)

(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.



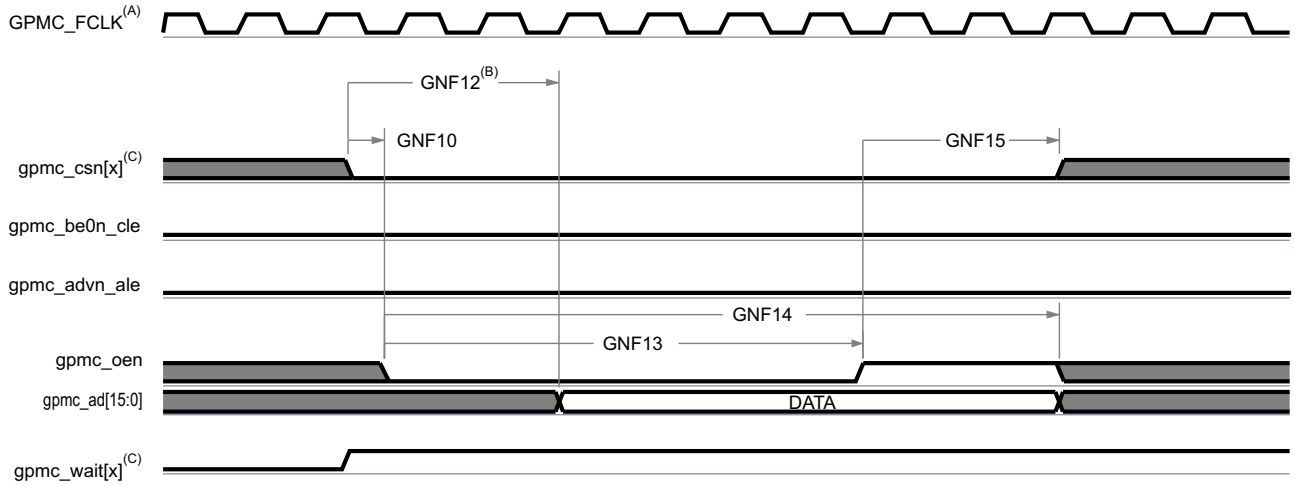

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.

**図 5-44. GPMC and NAND Flash—Command Latch Cycle**



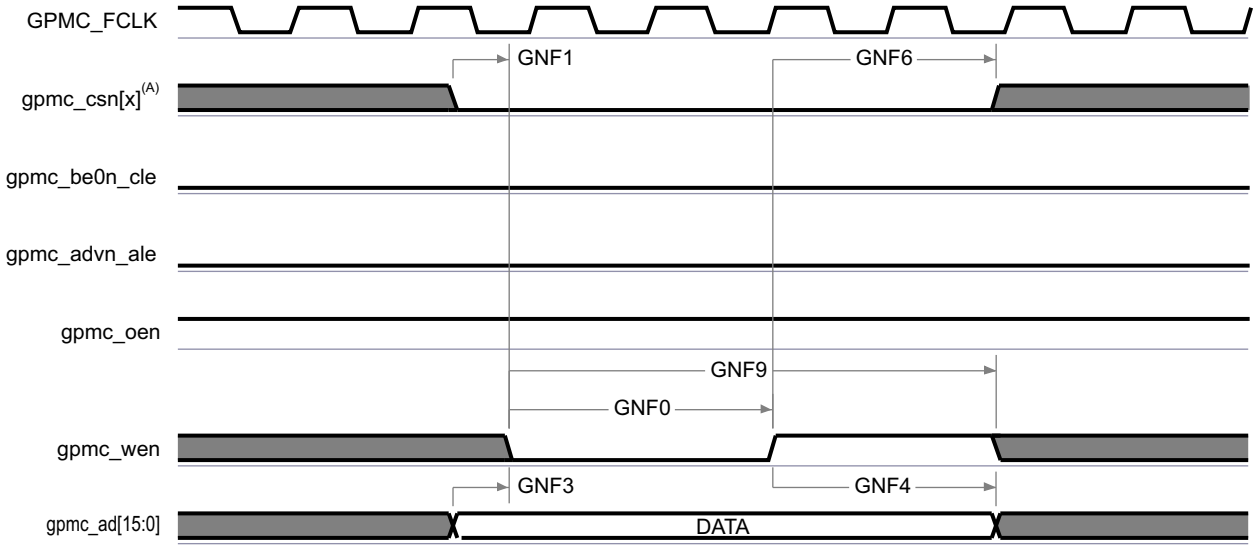

A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.

**図 5-45. GPMC and NAND Flash—Address Latch Cycle**




A. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
B. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
C. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6. In gpmc_wait[x], x is equal to 0 or 1.

**図 5-46. GPMC and NAND Flash—Data Read Cycle**




A. In gpmc_csn[x], x is equal to 0, 1, 2, 3, 4, 5, or 6.

**図 5-47. GPMC and NAND Flash—Data Write Cycle**

#### 5.12.8.2 Memory Interface

The device has a dedicated interface to LPDDR2, DDR3, and DDR3L SDRAM. It supports JEDEC standard compliant LPDDR2, DDR3, and DDR3L SDRAM devices with a 16- or 32-bit data path to external SDRAM memory.

For more details on the LPDDR2, DDR3, and DDR3L memory interface, see the EMIF section of the *AM437x Sitara Processors Technical Reference Manual*.

##### *5.12.8.2.1 DDR3 and DDR3L Routing Guidelines*

This section provides the timing specification for the DDR3 and DDR3L interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR3 or DDR3L memory system without the need for a complex timing closure process. For more information regarding the guidelines, see *Understanding TI's PCB Routing Rule-Based DDR Timing Specification*. This application report provides generic guidelines and approach. All the specifications provided in the data manual take precedence over the generic guidelines and must be adhered to for a reliable DDR3 or DDR3L interface operation.

注

All references to DDR3 in this section apply to DDR3 and DDR3L devices, unless otherwise noted.

###### *5.12.8.2.1.1 Board Designs*

TI only supports board designs using DDR3 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3 memory interface are shown in 表 5-48 and 図 5-48.

**表 5-48. Switching Characteristics for DDR3 Memory Interface**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(DDR\_CK)}$<br>$t_{c(DDR\_CKn)}$ | Cycle time, DDR_CK and DDR_CKn | 2.5 | 3.3(1) | ns |

(1) The JEDEC JESD79-3F Standard defines the maximum clock period of 3.3 ns for all standard-speed bin DDR3 and DDR3L memory devices. Therefore, all standard-speed bin DDR3 and DDR3L memory devices are required to operate at 303 MHz.

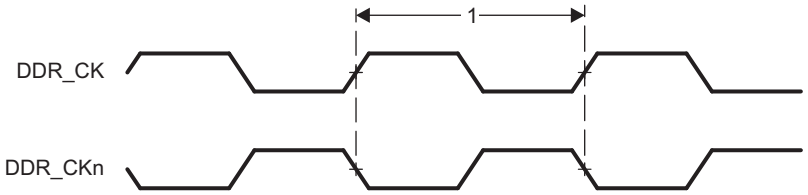



**図 5-48. DDR3 Memory Interface Clock Timing**

#### 5.12.8.2.1.2 DDR3 Device Combinations

Because there are several possible combinations of device counts and single-side or dual-side mounting, 表 5-49 summarizes the supported device configurations.

**表 5-49. Supported DDR3 Device Combinations**

| NUMBER OF DDR3 DEVICES | DDR3 DEVICE WIDTH (BITS) | MIRRORED? | DDR3 EMIF WIDTH (BITS) |
|---|---|---|---|
| 1 | 16 | N | 16 |
| 2 | 8 | Y(1) | 16 |
| 2 | 16 | Y(1) | 32 |
| 4 | 8 | Y(1) | 32 |

(1) DDR3 devices are mirrored when half of the devices are placed on the top of the board and the other half are placed on the bottom of the board.

#### 5.12.8.2.1.3 DDR3 Interface

##### 5.12.8.2.1.3.1 DDR3 Interface Schematic

The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used.

図 5-49 shows the schematic connections for 16-bit interface using one x16 DDR3 device. 図 5-50 shows the schematic connections for 16-bit interface without using $V_{TT}$ termination for the ADDR_CTRL net class signals. 図 5-51 shows the schematic connections for 16-bit interface using two x8 DDR3 devices.

図 5-52 shows the schematic connections for 32-bit interface using two x16 DDR3 device and 図 5-53 shows the schematic connections for 32-bit interface using four x8 DDR3 devices.

When not using all or part of a DDR3 interface, the proper method of handling the unused pins is to tie off the DDR_DQS[x] pins to the VDDS_DDR supply via a 1-kΩ resistor and pulling the DDR_DQSn[x] pins to ground via a 1k-Ω resistor. This must be done for each byte not used. Although these signals have internal pullup and pulldown, external pullup and pulldown provide additional protection against external electrical noise causing activity on the signals. Also, include the 49.9-Ω pulldown for DDR_VTP. The VDDS_DDR and DDR_VREF power supply terminals need to be connected to their respective power supplies even if the DDR3 interface is not being used. All other DDR3 interface pins can be left unconnected. The supported modes for use of the DDR3 EMIF are 32 bits wide, 16 bits wide, or not used.

The device can only source one load connected to the DQS[x] and DQ[x] net class signals and up to four loads connected to the CK and ADDR_CTRL net class signals. For more information related to net classes, see 5.12.8.2.1.3.9.

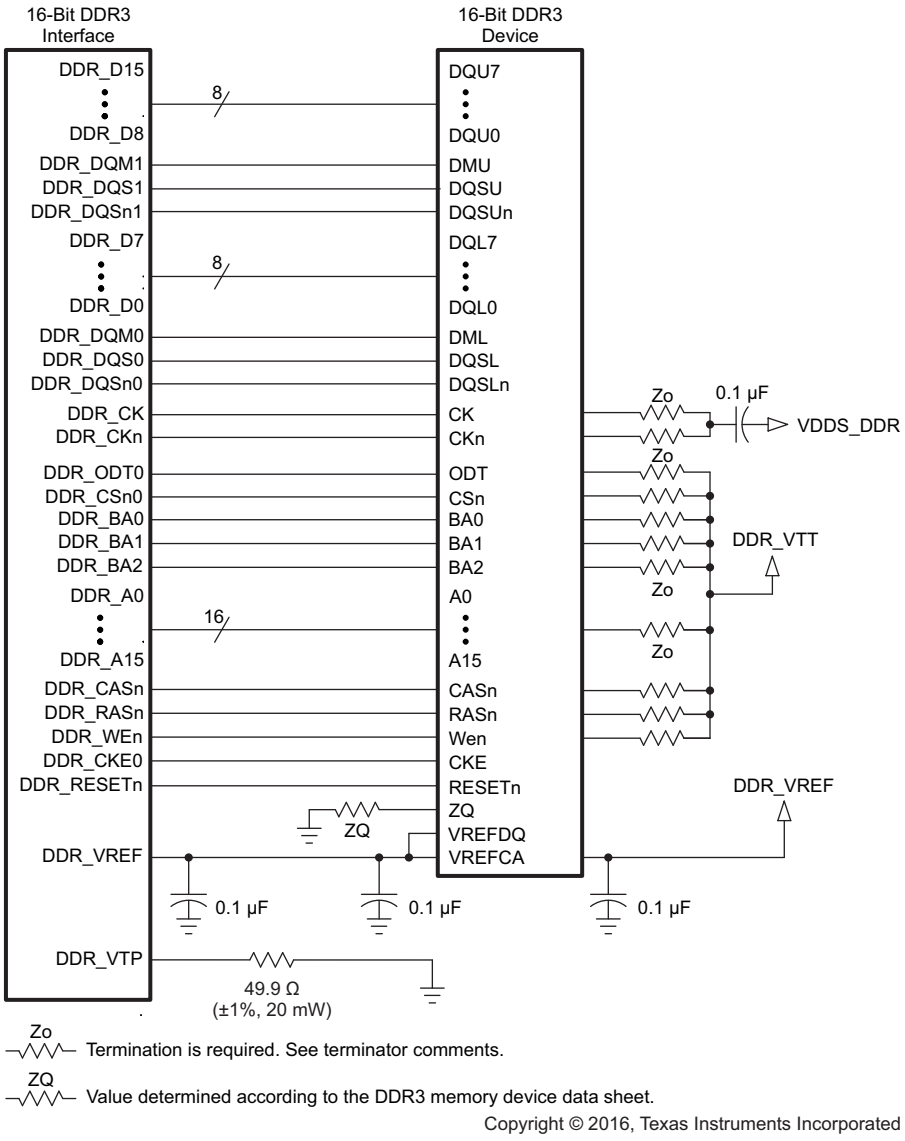
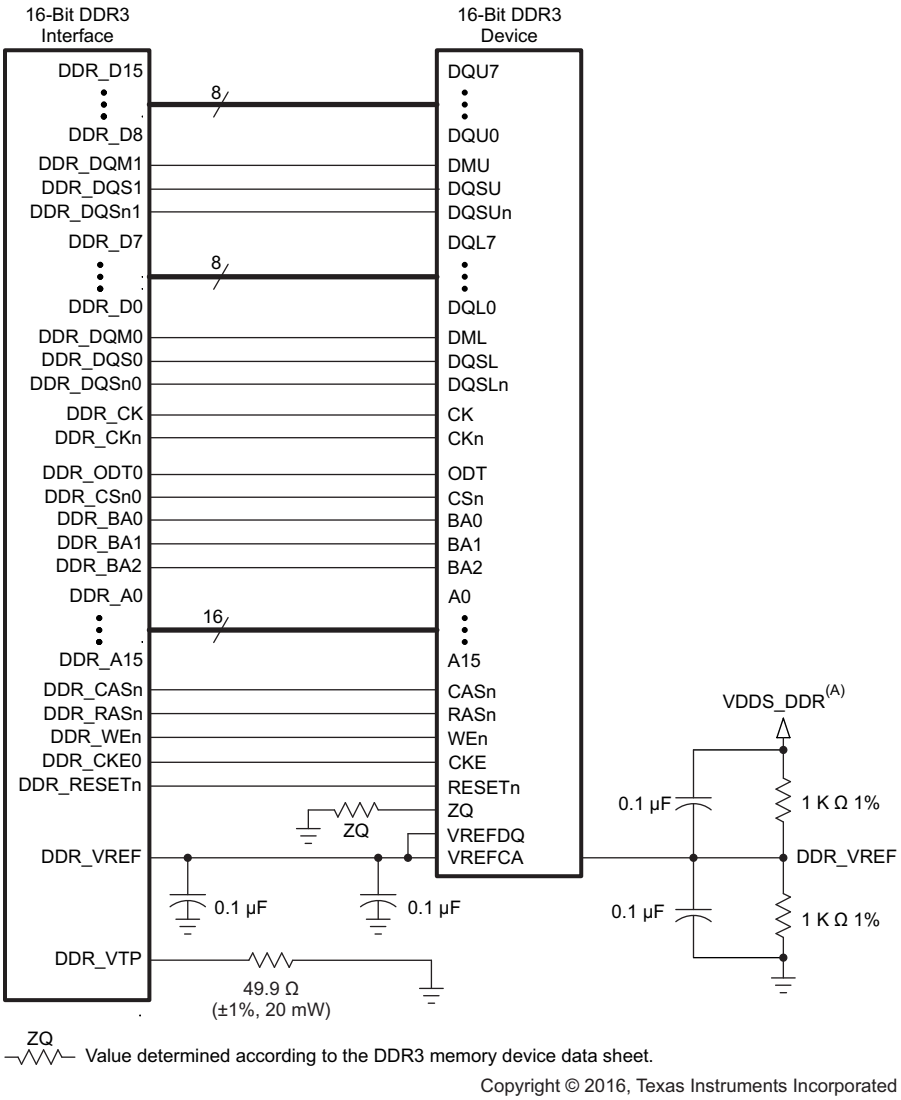




**図 5-49. 16-Bit DDR3 Interface Using One 16-Bit DDR3 Device With $V_{TT}$ Termination**






A. VDDS_DDR is the power supply for the DDR3 memories and the DDR3 interface.

**図 5-50. 16-Bit DDR3 Interface Using One 16-Bit DDR3 Device Without $V_{TT}$ Termination**

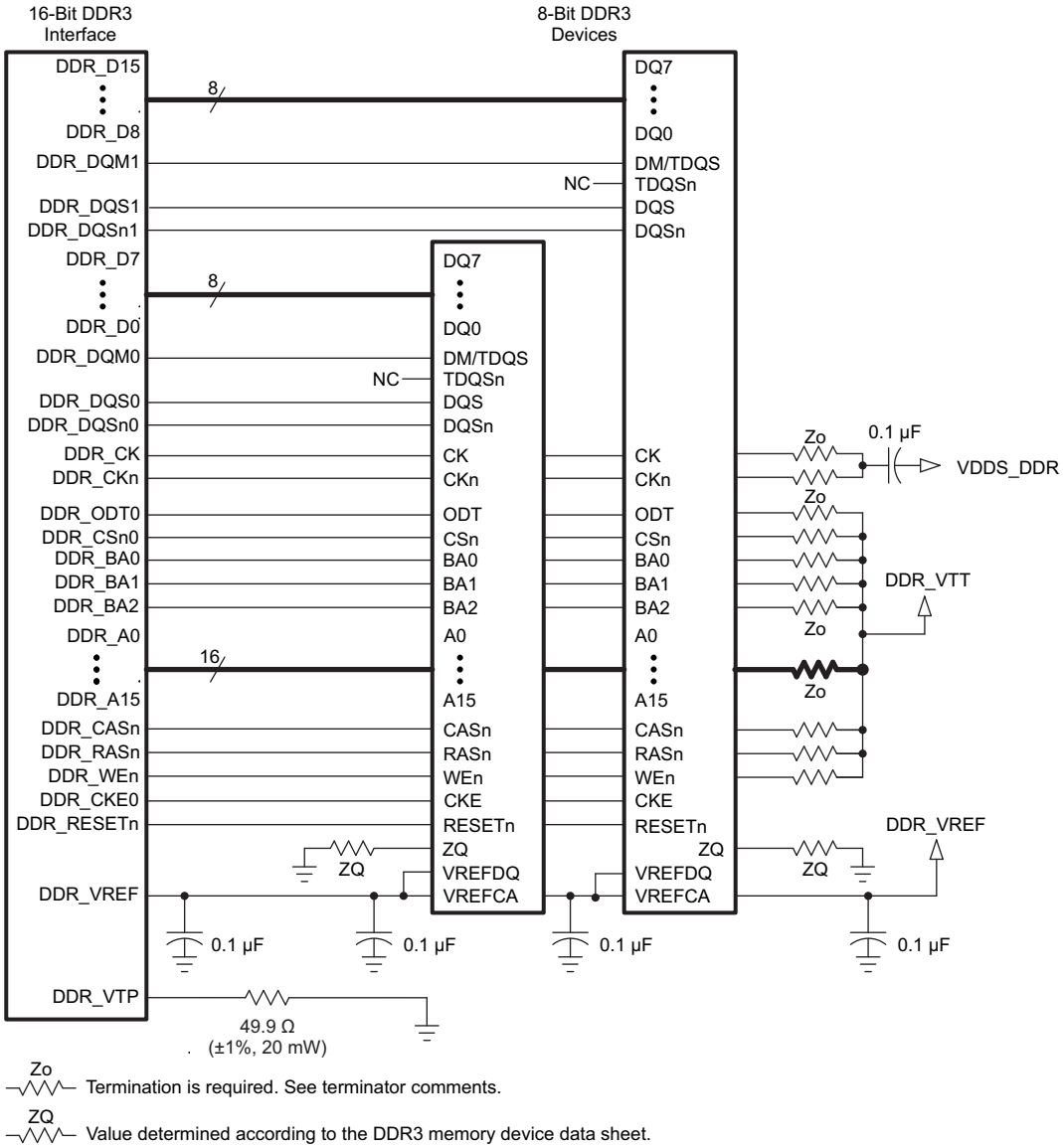



**図 5-51. 16-Bit DDR3 Interface Using Two 8-Bit DDR3 Devices With $V_{TT}$ Termination**

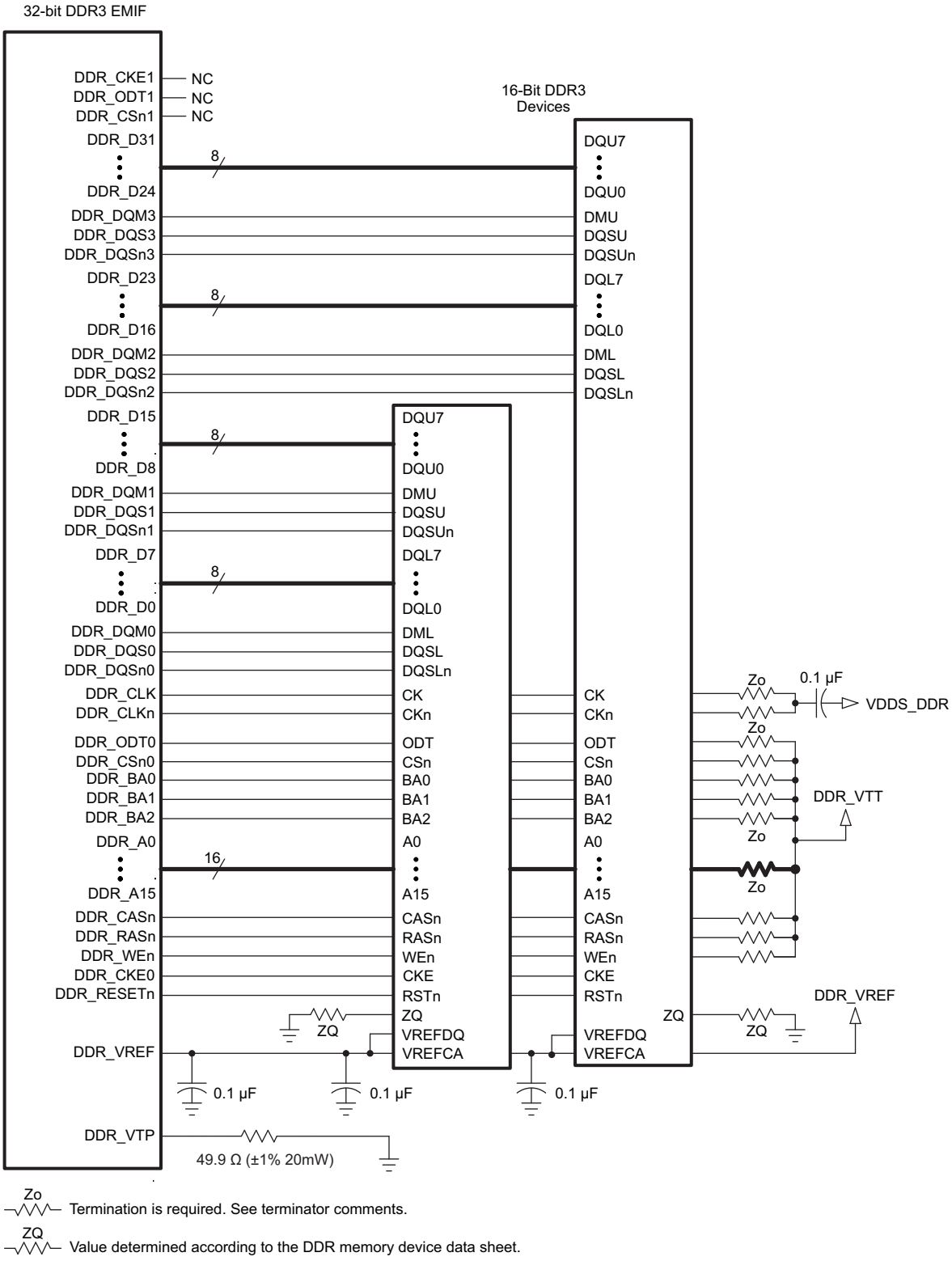



**図 5-52. 32-Bit DDR3 Interface Using Two 16-Bit DDR3 Devices With $V_{TT}$ Termination**

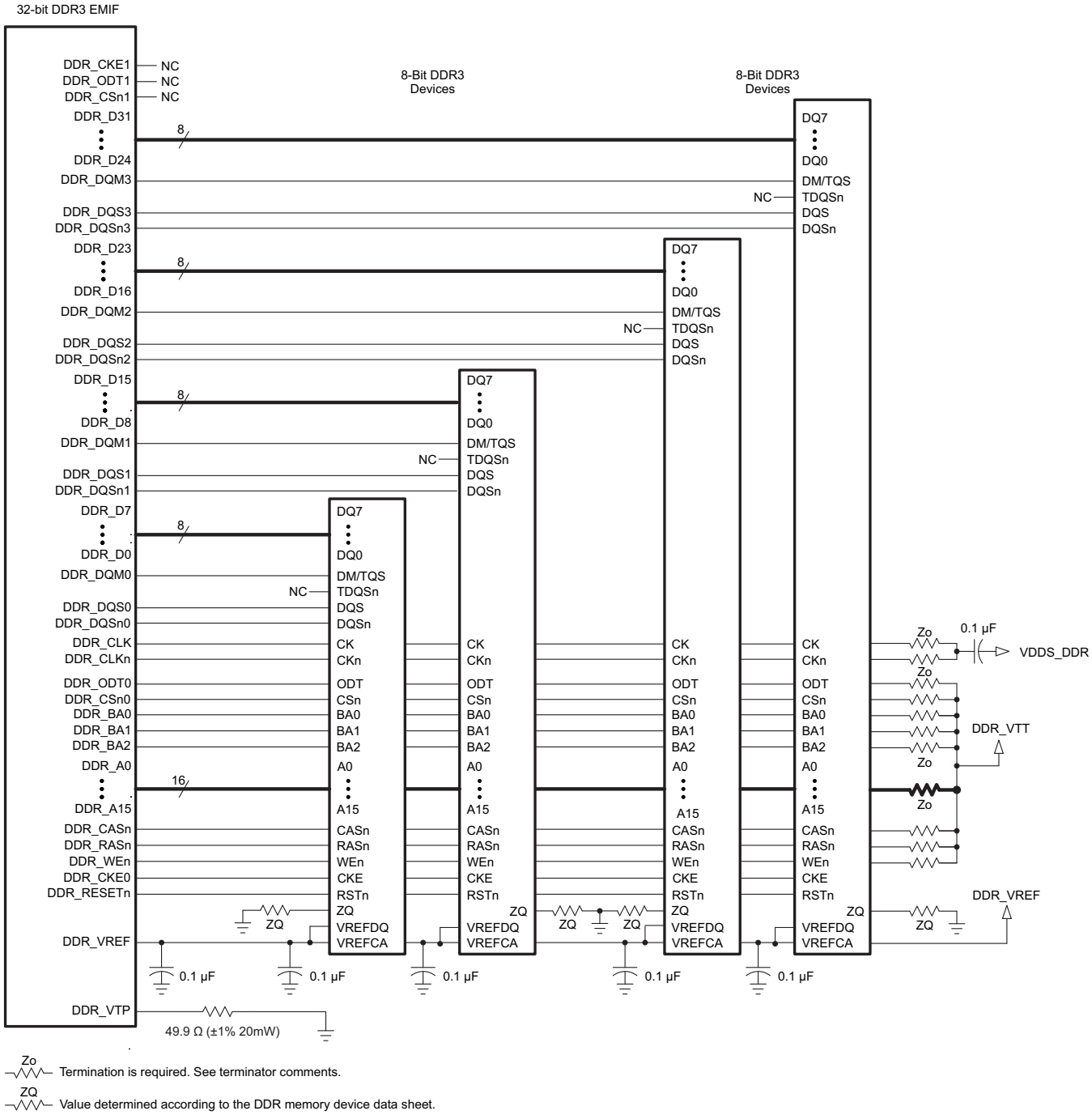



**図 5-53. 32-Bit DDR3 Interface Using Four 8-Bit DDR3 Devices With $V_{TT}$ Termination**

#### 5.12.8.2.1.3.2 Compatible JEDEC DDR3 Devices

表 5-50 shows the parameters of the JEDEC DDR3 devices that are compatible with this interface.

**表 5-50. Compatible JEDEC DDR3 Devices (Per Interface)**

| NO. | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | JEDEC DDR3 device speed grade | $t_{C(DDR\_CK)}$ and $t_{C(DDR\_CKn)}$ = 2.5ns | DDR3-1600 | | |
| 2 | JEDEC DDR3 device bit width | | x8 | x32 | |
| 3 | JEDEC DDR3 device count(1) | | 1 | 4 | Devices |

(1) For valid DDR3 device configurations and device counts, see 5.12.8.2.1.3.1, 図 5-49, and 図 5-51.

#### 5.12.8.2.1.3.3 DDR3 PCB Stackup

The minimum stackup for routing the DDR3 interface is a four-layer stack up as shown in 表 5-51. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance signal integrity and electromagnetic interference performance, or to reduce the size of the PCB footprint.

**表 5-51. Minimum PCB Stackup(1)**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top signal routing |
| 2 | Plane | Ground |
| 3 | Plane | Split Power Plane |
| 4 | Signal | Bottom signal routing |

(1) All signals that have critical signal integrity requirements should be routed first on layer 1. It may not be possible to route all of these signals on layer 1 which requires some to be routed on layer 4. When this is done, the signal routes on layer 4 should not cross splits in the power plane.

**表 5-52. PCB Stackup Specifications(1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing and plane layers | 4 | | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground reference layers under DDR3 routing region(2) | 1 | | | |
| 4 | Full VDDS_DDR power reference layers under the DDR3 routing region(2) | 1 | | | |
| 5 | Number of reference plane cuts allowed within DDR3 routing region(3) | | | 0 | |
| 6 | Number of layers between DDR3 routing layer and reference plane(4) | | | 0 | |
| 7 | PCB routing feature size | | 4 | | mils |
| 8 | PCB trace width, w | | 4 | | mils |
| 9 | PCB BGA escape via pad size(5) | | 18 | 20 | mils |
| 10 | PCB BGA escape via hole size | | 10 | | mils |
| 13 | Single-ended impedance, Zo(6) | | 50 | 75 | Ω |
| 14 | Impedance control(7)(8) | Zo-5 | Zo | Zo+5 | Ω |

(1) For the DDR3 device BGA pad size, see the DDR3 device manufacturer documentation.

(2) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.

(3) No traces should cross reference plane cuts within the DDR3 routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(4) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(5) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(6) Zo is the nominal singled-ended impedance selected for the PCB.

(7) This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Zo defined by the single-ended impedance parameter.

(8) Tighter impedance control is required to ensure flight time skew is minimal.

#### 5.12.8.2.1.3.4 DDR3 Placement

図 5-54 shows the required placement for the device as well as the DDR3 devices. The dimensions for this figure are defined in 表 5-53. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.

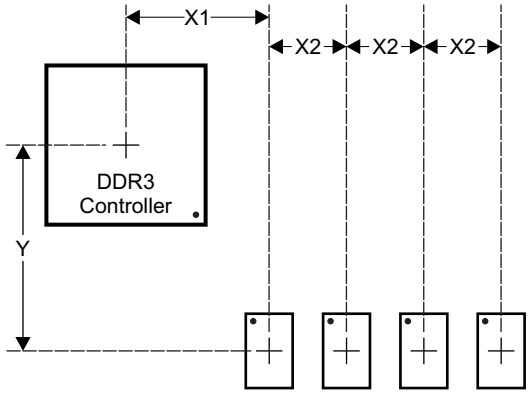



**図 5-54. Placement Specifications**

**表 5-53. Placement Specifications(1)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X1(2)(3)(4) | | 1000 | mils |
| 2 | X2(2)(3) | | 600 | mils |
| 3 | Y Offset(2)(3)(4) | | 1500 | mils |
| 4 | Clearance from non-DDR3 signal to DDR3 keepout region(5)(6) | 4 | | w |

(1) DDR3 keepout region to encompass entire DDR3 routing area.

(2) For dimension definitions, see 図 5-54.

(3) Measurements from center of device to center of DDR3 device.

(4) Minimizing X1 and Y improves timing margins.

(5) w is defined as the signal trace width.

(6) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

#### 5.12.8.2.1.3.5 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in 図 5-55. This region should encompass all DDR3 circuitry and the region size varies with component placement and DDR3 routing. Additional clearances required for the keepout region are shown in 表 5-53. Non-DDR3 signals should not be routed on the same signal layer as DDR3 signals within the DDR3 keepout region. Non-DDR3 signals may be routed in the region provided they are routed on layers separated from DDR3 signal layers by a ground layer. No breaks should be allowed in the reference ground or VDDS_DDR power plane in this region. In addition, the VDDS_DDR power plane should cover the entire keepout region.

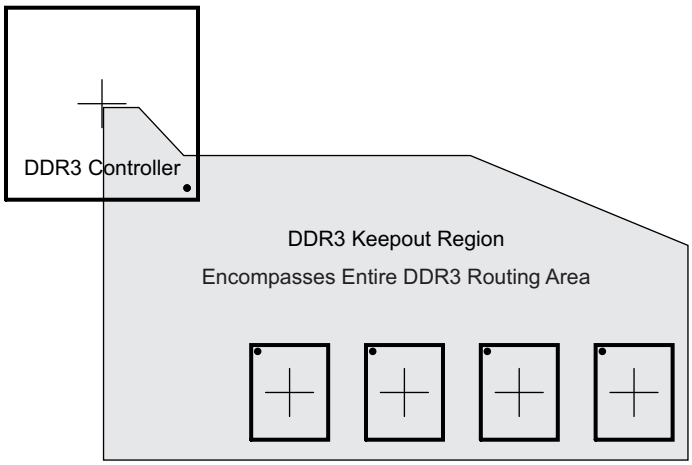



**図 5-55. DDR3 Keepout Region**

#### 5.12.8.2.1.3.6 DDR3 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. 表 5-54 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 interface and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

**表 5-54. Bulk Bypass Capacitors(1)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | VDDS_DDR bulk bypass capacitor count | 2 | | Devices |
| 2 | VDDS_DDR bulk bypass total capacitance | 20 | | µF |
| 3 | DDR3#1 bulk bypass capacitor count | 2 | | Devices |
| 4 | DDR3#1 bulk bypass total capacitance | 20 | | µF |
| 5 | DDR3#2 bulk bypass capacitor count(2) | 2 | | Devices |
| 6 | DDR3#2 bulk bypass total capacitance(2) | 20 | | µF |
| 7 | DDR3#3 bulk bypass capacitor count(3) | 2 | | Devices |
| 8 | DDR3#3 bulk bypass total capacitance(3) | 20 | | µF |
| 9 | DDR3#4bulk bypass capacitor count(3) | 2 | | Devices |
| 10 | DDR3#4 bulk bypass total capacitance(3) | 20 | | µF |

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

(2) Only used when two DDR3 devices are used.

(3) Only used when four DDR3 devices are used.

#### 5.12.8.2.1.3.7 DDR3 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, device DDR3 power, and device DDR3 ground connections. 表 5-55 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible.
2. Minimize the distance from the bypass cap to the power terminals being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limites on via sharing shown in 表 5-55.

**表 5-55. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | HS bypass capacitor package size(1) | | 0201 | 0402 | 10 mils |
| 2 | Distance, HS bypass capacitor to VDDS_DDR and VSS terminal being bypassed(2)(3)(4) | | | 400 | mils |
| 3 | VDDS_DDR HS bypass capacitor count | 20 | | | Devices |
| 4 | VDDS_DDR HS bypass capacitor total capacitance | 1 | | | μF |
| 5 | Trace length from VDDS_DDR and VSS terminal to connection via(2) | | 35 | 70 | mils |
| 6 | Distance, HS bypass capacitor to DDR3 device being bypassed(5) | | | 150 | mils |
| 7 | DDR3 device HS bypass capacitor count(6) | 12 | | | Devices |
| 8 | DDR3 device HS bypass capacitor total capacitance(6) | 0.85 | | | μF |
| 9 | Number of connection vias for each HS bypass capacitor(7)(8) | 2 | | | Vias |
| 10 | Trace length from bypass capacitor connect to connection via(2)(8) | | 35 | 100 | mils |
| 11 | Number of connection vias for each DDR3 device power and ground terminal(9) | 1 | | | Vias |
| 12 | Trace length from DDR3 device power and ground terminal to connection via(2)(7) | | 35 | 60 | mils |

(1) LxW, 10-mil units; for example, a 0402 is a 40x20-mil surface-mount capacitor.

(2) Closer and shorter is better.

(3) Measured from the nearest VDDS_DDR and ground terminal to the center of the capacitor package.

(4) Three of these capacitors should be underneath the device, between the cluster of VDDS_DDR and ground terminals, between the DDR3 interfaces on the package.

(5) Measured from the DDR3 device power and ground terminal to the center of the capacitor package.

(6) Per DDR3 device.

(7) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.

(8) An HS bypass capacitor may share a via with a DDR3 device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR3 device pad should be less than 150 mils.

(9) Up to two pairs of DDR3 power and ground terminals may share a via.

#### 5.12.8.2.1.3.8 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Because these are returns for signal current, the signal via size may be used for these capacitors.

#### 5.12.8.2.1.3.9 DDR3 Net Classes

表 5-56 lists the clock net classes for the DDR3 interface. 表 5-57 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

**表 5-56. Clock Net Class Definitions**

| CLOCK NET CLASS | PIN NAMES |
|---|---|
| CK | DDR_CK and DDR_CKn |
| DQS0 | DDR_DQS0 and DDR_DQSn0 |
| DQS1 | DDR_DQS1 and DDR_DQSn1 |
| DQS2 | DDR_DQS2 and DDR_DQSn2 |
| DQS3 | DDR_DQS3 and DDR_DQSn3 |

**表 5-57. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[15:0], DDR_CSn0, DDR_CSn1, DDR_CASn, DDR_RASn, DDR_WEn, DDR_CKE0, DDR_CKE1, DDR_ODT0, DDR_ODT1 |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |
| DQ2 | DQS2 | DDR_D[23:16], DDR_DQM2 |
| DQ3 | DQS3 | DDR_D[31:24], DDR_DQM3 |

#### 5.12.8.2.1.3.10 DDR3 Signal Termination

Signal terminations are required for the CK and ADDR_CTRL net class signals. On-device terminations (ODTs) are required on the DQS[x] and DQ[x] net class signals. Detailed termination specifications are covered in the routing rules in the following sections.

図 5-50 provides an example DDR3 schematic with one 16-bit DDR3 memory device that does not have $V_{TT}$ termination on the address and control signals. A typical DDR3 point-to-point topology may provide acceptable signal integrity without $V_{TT}$ termination. System performance should be verified by performing signal integrity analysis using specific PCB design details before implementing this topology.

#### 5.12.8.2.1.3.11 DDR3 DDR_VREF Routing

DDR_VREF is used as a reference by the input buffers of the DDR3 memories as well as the device. DDR_VREF is intended to be half the DDR3 power supply voltage and is typically generated with a voltage divider connected to the VDDS_DDR power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of DDR_VREF is allowed to accommodate routing congestion.

#### 5.12.8.2.1.3.12 DDR3 VTT

Like DDR_VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike DDR_VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power subplane. VTT should be bypassed near the terminator resistors.

#### 5.12.8.2.1.4 DDR3 CK and ADDR_CTRL Topologies and Routing Definition

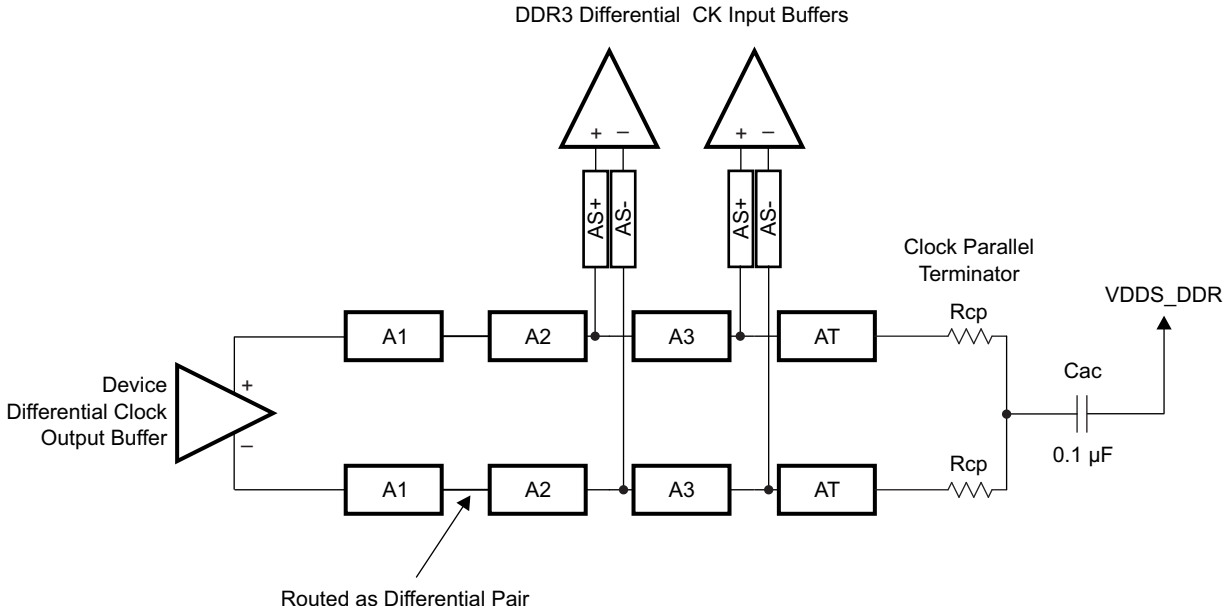
The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in 表 5-58.

##### 5.12.8.2.1.4.1 Using Two DDR3 Devices (x8 or x16)

Two DDR3 devices are supported on the DDR3 interface consisting of two x8 DDR3 devices arranged as one 16-bit bank or two x16 DDR3 devices arranged as one 32-bit bank. These two devices may be mounted on one side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

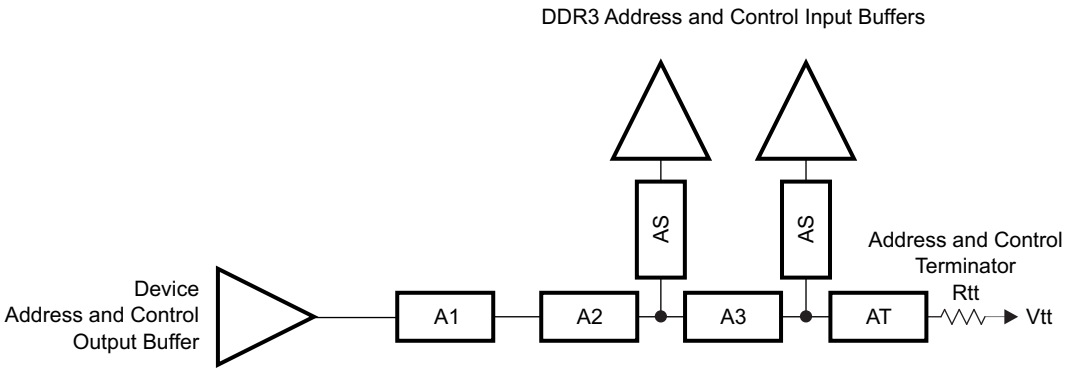
##### 5.12.8.2.1.4.2 CK and ADDR_CTRL Topologies, Two DDR3 Devices

図 5-56 shows the topology of the CK net classes and 図 5-57 shows the topology for the corresponding ADDR_CTRL net classes.




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-56. CK Topology for Two DDR3 Devices**

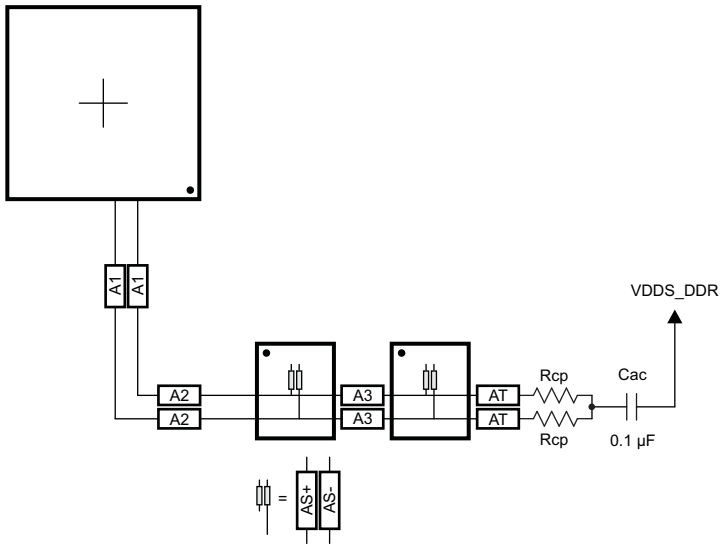



NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-57. ADDR_CTRL Topology for Two DDR3 Devices**

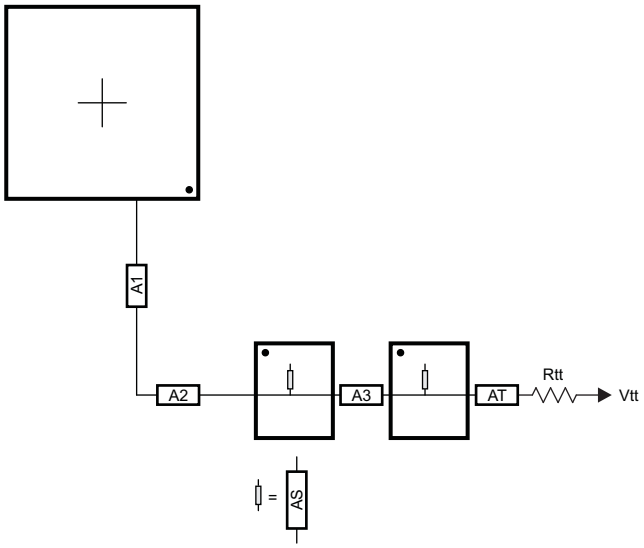
#### 5.12.8.2.1.4.3 CK and ADDR_CTRL Routing, Two DDR3 Devices

図 5-58 shows the CK routing for two DDR3 devices placed on the same side of the PCB. 図 5-59 shows the corresponding ADDR_CTRL routing.




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

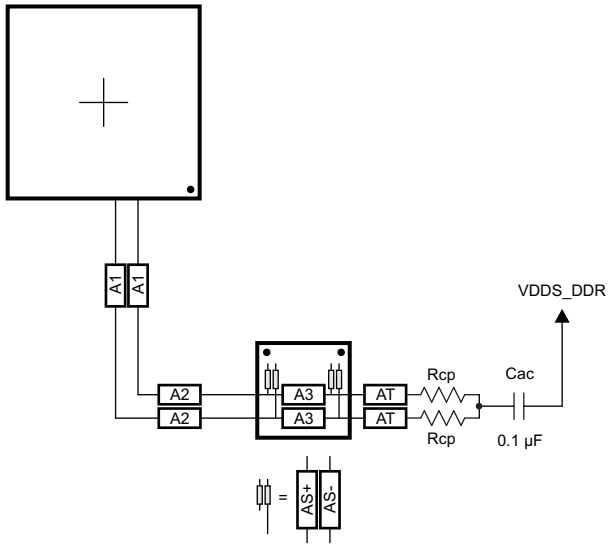
**図 5-58. CK Routing for Two Single-Side DDR3 Devices**




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

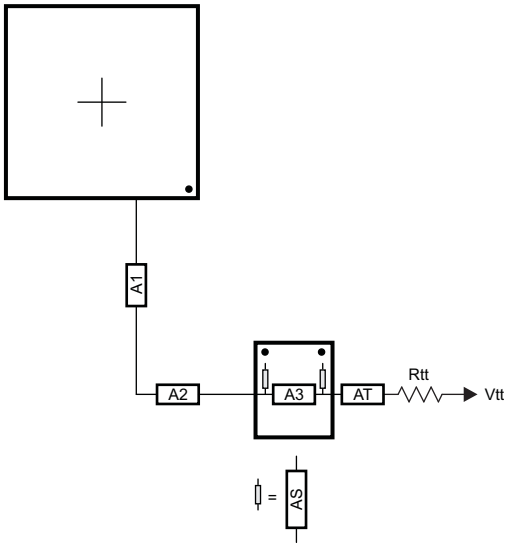
**図 5-59. ADDR_CTRL Routing for Two Single-Side DDR3 Devices**

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. 図 5-60 and 図 5-61 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-60. CK Routing for Two Mirrored DDR3 Devices**




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

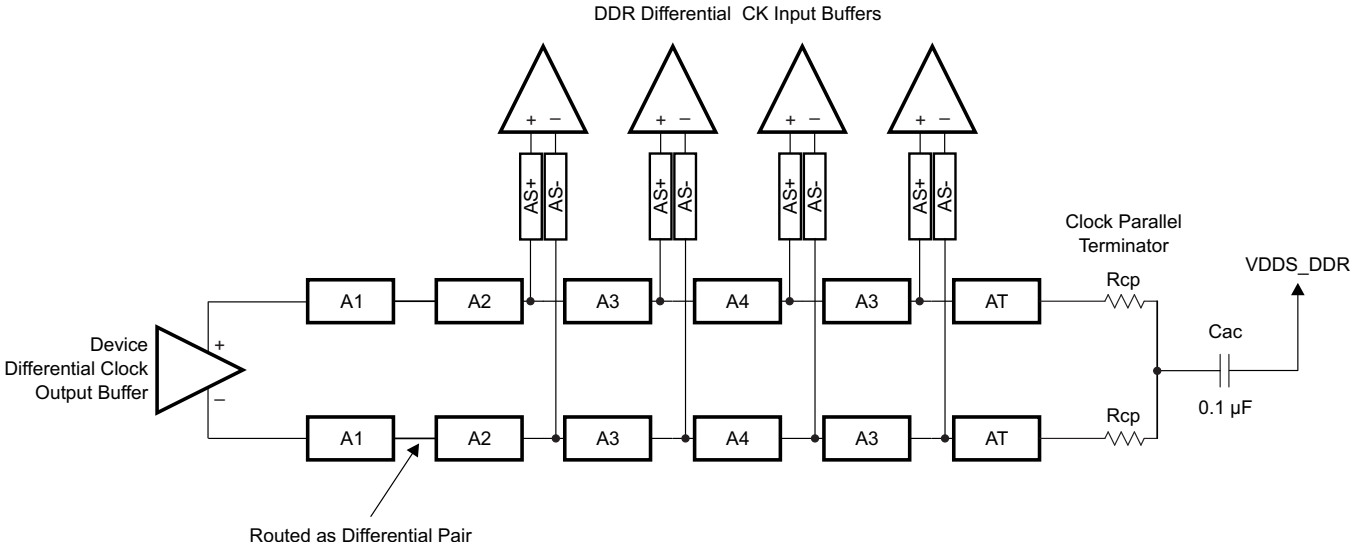
**図 5-61. ADDR_CTRL Routing for Two Mirrored DDR3 Devices**

#### 5.12.8.2.1.4.4 Using Four 8-Bit DDR3 Devices

Two DDR3 devices are supported on the DDR3 interface consisting of four x8 DDR3 devices arranged as one 32-bit bank. These four devices may be mounted on one side of the PCB, or may be mirrored in pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

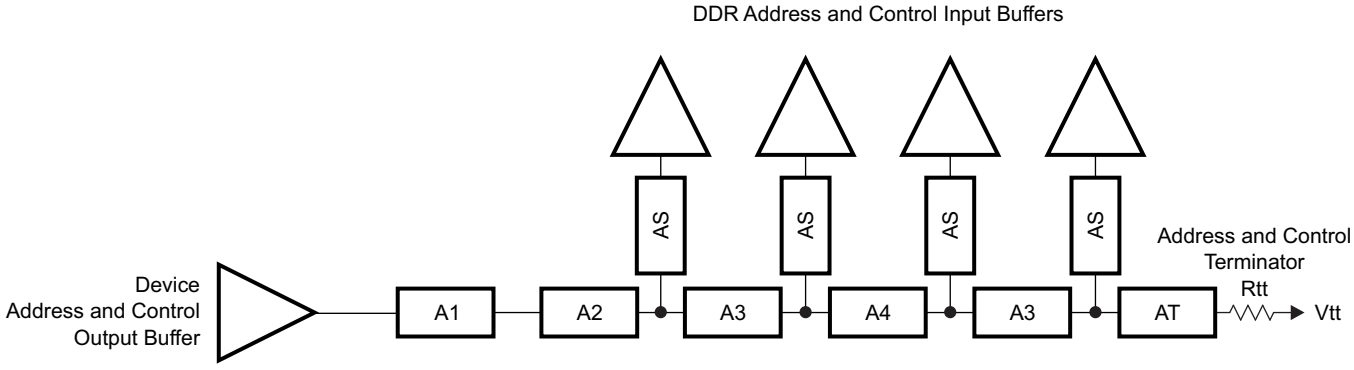
#### 5.12.8.2.1.4.5 CK and ADDR_CTRL Topologies, Four DDR3 Devices

図 5-62 shows the topology of the CK net classes and 図 5-63 shows the topology for the corresponding ADDR_CTRL net classes.




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-62. CK Topology for Four DDR3 Devices**

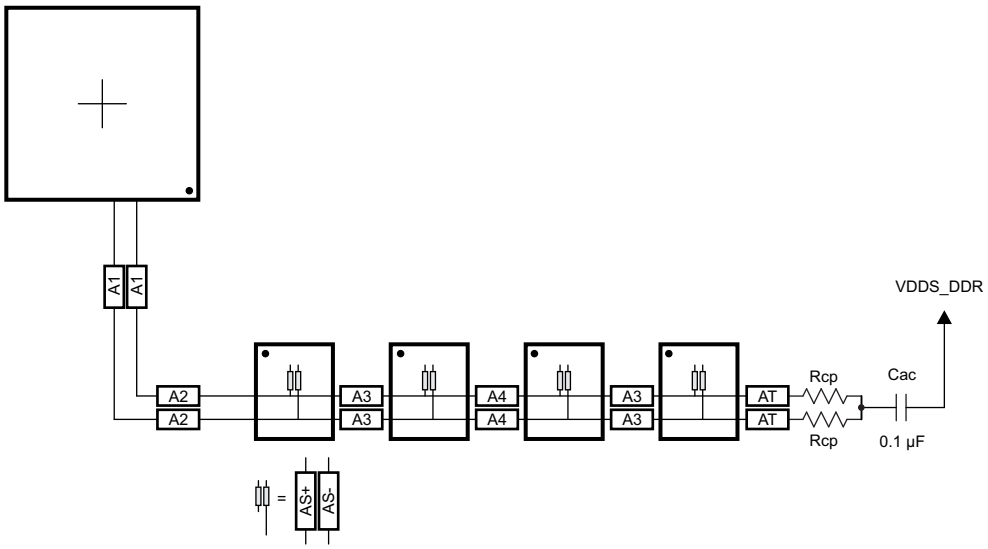



NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-63. ADDR_CTRL Topology for Four DDR3 Devices**

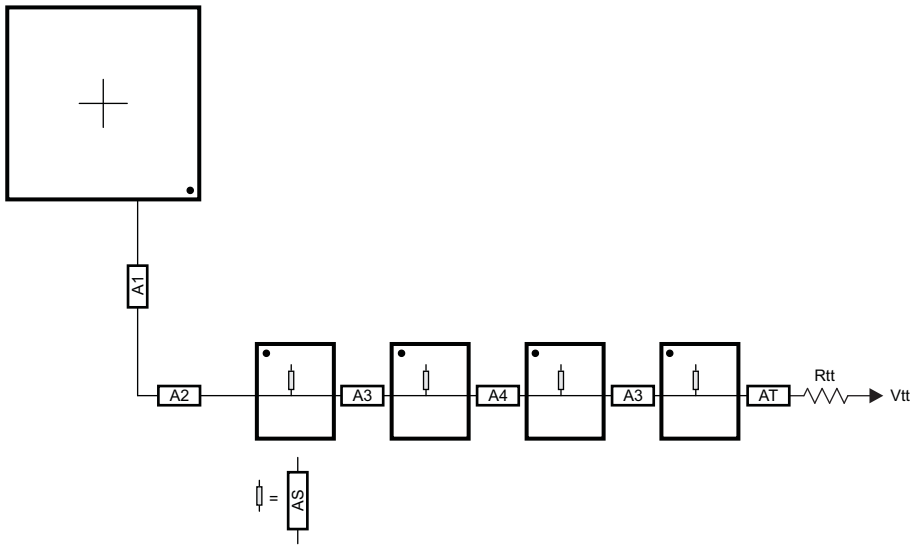
#### 5.12.8.2.1.4.6 CK and ADDR_CTRL Routing, Four DDR3 Devices

図 5-64 shows the CK routing for four DDR3 devices placed on the same side of the PCB. 図 5-65 shows the corresponding ADDR_CTRL routing.




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-64. CK Routing for Four Single-Side DDR3 Devices**




NOTE: For routing definitions, see 表 5-58, *CK and ADDR_CTRL Routing Specification*.

**図 5-65. ADDR_CTRL Routing for Four Single-Side DDR3 Devices**

To save PCB space, the four DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. 図 5-66 and 図 5-67 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a single-pair configuration.

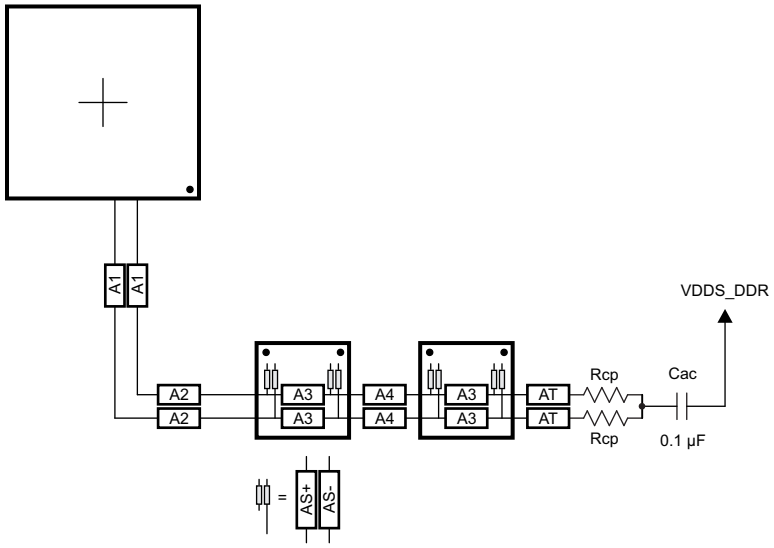



**図 5-66. CK Routing for Four Mirrored DDR3 Devices**

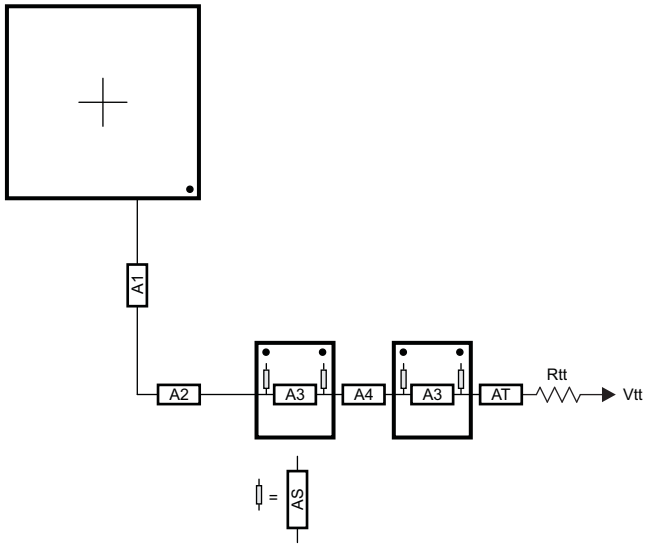



**図 5-67. ADDR_CTRL Routing for Four Mirrored DDR3 Devices**

#### 5.12.8.2.1.4.7 One 16-Bit DDR3 Device

One DDR3 device is supported on the DDR3 interface consisting of one x16 DDR3 device arranged as one 16-bit bank.

#### 5.12.8.2.1.4.8 CK and ADDR_CTRL Topologies, One DDR3 Device

図 5-68 shows the topology of the CK net classes and 図 5-69 shows the topology for the corresponding ADDR_CTRL net classes.

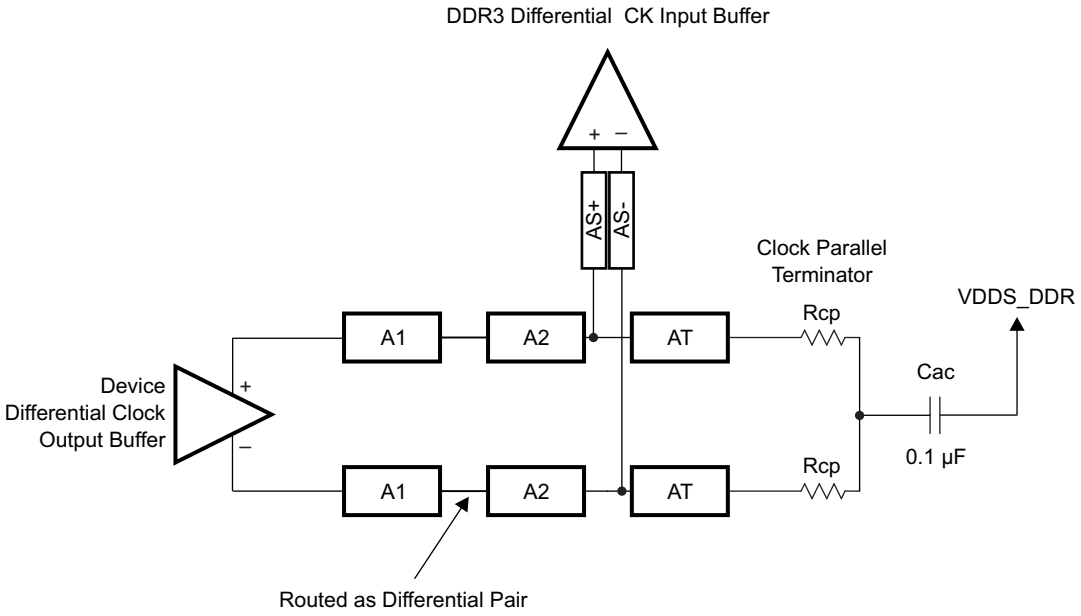



**図 5-68. CK Topology for One DDR3 Device**

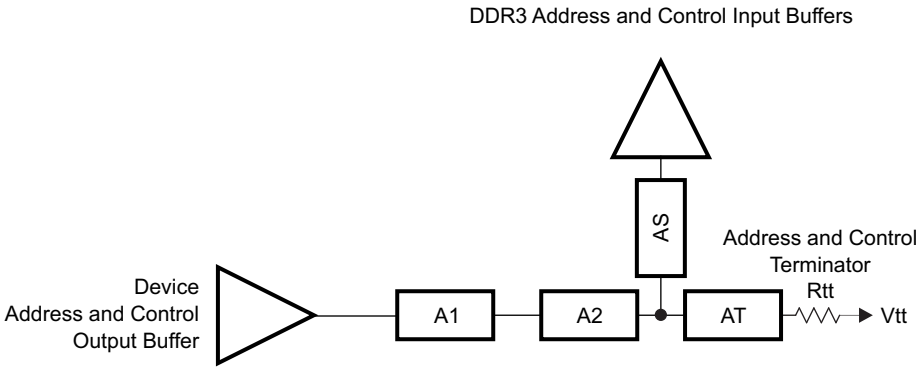



**図 5-69. ADDR_CTRL Topology for One DDR3 Device**

#### 5.12.8.2.1.4.9 CK and ADDR_CTRL Routing, One DDR3 Device

図 5-70 shows the CK routing for one DDR3 device. 図 5-71 shows the corresponding ADDR_CTRL routing.

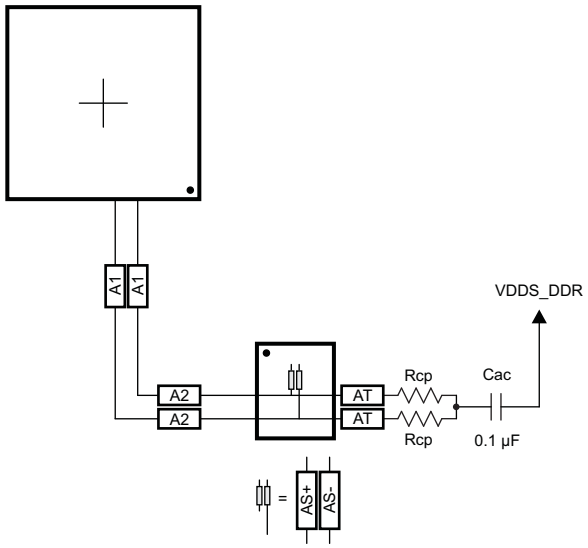



**図 5-70. CK Routing for One DDR3 Device**

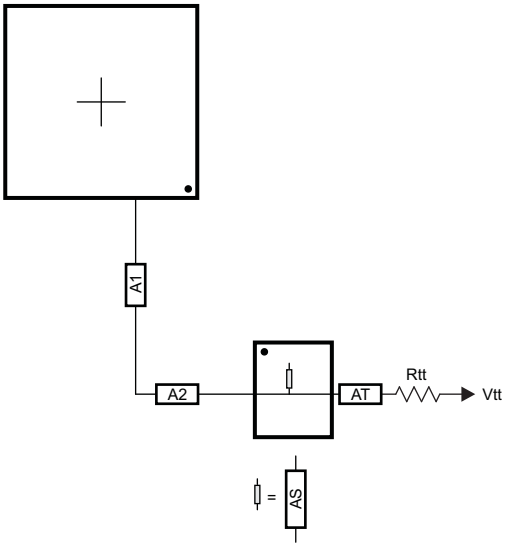


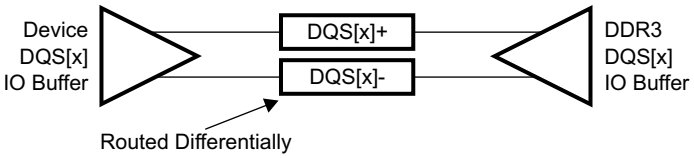

**図 5-71. ADDR_CTRL Routing for One DDR3 Device**

#### 5.12.8.2.1.5 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

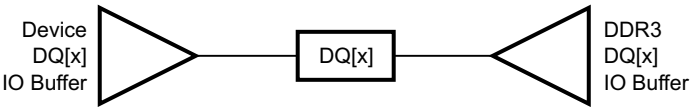
##### 5.12.8.2.1.5.1 DQS[x] and DQ[x] Topologies, Any Number of Allowed DDR3 Devices

DQS[x] lines are point-to-point differential, and DQ[x] lines are point-to-point singled ended. 図 5-72 and 図 5-73 show these topologies.




x = 0, 1, 2, 3

**図 5-72. DQS[x] Topology**

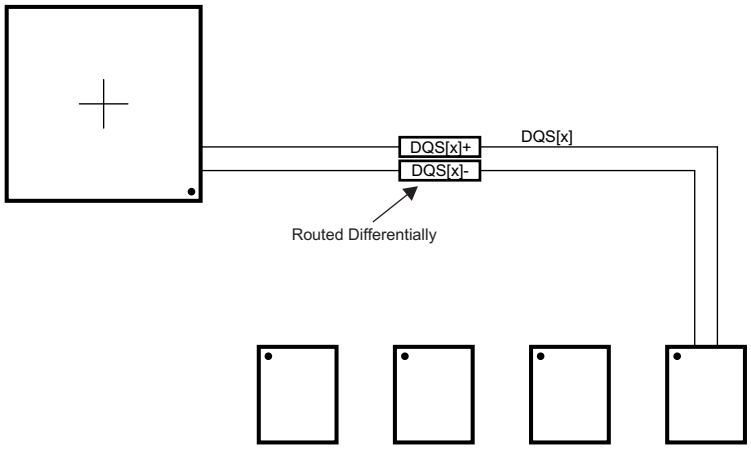



x = 0, 1, 2, 3

**図 5-73. DQ[x] Topology**

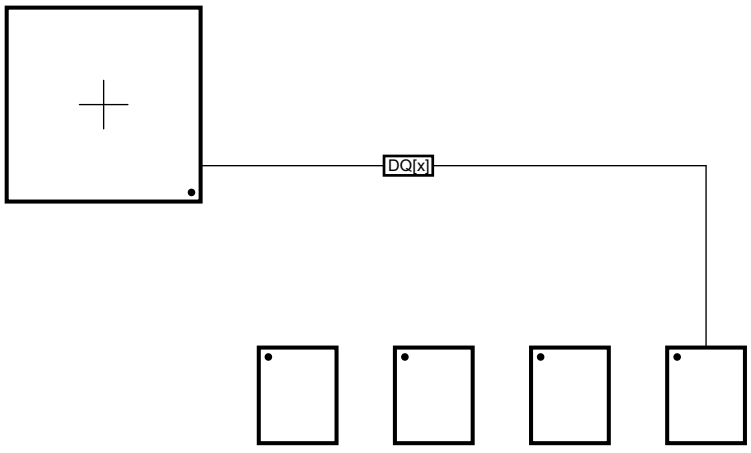
### *5.12.8.2.1.5.2 DQS[x] and DQ[x] Routing, Any Number of Allowed DDR3 Devices*

図 5-74 and 図 5-75 show the DQS[x] and DQ[x] routing.




x = 0, 1, 2, 3

**図 5-74. DQS[x] Routing With Any Number of Allowed DDR3 Devices**




x = 0, 1, 2, 3

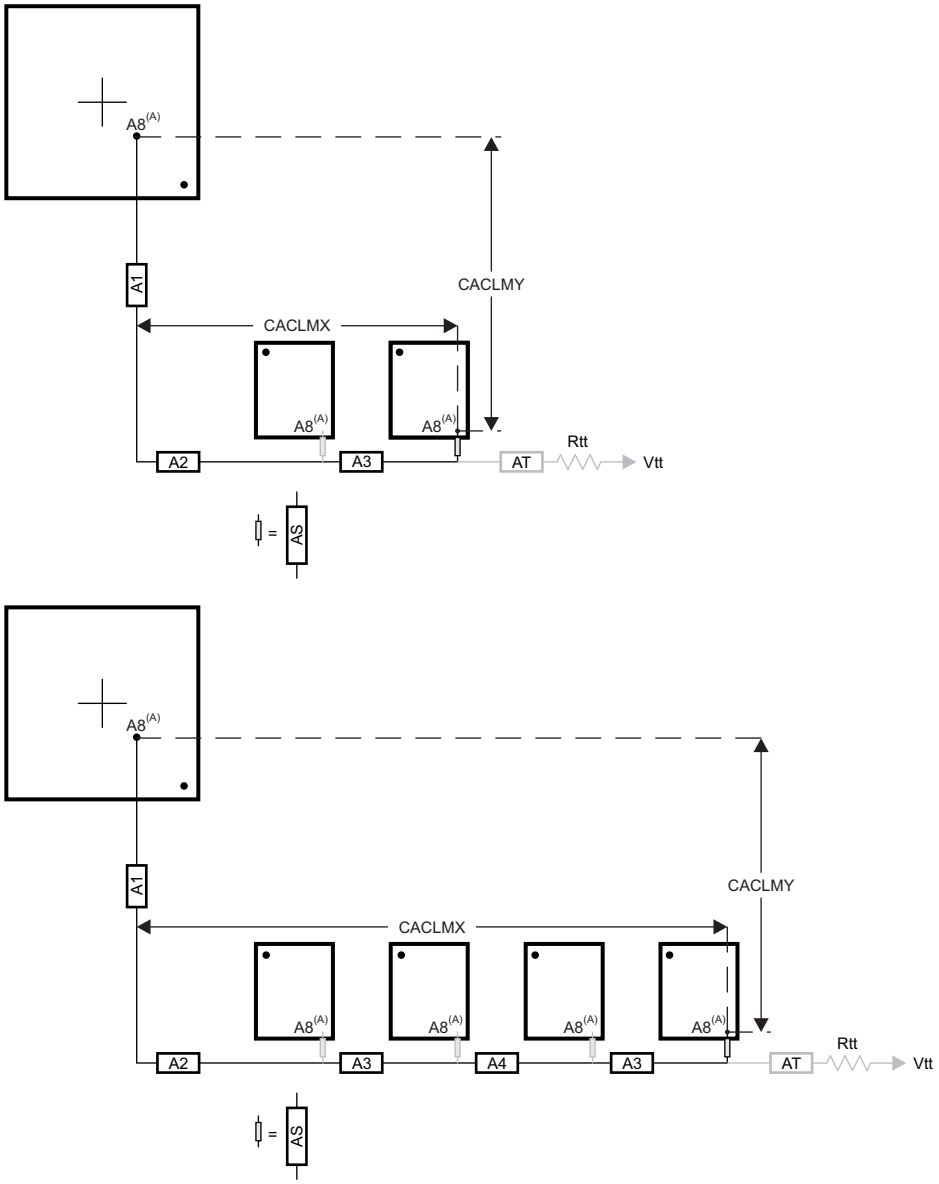
**図 5-75. DQ[x] Routing With Any Number of Allowed DDR3 Devices**

#### 5.12.8.2.1.6 Routing Specification

##### 5.12.8.2.1.6.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the device and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. 図 5-76 shows this distance for two loads. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK and ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in 表 5-58.




A. It is very likely that the longest CK and ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK and ADDR_CTRL skew matching and length control.

The length of shorter CK and ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Nonincluded lengths are grayed out in the figure.

Assuming A8 is the longest, CACLM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

**図 5-76. CACLM for Two or Four Address Loads on One Side of PCB**

**表 5-58. CK and ADDR_CTRL Routing Specification(1)(2)(3)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | A1+A2 length | | | 2500 | mils |
| 2 | A1+A2 skew | | | 25 | mils |
| 3 | A3 length | | | 660 | mils |
| 4 | A3 skew(4) | | | 25 | mils |
| 5 | A3 skew(5) | | | 125 | mils |

表 5-58. CK and ADDR_CTRL Routing Specification(1)(2)(3) (continued)

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 6 | A4 length | | | 660 | mils |
| 7 | A4 skew | | | 25 | mils |
| 8 | AS length | | | 100 | mils |
| 9 | AS skew | | | 25 | mils |
| 10 | AS+ and AS- length | | | 70 | mils |
| 11 | AS+ and AS- skew | | | 5 | mils |
| 12 | AT length(6) | | 500 | | mils |
| 13 | AT skew(7) | | 100 | | mils |
| 14 | AT skew(8) | | | 5 | mils |
| 15 | CK and ADDR_CTRL nominal trace length(9) | CACLM-50 | CACLM | CACLM+50 | mils |
| 16 | Center-to-center CK to other DDR3 trace spacing(10) | 4 | | | w |
| 17 | Center-to-center ADDR_CTRL to other DDR3 trace spacing(10)(11) | 4 | | | w |
| 18 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(10) | 3 | | | w |
| 19 | CK center-to-center spacing(12) | | | | |
| 20 | CK spacing to other net(10) | 4 | | | w |
| 21 | Rcp(13) | Zo-1 | Zo | Zo+1 | Ω |
| 22 | Rtt(13)(14) | Zo-5 | Zo | Zo+5 | Ω |

(1) CK represents the clock net class, and ADDR_CTRL represents the address and control signal net class.

(2) The use of vias should be minimized.

(3) Additional bypass capacitors are required when using the VDDS_DDR plane as the reference plane to allow the return current to jump between the VDDS_DDR plane and the ground plane when the net class switches layers at a via.

(4) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).

(5) Nonmirrored configuration (all DDR3 memories on same side of PCB).

(6) While this length can be increased for convenience, its length should be minimized.

(7) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.

(8) CK net class only.

(9) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see 5.12.8.2.1.6.1 and 図 5-76.

(10) Center-to-center spacing is allowed to fall to minimum (w) for up to 1250 mils of routed length.

(11) Signals from one DQ net class should be considered other DDR3 traces to another DQ net class.

(12) CK spacing set to ensure proper differential impedance. Differential impedance should be Zo x 2, where Zo is the single-ended impedance defined in 表 5-52.

(13) Source termination (series resistor at driver) is specifically not allowed.

(14) Termination values should be uniform across the net class.

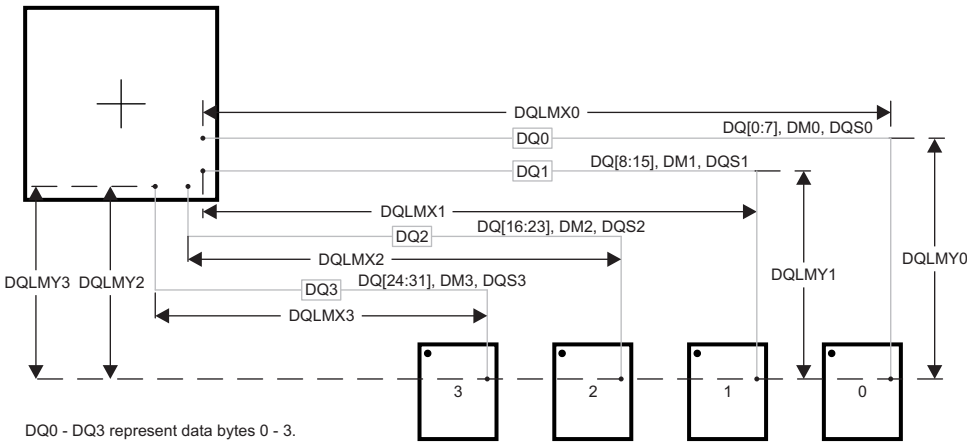
#### 5.12.8.2.1.6.2 DQS[x] and DQ[x] Routing Specification

Skew within the DQS[x] and DQ[x] net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 16-bit interface, there are two DQLMs, DQLM0 and DQLM1.

注

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS[x] and DQ[x] pin locations on the device and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. 図 5-77 shows this distance for a two-load case. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS[x] and DQ[x] routing, these specifications are contained in 表 5-59.




There are four DQLMs, one for each byte (16-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

**図 5-77. DQLM for Any Number of Allowed DDR3 Devices**

**表 5-59. DQS[x] and DQ[x] Routing Specification(1)(2)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DQ0 nominal length(3)(4) | | | DQLM0 | mils |
| 2 | DQ1 nominal length(3)(5) | | | DQLM1 | mils |
| 3 | DQ2 nominal length | | | DQLM2 | mils |
| 4 | DQ3 nominal length | | | DQLM3 | mils |
| 5 | DQ[x] skew(6) | | | 25 | mils |
| 6 | DQS[x] skew | | | 5 | mils |
| 7 | DQS[x]-to-DQ[x] skew(6)(7) | | | 25 | mils |
| 8 | Center-to-center DQ[x] to other DDR3 trace spacing(8)(9) | 4 | | | w |
| 9 | Center-to-center DQ[x] to other DQ[x] trace spacing(8)(10) | 3 | | | w |
| 10 | DQS[x] center-to-center spacing(11) | | | | |
| 11 | DQS[x] center-to-center spacing to other net(8) | 4 | | | w |

(1) DQS[x] represents the DQS0 and DQS1 clock net classes, and DQ[x] represents the DQ0 and DQ1 signal net classes.

(2) External termination disallowed. Data termination should use built-in ODT functionality.

(3) DQLMn is the longest Manhattan distance of a byte. For definition, see 5.12.8.2.1.6.2 and 図 5-77.

(4) DQLM0 is the longest Manhattan length for the DQ0 net class.

(5) DQLM1 is the longest Manhattan length for the DQ1 net class.

(6) Length matching is only done within a byte. Length matching across bytes is not required. To maintain tighter delay skew, route the DQ[x] and DQS[x] signals within a byte to have same number of VIA and layer transitions.

(7) Each DQS clock net class is length matched to its associated DQ signal net class.

(8) Center-to-center spacing is allowed to fall to minimum for up to 1250 mils of routed length.

(9) Other DDR3 trace spacing means signals that are not part of the same DQ[x] signal net class.

(10) This applies to spacing within same DQ[x] signal net class.

(11) DQS[x] pair spacing is set to ensure proper differential impedance. Differential impedance should be Zo × 2, where Zo is the single-ended impedance defined in 表 5-52.

#### 5.12.8.2.2 LPDDR2 Routing Guidelines

This section provides the timing specification for the LPDDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable LPDDR2 memory system without the need for a complex timing closure process. For more information regarding guidelines for using this LPDDR2 specification, see *Understanding TI's PCB Routing Rule-Based DDR Timing Specification*. This application report provides generic guidelines and approach. All the specifications provided in the data manual take precedence over the generic guidelines and must be adhered to for a reliable LPDDR2 interface operation.

##### 5.12.8.2.2.1 LPDDR2 Board Designs

TI only supports board designs using LPDDR2 memory that follow the guidelines in this document. The switching characteristics and timing diagram for the LPDDR2 memory interface are shown in 表 5-60 and 図 5-78.

**表 5-60. Switching Characteristics for LPDDR2 Memory Interface**

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(DDR\_CK)}$ | Cycle time, DDR_CK and DDR_CKn | 7.52 | 3.76(1) | ns |

(1) The JEDEC JESD209-2F standard defines the maximum clock period of 100 ns for all standard-speed bin LPDDR2 memory. The device has only been tested per the limits published in this table.

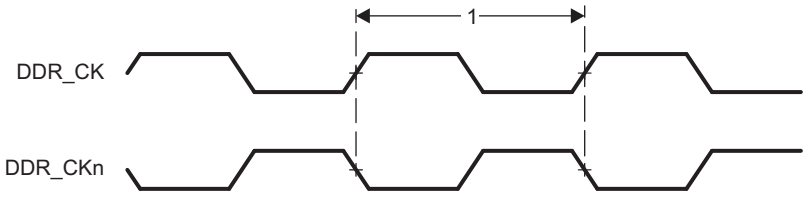



**図 5-78. LPDDR2 Memory Interface Clock Timing**

##### 5.12.8.2.2.2 LPDDR2 Device Configurations

There are several possible combinations of device counts and single-side or dual-side mounting. 表 5-61 lists all the supported configurations.

**表 5-61. Supported LPDDR2 Device Combinations**

| NUMBER OF LPDDR2 DEVICES | LPDDR2 DEVICE WIDTH (BITS) | MIRRORED?(1) | LPDDR2 EMIF WIDTH (BITS) |
|---|---|---|---|
| 1 | 32 | N | 32 |
| 2(2) | 32 | N | 32 |
| 1 | 16 | N | 16 |
| 2(2) | 16 | N | 16 |

(1) Two LPDDR2 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.

(2) Two devices are supported only with twin-die configuration which embeds two devices in the same package.

Details on treating unused pins are listed in 5.12.8.2.2.3.1.

#### 5.12.8.2.2.3 LPDDR2 Interface

##### 5.12.8.2.2.3.1 LPDDR2 Interface Schematic

The LPDDR2 interface schematic varies, depending upon the width of the LPDDR2 devices used. 図 5-79 shows the schematic connections for 16-bit interface using one x16 LPDDR2 device. Two x16 LPDDR2 devices are supported for twin-die configuration which embeds two devices in the same package.

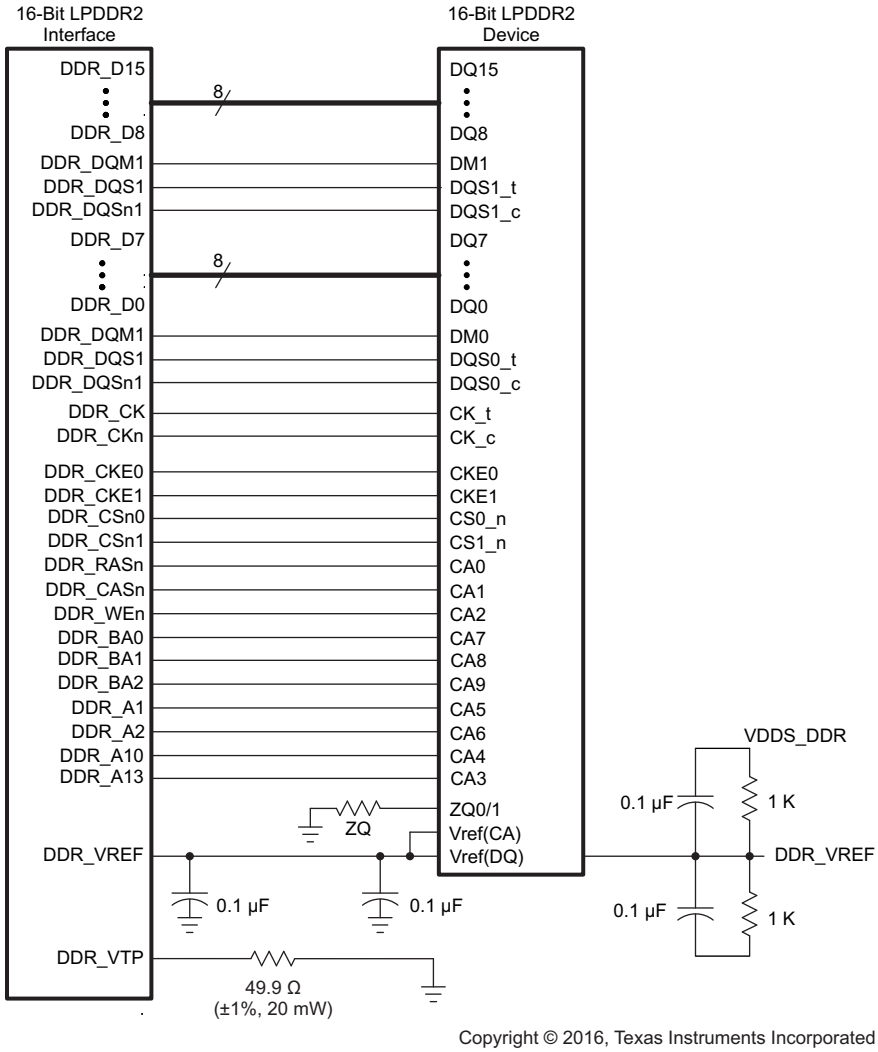



**図 5-79. 16-Bit Interface Using One 16-Bit LPDDR2 Device**

図 5-80 shows the schematic connections for 32-bit interface using one x32 LPDDR2 device.

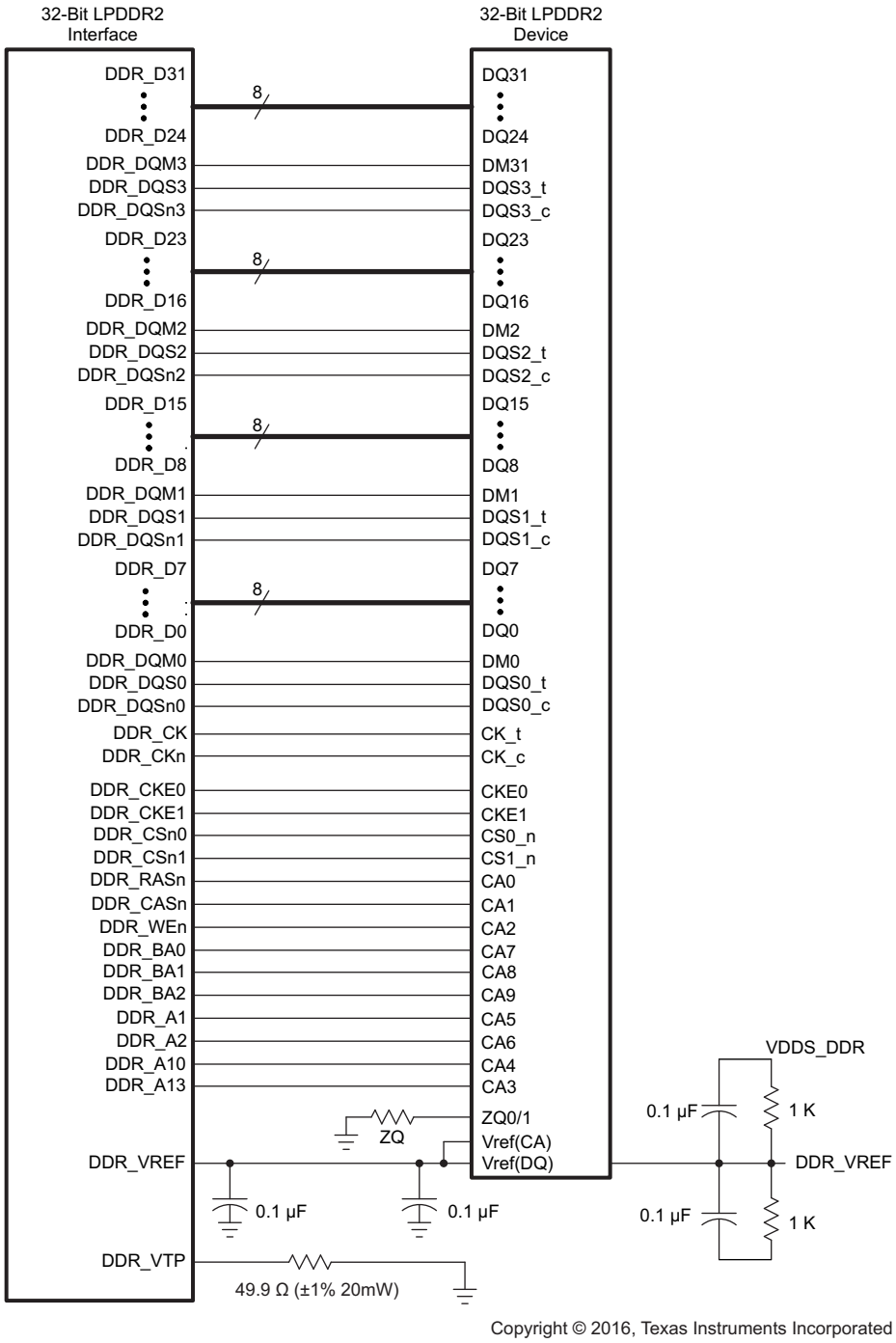



**図 5-80. 32-Bit Interface Using One 32-Bit LPDDR2 Device**

When not using a part of LPDDR2 interface (using x16 or not using the LPDDR2 interface):

- Connect the VDDS_DDR supply to 1.8 V
- Connect the DDR_VREF supply to 0.9 V
- Tie off DDR_DQS[x] (x=0,1,2,3) that are unused to VSS via 1 kΩ
- Tie off DDR_DQSn[x] (x=0,1,2,3) that are unused to VDDS_DDR via 1 kΩ
- All other unused pins can be left as NC.

**Note:** All the unused DDR ADDR_CTRL lines used for DDR3 operation should be left as NC.

#### 5.12.8.2.2.3.2 Compatible JEDEC LPDDR2 Devices

表 5-62 shows the supported LPDDR2 device configurations which are compatible with this interface.

**表 5-62. Compatible JEDEC LPDDR2 Devices (Per Interface)**

| NO. | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | JEDEC LPDDR2 device speed grade | $t_{c(DDR\_CK)}$ and $t_{c(DDR\_CKn)}$ | LPDDR2-533 | | |
| 2 | JEDEC LPDDR2 device bit width | | x16 | x32 | Bits |
| 3 | JEDEC LPDDR2 device count | | 1 | 2(1) | Devices |

(1) Two devices are supported only with twin-die configuration which embeds two devices in the same package.

#### 5.12.8.2.2.3.3 LPDDR2 PCB Stackup

表 5-63 shows the minimum stackup requirements. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance signal integrity and electromagnetic interference performance, or to reduce the size of the PCB footprint.

**表 5-63. Minimum PCB Stackup**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top signal routing |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Bottom signal routing |

PCB stackup specifications for LPDDR2 interface are listed in 表 5-64.

**表 5-64. PCB Stackup Specifications(1)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB routing and plane layers | 4 | | | |
| 2 | Signal routing layers | 2 | | | |
| 3 | Full ground reference layers under LPDDR2 routing region(1) | 1 | | | |
| 4 | Full VDDS_DDR power reference layers under the LPDDR2 routing region(1) | 1 | | | |
| 5 | Number of reference plane cuts allowed within LPDDR2 routing region(2) | | | 0 | |
| 6 | Number of layers between LPDDR2 routing layer and reference plane(3) | | | 0 | |
| 7 | PCB routing feature size | | 4 | | mils |
| 8 | PCB trace width, w | | 4 | | mils |
| 9 | PCB BGA escape via pad size(4) | | 18 | 20 | mils |
| 10 | PCB BGA escape via hole size | | 10 | | mils |
| 11 | Single-ended impedance, Zo(5) | | 50 | 75 | Ω |
| 12 | Impedance control(6)(7) | Zo-5 | Zo | Zo+5 | Ω |

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.

(2) No traces should cross reference plane cuts within the LPDDR2 routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.

(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.

(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.

(5) Zo is the nominal singled-ended impedance selected for the PCB.

(6) This parameter specifies the AC characteristic impedance tolerance for each segment of a PCB signal trace relative to the chosen Zo defined by the single-ended impedance parameter.

(7) Tighter impedance control is required to ensure flight time skew is minimal.

#### 5.12.8.2.2.3.4 LPDDR2 Placement

図 5-81 shows the placement rules for the device as well as the LPDDR2 memory device. Placement restrictions are provided as a guidance to restrict maximum trace lengths and allow for proper routing space.

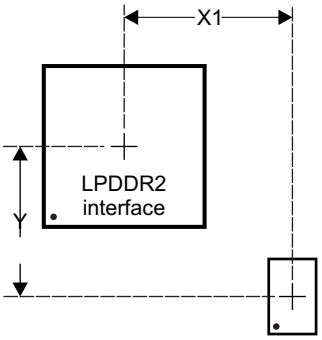



**図 5-81. Placement Specifications**

**表 5-65. Placement Specifications(1)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X1 Offset(2)(3) | | 1500 | mils |
| 2 | Y Offset(2)(3)(4) | | 1500 | mils |
| 3 | Clearance from non-LPDDR2 signal to LPDDR2 keepout region(4)(5) | 4 | | w |

(1) LPDDR2 keepout region to encompass entire LPDDR2 routing area.

(2) Measurements from center of device to center of LPDDR2 device.

(3) Minimizing X1 and Y improves timing margins.

(4) w is defined as the signal trace width.

(5) Non-LPDDR2 signals allowed within LPDDR2 keepout region provided they are separated from LPDDR2 routing layers by a ground plane.

#### 5.12.8.2.2.3.5 LPDDR2 Keepout Region

The region of the PCB used for LPDDR2 circuitry must be isolated from other signals. The LPDDR2 keepout region is defined for this purpose and is shown in 図 5-82. This region should encompass all LPDDR2 circuitry and the region size varies with component placement and LPDDR2 routing. Non-LPDDR2 signals should not be routed on the same signal layer as LPDDR2 signals within the LPDDR2 keepout region. Non-LPDDR2 signals may be routed in the region provided they are routed on layers separated from LPDDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground or VDDS_DDR power plane in this region. In addition, the VDDS_DDR power plane should cover the entire keepout region.

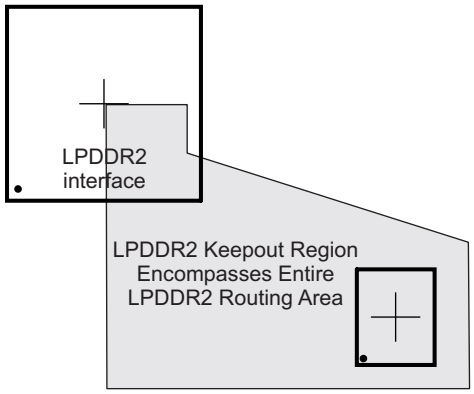



**図 5-82. LPDDR2 Keepout Region**

#### *5.12.8.2.2.3.6 LPDDR2 Net Classes*

**表 5-66. Clock Net Class Definitions for the LPDDR2 Interface**

| CLOCK NET CLASS | PIN NAMES |
|---|---|
| CK | DDR_CK and DDR_CKn |
| DQS0 | DDR_DQS0 and DDR_DQSn0 |
| DQS1 | DDR_DQS1 and DDR_DQSn1 |
| DQS2 | DDR_DQS2 and DDR_DQSn2 |
| DQS3 | DDR_DQS3 and DDR_DQSn3 |

**表 5-67. Signal Net Class and Associated Clock Net Class for LPDDR2 Interface**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_CSn0, DDR_CSn1, DDR_CKE0, DDR_CKE1, DDR_RASn, DDR_CASn, DDR_WEn, DDR_A1, DDR_A2, DDR_A10, DDR_A13 |
| DQ0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| DQ1 | DQS1 | DDR_D[15:8], DDR_DQM1 |
| DQ2 | DQS2 | DDR_D[23:16], DDR_DQM2 |
| DQ3 | DQS3 | DDR_D[31:24], DDR_DQM3 |

#### *5.12.8.2.2.3.7 LPDDR2 Signal Termination*

On-device termination (ODT) is available for DQ[3:0] signal net classes, but is not specifically required for normal operation. System designers may evaluate the need for additional series termination if required based on signal integrity, EMI and overshoot/undershoot reduction.

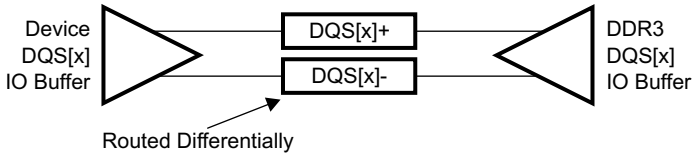
#### *5.12.8.2.2.3.8 LPDDR2 DDR_VREF Routing*

DDR_VREF is the reference voltage for the input buffers on the LPDDR2 memory as well as the device. DDR_VREF is intended to be half the LPDDR2 power supply voltage and is typically generated with a voltage divider connected to the VDDS_DDR power supply. It should be routed as a nominal 20-mil wide trace with 0.1-µF bypass capacitors near each device connection. Narrowing of DDR_VREF is allowed to accommodate routing congestion.

#### 5.12.8.2.2.4 Routing Specification

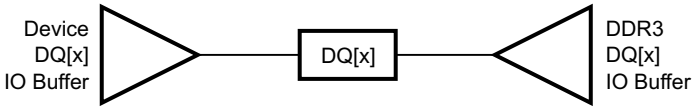
##### 5.12.8.2.2.4.1 DQS[x] and DQ[x] Routing Specification

DQS[x] lines are point-to-point differential and DQ[x] lines are point-to-point single ended. 図 5-83 and 図 5-84 represent the supported topologies. 図 5-85 and 図 5-86 show the DQS[x] and DQ[x] routing. 図 5-87 shows the DQLM for the LPDDR2 interface.



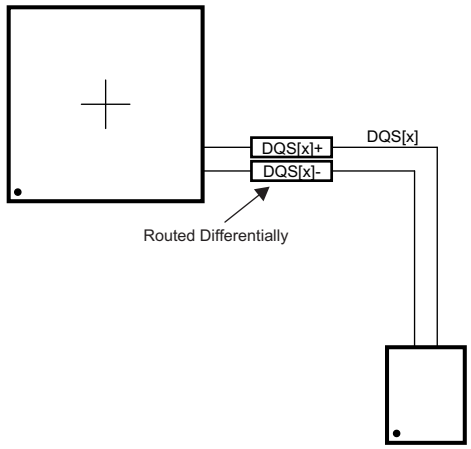

x = 0, 1, 2, 3

**図 5-83. DQS[x] Topology**



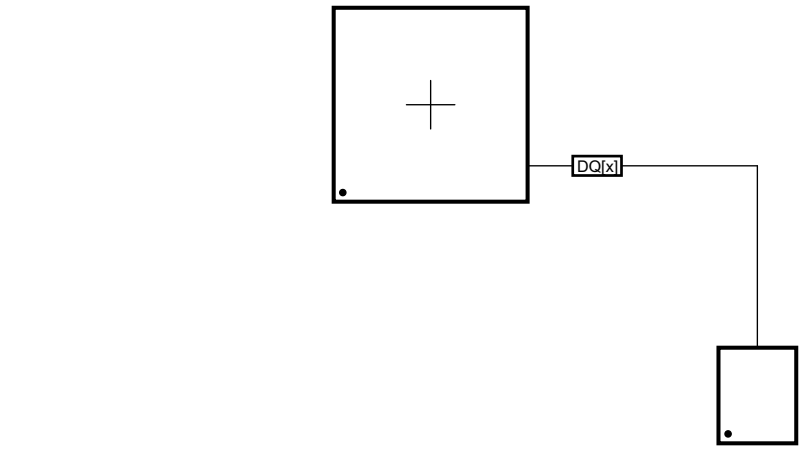

x = 0, 1, 2, 3

**図 5-84. DQ[x] Topology**



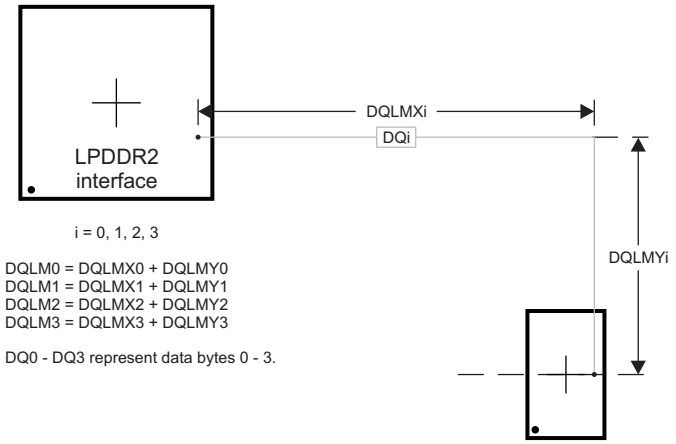

x = 0, 1, 2, 3

**図 5-85. DQS[x] Routing**




x = 0, 1, 2, 3

**図 5-86. DQ[x] Routing**




There are four DQLMs, one for each data byte, in a 32-bit interface and two DQLMs, one for each data byte, in a 16-bit interface. Each DQLM is the longest Manhattan distance of the byte.

**図 5-87. DQLM for LPDDR2 Interface**

Trace routing specifications for the DQ[x] and the DQS[x] are specified in 表 5-68.

**表 5-68. DQS[x] and DQ[x] Routing Specification(1)(2)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DQ0 nominal length(3)(4) | | | DQLM0 | mils |
| 2 | DQ1 nominal length(3)(5) | | | DQLM1 | mils |
| 3 | DQ2 nominal length (3)(6) | | | DQLM2 | mils |
| 4 | DQ3 nominal length (3)(7) | | | DQLM3 | mils |
| 5 | DQ[x] skew(8) | | | 50 | mils |
| 6 | DQS[x] skew | | | 10 | mils |
| 7 | Via count per each trace in DQ[x], DQS[x] | | | 2 | |
| 8 | Via count difference across a given DQ[x], DQS[x] | | | 0 | |
| 9 | DQS[x]-to-DQ[x] skew(8)(9) | | | 50 | mils |
| 10 | Center-to-center DQ[x] to other LPDDR2 trace spacing(10)(11) | 4 | | | w |
| 11 | Center-to-center DQ[x] to other DQ[x] trace spacing(10)(12) | 3 | | | w |
| 12 | DQS[x] center-to-center spacing(13) | | | | |
| 13 | DQS[x] center-to-center spacing to other net(10) | 4 | | | w |

(1) DQS[x] represents the DQS0, DQS1, DQS2, DQS3 clock net classes, and DQ[x] represents the DQ0, DQ1, DQ2, DQ3 signal net classes.
(2) External termination disallowed. Data termination should use built-in ODT functionality.
(3) DQLMn is the longest Manhattan distance of a byte.
(4) DQLM0 is the longest Manhattan length for the DQ0 net class.
(5) DQLM1 is the longest Manhattan length for the DQ1 net class.
(6) DQLM2 is the longest Manhattan length for the DQ2 net class.
(7) DQLM3 is the longest Manhattan length for the DQ3 net class.
(8) Length matching is only done within a byte. Length matching across bytes is not required.
(9) Each DQS clock net class is length matched to its associated DQ signal net class.
(10) Center-to-center spacing is allowed to fall to minimum for up to 1000 mils of routed length.
(11) Other LPDDR2 trace spacing means signals that are not part of the same DQ[x] signal net class.
(12) This applies to spacing within same DQ[x] signal net class.
(13) DQS[x] pair spacing is set to ensure proper differential impedance. Differential impedance should be Zo x 2, where Zo is the single-ended impedance.

#### *5.12.8.2.2.4.2 CK and ADDR_CTRL Routing Specification*

CK signals are routed as point-to-point differential, and ADDR_CTRL signals are routed as point-to-point single ended. The supported topology for CK and ADDR_CTRL are shown in 図 5-88 through 図 5-91. ADDR_CTRL are routed very similar to DQ and CK is routed very similar to DQS.

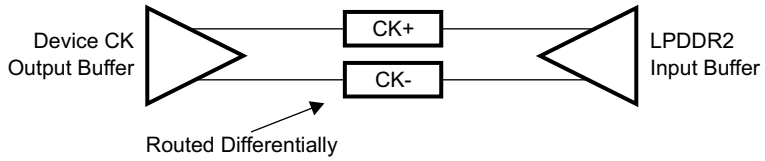



**図 5-88. CK Signals Topology**


**図 5-89. ADDR_CTRL Signals Topology**

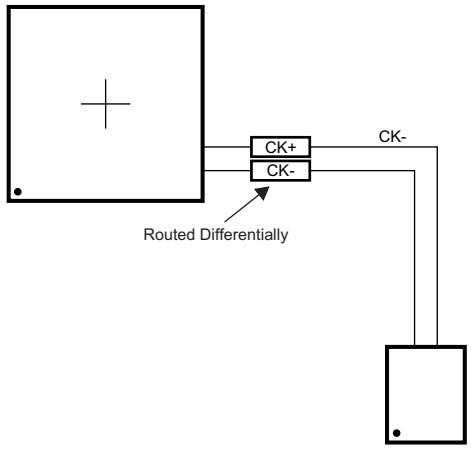



**図 5-90. CK Signals Routing**

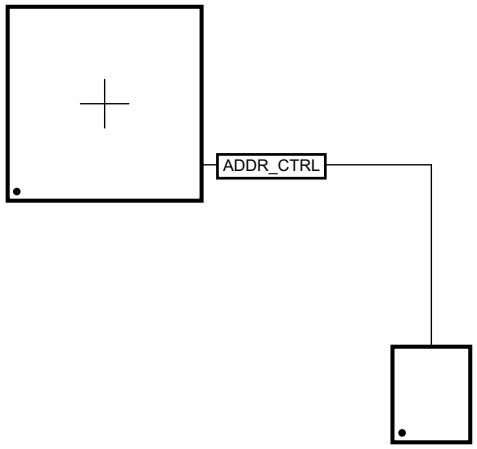
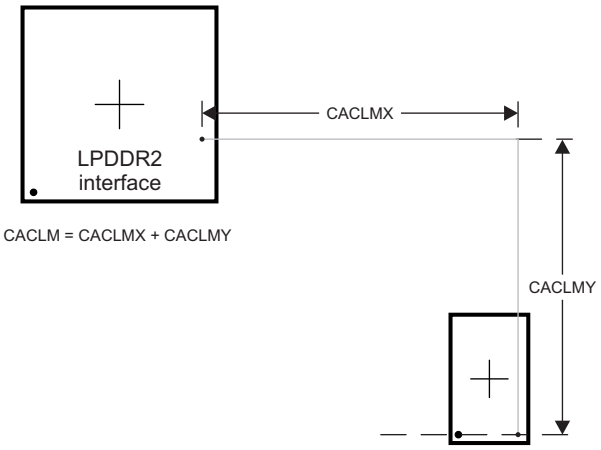



**図 5-91. ADDR_CTRL Signals Routing**




CACLM is the longest Manhattan distance of the CK/ADDR_CTRL signal class.

**図 5-92. CACLM for LPDDR2 Interface**

Trace routing specifications for the CK and the ADD_CTRL are specified in 表 5-69.

**表 5-69. CK and ADDR_CTRL Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | CK and ADDR_CTRL nominal trace length(1) | | | CACLM | mils |
| 2 | ADDR_CTRL skew | | | 50 | mils |
| 3 | CK skew | | | 10 | mils |
| 4 | Via count per each trace ADDR_CTRL, CK | | | 2 | |
| 5 | Via count difference across ADDR_CTRL, CK | | | 0 | |
| 6 | ADDR_CTRL-to-CK skew | | | 50 | mils |
| 7 | Center-to-center ADDR_CTRL to other LPDDR2 trace spacing(2)(3) | 4 | | | w |
| 8 | Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(2) | 3 | | | w |
| 9 | CK center-to-center spacing(4) | | | | |
| 10 | CK center-to-center spacing to other net(2) | 4 | | | w |

(1) CACLM is the longest Manhattan distance of ADDR_CTRL and CK.

(2) Center-to-center spacing is allowed to fall to minimum for up to 1000 mils of routed length.

(3) Other LPDDR2 trace spacing means signals that are not part of the same CK, ADDR_CTRL signal net class.

(4) CK pair spacing is set to ensure proper differential impedance. Differential impedance should be Zo x 2, where Zo is the single ended impedance.

### 5.12.9 Display Subsystem (DSS)

注

For more information, see the Display Subsystem chapter of the *AM437x Sitara Processors Technical Reference Manual*.

The display subsystem (DSS) provides the logic to display the video frame from external (SDRAM) or internal (SRAM) memory on an LCD panel or a TV set. The display subsystem integrates the following elements:

- Display controller (DISPC) module
- Remote frame buffer interface (RFBI) module

The DSS can be used in the following configuration: LCD display with parallel interface

#### 5.12.9.1 DSS—Parallel Interface

In parallel interface, the paths of the display subsystem modules are the display controller and the RFBI. The display controller has two I/O pad modes and could be in the following configuration:

- Bypass mode (RFBI disabled), which implements the MIPI DPI protocol
- RFBI mode (RFBI enabled), which implements MIPI DBI 2.0 type B protocol

##### 5.12.9.1.1 DSS—Parallel Interface—Bypass Mode

Two types of LCD panel are supported:

- Thin film transistor (TFT) or active matrix technology
- Supertwisted nematic (STN) or passive matrix technology

Both configurations are discussed in the following paragraphs.

###### 5.12.9.1.1.1 DSS—Parallel Interface—Bypass Mode—TFT Mode

表 5-71 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-93).

**表 5-70. DSS Timing Conditions—TFT Mode**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance | | 10 | pF |

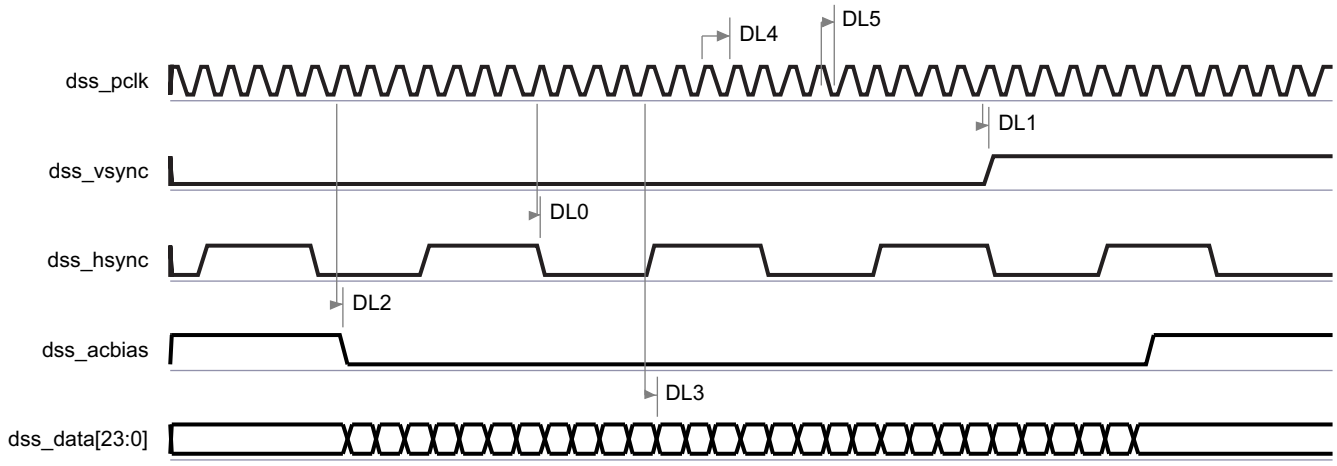
**表 5-71. DSS Switching Characteristics—TFT Mode**

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL0 | $t_{d(pclkA\text{-}hsync)}$ | Delay time, output pixel clock dss_pclk active edge to output horizontal synchronization dss_hsync transition | -2.4 | 2.4 | -3.5 | 2.5 | ns |
| DL1 | $t_{d(pclkA\text{-}vsync)}$ | Delay time, output pixel clock dss_pclk active edge to output vertical synchronization dss_vsync transition | -2.4 | 2.4 | -3.5 | 2.5 | ns |
| DL2 | $t_{d(pclkA\text{-}acbiasA)}$ | Delay time, output pixel clock dss_pclk active edge to output data enable dss_acbias active level | -2.4 | 2.4 | -3.5 | 2.5 | ns |
| DL3 | $t_{d(pclkA\text{-}dV)}$ | Delay time, output pixel clock dss_pclk active edge to output data dss_data[23:0] valid | -2.4 | 2.4 | -3.5 | 2.5 | ns |
| DL4 | $1 / t_{c(pclk)}$ | Frequency(1), output pixel clock dss_pclk | | 100 | | 75 | MHz |

表 5-71. DSS Switching Characteristics—TFT Mode (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL5 | $t_{w(pclk)}$ | Pulse duration, output pixel clock dss_pclk low or high | 0.45P(2) | 0.55P(2)(3) | 0.45P(2) | 0.55P(2)(3) | ns |
| | $t_{J(pclk)}$ | Peak-peak jitter, output pixel clock dss_pclk | | 200 | | 200 | ps |

(1) The pixel clock frequency is software programmable via the pixel clock DISPC_DIVISOR register.
(2) P = dss_pclk period in ns
(3) $t_{w(pclk)}$ = 0.66P when DISPC_DIVISOR[7:0] PCD = 3




A. The pixel data bus depends on the use of 8-, 9-, 12-, 16-, 18-, or 24-bit per pixel data output pins.
B. The pixel clock frequency is programmable.
C. All timings not illustrated in the waveform are progammable by software, and control signal polarity and driven edge of dss_pclk too.
D. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

図 5-93. DSS—TFT Mode

### 5.12.9.1.1.2 DSS—Parallel Interface—Bypass Mode—STN Mode

表 5-73 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-94).

表 5-72. DSS Timing Conditions—STN Mode

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance | | 40 | pF |

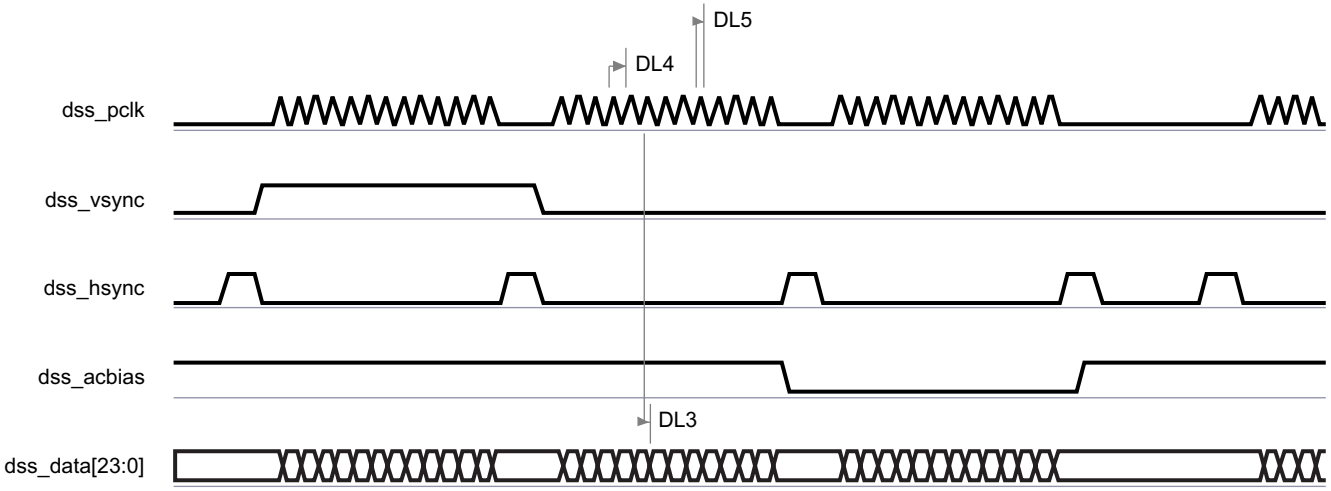
表 5-73. DSS Switching Characteristics—STN Mode(1)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DL3 | $t_{d(pclkA-dV)}$ | Delay time, output pixel clock dss_pclk active edge to output data dss_data[7:0] valid | -6 | 6 | -6 | 6 | ns |
| DL4 | 1 / $t_{c(pclk)}$ | Frequency(2), output pixel clock dss_pclk | | 45 | | 45 | MHz |
| DL5 | $t_{w(pclk)}$ | Pulse duration, output pixel clock dss_pclk low or high | 0.45P(3) | 0.55P(3)(4) | 0.45P(3) | 0.55P(3)(4) | ns |

(1) The DSS in STN mode is used with 4 or 8 pins only; unused pixel data bits always remain low.
(2) The pixel clock frequency is software programmable via the pixel clock divider DISPC_DIVISOR register.
(3) P = dss_pclk period in ns
(4) $t_{W(pclk)}$ = 0.66P when DISPC_DIVISOR[7:0] PCD = 3

表 5-73. DSS Switching Characteristics—STN Mode[1] (continued)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| | $t_{J(pclk)}$ | Peak-peak jitter, output pixel clock dss_pclk | | 200 | | 200 | ps |




A. The pixel data bus depends on the use of 4-, 8-, 12-, 16-, 18-, or 24-bit per pixel data output pins.
B. All timings not illustrated in the waveform are progammable by software, and control signal polarity and driven edge of dss_pclk too.
C. dss_vsync width must be programmed to be as small as possible.
D. The pixel clock frequency is programmable.
E. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

**図 5-94. DSS—STN Mode**

### *5.12.9.1.2 DSS—Parallel Interface—RFBI Mode—Applications*

#### *5.12.9.1.2.1 DSS—Parallel Interface—RFBI Mode—MIPI DBI 2.0—LCD Panel*

The Remote Frame Buffer Interface (RFBI) module provides the necessary control signals and data (MIPI® DBI 2.0 type B protocol) to interface to the LCD driver of the LCD panel.

表 5-75 and 表 5-76 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-95, 図 5-96, and 図 5-97).

表 5-74. DSS Timing Conditions—RFBI Mode—MIPI DBI 2.0—LCD Panel[1]

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Input Conditions** | | | | |
| $t_R$ | Input signal rise time | | 7 | ns |
| $t_F$ | Input signal fall time | | 7 | ns |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance | | 30 | pF |

(1) For any information regarding the RFBI registers configuration, see the Display Subsystem / Display Subsystem Environment / LCD Support / Parallel Interface / Parallel Interface in RFBI Mode (MIPI DBI Protocol) / Transaction Timing Diagrams section of the *AM437x Sitara Processors Technical Reference Manual*.

### 表 5-75. DSS Timing Requirements—RFBI Mode—MIPI DBI 2.0—LCD Panel

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| DR0 | $t_{su(dV-rdH)}$ | Setup time, input data rfbi_da[15:0] valid to output read enable rfbi_rd high | 7 | | 7 | | ns |
| DR1 | $t_{h(rdH-dIV)}$ | Hold time, output read enable rfbi_rd high to input data rfbi_da[15:0] invalid | 5 | | 5 | | ns |
| | $t_{d(Data\ sampled)}$ | Input data rfbi_da[15:0] sampled at the end of the access time | N(1) | | N(1) | | ns |

(1) N = (AccessTime) × (TimeParaGranularity + 1) × L4CLK

### 表 5-76. DSS Switching Characteristics—RFBI Mode—MIPI DBI 2.0—LCD Panel

| PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{w(wrH)}$ | Pulse duration, output write enable rfbi_wr high | A(1) | | A(1) | | ns |
| $t_{w(wrL)}$ | Pulse duration, output write enable rfbi_wr low | B(2) | | B(2) | | ns |
| $t_{d(a0-wrL)}$ | Delay time, output command/data control rfbi_a0 transition to output write enable rfbi_wr low | C(3) | | C(3) | | ns |
| $t_{d(wrH-a0)}$ | Delay time, output write enable rfbi_wr high to output command/data control rfbi_a0 transition | D(4) | | D(4) | | ns |
| $t_{d(csx-wrL)}$ | Delay time, output chip select rfbi_csx(14) low to output write enable rfbi_wr low | E(5) | | E(5) | | ns |
| $t_{d(wrH-csxH)}$ | Delay time, output write enable rfbi_wr high to output chip select rfbi_csx(14) high | F(6) | | F(6) | | ns |
| $t_{d(dV)}$ | Output data rfbi_da[15:0] valid | G(7) | | G(7) | | ns |
| $t_{d(a0H-rdL)}$ | Delay time, output command/data control rfbi_a0 high to output read enable rfbi_rd low | H(8) | | H(8) | | ns |
| $t_{d(rdlH-a0)}$ | Delay time, output read enable rfbi_rd high to output command/data control rfbi_a0 transition | I(9) | | I(9) | | ns |
| $t_{w(rdH)}$ | Pulse duration, output read enable rfbi_rd high | J(10) | | J(10) | | ns |
| $t_{w(rdL)}$ | Pulse duration, output read enable rfbi_rd low | K(11) | | K(11) | | ns |
| $t_{d(rdL-csxL)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx(14) low | L(12) | | L(12) | | ns |
| $t_{d(rdH-csxH)}$ | Delay time, output read enable rfbi_rd high to output chip select rfbi_csx(14) high | M(13) | | M(13) | | ns |

(1) A = (WECycleTime – WEOffTime) × (TimeParaGranularity + 1) × L4CLK

(2) B = (WEOffTime – WEOntime) × (TimeParaGranularity + 1) × L4CLK

(3) C = WEOnTime × (TimeParaGranularity + 1) × L4CLK

(4) D = (WECycleTime + CSPulseWidth – WEOffTime) × (TimeParaGranularity + 1) × L4CLK if mode Write to Read or Read to Write is enabled

(5) E = (WEOnTime – CSOnTime) × (TimeParaGranularity + 1) × L4CLK

(6) F = (CSOffTime – WEOffTime) × (TimeParaGranularity + 1) × L4CLK

(7) G = WECycleTime × (TimeParaGranularity + 1) × L4CLK

(8) H = REOnTime × (TimeParaGranularity + 1) × L4CLK

(9) I = (RECycleTime + CSPulseWidth – REOffTime) × (TimeParaGranularity + 1) × L4CLK if mode Write to Read or Read to Write is enabled

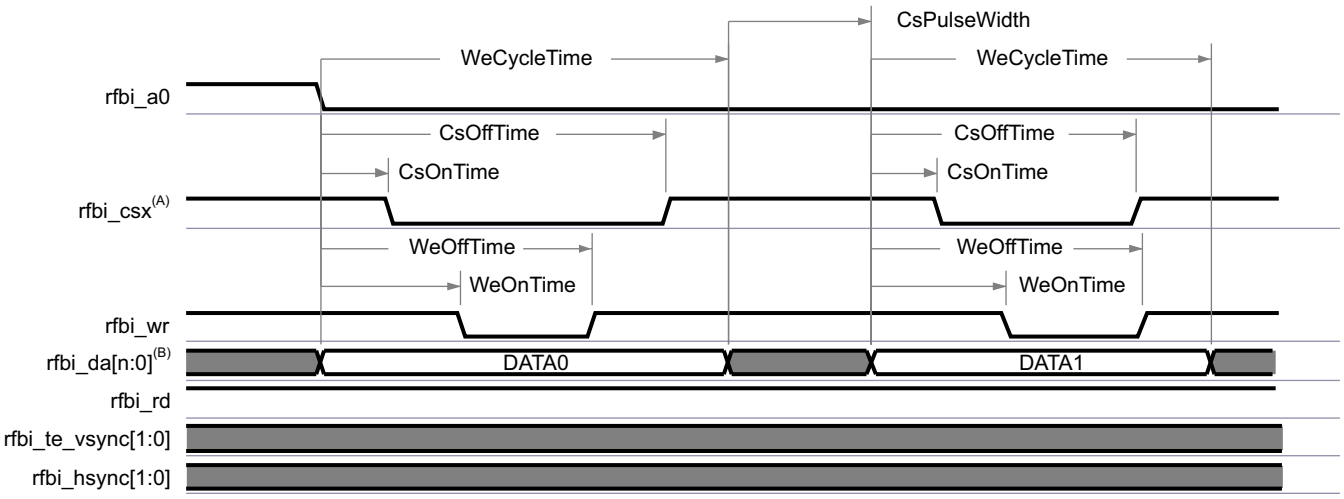
(10) J = (RECycleTime – REOffTime) × (TimeParaGranularity + 1) × L4CLK

(11) K = (REOffTime – REOntime) × (TimeParaGranularity + 1) × L4CLK

(12) L = (REOnTime – CSOnTime) × (TimeParaGranularity + 1) × L4CLK

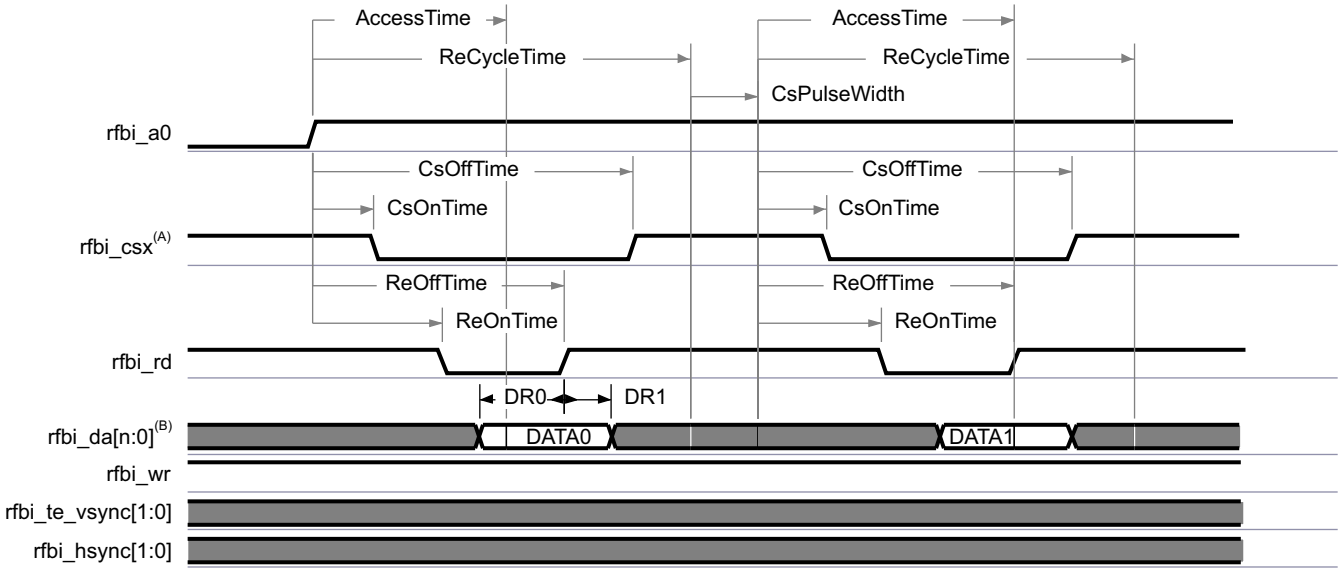
(13) M = (CSOffTime – REOffTime) × (TimeParaGranularity + 1) × L4CLK

(14) In rfbi_csx, x is equal to 0 or 1.



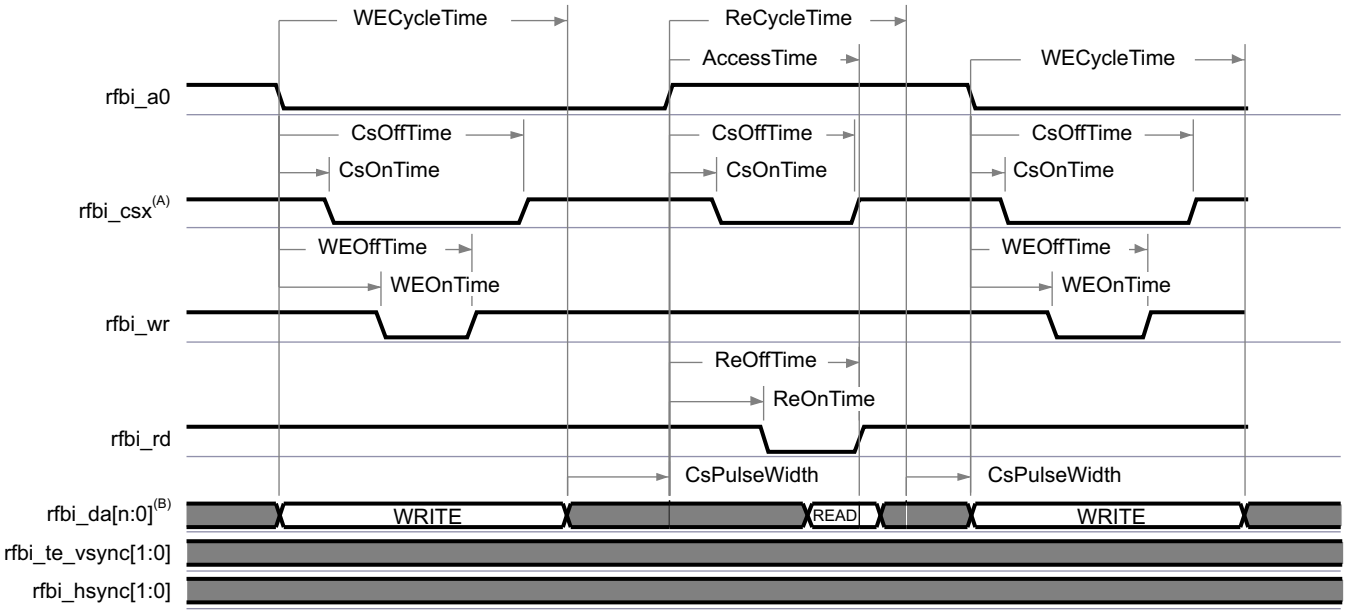

A. In rfbi_csx, x is equal to 0 or 1.
B. rfbi_da[n:0], n up to 15
C. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

**図 5-95. DSS—RFBI Mode—MIPI DBI 2.0—LCD Panel—Command / Data Write**




A. In rfbi_csx, x is equal to 0 or 1.
B. rfbi_da[n:0], n up to 15
C. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

**図 5-96. DSS—RFBI Mode—MIPI DBI 2.0—LCD Panel—Command / Data Read**




A. In rfbi_csx, x is equal to 0 or 1.
B. rfbi_da[n:0], n up to 15
C. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

**図 5-97. DSS—RFBI Mode—MIPI DBI 2.0—LCD Panel—Command / Data Write to Read and Read to Write Modes**

#### *5.12.9.1.2.2 DSS—Parallel Interface—RFBI Mode—Pico DLP*

The Remote Frame Buffer Interface (RFBI) module can provide also the necessary control signals and data to interface to the Pico DLP driver of the Pico DLP panel. 表 5-77 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see 図 5-98).

**表 5-77. DSS Timing Conditions—RFBI Mode—Pico DLP**

| TIMING CONDITION PARAMETER | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| **Output Condition** | | | | |
| $C_{LOAD}$ | Output load capacitance | | 5 | pF |

To use Pico DLP application, RFBI register must be configured as shown in 表 5-78:

**表 5-78. DSS Register Configuration—RFBI Mode—Pico DLP**

| DESCRIPTION | REGISTER AND BIT FIELD(1) | BIT | VALUES |
|---|---|---|---|
| Selection parallel mode | RFBI_CONFIGi and ParallelMode | [1:0] | 0b11: 16-bit parallel output interface selected |
| Time Granularity (multiplies signal timing latencies by 2). | RFBI_CONFIGi andTimeGranularity | [4] | 0b0: x2 latency disable |
| CS signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and CSOnTime | [3:0] | 0b0000 |
| CS signal deassertion time from Start Access Time | RFBI_ONOFF_TIMEi and CSOffTime | [9:4] | 0b000100: 4 cycles |
| WE signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and WEOnTime | [13:10] | 0b0000 |
| WE signal deassertion time from Start Access Time | RFBI_ONOFF_TIMEi and WEOffTime | [19:14] | 0b000010: 2 cycles |
| RE signal assertion time from Start Access Time | RFBI_ONOFF_TIMEi and REOnTime | [23:20] | 0b0000 |

表 5-78. DSS Register Configuration—RFBI Mode—Pico DLP (continued)

| DESCRIPTION | REGISTER AND BIT FIELD(1) | BIT | VALUES |
|---|---|---|---|
| RE signal deassertion time from Start Access Time | RFBI_ONOFF_TIMEi and REOffTime | [29:24] | 0b0000 |
| Write cycle time | RFBI_CYCLE_TIMEi and WECycleTime | [5:0] | 0b000100: 4 cycles |
| Read cycle time | RFBI_CYCLE_TIMEi and ReCycleTime | [11:6] | 0b000000 |
| CS pulse width | RFBI_CYCLE_TIMEi and CSPulseWidth | [17:12] | 0b000000 |
| Read to Write CS pulse width enable | RFBI_CYCLE_TIMEi and RWEnable | [18] | 0b0 |
| Read to Read CS pulse width enable | RFBI_CYCLE_TIMEi and RREnable | [19] | 0b0 |
| Write to Write CS pulse width enable | RFBI_CYCLE_TIMEi and WWEnable | [20] | 0b0 |
| Write to Read CS pulse width enable | RFBI_CYCLE_TIMEi and WREnable | [21] | 0b0 |
| From Start Access Time to CLK rising edge used for the first data capture | RFBI_CYCLE_TIMEi and AccessTime | [27:22] | 0b000000 |

(1) i is equal to 0 or 1. For more information, see the DSS chapter in the *AM437x Sitara Processors Technical Reference Manual*.

### 表 5-79. DSS Switching Characteristics—RFBI Mode—Pico DLP[1][2][3]

| PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{w(wrH)}$ | Pulse duration, output write enable rfbi_wr high | A[4] | | A[4] | | ns |
| $t_{w(wrL)}$ | Pulse duration, output write enable rfbi_wr low | B[5] | | B[5] | | ns |
| $t_{d(a0\text{-}wrL)}$ | Delay time, output command/data control rfbi_a0 transition to output write enable rfbi_wr low | C[6] | | C[6] | | ns |
| $t_{d(wrH\text{-}a0)}$ | Delay time, output write enable rfbi_wr high to output command/data control rfbi_a0 transition | D[7] | | D[7] | | ns |
| $t_{d(csx\text{-}wrL)}$ | Delay time, output chip select rfbi_csx[8] low to output write enable rfbi_wr low | E[9] | | E[9] | | ns |
| $t_{d(wrH\text{-}csxH)}$ | Delay time, output write enable rfbi_wr high to output chip select rfbi_csx[8] high | F[10] | | F[10] | | ns |
| $t_{d(dataV)}$ | Output data rfbi_da[15:0][11] valid | G[12] | | G[12] | | ns |
| $t_{d(Skew)}$ | Skew between output write enable falling rfbi_wr and output data rfbi_da[15:0][11] high or low | 15.5 | | 15.5 | | ns |
| $t_{d(a0H\text{-}rdL)}$ | Delay time, output command/data control rfbi_a0 high to output read enable rfbi_rd low | H[13] | | H[13] | | ns |
| $t_{d(rdlH\text{-}a0)}$ | Delay time, output read enable rfbi_rd high to output command/data control rfbi_a0 transition | I[14] | | I[14] | | ns |
| $t_{w(rdH)}$ | Pulse duration, output read enable rfbi_rd high | J[15] | | J[15] | | ns |
| $t_{w(rdL)}$ | Pulse duration, output read enable rfbi_rd low | K[16] | | K[16] | | ns |
| $t_{d(rdL\text{-}csxL)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx[8] low | L[17] | | L[17] | | ns |
| $t_{d(rdL\text{-}csxH)}$ | Delay time, output read enable rfbi_rd low to output chip select rfbi_csx[8] high | M[18] | | M[18] | | ns |
| CsOnTime | CS signal assertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | 0[19] | | | | ns |
| CsOffTime | CS signal deassertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | 40[19] | | | | ns |
| WeOnTime | WE signal assertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | 0[19] | | | | ns |
| WeOffTime | WE signal deassertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | 20[19] | | | | ns |
| ReOnTime | RE signal assertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | - | | | | ns |
| ReOffTime | RE signal deassertion time from Start Access Time – RFBI_ONOFF_TIMEi Register | - | | | | ns |
| WeCycleTime | Write cycle time – RFBI_CYCLE_TIMEi Register | 40[19] | | | | ns |
| ReCycleTime | Read cycle time – RFBI_CYCLE_TIMEi Register | - | | | | ns |
| CsPulseWidth | CS pulse width – RFBI_CYCLE_TIMEi Register | 0[19] | | | | ns |

(1) See DM Operating Condition Addendum for OPP voltages.

(2) At OPP100, L4 clock is 100 MHz and at OPP50, L4 clock is 50 MHz.

(3) rfbi_wr must be at 25 MHz.

(4) A = (WECycleTime – WEOffTime) × (TimeParaGranularity + 1) × L4CLK

(5) B = (WEOffTime – WEOntime) × (TimeParaGranularity + 1) × L4CLK

(6) C = WEOnTime × (TimeParaGranularity + 1) × L4CLK

(7) D = (WECycleTime + CSPulseWidth – WEOffTime) × (TimeParaGranularity + 1) × L4CLK if mode Write to Read or Read to Write is enabled.

(8) In rfbi_csx, x is equal to 0 or 1.

(9) E = (WEOnTime – CSOnTime) × (TimeParaGranularity + 1) × L4CLK

(10) F = (CSOffTime – WEOffTime) × (TimeParaGranularity + 1) × L4CLK

(11) 16-bit parallel output interface is selected in DSS register.

(12) G = WECycleTime × (TimeParaGranularity + 1) × L4CLK

(13) H = REOnTime × (TimeParaGranularity + 1) × L4CLK

(14) I = (RECycleTime + CSPulseWidth – REOffTime) × (TimeParaGranularity + 1) × L4CLK if mode Write to Read or Read to Write is enabled.

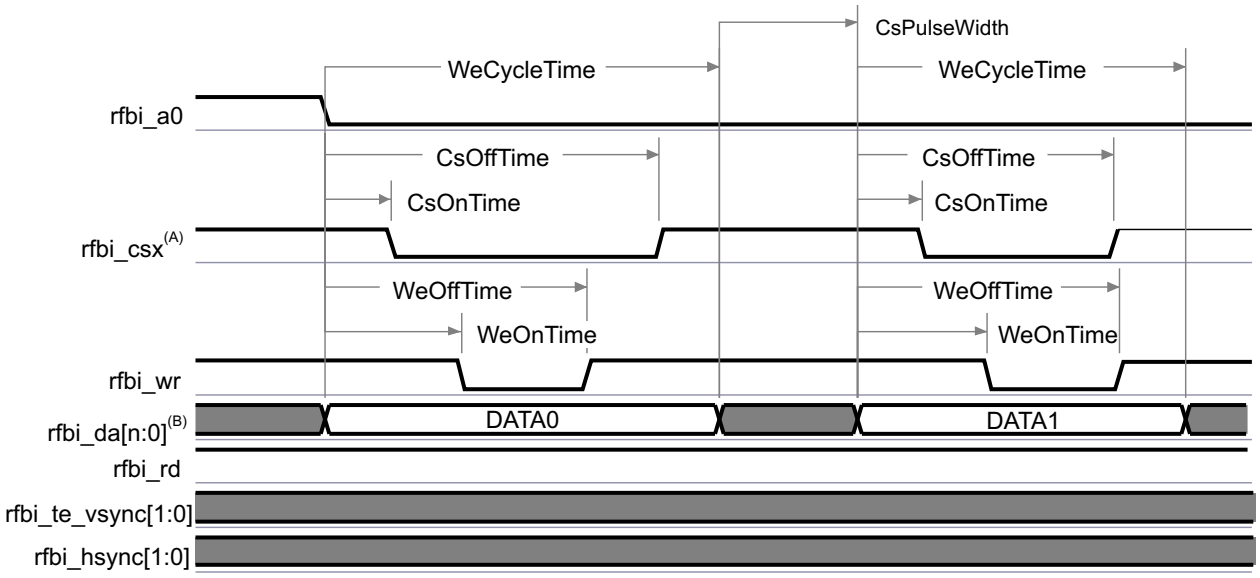
(15) J = (RECycleTime – REOffTime) × (TimeParaGranularity + 1) × L4CLK

(16) K = (REOffTime – REOntime) × (TimeParaGranularity + 1) × L4CLK

(17) L = (REOnTime – CSOnTime) × (TimeParaGranularity + 1) × L4CLK

(18) M = (CSOffTime – REOffTime) × (TimeParaGranularity + 1) × L4CLK

(19) These values are calculated by the following formula: RFBI Register (Value) × L4 Clock (ns).




A. In rfbi_csx, x is equal to 0 or 1.
B. rfbi_da[n:0], n up to 15

**図 5-98. DSS—RFBI Mode—Pico DLP—Command / Data Write**

### *5.12.10 Camera (VPFE)*

The camera (VPFE) controller receives input video/image data from external capture devices and stores it to external memory which is transferred into the external memory via a built-in DMA engine. An internal buffer block provides a high bandwidth path between the module and the external memory. The Cortex-A9 will process the image data based on application requirements.

#### 5.12.10.1 Camera (VPFE) Timing

The following tables assume testing over recommended operating conditions.

**表 5-80. VPFE Timing Requirements**

| NO. | | | 1.8 V, 3.3 V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | OPP50 | | OPP100 | | |
| | | | MIN | MAX | MIN | MAX | |
| VF1 | $t_{c(CAMx\_CLK)}$ | Cycle time, pixel clock input, CAMx_CLK | 20 | | 13.3 | | ns |
| VF2 | $t_{su(CAMx\_D\text{-}CAMx\_CLK)}$ | Setup time, CAMx_D to CAMx_CLK rising edge | 7.5 | | 3.5 | | ns |
| VF3 | $t_{su(CAMx\_HD\text{-}CAMx\_CLK)}$ | Setup time, CAMx_HD to CAMx_CLK rising edge | 7.5 | | 3.5 | | ns |
| VF4 | $t_{su(CAMx\_VD\text{-}CAMx\_CLK)}$ | Setup time, CAMx_VD to CAMx_CLK rising edge | 7.5 | | 3.5 | | ns |
| VF5 | $t_{su(CAMx\_WEN\text{-}CAMx\_CLK)}$ | Setup time, CAMx_WEN to CAMx_CLK rising edge | 7.5 | | 3.5 | | ns |
| VF6 | $t_{su(C\_FLD\text{-}CAMx\_CLK)}$ | Setup time, CAMx_FIELD to CAMx_CLK rising edge | 7.5 | | 3.5 | | ns |

表 5-80. VPFE Timing Requirements (continued)

| NO. | | | 1.8 V, 3.3 V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | OPP50 | | OPP100 | | |
| | | | MIN | MAX | MIN | MAX | |
| VF7 | $t_{h(CAMx\_CLK-CAMx\_D)}$ | Hold time, CAMx_D valid after CAMx_CLK rising edge | 6.5 | | 2.5 | | ns |
| VF8 | $t_{h(VDIN-HD-CAMx\_CLK)}$ | Hold time, CAMx_HD to CAMx_CLK rising edge | 6.5 | | 2.5 | | ns |
| VF9 | $t_{h(CAMx\_VD-CAMx\_CLK)}$ | Hold time, CAMx_VD to CAMx_CLK rising edge | 6.5 | | 2.5 | | ns |
| VF10 | $t_{h(CAMx\_WEN-CAMx\_CLK)}$ | Hold time, CAMx_WEN to CAMx_CLK rising edge | 6.5 | | 2.5 | | ns |
| VF11 | $t_{h(C\_FLD-CAMx\_CLK)}$ | Hold time, CAMx_FIELD to CAMx_CLK rising edge | 6.5 | | 2.5 | | ns |

表 5-81. VPFE Output Switching Characteristics

| NO. | PARAMETER | | 1.8 V, 3.3 V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | OPP50 | | OPP100 | | |
| | | | MIN | MAX | MIN | MAX | |
| VF12 | $t_{d(CAMx\_HD-CAMx\_CLK)}$ | Output delay time, CAMx_HD to CLK rising edge | 9 | 15 | 2 | 9 | ns |
| VF13 | $t_{d(CAMx\_VD-CAMx\_CLK)}$ | Output delay time, CAMx_VD to CLK rising edge | 9 | 15 | 2 | 9 | ns |
| VF14 | $t_{d(CAMx\_WEN-CAMx\_CLK)}$ | Output delay time, CAMx_WEN to CLK rising edge | 9 | 15 | 2 | 9 | ns |

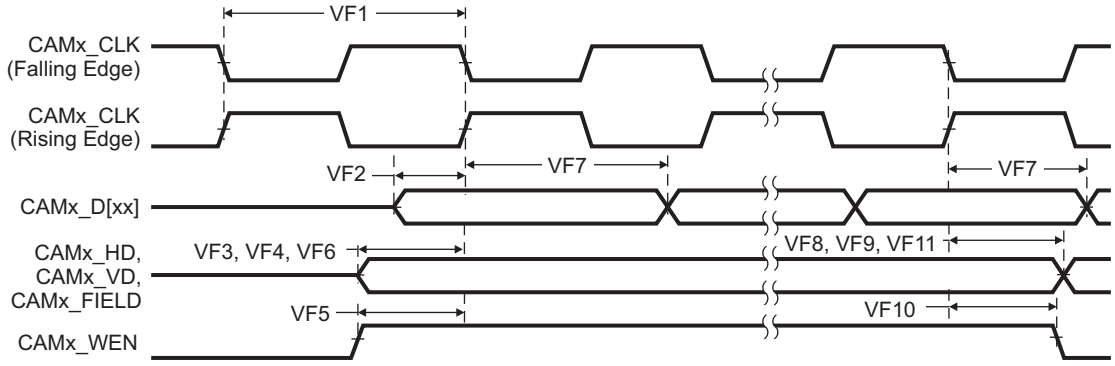



図 5-99. Camera Input Timings

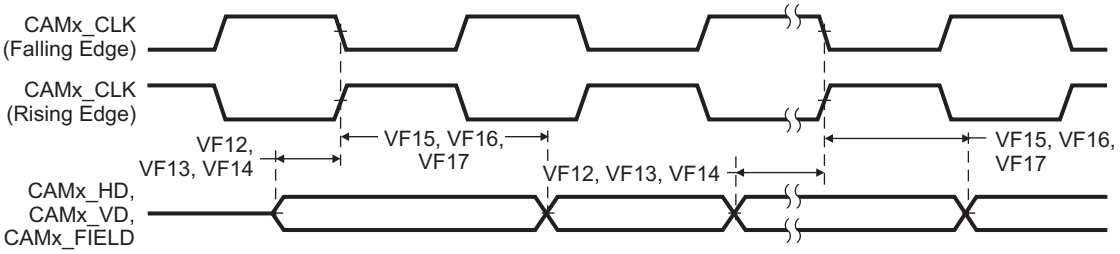



図 5-100. Camera Output Timings

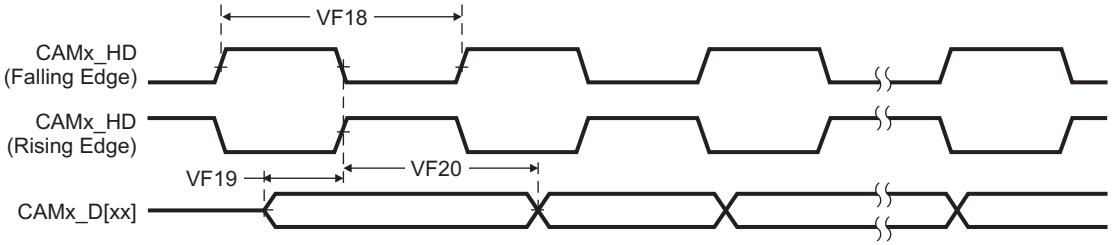



**図 5-101. Camera Input Timings With VDIN0_HD as Pixel Clock**

### 5.12.11 Inter-Integrated Circuit ($I^2C$)

For more information, see the Inter-Integrated Circuit ($I^2C$) section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

#### 5.12.11.1 I2C Electrical Data and Timing

**表 5-82. I2C Timing Conditions - Slave Mode**

| TIMING CONDITION PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| **Output Condition** | | | | | | |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

**表 5-83. Timing Requirements for I2C Input Timings**

(see 図 5-102)

| NO. | | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | us |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup Time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | us |
| 3 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | us |
| 4 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | us |
| 5 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | us |
| 6 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100(1) | | ns |
| 7 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0(2) | 3.45(3) | 0(2) | 0.9(3) | us |
| 8 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | us |
| 9 | $t_{r(SDA)}$ | Rise time, SDA | | 1000 | | 300 | ns |
| 10 | $t_{r(SCL)}$ | Rise time, SCL | | 1000 | | 300 | ns |
| 11 | $t_{f(SDA)}$ | Fall time, SDA | | 300 | | 300 | ns |
| 12 | $t_{f(SCL)}$ | Fall time, SCL | | 300 | | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, high before SDA high (for STOP condition) | 4 | | 0.6 | | us |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | 0 | 50 | 0 | 50 | ns |

(1) A fast-mode I2C-bus™ device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the standard-mode I2C-Bus Specification) before the SCL line is released.

(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

(3) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

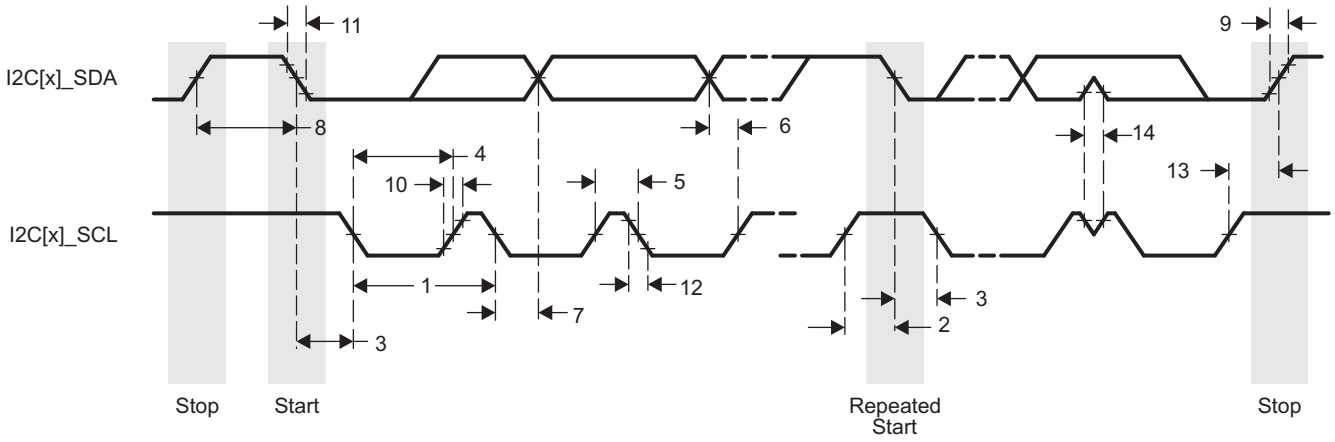



**図 5-102. I2C Receive Timing**

**表 5-84. Switching Characteristics for I2C Output Timings**

(see 図 5-103)

| NO. | PARAMETER | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 15 | $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | us |
| 16 | $t_{su(SCLH-SDAL)}$ | Setup Time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | us |
| 17 | $t_{h(SDAL-SCLL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | us |
| 18 | $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | us |
| 19 | $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | us |
| 20 | $t_{su(SDAV-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| 21 | $t_{h(SCLL-SDAV)}$ | Hold time, SDA valid after SCL low | 0 | 3.45 | 0 | 0.9 | us |
| 22 | $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | us |
| 27 | $t_{su(SCLH-SDAH)}$ | Setup time, high before SDA high (for STOP condition) | 4 | | 0.6 | | us |

(1) Cb is line load in pF.

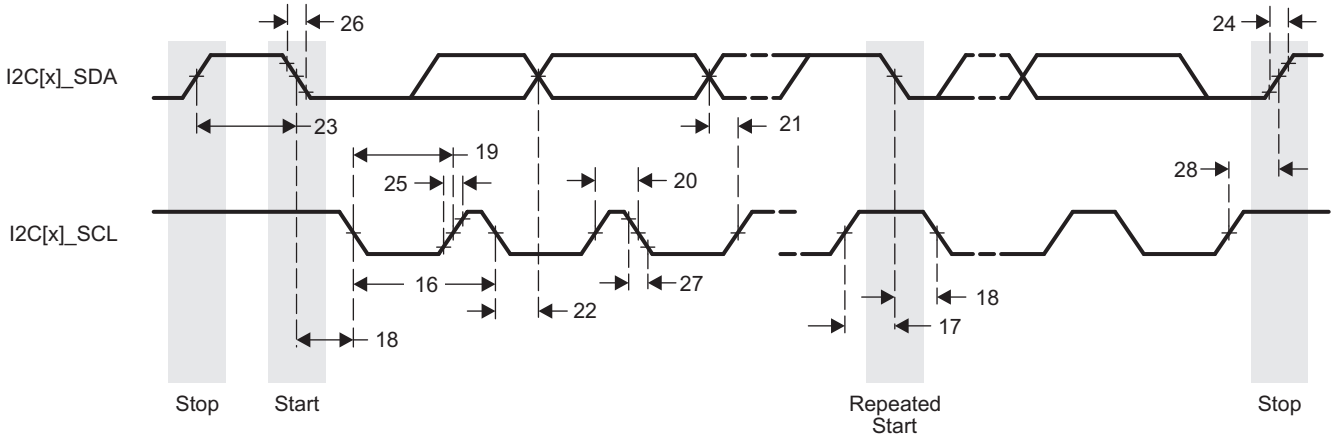



**図 5-103. I2C Transmit Timing**

### 5.12.12 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

#### 5.12.12.1 McASP Device-Specific Information

The device includes two multichannel audio serial port (McASP) interface peripherals (McASP0 and McASP1). The McASP module consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or, alternatively, the transmit and receive sections may be synchronized. The McASP module also includes shift registers that may be configured to operate as either transmit data or receive data.

The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a DIT format where the bit stream is encoded for SPDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP peripheral supports the TDM synchronous serial format.

The McASP module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format; however, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode, which is useful for nonaudio data (for example, passing control information between two devices).

The McASP peripheral has additional capability for flexible clock generation and error detection/handling, as well as error management.

The device McASP0 and McASP1 modules have up to four serial data pins each. The McASP FIFO size is 256 bytes and two DMA and two interrupt requests are supported. Buffers are used transparently to better manage DMA, which can be leveraged to manage data flow more efficiently.

For more detailed information on and the functionality of the McASP peripheral, see the Multichannel Audio Serial Port (McASP) section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

### 5.12.12.2 McASP Electrical Data and Timing

**表 5-85. McASP Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_R$ | Input signal rise time | 1(1) | | 4(1) | ns |
| $t_F$ | Input signal fall time | 1(1) | | 4(1) | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | 15 | | 30 | pF |

(1) Except when specified otherwise.

**表 5-86. Timing Requirements for McASP(1)**

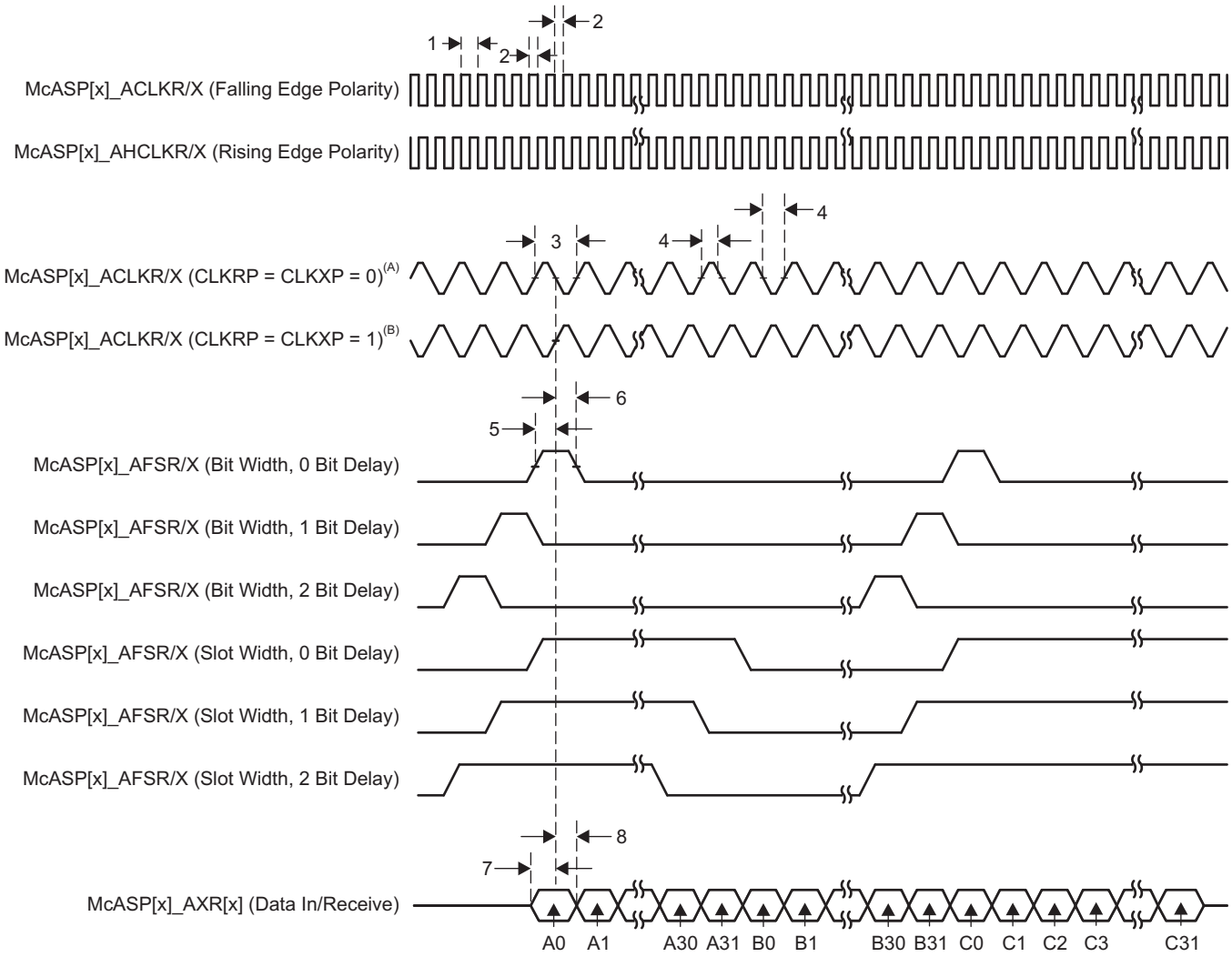
(see 図 5-104)

| NO. | | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX | | 20 | | 38.46 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low | | 0.5P - 2.5(2) | | 0.5P - 2.5(2) | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX | | 20 | | 38.46 | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low | | 0.5R - 2.5(3) | | 0.5R - 2.5(3) | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, McASP[x]_AFSR and McASP[x]_AFSX input valid before McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | 12.3 | | 15.5 | | ns |
| | | | ACLKR and ACLKX ext in | 4 | | 6 | | |
| | | | ACLKR and ACLKX ext out | 4 | | 6 | | |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, McASP[x]_AFSR and McASP[x]_AFSX input valid after McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | -1 | | -1 | | ns |
| | | | ACLKR and ACLKX ext in | 1.6 | | 2.3 | | |
| | | | ACLKR and ACLKX ext out | 1.6 | | 2.3 | | |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, McASP[x]_AXR input valid before McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | 12.3 | | 15.5 | | ns |
| | | | ACLKR and ACLKX ext in | 4 | | 6 | | |
| | | | ACLKR and ACLKX ext out | 4 | | 6 | | |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, McASP[x]_AXR input valid after McASP[x]_ACLKR and McASP[x]_ACLKX | ACLKR and ACLKX int | -1 | | -1 | | ns |
| | | | ACLKR and ACLKX ext in | 1.6 | | 2.3 | | |
| | | | ACLKR and ACLKX ext out | 1.6 | | 2.3 | | |

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) P = McASP[x]_AHCLKR and McASP[x]_AHCLKX period in nano seconds (ns).

(3) R = McASP[x]_ACLKR and McASP[x]_ACLKX period in ns.




A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**図 5-104. McASP Input Timing**

### 表 5-87. Switching Characteristics for McASP[1]

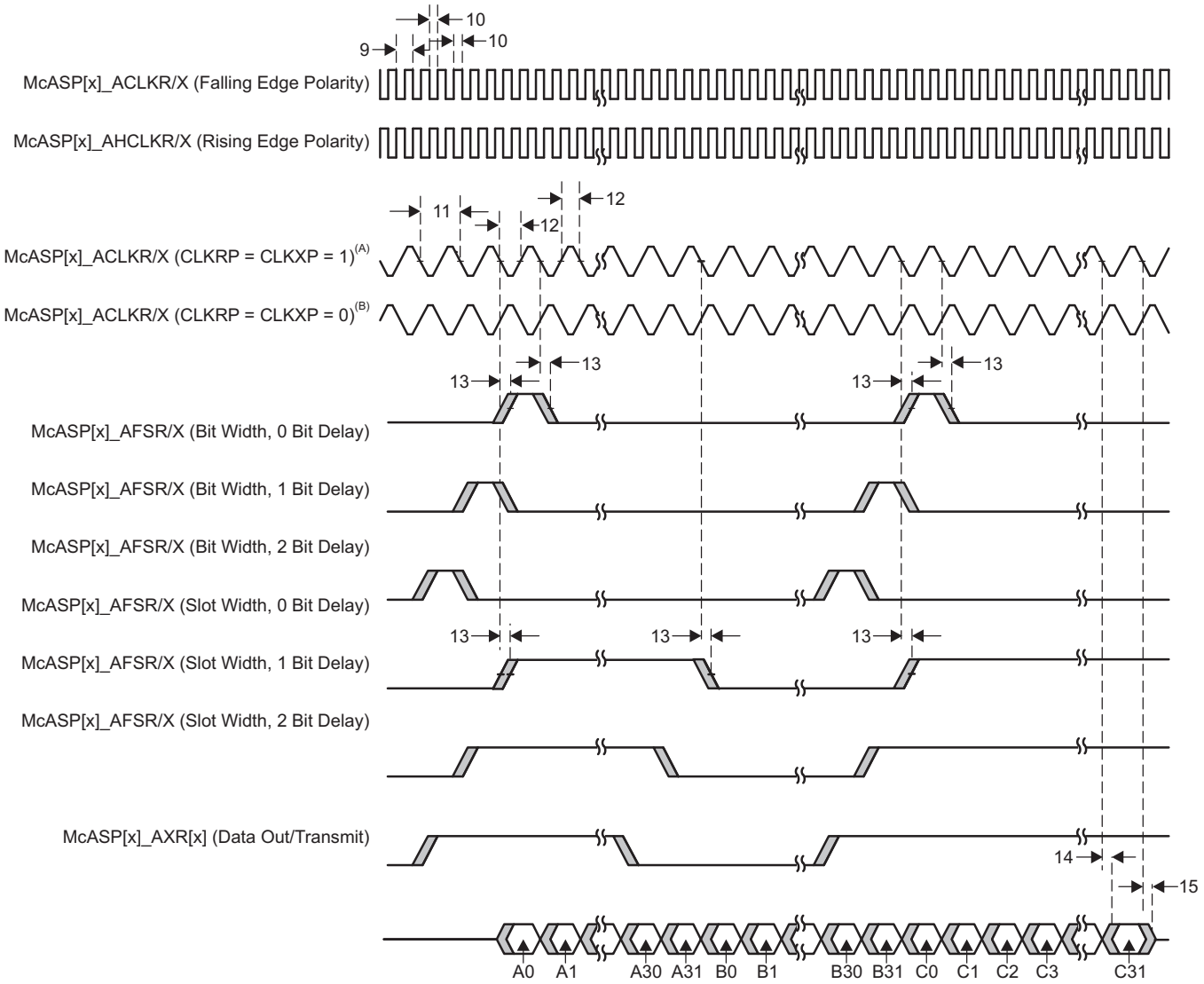
(see 図 5-105)

| NO. | | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, McASP[x]_AHCLKR and McASP[x]_AHCLKX | | 20[2] | | 38.46 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, McASP[x]_AHCLKR and McASP[x]_AHCLKX high or low | | 0.5P - 2.5[3] | | 0.5P - 2.5[3] | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, McASP[x]_ACLKR and McASP[x]_ACLKX | | 20 | | 38.46 | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, McASP[x]_ACLKR and McASP[x]_ACLKX high or low | | 0.5P - 2.5[3] | | 0.5P - 2.5[3] | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid | ACLKR and ACLKX int | 0 | 7.25 | 0 | 8.5 | ns |
| | | | ACLKR and ACLKX ext in | 2 | 14 | 2.7 | 18 | |
| | | Delay time, McASP[x]_ACLKR and McASP[x]_ACLKX transmit edge to McASP[x]_AFSR and McASP[x]_AFSX output valid with Pad Loopback | ACLKR and ACLKX ext out | 2 | 14 | 2.7 | 18 | |
| 14 | $t_{d(ACLKX-AXR)}$ | Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid | ACLKX int | 0 | 7.25 | 0 | 8.5 | ns |
| | | | ACLKX ext in | 2 | 14 | 2.7 | 18 | |
| | | Delay time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output valid with Pad Loopback | ACLKX ext out | 2 | 14 | 2.7 | 18 | |
| 15 | $t_{dis(ACLKX-AXR)}$ | Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance | ACLKX int | 0 | 7.25 | 0 | 8.5 | ns |
| | | | ACLKX ext in | 2 | 14 | 2.7 | 18 | |
| | | Disable time, McASP[x]_ACLKX transmit edge to McASP[x]_AXR output high impedance with Pad Loopback | ACLKX ext out | 2 | 14 | 2.7 | 18 | |

(1) ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1

(2) 50 MHz

(3) P = AHCLKR and AHCLKX period.




A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**図 5-105. McASP Output Timing**

### 5.12.13 Multichannel Serial Port Interface (McSPI)

For more information, see the Multichannel Serial Port Interface (McSPI) section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

#### 5.12.13.1 McSPI Electrical Data and Timing

The following timings are applicable to the different configurations of McSPI in master or slave mode for any McSPI and any channel (n).

##### 5.12.13.1.1 McSPI—Slave Mode

**表 5-88. McSPI Timing Conditions—Slave Mode**

| TIMING CONDITION PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **Input Conditions** | | | | |
| $t_r$ | Input signal rise time | | 5 | ns |
| $t_f$ | Input signal fall time | | 5 | ns |
| **Output Condition** | | | | |
| $C_{load}$ | Output load capacitance | | 20 | pF |

**表 5-89. Timing Requirements for McSPI Input Timings—Slave Mode**

(see 図 5-106)

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK | 62.5 | | 83.2 | | ns |
| 2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, SPI_CLK low | 0.45P(1) | 0.45P(1) | 0.45P(1) | 0.45P(1) | ns |
| 3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, SPI_CLK high | 0.45P(1) | 0.45P(1) | 0.45P(1) | 0.45P(1) | ns |
| 4 | $t_{su(SIMO-SPICLK)}$ | Setup time, SPI_D[x] (SIMO) valid before SPI_CLK active edge(2)(3) | 12 | | 13 | | ns |
| 5 | $t_{h(SPICLK-SIMO)}$ | Hold time, SPI_D[x] (SIMO) valid after SPI_CLK active edge(2)(3) | 12 | | 13 | | ns |
| 8 | $t_{su(CS-SPICLK)}$ | Setup time, SPI_CS valid before SPI_CLK first edge(2) | 12 | | 13 | | ns |
| 9 | $t_{h(SPICLK-CS)}$ | Hold time, SPI_CS valid after SPI_CLK last edge(2) | 12 | | 13 | | ns |

(1) P = SPI_CLK period.

(2) This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to drive output data and capture input data.

(3) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

**表 5-90. Switching Characteristics for McSPI Output Timings—Slave Mode**

(see 図 5-107)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 6 | $t_{d(SPICLK-SOMI)}$ | Delay time, SPI_CLK active edge to SPI_D[x] (SOMI) transition(1)(2) | | 17 | 0 | 19 | ns |
| 7 | $t_{d(CS-SOMI)}$ | Delay time, SPI_CS active edge to SPI_D[x] (SOMI) transition(2) | | 26 | | 29 | ns |

(1) This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to drive output data and capture input data.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

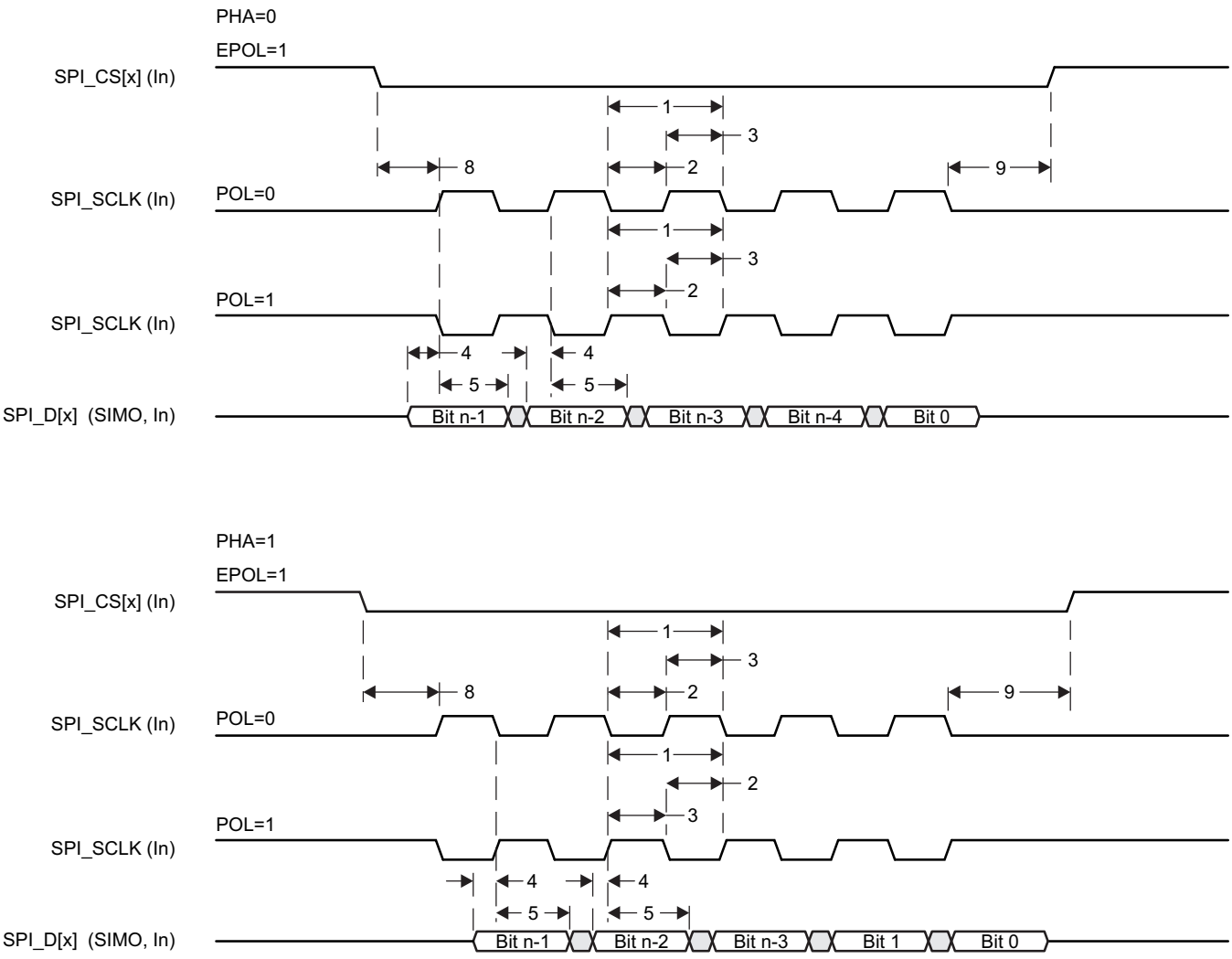



**図 5-106. SPI Slave Mode Receive Timing**

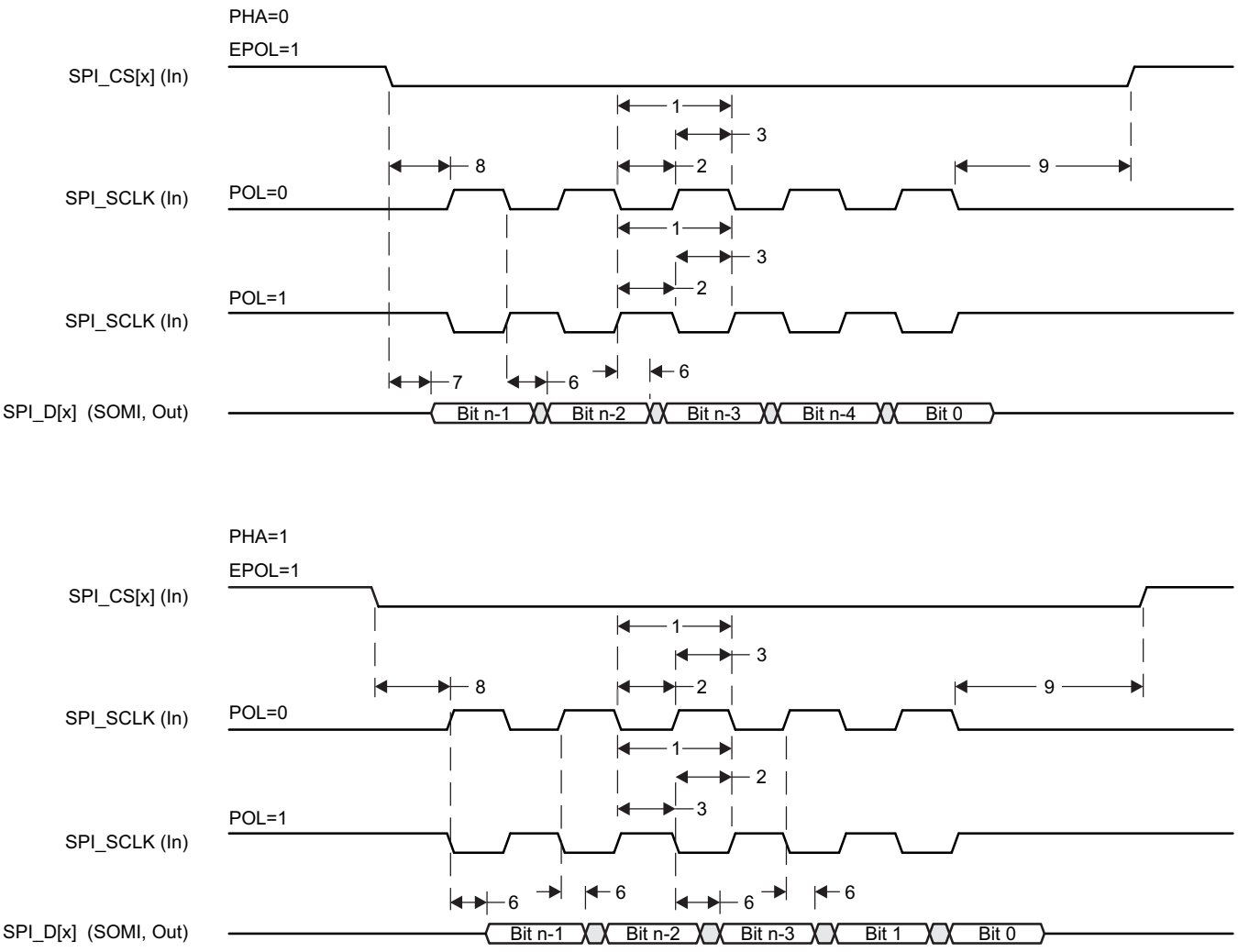



**図 5-107. SPI Slave Mode Transmit Timing**

#### 5.12.13.1.2 McSPI—Master Mode

**表 5-91. McSPI Timing Conditions—Master Mode**

| TIMING CONDITION PARAMETER | | LOW LOAD | | HIGH LOAD | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| **Input Conditions** | | | | | | |
| $t_r$ | Input signal rise time | | 4 | | 8 | ns |
| $t_f$ | Input signal fall time | | 4 | | 8 | ns |
| **Output Condition** | | | | | | |
| $C_{load}$ | Output load capacitance | | 5 | | 25 | pF |

**表 5-92. Timing Requirements for McSPI Input Timings—Master Mode**

(see 図 5-108)

| NO. | | | OPP100 | | | | OPP50 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | LOW LOAD | | HIGH LOAD | | LOW LOAD | | HIGH LOAD | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 4 | $t_{su(SOMI-SPICLK)}$[1] | Setup time, SPI_D[x] (SOMI) valid before SPI_CLK active edge[2] | 3 | | 4.5 | | 4.5 | | 4.5 | | ns |
| 5 | $t_{h(SPICLK-SOMI)}$[1] | Hold time, SPI_D[x] (SOMI) valid after SPI_CLK active edge[2] | 6 | | 6 | | 6 | | 6 | | ns |

(1) This timing applies to all configurations regardless of MCSPIX_CLK polarity and which clock edges are used to capture input data.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

**表 5-93. Switching Characteristics for McSPI Output Timings—Master Mode**

(see 図 5-109)

| NO. | PARAMETER | | | OPP100 | | | | OPP50 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | LOW LOAD | | HIGH LOAD | | LOW LOAD | | HIGH LOAD | | |
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPICLK)}$ | Cycle time, SPI_CLK | | 20.8 | | 41.6 | | 41.6 | | 41.6 | | ns |
| 2 | $t_{w(SPICLKL)}$ | Typical Pulse duration, SPI_CLK low | | 0.45P[1] | 0.45P[1] | 0.45P[1] | 0.55P[1] | 0.45P[1] | 0.45P[1] | 0.45P[1] | 0.45P[1] | ns |
| 3 | $t_{w(SPICLKH)}$ | Typical Pulse duration, SPI_CLK high | | 0.45P[1] | 0.45P[1] | 0.45P[1] | 0.55P[1] | 0.45P[1] | 0.45P[1] | 0.45P[1] | 0.45P[1] | ns |
| 6 | $t_{d(SPICLK-SIMO)}$ | Delay time, SPI_CLK active edge to SPI_D[x] (SIMO) transition[2] | | -1 | 4.5 | -1 | 6.5 | 0 | 6.5 | 0 | 6.5 | ns |
| 7 | $t_{d(CS-SIMO)}$ | Delay time, SPI_CS active edge to SPI_D[x] (SIMO) transition[2] | | | 4.5 | | 6.5 | | 6.5 | | 6.5 | ns |
| 8 | $t_{d(CS-SPICLK)}$ | Delay time, SPI_CS active to SPI_CLK first edge | Mode 1 and 3[3] | A - 4.2[4] | | A - 4.2[4] | | A - 5.2[4] | | A - 5.2[4] | | ns |
| | | | Mode 0 and 2[3] | B - 4.2[5] | | B - 4.2[5] | | B - 5.2[5] | | B - 5.2[5] | | ns |
| 9 | $t_{d(SPICLK-CS)}$ | Delay time, SPI_CLK last edge to SPI_CS inactive | Mode 1 and 3[3] | B - 4.2[5] | | B - 4.2[5] | | B - 5.2[5] | | B - 5.2[5] | | ns |
| | | | Mode 0 and 2[3] | A - 4.2[4] | | A - 4.2[4] | | A - 5.2[4] | | A - 5.2[4] | | ns |

(1) P = SPI_CLK period.

(2) Pins SPIx_D0 and SPIx_D1 can function as SIMO or SOMI.

(3) The polarity of SPIx_CLK and the active edge (rising or falling) on which mcspix_simo is driven and mcspix_somi is latched is all software configurable:
- SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 1 (Modes 1 and 3).
- SPIx_CLK(1) phase programmable with the bit PHA of MCSPI_CH(i)CONF register: PHA = 0 (Modes 0 and 2).

(4) Case P = 20.8 ns, A = (TCS+1)*TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).
Case P > 20.8 ns, A = (TCS+0.5)*Fratio*TSPICLKREF (TCS is a bit field of MCSPI_CH(i)CONF register).

Note: P = SPI_CLK clock period.

(5) B = (TCS+0.5)*TSPICLKREF*Fratio (TCS is a bit field of MCSPI_CH(i)CONF register, Fratio: Even≥2).

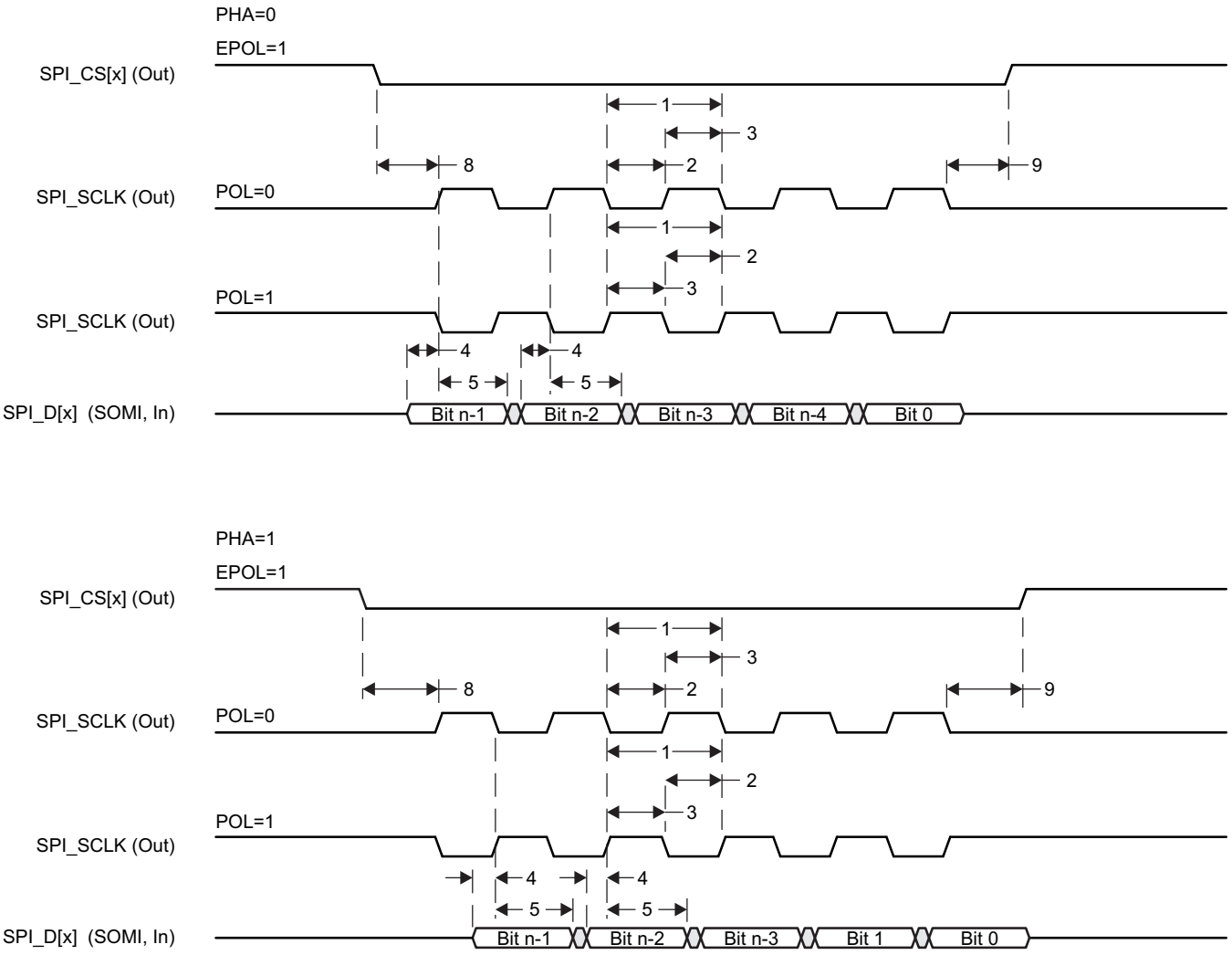



**図 5-108. SPI Master Mode Receive Timing**

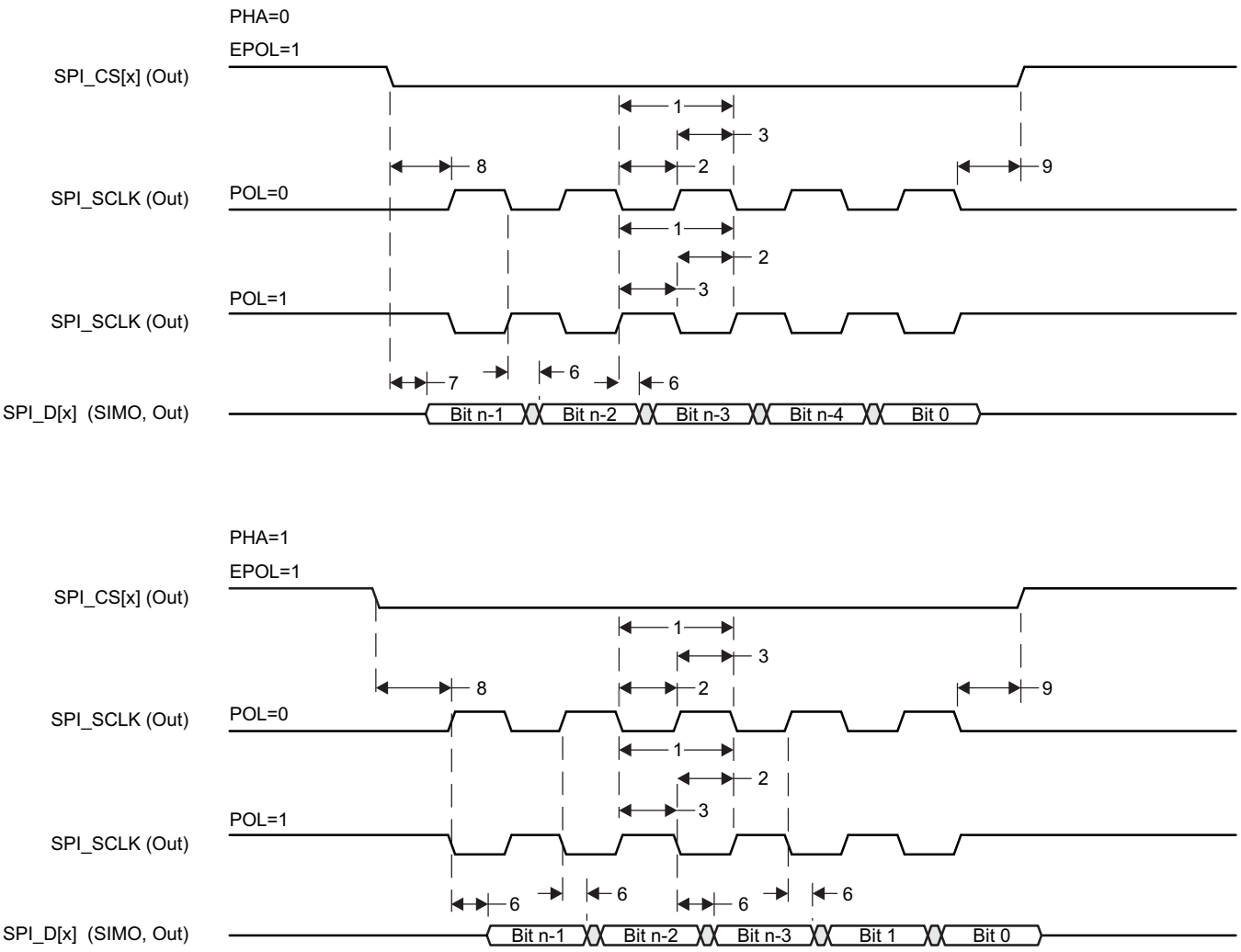



**図 5-109. SPI Master Mode Transmit Timing**

### 5.12.14 Quad Serial Port Interface (QSPI)

The Quad SPI (QSPI) module allows single, dual or quad read access to external SPI devices. This module provides a memory mapped register interface, which provides a direct interface to access data from external SPI devices and to simplify software requirements. It functions as a master only. There is one QSPI module in the device and it is primary intended for fast booting from quad-SPI flash memories.

General SPI features:

- Programmable clock divider
- Six pin interface (QSPI_CLK, QSPI_D0, QSPI_D1,QSPI_D2,QSPI_D3, QSPI_CS0)
- One external chip select signal
- Support for 3-, 4- or 6-pin SPI interface
- Programmable CS0 to DATA_OUT delay from 0 to 3 QSPI_CLKs
- Only supports SPI MODE 3

注

For more information, see the Quad Serial Port Interface section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

表 5-94 displays the switching characteristics for the Quad SPI module.

**表 5-94. QSPI Switching Characteristics**

(see 図 5-110 and 図 5-111)

| NO. | PARAMETER | | OPP100 | | OPP50 | | |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | UNIT |
| 1 | $t_{c(QSPI\_CLK)}$ | Cycle time, QSPI_CLK | 20.8(1) | | 20.8(1) | | ns |
| 2 | $t_{w(QSPI\_CLKL)}$ | Pulse duration, QSPI_CLK low | 9.77(1) | | 9.77(1) | | ns |
| 3 | $t_{w(QSPI\_CLKH)}$ | Pulse duration, QSPI_CLK high | 9.77(1) | | 9.77(1) | | ns |
| 4 | $t_{d(CS\text{-}QSPI\_CLK)}$ | Delay time, QSPI_CSn active edge to QSPI_CLK transition | M*P+5(2)(3) | | M*P+5(2)(3) | | ns |
| 5 | $t_{d(QSPI\_CLK\text{-}QSPI\_CSn)}$ | Delay time, QSPI_CLK transition to QSPI_CSn inactive edge | M*P+5(2)(3) | | M*P+5(2)(3) | | ns |
| 6 | $t_{d(QSPI\_CLK\text{-}D1)}$ | Delay time, QSPI_CLK active edge to QSPI_D[0] transition | 0 | 5.5 | 0 | 5.5 | ns |
| 7 | $t_{su(D\text{-}QSPI\_CLK)}$ | Setup time, QSPI_D[3:0] valid before active QSPI_CLK edge | 8.5 | | 8.5 | | ns |
| 8 | $t_{h(QSPI\_CLK\text{-}D)}$ | Hold time, QSPI_D[3:0] valid after active QSPI_CLK edge | 0 | | 0 | | ns |

(1) Maximum supported frequency is 48 MHz.
(2) P = QSPI_CLK period.
(3) M = Programmable via Data Delay Zero (DD0) register.

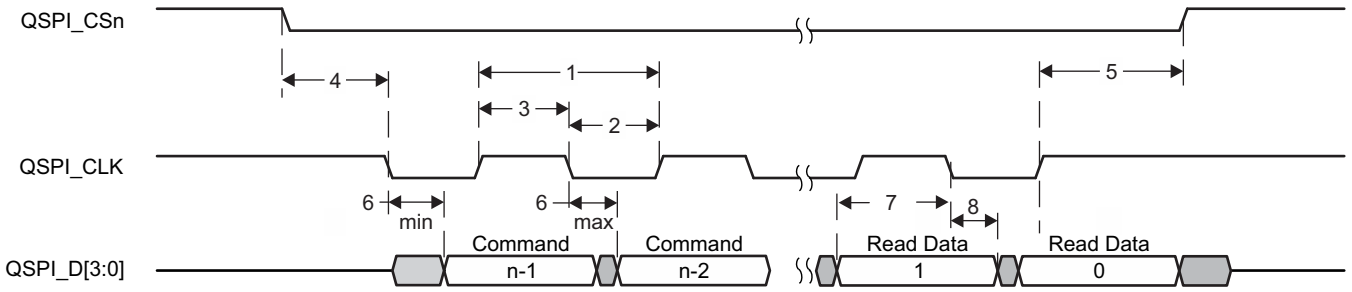



**図 5-110. QSPI Read Active High Polarity**

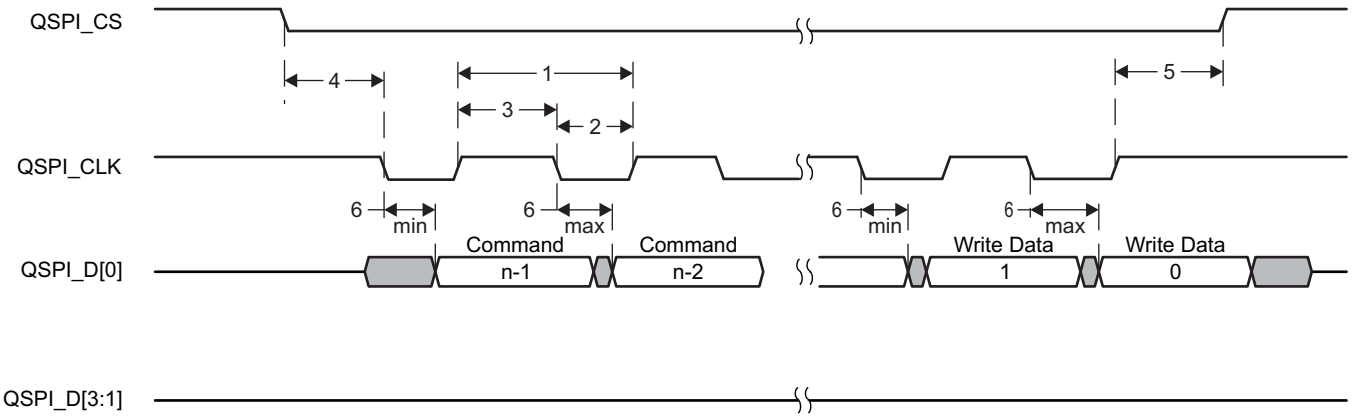



**図 5-111. QSPI Write Active High Polarity**

### *5.12.15 HDQ/1-Wire Interface (HDQ/1-Wire)*

注

For more information, see HDQ/1-Wire Interface chapter of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

The module is intended to work with both HDQ and 1-Wire protocols. The protocols use one wire to communicate between the master and the slave. The protocols employ an asynchronous return to one mechanism where, after any command, the line is pulled high.

#### 5.12.15.1 HDQ Protocol

表 5-95 and 表 5-96 assume testing over the recommended operating conditions (see 図 5-112, 図 5-113, 図 5-114, and 図 5-115).

**表 5-95. HDQ Timing Requirements**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{CYCD}$ | Bit window | 190 | | µs |
| $t_{HW1}$ | Reads 1 | 32 | 66 | µs |
| $t_{HW0}$ | Reads 0 | 70 | 145 | µs |
| $t_{RSPS}$ | Command to host respond time(1) | 190 | 320 | µs |

(1) Defined by software

**表 5-96. HDQ Switching Characteristics**

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{B}$ | Break timing | 190 | | µs |
| $t_{BR}$ | Break recovery | 40 | | µs |
| $t_{CYCH}$ | Bit window | 190 | 250 | µs |
| $t_{DW1}$ | Sends 1 (write) | 0.5 | 50 | µs |
| $t_{DW0}$ | Sends 0 (write) | 86 | 145 | µs |

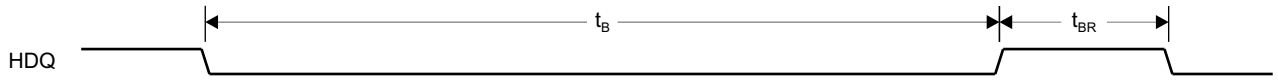



図 5-112. HDQ Break (Reset) Timing

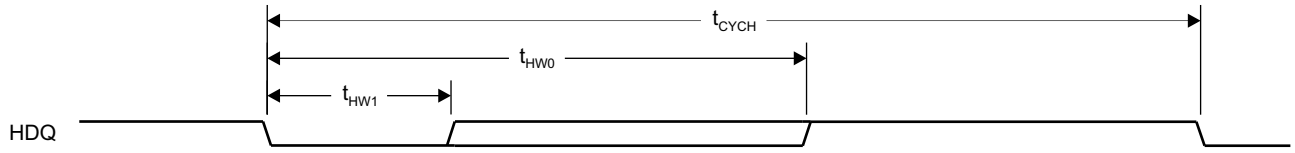



図 5-113. HDQ Read Bit Timing (Data)

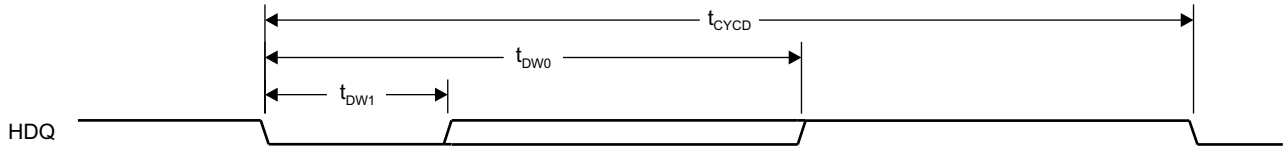



図 5-114. HDQ Write Bit Timing (Command/Address or Data)

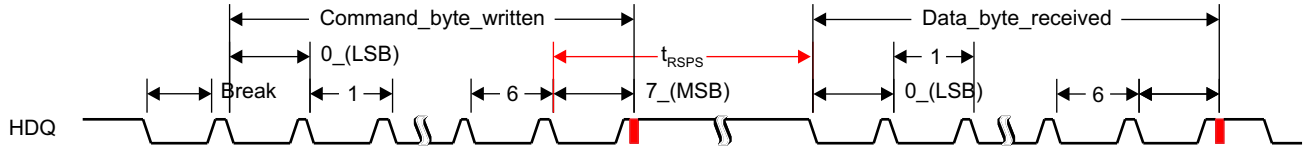



図 5-115. HDQ Communication Timing

### 5.12.15.2 1-Wire Protocol

表 5-97 and 表 5-98 assume testing over the recommended operating conditions (see 図 5-116, 図 5-117, and 図 5-118).

表 5-97. HDQ/1-Wire Timing Requirements—1-Wire Mode

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{PDH}$ | Presence pulse delay high | 15 | 60 | µs |
| $t_{PDL}$ | Presence pulse delay low | 60 | 240 | µs |
| $t_{RDV} + t_{REL}$ | Read bit-zero time | | 60 | µs |

表 5-98. HDQ/1-Wire Switching Characteristics—1-Wire Mode

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{RSTL}$ | Reset time low | 480 | 960 | µs |
| $t_{RSTH}$ | Reset time high | 480 | | µs |
| $t_{SLOT}$ | Bit cycle time | 60 | 120 | µs |
| $t_{LOW1}$ | Write bit-one time | 1 | 15 | µs |
| $t_{LOW0}$ | Write bit-zero time | 60 | 120 | µs |
| $t_{REC}$ | Recovery time | 1 | | µs |
| $t_{LOWR}$ | Read bit strobe time | 1 | 15 | µs |

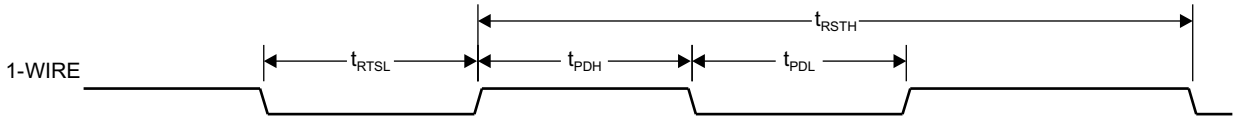



図 5-116. 1-Wire Break (Reset) Timing

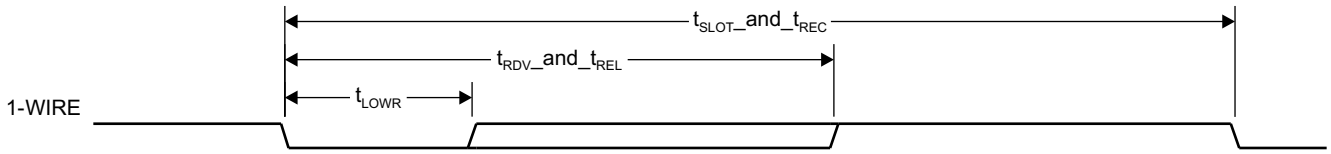



**図 5-117. 1-Wire Read Bit Timing (Data)**

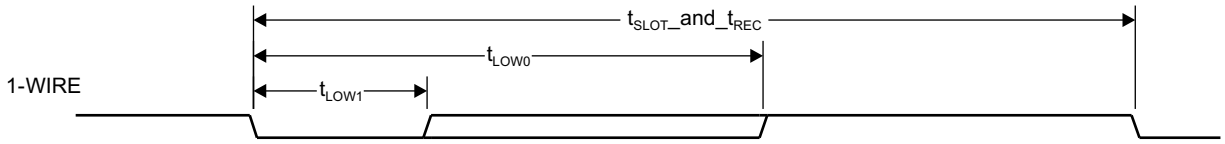



**図 5-118. 1-Wire Write Bit Timing (Command/Address or Data)**

### 5.12.16 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS)

For more information, see the Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem Interface (PRU-ICSS) section of the *AM437x Sitara Processors Technical Reference Manual*.

#### 5.12.16.1 Programmable Real-Time Unit (PRU-ICSS PRU)

**表 5-99. PRU-ICSS PRU Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **Output Condition** | | | | |
| $C_{load}$ | Capacitive load for each bus line | 3 | 30 | pF |

##### 5.12.16.1.1 PRU-ICSS PRU Direct Input/Output Mode Electrical Data and Timing

**表 5-100. PRU-ICSS PRU Timing Requirements - Direct Input Mode**

(see 図 5-119)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(GPI)}$ | Pulse width, GPI | 2*P(1) | | ns |
| 2 | $t_{r(GPI)}$ | Rise time, GPI | 1.00 | 3.00 | ns |
| | $t_{f(GPI)}$ | Fall time, GPI | 1.00 | 3.00 | |
| 3 | $t_{sk(GPI)}$ | Internal skew between GPI[n:0] signals(2) | | 5.00 | ns |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.
(2) n = 16, 11 for PRU-ICSS1 and 19 for PRU-ICSS0

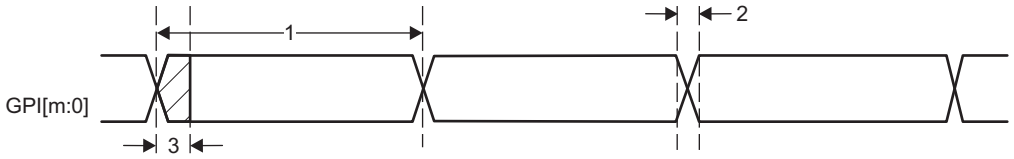



**図 5-119. PRU-ICSS PRU Direct Input Timing**

**表 5-101. PRU-ICSS PRU Switching Requirements - Direct Output Mode**

(see 図 5-103)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(GPO)}$ | Pulse width, GPO | 2*P(1) | | ns |
| 3 | $t_{sk(GPO)}$ | Internal skew between GPO[n:0] signals(2) | | 5.00 | ns |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.
(2) n = 11 for PRU-ICSS1 and 19 for PRU-ICSS0

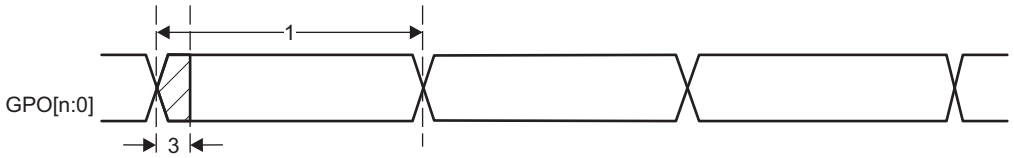



**図 5-120. PRU-ICSS PRU Direct Output Timing**

#### 5.12.16.1.2 PRU-ICSS PRU Parallel Capture Mode Electrical Data and Timing

**表 5-102. PRU-ICSS PRU Timing Requirements - Parallel Capture Mode**

(see 図 5-121 and 図 5-122)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLOCKIN)}$ | Cycle time, CLOCKIN | 20.00 | | ns |
| 2 | $t_{w(CLOCKIN\_L)}$ | Pulse duration, CLOCKIN low | 10.00 | | ns |
| 3 | $t_{w(CLOCKIN\_H)}$ | Pulse duration, CLOCKIN high | 10.00 | | ns |
| 4 | $t_{r(CLOCKIN)}$ | Rising time, CLOCKIN | 1.00 | 3.00 | ns |
| 5 | $t_{f(CLOCKIN)}$ | Falling time, CLOCKIN | 1.00 | 3.00 | ns |
| 6 | $t_{su(DATAIN-CLOCKIN)}$ | Setup time, DATAIN valid before CLOCKIN | 4.00 | | ns |
| 7 | $t_{h(CLOCKIN-DATAIN)}$ | Hold time, DATAIN valid after CLOCKIN | 0 | | ns |
| 8 | $t_{r(DATAIN)}$ | Rising time, DATAIN | 1.00 | 3.00 | ns |
| | $t_{f(DATAIN)}$ | Falling time, DATAIN | 1.00 | 3.00 | |

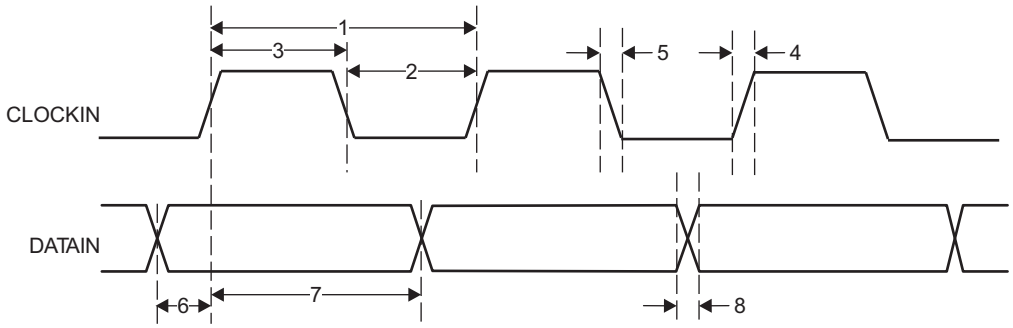



**図 5-121. PRU-ICSS PRU Parallel Capture Timing - Rising Edge Mode**

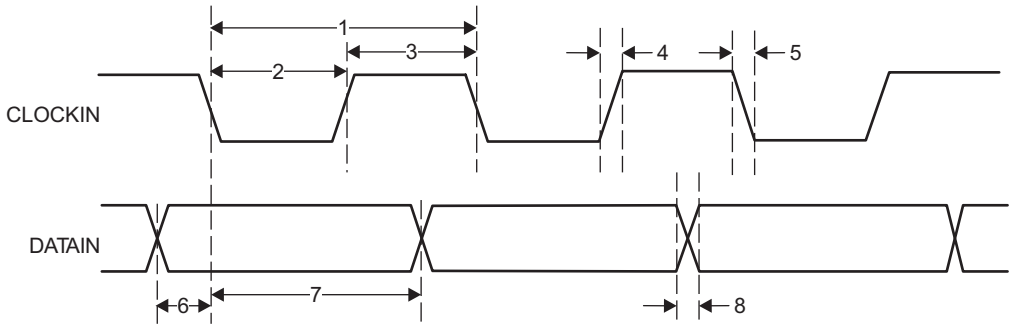



**図 5-122. PRU-ICSS PRU Parallel Capture Timing - Falling Edge Mode**

#### 5.12.16.1.3 PRU-ICSS PRU Shift Mode Electrical Data and Timing

**表 5-103. PRU-ICSS PRU Timing Requirements - Shift In Mode**

(see 図 5-123)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(DATAIN)}$ | Cycle time, DATAIN | 10.00 | | ns |
| 2 | $t_{w(DATAIN)}$ | Pulse width, DATAIN | 0.45*P (1) | 0.55*P (1) | ns |
| 3 | $t_{r(DATAIN)}$ | Rising time, DATAIN | 1.00 | 3.00 | ns |
| 4 | $t_{f(DATAIN)}$ | Falling time, DATAIN | 1.00 | 3.00 | ns |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.

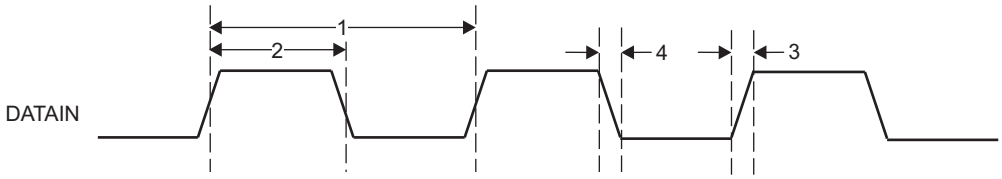



**図 5-123. PRU-ICSS PRU Shift In Timing**

**表 5-104. PRU-ICSS PRU Switching Requirements - Shift Out Mode**

(see 図 5-124)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(CLOCKOUT)}$ | Cycle time, CLOCKOUT | 10.00 | | ns |
| 2 | $t_{w(CLOCKOUT)}$ | Pulse width, CLOCKOUT | 0.45*P (1) | 0.55*P (1) | ns |
| 3 | $t_{r(CLOCKOUT)}$ | Rising time, CLOCKOUT | 1.00 | 3.00 | ns |
| 4 | $t_{f(CLOCKOUT)}$ | Falling time, CLOCKOUT | 1.00 | 3.00 | ns |
| 5 | $t_{d(CLOCKOUT-DATAOUT)}$ | Delay time, CLOCKOUT to DATAOUT Valid | -1.50 | 3.00 | ns |
| 6 | $t_{r(DATAOUT)}$ | Rising time, DATAOUT | 1.00 | 3.00 | ns |
| | $t_{f(DATAOUT)}$ | Falling time, DATAOUT | 1.00 | 3.00 | |

(1) P = L3_CLK (PRU-ICSS ocp clock) period.

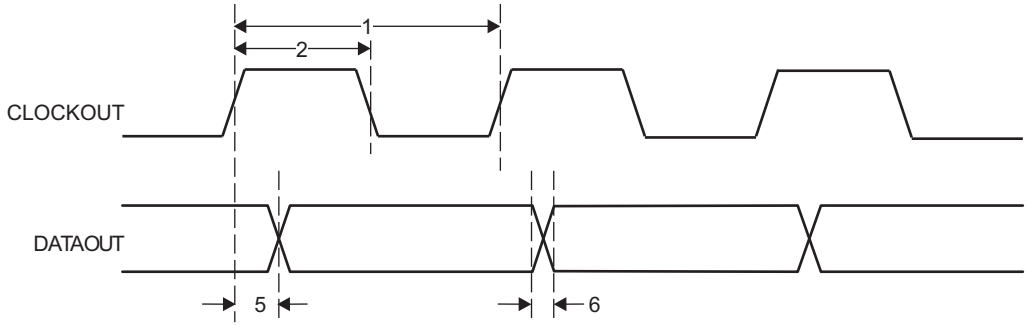



**図 5-124. PRU-ICSS PRU Shift Out Timing**

### *5.12.16.1.4 PRU-ICSS Sigma Delta Electrical Data and Timing*

**表 5-105. PRU-ICSS Timing Requirements - Sigma Delta Mode**

(see 図 5-125 and 図 5-126)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(SDx\_CLK)}$ | Pulse width, SDx_CLK | 20.00 | | ns |
| 2 | $t_{r(SDx\_CLK)}$ | Rising time, SDx_CLK | 1.00 | 3.00 | ns |
| 3 | $t_{f(SDx\_CLK)}$ | Falling time, SDx_CLK | 1.00 | 3.00 | ns |
| 4 | $t_{su(SDx\_D-SDx\_CLK)}$ | Setup time, SDx_D valid before SDx_CLK active edge | 10.00 | | ns |
| 5 | $t_{h(SDx\_CLK-SDx\_D)}$ | Hold time, SDx_D valid before SDx_CLK active edge | 5.00 | | ns |
| 6 | $t_{r(SDx\_D)}$ | Rising time, SDx_D | 1.00 | 3.00 | ns |
| | $t_{f(SDx\_D)}$ | Falling time, SDx_D | 1.00 | 3.00 | |

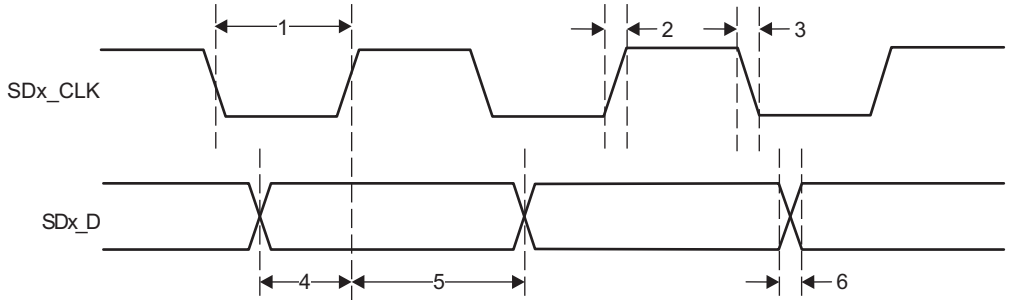



**図 5-125. PRU-ICSS Sigma Delta Timing - SD_CLK Rising Active Edge**

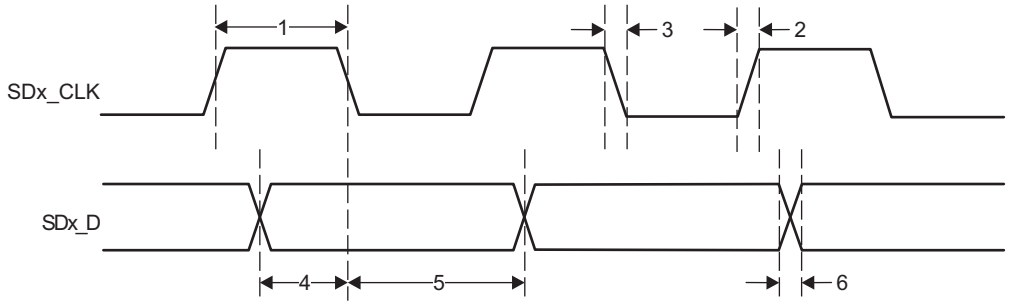



**図 5-126. PRU-ICSS Sigma Delta Timing - SD_CLK Falling Active Edge**

#### *5.12.16.1.5 PRU-ICSS ENDAT Electrical Data and Timing*

**表 5-106. PRU-ICSS Timing Requirements - ENDAT Mode**

(see 図 5-127)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(ENDATx\_IN)}$ | Pulse width, ENDATx_IN | 40.00 | | ns |
| 2 | $t_{r(ENDATx\_IN)}$ | Rising time, ENDATx_IN | 1.00 | 10.00 | ns |
| 3 | $t_{f(ENDATx\_IN)}$ | Falling time, ENDATx_IN | 1.00 | 10.00 | ns |

**表 5-107. PRU-ICSS Switching Requirements - ENDAT Mode**

(see 図 5-127)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 4 | $t_{w(ENDATx\_CLK)}$ | Pulse width, ENDATx_CLK | 20.00 | | ns |
| 5 | $t_{r(ENDATx\_CLK)}$ | Rising time, ENDATx_CLK | 1.00 | 3.00 | ns |
| 6 | $t_{f(ENDATx\_CLK)}$ | Falling time, ENDATx_CLK | 1.00 | 3.00 | ns |
| 7 | $t_{d(ENDATx\_OUT-ENDATx\_CLK)}$ | Delay time, ENDATx_CLK fall to ENDATx_OUT | -10.00 | 10.00 | ns |
| 8 | $t_{r(ENDATx\_OUT)}$ | Rising time, ENDATx_OUT | 1.00 | 3.00 | ns |
| | $t_{f(ENDATx\_OUT)}$ | Falling time, ENDATx_OUT | 1.00 | 3.00 | |
| 9 | $t_{d(ENDATx\_OUT\_EN-ENDATx\_CLK)}$ | Delay time, ENDATx_CLK Fall to ENDATx_OUT_EN | -10.00 | 10.00 | ns |

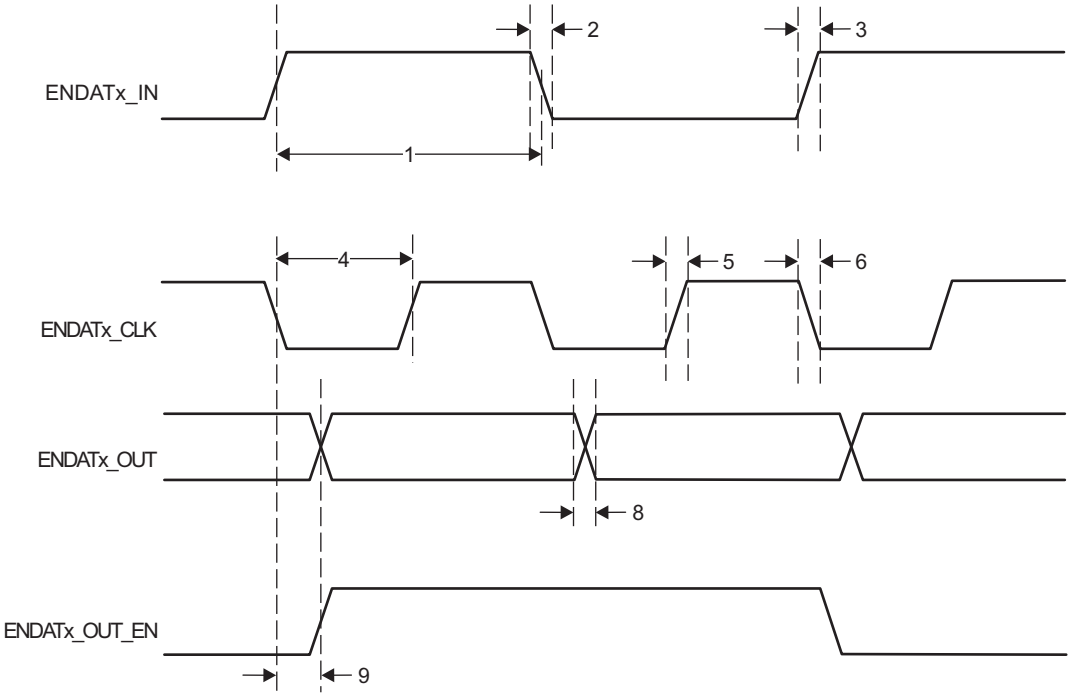



**図 5-127. PRU-ICSS ENDAT Timing**

### 5.12.16.2 PRU-ICSS EtherCAT (PRU-ICSS ECAT)

**表 5-108. PRU-ICSS ECAT Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **Output Condition** | | | | |
| $C_{load}$ | Capacitive load for each bus line | | 30 | pF |

#### *5.12.16.2.1 PRU-ICSS ECAT Electrical Data and Timing*

**表 5-109. PRU-ICSS ECAT Timing Requirements - Input Validated With LATCH_IN**

(see 図 5-128)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDIO\_LATCH\_IN)}$ | Pulse width, EDIO_LATCH_IN | 100.00 | | ns |
| 2 | $t_{r(EDIO\_LATCH\_IN)}$ | Rising time, EDIO_LATCH_IN | 1.00 | 3.00 | ns |
| 3 | $t_{f(EDIO\_LATCH\_IN)}$ | Falling time, EDIO_LATCH_IN | 1.00 | 3.00 | ns |
| 4 | $t_{su(EDIO\_DATA\_IN-EDIO\_LATCH\_IN)}$ | Setup time, EDIO_DATA_IN valid before EDIO_LATCH_IN active edge | 20.00 | | ns |
| 5 | $t_{h(EDIO\_LATCH\_IN-EDIO\_DATA\_IN)}$ | Hold time, EDIO_DATA_IN valid after EDIO_LATCH_IN active edge | 20.00 | | ns |
| 6 | $t_{r(EDIO\_DATA\_IN)}$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_{f(EDIO\_DATA\_IN)}$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | |

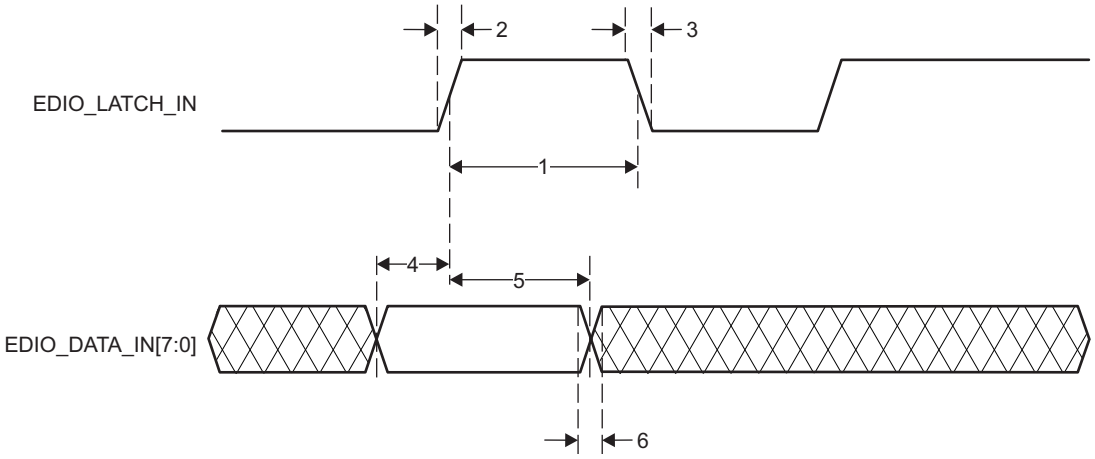



**図 5-128. PRU-ICSS ECAT Input Validated With LATCH_IN Timing**

**表 5-110. PRU-ICSS ECAT Timing Requirements - Input Validated With SYNCx**

(see 図 5-129)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDC\_SYNCx\_OUT)}$ | Pulse width, EDC_SYNCx_OUT | 100.00 | | ns |
| 2 | $t_{r(EDC\_SYNCx\_OUT)}$ | Rising time, EDC_SYNCx_OUT | 1.00 | 3.00 | ns |
| 3 | $t_{f(EDC\_SYNCx\_OUT)}$ | Falling time, EDC_SYNCx_OUT | 1.00 | 3.00 | ns |
| 4 | $t_{su(EDIO\_DATA\_IN-EDC\_SYNCx\_OUT)}$ | Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge | 24.50 | | ns |
| 5 | $t_{h(EDC\_SYNCx\_OUT-EDIO\_DATA\_IN)}$ | Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge | 22.00 | | ns |
| 6 | $t_{r(EDIO\_DATA\_IN)}$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_{f(EDIO\_DATA\_IN)}$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | |

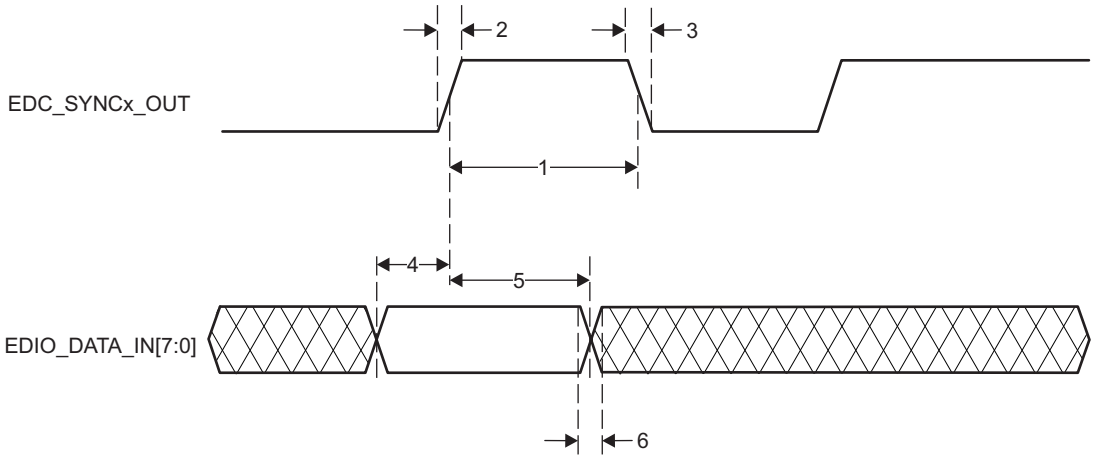



**図 5-129. PRU-ICSS ECAT Input Validated With SYNCx Timing**

### 表 5-111. PRU-ICSS ECAT Timing Requirements - Input Validated With Start of Frame (SOF)

(see 図 5-130)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDIO\_SOF)}$ | Pulse duration, EDIO_SOF | 4*P(1) | 5*P(1) | ns |
| 2 | $t_{r(EDIO\_SOF)}$ | Rising time, EDIO_SOF | 1.00 | 3.00 | ns |
| 3 | $t_{f(EDIO\_SOF)}$ | Falling time, EDIO_SOF | 1.00 | 3.00 | ns |
| 4 | $t_{su(EDIO\_DATA\_IN-EDIO\_SOF)}$ | Setup time, EDIO_DATA_IN valid before EDIO_SOF active edge | 20.00 | | ns |
| 5 | $t_{h(EDIO\_SOF-EDIO\_DATA\_IN)}$ | Hold time, EDIO_DATA_IN valid after EDIO_SOF active edge | 20.00 | | ns |
| 6 | $t_{r(EDIO\_DATA\_IN)}$ | Rising time, EDIO_DATA_IN | 1.00 | 3.00 | ns |
| | $t_{f(EDIO\_DATA\_IN)}$ | Falling time, EDIO_DATA_IN | 1.00 | 3.00 | |

(1) P = PRU-ICSS IEP clock source period.

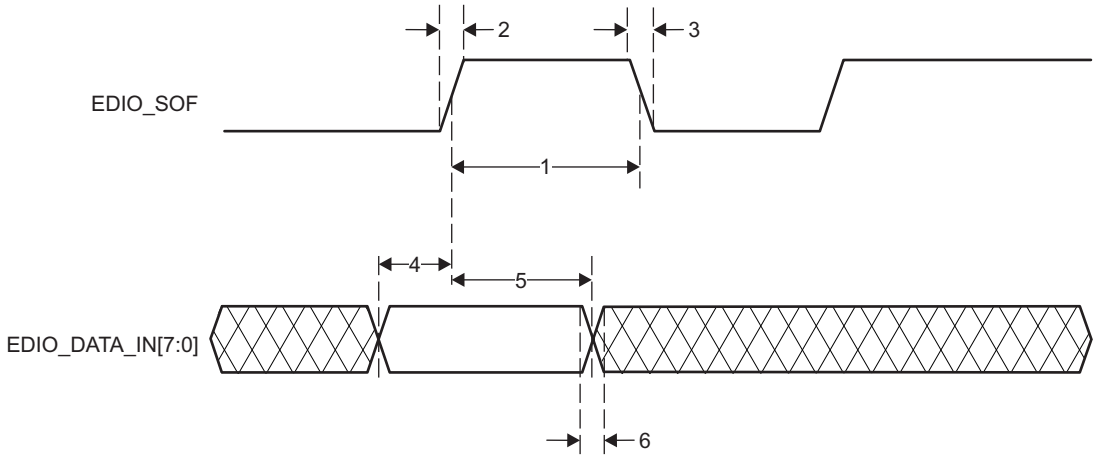



**図 5-130. PRU-ICSS ECAT Input Validated With SOF**

### 表 5-112. PRU-ICSS ECAT Timing Requirements - LATCHx_IN

(see 図 5-131)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDC\_LATCHx\_IN)}$ | Pulse duration, EDC_LATCHx_IN | 3*P(1) | | ns |
| 2 | $t_{r(EDC\_LATCHx\_IN)}$ | Rising time, EDC_LATCHx_IN | 1.00 | 3.00 | ns |
| 3 | $t_{f(EDC\_LATCHx\_IN)}$ | Falling time, EDC_LATCHx_IN | 1.00 | 3.00 | ns |

(1) P = PRU-ICSS IEP clock source period.

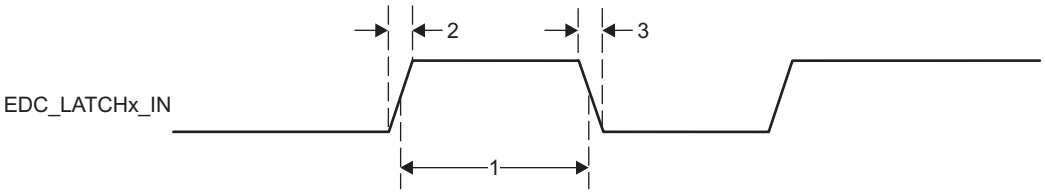



**図 5-131. PRU-ICSS ECAT LATCHx_IN Timing**

**表 5-113. PRU-ICSS ECAT Switching Requirements - Digital IOs**

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{w(EDIO\_OUTVALID)}$ | Pulse duration, EDIO_OUTVALID | 14*P(1) | 32*P(1) | ns |
| 2 | $t_{r(EDIO\_OUTVALID)}$ | Rising time, EDIO_OUTVALID | 1.00 | 3.00 | ns |
| 3 | $t_{f(EDIO\_OUTVALID)}$ | Falling time, EDIO_OUTVALID | 1.00 | 3.00 | ns |
| 4 | $t_{d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)}$ | Delay time, EDIO_OUTVALID to EDIO_DATA_OUT | 0.00 | 18*P(1) | ns |
| 5 | $t_{r(EDIO\_DATA\_OUT)}$ | Rising time, EDIO_DATA_OUT | 1.00 | 3.00 | ns |
| 6 | $t_{f(EDIO\_DATA\_OUT)}$ | Falling time, EDIO_DATA_OUT | 1.00 | 3.00 | ns |
| 7 | $t_{sk(EDIO\_DATA\_OUT)}$ | EDIO_DATA_OUT skew | | 8.00 | ns |

(1) P = PRU-ICSS IEP clock source period.

### 5.12.16.3 PRU-ICSS MII_RT and Switch

**表 5-114. PRU-ICSS MII_RT Switch Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_r$ | Input signal rise time | 1(1) | | 5(1) | ns |
| $t_f$ | Input signal fall time | 1(1) | | 5(1) | ns |
| **Output Condition** | | | | | |
| $C_{LOAD}$ | Output load capacitance | | | 20 | pF |

(1) Except when specified otherwise.

#### *5.12.16.3.1 PRU-ICSS MDIO Electrical Data and Timing*

**表 5-115. PRU-ICSS MDIO Timing Requirements - MDIO_DATA**

(see 図 5-132)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{su(MDIO-MDC)}$ | Setup time, MDIO valid before MDC high | 90 | | | ns |
| 2 | $t_{h(MDIO-MDC)}$ | Hold time, MDIO valid from MDC high | 0 | | | ns |

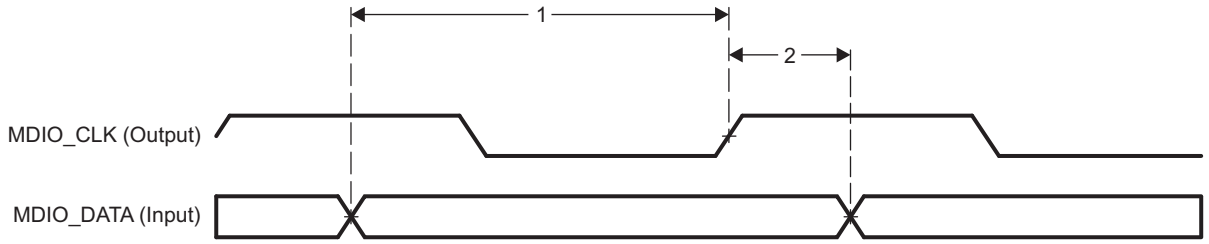



**図 5-132. PRU-ICSS MDIO_DATA Timing - Input Mode**

**表 5-116. PRU-ICSS MDIO Switching Characteristics - MDIO_CLK**

(see 図 5-133)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{c(MDC)}$ | Cycle time, MDC | 400 | | | ns |
| 2 | $t_{w(MDCH)}$ | Pulse duration, MDC high | 160 | | | ns |
| 3 | $t_{w(MDCL)}$ | Pulse duration, MDC low | 160 | | | ns |

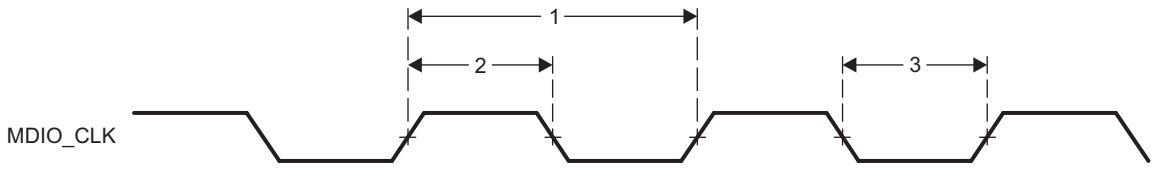



**図 5-133. PRU-ICSS MDIO_CLK Timing**

**表 5-117. PRU-ICSS MDIO Switching Characteristics - MDIO_DATA**

(see 図 5-134)

| NO. | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| 1 | $t_{d(MDC-MDIO)}$ | Delay time, MDC high to MDIO valid | 10 | | (P*0.5)–10 (1) | ns |

(1) P = MDIO_CLK period.

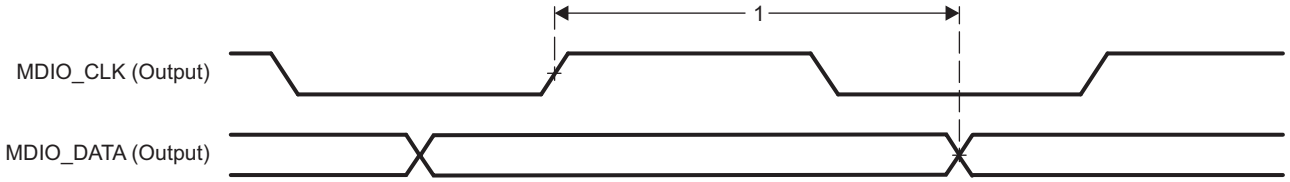



**図 5-134. PRU-ICSS MDIO_DATA Timing - Output Mode**

### *5.12.16.3.2 PRU-ICSS MII_RT Electrical Data and Timing*

注

In order to guarantee the MII_RT I/O timing values published in the device data manual, the PRU ocp_clk clock must be configured for 200 MHz (default value) and the TX_CLK_DELAY bit field in the PRUSS_MII_RT TXCFG0/1 register must be configured as follows:

- 100 Mbps mode: 6h (non-default value)
- 10 Mbps mode: 0h (default value)

**表 5-118. PRU-ICSS MII_RT Timing Requirements - MII_RXCLK**

(see 図 5-135)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(RX\_CLK)}$ | Cycle time, RX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_{w(RX\_CLKH)}$ | Pulse Duration, RX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_{w(RX\_CLKL)}$ | Pulse Duration, RX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_{t(RX\_CLK)}$ | Transition time, RX_CLK | | | 3 | | | 3 | ns |

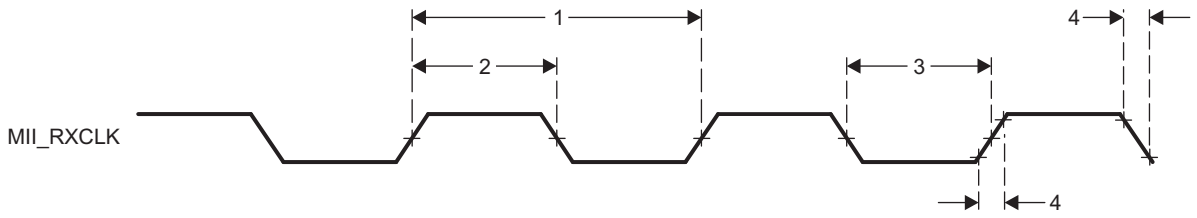



**図 5-135. PRU-ICSS MII_RXCLK Timing**

**表 5-119. PRU-ICSS MII_RT Timing Requirements - MII[x]_TXCLK**

(see 図 5-136)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{c(TX\_CLK)}$ | Cycle time, TX_CLK | 399.96 | | 400.04 | 39.996 | | 40.004 | ns |
| 2 | $t_{w(TX\_CLKH)}$ | Pulse Duration, TX_CLK high | 140 | | 260 | 14 | | 26 | ns |
| 3 | $t_{w(TX\_CLKL)}$ | Pulse Duration, TX_CLK low | 140 | | 260 | 14 | | 26 | ns |
| 4 | $t_{t(TX\_CLK)}$ | Transition time, TX_CLK | | | 3 | | | 3 | ns |

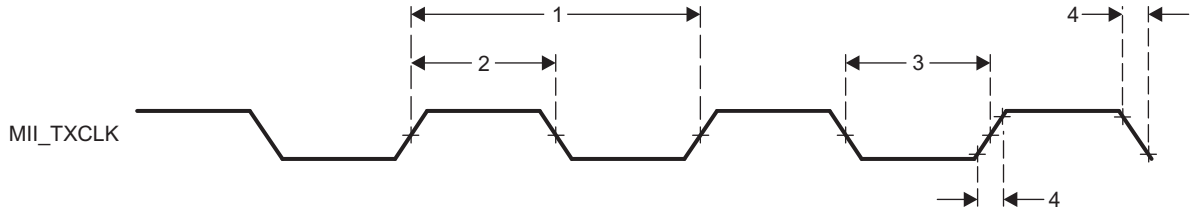



**図 5-136. PRU-ICSS MII_TXCLK Timing**

**表 5-120. PRU-ICSS MII_RT Timing Requirements - MII_RXD[3:0], MII_RXDV, and MII_RXER**

(see 図 5-137)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(RXD-RX\_CLK)}$ | Setup time, RXD[3:0] valid before RX_CLK | 8 | | | 8 | | | ns |
| | $t_{su(RX\_DV-RX\_CLK)}$ | Setup time, RX_DV valid before RX_CLK | | | | | | | |
| | $t_{su(RX\_ER-RX\_CLK)}$ | Setup time, RX_ER valid before RX_CLK | | | | | | | |
| 2 | $t_{h(RX\_CLK-RXD)}$ | Hold time RXD[3:0] valid after RX_CLK | 8 | | | 8 | | | ns |
| | $t_{h(RX\_CLK-RX\_DV)}$ | Hold time RX_DV valid after RX_CLK | | | | | | | |
| | $t_{h(RX\_CLK-RX\_ER)}$ | Hold time RX_ER valid after RX_CLK | | | | | | | |

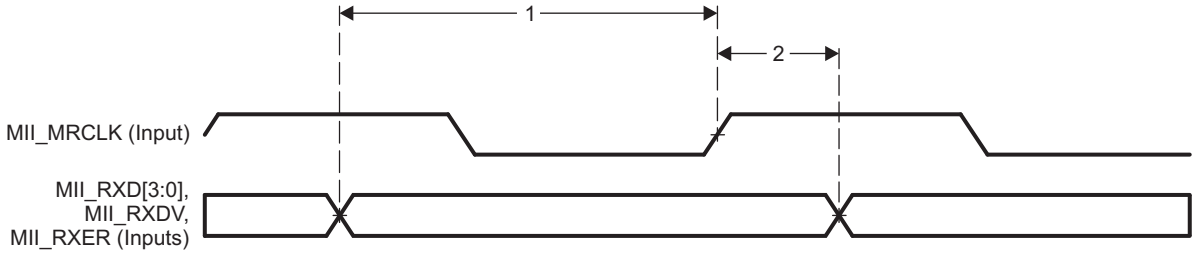



**図 5-137. PRU-ICSS MII_RXD[3:0], MII_RXDV, and MII_RXER Timing**

**表 5-121. PRU-ICSS MII_RT Switching Characteristics - MII_TXD[3:0] and MII_TXEN**

(see 図 5-138)

| NO. | | | 10 Mbps | | | 100 Mbps | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{d(TX\_CLK-TXD)}$ | Delay time, TX_CLK high to TXD[3:0] valid | 5 | | 27 | 5 | | 25 | ns |
| | $t_{d(TX\_CLK-TX\_EN)}$ | Delay time, TX_CLK to TX_EN valid | | | | | | | |

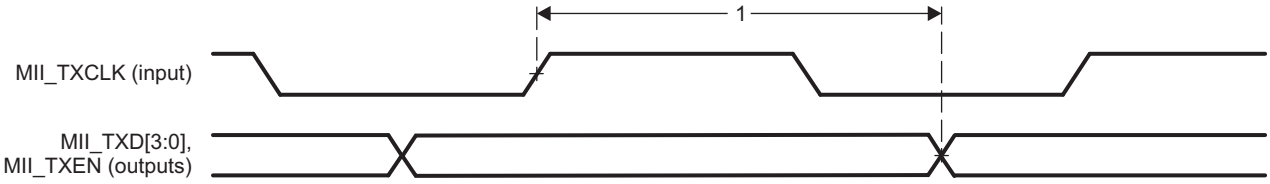



**図 5-138. PRU-ICSS MII_TXD[3:0], MII_TXEN Timing**

### 5.12.16.4 PRU-ICSS Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)

**表 5-122. Timing Requirements for PRU-ICSS UART Receive**

(see 図 5-139)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3 | $t_{w(RX)}$ | Pulse width, receive start, stop, data bit | 0.96U (1) | 1.05U (1) | ns |

(1) U = UART baud time = 1/programmed baud rate.

**表 5-123. Switching Characteristics Over Recommended Operating Conditions for PRU-ICSS UART Transmit**

(see 図 5-139)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $f_{baud(baud)}$ | Maximum programmable baud rate | 0 | 12 | MHz |
| 2 | $t_{w(TX)}$ | Pulse width, transmit start, stop, data bit | U - 2 (1) | U + 2 (1) | ns |

(1) U = UART baud time = 1/programmed baud rate.

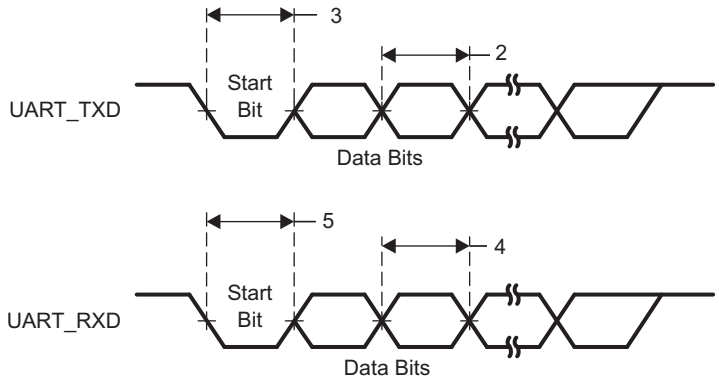



**図 5-139. PRU-ICSS UART Timing**

### 5.12.17 Multimedia Card (MMC) Interface

For more information, see the Multimedia Card (MMC) section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

#### 5.12.17.1 MMC Electrical Data and Timing

**表 5-124. MMC Timing Conditions**

| TIMING CONDITION PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Input Conditions** | | | | | |
| $t_r$ | Input signal rise time | 1 | | 5 | ns |
| $t_f$ | Input signal fall time | 1 | | 5 | ns |
| **Output Condition** | | | | | |
| $C_{load}$ | Output load capacitance | 3 | | 30 | pF |

**表 5-125. Timing Requirements for MMC[0]_CMD and MMC[0]_DAT[7:0]**

(see 図 5-140)

| NO. | | | OPP50/OPP100 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.8 V | | | 3.3 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, MMC_CMD valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 2 | $t_{h(CLKH-CMDV)}$ | Hold time, MMC_CMD valid after MMC_CLK rising clock edge | 1.5 | | | 1.5 | | | ns |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, MMC_DATx valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, MMC_DATx valid after MMC_CLK rising clock edge | 1.5 | | | 1.5 | | | ns |

**表 5-126. Timing Requirements for MMC[1/2]_CMD and MMC[1/2]_DAT[7:0]**

(see 図 5-140)

| NO. | | | OPP50/OPP100 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.8 V | | | 3.3 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, MMC_CMD valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 2 | $t_{h(CLKH-CMDV)}$ | Hold time, MMC_CMD valid after MMC_CLK rising clock edge | 2.55 | | | 3.76 | | | ns |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, MMC_DATx valid before MMC_CLK rising clock edge | 4.1 | | | 4.1 | | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, MMC_DATx valid after MMC_CLK rising clock edge | 2.55 | | | 3.76 | | | ns |

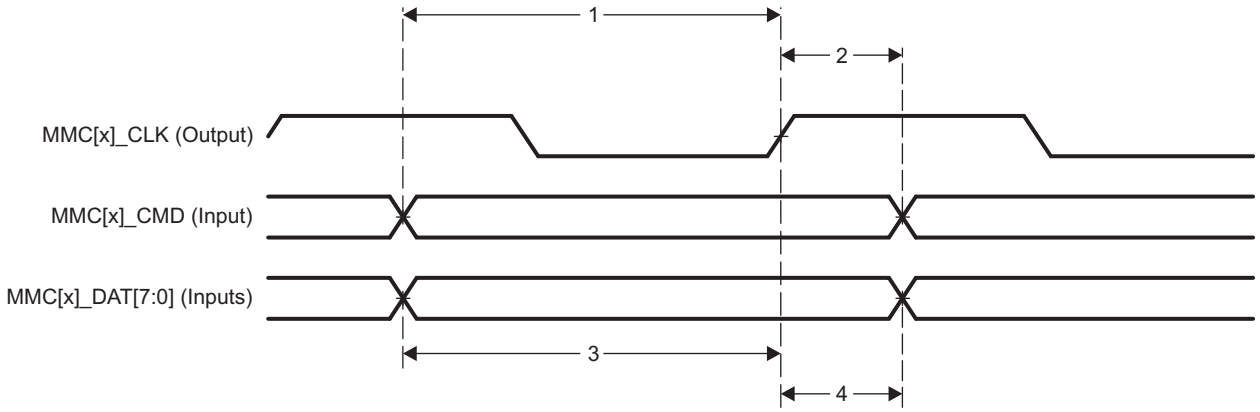



**図 5-140. MMC[x]_CMD and MMC[x]_DAT[7:0] Input Timing**

**表 5-127. Switching Characteristics for MMC[x]_CLK**

(see 図 5-141)

| NO. | PARAMETER | | STANDARD MODE | | | HIGH-SPEED MODE | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 5 | $f_{op(CLK)}$ | Operating frequency, MMC_CLK | | | 24 | | | 48 | MHz |
| | $t_{cop(CLK)}$ | Operating period: MMC_CLK | 41.7 | | | 20.8 | | | ns |
| | $f_{id(CLK)}$ | Identification mode frequency, MMC_CLK | | | 400 | | | 400 | kHz |
| | $t_{cid(CLK)}$ | Identification mode period: MMC_CLK | 2500 | | | 2500 | | | ns |
| 6 | $t_{w(CLKL)}$ | Pulse duration, MMC_CLK low | (0.5*P) - $t_{f(CLK)}$ (1) | | | (0.5*P) - $t_{f(CLK)}$ (1) | | | ns |
| 7 | $t_{w(CLKH)}$ | Pulse duration, MMC_CLK high | (0.5*P) - $t_{r(CLK)}$ (1) | | | (0.5*P) - $t_{r(CLK)}$ (1) | | | ns |

(1) P = MMC_CLK period.

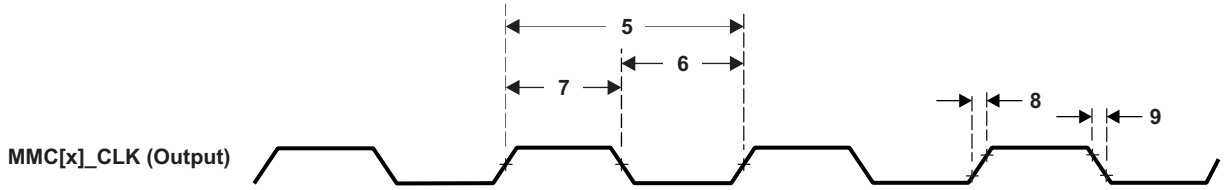



**図 5-141. MMC[x]_CLK Timing**

**表 5-128. Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0]—HSPE=0**

(see 図 5-142)

| NO. | PARAMETER | | OPP50/OPP100 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.8 V | | | 3.3 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 10 | $t_{d(CLKL-CMD)}$ | Delay time, MMC_CLK falling clock edge to MMC_CMD transition | -7.4 | | 4.4 | -7.4 | | 4.4 | ns |
| 11 | $t_{d(CLKL-DAT)}$ | Delay time, MMC_CLK falling clock edge to MMC_DATx transition | -7.4 | | 4.4 | -7.4 | | 4.4 | ns |

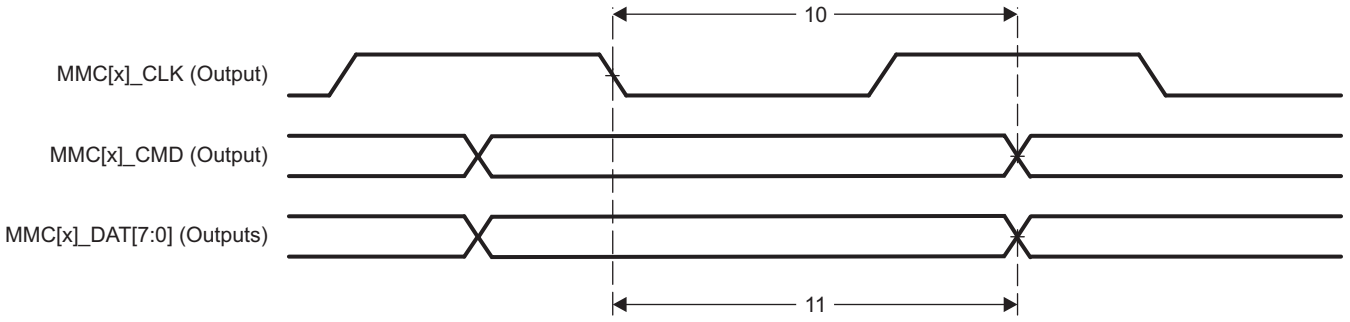



**図 5-142. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—HSPE=0**

**表 5-129. Switching Characteristics for MMC[x]_CMD and MMC[x]_DAT[7:0]—HSPE=1**

(see 図 5-143)

| NO. | PARAMETER | | OPP50/OPP100 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.8 V | | | 3.3 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| 12 | $t_{d(CLKL-CMD)}$ | Delay time, MMC_CLK rising clock edge to MMC_CMD transition | 0.8 | | 7.4 | 0.8 | | 7.4 | ns |
| 13 | $t_{d(CLKL-DAT)}$ | Delay time, MMC_CLK rising clock edge to MMC_DATx transition | 0.8 | | 7.4 | 0.8 | | 7.4 | ns |

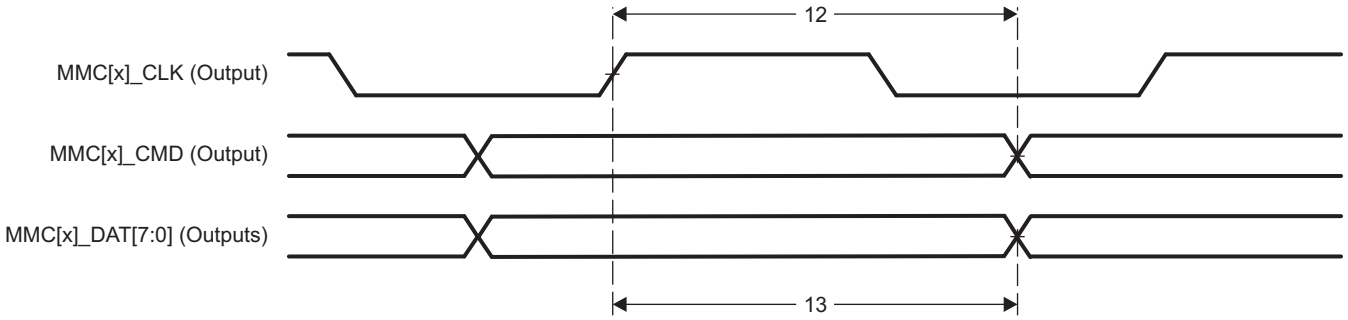



**図 5-143. MMC[x]_CMD and MMC[x]_DAT[7:0] Output Timing—HSPE=1**

### 5.12.18 Universal Asynchronous Receiver/Transmitter (UART)

For more information, see the Universal Asynchronous Receiver/Transmitter (UART) section of the *AM437x ARM Cortex-A9 Microprocessors (MPUs) Technical Reference Manual*.

#### 5.12.18.1 UART Electrical Data and Timing

**表 5-130. Timing Requirements for UARTx Receive**

(see 図 5-144)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 3 | $t_{w(RX)}$ | Pulse width, receive start, stop, data bit | 0.96U(1) | 1.05U(1) | ns |

(1) U = UART baud time = 1/programmed baud rate.

**表 5-131. for UARTx Transmit**

(see 図 5-144)

| NO. | PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $f_{baud(baud)}$ | Maximum programmable baud rate | | 3.6864 | MHz |
| 2 | $t_{w(TX)}$ | Pulse width, transmit start, stop, data bit | U - 2(1) | U + 2(1) | ns |

(1) U = UART baud time = 1/programmed baud rate.

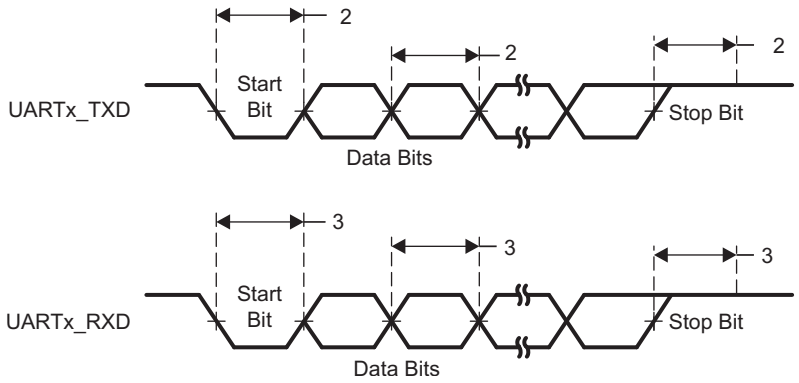



**図 5-144. UART Timings**

### 5.12.18.2 UART IrDA Interface

The IrDA module operates in three different modes:

- Slow infrared (SIR) (≤ 115.2 kbps)
- Medium infrared (MIR) (0.576 Mbps and 1.152 Mbps)
- Fast infrared (FIR) (4 Mbps).

図 5-145 shows the UART IrDA pulse parameters. 表 5-132 and 表 5-133 list the signaling rates and pulse durations for UART IrDA receive and transmit modes.

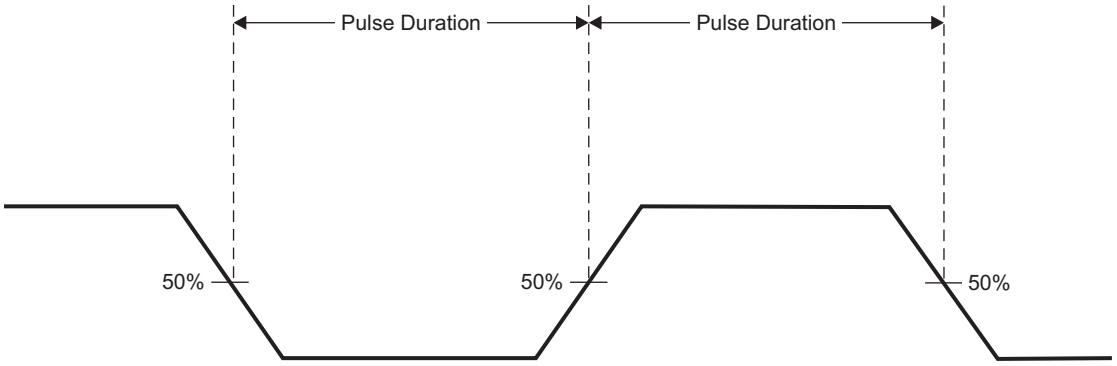



**図 5-145. UART IrDA Pulse Parameters**

**表 5-132. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| **SIR** | | | |
| 2.4 kbps | 1.41 | 88.55 | µs |
| 9.6 kbps | 1.41 | 22.13 | µs |
| 19.2 kbps | 1.41 | 11.07 | µs |
| 38.4 kbps | 1.41 | 5.96 | µs |
| 57.6 kbps | 1.41 | 4.34 | µs |
| 115.2 kbps | 1.41 | 2.23 | µs |
| **MIR** | | | |
| 0.576 Mbps | 297.2 | 518.8 | ns |
| 1.152 Mbps | 149.6 | 258.4 | ns |
| **FIR** | | | |
| 4 Mbps (Single pulse) | 67 | 164 | ns |
| 4 Mbps (Double pulse) | 190 | 289 | ns |

**表 5-133. UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode**

| SIGNALING RATE | ELECTRICAL PULSE DURATION | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| **SIR** | | | |
| 2.4 kbps | 78.1 | 78.1 | µs |
| 9.6 kbps | 19.5 | 19.5 | µs |
| 19.2 kbps | 9.75 | 9.75 | µs |
| 38.4 kbps | 4.87 | 4.87 | µs |
| 57.6 kbps | 3.25 | 3.25 | µs |
| 115.2 kbps | 1.62 | 1.62 | µs |
| **MIR** | | | |
| 0.576 Mbps | 414 | 419 | ns |
| 1.152 Mbps | 206 | 211 | ns |
| **FIR** | | | |
| 4 Mbps (Single pulse) | 123 | 128 | ns |
| 4 Mbps (Double pulse) | 248 | 253 | ns |

## 5.13 Emulation and Debug

### 5.13.1 IEEE 1149.1 JTAG

#### 5.13.1.1 JTAG Electrical Data and Timing

**表 5-134. Timing Requirements for JTAG**

(see 図 5-146)

| NO. | | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 60 | | 60 | | ns |
| 1a | $t_{w(TCKH)}$ | Pulse duration, TCK high (40% of $t_c$) | 24 | | 24 | | ns |
| 1b | $t_{w(TCKL)}$ | Pulse duration, TCK low (40% of $t_c$) | 24 | | 24 | | ns |
| 3 | $t_{su(TDI-TCKH)}$ | Input setup time, TDI valid to TCK high | 3 | | 3 | | ns |
| | $t_{su(TMS-TCKH)}$ | Input setup time, TMS valid to TCK high | 3 | | 3 | | ns |
| 4 | $t_{h(TCKH-TDI)}$ | Input hold time, TDI valid from TCK high | 8 | | 8 | | ns |
| | $t_{h(TCKH-TMS)}$ | Input hold time, TMS valid from TCK high | 8 | | 8 | | ns |

**表 5-135. Switching Characteristics for JTAG**

(see 図 5-146)

| NO. | PARAMETER | | OPP100 | | OPP50 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 2 | $t_{d(TCKL-TDO)}$ | Delay time, TCK low to TDO valid | 0 | 23 | 0 | 23 | ns |

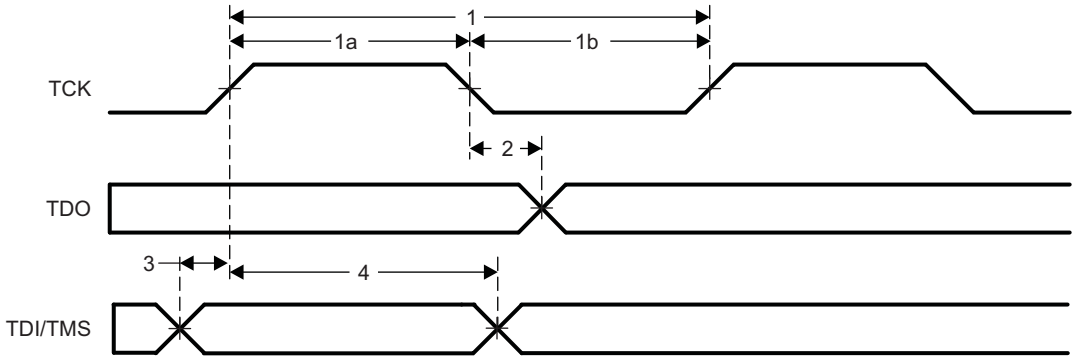



**図 5-146. JTAG Timing**

# 6 Device and Documentation Support

## 6.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all processors and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM4379xZDN). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

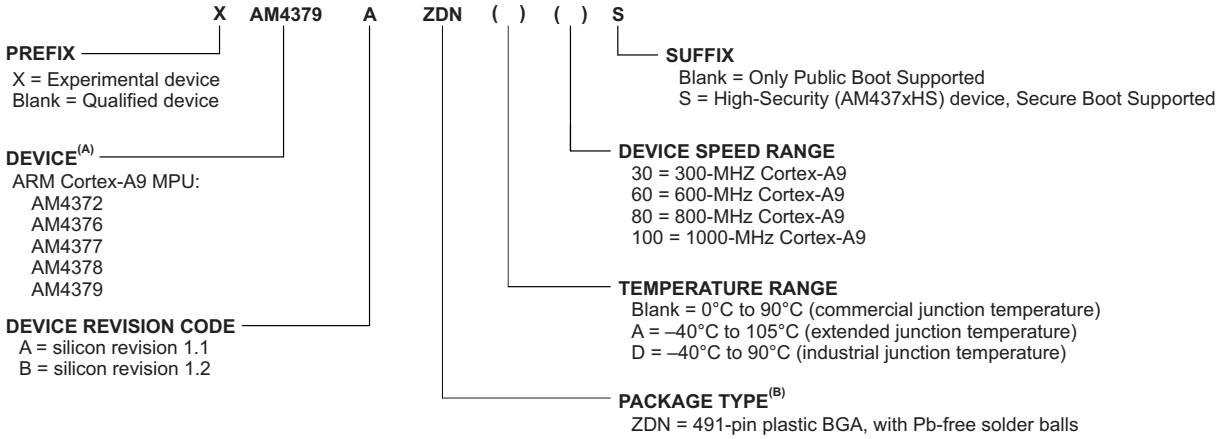
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZDN), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, 80 is 800 MHz). 図 6-1 provides a legend for reading the complete device name for any device.

For orderable part numbers of AM437x devices in the ZDN package type, see the Package Option Addendum of this document, the TI website, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *AM437x Sitara Processors Silicon Errata*.




A. The device shown in this device nomenclature example is one of several valid part numbers for this family of devices. For orderable device part numbers, see the Package Option Addendum of this document.

B. BGA = Ball Grid Array.

**図 6-1. Device Nomenclature**

## 6.2 Tools and Software

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### Models

**AM437x BSDL Model** ZDN package BSDL model.

**AM437x IBIS Model** ZDN package IBIS model.

### Design Kits and Evaluation Modules

**AM437x Evaluation Module** Enables developers to immediately start evaluating the AM437x processor family (AM4372, AM4376, AM4377, AM4378 and AM4379) and begin building applications such as portable navigation, patient monitoring, home/building automation, barcode scanners, portable data terminals and others.

**AM437x Industrial Development Kit (IDK)** An application development platform for evaluating the industrial communication and control capabilities of Sitara AM4379 and AM4377 processors for industrial applications.

**AM437x Starter Kit** Provides a stable and affordable platform to quickly start evaluation of Sitara ARM Cortex-A9 AM437x Processors (AM4372, AM4376, AM4378) and accelerate development for HMI, industrial and networking applications. It is a low-cost development platform based on the ARM Cortex-A9 processor that is integrated with options such as Dual Gigabit Ethernet, DDR3L, Camera and Capacitive Touch Screen LCD.

### TI Designs

**ARM MPU with Integrated BiSS C Master Interface Reference Design** Impelementation of BiSS C Master protocol on Industrial Communication Sub-System (PRU-ICSS). The design provides full documentation and source code for Programmable Realtime Unit (PRU).

**Sercos III Slave For AM437x Communication Development Platform Reference Design** Combines the AM437x Sitara processor family from Texas Instruments (TI) and the Sercos III media access control (MAC) layer into a single system-on-chip (SoC) solution. Targeted for Sercos III slave communications, the TIDEP0039 allows designers to implement the real-time Sercos III communication standard for a broad range of industrial automation equipment.

**EnDat 2.2 System Reference Design** Implements the EnDat 2.2 Master protocol stack and hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. The design is composed of the EnDat 2.2 Master protocol stack, half-duplex communications using RS485 transceivers and the line termination implemented on the Sitara AM437x Industrial Development Kit.

**Acontis EtherCAT Master Stack Reference Design** A highly portable software stack that can be used on various embedded platforms. The EC-Master supports the high performane TI Sitara MPUs, it provides a sophisticated EtherCAT Master solution which customers can use to implement EtherCAT communication interface boards, EtherCAT based PLC or motion control applications.

**SPI Master with Signal Path Delay Compensation Reference Design** Describes the implementation of the SPI master protocol with signal path delay compensation on PRU-ICSS. It supports the 32-bit communication protocol of ADS8688 with a SPI clock frequency of up to 16.7MHz.

**Isolated Current Shunt and Voltage Measurement Reference Design for Motor Drives Using AM437x**
Uses the AMC130x reinforced isolated delta-sigma modulators along with AM437x Sitara ARM Cortex-A9 Processor, which implements Sinc filters on PRU-ICSS. The design provides an ability to evaluate the performance of these measurements: three motor currents, three inverter voltages, and the DC Link voltage.

**Single Chip Drive for Industrial Communications and Motor Control** Implements a hardware interface solution based on the HEIDENHAIN EnDat 2.2 standard for position or rotary encoders. The platform also allows designers to implement real-time EtherCAT communications standards in a broad range of industrial automation equipment.

**AM437x Low Power Suspend Mode with LPDDR2** Realizes processor power consumption less than 0.1 mW while keeping LPDDR2 memory in self refresh consuming ~ 1.6 mW. The system solution is comprised of AM437x Sitara processor, LPDDR2 memory and TPS65218 power management IC and optimized for new low power mode along with support for legacy low power modes.

**AM437x Discrete Power Reference Design** Provides flexibility to power designers. This reference design implementation is a BOM-optimized discrete power solution for the AM437x processor with a minimal number of discrete ICs and basic feature set. T

**Embedded USB 2.0 Reference Design** The USB 2.0 reference design guidelines are extremely important for designers considering USB2.0 electrical compliance testing. The guidelines are applicable to AM335x and AM437x but also generic to other processors. The approach taken for these guidelines is highly practical, without complex formulas or theory.

**ARM MPU with Integrated HIPERFACE DSL Master Interface Reference Design** Implementation of HIPERFACE DSL Master protocol on Industrial Communication Sub-System (PRU-ICSS). The two wire interface allows for integration of position feedback wires into motor cable. Complete solution consists of AM437x PRU-ICSS firmware and TIDA-00177 transceiver reference design.

**Software**

**Processor SDK for AM437X Sitara Processors - Linux and TI-RTOS Support** A unified software platform for TI embedded processors providing easy setup and fast out-of-the-box access to benchmarks and demos. All releases of Processor SDK are consistent across TI's broad portfolio, allowing developers to seamlessly reuse and migrate software across devices.

**Programmable Real-time Unit (PRU) Software Support Package** An add-on package that provides a framework and examples for developing software for the Programmable Real-time Unit sub-system and Industrial Communication Sub-System (PRU-ICSS) in the supported TI processors.

**SYS/BIOS Industrial Software Development Kit (SDK) for Sitara Processors** Gives customers the ability to easily add real-time industrial communications to their design so they can focus on differentiating their application code.

**TI Dual-Mode Bluetooth® Stack** Comprised of Single-Mode and Dual-Mode offerings implementing the Bluetooth 4.0 specification. The Bluetooth stack is fully Bluetooth Special Interest Group (SIG) qualified, certified and royalty-free, provides simple command line sample applications to speed development, and upon request has MFI capability.

### Development Tools

**Clock Tree Tool for Sitara ARM Processors** Interactive clock tree configuration software that provides information about the clocks and modules in Sitara devices.

**Pin Mux Tool** Provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDK) or used to configure customer's custom software. Version 3 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

**Power Estimation Tool (PET)** Provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

**XDS200 USB Debug Probe** Connects to the target board via a TI 20-pin connector (with multiple adapters for TI 14-pin, ARM 10-pin and ARM 20-pin) and to the host PC via USB2.0 High Speed (480Mbps). It also requires a license of Code Composer Studio IDE running on the host PC.

**XDS560v2 System Trace USB and Ethernet Debug Probe** Adds system pin trace in its large external memory buffer. Available for selected TI devices, this external memory buffer captures device-level information that allows obtaining accurate bus performance activity and throughput, as well as power management of core and peripherals. Also, all XDS debug probes support Core and System Trace in all ARM and DSP processors that feature an Embedded Trace Buffer (ETB).

**XDS560v2 System Trace USB Debug Probe** Adds system pin trace in its large external memory buffer. Available for selected TI devices, this external memory buffer captures device-level information that allows obtaining accurate bus performance activity and throughput, as well as power management of core and peripherals. Also, all XDS debug probes support Core and System Trace in all ARM and DSP processors that feature an Embedded Trace Buffer (ETB).

## 6.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

### Errata

**AM437x Sitara Processors Silicon Errata** Describes the known exceptions to the functional specifications for this microprocessor.

### Application Reports

**High-Speed Interface Layout Guidelines** As modern bus interface frequencies scale higher, care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution.

### User's Guides

**AM437x Sitara Processors Technical Reference Manual** Collection of documents providing detailed information on the device including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem as well as a functional description of the peripherals supported is also included.

**Discrete Power Solution for AM437x** Details the implementation of a BOM-optimized discrete power solution for the AM437x processor with a minimal number of discrete ICs and basic feature set. The solution represents a baseline for a discrete power solution that can be extended for additional features of the AM437x processor.

**Powering the AM335x/AM437x with TPS65218** A reference for connectivity between the TPS65218 power management IC and the AM335x or AM437x processor.

**AM437x GP EVM Hardware User's Guide** Describes the hardware architecture of the AM437x Evaluation Module (EVM) (part number TMDXEVM437X), which is based on the Texas Instruments (TI) AM437x processor. This EVM is also commonly known as the AM437x General Purpose (GP) EVM.

**White Papers**

**Highly Integrated industrial Drive to Connect, Control and Communicate** Discusses the overall drive architecture with emphasis on the highly integrated industrial drive solution by Texas Instruments.

**Ensuring Real-Time Predictability** High-performance processors like ARM Cortex-A cores have an entirely different set of resources and pro- cessing capabilities than those of real-time processing cores, like the Programmable Real-Time Unit (PRU) coprocessor in TI's Sitara processors.

**Mainline Linux Ensures Stability and Innovation** Enabling and empowering the rapid development of new functionality starts at the foundational level of the system's software environment – that is, at the level of the Linux kernel – and builds upward from there.

**Scalable Solutions for HMI** A well designed HMI system decreases that gap between the production process and operator through an intuitive visualization system, layers of detail to allow for a bird's eye view down to the minute details, as well as training material and documentation at the operators' fingertips.

**Linaro Speeds Development in TI Linux SDKs** Linaro's software is not a Linux distribution; in fact, it is distribution neutral. The focus of the organization's 120 engineers is on optimizing base-level open-source software in areas that interact directly with the silicon such as multimedia, graphics, power management, the Linux kernel and booting processes.

**Getting Started on TI ARM Embedded Processor Development** Beginning with an overview of ARM technology and available processor platforms, this paper will then explore the fundamentals of embedded design that influence a system's architecture and, consequently, impact processor selection.

**The Yocto Project: Changing the Way Embedded Linux Software Solutions are Developed** Enabling complex silicon devices such as SoC with operating firmware and application software can be a challenge for equipment manufacturers who often are more comfortable with hardware than software issues.

**Other Documents**

**Sitara AM437x Processor With ARM Cortex-A9 Core** TI continues to optimize and expand its portfolio of Sitara processor solutions for the embedded market. With the Sitara AM437x processors support for the ARM Cortex-A9 core, extending performance by up to 40 percent over the current Sitara AM335x processor line.

**Sitara Processors** Using the ARM Cortex-A series of cores, are optimized system solutions that go beyond the core, delivering products that support rich graphics capabilities, LCD displays and multiple industrial protocols.

**AM437x Evaluation Module Quick Start Guide** Designed to help you through the initial setup of the EVM. This EVM allows you to experience Linux and other operating systems (OSs) that showcase the AM437x Cortex-A9 processor, 3D graphics and more.

The following documents are related to the processor. Copies of these documents can be obtained directly from the internet or from your Texas Instruments representative. To determine the revision of the Cortex-A9 core used on your device, see the device-specific errata.

**Cortex-A9 Technical Reference Manual** Technical reference manual for the Cortex-A9 processor.

**ARM Core Cortex-A9 (AT400/AT401) Errata Notice** Provides a list of advisories for the different revisions of the Cortex-A9 processor. For a copy of this document, contact your TI representative.

## 6.4 Related Links

表 6-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 6-1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| AM4372 | Click here | Click here | Click here | Click here | Click here |
| AM4376 | Click here | Click here | Click here | Click here | Click here |
| AM4377 | Click here | Click here | Click here | Click here | Click here |
| AM4378 | Click here | Click here | Click here | Click here | Click here |
| AM4379 | Click here | Click here | Click here | Click here | Click here |

## 6.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 6.6 商標

Sitara, E2E are trademarks of Texas Instruments.
NEON is a trademark of ARM Ltd or its subsidiaries.
ARM, Cortex are registered trademarks of ARM Ltd or its subsidiaries.
Bluetooth is a registered trademark of Bluetooth SIG.
EtherCAT is a registered trademark of EtherCAT Technology Group.
PowerVR SGX is a trademark of Imagination Technologies Limited.
Linux is a registered trademark of Linus Torvalds.
1-Wire is a registered trademark of Maxim Integrated Products, Inc.
EtherNet/IP is a trademark of ODVA, Inc.
PROFIBUS, PROFINET are registered trademarks of PROFIBUS & PROFINET International (PI).
All other trademarks are the property of their respective owners.

## 6.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 6.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical, Packaging, and Orderable Information

## 7.1 Via Channel

The ZDN package has been specially engineered with Via Channel technology. This technology allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with the 0.65-mm pitch package, and substantially reduces PCB costs. It allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel BGA technology.

注

Via Channel technology implemented on the this package makes it possible to build a product with a 4-layer PCB, but a 4-layer PCB may not meet system performance goals. Therefore, system performance using a 4-layer PCB design must be evaluated during product design.

## 7.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device. This data is subject to change without notice and without revision of this document.

The following figure is a preliminary package drawing for the ZDN package option.

**Note:** The ZDN package is shown with a 17-mm × 17-mm array of 491 solder balls with 0.65-mm pitch, with via channel array (VCA) technology.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AM4372BZDN60 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4372BZDN60 |
| AM4372BZDN60.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4372BZDN60 |
| AM4372BZDN80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4372BZDN80 |
| AM4372BZDN80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4372BZDN80 |
| AM4372BZDNA60 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4372BZDNA60 |
| AM4372BZDNA60.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4372BZDNA60 |
| AM4372BZDNA80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4372BZDNA80 |
| AM4372BZDNA80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4372BZDNA80 |
| AM4376BZDN100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4376BZDN100 |
| AM4376BZDN100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4376BZDN100 |
| AM4376BZDN80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4376BZDN80 |
| AM4376BZDN80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4376BZDN80 |
| AM4376BZDNA100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4376BZDNA100 |
| AM4376BZDNA100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4376BZDNA100 |
| AM4376BZDNA80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4376BZDNA80 |
| AM4376BZDNA80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4376BZDNA80 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AM4376BZDND100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND100 |
| AM4376BZDND100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND100 |
| AM4376BZDND30 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND30 |
| AM4376BZDND30.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND30 |
| AM4376BZDND80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND80 |
| AM4376BZDND80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4376BZDND80 |
| AM4377BZDNA100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4377BZDNA100 |
| AM4377BZDNA100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4377BZDNA100 |
| AM4377BZDNA80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4377BZDNA80 |
| AM4377BZDNA80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4377BZDNA80 |
| AM4377BZDND100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4377BZDND100 |
| AM4377BZDND100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4377BZDND100 |
| AM4377BZDND80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4377BZDND80 |
| AM4377BZDND80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4377BZDND80 |
| AM4378BZDN100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4378BZDN100 |
| AM4378BZDN100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4378BZDN100 |
| AM4378BZDN80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4378BZDN80 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| AM4378BZDN80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | 0 to 90 | AM4378BZDN80 |
| AM4378BZDNA100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4378BZDNA100 |
| AM4378BZDNA100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4378BZDNA100 |
| AM4378BZDNA80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4378BZDNA80 |
| AM4378BZDNA80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4378BZDNA80 |
| AM4378BZDND100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4378BZDND100 |
| AM4378BZDND100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4378BZDND100 |
| AM4378BZDND80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4378BZDND80 |
| AM4378BZDND80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 90 | AM4378BZDND80 |
| AM4379BZDNA100 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4379BZDNA100 |
| AM4379BZDNA100.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | - | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4379BZDNA100 |
| AM4379BZDNA80 | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4379BZDNA80 |
| AM4379BZDNA80.B | Active | Production | NFBGA (ZDN) \| 491 | 90 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-3-260C-168 HR | -40 to 105 | AM4379BZDNA80 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

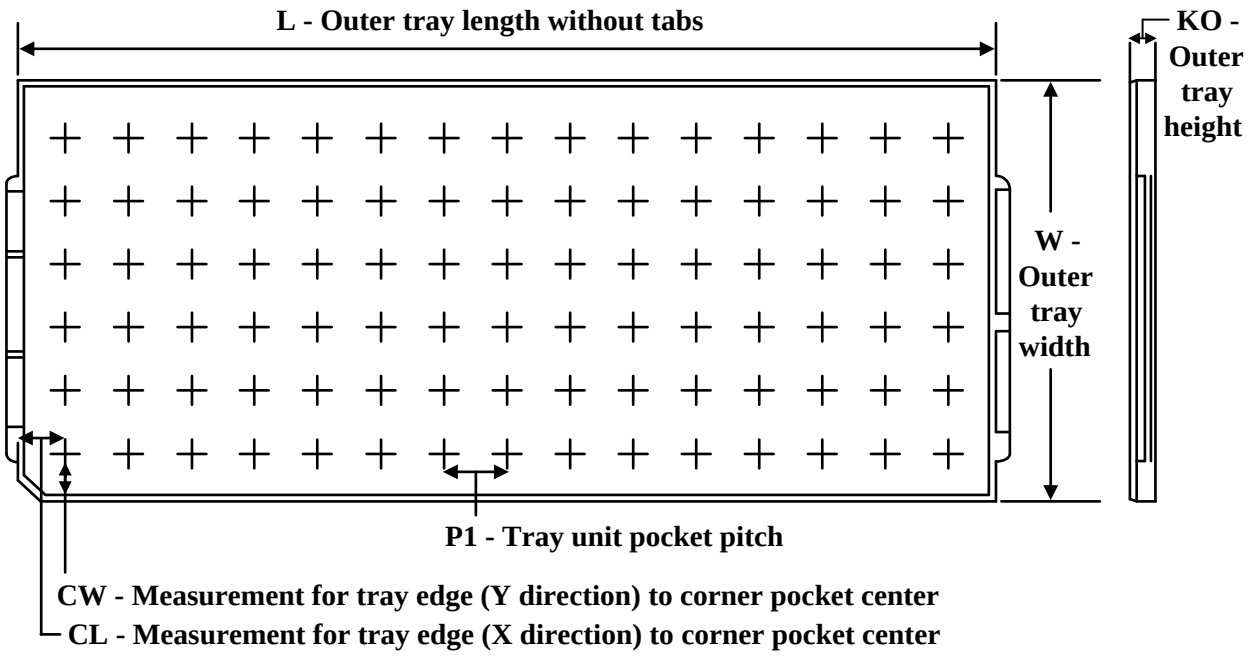
**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TRAY



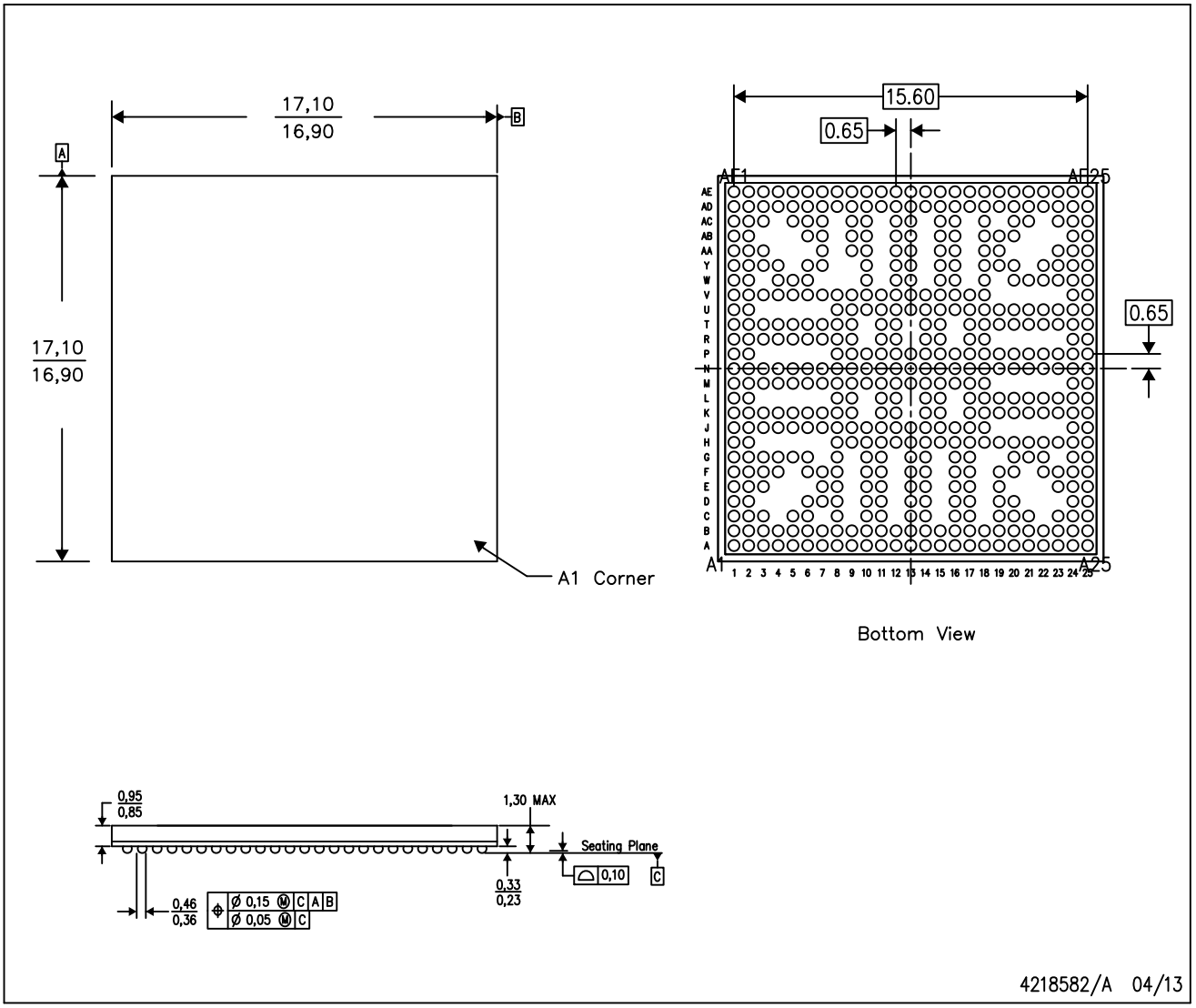

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM4372BZDN60 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDN60.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDN80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDN80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDNA60 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDNA60.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDNA80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4372BZDNA80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDN100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDN100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDN80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDN80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDNA100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDNA100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDNA80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDNA80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDND100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM4376BZDND100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDND30 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDND30.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDND80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4376BZDND80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDNA100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDNA100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDNA80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDNA80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDND100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDND100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDND80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4377BZDND80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDN100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDN100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDN80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDN80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDNA100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDNA100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDNA80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDNA80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDND100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDND100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDND80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4378BZDND80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4379BZDNA100 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4379BZDNA100.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4379BZDNA80 | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |
| AM4379BZDNA80.B | ZDN | NFBGA | 491 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 19.5 | 21 | 19.2 |

ZDN (S–PBGA–N491) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. nFBGA package configuration.
D. This is a Pb–free solder ball design.

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最終更新日：2025 年 10 月