AM62x Sitara™ プロセッサ

1 特長

プロセッサ・コア:

- 最高 1.4GHz、クワッド 64 ビットまでの Arm® Cortex®-A53 マイクロプロセッサ・サブシステム
  - SECDED ECC 付き 512KB L2 共有キャッシュを搭載したクワッド・コア Cortex-A53 クラスタ
  - 各 A53 コアには、SECDED ECC を備えた 32KB L1 D キャッシュおよびパリティ保護を備えた 32KB L1 I キャッシュを搭載
- 最高 400MHz、シングル・コア Arm® Cortex®-M4F MCU
  - 256KB の SRAM (SECDED ECC 付き)
- 専用デバイス / パワー・マネージャ

マルチメディア:

- ディスプレイ・サブシステム
  - デュアル・ディスプレイのサポート
  - 各ディスプレイで 1920x1080 @ 60fps
  - 1 個の 2048x1080 + 1 個の 1280x720
  - ディスプレイごとに独立した PLL を使用して、最大 165MHz のピクセル・クロックをサポートします
  - OLDI (4 レーン LVDS - 2x) および DPI (24 ビット RGB LVCMOS)
  - 凍結フレーム検出や MISR データ・チェックなどの安全機能をサポートします
- 3D グラフィックス処理ユニット
  - クロックあたり 1 ピクセル以上
  - 500 メガピクセル / 秒を超える速度
  - 500 を超える MTexels/s、8 を超える GFLOP
  - 少なくとも 2 つの合成層をサポート
  - 最大 2048x1080 @ 60fps をサポート
  - ARGB32、RGB565、YUV 形式をサポート
  - 2D グラフィックス対応
  - OpenGL ES 3.1、Vulkan 1.2
- 1 つのカメラ・シリアル・インターフェイス (CSI-Rx) - DPHY 付きの 4 レーン
  - MIPI® CSI-2 v1.3 準拠 + MIPI D-PHY 1.2
  - 最大 1.5Gbps の 1、2、3、4 データ・レーン・モードをサポート
  - CRC チェック + RAM 上の ECC による ECC 検証 / 訂正
  - 仮想チャネルのサポート (最大 16)
  - DMA 経由で DDR にストリーム・データを直接書き込む機能

メモリ・サブシステム:

- 最大 816KB のオンチップ RAM
  - SECDED ECC 付きの 64KB のオンチップ RAM (OCSRAM) は、最大 2 つの独立したメモリ・バンクについて、32KB 単位でより小さなバンクに分割できます
  - SMS サブシステムに SECDED ECC を搭載した 256KB のオンチップ RAM
  - テキサス・インスツルメンツのセキュリティ・ファームウェア用の SMS サブシステムに SECDED ECC を搭載した 176KB のオンチップ RAM
  - Cortex-M4F MCU サブシステムに SECDED ECC を搭載した 256KB のオンチップ RAM
  - デバイス / パワー・マネージャ・サブシステムに SECDED ECC を搭載した 64KB のオンチップ RAM
- DDR サブシステム (DDRSS)
  - LPDDR4、DDR4 メモリ・タイプをサポート
  - インライン ECC 付きの 16 ビット・データ・バス
  - 最高 1600MT/s の速度をサポート
  - アドレス可能な最大距離
    - 8GBytes + DDR4
    - 4GBytes + LPDDR4

機能安全:

- 機能安全準拠予定 [産業用]
  - 機能安全アプリケーション向けに開発
  - IEC 61508 機能安全システム設計を支援するドキュメントを準備中
  - SIL 3 までを対象とする決定論的対応能力
  - SIL 2 までを対象とするハードウェア・インテグリティ
  - 安全関連認証
    - TUV SUD による IEC 61508 認定を計画中
- 機能安全準拠予定 [車載用]
  - 機能安全アプリケーション向けに開発
  - ISO 26262 機能安全システム設計を支援するドキュメントを準備中
  - ASIL D までを対象とする決定論的対応能力
  - ASIL B までを対象とするハードウェア・インテグリティ
  - 安全関連認証
    - TUV SUD による ISO 26262 認定を計画中
- AEC - Q100 認定済み

セキュリティ:

- セキュア・ブート対応
  - ハードウェアで強化された信頼の基点 (RoT:Root-of-Trust)
  - バックアップ・キーによる RoT の切り替えをサポート
  - テイクオーバー保護、IP 保護、ロールバック禁止保護のサポート
- 信頼できる実行環境 (TEE) に対応
  - Arm TrustZone® をベースとする TEE
  - 分離用の広範なファイアウォール・サポート
  - セキュアなウォッチドッグ / タイマ / IPC
  - セキュアなストレージのサポート
  - リプレイ保護メモリ・ブロック (RPMB) のサポート
- 専用セキュリティ・コントローラ、ユーザー・プログラマブルな HSM コア、専用セキュリティ DMA および IPC サブシステム付き、絶縁処理用
- 暗号化アクセラレーション対応
  - 受信データ・ストリームに基づいてキーマテリアルを自動的に切り替えできるセッション認識暗号化エンジン
    - 暗号化コアをサポート
  - AES - 128/192/256 ビットのキー・サイズ
  - SHA2 - 224/256/384/512 ビットのキー・サイズ
  - DRBG と真性乱数発生器
  - セキュア・ブート対応のため PKA (公開鍵アクセラレータ) により RSA/ECC 処理を支援
- デバッグのセキュリティ
  - ソフトウェア制御によるセキュアなデバッグ・アクセス
  - セキュリティ対応のデバッグ

PRU サブシステム:

- 最大 333MHz で動作するデュアル・コア・プログラマブル・リアルタイム・ユニット・サブシステム (PRUSS)
- 追加の機能など、サイクル精度の高いプロトコルを実現するために GPIO を駆動することを目的としています。
  - 汎用入出力 (GPIO)
  - UART
  - I^2C
  - 外部 ADC
- PRU ごとに 16KB のプログラム・メモリ、SECDED ECC 付き
- PRU ごとに 8KB のデータ・メモリ、SECDED ECC 付き
- 32KB 汎用メモリ、SECDED ECC 付き
- CRC32/16 HW アクセラレータ
- 30 x 32 ビット・レジスタの 3 バンクを備えたスクラッチ・パッド・メモリ
- 9 個のキャプチャ・イベントと 16 個の比較イベントを搭載した 1 つの産業用 64 ビット・タイマと、低速および高速の補正
- 1 つの割り込みコントローラ (INTC)、最小 64 の入力イベントをサポート

高速インターフェイス:

- 次の機能をサポートするイーサネット・スイッチを内蔵 (合計 2 つの外部ポート)
  - RMII (10/100) または RGMII (10/100/1000)
  - IEEE1588 (Annex D、Annex E、Annex F と 802.1AS PTP)
  - Clause 45 MDIO PHY 管理
  - ALE エンジン (512 の分類子) に基づくパケット分類器
  - プライオリティ・ベースのフロー制御
  - 時間に制約のあるネットワーク機能 (TSN) のサポート
  - 4 個の CPU ハードウェア割り込みペーシング
  - ハードウェアの IP/UDP/TCP チェックサム・オフロード
- 2 つの USB2.0 ポート
  - USB ホスト、USB ペリフェラル、USB デュアルロール・デバイス (DRD モード) として構成可能なポート
  - USB VBUS 検出機能を内蔵
  - USB 経由のトレースをサポート

一般的な接続機能:

- 9 個のユニバーサル非同期レシーバ・トランスミッタ (UART)
- 5 個のシリアル・ペリフェラル・インターフェイス (SPI) コントローラ
- 6 個の内蔵回路間 (I^2C) ポート
- 3 個のマルチチャネル・オーディオ・シリアル・ポート (McASP)
  - 最高 50MHz の送信および受信クロック
  - TX と RX の各クロックが独立した 3 個の McASP で最大 16/10/6 本のシリアル・データ・ピン
  - 時分割多重化 (TDM)、IC 間サウンド (I2S)、および類似のフォーマットをサポート
  - デジタル・オーディオ・インターフェイス送信 (SPDIF、IEC60958-1、AES-3 フォーマット) をサポート
  - 送受信用 FIFO バッファ (256 バイト)
  - オーディオ・リファレンス出力クロックのサポート
- 3 個の拡張 PWM モジュール (ePWM)
- 3 個の拡張直交エンコーダ・パルス・モジュール (eQEP)
- 3 個の拡張キャプチャ・モジュール (eCAP)
- 汎用 I/O (GPIO) では、すべての LVCMOS I/O を GPIO として構成できます
- 3 個のコントローラ・エリア・ネットワーク (CAN) モジュール、CAN-FD をサポート
  - CAN プロトコル 2.0A、B、ISO 11898-1 に準拠
  - 完全な CAN FD のサポート (最大 64 データ・バイト)
  - メッセージ RAM のパリティ / ECC チェック
  - 最大速度:8Mbps

メディアおよびデータ・ストレージ:

- 2 つのマルチメディア・カード / セキュア・デジタル® (MMC/SD®) インターフェイス
  - 1 個の 8 ビット eMMC インターフェイス、最大速度 HS200
  - 2 個の 4 ビット SD/SDIO インターフェイス、最大 UHS-I
  - eMMC 5.1、SD 3.0、SDIO バージョン 3.0 に準拠
- 最大 133MHz の 1 つの汎用メモリ・コントローラ (GPMC)
  - 柔軟な 8 および 16 ビットの非同期メモリ・インターフェイスと、最大 4 つのチップ (22 ビット・アドレス) セレクト (NAND、NOR、Muxed-NOR、SRAM)
  - BCH コードを使用して 4、8、または 16 ビット ECC をサポート
  - ハミング・コードを使用して 1 ビット ECC をサポート
  - エラー特定モジュール (ELM)
    - GPMC と組み合わせて使用すると、BCH アルゴリズムで生成されたシンドローム多項式により、データ・エラーのアドレスを特定可能
    - BCH アルゴリズムに基づいて、512 バイトのブロックごとに 4、8、または 16 ビットのエラーを特定可能
- DDR/SDR をサポートする OSPI/QSPI
  - シリアル NAND およびシリアル NOR フラッシュ・デバイスをサポート
  - 4GByte のメモリ・アドレスをサポート
  - オプションのオンザフライ暗号化を備えた XIP モード

パワー・マネージメント:

- デバイス / パワー・マネージャでサポートされている低消費電力モード
  - CAN/GPIO/UART ウェークアップに対する部分的 IO サポート
  - ディープスリープ
  - MCU のみ
  - スタンバイ
  - Cortex-A53 用のダイナミック周波数スケーリング

最適なパワー・マネージメント・ソリューション:

- 推奨される TPS65219 パワー・マネージメント IC (PMIC)
  - デバイスの電源要件を満たすように特別に設計されたコンパニオン PMIC
  - さまざまな使用事例をサポートするためのフレキシブルなマッピングと工場出荷時にプログラムされた構成

ブート・オプション:

- UART
- I^2C EEPROM
- OSPI/QSPI フラッシュ
- GPMC NOR/NAND フラッシュ
- シリアル NAND フラッシュ
- SD カード
- eMMC
- マス・ストレージ・デバイスからの USB (ホスト) ブート
- 外部ホストからの USB (デバイス) ブート (DFU モード)
- イーサネット

テクノロジー / パッケージ:

- 16nm テクノロジー
- 13mm × 13mm、0.5mm ピッチ、425 ピン FCCSP BGA (ALW)
- 17.2mm × 23mm、0.8mm ピッチ、441 ピンの FCBGA (AMC)

2 アプリケーション

- ヒューマン・マシン・インターフェイス (HMI)
- リテール・オートメーション
- ドライバー監視システム (DMS / OMS) / 車内監視 (ICM)
- テレマティクス制御ユニット (TCU)
- 3D ポイント・クラウド
- 路車間 (V2X) / 車車間 (V2V)
- 再構成可能な 3D 車載インストルメント・クラスタ
- 家電製品向けユーザー・インターフェイスとコネクティビティ
- 医療用機器

3 概要

低コストの AM62x Sitara™ MPU アプリケーション・プロセッサ・ファミリは、Linux® アプリケーション開発向けに構築されています。スケーラブルな Arm® Cortex®-A53 の性能と、デュアル・ディスプレイ・サポートや 3D グラフィックス・アクセラレーションなどの組込み機能に加えて、広範なペリフェラル・セットを搭載する AM62x デバイスは広範な産業用および車載用アプリケーションに適しており、インテリジェントな機能と最適化された電源アーキテクチャも提供します。

アプリケーションの一部を以下に示します。

- 産業用ヒューマン・マシン・インターフェイス (HMI)
- EV 充電ステーション
- タッチレスのビル・アクセス
- ドライバー監視システム

AM62x Sitara™ プロセッサは、13 x 13mm パッケージ (ALW) の産業用グレードであり、17.2 x 17.2mm パッケージ (AMC) の AEC-Q100 車載規格に適合できます。産業用および車載用の機能安全要件は、内蔵された Cortex-M4F コアと専用ペリフェラルを使用して満たすことができます。これらはすべて、AM62x プロセッサの残り部分から絶縁できます。

3 ポートのギガビット・イーサネット・スイッチには、1 つの内部ポートと 2 つの外部ポートがあり、時間に制約のあるネットワーク機能 (TSN) をサポートしています。デバイスに追加の PRU モジュールが搭載されているため、お客様独自の使用事例でリアルタイム I/O 機能を実現できます。さらに、AM62x に搭載されている広範なペリフェラル・セットにより、以下のようなシステム・レベルのコネクティビティを実現できます。USB、MMC/SD、カメラ・インターフェイス、OSPI、CAN-FD、GPMC により、外部 ASIC/FPGA とのパラレル・ホスト・インターフェイスを実現。AM62x デバイスは、内蔵のハードウェア・セキュリティ・モジュール (HSM) を使用した IP 保護用セキュア・ブートもサポートしており、消費電力が重要なポータブル・アプリケーション向けに高度なパワー・マネージメント・サポートを採用しています

AM62x プロセッサ・ファミリの製品:

- AM625 – Arm®Cortex®-A53 ベースのエッジ AI とフル HD デュアル・ディスプレイを搭載したヒューマン・マシン・インタラクション向け SoC
- AM625-Q1 – デジタル・クラスタ向けに安全機能を内蔵した車載ディスプレイ向け SoC
- AM623 – Arm® Cortex®-A53 ベースの物体検出機能とジェスチャ認識機能搭載、IoT (モノのインターネット) とゲートウェイ向け SoC
- AM620-Q1 – ドライバー監視、ネットワーク、V2X システム向けの安全機能を内蔵した車載コンピューティング向け SoC

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AM625	ALW (FCCSP BGA、425)	13mm × 13mm
AM625-Q1	AMC (FCBGA、441)	17.2mm × 17.2mm
AM623	ALW (FCCSP BGA、425)	13mm × 13mm

パッケージ情報 (continued)

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AM620-Q1	AMC (FCBGA、441)	17.2mm × 17.2mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

3.1 機能ブロック図

このデバイスの機能ブロック図を、図 3-1 に示します。

注

テキサス・インスツルメンツのソフトウェア開発キット (SDK) が現在サポートしているデバイス機能を理解するには、**Processor-SDK-AM62x** にある「ダウンロード」タブ・オプションにある AM62x ソフトウェア・ビルド・シートを検索してください。

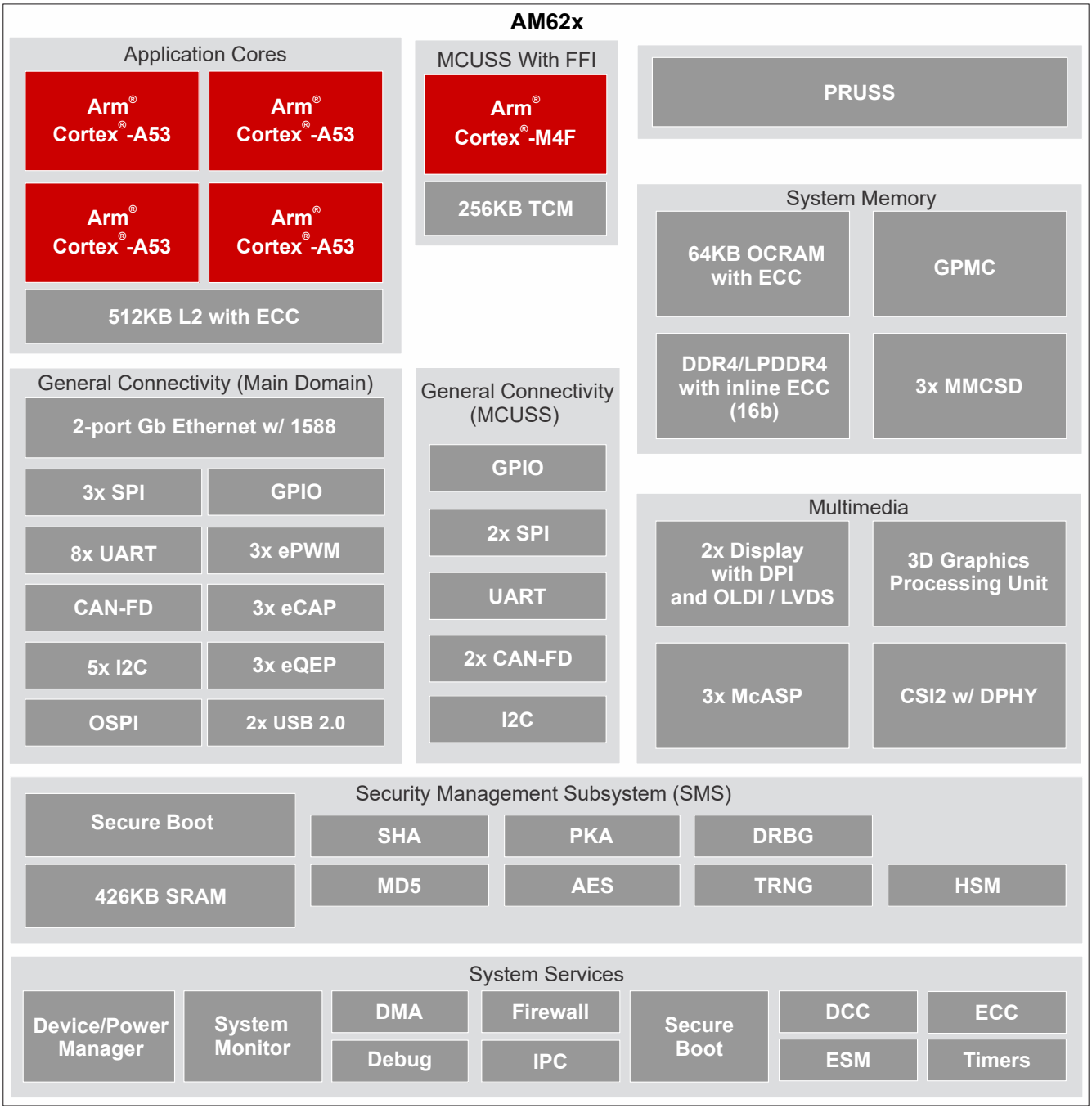

図 3-1. 機能ブロック図

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4 Revision History

Changes from November 12, 2022 to June 15, 2023 (from Revision A (NOVEMBER 2022) to Revision B (JUNE 2023)) **Page**

where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 210
- (OSPI0 Switching Characteristics – PHY SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 212
- (OSPI0 Switching Characteristics – PHY DDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 214
- (OSPI0 Timing Requirements – Tap SDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O19 and O20. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....216
- (OSPI0 Switching Characteristics – Tap SDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM..... 216
- (OSPI0 Timing Requirements – Tap DDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O13 and O14. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM.....218
- (OSPI0 Switching Characteristics – Tap DDR Mode): Updated the minimum data output delay and maximum data output delay formulas in parameter O6. Also updated Note 1 and Note 5, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 5 so it matches the clock name used in the TRM..... 218
- (PRUSS PRU Switching Characteristics – Direct Output Mode): Changed the maximum skew value for the GPO to GPO parameter (PRDO1) from 3ns to 2ns.....220
- (PRUSS UART Switching Characteristics): Added a maximum value and units to the start bit low pulse width parameter (4).....225
- (Device Nomenclature): Updated the orderable part number example in the first paragraph by removing the "X" prefix.....248
- (Device Nomenclature): Changed "ALV package type" in the last paragraph to "ALW or AMC package types".....248
- (Device Naming Convention): Added AM620x devices.....250
- (Device Naming Convention): Changed "ppp" to "PPP" to match the upper case letters used in the Standard Package Symbolization figure..... 250

5 Device Comparison

表 5-1 shows a comparison between devices, highlighting the differences.

注

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

注

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM62x Software Build Sheet* located in the Downloads tab option provided at **Processor-SDK-AM62x**.

表 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM625, AM625-Q1			AM623			AM620-Q1		
		AM6254	**AM6252**	**AM6251**	**AM6234**	**AM6232**	**AM6231**	**AM6204**	**AM6202**	**AM6201**
WKUP_MMR0_JTAG_USER_ID[31:13][1] Register bit values by device "Features" code (See Device Naming Convention for more information on device features)										
C:		0x1D123	0x1D0A3	–	0x1D103	0x1D083	–	–	–	–
G:		0x1D127	0x1D0A7	0x1D067	0x1D107	0x1D087	0x1D047	0x1D307	0x1D287	0x1D247
PROCESSORS AND ACCELERATORS										
Speed Grades (See Device Speed Grades)		T, S, K, G								
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core	Dual Core	Single Core	Quad Core	Dual Core	Single Core	Quad Core	Dual Core	Single Core
Arm Cortex-M4F in MCU domain	Arm M4F	Single Core Functional Safety Optional[5]								
3D Graphics Engine (OpenGL ES 3.1, Vulkan 1.2)	3D Graphics engine	Yes	Yes	Yes	No	No	No	No	No	No
Device Management Subsystem	WKUP_R5F	Single core								
Crypto Accelerators	Security	Yes								
PROGRAM AND DATA STORAGE										
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	64KB (with SECDED ECC)								
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB								
DDR4/LPDDR4 DDR Subsystem	DDRSS	16-bit data with inline ECC; up to 8GB using DDR4 or 4GB using LPDDR4								
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC								
PERIPHERALS										
Display Subsystem	DSS	1x DPI						No		
		1x LVDS						No		
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	3								
General-Purpose I/O	GPIO	Up to 170								
Inter-Integrated Circuit Interface	I2C	6								
Multichannel Audio Serial Port	MCASP	3								
Multichannel Serial Peripheral Interface	MCSPI	5								
Multi-Media Card/ Secure Digital Interface	MM/CSD	1x eMMC (8-bits)								
		2x SD/SDIO (4-bits)								

表 5-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	AM625, AM625-Q1			AM623			AM620-Q1		
		AM6254	AM6252	AM6251	AM6234	AM6232	AM6231	AM6204	AM6202	AM6201
Flash Subsystem (FSS)(2)	OSPI0/QSPI0	Yes(2)								
Programmable Real-Time Unit Subsystem(3)	PRUSS	2x PRU Cores (Optional)								
Industrial Communication Subsystem Support(4)	PRUSS	No								
Gigabit Ethernet Interface	CPSW3G	Yes								
General-Purpose Timers	TIMER	12 (4 in MCU Channel)								
Enhanced Pulse-Width Modulator Module	EPWM	3								
Enhanced Capture Module	ECAP	3								
Enhanced Quadrature Encoder Pulse Module	EQEP	3								
Universal Asynchronous Receiver and Transmitter	UART	9								
CSI2-RX Controller with DPHY	CSI-RX	1								
USB2.0 Controller with PHY	USB 2.0	2								

(1) For more details about the WKUP_MMR0_JTAG_USER_ID register and DEVICE_ID bit field, see the device TRM.
(2) One flash interface, configured as OSPI0 or QSPI0.
(3) PRU Subsystem (PRUSS) is available when selecting an orderable part number that includes a Features code of C. Refer to Device Naming Convention for definition of feature codes.
(4) Industrial Communication Subsystem support is not available for this family of devices.
(5) Functional Safety is available when selecting an orderable part number that includes a Functional Safety code of F. Refer to Device Naming Convention for definition of feature codes.

5.1 Related Products

Sitara™ processors Broad family of scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara processors have the reliability needed for use in industrial applications.

AM625 Sitara™ processors Human-machine-interaction SoC with Arm® Cortex®-A53-based edge AI and full-HD dual display. The low-cost AM625x Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance and embedded features, such as: dual-display support and 3D graphics acceleration, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

AM623 Sitara™ processors Internet of Things (IoT) and gateway SoC with Arm® Cortex®-A53-based object and gesture recognition. The low-cost AM623x Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance and embedded features, such as: dual-display support, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

Sitara™ AM62x Developer Portal TI provides a wide range of design resource to ease customers' evaluation and development on AM62x platform. You can find the most important design resource in this page, such as evaluation boards/reference designs, demos, software development kit for Linux/Android/Realtime-Linux/FreeRTOS, SDK developer guide, configuration tools, Linux academy.

Sitara™ AM62x processors - Design Galley TI provides many reference designs containing 'building block' solutions to enable customers to rapidly develop their own unique products and solutions. here are 10+ reference designs with demos for analytic, HMI, and connectivity.

6 Terminal Configuration and Functions

6.1 Pin Diagrams

注

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

図 6-1 shows the ball locations for the 425-ball flip chip ball grid array (FCCSP BGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjunction with セクション 6.2.1 through 表 6-74 (*Pin Attributes table and all Signal Descriptions tables, including the Connectivity Requirements table*).

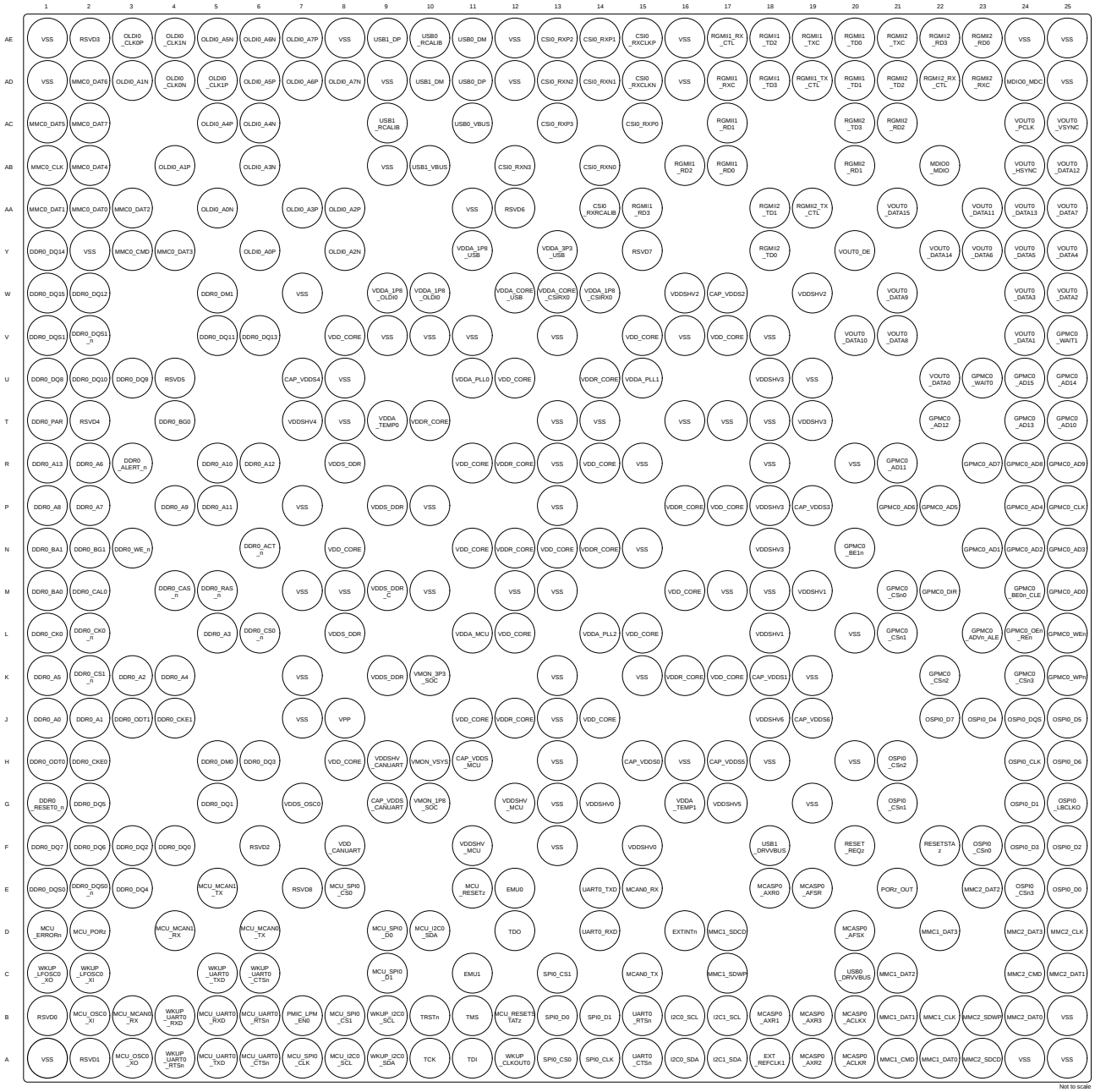


図 6-1. ALW FCCSP Package (Bottom View)

図 6-2 shows the ball locations for the 441-ball flip chip ball grid array (FCBGA BGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjunction with セクション 6.2.1 through 表 6-74 (*Pin Attributes table and all Signal Descriptions tables, including the Connectivity Requirements table*).

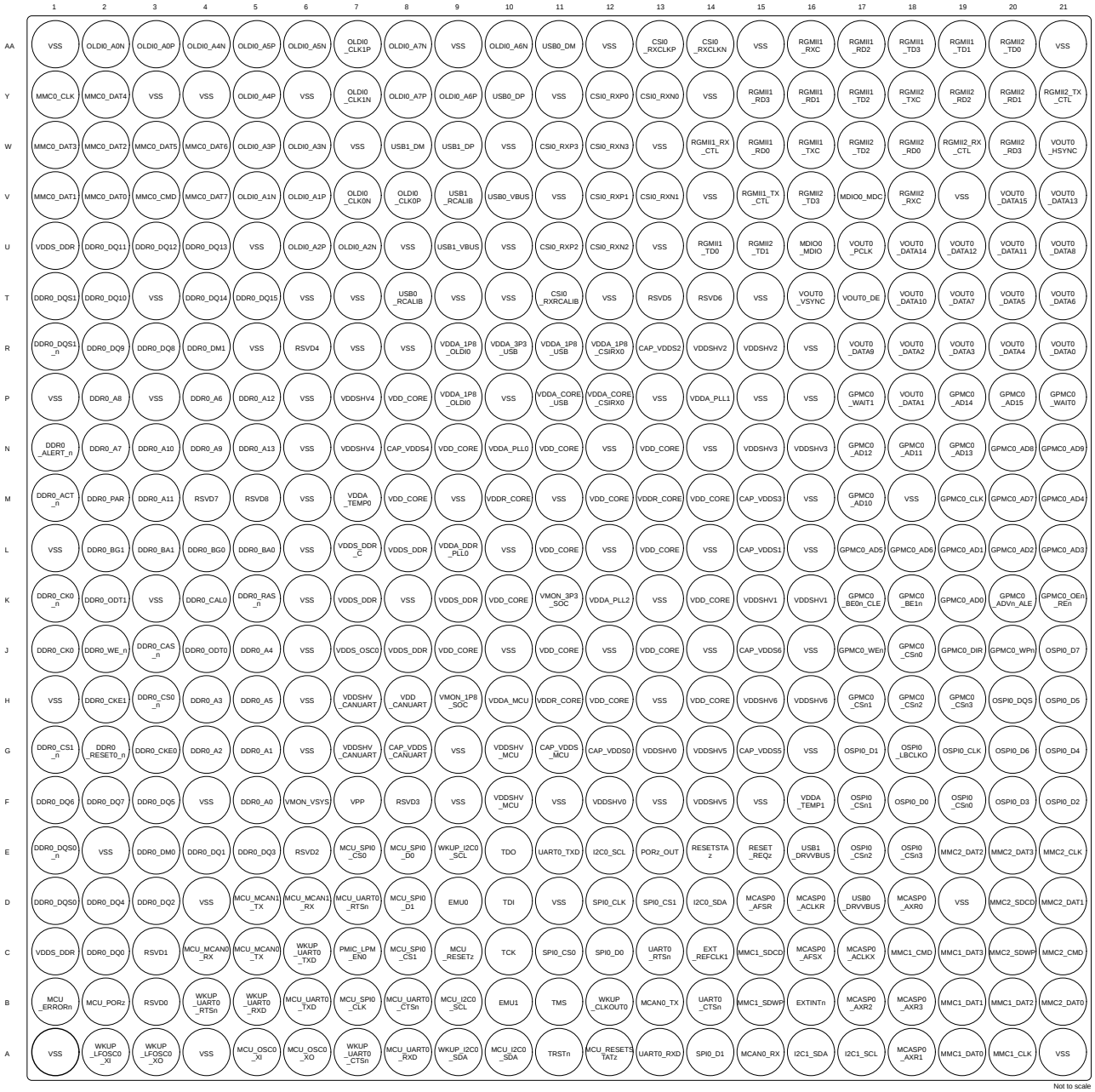


図 6-2. AMC FCBGA Package (Bottom View)

6.2 Pin Attributes

The following list describes the contents of each column in 表 6-1, *Pin Attributes (ALW, AMC Packages)*:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

注

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

表 6-1, *Pin Attributes (ALW, AMC Packages)* only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see the *Pad Configuration Registers* section in the *Device Configuration* chapter of the device TRM. For information associated with peripheral signal multiplexing, see the respective peripheral chapter in the device TRM.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

注

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   d. An empty box means Not Applicable.

注

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor.
6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box means Not Applicable.
7. **BALL STATE DURING RESET RX/TX/PULL:** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - Low: The output buffer is enabled and drives V_{OL}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
8. **BALL STATE AFTER RESET RX/TX/PULL:** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU_PORz is deasserted.

   An empty box means Not Applicable.

10. **I/O OPERATING VOLTAGE**: This column describes I/O operating voltage options of the respective power supply, when applicable.

    An empty box means Not Applicable.

    For more information, see valid operating voltage range(s) defined for each power supply in セクション 7.5, *Recommended Operating Conditions*.

11. **POWER:** The power supply of the associated I/O, when applicable.

    An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box means Not Applicable.

    For more information, see the hysteresis values in セクション 7.8, *Electrical Characteristics*.

13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in セクション 7.8, *Electrical Characteristics*.

14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box means No internal pull.

15. **PADCONFIG Register:**Name of the IO pad configuration register associated with Ball.

16. **PADCONFIG Address:**Physical address of the IO pad configuration register associated with Ball.

表 6-1. Pin Attributes (ALW, AMC Packages)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
H15	G12	CAP_VDDS0	CAP_VDDS0		CAP									
K18	L15	CAP_VDDS1	CAP_VDDS1		CAP									
W17	R13	CAP_VDDS2	CAP_VDDS2		CAP									
P19	M15	CAP_VDDS3	CAP_VDDS3		CAP									
U7	N8	CAP_VDDS4	CAP_VDDS4		CAP									
H17	G15	CAP_VDDS5	CAP_VDDS5		CAP									
J19	J15	CAP_VDDS6	CAP_VDDS6		CAP									
G9	G8	CAP_VDDS_CANUART	CAP_VDDS_CANUART		CAP									
H11	G11	CAP_VDDS_MCU	CAP_VDDS_MCU		CAP									
AD15	AA14	CSI0_RXCLKN	CSI0_RXCLKN		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AE15	AA13	CSI0_RXCLKP	CSI0_RXCLKP		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AA14	T11	CSI0_RXRCALIB	CSI0_RXRCALIB		A					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AB14	Y13	CSI0_RXN0	CSI0_RXN0		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AD14	V13	CSI0_RXN1	CSI0_RXN1		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AD13	U12	CSI0_RXN2	CSI0_RXN2		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AB12	W12	CSI0_RXN3	CSI0_RXN3		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AC15	Y12	CSI0_RXP0	CSI0_RXP0		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AE14	V12	CSI0_RXP1	CSI0_RXP1		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AE13	U11	CSI0_RXP2	CSI0_RXP2		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
AC13	W11	CSI0_RXP3	CSI0_RXP3		I					1.8 V	VDDA_1P8_CSIRX		D-PHY	
N6	M1	DDR0_ACT_n	DDR0_ACT_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R3	N1	DDR0_ALERT_n	DDR0_ALERT_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M4	J3	DDR0_CAS_n	DDR0_CAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T1	M2	DDR0_PAR	DDR0_PAR		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M5	K5	DDR0_RAS_n	DDR0_RAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N3	J2	DDR0_WE_n	DDR0_WE_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J1	F5	DDR0_A0	DDR0_A0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J2	G5	DDR0_A1	DDR0_A1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K3	G4	DDR0_A2	DDR0_A2		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L5	H4	DDR0_A3	DDR0_A3		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
K4	J5	DDR0_A4	DDR0_A4		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K1	H5	DDR0_A5	DDR0_A5		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R2	P4	DDR0_A6	DDR0_A6		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P2	N2	DDR0_A7	DDR0_A7		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P1	P2	DDR0_A8	DDR0_A8		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P4	N4	DDR0_A9	DDR0_A9		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R5	N3	DDR0_A10	DDR0_A10		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P5	M3	DDR0_A11	DDR0_A11		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R6	P5	DDR0_A12	DDR0_A12		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R1	N5	DDR0_A13	DDR0_A13		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M1	L5	DDR0_BA0	DDR0_BA0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N1	L3	DDR0_BA1	DDR0_BA1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T4	L4	DDR0_BG0	DDR0_BG0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N2	L2	DDR0_BG1	DDR0_BG1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M2	K4	DDR0_CAL0	DDR0_CAL0		A					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L1	J1	DDR0_CK0	DDR0_CK0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L2	K1	DDR0_CK0_n	DDR0_CK0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H2	G3	DDR0_CKE0	DDR0_CKE0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J4	H2	DDR0_CKE1	DDR0_CKE1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L6	H3	DDR0_CS0_n	DDR0_CS0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K2	G1	DDR0_CS1_n	DDR0_CS1_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H5	E3	DDR0_DM0	DDR0_DM0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W5	R4	DDR0_DM1	DDR0_DM1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F4	C2	DDR0_DQ0	DDR0_DQ0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G5	E4	DDR0_DQ1	DDR0_DQ1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F3	D3	DDR0_DQ2	DDR0_DQ2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H6	E5	DDR0_DQ3	DDR0_DQ3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E3	D2	DDR0_DQ4	DDR0_DQ4		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G2	F3	DDR0_DQ5	DDR0_DQ5		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F2	F1	DDR0_DQ6	DDR0_DQ6		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F1	F2	DDR0_DQ7	DDR0_DQ7		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U1	R3	DDR0_DQ8	DDR0_DQ8		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U3	R2	DDR0_DQ9	DDR0_DQ9		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U2	T2	DDR0_DQ10	DDR0_DQ10		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V5	U2	DDR0_DQ11	DDR0_DQ11		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W2	U3	DDR0_DQ12	DDR0_DQ12		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V6	U4	DDR0_DQ13	DDR0_DQ13		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y1	T4	DDR0_DQ14	DDR0_DQ14		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W1	T5	DDR0_DQ15	DDR0_DQ15		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E1	D1	DDR0_DQS0	DDR0_DQS0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E2	E1	DDR0_DQS0_n	DDR0_DQS0_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V1	T1	DDR0_DQS1	DDR0_DQS1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V2	R1	DDR0_DQS1_n	DDR0_DQS1_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H1	J4	DDR0_ODT0	DDR0_ODT0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
J3	K2	DDR0_ODT1	DDR0_ODT1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G1	G2	DDR0_RESET0_n	DDR0_RESET0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E12	D9	EMU0 PADCONFIG: MCU_PADCONFIG30 0x04084078	EMU0	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C11	B10	EMU1 PADCONFIG: MCU_PADCONFIG31 0x0408407C	EMU1	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D16	B16	EXTINTn PADCONFIG: PADCONFIG125 0x000F41F4	EXTINTn	0	I	1	Off / Off / NA	Off / Off / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
			GPIO1_31	7	IOD	pad								
A18	C14	EXT_REFCLK1 PADCONFIG: PADCONFIG124 0x000F41F0	EXT_REFCLK1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SYNC1_OUT	1	O									
			SPI2_CS3	2	IO	1								
			SYSCLKOUT0	3	O									
			TIMER_IO4	4	IO	0								
			CLKOUT0	5	O									
			CP_GEMAC_CPTS0_RFT_CLK	6	I	0								
			GPIO1_30	7	IO	pad								
			ECAP0_IN_APWM_OUT	8	IO	0								
L23	K20	GPMC0_ADVn_ALE PADCONFIG: PADCONFIG33 0x000F4084	GPMC0_ADVn_ALE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_AXR2	2	IO	0								
			PR0_PRU0_GPO9	4	IO	0								
			PR0_PRU0_GPI9	5	I	0								
			TRC_DATA7	6	O									
			GPIO0_32	7	IO	pad								
P25	M19	GPMC0_CLK PADCONFIG: PADCONFIG31 0x000F407C	GPMC0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_AXR3	2	IO	0								
			GPMC0_FCLK_MUX	3	O									
			PR0_PRU0_GPO8	4	IO	0								
			PR0_PRU0_GPI8	5	I	0								
			TRC_DATA6	6	O									
			GPIO0_31	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
M22	J19	GPMC0_DIR PADCONFIG: PADCONFIG41 0x000F40A4	GPMC0_DIR	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_ECAP0_IN_APWM_OUT	1	IO	0								
			MCASP2_AXR13	3	IO	0								
			PR0_PRU0_GPO16	4	IO	0								
			PR0_PRU0_GPI16	5	I	0								
			TRC_DATA14	6	O									
			GPIO0_40	7	IO	pad								
			EQEP2_S	8	IO	0								
L24	K21	GPMC0_OEn_REn PADCONFIG: PADCONFIG34 0x000F4088	GPMC0_OEn_REn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_AXR1	2	IO	0								
			PR0_PRU0_GPO10	4	IO	0								
			PR0_PRU0_GPI10	5	I	0								
			TRC_DATA8	6	O									
			GPIO0_33	7	IO	pad								
L25	J17	GPMC0_WEn PADCONFIG: PADCONFIG35 0x000F408C	GPMC0_WEn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_AXR0	2	IO	0								
			PR0_PRU0_GPO11	4	IO	0								
			PR0_PRU0_GPI11	5	I	0								
			TRC_DATA9	6	O									
			GPIO0_34	7	IO	pad								
K25	J20	GPMC0_WPn PADCONFIG: PADCONFIG40 0x000F40A0	GPMC0_WPn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			AUDIO_EXT_REFCLK1	1	IO	0								
			GPMC0_A22	2	OZ									
			UART6_TXD	3	O									
			PR0_PRU0_GPO15	4	IO	0								
			PR0_PRU0_GPI15	5	I	0								
			TRC_DATA13	6	O									
			GPIO0_39	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
M25	K19	GPMC0_AD0 PADCONFIG: PADCONFIG15 0x000F403C	GPMC0_AD0	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO8	1	O									
			PR0_PRU1_GPI8	2	I	0								
			MCASP2_AXR4	3	IO	0								
			PR0_PRU0_GPO0	4	IO	0								
			PR0_PRU0_GPI0	5	I	0								
			TRC_CLK	6	O									
			GPIO0_15	7	IO	pad								
			BOOTMODE00	Bootstrap	I									
N23	L19	GPMC0_AD1 PADCONFIG: PADCONFIG16 0x000F4040	GPMC0_AD1	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO9	1	O									
			PR0_PRU1_GPI9	2	I	0								
			MCASP2_AXR5	3	IO	0								
			PR0_PRU0_GPO1	4	IO	0								
			PR0_PRU0_GPI1	5	I	0								
			TRC_CTL	6	O									
			GPIO0_16	7	IO	pad								
			BOOTMODE01	Bootstrap	I									
N24	L20	GPMC0_AD2 PADCONFIG: PADCONFIG17 0x000F4044	GPMC0_AD2	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO10	1	O									
			PR0_PRU1_GPI10	2	I	0								
			MCASP2_AXR6	3	IO	0								
			PR0_PRU0_GPO2	4	IO	0								
			PR0_PRU0_GPI2	5	I	0								
			TRC_DATA0	6	O									
			GPIO0_17	7	IO	pad								
			BOOTMODE02	Bootstrap	I									
N25	L21	GPMC0_AD3 PADCONFIG: PADCONFIG18 0x000F4048	GPMC0_AD3	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO11	1	O									
			PR0_PRU1_GPI11	2	I	0								
			MCASP2_AXR7	3	IO	0								
			PR0_PRU0_GPO3	4	IO	0								
			PR0_PRU0_GPI3	5	I	0								
			TRC_DATA1	6	O									
			GPIO0_18	7	IO	pad								
			BOOTMODE03	Bootstrap	I									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
P24	M21	GPMC0_AD4 PADCONFIG: PADCONFIG19 0x000F404C	GPMC0_AD4	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO12	1	O									
			PR0_PRU1_GPI12	2	I	0								
			MCASP2_AXR8	3	IO	0								
			PR0_PRU0_GPO4	4	IO	0								
			PR0_PRU0_GPI4	5	I	0								
			TRC_DATA2	6	O									
			GPIO0_19	7	IO	pad								
			BOOTMODE04	Bootstrap	I									
P22	L17	GPMC0_AD5 PADCONFIG: PADCONFIG20 0x000F4050	GPMC0_AD5	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO13	1	O									
			PR0_PRU1_GPI13	2	I	0								
			MCASP2_AXR9	3	IO	0								
			PR0_PRU0_GPO5	4	IO	0								
			PR0_PRU0_GPI5	5	I	0								
			TRC_DATA3	6	O									
			GPIO0_20	7	IO	pad								
			BOOTMODE05	Bootstrap	I									
P21	L18	GPMC0_AD6 PADCONFIG: PADCONFIG21 0x000F4054	GPMC0_AD6	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO14	1	O									
			PR0_PRU1_GPI14	2	I	0								
			MCASP2_AXR10	3	IO	0								
			PR0_PRU0_GPO6	4	IO	0								
			PR0_PRU0_GPI6	5	I	0								
			TRC_DATA4	6	O									
			GPIO0_21	7	IO	pad								
			BOOTMODE06	Bootstrap	I									
R23	M20	GPMC0_AD7 PADCONFIG: PADCONFIG22 0x000F4058	GPMC0_AD7	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO15	1	O									
			PR0_PRU1_GPI15	2	I	0								
			MCASP2_AXR11	3	IO	0								
			PR0_PRU0_GPO7	4	IO	0								
			PR0_PRU0_GPI7	5	I	0								
			TRC_DATA5	6	O									
			GPIO0_22	7	IO	pad								
			BOOTMODE07	Bootstrap	I									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R24	N20	GPMC0_AD8 PADCONFIG: PADCONFIG23 0x000F405C	GPMC0_AD8	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA16	1	O									
			UART2_RXD	2	I	1								
			MCASP2_AXR0	3	IO	0								
			PR0_PRU1_GPO0	4	O									
			PR0_PRU1_GPI0	5	I	0								
			GPIO0_23	7	IO	pad								
			BOOTMODE08	Bootstrap	I									
R25	N21	GPMC0_AD9 PADCONFIG: PADCONFIG24 0x000F4060	GPMC0_AD9	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA17	1	O									
			UART2_TXD	2	O									
			MCASP2_AXR1	3	IO	0								
			PR0_PRU1_GPO1	4	O									
			PR0_PRU1_GPI1	5	I	0								
			GPIO0_24	7	IO	pad								
			BOOTMODE09	Bootstrap	I									
T25	M17	GPMC0_AD10 PADCONFIG: PADCONFIG25 0x000F4064	GPMC0_AD10	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA18	1	O									
			UART3_RXD	2	I	1								
			MCASP2_AXR2	3	IO	0								
			PR0_PRU1_GPO2	4	O									
			PR0_PRU1_GPI2	5	I	0								
			GPIO0_25	7	IO	pad								
			OBSCLK0	8	O									
			BOOTMODE10	Bootstrap	I									
R21	N18	GPMC0_AD11 PADCONFIG: PADCONFIG26 0x000F4068	GPMC0_AD11	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA19	1	O									
			UART3_TXD	2	O									
			MCASP2_AXR3	3	IO	0								
			PR0_PRU1_GPO3	4	O									
			PR0_PRU1_GPI3	5	I	0								
			TRC_DATA23	6	O									
			GPIO0_26	7	IO	pad								
			BOOTMODE11	Bootstrap	I									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T22	N17	GPMC0_AD12 PADCONFIG: PADCONFIG27 0x000F406C	GPMC0_AD12	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA20	1	O									
			UART4_RXD	2	I	1								
			MCASP2_AFSX	3	IO	0								
			PR0_PRU0_GPO0	4	IO	0								
			PR0_PRU0_GPI0	5	I	0								
			TRC_DATA22	6	O									
			GPIO0_27	7	IO	pad								
			BOOTMODE12	Bootstrap	I									
T24	N19	GPMC0_AD13 PADCONFIG: PADCONFIG28 0x000F4070	GPMC0_AD13	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA21	1	O									
			UART4_TXD	2	O									
			MCASP2_ACLKX	3	IO	0								
			PR0_PRU0_GPO1	4	IO	0								
			PR0_PRU0_GPI1	5	I	0								
			TRC_DATA21	6	O									
			GPIO0_28	7	IO	pad								
			BOOTMODE13	Bootstrap	I									
U25	P19	GPMC0_AD14 PADCONFIG: PADCONFIG29 0x000F4074	GPMC0_AD14	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA22	1	O									
			UART5_RXD	2	I	1								
			MCASP2_AFSR	3	IO	0								
			PR0_PRU0_GPO2	4	IO	0								
			PR0_PRU0_GPI2	5	I	0								
			TRC_DATA20	6	O									
			GPIO0_29	7	IO	pad								
			UART2_CTSn	8	I	1								
			BOOTMODE14	Bootstrap	I									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U24	P20	GPMC0_AD15 PADCONFIG: PADCONFIG30 0x000F4078	GPMC0_AD15	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_DATA23	1	O									
			UART5_TXD	2	O									
			MCASP2_ACLKR	3	IO	0								
			PR0_PRU0_GPO3	4	IO	0								
			PR0_PRU0_GPI3	5	I	0								
			TRC_DATA19	6	O									
			GPIO0_30	7	IO	pad								
			UART2_RTSn	8	O									
			BOOTMODE15	Bootstrap	I									
M24	K17	GPMC0_BE0n_CLE PADCONFIG: PADCONFIG36 0x000F4090	GPMC0_BE0n_CLE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_ACLKX	2	IO	0								
			PR0_PRU0_GPO12	4	IO	0								
			PR0_PRU0_GPI12	5	I	0								
			TRC_DATA10	6	O									
			GPIO0_35	7	IO	pad								
N20	K18	GPMC0_BE1n PADCONFIG: PADCONFIG37 0x000F4094	GPMC0_BE1n	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP2_AXR12	3	IO	0								
			PR0_PRU0_GPO13	4	IO	0								
			PR0_PRU0_GPI13	5	I	0								
			TRC_DATA11	6	O									
			GPIO0_36	7	IO	pad								
M21	J18	GPMC0_CSn0 PADCONFIG: PADCONFIG42 0x000F40A8	GPMC0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP2_AXR14	3	IO	0								
			PR0_PRU0_GPO17	4	IO	0								
			PR0_PRU0_GPI17	5	I	0								
			TRC_DATA15	6	O									
			GPIO0_41	7	IO	pad								
L21	H17	GPMC0_CSn1 PADCONFIG: PADCONFIG43 0x000F40AC	GPMC0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			PR0_PRU1_GPO16	1	O									
			PR0_PRU1_GPI16	2	I	0								
			MCASP2_AXR15	3	IO	0								
			PR0_PRU0_GPO18	4	IO	0								
			PR0_PRU0_GPI18	5	I	0								
			TRC_DATA16	6	O									
			GPIO0_42	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
K22	H18	GPMC0_CSn2 PADCONFIG: PADCONFIG44 0x000F40B0	GPMC0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			I2C2_SCL	1	IOD	1								
			MCASP1_AXR4	2	IO	0								
			UART4_RXD	3	I	1								
			PR0_PRU0_GPO19	4	IO	0								
			PR0_PRU0_GPI19	5	I	0								
			TRC_DATA17	6	O									
			GPIO0_43	7	IO	pad								
			MCASP1_AFSR	8	IO	0								
K24	H19	GPMC0_CSn3 PADCONFIG: PADCONFIG45 0x000F40B4	GPMC0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			I2C2_SDA	1	IOD	1								
			GPMC0_A20	2	OZ									
			UART4_TXD	3	O									
			MCASP1_AXR5	4	IO	0								
			TRC_DATA18	6	O									
			GPIO0_44	7	IO	pad								
			MCASP1_ACLKR	8	IO	0								
U23	P21	GPMC0_WAIT0 PADCONFIG: PADCONFIG38 0x000F4098	GPMC0_WAIT0	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			MCASP1_AFSX	2	IO	0								
			PR0_PRU0_GPO14	4	IO	0								
			PR0_PRU0_GPI14	5	I	0								
			TRC_DATA12	6	O									
			GPIO0_37	7	IO	pad								
V25	P17	GPMC0_WAIT1 PADCONFIG: PADCONFIG39 0x000F409C	GPMC0_WAIT1	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			VOUT0_EXTPCLKIN	1	I	0								
			GPMC0_A21	2	OZ									
			UART6_RXD	3	I	1								
			GPIO0_38	7	IO	pad								
			EQEP2_I	8	IO	0								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B16	E12	I2C0_SCL PADCONFIG: PADCONFIG120 0x000F41E0	I2C0_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			PR0_IEP0_EDIO_DATA_IN_OUT30	1	IO	0								
			SYNC0_OUT	2	O									
			OBSCLK0	3	O									
			UART1_DCDn	4	I	1								
			EQEP2_A	5	I	0								
			EHRPWM_SOCA	6	O									
			GPIO1_26	7	IO	pad								
			ECAP1_IN_APWM_OUT	8	IO	0								
			SPI2_CS0	9	IO	1								
A16	D14	I2C0_SDA PADCONFIG: PADCONFIG121 0x000F41E4	I2C0_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			PR0_IEP0_EDIO_DATA_IN_OUT31	1	IO	0								
			SPI2_CS2	2	IO	1								
			TIMER_IO5	3	IO	0								
			UART1_DSRn	4	I	1								
			EQEP2_B	5	I	0								
			EHRPWM_SOCB	6	O									
			GPIO1_27	7	IO	pad								
			ECAP2_IN_APWM_OUT	8	IO	0								
B17	A17	I2C1_SCL PADCONFIG: PADCONFIG122 0x000F41E8	I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART1_RXD	1	I	1								
			TIMER_IO0	2	IO	0								
			SPI2_CS1	3	IO	1								
			EHRPWM0_SYNCI	4	I	0								
			GPIO1_28	7	IO	pad								
			EHRPWM2_A	8	IO	0								
			MMC2_SDCD	9	I	1								
A17	A16	I2C1_SDA PADCONFIG: PADCONFIG123 0x000F41EC	I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART1_TXD	1	O									
			TIMER_IO1	2	IO	0								
			SPI2_CLK	3	IO	0								
			EHRPWM0_SYNCO	4	O									
			GPIO1_29	7	IO	pad								
			EHRPWM2_B	8	IO	0								
			MMC2_SDWP	9	I	1								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E15	A15	MCAN0_RX PADCONFIG: PADCONFIG119 0x000F41DC	MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART5_TXD	1	O									
			TIMER_IO3	2	IO	0								
			SYNC3_OUT	3	O									
			UART1_RIn	4	I	1								
			EQEP2_S	5	IO	0								
			PR0_UART0_TXD	6	O									
			GPIO1_25	7	IO	pad								
			MCASP2_AXR1	8	IO	0								
			EHRPWM_TZn_IN4	9	I	0								
C15	B13	MCAN0_TX PADCONFIG: PADCONFIG118 0x000F41D8	MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART5_RXD	1	I	1								
			TIMER_IO2	2	IO	0								
			SYNC2_OUT	3	O									
			UART1_DTRn	4	O									
			EQEP2_I	5	IO	0								
			PR0_UART0_RXD	6	I	1								
			GPIO1_24	7	IO	pad								
			MCASP2_AXR0	8	IO	0								
			EHRPWM_TZn_IN3	9	I	0								
A20	D16	MCASP0_ACLKR PADCONFIG: PADCONFIG108 0x000F41B0	MCASP0_ACLKR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_CLK	1	IO	0								
			UART1_TXD	2	O									
			EHRPWM0_B	6	IO	0								
			GPIO1_14	7	IO	pad								
			EQEP1_I	8	IO	0								
B20	C17	MCASP0_ACLKX PADCONFIG: PADCONFIG105 0x000F41A4	MCASP0_ACLKX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_CS1	1	IO	1								
			ECAP2_IN_APWM_OUT	2	IO	0								
			GPIO1_11	7	IO	pad								
			EQEP1_A	8	I	0								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E19	D15	MCASP0_AFSR PADCONFIG: PADCONFIG107 0x000F41AC	MCASP0_AFSR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_CS0	1	IO	1								
			UART1_RXD	2	I	1								
			EHRPWM0_A	6	IO	0								
			GPIO1_13	7	IO	pad								
			EQEP1_S	8	IO	0								
D20	C16	MCASP0_AFSX PADCONFIG: PADCONFIG106 0x000F41A8	MCASP0_AFSX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_CS3	1	IO	1								
			AUDIO_EXT_REFCLK1	2	IO	0								
			GPIO1_12	7	IO	pad								
			EQEP1_B	8	I	0								
E18	D18	MCASP0_AXR0 PADCONFIG: PADCONFIG104 0x000F41A0	MCASP0_AXR0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			PR0_ECAP0_IN_APWM_OUT	1	IO	0								
			AUDIO_EXT_REFCLK0	2	IO	0								
			PR0_UART0_TXD	5	O									
			EHRPWM1_B	6	IO	0								
			GPIO1_10	7	IO	pad								
			EQEP0_I	8	IO	0								
B18	A18	MCASP0_AXR1 PADCONFIG: PADCONFIG103 0x000F419C	MCASP0_AXR1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_CS2	1	IO	1								
			ECAP1_IN_APWM_OUT	2	IO	0								
			PR0_UART0_RXD	5	I	1								
			EHRPWM1_A	6	IO	0								
			GPIO1_9	7	IO	pad								
			EQEP0_S	8	IO	0								
A19	B17	MCASP0_AXR2 PADCONFIG: PADCONFIG102 0x000F4198	MCASP0_AXR2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_D1	1	IO	0								
			UART1_RTSn	2	O									
			UART6_TXD	3	O									
			PR0_IEP0_EDIO_DATA_IN_OUT29	4	IO	0								
			ECAP2_IN_APWM_OUT	5	IO	0								
			PR0_UART0_TXD	6	O									
			GPIO1_8	7	IO	pad								
			EQEP0_B	8	I	0								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B19	B18	MCASP0_AXR3 PADCONFIG: PADCONFIG101 0x000F4194	MCASP0_AXR3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI2_D0	1	IO	0								
			UART1_CTSn	2	I	1								
			UART6_RXD	3	I	1								
			PR0_IEP0_EDIO_DATA_IN_OUT28	4	IO	0								
			ECAP1_IN_APWM_OUT	5	IO	0								
			PR0_UART0_RXD	6	I	1								
			GPIO1_7	7	IO	pad								
			EQEP0_A	8	I	0								
D1	B1	MCU_ERRORn PADCONFIG: MCU_PADCONFIG24 0x04084060	MCU_ERRORn	0	IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC0	Yes	LVCMOS	PU/PD
A8	B9	MCU_I2C0_SCL PADCONFIG: MCU_PADCONFIG17 0x04084044	MCU_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
			MCU_GPIO0_17	7	IOD	pad								
D10	A10	MCU_I2C0_SDA PADCONFIG: MCU_PADCONFIG18 0x04084048	MCU_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
			MCU_GPIO0_18	7	IOD	pad								
B3	C4	MCU_MCAN0_RX PADCONFIG: MCU_PADCONFIG14 0x04084038	MCU_MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_TIMER_IO0	1	IO	0								
			MCU_SPI1_CS3	2	IO	1								
			MCU_GPIO0_14	7	IO	pad								
D6	C5	MCU_MCAN0_TX PADCONFIG: MCU_PADCONFIG13 0x04084034	MCU_MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			WKUP_TIMER_IO0	1	IO	0								
			MCU_SPI0_CS3	2	IO	1								
			MCU_GPIO0_13	7	IO	pad								
D4	D6	MCU_MCAN1_RX PADCONFIG: MCU_PADCONFIG16 0x04084040	MCU_MCAN1_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_TIMER_IO3	1	IO	0								
			MCU_SPI0_CS2	2	IO	1								
			MCU_SPI1_CS2	3	IO	1								
			MCU_SPI1_CLK	4	IO	0								
			MCU_GPIO0_16	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E5	D5	MCU_MCAN1_TX PADCONFIG: MCU_PADCONFIG15 0x0408403C	MCU_MCAN1_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_TIMER_IO2	1	IO	0								
			MCU_SPI1_CS1	3	IO	1								
			MCU_EXT_REFCLK0	4	I	0								
			MCU_GPIO0_15	7	IO	pad								
B2	A5	MCU_OSC0_XI	MCU_OSC0_XI		I					1.8 V	VDDS_OSC0		HFOSC	
A3	A6	MCU_OSC0_XO	MCU_OSC0_XO		O					1.8 V	VDDS_OSC0		HFOSC	
D2	B2	MCU_PORz PADCONFIG: MCU_PADCONFIG22 0x04084058	MCU_PORz	0	I				0	1.8 V	VDDS_OSC0	Yes	FS RESET	
B12	A12	MCU_RESETSTATz PADCONFIG: MCU_PADCONFIG23 0x0408405C	MCU_RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			MCU_GPIO0_21	7	IO	pad								
E11	C9	MCU_RESETz PADCONFIG: MCU_PADCONFIG21 0x04084054	MCU_RESETz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A7	B7	MCU_SPI0_CLK PADCONFIG: MCU_PADCONFIG2 0x04084008	MCU_SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			MCU_GPIO0_2	7	IO	pad								
E8	E7	MCU_SPI0_CS0 PADCONFIG: MCU_PADCONFIG0 0x04084000	MCU_SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			WKUP_TIMER_IO1	4	IO	0								
			MCU_GPIO0_0	7	IO	pad								
B8	C8	MCU_SPI0_CS1 PADCONFIG: MCU_PADCONFIG1 0x04084004	MCU_SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			MCU_OBSCLK0	1	O									
			MCU_SYSCLKOUT0	2	O									
			MCU_EXT_REFCLK0	3	I	0								
			MCU_TIMER_IO1	4	IO	0								
			MCU_GPIO0_1	7	IO	pad								
D9	E8	MCU_SPI0_D0 PADCONFIG: MCU_PADCONFIG3 0x0408400C	MCU_SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			MCU_GPIO0_3	7	IO	pad								
C9	D8	MCU_SPI0_D1 PADCONFIG: MCU_PADCONFIG4 0x04084010	MCU_SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
			MCU_GPIO0_4	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A6	B8	MCU_UART0_CTSn PADCONFIG: MCU_PADCONFIG7 0x0408401C	MCU_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_TIMER_IO0	1	IO	0								
			MCU_SPI1_D0	3	IO	0								
			MCU_GPIO0_7	7	IO	pad								
B6	D7	MCU_UART0_RTSn PADCONFIG: MCU_PADCONFIG8 0x04084020	MCU_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_TIMER_IO1	1	IO	0								
			MCU_SPI1_D1	3	IO	0								
			MCU_GPIO0_8	7	IO	pad								
B5	A8	MCU_UART0_RXD PADCONFIG: MCU_PADCONFIG5 0x04084014	MCU_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_GPIO0_5	7	IO	pad								
A5	B6	MCU_UART0_TXD PADCONFIG: MCU_PADCONFIG6 0x04084018	MCU_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_GPIO0_6	7	IO	pad								
AD24	V17	MDIO0_MDC PADCONFIG: PADCONFIG88 0x000F4160	MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			GPIO0_86	7	IO	pad								
AB22	U16	MDIO0_MDIO PADCONFIG: PADCONFIG87 0x000F415C	MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			GPIO0_85	7	IO	pad								
AB1	Y1	MMC0_CLK PADCONFIG: PADCONFIG134 0x000F4218	MMC0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			I2C3_SCL	1	IOD	1								
			EHRPWM2_A	2	IO	0								
			PR0_PRU1_GPO4	3	O									
			PR0_PRU1_GPI4	4	I	0								
			SPI1_CS1	5	IO	1								
			TIMER_IO4	6	IO	0								
			GPIO1_40	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y3	V3	MMC0_CMD PADCONFIG: PADCONFIG136 0x000F4220	MMC0_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			I2C3_SDA	1	IOD	1								
			EHRPWM2_B	2	IO	0								
			PR0_PRU0_GPO4	3	IO	0								
			PR0_PRU0_GPI4	4	I	0								
			SPI1_CS2	5	IO	1								
			TIMER_IO5	6	IO	0								
			GPIO1_41	7	IO	pad								
B22	A20	MMC1_CLK PADCONFIG: PADCONFIG141 0x000F4234	MMC1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			TIMER_IO4	2	IO	0								
			UART3_RXD	3	I	1								
			GPIO1_46	7	IO	pad								
A21	C18	MMC1_CMD PADCONFIG: PADCONFIG143 0x000F423C	MMC1_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			TIMER_IO5	2	IO	0								
			UART3_TXD	3	O									
			GPIO1_47	7	IO	pad								
D17	C15	MMC1_SDCD PADCONFIG: PADCONFIG144 0x000F4240	MMC1_SDCD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART6_RXD	1	I	1								
			TIMER_IO6	2	IO	0								
			UART3_RTSn	3	O									
			GPIO1_48	7	IO	pad								
C17	B15	MMC1_SDWP PADCONFIG: PADCONFIG145 0x000F4244	MMC1_SDWP	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			UART6_TXD	1	O									
			TIMER_IO7	2	IO	0								
			UART3_CTSn	3	I	1								
			GPIO1_49	7	IO	pad								
D25	E21	MMC2_CLK PADCONFIG: PADCONFIG70 0x000F4118	MMC2_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_ACLKR	1	IO	0								
			MCASP1_AXR5	2	IO	0								
			UART6_RXD	3	I	1								
			GPIO0_69	7	IO	pad								
C24	C21	MMC2_CMD PADCONFIG: PADCONFIG72 0x000F4120	MMC2_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_AFSR	1	IO	0								
			MCASP1_AXR4	2	IO	0								
			UART6_TXD	3	O									
			GPIO0_70	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A23	D20	MMC2_SDCD PADCONFIG: PADCONFIG73 0x000F4124	MMC2_SDCD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
			MCASP1_ACLKX	1	IO	0								
			UART4_RXD	3	I	1								
			GPIO0_71	7	IO	pad								
B23	C20	MMC2_SDWP PADCONFIG: PADCONFIG74 0x000F4128	MMC2_SDWP	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
			MCASP1_AFSX	1	IO	0								
			UART4_TXD	3	O									
			GPIO0_72	7	IO	pad								
AA2	V2	MMC0_DAT0 PADCONFIG: PADCONFIG133 0x000F4214	MMC0_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART3_CTSn	1	I	1								
			EHRPWM_TZn_IN1	2	I	0								
			PR0_PRU0_GPO3	3	IO	0								
			PR0_PRU0_GPI3	4	I	0								
			SPI2_CLK	6	IO	0								
			GPIO1_39	7	IO	pad								
AA1	V1	MMC0_DAT1 PADCONFIG: PADCONFIG132 0x000F4210	MMC0_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART3_RTSn	1	O									
			EHRPWM1_B	2	IO	0								
			PR0_PRU0_GPO2	3	IO	0								
			PR0_PRU0_GPI2	4	I	0								
			SPI1_CS3	5	IO	1								
			SPI2_CS0	6	IO	1								
			GPIO1_38	7	IO	pad								
AA3	W2	MMC0_DAT2 PADCONFIG: PADCONFIG131 0x000F420C	MMC0_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART3_TXD	1	O									
			EHRPWM1_A	2	IO	0								
			PR0_PRU0_GPO1	3	IO	0								
			PR0_PRU0_GPI1	4	I	0								
			SPI1_CLK	5	IO	0								
			TIMER_IO0	6	IO	0								
			GPIO1_37	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y4	W1	MMC0_DAT3 PADCONFIG: PADCONFIG130 0x000F4208	MMC0_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART3_RXD	1	I	1								
			EHRPWM0_B	2	IO	0								
			PR0_PRU0_GPO0	3	IO	0								
			PR0_PRU0_GPI0	4	I	0								
			SPI1_CS0	5	IO	1								
			SPI2_CS2	6	IO	1								
			GPIO1_36	7	IO	pad								
AB2	Y2	MMC0_DAT4 PADCONFIG: PADCONFIG129 0x000F4204	MMC0_DAT4	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART2_CTSn	1	I	1								
			EHRPWM0_A	2	IO	0								
			PR0_PRU1_GPO3	3	O									
			PR0_PRU1_GPI3	4	I	0								
			SPI2_D1	6	IO	0								
			GPIO1_35	7	IO	pad								
AC1	W3	MMC0_DAT5 PADCONFIG: PADCONFIG128 0x000F4200	MMC0_DAT5	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART2_RTSn	1	O									
			EHRPWM_TZn_IN2	2	I	0								
			PR0_PRU1_GPO2	3	O									
			PR0_PRU1_GPI2	4	I	0								
			SPI2_D0	6	IO	0								
			GPIO1_34	7	IO	pad								
AD2	W4	MMC0_DAT6 PADCONFIG: PADCONFIG127 0x000F41FC	MMC0_DAT6	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART2_TXD	1	O									
			EHRPWM0_SYNCO	2	O									
			PR0_PRU1_GPO1	3	O									
			PR0_PRU1_GPI1	4	I	0								
			SPI1_D1	5	IO	0								
			SPI2_CS3	6	IO	1								
			GPIO1_33	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AC2	V4	MMC0_DAT7 PADCONFIG: PADCONFIG126 0x000F41F8	MMC0_DAT7	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	SDIO	PU/PD
			UART2_RXD	1	I	1								
			EHRPWM0_SYNCI	2	I	0								
			PR0_PRU1_GPO0	3	O									
			PR0_PRU1_GPI0	4	I	0								
			SPI1_D0	5	IO	0								
			SPI2_CS1	6	IO	1								
			GPIO1_32	7	IO	pad								
A22	A19	MMC1_DAT0 PADCONFIG: PADCONFIG140 0x000F4230	MMC1_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
			TIMER_IO3	2	IO	0								
			UART2_CTSn	3	I	1								
			ECAP2_IN_APWM_OUT	4	IO	0								
			GPIO1_45	7	IO	pad								
B21	B19	MMC1_DAT1 PADCONFIG: PADCONFIG139 0x000F422C	MMC1_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
			TIMER_IO2	2	IO	0								
			UART2_RTSn	3	O									
			ECAP1_IN_APWM_OUT	4	IO	0								
			GPIO1_44	7	IO	pad								
C21	B20	MMC1_DAT2 PADCONFIG: PADCONFIG138 0x000F4228	MMC1_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			CP_GEMAC_CPTS0_TS_SYNC	1	O									
			TIMER_IO1	2	IO	0								
			UART2_TXD	3	O									
			GPIO1_43	7	IO	pad								
D22	C19	MMC1_DAT3 PADCONFIG: PADCONFIG137 0x000F4224	MMC1_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
			CP_GEMAC_CPTS0_TS_COMP	1	O									
			TIMER_IO0	2	IO	0								
			UART2_RXD	3	I	1								
			GPIO1_42	7	IO	pad								
B24	B21	MMC2_DAT0 PADCONFIG: PADCONFIG69 0x000F4114	MMC2_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_AXR0	1	IO	0								
			GPIO0_68	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C25	D21	MMC2_DAT1 PADCONFIG: PADCONFIG68 0x000F4110	MMC2_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_AXR1	1	IO	0								
			GPIO0_67	7	IO	pad								
E23	E19	MMC2_DAT2 PADCONFIG: PADCONFIG67 0x000F410C	MMC2_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_AXR2	1	IO	0								
			UART5_TXD	3	O									
			GPIO0_66	7	IO	pad								
D24	E20	MMC2_DAT3 PADCONFIG: PADCONFIG66 0x000F4108	MMC2_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
			MCASP1_AXR3	1	IO	0								
			UART5_RXD	3	I	1								
			GPIO0_65	7	IO	pad								
AA5	AA2	OLDI0_A0N	OLDI0_A0N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
Y6	AA3	OLDI0_A0P	OLDI0_A0P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD3	V5	OLDI0_A1N	OLDI0_A1N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AB4	V6	OLDI0_A1P	OLDI0_A1P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
Y8	U7	OLDI0_A2N	OLDI0_A2N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AA8	U6	OLDI0_A2P	OLDI0_A2P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AB6	W6	OLDI0_A3N	OLDI0_A3N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AA7	W5	OLDI0_A3P	OLDI0_A3P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC6	AA4	OLDI0_A4N	OLDI0_A4N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC5	Y5	OLDI0_A4P	OLDI0_A4P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE5	AA6	OLDI0_A5N	OLDI0_A5N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD6	AA5	OLDI0_A5P	OLDI0_A5P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE6	AA10	OLDI0_A6N	OLDI0_A6N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD7	Y9	OLDI0_A6P	OLDI0_A6P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD8	AA8	OLDI0_A7N	OLDI0_A7N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE7	Y8	OLDI0_A7P	OLDI0_A7P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD4	V7	OLDI0_CLK0N	OLDI0_CLK0N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE3	V8	OLDI0_CLK0P	OLDI0_CLK0P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE4	Y7	OLDI0_CLK1N	OLDI0_CLK1N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD5	AA7	OLDI0_CLK1P	OLDI0_CLK1P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
H24	G19	OSPI0_CLK PADCONFIG: PADCONFIG0 0x000F4000	OSPI0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_0	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
J24	H20	OSPI0_DQS PADCONFIG: PADCONFIG2 0x000F4008	OSPI0_DQS	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			UART5_CTSn	5	I	1								
			GPIO0_2	7	IO	pad								
G25	G18	OSPI0_LBCLKO PADCONFIG: PADCONFIG1 0x000F4004	OSPI0_LBCLKO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			UART5_RTSn	5	O									
			GPIO0_1	7	IO	pad								
F23	F19	OSPI0_CSn0 PADCONFIG: PADCONFIG11 0x000F402C	OSPI0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_11	7	IO	pad								
G21	F17	OSPI0_CSn1 PADCONFIG: PADCONFIG12 0x000F4030	OSPI0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_12	7	IO	pad								
H21	E17	OSPI0_CSn2 PADCONFIG: PADCONFIG13 0x000F4034	OSPI0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			SPI1_CS1	1	IO	1								
			OSPI0_RESET_OUT1	2	O									
			MCASP1_AFSR	3	IO	0								
			MCASP1_AXR2	4	IO	0								
			UART5_RXD	5	I	1								
			GPIO0_13	7	IO	pad								
E24	E18	OSPI0_CSn3 PADCONFIG: PADCONFIG14 0x000F4038	OSPI0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			OSPI0_RESET_OUT0	1	O									
			OSPI0_ECC_FAIL	2	I	1								
			MCASP1_ACLKR	3	IO	0								
			MCASP1_AXR3	4	IO	0								
			UART5_TXD	5	O									
			GPIO0_14	7	IO	pad								
E25	F18	OSPI0_D0 PADCONFIG: PADCONFIG3 0x000F400C	OSPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_3	7	IO	pad								
G24	G17	OSPI0_D1 PADCONFIG: PADCONFIG4 0x000F4010	OSPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_4	7	IO	pad								
F25	F21	OSPI0_D2 PADCONFIG: PADCONFIG5 0x000F4014	OSPI0_D2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_5	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F24	F20	OSPI0_D3 PADCONFIG: PADCONFIG6 0x000F4018	OSPI0_D3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			GPIO0_6	7	IO	pad								
J23	G21	OSPI0_D4 PADCONFIG: PADCONFIG7 0x000F401C	OSPI0_D4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			SPI1_CS0	1	IO	1								
			MCASP1_AXR1	2	IO	0								
			UART6_RXD	3	I	1								
			GPIO0_7	7	IO	pad								
J25	H21	OSPI0_D5 PADCONFIG: PADCONFIG8 0x000F4020	OSPI0_D5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			SPI1_CLK	1	IO	0								
			MCASP1_AXR0	2	IO	0								
			UART6_TXD	3	O									
			GPIO0_8	7	IO	pad								
H25	G20	OSPI0_D6 PADCONFIG: PADCONFIG9 0x000F4024	OSPI0_D6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			SPI1_D0	1	IO	0								
			MCASP1_ACLKX	2	IO	0								
			UART6_RTSn	3	O									
			GPIO0_9	7	IO	pad								
J22	J21	OSPI0_D7 PADCONFIG: PADCONFIG10 0x000F4028	OSPI0_D7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
			SPI1_D1	1	IO	0								
			MCASP1_AFSX	2	IO	0								
			UART6_CTSn	3	I	1								
			GPIO0_10	7	IO	pad								
B7	C7	PMIC_LPM_EN0 PADCONFIG: MCU_PADCONFIG32 0x04084080	PMIC_LPM_EN0	0	O		Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_GPIO0_22	7	IO	pad								
E21	E13	PORz_OUT PADCONFIG: PADCONFIG148 0x000F4250	PORz_OUT	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
F22	E14	RESETSTATz PADCONFIG: PADCONFIG147 0x000F424C	RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
F20	E15	RESET_REQz PADCONFIG: PADCONFIG146 0x000F4248	RESET_REQz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AD17	AA16	RGMII1_RXC PADCONFIG: PADCONFIG82 0x000F4148	RGMII1_RXC	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_REF_CLK	1	I	0								
			PR0_UART0_CTSn	2	I	1								
			GPIO0_80	7	IO	pad								
AE17	W14	RGMII1_RX_CTL PADCONFIG: PADCONFIG81 0x000F4144	RGMII1_RX_CTL	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_RX_ER	1	I	0								
			GPIO0_79	7	IO	pad								
AE19	W16	RGMII1_TXC PADCONFIG: PADCONFIG76 0x000F4130	RGMII1_TXC	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_CRS_DV	1	I	0								
			GPIO0_74	7	IO	pad								
AD19	V15	RGMII1_TX_CTL PADCONFIG: PADCONFIG75 0x000F412C	RGMII1_TX_CTL	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_TX_EN	1	O									
			GPIO0_73	7	IO	pad								
AD23	V18	RGMII2_RXC PADCONFIG: PADCONFIG96 0x000F4180	RGMII2_RXC	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_REF_CLK	1	I	0								
			MCASP2_AXR1	2	IO	0								
			PR0_PRU0_GPO1	3	IO	0								
			PR0_PRU0_GPI1	4	I	0								
			PR0_ECAP0_SYNC_IN	5	I	0								
			GPIO1_2	7	IO	pad								
AD22	W19	RGMII2_RX_CTL PADCONFIG: PADCONFIG95 0x000F417C	RGMII2_RX_CTL	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_RX_ER	1	I	0								
			MCASP2_AXR3	2	IO	0								
			PR0_PRU0_GPO0	3	IO	0								
			PR0_PRU0_GPI0	4	I	0								
			GPIO1_1	7	IO	pad								
AE21	Y18	RGMII2_TXC PADCONFIG: PADCONFIG90 0x000F4168	RGMII2_TXC	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_CRS_DV	1	I	0								
			MCASP2_AXR5	2	IO	0								
			PR0_PRU1_GPO1	3	O									
			PR0_PRU1_GPI1	4	I	0								
			GPIO0_88	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA19	Y21	RGMII2_TX_CTL PADCONFIG: PADCONFIG89 0x000F4164	RGMII2_TX_CTL	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_TX_EN	1	O									
			MCASP2_AXR4	2	IO	0								
			PR0_PRU1_GPO0	3	O									
			PR0_PRU1_GPI0	4	I	0								
			GPIO0_87	7	IO	pad								
AB17	W15	RGMII1_RD0 PADCONFIG: PADCONFIG83 0x000F414C	RGMII1_RD0	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_RXD0	1	I	0								
			GPIO0_81	7	IO	pad								
AC17	Y16	RGMII1_RD1 PADCONFIG: PADCONFIG84 0x000F4150	RGMII1_RD1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_RXD1	1	I	0								
			GPIO0_82	7	IO	pad								
AB16	AA17	RGMII1_RD2 PADCONFIG: PADCONFIG85 0x000F4154	RGMII1_RD2	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			PR0_UART0_RTSn	2	O									
			GPIO0_83	7	IO	pad								
AA15	Y15	RGMII1_RD3 PADCONFIG: PADCONFIG86 0x000F4158	RGMII1_RD3	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			GPIO0_84	7	IO	pad								
AE20	U14	RGMII1_TD0 PADCONFIG: PADCONFIG77 0x000F4134	RGMII1_TD0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_TXD0	1	O									
			GPIO0_75	7	IO	pad								
AD20	AA19	RGMII1_TD1 PADCONFIG: PADCONFIG78 0x000F4138	RGMII1_TD1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII1_TXD1	1	O									
			GPIO0_76	7	IO	pad								
AE18	Y17	RGMII1_TD2 PADCONFIG: PADCONFIG79 0x000F413C	RGMII1_TD2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			PR0_UART0_RXD	2	I	1								
			GPIO0_77	7	IO	pad								
AD18	AA18	RGMII1_TD3 PADCONFIG: PADCONFIG80 0x000F4140	RGMII1_TD3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			PR0_UART0_TXD	2	O									
			GPIO0_78	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AE23	W18	RGMII2_RD0 PADCONFIG: PADCONFIG97 0x000F4184	RGMII2_RD0	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_RXD0	1	I	0								
			MCASP2_AXR2	2	IO	0								
			PR0_PRU0_GPO2	3	IO	0								
			PR0_PRU0_GPI2	4	I	0								
			PR0_UART0_RTSn	6	O									
			GPIO1_3	7	IO	pad								
AB20	Y20	RGMII2_RD1 PADCONFIG: PADCONFIG98 0x000F4188	RGMII2_RD1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_RXD1	1	I	0								
			MCASP2_AFSR	2	IO	0								
			PR0_PRU0_GPO3	3	IO	0								
			PR0_PRU0_GPI3	4	I	0								
			MCASP2_AXR7	5	IO	0								
			GPIO1_4	7	IO	pad								
AC21	Y19	RGMII2_RD2 PADCONFIG: PADCONFIG99 0x000F418C	RGMII2_RD2	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			MCASP2_AXR0	2	IO	0								
			PR0_PRU0_GPO4	3	IO	0								
			PR0_PRU0_GPI4	4	I	0								
			PR0_UART0_RXD	5	I	1								
			GPIO1_5	7	IO	pad								
			EQEP2_A	8	I	0								
AE22	W20	RGMII2_RD3 PADCONFIG: PADCONFIG100 0x000F4190	RGMII2_RD3	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			AUDIO_EXT_REFCLK0	2	IO	0								
			PR0_PRU0_GPO16	3	IO	0								
			PR0_PRU0_GPI16	4	I	0								
			PR0_UART0_TXD	5	O									
			GPIO1_6	7	IO	pad								
			EQEP2_B	8	I	0								
Y18	AA20	RGMII2_TD0 PADCONFIG: PADCONFIG91 0x000F416C	RGMII2_TD0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_TXD0	1	O									
			MCASP2_AXR6	2	IO	0								
			PR0_PRU1_GPO2	3	O									
			PR0_PRU1_GPI2	4	I	0								
			GPIO0_89	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA18	U15	RGMII2_TD1 PADCONFIG: PADCONFIG92 0x000F4170	RGMII2_TD1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			RMII2_TXD1	1	O									
			MCASP2_ACLKR	2	IO	0								
			PR0_PRU1_GPO3	3	O									
			PR0_PRU1_GPI3	4	I	0								
			MCASP2_AXR8	5	IO	0								
			GPIO0_90	7	IO	pad								
AD21	W17	RGMII2_TD2 PADCONFIG: PADCONFIG93 0x000F4174	RGMII2_TD2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			MCASP2_AFSX	2	IO	0								
			PR0_PRU1_GPO4	3	O									
			PR0_PRU1_GPI4	4	I	0								
			PR0_ECAP0_IN_APWM_OUT	5	IO	0								
			GPIO0_91	7	IO	pad								
			EQEP2_I	8	IO	0								
AC20	V16	RGMII2_TD3 PADCONFIG: PADCONFIG94 0x000F4178	RGMII2_TD3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
			MCASP2_ACLKX	2	IO	0								
			PR0_PRU1_GPO16	3	O									
			PR0_PRU1_GPI16	4	I	0								
			PR0_ECAP0_SYNC_OUT	5	O									
			PR0_UART0_CTSn	6	I	1								
			GPIO1_0	7	IO	pad								
			EQEP2_S	8	IO	0								
B1	B3	RSVD0	RSVD0		N/A									
A2	C3	RSVD1	RSVD1		N/A									
F6	E6	RSVD2	RSVD2		N/A									
AE2	F8	RSVD3	RSVD3		N/A									
T2	R6	RSVD4	RSVD4		N/A									
U4	T13	RSVD5	RSVD5		N/A									
AA12	T14	RSVD6	RSVD6		N/A									
Y15	M4	RSVD7	RSVD7		N/A									
E7	M5	RSVD8	RSVD8		N/A									
A14	D12	SPI0_CLK PADCONFIG: PADCONFIG111 0x000F41BC	SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			CP_GEMAC_CPTS0_TS_SYNC	1	O									
			EHRPWM1_A	2	IO	0								
			GPIO1_17	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A13	C11	SPI0_CS0 PADCONFIG: PADCONFIG109 0x000F41B4	SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			EHRPWM0_A	2	IO	0								
			PR0_ECAP0_SYNC_IN	6	I	0								
			GPIO1_15	7	IO	pad								
C13	D13	SPI0_CS1 PADCONFIG: PADCONFIG110 0x000F41B8	SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			CP_GEMAC_CPTS0_TS_COMP	1	O									
			EHRPWM0_B	2	IO	0								
			ECAP0_IN_APWM_OUT	3	IO	0								
			GPIO1_16	7	IO	pad								
			EHRPWM_TZn_IN5	9	I	0								
B13	C12	SPI0_D0 PADCONFIG: PADCONFIG112 0x000F41C0	SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
			EHRPWM1_B	2	IO	0								
			GPIO1_18	7	IO	pad								
B14	A14	SPI0_D1 PADCONFIG: PADCONFIG113 0x000F41C4	SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
			EHRPWM_TZn_IN0	2	I	0								
			GPIO1_19	7	IO	pad								
A10	C10	TCK PADCONFIG: MCU_PADCONFIG25 0x04084064	TCK	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A11	D10	TDI PADCONFIG: MCU_PADCONFIG27 0x0408406C	TDI	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D12	E10	TDO PADCONFIG: MCU_PADCONFIG28 0x04084070	TDO	0	OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B11	B11	TMS PADCONFIG: MCU_PADCONFIG29 0x04084074	TMS	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B10	A11	TRSTn PADCONFIG: MCU_PADCONFIG26 0x04084068	TRSTn	0	I		On / Off / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A15	B14	UART0_CTSn PADCONFIG: PADCONFIG116 0x000F41D0	UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI0_CS2	1	IO	1								
			I2C3_SCL	2	IOD	1								
			UART2_RXD	3	I	1								
			TIMER_IO6	4	IO	0								
			AUDIO_EXT_REFCLK0	5	IO	0								
			PR0_ECAP0_SYNC_OUT	6	O									
			GPIO1_22	7	IO	pad								
			MCASP2_AFSX	8	IO	0								
			MMC2_SDCD	9	I	1								
B15	C13	UART0_RTSn PADCONFIG: PADCONFIG117 0x000F41D4	UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			SPI0_CS3	1	IO	1								
			I2C3_SDA	2	IOD	1								
			UART2_TXD	3	O									
			TIMER_IO7	4	IO	0								
			AUDIO_EXT_REFCLK1	5	IO	0								
			PR0_ECAP0_IN_APWM_OUT	6	IO	0								
			GPIO1_23	7	IO	pad								
			MCASP2_ACLKX	8	IO	0								
			MMC2_SDWP	9	I	1								
D14	A13	UART0_RXD PADCONFIG: PADCONFIG114 0x000F41C8	UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			ECAP1_IN_APWM_OUT	1	IO	0								
			SPI2_D0	2	IO	0								
			EHRPWM2_A	3	IO	0								
			GPIO1_20	7	IO	pad								
E14	E11	UART0_TXD PADCONFIG: PADCONFIG115 0x000F41CC	UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
			ECAP2_IN_APWM_OUT	1	IO	0								
			SPI2_D1	2	IO	0								
			EHRPWM2_B	3	IO	0								
			GPIO1_21	7	IO	pad								
AE11	AA11	USB0_DM	USB0_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AD11	Y10	USB0_DP	USB0_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C20	D17	USB0_DRVVBUS	USB0_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		PADCONFIG: PADCONFIG149 0x000F4254	GPIO1_50	7	IO	pad								
AE10	T8	USB0_RCALIB	USB0_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AC11	V10	USB0_VBUS	USB0_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AD10	W8	USB1_DM	USB1_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AE9	W9	USB1_DP	USB1_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
F18	E16	USB1_DRVVBUS	USB1_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		PADCONFIG: PADCONFIG150 0x000F4258	GPIO1_51	7	IO	pad								
AC9	V9	USB1_RCALIB	USB1_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AB10	U9	USB1_VBUS	USB1_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
Y11	R11	VDDA_1P8_USB	VDDA_1P8_USB		PWR									
W14	R12	VDDA_1P8_CSIRX0	VDDA_1P8_CSIRX0		PWR									
W10, W9	P9, R9	VDDA_1P8_OLDI0	VDDA_1P8_OLDI0		PWR									
Y13	R10	VDDA_3P3_USB	VDDA_3P3_USB		PWR									
W13	P12	VDDA_CORE_CSIRX0	VDDA_CORE_CSIRX0		PWR									
W12	P11	VDDA_CORE_USB	VDDA_CORE_USB		PWR									
	L9	VDDA_DDR_PLL0	VDDA_DDR_PLL0		PWR									
L11	H10	VDDA_MCU	VDDA_MCU		PWR									
U11	N10	VDDA_PLL0	VDDA_PLL0		PWR									
U15	P14	VDDA_PLL1	VDDA_PLL1		PWR									
L14	K12	VDDA_PLL2	VDDA_PLL2		PWR									
T9	M7	VDDA_TEMP0	VDDA_TEMP0		PWR									
G16	F16	VDDA_TEMP1	VDDA_TEMP1		PWR									
J12, K16, N12, N14, P16, R12, T10, U14	H11, M10, M13	VDDR_CORE	VDDR_CORE		PWR									
F15, G14	F12, G13	VDDSHV0	VDDSHV0		PWR									
L18, M19	K15, K16	VDDSHV1	VDDSHV1		PWR									
W16, W19	R14, R15	VDDSHV2	VDDSHV2		PWR									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N18, P18, T19, U18	N15, N16	VDDSHV3	VDDSHV3		PWR									
T7	N7, P7	VDDSHV4	VDDSHV4		PWR									
G17	F14, G14	VDDSHV5	VDDSHV5		PWR									
J18	H15, H16	VDDSHV6	VDDSHV6		PWR									
H9	G7, H7	VDDSHV_CANUART	VDDSHV_CANUART		PWR									
F11, G12	F10, G10	VDDSHV_MCU	VDDSHV_MCU		PWR									
K9, L8, P9, R8	C1, J8, K7, K9, L8, U1	VDDS_DDR	VDDS_DDR		PWR									
M9	L7	VDDS_DDR_C	VDDS_DDR_C		PWR									
G7	J7	VDDS_OSC0	VDDS_OSC0		PWR									
F8	H8	VDD_CANUART	VDD_CANUART		PWR									
H8, J11, J14, K17, L12, L15, M16, N11, N13, N8, P17, R11, R14, U12, V15, V17, V8	H12, H14, J11, J13, J9, K10, K14, L11, L13, M12, M14, M8, N11, N13, N9, P8	VDD_CORE	VDD_CORE		PWR									
G10	H9	VMON_1P8_SOC	VMON_1P8_SOC		A									
K10	K11	VMON_3P3_SOC	VMON_3P3_SOC		A									
H10	F6	VMON_VSYS	VMON_VSYS		A									
Y20	T17	VOUT0_DE PADCONFIG: PADCONFIG63 0x000F40FC	VOUT0_DE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A17	1	OZ									
			PR0_PRU1_GPO17	2	O									
			PR0_PRU1_GPI17	3	I	0								
			UART3_CTSn	4	I	1								
			PR0_PRU0_GPO7	5	IO	0								
			PR0_PRU0_GPI7	6	I	0								
			GPIO0_62	7	IO	pad								
AB24	W21	VOUT0_HSYNC PADCONFIG: PADCONFIG62 0x000F40F8	VOUT0_HSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A16	1	OZ									
			PR0_PRU1_GPO15	2	O									
			PR0_PRU1_GPI15	3	I	0								
			UART3_RTSn	4	O									
			PR0_PRU0_GPO6	5	IO	0								
			PR0_PRU0_GPI6	6	I	0								
			GPIO0_61	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AC24	U17	VOUT0_PCLK PADCONFIG: PADCONFIG65 0x000F4104	VOUT0_PCLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A19	1	OZ									
			PR0_PRU1_GPO19	2	O									
			PR0_PRU1_GPI19	3	I	0								
			UART2_CTSn	4	I	1								
			PR0_PRU0_GPO19	5	IO	0								
			PR0_PRU0_GPI19	6	I	0								
			GPIO0_64	7	IO	pad								
			PR0_ECAP0_IN_APWM_OUT	8	IO	0								
AC25	T16	VOUT0_VSYNC PADCONFIG: PADCONFIG64 0x000F4100	VOUT0_VSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A18	1	OZ									
			PR0_PRU1_GPO18	2	O									
			PR0_PRU1_GPI18	3	I	0								
			UART2_RTSn	4	O									
			PR0_PRU0_GPO18	5	IO	0								
			PR0_PRU0_GPI18	6	I	0								
			GPIO0_63	7	IO	pad								
U22	R21	VOUT0_DATA0 PADCONFIG: PADCONFIG46 0x000F40B8	VOUT0_DATA0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A0	1	OZ									
			PR0_PRU1_GPO0	2	O									
			PR0_PRU1_GPI0	3	I	0								
			UART2_RXD	4	I	1								
			PR0_PRU0_GPO8	5	IO	0								
			PR0_PRU0_GPI8	6	I	0								
			GPIO0_45	7	IO	pad								
V24	P18	VOUT0_DATA1 PADCONFIG: PADCONFIG47 0x000F40BC	VOUT0_DATA1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A1	1	OZ									
			PR0_PRU1_GPO1	2	O									
			PR0_PRU1_GPI1	3	I	0								
			UART2_TXD	4	O									
			PR0_PRU0_GPO9	5	IO	0								
			PR0_PRU0_GPI9	6	I	0								
			GPIO0_46	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W25	R18	VOUT0_DATA2 PADCONFIG: PADCONFIG48 0x000F40C0	VOUT0_DATA2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A2	1	OZ									
			PR0_PRU1_GPO2	2	O									
			PR0_PRU1_GPI2	3	I	0								
			UART3_RXD	4	I	1								
			PR0_PRU0_GPO10	5	IO	0								
			PR0_PRU0_GPI10	6	I	0								
			GPIO0_47	7	IO	pad								
W24	R19	VOUT0_DATA3 PADCONFIG: PADCONFIG49 0x000F40C4	VOUT0_DATA3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A3	1	OZ									
			PR0_PRU1_GPO3	2	O									
			PR0_PRU1_GPI3	3	I	0								
			UART3_TXD	4	O									
			PR0_PRU0_GPO11	5	IO	0								
			PR0_PRU0_GPI11	6	I	0								
			GPIO0_48	7	IO	pad								
Y25	R20	VOUT0_DATA4 PADCONFIG: PADCONFIG50 0x000F40C8	VOUT0_DATA4	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A4	1	OZ									
			PR0_PRU1_GPO4	2	O									
			PR0_PRU1_GPI4	3	I	0								
			UART4_RXD	4	I	1								
			PR0_PRU0_GPO12	5	IO	0								
			PR0_PRU0_GPI12	6	I	0								
			GPIO0_49	7	IO	pad								
Y24	T20	VOUT0_DATA5 PADCONFIG: PADCONFIG51 0x000F40CC	VOUT0_DATA5	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A5	1	OZ									
			PR0_PRU1_GPO5	2	O									
			PR0_PRU1_GPI5	3	I	0								
			UART4_TXD	4	O									
			PR0_PRU0_GPO13	5	IO	0								
			PR0_PRU0_GPI13	6	I	0								
			GPIO0_50	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y23	T21	VOUT0_DATA6 PADCONFIG: PADCONFIG52 0x000F40D0	VOUT0_DATA6	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A6	1	OZ									
			PR0_PRU1_GPO6	2	O									
			PR0_PRU1_GPI6	3	I	0								
			UART5_RXD	4	I	1								
			PR0_PRU0_GPO14	5	IO	0								
			PR0_PRU0_GPI14	6	I	0								
			GPIO0_51	7	IO	pad								
AA25	T19	VOUT0_DATA7 PADCONFIG: PADCONFIG53 0x000F40D4	VOUT0_DATA7	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A7	1	OZ									
			PR0_PRU1_GPO7	2	O									
			PR0_PRU1_GPI7	3	I	0								
			UART5_TXD	4	O									
			PR0_PRU0_GPO15	5	IO	0								
			PR0_PRU0_GPI15	6	I	0								
			GPIO0_52	7	IO	pad								
V21	U21	VOUT0_DATA8 PADCONFIG: PADCONFIG54 0x000F40D8	VOUT0_DATA8	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A8	1	OZ									
			PR0_PRU1_GPO16	2	O									
			PR0_PRU1_GPI16	3	I	0								
			UART6_RXD	4	I	1								
			PR0_PRU0_GPO17	5	IO	0								
			PR0_PRU0_GPI17	6	I	0								
			GPIO0_53	7	IO	pad								
W21	R17	VOUT0_DATA9 PADCONFIG: PADCONFIG55 0x000F40DC	VOUT0_DATA9	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A9	1	OZ									
			PR0_PRU1_GPO8	2	O									
			PR0_PRU1_GPI8	3	I	0								
			UART6_TXD	4	O									
			PR0_PRU0_GPO16	5	IO	0								
			PR0_PRU0_GPI16	6	I	0								
			GPIO0_54	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V20	T18	VOUT0_DATA10 PADCONFIG: PADCONFIG56 0x000F40E0	VOUT0_DATA10	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A10	1	OZ									
			PR0_PRU1_GPO9	2	O									
			PR0_PRU1_GPI9	3	I	0								
			UART6_RTSn	4	O									
			PR0_PRU0_GPO0	5	IO	0								
			PR0_PRU0_GPI0	6	I	0								
			GPIO0_55	7	IO	pad								
AA23	U20	VOUT0_DATA11 PADCONFIG: PADCONFIG57 0x000F40E4	VOUT0_DATA11	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A11	1	OZ									
			PR0_PRU1_GPO10	2	O									
			PR0_PRU1_GPI10	3	I	0								
			UART6_CTSn	4	I	1								
			PR0_PRU0_GPO1	5	IO	0								
			PR0_PRU0_GPI1	6	I	0								
			GPIO0_56	7	IO	pad								
AB25	U19	VOUT0_DATA12 PADCONFIG: PADCONFIG58 0x000F40E8	VOUT0_DATA12	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A12	1	OZ									
			PR0_PRU1_GPO11	2	O									
			PR0_PRU1_GPI11	3	I	0								
			UART5_RTSn	4	O									
			PR0_PRU0_GPO2	5	IO	0								
			PR0_PRU0_GPI2	6	I	0								
			GPIO0_57	7	IO	pad								
AA24	V21	VOUT0_DATA13 PADCONFIG: PADCONFIG59 0x000F40EC	VOUT0_DATA13	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A13	1	OZ									
			PR0_PRU1_GPO12	2	O									
			PR0_PRU1_GPI12	3	I	0								
			UART5_CTSn	4	I	1								
			PR0_PRU0_GPO3	5	IO	0								
			PR0_PRU0_GPI3	6	I	0								
			GPIO0_58	7	IO	pad								

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y22	U18	VOUT0_DATA14 PADCONFIG: PADCONFIG60 0x000F40F0	VOUT0_DATA14	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A14	1	OZ									
			PR0_PRU1_GPO13	2	O									
			PR0_PRU1_GPI13	3	I	0								
			UART4_RTSn	4	O									
			PR0_PRU0_GPO4	5	IO	0								
			PR0_PRU0_GPI4	6	I	0								
			GPIO0_59	7	IO	pad								
AA21	V20	VOUT0_DATA15 PADCONFIG: PADCONFIG61 0x000F40F4	VOUT0_DATA15	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
			GPMC0_A15	1	OZ									
			PR0_PRU1_GPO14	2	O									
			PR0_PRU1_GPI14	3	I	0								
			UART4_CTSn	4	I	1								
			PR0_PRU0_GPO5	5	IO	0								
			PR0_PRU0_GPI5	6	I	0								
			GPIO0_60	7	IO	pad								
J8	F7	VPP	VPP		PWR									

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A1, A24, A25, AA11, AB9, AD1, AD12, AD16, AD25, AD9, AE1, AE12, AE16, AE24, AE25, AE8, B25, F13, G13, G19, H13, H16, H18, H20, J13, J7, K13, K15, K19, K7, L20, M10, M12, M13, M17, M18, M7, M8, N15, P10, P13, P7, R13, R15, R18, R20, T13, T14, T16, T17, T18, T8, U19, U8, V10, V11, V13, V16, V18, V9, W7, Y2	A1, A21, A4, AA1, AA12, AA15, AA21, AA9, D11, D19, D4, E2, F11, F13, F15, F4, F9, G16, G6, G9, H1, H13, H6, J10, J12, J14, J16, J6, K13, K3, K6, K8, L1, L10, L12, L14, L16, L6, M11, M16, M18, M6, M9, N12, N14, N6, P1, P10, P13, P15, P16, P3, P6, R16, R5, R7, R8, T10, T12, T15, T3, T6, T7, T9, U10, U13, U5, U8, V11, V14, V19, W10, W13, W7, Y11, Y14, Y3, Y4, Y6	VSS	VSS		PWR									
A12	B12	WKUP_CLKOUT0 PADCONFIG: MCU_PADCONFIG33 0x04084084	WKUP_CLKOUT0 MCU_GPIO0_23	0 7	O IO	 pad	Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B9	E9	WKUP_I2C0_SCL PADCONFIG: MCU_PADCONFIG19 0x0408404C	WKUP_I2C0_SCL MCU_GPIO0_19	0 7	IOD IOD	1 pad	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
A9	A9	WKUP_I2C0_SDA PADCONFIG: MCU_PADCONFIG20 0x04084050	WKUP_I2C0_SDA MCU_GPIO0_20	0 7	IOD IOD	1 pad	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
C2	A2	WKUP_LFOSC0_XI	WKUP_LFOSC0_XI		I					1.8 V	VDDS_OSC0		LFXOSC	
C1	A3	WKUP_LFOSC0_XO	WKUP_LFOSC0_XO		O					1.8 V	VDDS_OSC0		LFXOSC	

表 6-1. Pin Attributes (ALW, AMC Packages) (continued)

ALW BALL NUMBER [1]	AMC BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C6	A7	WKUP_UART0_CTSn PADCONFIG: MCU_PADCONFIG11 0x0408402C	WKUP_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			WKUP_TIMER_IO0	1	IO	0								
			MCU_SPI1_CS0	3	IO	1								
			MCU_GPIO0_11	7	IO	pad								
A4	B4	WKUP_UART0_RTSn PADCONFIG: MCU_PADCONFIG12 0x04084030	WKUP_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			WKUP_TIMER_IO1	1	IO	0								
			MCU_SPI1_CLK	3	IO	0								
			MCU_GPIO0_12	7	IO	pad								
B4	B5	WKUP_UART0_RXD PADCONFIG: MCU_PADCONFIG9 0x04084024	WKUP_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_SPI0_CS2	2	IO	1								
			MCU_GPIO0_9	7	IO	pad								
C5	C6	WKUP_UART0_TXD PADCONFIG: MCU_PADCONFIG10 0x04084028	WKUP_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
			MCU_SPI1_CS2	2	IO	1								
			MCU_GPIO0_10	7	IO	pad								

6.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

> 注
>
> Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Ball number(s) associated with signal

For more information on the IO cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

6.3.1 CPSW3G

6.3.1.1 MAIN Domain

表 6-2. CPSW3G0 RGMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	AD17	AA16
RGMII1_RX_CTL	I	RGMII Receive Control	AE17	W14
RGMII1_TXC	IO	RGMII Transmit Clock	AE19	W16
RGMII1_TX_CTL	O	RGMII Transmit Control	AD19	V15
RGMII1_RD0	I	RGMII Receive Data 0	AB17	W15
RGMII1_RD1	I	RGMII Receive Data 1	AC17	Y16
RGMII1_RD2	I	RGMII Receive Data 2	AB16	AA17
RGMII1_RD3	I	RGMII Receive Data 3	AA15	Y15
RGMII1_TD0	O	RGMII Transmit Data 0	AE20	U14
RGMII1_TD1	O	RGMII Transmit Data 1	AD20	AA19
RGMII1_TD2	O	RGMII Transmit Data 2	AE18	Y17
RGMII1_TD3	O	RGMII Transmit Data 3	AD18	AA18

表 6-3. CPSW3G0 RGMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	AD23	V18
RGMII2_RX_CTL	I	RGMII Receive Control	AD22	W19
RGMII2_TXC	IO	RGMII Transmit Clock	AE21	Y18
RGMII2_TX_CTL	O	RGMII Transmit Control	AA19	Y21
RGMII2_RD0	I	RGMII Receive Data 0	AE23	W18
RGMII2_RD1	I	RGMII Receive Data 1	AB20	Y20
RGMII2_RD2	I	RGMII Receive Data 2	AC21	Y19
RGMII2_RD3	I	RGMII Receive Data 3	AE22	W20
RGMII2_TD0	O	RGMII Transmit Data 0	Y18	AA20
RGMII2_TD1	O	RGMII Transmit Data 1	AA18	U15
RGMII2_TD2	O	RGMII Transmit Data 2	AD21	W17
RGMII2_TD3	O	RGMII Transmit Data 3	AC20	V16

表 6-4. CPSW3G0 RMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	AE19	W16
RMII1_REF_CLK	I	RMII Reference Clock	AD17	AA16
RMII1_RX_ER	I	RMII Receive Data Error	AE17	W14
RMII1_TX_EN	O	RMII Transmit Enable	AD19	V15
RMII1_RXD0	I	RMII Receive Data 0	AB17	W15
RMII1_RXD1	I	RMII Receive Data 1	AC17	Y16
RMII1_TXD0	O	RMII Transmit Data 0	AE20	U14
RMII1_TXD1	O	RMII Transmit Data 1	AD20	AA19

表 6-5. CPSW3G0 RMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	AE21	Y18
RMII2_REF_CLK	I	RMII Reference Clock	AD23	V18
RMII2_RX_ER	I	RMII Receive Data Error	AD22	W19
RMII2_TX_EN	O	RMII Transmit Enable	AA19	Y21
RMII2_RXD0	I	RMII Receive Data 0	AE23	W18
RMII2_RXD1	I	RMII Receive Data 1	AB20	Y20
RMII2_TXD0	O	RMII Transmit Data 0	Y18	AA20
RMII2_TXD1	O	RMII Transmit Data 1	AA18	U15

6.3.2 CPTS

注

Some CPTS signals are connected directly to CPTS modules within the device. Other CPTS signals are connected to the Time Sync Router and fanned out to peripherals linked to the router. Input signals are sent to the peripherals while output signals are sourced from the peripherals. For more information, see the Time Sync and Compare Events section in the Time Sync chapter in the device TRM.

6.3.2.1 MAIN Domain

表 6-6. CPTS Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock Input	A18	C14
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	C13, D22	C19, D13
CP_GEMAC_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS	A14, C21	B20, D12
CP_GEMAC_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	B13, B21	B19, C12
CP_GEMAC_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	A22, B14	A14, A19
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	B16	E12
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	A18	C14
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	C15	B13
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	E15	A15

6.3.3 CSI-2

6.3.3.1 MAIN Domain

表 6-7. CSIRX0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
CSI0_RXCLKN	I	CSI-2 Differential Receive Clock Input (negative)	AD15	AA14
CSI0_RXCLKP	I	CSI-2 Differential Receive Clock Input (positive)	AE15	AA13
CSI0_RXRCALIB (1)	A	CSI-2 D-PHY connection to external calibration resistor	AA14	T11
CSI0_RXN0	I	CSI-2 Differential Receive Input (negative)	AB14	Y13
CSI0_RXN1	I	CSI-2 Differential Receive Input (negative)	AD14	V13
CSI0_RXN2	I	CSI-2 Differential Receive Input (negative)	AD13	U12
CSI0_RXN3	I	CSI-2 Differential Receive Input (negative)	AB12	W12
CSI0_RXP0	I	CSI-2 Differential Receive Input (positive)	AC15	Y12
CSI0_RXP1	I	CSI-2 Differential Receive Input (positive)	AE14	V12
CSI0_RXP2	I	CSI-2 Differential Receive Input (positive)	AE13	U11
CSI0_RXP3	I	CSI-2 Differential Receive Input (positive)	AC13	W11

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

6.3.4 DDRSS

6.3.4.1 MAIN Domain

表 6-8. DDRSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
DDR0_ACT_n	O	DDRSS Activation Command	N6	M1
DDR0_ALERT_n	IO	DDRSS Alert	R3	N1
DDR0_CAS_n	O	DDRSS Column Address Strobe	M4	J3
DDR0_PAR	O	DDRSS Command and Address Parity	T1	M2
DDR0_RAS_n	O	DDRSS Row Address Strobe	M5	K5

表 6-8. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
DDR0_WE_n	O	DDRSS Write Enable	N3	J2
DDR0_A0	O	DDRSS Address Bus	J1	F5
DDR0_A1	O	DDRSS Address Bus	J2	G5
DDR0_A2	O	DDRSS Address Bus	K3	G4
DDR0_A3	O	DDRSS Address Bus	L5	H4
DDR0_A4	O	DDRSS Address Bus	K4	J5
DDR0_A5	O	DDRSS Address Bus	K1	H5
DDR0_A6	O	DDRSS Address Bus	R2	P4
DDR0_A7	O	DDRSS Address Bus	P2	N2
DDR0_A8	O	DDRSS Address Bus	P1	P2
DDR0_A9	O	DDRSS Address Bus	P4	N4
DDR0_A10	O	DDRSS Address Bus	R5	N3
DDR0_A11	O	DDRSS Address Bus	P5	M3
DDR0_A12	O	DDRSS Address Bus	R6	P5
DDR0_A13	O	DDRSS Address Bus	R1	N5
DDR0_BA0	O	DDRSS Bank Address	M1	L5
DDR0_BA1	O	DDRSS Bank Address	N1	L3
DDR0_BG0	O	DDRSS Bank Group	T4	L4
DDR0_BG1	O	DDRSS Bank Group	N2	L2
DDR0_CAL0 (1)	A	IO Pad Calibration Resistor	M2	K4
DDR0_CK0	O	DDRSS Clock	L1	J1
DDR0_CK0_n	O	DDRSS Negative Clock	L2	K1
DDR0_CKE0	O	DDRSS Clock Enable	H2	G3
DDR0_CKE1	O	DDRSS Clock Enable	J4	H2
DDR0_CS0_n	O	DDRSS Chip Select	L6	H3
DDR0_CS1_n	O	DDRSS Chip Select	K2	G1
DDR0_DM0	IO	DDRSS Data Mask	H5	E3
DDR0_DM1	IO	DDRSS Data Mask	W5	R4
DDR0_DQ0	IO	DDRSS Data	F4	C2
DDR0_DQ1	IO	DDRSS Data	G5	E4
DDR0_DQ2	IO	DDRSS Data	F3	D3
DDR0_DQ3	IO	DDRSS Data	H6	E5
DDR0_DQ4	IO	DDRSS Data	E3	D2
DDR0_DQ5	IO	DDRSS Data	G2	F3
DDR0_DQ6	IO	DDRSS Data	F2	F1
DDR0_DQ7	IO	DDRSS Data	F1	F2
DDR0_DQ8	IO	DDRSS Data	U1	R3
DDR0_DQ9	IO	DDRSS Data	U3	R2
DDR0_DQ10	IO	DDRSS Data	U2	T2
DDR0_DQ11	IO	DDRSS Data	V5	U2
DDR0_DQ12	IO	DDRSS Data	W2	U3
DDR0_DQ13	IO	DDRSS Data	V6	U4
DDR0_DQ14	IO	DDRSS Data	Y1	T4
DDR0_DQ15	IO	DDRSS Data	W1	T5
DDR0_DQS0	IO	DDRSS Data Strobe	E1	D1

表 6-8. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
DDR0_DQS0_n	IO	DDRSS Complimentary Data Strobe	E2	E1
DDR0_DQS1	IO	DDRSS Data Strobe	V1	T1
DDR0_DQS1_n	IO	DDRSS Complimentary Data Strobe	V2	R1
DDR0_ODT0	O	DDRSS On-Die Termination for Chip Select 0	H1	J4
DDR0_ODT1	O	DDRSS On-Die Termination for Chip Select 1	J3	K2
DDR0_RESET0_n	O	DDRSS Reset	G1	G2

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage should be applied to this pin.

6.3.5 DSS

6.3.5.1 MAIN Domain

表 6-9. DSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
VOUT0_DE	O	Video Output Data Enable	Y20	T17
VOUT0_EXTPCLKIN	I	Video Output External Pixel Clock Input	V25	P17
VOUT0_HSYNC	O	Video Output Horizontal Sync	AB24	W21
VOUT0_PCLK	O	Video Output Pixel Clock Output	AC24	U17
VOUT0_VSYNC	O	Video Output Vertical Sync	AC25	T16
VOUT0_DATA0	O	Video Output Data 0	U22	R21
VOUT0_DATA1	O	Video Output Data 1	V24	P18
VOUT0_DATA2	O	Video Output Data 2	W25	R18
VOUT0_DATA3	O	Video Output Data 3	W24	R19
VOUT0_DATA4	O	Video Output Data 4	Y25	R20
VOUT0_DATA5	O	Video Output Data 5	Y24	T20
VOUT0_DATA6	O	Video Output Data 6	Y23	T21
VOUT0_DATA7	O	Video Output Data 7	AA25	T19
VOUT0_DATA8	O	Video Output Data 8	V21	U21
VOUT0_DATA9	O	Video Output Data 9	W21	R17
VOUT0_DATA10	O	Video Output Data 10	V20	T18
VOUT0_DATA11	O	Video Output Data 11	AA23	U20
VOUT0_DATA12	O	Video Output Data 12	AB25	U19
VOUT0_DATA13	O	Video Output Data 13	AA24	V21
VOUT0_DATA14	O	Video Output Data 14	Y22	U18
VOUT0_DATA15	O	Video Output Data 15	AA21	V20
VOUT0_DATA16	O	Video Output Data 16	R24	N20
VOUT0_DATA17	O	Video Output Data 17	R25	N21
VOUT0_DATA18	O	Video Output Data 18	T25	M17
VOUT0_DATA19	O	Video Output Data 19	R21	N18
VOUT0_DATA20	O	Video Output Data 20	T22	N17
VOUT0_DATA21	O	Video Output Data 21	T24	N19
VOUT0_DATA22	O	Video Output Data 22	U25	P19
VOUT0_DATA23	O	Video Output Data 23	U24	P20

6.3.6 ECAP

6.3.6.1 MAIN Domain

表 6-10. ECAP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	A18, C13	C14, D13

表 6-11. ECAP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	B16, B18, B19, B21, D14	A13, A18, B18, B19, E12

表 6-12. ECAP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	A16, A19, A22, B20, E14	A19, B17, C17, D14, E11

6.3.7 Emulation and Debug

6.3.7.1 MAIN Domain

表 6-13. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
TRC_CLK	O	Trace Clock	M25	K19
TRC_CTL	O	Trace Control	N23	L19
TRC_DATA0	O	Trace Data 0	N24	L20
TRC_DATA1	O	Trace Data 1	N25	L21
TRC_DATA2	O	Trace Data 2	P24	M21
TRC_DATA3	O	Trace Data 3	P22	L17
TRC_DATA4	O	Trace Data 4	P21	L18
TRC_DATA5	O	Trace Data 5	R23	M20
TRC_DATA6	O	Trace Data 6	P25	M19
TRC_DATA7	O	Trace Data 7	L23	K20
TRC_DATA8	O	Trace Data 8	L24	K21
TRC_DATA9	O	Trace Data 9	L25	J17
TRC_DATA10	O	Trace Data 10	M24	K17
TRC_DATA11	O	Trace Data 11	N20	K18
TRC_DATA12	O	Trace Data 12	U23	P21
TRC_DATA13	O	Trace Data 13	K25	J20
TRC_DATA14	O	Trace Data 14	M22	J19
TRC_DATA15	O	Trace Data 15	M21	J18
TRC_DATA16	O	Trace Data 16	L21	H17
TRC_DATA17	O	Trace Data 17	K22	H18
TRC_DATA18	O	Trace Data 18	K24	H19
TRC_DATA19	O	Trace Data 19	U24	P20
TRC_DATA20	O	Trace Data 20	U25	P19
TRC_DATA21	O	Trace Data 21	T24	N19
TRC_DATA22	O	Trace Data 22	T22	N17

表 6-13. Trace Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
TRC_DATA23	O	Trace Data 23	R21	N18

6.3.7.2 MCU Domain

表 6-14. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EMU0	IO	Emulation Control 0	E12	D9
EMU1	IO	Emulation Control 1	C11	B10
TCK	I	JTAG Test Clock Input	A10	C10
TDI	I	JTAG Test Data Input	A11	D10
TDO	OZ	JTAG Test Data Output	D12	E10
TMS	I	JTAG Test Mode Select Input	B11	B11
TRSTn	I	JTAG Reset	B10	A11

6.3.8 EPWM

6.3.8.1 MAIN Domain

表 6-15. EPWM Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	B16	E12
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	A16	D14
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	B14	A14
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	AA2	V2
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	AC1	W3
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	C15	B13
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	E15	A15
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	C13	D13

表 6-16. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EHRPWM0_A	IO	EHRPWM Output A	A13, AB2, E19	C11, D15, Y2
EHRPWM0_B	IO	EHRPWM Output B	A20, C13, Y4	D13, D16, W1
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	AC2, B17	A17, V4
EHRPWM0_SYNCO	O	Sync Input to EHRPWM module from an external pin	A17, AD2	A16, W4

表 6-17. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EHRPWM1_A	IO	EHRPWM Output A	A14, AA3, B18	A18, D12, W2
EHRPWM1_B	IO	EHRPWM Output B	AA1, B13, E18	C12, D18, V1

表 6-18. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EHRPWM2_A	IO	EHRPWM Output A	AB1, B17, D14	A13, A17, Y1
EHRPWM2_B	IO	EHRPWM Output B	A17, E14, Y3	A16, E11, V3

6.3.9 EQEP

6.3.9.1 MAIN Domain

表 6-19. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EQEP0_A (1)	I	EQEP Quadrature Input A	B19	B18
EQEP0_B (1)	I	EQEP Quadrature Input B	A19	B17
EQEP0_I (1)	IO	EQEP Index	E18	D18
EQEP0_S (1)	IO	EQEP Strobe	B18	A18

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 6-20. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EQEP1_A (1)	I	EQEP Quadrature Input A	B20	C17
EQEP1_B (1)	I	EQEP Quadrature Input B	D20	C16
EQEP1_I (1)	IO	EQEP Index	A20	D16
EQEP1_S (1)	IO	EQEP Strobe	E19	D15

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 6-21. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
EQEP2_A (1)	I	EQEP Quadrature Input A	AC21, B16	E12, Y19
EQEP2_B (1)	I	EQEP Quadrature Input B	A16, AE22	D14, W20
EQEP2_I (1)	IO	EQEP Index	AD21, C15, V25	B13, P17, W17
EQEP2_S (1)	IO	EQEP Strobe	AC20, E15, M22	A15, J19, V16

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.10 GPIO

6.3.10.1 MAIN Domain

表 6-22. GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO0_0	IO	General Purpose Input/Output	H24	G19
GPIO0_1	IO	General Purpose Input/Output	G25	G18
GPIO0_2	IO	General Purpose Input/Output	J24	H20
GPIO0_3	IO	General Purpose Input/Output	E25	F18
GPIO0_4	IO	General Purpose Input/Output	G24	G17
GPIO0_5	IO	General Purpose Input/Output	F25	F21
GPIO0_6	IO	General Purpose Input/Output	F24	F20
GPIO0_7	IO	General Purpose Input/Output	J23	G21
GPIO0_8	IO	General Purpose Input/Output	J25	H21
GPIO0_9	IO	General Purpose Input/Output	H25	G20
GPIO0_10	IO	General Purpose Input/Output	J22	J21
GPIO0_11	IO	General Purpose Input/Output	F23	F19
GPIO0_12	IO	General Purpose Input/Output	G21	F17

表 6-22. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO0_13 (1)	IO	General Purpose Input/Output	H21	E17
GPIO0_14 (1)	IO	General Purpose Input/Output	E24	E18
GPIO0_15	IO	General Purpose Input/Output	M25	K19
GPIO0_16	IO	General Purpose Input/Output	N23	L19
GPIO0_17	IO	General Purpose Input/Output	N24	L20
GPIO0_18	IO	General Purpose Input/Output	N25	L21
GPIO0_19	IO	General Purpose Input/Output	P24	M21
GPIO0_20	IO	General Purpose Input/Output	P22	L17
GPIO0_21	IO	General Purpose Input/Output	P21	L18
GPIO0_22	IO	General Purpose Input/Output	R23	M20
GPIO0_23	IO	General Purpose Input/Output	R24	N20
GPIO0_24	IO	General Purpose Input/Output	R25	N21
GPIO0_25	IO	General Purpose Input/Output	T25	M17
GPIO0_26	IO	General Purpose Input/Output	R21	N18
GPIO0_27	IO	General Purpose Input/Output	T22	N17
GPIO0_28	IO	General Purpose Input/Output	T24	N19
GPIO0_29	IO	General Purpose Input/Output	U25	P19
GPIO0_30	IO	General Purpose Input/Output	U24	P20
GPIO0_31	IO	General Purpose Input/Output	P25	M19
GPIO0_32	IO	General Purpose Input/Output	L23	K20
GPIO0_33	IO	General Purpose Input/Output	L24	K21
GPIO0_34	IO	General Purpose Input/Output	L25	J17
GPIO0_35	IO	General Purpose Input/Output	M24	K17
GPIO0_36	IO	General Purpose Input/Output	N20	K18
GPIO0_37	IO	General Purpose Input/Output	U23	P21
GPIO0_38	IO	General Purpose Input/Output	V25	P17
GPIO0_39	IO	General Purpose Input/Output	K25	J20
GPIO0_40	IO	General Purpose Input/Output	M22	J19
GPIO0_41	IO	General Purpose Input/Output	M21	J18
GPIO0_42	IO	General Purpose Input/Output	L21	H17
GPIO0_43 (1)	IO	General Purpose Input/Output	K22	H18
GPIO0_44 (1)	IO	General Purpose Input/Output	K24	H19
GPIO0_45	IO	General Purpose Input/Output	U22	R21
GPIO0_46	IO	General Purpose Input/Output	V24	P18
GPIO0_47	IO	General Purpose Input/Output	W25	R18
GPIO0_48	IO	General Purpose Input/Output	W24	R19
GPIO0_49	IO	General Purpose Input/Output	Y25	R20
GPIO0_50	IO	General Purpose Input/Output	Y24	T20
GPIO0_51	IO	General Purpose Input/Output	Y23	T21
GPIO0_52	IO	General Purpose Input/Output	AA25	T19
GPIO0_53	IO	General Purpose Input/Output	V21	U21
GPIO0_54	IO	General Purpose Input/Output	W21	R17
GPIO0_55	IO	General Purpose Input/Output	V20	T18
GPIO0_56	IO	General Purpose Input/Output	AA23	U20
GPIO0_57	IO	General Purpose Input/Output	AB25	U19

表 6-22. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO0_58	IO	General Purpose Input/Output	AA24	V21
GPIO0_59	IO	General Purpose Input/Output	Y22	U18
GPIO0_60	IO	General Purpose Input/Output	AA21	V20
GPIO0_61	IO	General Purpose Input/Output	AB24	W21
GPIO0_62	IO	General Purpose Input/Output	Y20	T17
GPIO0_63	IO	General Purpose Input/Output	AC25	T16
GPIO0_64	IO	General Purpose Input/Output	AC24	U17
GPIO0_65 (1)	IO	General Purpose Input/Output	D24	E20
GPIO0_66 (1)	IO	General Purpose Input/Output	E23	E19
GPIO0_67 (1)	IO	General Purpose Input/Output	C25	D21
GPIO0_68 (1)	IO	General Purpose Input/Output	B24	B21
GPIO0_69 (1)	IO	General Purpose Input/Output	D25	E21
GPIO0_70 (1)	IO	General Purpose Input/Output	C24	C21
GPIO0_71 (1)	IO	General Purpose Input/Output	A23	D20
GPIO0_72 (1)	IO	General Purpose Input/Output	B23	C20
GPIO0_73	IO	General Purpose Input/Output	AD19	V15
GPIO0_74	IO	General Purpose Input/Output	AE19	W16
GPIO0_75	IO	General Purpose Input/Output	AE20	U14
GPIO0_76	IO	General Purpose Input/Output	AD20	AA19
GPIO0_77	IO	General Purpose Input/Output	AE18	Y17
GPIO0_78	IO	General Purpose Input/Output	AD18	AA18
GPIO0_79	IO	General Purpose Input/Output	AE17	W14
GPIO0_80	IO	General Purpose Input/Output	AD17	AA16
GPIO0_81	IO	General Purpose Input/Output	AB17	W15
GPIO0_82	IO	General Purpose Input/Output	AC17	Y16
GPIO0_83	IO	General Purpose Input/Output	AB16	AA17
GPIO0_84	IO	General Purpose Input/Output	AA15	Y15
GPIO0_85	IO	General Purpose Input/Output	AB22	U16
GPIO0_86	IO	General Purpose Input/Output	AD24	V17
GPIO0_87	IO	General Purpose Input/Output	AA19	Y21
GPIO0_88	IO	General Purpose Input/Output	AE21	Y18
GPIO0_89	IO	General Purpose Input/Output	Y18	AA20
GPIO0_90	IO	General Purpose Input/Output	AA18	U15
GPIO0_91	IO	General Purpose Input/Output	AD21	W17

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 6-23. GPIO1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO1_0	IO	General Purpose Input/Output	AC20	V16
GPIO1_1	IO	General Purpose Input/Output	AD22	W19
GPIO1_2	IO	General Purpose Input/Output	AD23	V18
GPIO1_3	IO	General Purpose Input/Output	AE23	W18
GPIO1_4	IO	General Purpose Input/Output	AB20	Y20
GPIO1_5	IO	General Purpose Input/Output	AC21	Y19

表 6-23. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO1_6	IO	General Purpose Input/Output	AE22	W20
GPIO1_7	IO	General Purpose Input/Output	B19	B18
GPIO1_8	IO	General Purpose Input/Output	A19	B17
GPIO1_9	IO	General Purpose Input/Output	B18	A18
GPIO1_10	IO	General Purpose Input/Output	E18	D18
GPIO1_11	IO	General Purpose Input/Output	B20	C17
GPIO1_12	IO	General Purpose Input/Output	D20	C16
GPIO1_13	IO	General Purpose Input/Output	E19	D15
GPIO1_14	IO	General Purpose Input/Output	A20	D16
GPIO1_15	IO	General Purpose Input/Output	A13	C11
GPIO1_16 (1)	IO	General Purpose Input/Output	C13	D13
GPIO1_17	IO	General Purpose Input/Output	A14	D12
GPIO1_18	IO	General Purpose Input/Output	B13	C12
GPIO1_19	IO	General Purpose Input/Output	B14	A14
GPIO1_20	IO	General Purpose Input/Output	D14	A13
GPIO1_21	IO	General Purpose Input/Output	E14	E11
GPIO1_22	IO	General Purpose Input/Output	A15	B14
GPIO1_23	IO	General Purpose Input/Output	B15	C13
GPIO1_24	IO	General Purpose Input/Output	C15	B13
GPIO1_25	IO	General Purpose Input/Output	E15	A15
GPIO1_26	IO	General Purpose Input/Output	B16	E12
GPIO1_27	IO	General Purpose Input/Output	A16	D14
GPIO1_28	IO	General Purpose Input/Output	B17	A17
GPIO1_29	IO	General Purpose Input/Output	A17	A16
GPIO1_30	IO	General Purpose Input/Output	A18	C14
GPIO1_31 (1)	IOD	General Purpose Input/Output	D16	B16
GPIO1_32 (1)	IO	General Purpose Input/Output	AC2	V4
GPIO1_33 (1)	IO	General Purpose Input/Output	AD2	W4
GPIO1_34 (1)	IO	General Purpose Input/Output	AC1	W3
GPIO1_35 (1)	IO	General Purpose Input/Output	AB2	Y2
GPIO1_36 (1)	IO	General Purpose Input/Output	Y4	W1
GPIO1_37 (1)	IO	General Purpose Input/Output	AA3	W2
GPIO1_38 (1)	IO	General Purpose Input/Output	AA1	V1
GPIO1_39 (1)	IO	General Purpose Input/Output	AA2	V2
GPIO1_40 (1)	IO	General Purpose Input/Output	AB1	Y1
GPIO1_41 (1)	IO	General Purpose Input/Output	Y3	V3
GPIO1_42 (1)	IO	General Purpose Input/Output	D22	C19
GPIO1_43 (1)	IO	General Purpose Input/Output	C21	B20
GPIO1_44 (1)	IO	General Purpose Input/Output	B21	B19
GPIO1_45 (1)	IO	General Purpose Input/Output	A22	A19
GPIO1_46 (1)	IO	General Purpose Input/Output	B22	A20
GPIO1_47 (1)	IO	General Purpose Input/Output	A21	C18
GPIO1_48 (1)	IO	General Purpose Input/Output	D17	C15
GPIO1_49 (2)	IO	General Purpose Input/Output	C17	B15
GPIO1_50	IO	General Purpose Input/Output	C20	D17

表 6-23. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPIO1_51	IO	General Purpose Input/Output	F18	E16

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.
(2) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.10.2 MCU Domain

表 6-24. MCU_GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_GPIO0_0 (1)	IO	General Purpose Input/Output	E8	E7
MCU_GPIO0_1 (1)	IO	General Purpose Input/Output	B8	C8
MCU_GPIO0_2	IO	General Purpose Input/Output	A7	B7
MCU_GPIO0_3	IO	General Purpose Input/Output	D9	E8
MCU_GPIO0_4	IO	General Purpose Input/Output	C9	D8
MCU_GPIO0_5	IO	General Purpose Input/Output	B5	A8
MCU_GPIO0_6	IO	General Purpose Input/Output	A5	B6
MCU_GPIO0_7 (1)	IO	General Purpose Input/Output	A6	B8
MCU_GPIO0_8 (1)	IO	General Purpose Input/Output	B6	D7
MCU_GPIO0_9	IO	General Purpose Input/Output	B4	B5
MCU_GPIO0_10	IO	General Purpose Input/Output	C5	C6
MCU_GPIO0_11 (1)	IO	General Purpose Input/Output	C6	A7
MCU_GPIO0_12 (1)	IO	General Purpose Input/Output	A4	B4
MCU_GPIO0_13	IO	General Purpose Input/Output	D6	C5
MCU_GPIO0_14	IO	General Purpose Input/Output	B3	C4
MCU_GPIO0_15 (1)	IO	General Purpose Input/Output	E5	D5
MCU_GPIO0_16 (1)	IO	General Purpose Input/Output	D4	D6
MCU_GPIO0_17	IOD	General Purpose Input/Output	A8	B9
MCU_GPIO0_18	IOD	General Purpose Input/Output	D10	A10
MCU_GPIO0_19	IOD	General Purpose Input/Output	B9	E9
MCU_GPIO0_20	IOD	General Purpose Input/Output	A9	A9
MCU_GPIO0_21	IO	General Purpose Input/Output	B12	A12
MCU_GPIO0_22	IO	General Purpose Input/Output	B7	C7
MCU_GPIO0_23	IO	General Purpose Input/Output	A12	B12

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.11 GPMC

6.3.11.1 MAIN Domain

表 6-25. GPMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	L23	K20
GPMC0_CLK	O	GPMC clock	P25	M19
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	M22	J19
GPMC0_FCLK_MUX	O	GPMC functional clock output	P25	M19
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	L24	K21

表 6-25. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPMC0_WEn	O	GPMC Write Enable (active low)	L25	J17
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	K25	J20
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	U22	R21
GPMC0_A1	OZ	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	V24	P18
GPMC0_A2	OZ	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	W25	R18
GPMC0_A3	OZ	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	W24	R19
GPMC0_A4	OZ	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	Y25	R20
GPMC0_A5	OZ	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	Y24	T20
GPMC0_A6	OZ	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	Y23	T21
GPMC0_A7	OZ	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	AA25	T19
GPMC0_A8	OZ	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	V21	U21
GPMC0_A9	OZ	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	W21	R17
GPMC0_A10	OZ	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	V20	T18
GPMC0_A11	OZ	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA23	U20
GPMC0_A12	OZ	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB25	U19
GPMC0_A13	OZ	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA24	V21
GPMC0_A14	OZ	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y22	U18
GPMC0_A15	OZ	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA21	V20
GPMC0_A16	OZ	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AB24	W21
GPMC0_A17	OZ	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y20	T17
GPMC0_A18	OZ	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC25	T16
GPMC0_A19	OZ	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC24	U17

表 6-25. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPMC0_A20	OZ	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	K24	H19
GPMC0_A21	OZ	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	V25	P17
GPMC0_A22	OZ	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	K25	J20
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	M25	K19
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	N23	L19
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	N24	L20
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	N25	L21
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	P24	M21
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	P22	L17
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	P21	L18
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	R23	M20
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	R24	N20
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	R25	N21
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	T25	M17
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	R21	N18
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	T22	N17
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	T24	N19
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	U25	P19
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	U24	P20

表 6-25. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	M24	K17
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	N20	K18
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	M21	J18
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	L21	H17
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	K22	H18
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	K24	H19
GPMC0_WAIT0	I	GPMC External Indication of Wait	U23	P21
GPMC0_WAIT1	I	GPMC External Indication of Wait	V25	P17

6.3.12 I2C

6.3.12.1 MAIN Domain

表 6-26. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
I2C0_SCL	IOD	I2C Clock	B16	E12
I2C0_SDA	IOD	I2C Data	A16	D14

表 6-27. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
I2C1_SCL	IOD	I2C Clock	B17	A17
I2C1_SDA	IOD	I2C Data	A17	A16

表 6-28. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
I2C2_SCL	IOD	I2C Clock	K22	H18
I2C2_SDA	IOD	I2C Data	K24	H19

表 6-29. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
I2C3_SCL	IOD	I2C Clock	A15, AB1	B14, Y1
I2C3_SDA	IOD	I2C Data	B15, Y3	C13, V3

6.3.12.2 MCU Domain

表 6-30. MCU_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_I2C0_SCL	IOD	I2C Clock	A8	B9
MCU_I2C0_SDA	IOD	I2C Data	D10	A10

6.3.12.3 WKUP Domain

表 6-31. WKUP_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
WKUP_I2C0_SCL	IOD	I2C Clock	B9	E9
WKUP_I2C0_SDA	IOD	I2C Data	A9	A9

6.3.13 MCAN

6.3.13.1 MAIN Domain

表 6-32. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCAN0_RX	I	MCAN Receive Data	E15	A15
MCAN0_TX	O	MCAN Transmit Data	C15	B13

6.3.13.2 MCU Domain

表 6-33. MCU_MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_MCAN0_RX	I	MCAN Receive Data	B3	C4
MCU_MCAN0_TX	O	MCAN Transmit Data	D6	C5

表 6-34. MCU_MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_MCAN1_RX	I	MCAN Receive Data	D4	D6
MCU_MCAN1_TX	O	MCAN Transmit Data	E5	D5

6.3.14 MCASP

6.3.14.1 MAIN Domain

表 6-35. MCASP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCASP0_ACLKR	IO	MCASP Receive Bit Clock	A20	D16
MCASP0_ACLKX	IO	MCASP Transmit Bit Clock	B20	C17
MCASP0_AFSR	IO	MCASP Receive Frame Sync	E19	D15
MCASP0_AFSX	IO	MCASP Transmit Frame Sync	D20	C16
MCASP0_AXR0	IO	MCASP Serial Data (Input/Output)	E18	D18
MCASP0_AXR1	IO	MCASP Serial Data (Input/Output)	B18	A18
MCASP0_AXR2	IO	MCASP Serial Data (Input/Output)	A19	B17
MCASP0_AXR3	IO	MCASP Serial Data (Input/Output)	B19	B18

表 6-36. MCASP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCASP1_ACLKR	IO	MCASP Receive Bit Clock	D25, E24, K24	E18, E21, H19
MCASP1_ACLKX	IO	MCASP Transmit Bit Clock	A23, H25, M24	D20, G20, K17
MCASP1_AFSR	IO	MCASP Receive Frame Sync	C24, H21, K22	C21, E17, H18
MCASP1_AFSX	IO	MCASP Transmit Frame Sync	B23, J22, U23	C20, J21, P21
MCASP1_AXR0	IO	MCASP Serial Data (Input/Output)	B24, J25, L25	B21, H21, J17
MCASP1_AXR1	IO	MCASP Serial Data (Input/Output)	C25, J23, L24	D21, G21, K21
MCASP1_AXR2	IO	MCASP Serial Data (Input/Output)	E23, H21, L23	E17, E19, K20
MCASP1_AXR3	IO	MCASP Serial Data (Input/Output)	D24, E24, P25	E18, E20, M19
MCASP1_AXR4	IO	MCASP Serial Data (Input/Output)	C24, K22	C21, H18
MCASP1_AXR5	IO	MCASP Serial Data (Input/Output)	D25, K24	E21, H19

表 6-37. MCASP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCASP2_ACLKR	IO	MCASP Receive Bit Clock	AA18, U24	P20, U15
MCASP2_ACLKX	IO	MCASP Transmit Bit Clock	AC20, B15, T24	C13, N19, V16
MCASP2_AFSR	IO	MCASP Receive Frame Sync	AB20, U25	P19, Y20
MCASP2_AFSX	IO	MCASP Transmit Frame Sync	A15, AD21, T22	B14, N17, W17
MCASP2_AXR0	IO	MCASP Serial Data (Input/Output)	AC21, C15, R24	B13, N20, Y19
MCASP2_AXR1	IO	MCASP Serial Data (Input/Output)	AD23, E15, R25	A15, N21, V18
MCASP2_AXR2	IO	MCASP Serial Data (Input/Output)	AE23, T25	M17, W18
MCASP2_AXR3	IO	MCASP Serial Data (Input/Output)	AD22, R21	N18, W19
MCASP2_AXR4	IO	MCASP Serial Data (Input/Output)	AA19, M25	K19, Y21
MCASP2_AXR5	IO	MCASP Serial Data (Input/Output)	AE21, N23	L19, Y18
MCASP2_AXR6	IO	MCASP Serial Data (Input/Output)	N24, Y18	AA20, L20
MCASP2_AXR7	IO	MCASP Serial Data (Input/Output)	AB20, N25	L21, Y20
MCASP2_AXR8	IO	MCASP Serial Data (Input/Output)	AA18, P24	M21, U15
MCASP2_AXR9	IO	MCASP Serial Data (Input/Output)	P22	L17
MCASP2_AXR10	IO	MCASP Serial Data (Input/Output)	P21	L18
MCASP2_AXR11	IO	MCASP Serial Data (Input/Output)	R23	M20
MCASP2_AXR12	IO	MCASP Serial Data (Input/Output)	N20	K18
MCASP2_AXR13	IO	MCASP Serial Data (Input/Output)	M22	J19
MCASP2_AXR14	IO	MCASP Serial Data (Input/Output)	M21	J18
MCASP2_AXR15	IO	MCASP Serial Data (Input/Output)	L21	H17

6.3.15 MCSPI

6.3.15.1 MAIN Domain

表 6-38. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
SPI0_CLK	IO	SPI Clock	A14	D12
SPI0_CS0	IO	SPI Chip Select 0	A13	C11
SPI0_CS1	IO	SPI Chip Select 1	C13	D13
SPI0_CS2	IO	SPI Chip Select 2	A15	B14
SPI0_CS3	IO	SPI Chip Select 3	B15	C13
SPI0_D0	IO	SPI Data 0	B13	C12
SPI0_D1	IO	SPI Data 1	B14	A14

表 6-39. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
SPI1_CLK	IO	SPI Clock	AA3, J25	H21, W2
SPI1_CS0	IO	SPI Chip Select 0	J23, Y4	G21, W1
SPI1_CS1	IO	SPI Chip Select 1	AB1, H21	E17, Y1
SPI1_CS2	IO	SPI Chip Select 2	Y3	V3
SPI1_CS3	IO	SPI Chip Select 3	AA1	V1
SPI1_D0	IO	SPI Data 0	AC2, H25	G20, V4

表 6-39. MCSPI1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
SPI1_D1	IO	SPI Data 1	AD2, J22	J21, W4

表 6-40. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
SPI2_CLK	IO	SPI Clock	A17, A20, AA2	A16, D16, V2
SPI2_CS0	IO	SPI Chip Select 0	AA1, B16, E19	D15, E12, V1
SPI2_CS1	IO	SPI Chip Select 1	AC2, B17, B20	A17, C17, V4
SPI2_CS2	IO	SPI Chip Select 2	A16, B18, Y4	A18, D14, W1
SPI2_CS3	IO	SPI Chip Select 3	A18, AD2, D20	C14, C16, W4
SPI2_D0	IO	SPI Data 0	AC1, B19, D14	A13, B18, W3
SPI2_D1	IO	SPI Data 1	A19, AB2, E14	B17, E11, Y2

6.3.15.2 MCU Domain

表 6-41. MCU_MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_SPI0_CLK	IO	SPI Clock	A7	B7
MCU_SPI0_CS0	IO	SPI Chip Select 0	E8	E7
MCU_SPI0_CS1	IO	SPI Chip Select 1	B8	C8
MCU_SPI0_CS2	IO	SPI Chip Select 2	B4, D4	B5, D6
MCU_SPI0_CS3	IO	SPI Chip Select 3	D6	C5
MCU_SPI0_D0	IO	SPI Data 0	D9	E8
MCU_SPI0_D1	IO	SPI Data 1	C9	D8

表 6-42. MCU_MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_SPI1_CLK	IO	SPI Clock	A4, D4	B4, D6
MCU_SPI1_CS0	IO	SPI Chip Select 0	C6	A7
MCU_SPI1_CS1	IO	SPI Chip Select 2	E5	D5
MCU_SPI1_CS2	IO	SPI Chip Select 2	C5, D4	C6, D6
MCU_SPI1_CS3	IO	SPI Chip Select 3	B3	C4
MCU_SPI1_D0	IO	SPI Data 0	A6	B8
MCU_SPI1_D1	IO	SPI Data 1	B6	D7

6.3.16 MDIO

6.3.16.1 MAIN Domain

表 6-43. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MDIO0_MDC	O	MDIO Clock	AD24	V17
MDIO0_MDIO	IO	MDIO Data	AB22	U16

6.3.17 MMC

6.3.17.1 MAIN Domain

表 6-44. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MMC0_CLK (1)	IO	MMC/SD/SDIO Clock	AB1	Y1
MMC0_CMD	IO	MMC/SD/SDIO Command	Y3	V3
MMC0_DAT0	IO	MMC/SD/SDIO Data	AA2	V2
MMC0_DAT1	IO	MMC/SD/SDIO Data	AA1	V1
MMC0_DAT2	IO	MMC/SD/SDIO Data	AA3	W2
MMC0_DAT3	IO	MMC/SD/SDIO Data	Y4	W1
MMC0_DAT4	IO	MMC/SD/SDIO Data	AB2	Y2
MMC0_DAT5	IO	MMC/SD/SDIO Data	AC1	W3
MMC0_DAT6	IO	MMC/SD/SDIO Data	AD2	W4
MMC0_DAT7	IO	MMC/SD/SDIO Data	AC2	V4

(1) For MMC0_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG135 register must remain in its default state of 0x1 because of retiming purposes.

表 6-45. MMC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MMC1_CLK (1)	IO	MMC/SD/SDIO Clock	B22	A20
MMC1_CMD	IO	MMC/SD/SDIO Command	A21	C18
MMC1_SDCD	I	SD Card Detect	D17	C15
MMC1_SDWP	I	SD Write Protect	C17	B15
MMC1_DAT0	IO	MMC/SD/SDIO Data	A22	A19
MMC1_DAT1	IO	MMC/SD/SDIO Data	B21	B19
MMC1_DAT2	IO	MMC/SD/SDIO Data	C21	B20
MMC1_DAT3	IO	MMC/SD/SDIO Data	D22	C19

(1) For MMC1_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG142 register must remain in its default state of 0x1 because of retiming purposes.

表 6-46. MMC2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MMC2_CLK (1)	IO	MMC/SD/SDIO Clock	D25	E21
MMC2_CMD	IO	MMC/SD/SDIO Command	C24	C21
MMC2_SDCD	I	SD Card Detect	A15, A23, B17	A17, B14, D20
MMC2_SDWP	I	SD Write Protect	A17, B15, B23	A16, C13, C20
MMC2_DAT0	IO	MMC/SD/SDIO Data	B24	B21
MMC2_DAT1	IO	MMC/SD/SDIO Data	C25	D21
MMC2_DAT2	IO	MMC/SD/SDIO Data	E23	E19
MMC2_DAT3	IO	MMC/SD/SDIO Data	D24	E20

(1) For MMC2_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG71 register must remain in its default state of 0x1 because of retiming purposes.

6.3.18 OLDI

6.3.18.1 MAIN Domain

表 6-47. OLDI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
OLDI0_A0N	IO	OLDI Differential Data (negative)	AA5	AA2

表 6-47. OLDI0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
OLDI0_A0P	IO	OLDI Differential Data (positive)	Y6	AA3
OLDI0_A1N	IO	OLDI Differential Data (negative)	AD3	V5
OLDI0_A1P	IO	OLDI Differential Data (positive)	AB4	V6
OLDI0_A2N	IO	OLDI Differential Data (negative)	Y8	U7
OLDI0_A2P	IO	OLDI Differential Data (positive)	AA8	U6
OLDI0_A3N	IO	OLDI Differential Data (negative)	AB6	W6
OLDI0_A3P	IO	OLDI Differential Data (positive)	AA7	W5
OLDI0_A4N	IO	OLDI Differential Data (negative)	AC6	AA4
OLDI0_A4P	IO	OLDI Differential Data (positive)	AC5	Y5
OLDI0_A5N	IO	OLDI Differential Data (negative)	AE5	AA6
OLDI0_A5P	IO	OLDI Differential Data (positive)	AD6	AA5
OLDI0_A6N	IO	OLDI Differential Data (negative)	AE6	AA10
OLDI0_A6P	IO	OLDI Differential Data (positive)	AD7	Y9
OLDI0_A7N	IO	OLDI Differential Data (negative)	AD8	AA8
OLDI0_A7P	IO	OLDI Differential Data (positive)	AE7	Y8
OLDI0_CLK0N	IO	OLDI Differential Clock (negative)	AD4	V7
OLDI0_CLK0P	IO	OLDI Differential Clock (positive)	AE3	V8
OLDI0_CLK1N	IO	OLDI Differential Clock (negative)	AE4	Y7
OLDI0_CLK1P	IO	OLDI Differential Clock (positive)	AD5	AA7

6.3.19 OSPI

6.3.19.1 MAIN Domain

表 6-48. OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
OSPI0_CLK	O	OSPI Clock	H24	G19
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	J24	H20
OSPI0_ECC_FAIL	I	OSPI ECC Status	E24	E18
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	G25	G18
OSPI0_CSn0	O	OSPI Chip Select 0 (active low)	F23	F19
OSPI0_CSn1	O	OSPI Chip Select 1 (active low)	G21	F17
OSPI0_CSn2	O	OSPI Chip Select 2 (active low)	H21	E17
OSPI0_CSn3	O	OSPI Chip Select 3 (active low)	E24	E18
OSPI0_D0	IO	OSPI Data 0	E25	F18
OSPI0_D1	IO	OSPI Data 1	G24	G17
OSPI0_D2	IO	OSPI Data 2	F25	F21
OSPI0_D3	IO	OSPI Data 3	F24	F20
OSPI0_D4	IO	OSPI Data 4	J23	G21
OSPI0_D5	IO	OSPI Data 5	J25	H21
OSPI0_D6	IO	OSPI Data 6	H25	G20
OSPI0_D7	IO	OSPI Data 7	J22	J21
OSPI0_RESET_OUT0	O	OSPI Reset	E24	E18
OSPI0_RESET_OUT1	O	OSPI Reset	H21	E17

6.3.20 Power Supply

表 6-49. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
CAP_VDDS0 (1)	CAP	External capacitor connection for IO group 0	H15	G12
CAP_VDDS1 (1)	CAP	External capacitor connection for IO group 1	K18	L15
CAP_VDDS2 (1)	CAP	External capacitor connection for IO group 2	W17	R13
CAP_VDDS3 (1)	CAP	External capacitor connection for IO group 3	P19	M15
CAP_VDDS4 (1)	CAP	External capacitor connection for IO group 4	U7	N8
CAP_VDDS5 (1)	CAP	External capacitor connection for IO group 5	H17	G15
CAP_VDDS6 (1)	CAP	External capacitor connection for IO group 6	J19	J15
CAP_VDDS_CANUART (1)	CAP	External capacitor connection for IO CANUART	G9	G8
CAP_VDDS_MCU (1)	CAP	External capacitor connection for IO MCU	H11	G11
VDDA_1P8_USB	PWR	USB 1.8 V analog supply	Y11	R11
VDDA_1P8_CSIRX0	PWR	CSIRX analog supply high	W14	R12
VDDA_1P8_OLDI0	PWR	OLDI analog supply	W10, W9	P9, R9
VDDA_3P3_USB	PWR	USB 3.3 V analog supply	Y13	R10
VDDA_CORE_CSIRX0	PWR	CSIRX analog supply low	W13	P12
VDDA_CORE_USB	PWR	USB Core Supply	W12	P11
VDDA_DDR_PLL0	PWR	DDR Deskew PLL analog supply		L9
VDDA_MCU	PWR	POR and MCU PLL analog supply	L11	H10
VDDA_PLL0	PWR	MAIN PLL, DDR PLL, DSS PLL0, and DSS PLL1 analog supply	U11	N10
VDDA_PLL1	PWR	PER0 PLL and PER1 PLL analog supply	U15	P14
VDDA_PLL2	PWR	ARM0 PLL and SMS PLL analog supply	L14	K12
VDDA_TEMP0	PWR	TEMP0 analog supply	T9	M7
VDDA_TEMP1	PWR	TEMP1 analog supply	G16	F16
VDDR_CORE	PWR	Core Supply	J12, K16, N12, N14, P16, R12, T10, U14	H11, M10, M13
VDDSHV0	PWR	IO supply for IO group 0	F15, G14	F12, G13
VDDSHV1	PWR	IO supply for IO group 1	L18, M19	K15, K16
VDDSHV2	PWR	IO supply for IO group 2	W16, W19	R14, R15
VDDSHV3	PWR	IO supply for IO group 3	N18, P18, T19, U18	N15, N16
VDDSHV4	PWR	IO supply for IO group 4	T7	N7, P7
VDDSHV5	PWR	IO supply for IO group 5	G17	F14, G14
VDDSHV6	PWR	IO supply for IO group 6	J18	H15, H16
VDDSHV_CANUART	PWR	IO supply for IO CANUART	H9	G7, H7
VDDSHV_MCU	PWR	IO supply for IO MCU	F11, G12	F10, G10
VDDS_DDR	PWR	DDR PHY IO supply	K9, L8, P9, R8	C1, J8, K7, K9, L8, U1
VDDS_DDR_C	PWR	DDR clock IO supply	M9	L7
VDDS_OSC0	PWR	MCU_OSC0 supply	G7	J7
VDD_CANUART	PWR	CANUART Core Supply	F8	H8

表 6-49. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
VDD_CORE	PWR	Core supply	H8, J11, J14, K17, L12, L15, M16, N11, N13, N8, P17, R11, R14, U12, V15, V17, V8	H12, H14, J11, J13, J9, K10, K14, L11, L13, M12, M14, M8, N11, N13, N9, P8
VPP	PWR	eFuse ROM programming supply	J8	F7
VSS	PWR	Ground	A1, A24, A25, AA11, AB9, AD1, AD12, AD16, AD25, AD9, AE1, AE12, AE16, AE24, AE25, AE8, B25, F13, G13, G19, H13, H16, H18, H20, J13, J7, K13, K15, K19, K7, L20, M10, M12, M13, M17, M18, M7, M8, N15, P10, P13, P7, R13, R15, R18, R20, T13, T14, T16, T17, T18, T8, U19, U8, V10, V11, V13, V16, V18, V9, W7, Y2	A1, A21, A4, AA1, AA12, AA15, AA21, AA9, D11, D19, D4, E2, F11, F13, F15, F4, F9, G16, G6, G9, H1, H13, H6, J10, J12, J14, J16, J6, K13, K3, K6, K8, L1, L10, L12, L14, L16, L6, M11, M16, M18, M6, M9, N12, N14, N6, P1, P10, P13, P15, P16, P3, P6, R16, R5, R7, R8, T10, T12, T15, T3, T6, T7, T9, U10, U13, U5, U8, V11, V14, V19, W10, W13, W7, Y11, Y14, Y3, Y4, Y6

(1) This pin must always be connected via a 1-µF capacitor to VSS.

6.3.21 PRUSS

注

The PRUSS contains a second layer of peripheral signal multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRUSS chapter in the device TRM

6.3.21.1 MAIN Domain

表 6-50. PRUSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PR0_ECAP0_IN_APWM_OUT	IO	PRUSS Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	AC24, AD21, B15, E18, M22	C13, D18, J19, U17, W17
PR0_ECAP0_SYNC_IN	I	PRUSS ECAP Sync Input	A13, AD23	C11, V18
PR0_ECAP0_SYNC_OUT	O	PRUSS ECAP Sync Output	A15, AC20	B14, V16
PR0_IEP0_EDIO_DATA_IN_OUT28	IO	PRUSS Industrial Ethernet Digital I/O Data Input/Output	B19	B18
PR0_IEP0_EDIO_DATA_IN_OUT29	IO	PRUSS Industrial Ethernet Digital I/O Data Input/Output	A19	B17

表 6-50. PRUSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PR0_IEP0_EDIO_DATA_IN_OUT30	IO	PRUSS Industrial Ethernet Digital I/O Data Input/Output	B16	E12
PR0_IEP0_EDIO_DATA_IN_OUT31	IO	PRUSS Industrial Ethernet Digital I/O Data Input/Output	A16	D14
PR0_PRU0_GPI0	I	PRUSS PRU Data Input	AD22, M25, T22, V20, Y4	K19, N17, T18, W1, W19
PR0_PRU0_GPI1	I	PRUSS PRU Data Input	AA23, AA3, AD23, N23, T24	L19, N19, U20, V18, W2
PR0_PRU0_GPI2	I	PRUSS PRU Data Input	AA1, AB25, AE23, N24, U25	L20, P19, U19, V1, W18
PR0_PRU0_GPI3	I	PRUSS PRU Data Input	AA2, AA24, AB20, N25, U24	L21, P20, V2, V21, Y20
PR0_PRU0_GPI4	I	PRUSS PRU Data Input	AC21, P24, Y22, Y3	M21, U18, V3, Y19
PR0_PRU0_GPI5	I	PRUSS PRU Data Input	AA21, P22	L17, V20
PR0_PRU0_GPI6	I	PRUSS PRU Data Input	AB24, P21	L18, W21
PR0_PRU0_GPI7	I	PRUSS PRU Data Input	R23, Y20	M20, T17
PR0_PRU0_GPI8	I	PRUSS PRU Data Input	P25, U22	M19, R21
PR0_PRU0_GPI9	I	PRUSS PRU Data Input	L23, V24	K20, P18
PR0_PRU0_GPI10	I	PRUSS PRU Data Input	L24, W25	K21, R18
PR0_PRU0_GPI11	I	PRUSS PRU Data Input	L25, W24	J17, R19
PR0_PRU0_GPI12	I	PRUSS PRU Data Input	M24, Y25	K17, R20
PR0_PRU0_GPI13	I	PRUSS PRU Data Input	N20, Y24	K18, T20
PR0_PRU0_GPI14	I	PRUSS PRU Data Input	U23, Y23	P21, T21
PR0_PRU0_GPI15	I	PRUSS PRU Data Input	AA25, K25	J20, T19
PR0_PRU0_GPI16	I	PRUSS PRU Data Input	AE22, M22, W21	J19, R17, W20
PR0_PRU0_GPI17	I	PRUSS PRU Data Input	M21, V21	J18, U21
PR0_PRU0_GPI18	I	PRUSS PRU Data Input	AC25, L21	H17, T16
PR0_PRU0_GPI19	I	PRUSS PRU Data Input	AC24, K22	H18, U17
PR0_PRU0_GPO0	IO	PRUSS PRU Data Output	AD22, M25, T22, V20, Y4	K19, N17, T18, W1, W19
PR0_PRU0_GPO1	IO	PRUSS PRU Data Output	AA23, AA3, AD23, N23, T24	L19, N19, U20, V18, W2
PR0_PRU0_GPO2	IO	PRUSS PRU Data Output	AA1, AB25, AE23, N24, U25	L20, P19, U19, V1, W18
PR0_PRU0_GPO3	IO	PRUSS PRU Data Output	AA2, AA24, AB20, N25, U24	L21, P20, V2, V21, Y20
PR0_PRU0_GPO4	IO	PRUSS PRU Data Output	AC21, P24, Y22, Y3	M21, U18, V3, Y19
PR0_PRU0_GPO5	IO	PRUSS PRU Data Output	AA21, P22	L17, V20
PR0_PRU0_GPO6	IO	PRUSS PRU Data Output	AB24, P21	L18, W21
PR0_PRU0_GPO7	IO	PRUSS PRU Data Output	R23, Y20	M20, T17
PR0_PRU0_GPO8	IO	PRUSS PRU Data Output	P25, U22	M19, R21
PR0_PRU0_GPO9	IO	PRUSS PRU Data Output	L23, V24	K20, P18

表 6-50. PRUSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PR0_PRU0_GPO10	IO	PRUSS PRU Data Output	L24, W25	K21, R18
PR0_PRU0_GPO11	IO	PRUSS PRU Data Output	L25, W24	J17, R19
PR0_PRU0_GPO12	IO	PRUSS PRU Data Output	M24, Y25	K17, R20
PR0_PRU0_GPO13	IO	PRUSS PRU Data Output	N20, Y24	K18, T20
PR0_PRU0_GPO14	IO	PRUSS PRU Data Output	U23, Y23	P21, T21
PR0_PRU0_GPO15	IO	PRUSS PRU Data Output	AA25, K25	J20, T19
PR0_PRU0_GPO16	IO	PRUSS PRU Data Output	AE22, M22, W21	J19, R17, W20
PR0_PRU0_GPO17	IO	PRUSS PRU Data Output	M21, V21	J18, U21
PR0_PRU0_GPO18	IO	PRUSS PRU Data Output	AC25, L21	H17, T16
PR0_PRU0_GPO19	IO	PRUSS PRU Data Output	AC24, K22	H18, U17
PR0_UART0_CTSn	I	PRUSS UART Clear to Send (active low)	AC20, AD17	AA16, V16
PR0_UART0_RTSn	O	PRUSS UART Request to Send (active low)	AB16, AE23	AA17, W18
PR0_UART0_RXD	I	PRUSS UART Receive Data	AC21, AE18, B18, B19, C15	A18, B13, B18, Y17, Y19
PR0_UART0_TXD	O	PRUSS UART Transmit Data	A19, AD18, AE22, E15, E18	A15, AA18, B17, D18, W20

表 6-51. PRUSS1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PR0_PRU1_GPI0	I	PRUSS PRU Data Input	AA19, AC2, R24, U22	N20, R21, V4, Y21
PR0_PRU1_GPI1	I	PRUSS PRU Data Input	AD2, AE21, R25, V24	N21, P18, W4, Y18
PR0_PRU1_GPI2	I	PRUSS PRU Data Input	AC1, T25, W25, Y18	AA20, M17, R18, W3
PR0_PRU1_GPI3	I	PRUSS PRU Data Input	AA18, AB2, R21, W24	N18, R19, U15, Y2
PR0_PRU1_GPI4	I	PRUSS PRU Data Input	AB1, AD21, Y25	R20, W17, Y1
PR0_PRU1_GPI5	I	PRUSS PRU Data Input	Y24	T20
PR0_PRU1_GPI6	I	PRUSS PRU Data Input	Y23	T21
PR0_PRU1_GPI7	I	PRUSS PRU Data Input	AA25	T19
PR0_PRU1_GPI8	I	PRUSS PRU Data Input	M25, W21	K19, R17
PR0_PRU1_GPI9	I	PRUSS PRU Data Input	N23, V20	L19, T18
PR0_PRU1_GPI10	I	PRUSS PRU Data Input	AA23, N24	L20, U20
PR0_PRU1_GPI11	I	PRUSS PRU Data Input	AB25, N25	L21, U19
PR0_PRU1_GPI12	I	PRUSS PRU Data Input	AA24, P24	M21, V21
PR0_PRU1_GPI13	I	PRUSS PRU Data Input	P22, Y22	L17, U18
PR0_PRU1_GPI14	I	PRUSS PRU Data Input	AA21, P21	L18, V20
PR0_PRU1_GPI15	I	PRUSS PRU Data Input	AB24, R23	M20, W21
PR0_PRU1_GPI16	I	PRUSS PRU Data Input	AC20, L21, V21	H17, U21, V16
PR0_PRU1_GPI17	I	PRUSS PRU Data Input	Y20	T17
PR0_PRU1_GPI18	I	PRUSS PRU Data Input	AC25	T16
PR0_PRU1_GPI19	I	PRUSS PRU Data Input	AC24	U17

表 6-51. PRUSS1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PR0_PRU1_GPO0	O	PRUSS PRU Data Output	AA19, AC2, R24, U22	N20, R21, V4, Y21
PR0_PRU1_GPO1	O	PRUSS PRU Data Output	AD2, AE21, R25, V24	N21, P18, W4, Y18
PR0_PRU1_GPO2	O	PRUSS PRU Data Output	AC1, T25, W25, Y18	AA20, M17, R18, W3
PR0_PRU1_GPO3	O	PRUSS PRU Data Output	AA18, AB2, R21, W24	N18, R19, U15, Y2
PR0_PRU1_GPO4	O	PRUSS PRU Data Output	AB1, AD21, Y25	R20, W17, Y1
PR0_PRU1_GPO5	O	PRUSS PRU Data Output	Y24	T20
PR0_PRU1_GPO6	O	PRUSS PRU Data Output	Y23	T21
PR0_PRU1_GPO7	O	PRUSS PRU Data Output	AA25	T19
PR0_PRU1_GPO8	O	PRUSS PRU Data Output	M25, W21	K19, R17
PR0_PRU1_GPO9	O	PRUSS PRU Data Output	N23, V20	L19, T18
PR0_PRU1_GPO10	O	PRUSS PRU Data Output	AA23, N24	L20, U20
PR0_PRU1_GPO11	O	PRUSS PRU Data Output	AB25, N25	L21, U19
PR0_PRU1_GPO12	O	PRUSS PRU Data Output	AA24, P24	M21, V21
PR0_PRU1_GPO13	O	PRUSS PRU Data Output	P22, Y22	L17, U18
PR0_PRU1_GPO14	O	PRUSS PRU Data Output	AA21, P21	L18, V20
PR0_PRU1_GPO15	O	PRUSS PRU Data Output	AB24, R23	M20, W21
PR0_PRU1_GPO16	O	PRUSS PRU Data Output	AC20, L21, V21	H17, U21, V16
PR0_PRU1_GPO17	O	PRUSS PRU Data Output	Y20	T17
PR0_PRU1_GPO18	O	PRUSS PRU Data Output	AC25	T16
PR0_PRU1_GPO19	O	PRUSS PRU Data Output	AC24	U17

6.3.22 Reserved

表 6-52. Reserved Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RSVD0	N/A	Reserved, must be left unconnected	B1	B3
RSVD1	N/A	Reserved, must be left unconnected	A2	C3
RSVD2	N/A	Reserved, must be left unconnected	F6	E6
RSVD3	N/A	Reserved, must be left unconnected	AE2	F8
RSVD4	N/A	Reserved, must be left unconnected	T2	R6
RSVD5	N/A	Reserved, must be left unconnected	U4	T13
RSVD6	N/A	Reserved, must be left unconnected	AA12	T14
RSVD7	N/A	Reserved, must be left unconnected	Y15	M4
RSVD8	N/A	Reserved, must be left unconnected	E7	M5

6.3.23 System and Miscellaneous

6.3.23.1 Boot Mode Configuration

6.3.23.1.1 MAIN Domain

表 6-53. Sysboot Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
BOOTMODE00	I	Bootmode pin 0	M25	K19

表 6-53. Sysboot Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
BOOTMODE01	I	Bootmode pin 1	N23	L19
BOOTMODE02	I	Bootmode pin 2	N24	L20
BOOTMODE03	I	Bootmode pin 3	N25	L21
BOOTMODE04	I	Bootmode pin 4	P24	M21
BOOTMODE05	I	Bootmode pin 5	P22	L17
BOOTMODE06	I	Bootmode pin 6	P21	L18
BOOTMODE07	I	Bootmode pin 7	R23	M20
BOOTMODE08	I	Bootmode pin 8	R24	N20
BOOTMODE09	I	Bootmode pin 9	R25	N21
BOOTMODE10	I	Bootmode pin 10	T25	M17
BOOTMODE11	I	Bootmode pin 11	R21	N18
BOOTMODE12	I	Bootmode pin 12	T22	N17
BOOTMODE13	I	Bootmode pin 13	T24	N19
BOOTMODE14	I	Bootmode pin 14	U25	P19
BOOTMODE15	I	Bootmode pin 15	U24	P20

6.3.23.2 Clock

6.3.23.2.1 MCU Domain

表 6-54. MCU Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_OSC0_XI	I	High frequency oscillator input	B2	A5
MCU_OSC0_XO	O	High frequency oscillator output	A3	A6

6.3.23.2.2 WKUP Domain

表 6-55. WKUP Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
WKUP_LFOSC0_XI	I	Low frequency (32.768 KHz) oscillator input	C2	A2
WKUP_LFOSC0_XO	O	Low frequency (32.768 KHz) oscillator output	C1	A3

6.3.23.3 System

6.3.23.3.1 MAIN Domain

表 6-56. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
AUDIO_EXT_REFCLK0	IO	External clock input to McASP or output from McASP	A15, AE22, E18	B14, D18, W20
AUDIO_EXT_REFCLK1	IO	External clock input to McASP or output from McASP	B15, D20, K25	C13, C16, J20
CLKOUT0	O	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A18	C14
EXTINTn	I	External Interrupt	D16	B16
EXT_REFCLK1	I	External clock input to Main Domain	A18	C14
OBSCLK0	O	Main Domain Observation clock output for test and debug purposes only	B16, T25	E12, M17
PORz_OUT	O	Main Domain POR status output	E21	E13

表 6-56. System Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
RESETSTATz	O	Main Domain warm reset status output	F22	E14
RESET_REQz	I	Main Domain external warm reset request input	F20	E15
SYSCLKOUT0	O	Main Domain system clock output (divided by 4) for test and debug purposes only	A18	C14

6.3.23.3.2 MCU Domain

表 6-57. MCU System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_ERRORn	IO	Error signal output from MCU Domain ESM	D1	B1
MCU_EXT_REFCLK0	I	External input to MCU Domain	B8, E5	C8, D5
MCU_OBSCLK0	O	MCU Domain Observation clock output for test and debug purposes only	B8	C8
MCU_PORz	I	MCU Domain cold reset	D2	B2
MCU_RESETSTATz	O	MCU Domain warm reset status output	B12	A12
MCU_RESETz	I	MCU Domain warm reset	E11	C9
MCU_SYSCLKOUT0	O	MCU Domain system clock output (divided by 4) for test and debug purposes only	B8	C8

6.3.23.3.3 WKUP Domain

表 6-58. WKUP System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
PMIC_LPM_EN0	O	Dual-function PMIC control output, Low Power Mode (active low) or PMIC Enable (active high)	B7	C7
WKUP_CLKOUT0	O	WKUP Domain CLKOUT0 output	A12	B12

6.3.23.4 VMON

表 6-59. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
VMON_1P8_SOC	A	Voltage monitor input for 1.8 V SoC power supply	G10	H9
VMON_3P3_SOC	A	Voltage monitor input for 3.3 V SoC power supply	K10	K11
VMON_VSYS	A	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	H10	F6

6.3.24 TIMER

6.3.24.1 MAIN Domain

表 6-60. TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	AA3, B17, D22	A17, C19, W2
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	A17, C21	A16, B20
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	B21, C15	B13, B19
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	A22, E15	A15, A19

表 6-60. TIMER Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	A18, AB1, B22	A20, C14, Y1
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	A16, A21, Y3	C18, D14, V3
TIMER_IO6	IO	Timer Inputs and Outputs (not tied to single timer instance)	A15, D17	B14, C15
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	B15, C17	B15, C13

6.3.24.2 MCU Domain

表 6-61. MCU_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	A6, B3	B8, C4
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B6, B8	C8, D7
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	E5	D5
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	D4	D6

6.3.24.3 WKUP Domain

表 6-62. WKUP_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
WKUP_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C6, D6	A7, C5
WKUP_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	A4, E8	B4, E7

6.3.25 UART

6.3.25.1 MAIN Domain

表 6-63. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	A15	B14
UART0_RTSn	O	UART Request to Send (active low)	B15	C13
UART0_RXD	I	UART Receive Data	D14	A13
UART0_TXD	O	UART Transmit Data	E14	E11

表 6-64. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	B19	B18
UART1_DCDn	I	UART Clear to Send (active low)	B16	E12
UART1_DSRn	I	UART Data Set Ready (active low)	A16	D14
UART1_DTRn	O	UART Data Terminal Ready (active low)	C15	B13
UART1_RIn	I	UART Ring Indicator	E15	A15
UART1_RTSn	O	UART Request to Send (active low)	A19	B17
UART1_RXD	I	UART Receive Data	B17, E19	A17, D15

表 6-64. UART1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART1_TXD	O	UART Transmit Data	A17, A20	A16, D16

表 6-65. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	A22, AB2, AC24, U25	A19, P19, U17, Y2
UART2_RTSn	O	UART Request to Send (active low)	AC1, AC25, B21, U24	B19, P20, T16, W3
UART2_RXD	I	UART Receive Data	A15, AC2, D22, R24, U22	B14, C19, N20, R21, V4
UART2_TXD	O	UART Transmit Data	AD2, B15, C21, R25, V24	B20, C13, N21, P18, W4

表 6-66. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	AA2, C17, Y20	B15, T17, V2
UART3_RTSn	O	UART Request to Send (active low)	AA1, AB24, D17	C15, V1, W21
UART3_RXD	I	UART Receive Data	B22, T25, W25, Y4	A20, M17, R18, W1
UART3_TXD	O	UART Transmit Data	A21, AA3, R21, W24	C18, N18, R19, W2

表 6-67. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	AA21	V20
UART4_RTSn	O	UART Request to Send (active low)	Y22	U18
UART4_RXD	I	UART Receive Data	A23, K22, T22, Y25	D20, H18, N17, R20
UART4_TXD	O	UART Transmit Data	B23, K24, T24, Y24	C20, H19, N19, T20

表 6-68. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	AA24, J24	H20, V21
UART5_RTSn	O	UART Request to Send (active low)	AB25, G25	G18, U19
UART5_RXD	I	UART Receive Data	C15, D24, H21, U25, Y23	B13, E17, E20, P19, T21
UART5_TXD	O	UART Transmit Data	AA25, E15, E23, E24, U24	A15, E18, E19, P20, T19

表 6-69. UART6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	AA23, J22	J21, U20
UART6_RTSn	O	UART Request to Send (active low)	H25, V20	G20, T18
UART6_RXD	I	UART Receive Data	B19, D17, D25, J23, V21, V25	B18, C15, E21, G21, P17, U21

表 6-69. UART6 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
UART6_TXD	O	UART Transmit Data	A19, C17, C24, J25, K25, W21	B15, B17, C21, H21, J20, R17

6.3.25.2 MCU Domain

表 6-70. MCU_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
MCU_UART0_CTSn	I	UART Clear to Send (active low)	A6	B8
MCU_UART0_RTSn	O	UART Request to Send (active low)	B6	D7
MCU_UART0_RXD	I	UART Receive Data	B5	A8
MCU_UART0_TXD	O	UART Transmit Data	A5	B6

6.3.25.3 WKUP Domain

表 6-71. WKUP_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
WKUP_UART0_CTSn	I	UART Clear to Send (active low)	C6	A7
WKUP_UART0_RTSn	O	UART Request to Send (active low)	A4	B4
WKUP_UART0_RXD	I	UART Receive Data	B4	B5
WKUP_UART0_TXD	O	UART Transmit Data	C5	C6

6.3.26 USB

6.3.26.1 MAIN Domain

表 6-72. USB0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	AE11	AA11
USB0_DP	IO	USB 2.0 Differential Data (positive)	AD11	Y10
USB0_DRVVBUS	O	USB VBUS control output (active high)	C20	D17
USB0_RCALIB (1)	A	Pin to connect to calibration resistor	AE10	T8
USB0_VBUS (2)	A	USB Level-shifted VBUS Input	AC11	V10

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 9.2.3, *USB VBUS Design Guidelines*.

表 6-73. USB1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALW PIN [4]	AMC PIN [4]
USB1_DM	IO	USB 2.0 Differential Data (negative)	AD10	W8
USB1_DP	IO	USB 2.0 Differential Data (positive)	AE9	W9
USB1_DRVVBUS	O	USB VBUS control output (active high)	F18	E16
USB1_RCALIB (1)	A	Pin to connect to calibration resistor	AC9	V9
USB1_VBUS (2)	A	USB Level-shifted VBUS Input	AB10	U9

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 9.2.3, *USB VBUS Design Guidelines*.

6.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

注

All power balls must be supplied with the voltages specified in セクション 7.5, *Recommended Operating Conditions*, unless otherwise specified .

注

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

表 6-74. Connectivity Requirements

ALW BALL NUMBER	AMC BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
D1 B10	B1 A11	MCU_ERRORn TRSTn	Each of these balls must be connected to VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
E12 C11 E11 F20 A10 A11 B11	D9 B10 C9 E15 C10 D10 B11	EMU0 EMU1 MCU_RESETz RESET_REQz TCK TDI TMS	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
A8 D10 B9 A9	B9 A10 E9 A9	MCU_I2C0_SCL MCU_I2C0_SDA WKUP_I2C0_SCL WKUP_I2C0_SDA	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level.
M25 N23 N24 N25 P24 P22 P21 R23 R24 R25 T25 R21 T22 T24 U25 U24	K19 L19 L20 L21 M21 L17 L18 M20 N20 N21 M17 N18 N17 N19 P19 P20	GPMC0_AD0 GPMC0_AD1 GPMC0_AD2 GPMC0_AD3 GPMC0_AD4 GPMC0_AD5 GPMC0_AD6 GPMC0_AD7 GPMC0_AD8 GPMC0_AD9 GPMC0_AD10 GPMC0_AD11 GPMC0_AD12 GPMC0_AD13 GPMC0_AD14 GPMC0_AD15	Each of these balls must be connected to the corresponding power supply(1) or VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.
K9 L8 P9 R8 - - M9	K9 L8 J8 K7 C1 U1 L7	VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR_C	If DDRSS is not used, each of these balls must be connected directly to VSS.

表 6-74. Connectivity Requirements (continued)

ALW BALL NUMBER	AMC BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
N6	M1	DDR0_ACT_n	
R3	N1	DDR0_ALERT_n	
M4	J3	DDR0_CAS_n	
T1	M2	DDR0_PAR	
M5	K5	DDR0_RAS_n	
N3	J2	DDR0_WE_n	
J1	F5	DDR0_A0	
J2	G5	DDR0_A1	
K3	G4	DDR0_A2	
L5	H4	DDR0_A3	
K4	J5	DDR0_A4	
K1	H5	DDR0_A5	
R2	P4	DDR0_A6	
P2	N2	DDR0_A7	
P1	P2	DDR0_A8	
P4	N4	DDR0_A9	
R5	N3	DDR0_A10	
P5	M3	DDR0_A11	
R6	P5	DDR0_A12	
R1	N5	DDR0_A13	
M1	L5	DDR0_BA0	
N1	L3	DDR0_BA1	
T4	L4	DDR0_BG0	
N2	L2	DDR0_BG1	
M2	K4	DDR0_CAL0	
L1	J1	DDR0_CK0	If DDRSS is not used, leave unconnected. Note: The DDR0 pins in this list can only be left unconnected when VDDS_DDR and VDDS_DDR_C are connected to VSS. The DDR0 pins must be connected as defined in the DDR Board Design and Layout Guidelines, when VDDS_DDR and VDDS_DDR_C are connected to a power source.
L2	K1	DDR0_CK0_n	
H2	G3	DDR0_CKE0	
J4	H2	DDR0_CKE1	
L6	H3	DDR0_CS0_n	
K2	G1	DDR0_CS1_n	
H5	E3	DDR0_DM0	
W5	R4	DDR0_DM1	
F4	C2	DDR0_DQ0	
G5	E4	DDR0_DQ1	
F3	D3	DDR0_DQ2	
H6	E5	DDR0_DQ3	
E3	D2	DDR0_DQ4	
G2	F3	DDR0_DQ5	
F2	F1	DDR0_DQ6	
F1	F2	DDR0_DQ7	
U1	R3	DDR0_DQ8	
U3	R2	DDR0_DQ9	
U2	T2	DDR0_DQ10	
V5	U2	DDR0_DQ11	
W2	U3	DDR0_DQ12	
V6	U4	DDR0_DQ13	
Y1	T4	DDR0_DQ14	
W1	T5	DDR0_DQ15	
E1	D1	DDR0_DQS0	
E2	E1	DDR0_DQS0_n	
V1	T1	DDR0_DQS1	
V2	R1	DDR0_DQS1_n	
H1	J4	DDR0_ODT0	
J3	K2	DDR0_ODT1	
G1	G2	DDR0_RESET0_n	
W12	P11	VDDA_CORE_USB	USB0 and USB1 share these power rails, so each of these balls must be connected to valid power sources when either USB0 or USB1 is used. If USB0 and USB1 are not used, each of these balls must be connected directly to VSS.
Y11	R11	VDDA_1P8_USB	
Y13	R10	VDDA_3P3_USB	

表 6-74. Connectivity Requirements (continued)

ALW BALL NUMBER	AMC BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
AE11 AD11 AE10 AC11 AD10 AE9 AC9 AB10	AA11 Y10 T8 V10 W8 W9 V9 U9	USB0_DM USB0_DP USB0_RCALIB USB0_VBUS USB1_DM USB1_DP USB1_RCALIB USB1_VBUS	If USB0 or USB1 is not used, leave the respective DM, DP, and VBUS balls unconnected. Note: The USB0_RCALIB and USB1_RCALIB pins can only be left unconnected when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to VSS. The USB0_RCALIB and USB1_RCALIB pins must be connected to VSS through separate appropriate external resistors when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to power sources.
W13 W14	P12 R12	VDDA_CORE_CSIRX0 VDDA_1P8_CSIRX0	If CSIRX0 is not used and the device boundary scan function is required, each of these balls must be connected to valid power sources. If CSIRX0 is not used and the device boundary scan function is not required, each of these balls can alternatively be connected directly to VSS.
AD15 AE15 AB14 AC15 AD14 AE14 AD13 AE13 AB12 AC13 AA14	AA14 AA13 Y13 Y12 V13 V12 U12 U11 W12 W11 T11	CSI0_RXCLKN CSI0_RXCLKP CSI0_RXN0 CSI0_RXP0 CSI0_RXN1 CSI0_RXP1 CSI0_RXN2 CSI0_RXP2 CSI0_RXN3 CSI0_RXP3 CSI0_RXRCALIB	If CSIRX0 is not used, leave unconnected.
AA5 Y6 AD3 AB4 Y8 AA8 AB6 AA7 AC6 AC5 AE5 AD6 AE6 AD7 AD8 AE7 AD4 AE3 AE4 AD5	AA2 AA3 V5 V6 U7 U6 W6 W5 AA4 Y5 AA6 AA5 AA10 Y9 AA8 Y8 V7 V8 Y7 AA7	OLDI0_A0N OLDI0_A0P OLDI0_A1N OLDI0_A1P OLDI0_A2N OLDI0_A2P OLDI0_A3N OLDI0_A3P OLDI0_A4N OLDI0_A4P OLDI0_A5N OLDI0_A5P OLDI0_A6N OLDI0_A6P OLDI0_A7N OLDI0_A7P OLDI0_CLK0N OLDI0_CLK0P OLDI0_CLK1N OLDI0_CLK1P	If OLDI0 is not used, leave unconnected.
H10	F6	VMON_VSYS	If VMON_VSYS is not used, this ball must be connected directly to VSS.
G10 K10	H9 K11	VMON_1P8_SOC VMON_3P3_SOC	If VMON_1P8_SOC and VMON_3P3_SOC are not used to monitor the SOC power rails, these balls must still be connected to their respective 1.8V and 3.3V power rails.

(1) To determine which power supply is associated with any IO, see POWER column of the *Pin Attributes* table.

注

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between V_{ILSS} and V_{IHSS}. The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1] [2]

PARAMETER			MIN	MAX	UNIT
VDD_CORE	Core supply		-0.3	1.05	V
VDDR_CORE	RAM supply		-0.3	1.05	V
VDD_CANUART	CANUART core supply		-0.3	1.05	V
VDDA_CORE_CSIRX0	CSIRX0 core supply		-0.3	1.05	V
VDDA_CORE_USB	USB0 and USB1 core supply		-0.3	1.05	V
VDDA_DDR_PLL0[3]	DDR Deskew PLL supply		-0.3	1.05	V
VDDS_DDR	DDR PHY IO supply		-0.3	1.57	V
VDDS_DDR_C	DDR clock IO supply		-0.3	1.57	V
VDDS_OSC0	MCU_OSC0 supply		-0.3	1.98	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply		-0.3	1.98	V
VDDA_PLL0	MAIN PLL, DDR PLL, DSS PLL0, and DSS PLL1 analog supply		-0.3	1.98	V
VDDA_PLL1	PER0 PLL and PER1 PLL analog supply		-0.3	1.98	V
VDDA_PLL2	ARM0 PLL and SMS PLL analog supply		-0.3	1.98	V
VDDA_1P8_CSIRX0	CSIRX0 1.8 V analog supply		-0.3	1.98	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply		-0.3	1.98	V
VDDA_1P8_USB	USB0 and USB1 1.8 V analog supply		-0.3	1.98	V
VDDA_TEMP0	TEMP0 analog supply		-0.3	1.98	V
VDDA_TEMP1	TEMP1 analog supply		-0.3	1.98	V
VPP	eFuse ROM programming supply		-0.3	1.98	V
VDDSHV_MCU	IO supply for IO MCU		-0.3	3.63	V
VDDSHV_CANUART	IO supply for IO CANUART		-0.3	3.63	V
VDDSHV0	IO supply for IO group 0		-0.3	3.63	V
VDDSHV1	IO supply for IO group 1		-0.3	3.63	V
VDDSHV2	IO supply for IO group 2		-0.3	3.63	V
VDDSHV3	IO supply for IO group 3		-0.3	3.63	V
VDDSHV4	IO supply for IO group 4		-0.3	3.63	V
VDDSHV5	IO supply for IO group 5		-0.3	3.63	V
VDDSHV6	IO supply for IO group 6		-0.3	3.63	V
VDDA_3P3_USB	USB0 and USB1 3.3 V analog supply		-0.3	3.63	V
Steady-state max voltage at all fail-safe IO pins		MCU_PORz	-0.3	3.63	V
		MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, and EXTINTn When operating at 1.8V	-0.3	1.98[4]	V
		MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, and EXTINTn When operating at 3.3V	-0.3	3.63[4]	
		VMON_1P8_SOC	-0.3	1.98	V
		VMON_3P3_SOC	-0.3	3.63	V
		VMON_VSYS[5]	-0.3	1.98	V

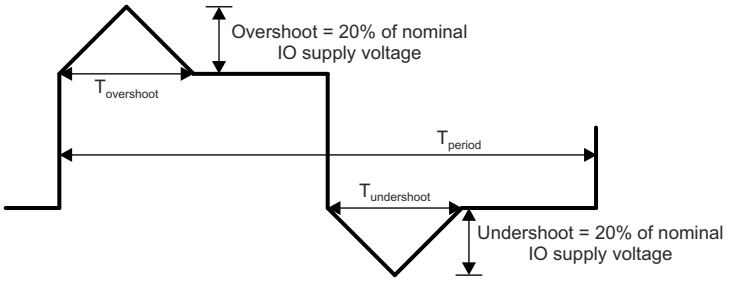
over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER			MIN	MAX	UNIT
Steady-state max voltage at all other IO pins(6)		USB0_VBUS, USB1_VBUS(7)	-0.3	3.6	V
		All other IO pins	-0.3	IO supply voltage + 0.3	V
Transient overshoot and undershoot at IO pin		20% of IO supply voltage for up to 20% of the signal period (see 図 7-1, *IO Transient Voltage Ranges*)		0.2 × VDD(8)	V
Latch-up performance(9)		I-Test	-100	100	mA
		Over-Voltage (OV) Test		1.5 x VDD(8)	V
T_{STG}	Storage temperature		-55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under セクション 7.5, *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) The VDDA_DDR_PLL0 power rail is only available on the AMC package. This power rail is internally connected to VDD_CORE in the ALW package.
(4) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum V_{IH} value found in the *I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics* section, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.
(5) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see セクション 9.2.4, *System Power Supply Monitor Design Guidelines*.
(6) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
(7) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 9.2.3, *USB Design Guidelines*.
(8) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(9) For current pulse injection (I-Test):
- Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For over-voltage performance (Over-Voltage (OV) Test):
- Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn, VMON_1P8_SOC, VMON_3P3_SOC, VMON_VSYS, and MCU_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the "Steady-state max voltage at all other IO pins" parameter in セクション 7.1.



A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

図 7-1. IO Transient Voltage Ranges

7.2 ESD Ratings for Devices which are not AEC - Q100 Qualified

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings for AEC - Q100 Qualified Devices in the AMC Package

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC - Q100-002[1]		±1000	V
		Charged-device model (CDM), per AEC - Q100-011	Corner pins (A1, A21, AA1, and AA21)	±750	
			All other pins	±250	

(1) AEC - Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.4 Power-On Hours (POH)

POWER ON HOURS (POH)[1] [2] [3]		
JUNCTION TEMPERATURE RANGE (T_J)		LIFETIME (POH)
Commercial	0°C to 95°C	100000
Extended Industrial	–40°C to 105°C	100000
Automotive	–40°C to 125°C	20000[4]

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) Automotive profile is defined as 20000 power on hours with a junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

7.5 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDD_CORE(2) VDDA_CORE_CSIRX0(2) VDDA_CORE_USB(2) VDDA_DDR_PLL0(2) (3)	Core supply CSIRX0 core supply USB0 and USB1 core supply DDR Deskew PLL supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDD_CANUART(4)	CANUART core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDDR_CORE	RAM supply		0.81	0.85	0.895	V
VDDS_DDR(5) VDDS_DDR_C(5)	DDR PHY IO supply DDR clock IO supply	1.1-V operation	1.06	1.1	1.17	V
		1.2-V operation	1.14	1.2	1.26	V
VDDS_OSC0	MCU_OSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL0	MAIN PLL, DDR PLL, DSS PLL0, and DSS PLL1 analog supply		1.71	1.8	1.89	V
VDDA_PLL1	PER0 PLL and PER1 PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL2	ARM0 PLL and SMS PLL analog supply		1.71	1.8	1.89	V
VDDA_1P8_CSIRX0	CSIRX0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB	USB0 and USB1 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	TEMP0 analog supply		1.71	1.8	1.89	V
VDDA_TEMP1	TEMP1 analog supply		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		see(6)	see(6)	see(6)	V
VMON_1P8_SOC	Voltage monitor for 1.8 V SoC power supply		1.71	1.8	1.89	V
VDDA_3P3_USB	USB0 and USB1 3.3 V analog supply		3.135	3.3	3.465	V
VMON_3P3_SOC	Voltage monitor for 3.3 V SoC power supply		3.135	3.3	3.465	V
VMON_VSYS	Voltage monitor pin		0	see(7)	1	V
USB0_VBUS	USB0 Level-shifted VBUS Input		0	see(8)	3.465	V
USB1_VBUS	USB1 Level-shifted VBUS Input		0	see(8)	3.465	V
VDDSHV_CANUART(9)	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV_MCU	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV0	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV3	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV4	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV5	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV6	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
T_J	Operating junction temperature range	Automotive	-40		125	°C
		Extended Industrial	-40		105	°C
		Commercial	0		95	°C

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 shall be sourced from the same power source. Care should be taken to ensure that voltage differential between VDD_CORE and VDDA_CORE_USB is within +/- 1%.
(3) The VDDA_DDR_PLL0 power rail is only available on the AMC package. This power rail is internally connected to VDD_CORE in the ALW package.
(4) VDD_CANUART shall be connected to an always on power source when using Partial IO low power mode. VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.
(5) VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source.
(6) Refer to the Recommended Operating Conditions for OTP eFuse Programming table for VPP supply voltages based on eFuse usage.
(7) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see セクション 9.2.4, *System Power Supply Monitor Design Guidelines*.
(8) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 9.2.3, *USB Design Guidelines*.
(9) VDDSHV_CANUART shall be connected to an always on power sources when using Partial IO low power mode. VDDSHV_CANUART shall be connected to any valid IO power source when not using Partial IO low power mode.

7.6 Operating Performance Points

This section describes maximum operating conditions of the device in 表 7-1 and describes each Operating Performance Point (OPP) for processor clocks and device core clocks in 表 7-2.

表 7-1. Device Speed Grades

Speed Grade	VDD_CORE (V)(1)	MAXIMUM OPERATING FREQUENCY (MHz)								MAXIMUM TRANSITION RATE (MT/s)(2)	
		A53SS (Cortex-A53x)	GPU	PRU	Main Infra (CBA)	MCUSS (Cortex-M4F)	Device/ Power Manager (Cortex-R5F)	SMS Subsystem (Dual Cortex-M4F)	OCSRAM	DDR4	LPDDR4
G	0.75/0.85	300	500	250	250	400	400	400	400	1600	1600
K	0.75/0.85	800	500	250	250	400	400	400	400	1600	1600
S	0.75/0.85	1000	500	333	250	400	400	400	400	1600	1600
T	0.75/0.85	1250	500	333	250	400	400	400	400	1600	1600
	0.85	1400									

(1) Nominal operating voltage, see *Recommended Operating Conditions*.
(2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

表 7-2. Device Operating Performance Points

OPP	A53SS(1)	FIXED OPERATING FREQUENCY OPTIONS (MHz)(2)							MT/s(3)	
		GPU	PRU	MAIN INFRA (CBA)	MCUSS	DEVICE/ POWER MANAGER	SMS / SMS CBA	OCSRAM	DDR4	LPDDR4
High	From ARM0 PLL Bypass to Speed Grade Maximum	500	333, 250, or 200	250	400 or 200	400	400	400	1600 (Max)	From DDR PLL Bypass(4) to 1600
Low		N/A		125		133	133	133	250 (DRAM DLL Bypass)	

(1) Default operating frequency, set by software at boot. Supports Dynamic Frequency Scaling after boot.
(2) Fixed operating frequency, set by software at boot.
(3) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.
(4) The DDR PLL output, which sources DDR0_CK0 and DDR0_CK0_n, is typically defined in units of frequency. So the "DDR PLL Bypass" transaction rate is equal to 2x the DDR PLL output frequency when operating in bypass mode.

7.7 Power Consumption Summary

For information on the device power consumption, see the AM62x Power Estimation Tool application note.

7.8 Electrical Characteristics

注

The interfaces or signals described in セクション 7.8 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Signal Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

7.8.1 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.3 × VDD[1]	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD[1]	V
V_{IH}	Input High Voltage		0.7 × VDD[1]		1.98[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD[1]			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDD[1]			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.2 × VDD[1]	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		18f[4] or 1.8E+6			V/s
3.3 V MODE [6]						
V_{IL}	Input Low Voltage				0.3 × VDD[1]	V
V_{ILSS}	Input Low Voltage Steady State				0.25 × VDD[1]	V
V_{IH}	Input High Voltage		0.7 × VDD[1]		3.63[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD[1]			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDD[1]			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.4	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		33f[4] or 3.3E+6		8E+7	V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) This value also defines the Absolute Maximum Ratings value the IO.
(3) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} value for attached components.
(4) f = toggle frequency of the input signal in Hz.
(5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(6) I2C Hs-mode is not supported when operating the IO in 3.3 V mode.

7.8.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC0	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC0			V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
SR_I (2)	Input Slew Rate		18f(1) or 1.8E+6			V/s

(1) f = toggle frequency of the input signal in Hz.
(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.8.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.65 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage			49		mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA

7.8.4 Low-Frequency Oscillator (LFXOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.30 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.70 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA

7.8.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.58	V
V_{ILSS}	Input Low Voltage Steady State				0.58	V
V_{IH}	Input High Voltage		1.27			V
V_{IHSS}	Input High Voltage Steady State		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDDSHV5 - 0.45			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	4			mA
SR_I (3)	Input Slew Rate		18f(2) or 1.8E+6			V/s
3.3 V MODE						
V_{IL}	Input Low Voltage				0.25 × VDDSHV5	V
V_{ILSS}	Input Low Voltage Steady State				0.15 × VDDSHV5	V
V_{IH}	Input High Voltage		0.625 × VDDSHV5			V
V_{IHSS}	Input High Voltage Steady State		0.625 × VDDSHV5			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.125 × VDDSHV5	V
V_{OH}	Output High Voltage		0.75 × VDDSHV5			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	10			mA
SR_I (3)	Input Slew Rate		33f(2) or 3.3E+6			V/s

(1) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(2) f = toggle frequency of the input signal in Hz.
(3) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.8.6 LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3-V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0.0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	9			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.8.7 OLDI LVDS (OLDI) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Voltage, Output High	Differential Load = 100Ω			1.5	V
V_{OL}	Voltage, Output Low		0.925			V
V_{OCM}	Voltage, Output Common Mode		1.125		1.375	V
ΔV_{OCM}	Delta Voltage, Output Common Mode (Difference between high and low steady-states)				30	mV
V_{OD}	Voltage, Output Differential		250		400	mV
ΔV_{OD}	Delta Voltage, Output Differential (Difference between high and low steady-states)				50	mV
I_{OS}	Current, Output Short-Circuit	V = VSS Differential Load = 100Ω			-5	mA
I_{OZ}	Current, Output High-Z	V = VDD(1) or V = VSS	-10	4	40	µA

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

7.8.8 CSI-2 (D-PHY) Electrical Characteristics

注

CSIRX0 is compliant with MIPI DPHY v1.2 dated August 1, 2014 including ECNs and Errata as applicable

7.8.9 USB2PHY Electrical Characteristics

注

The USB0 and USB1 interfaces are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

7.8.10 DDR Electrical Characteristics

注

The DDR interface is compatible with DDR4 devices that are **JESD79-4B standard-compliant**, and LPDDR4 devices that are **JESD209-4B standard-compliant**

7.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses.

7.9.1 Recommended Operating Conditions for OTP eFuse Programming

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)		See セクション 7.5		V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(1)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming(2)	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP current			400	mA
$SR_{(VPP)}$	VPP Slew Rate			6E + 4	V/s
T_j	Operating junction temperature range while programming eFuse ROM.	0	25	85	°C

(1) NC indicates No Connect.
(2) Supply voltage range includes DC errors and peak-to-peak noise.

7.9.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see セクション 7.11.2.2, *Power Supply Sequencing*).

7.9.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in セクション 7.9.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

7.9.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

7.10 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in セクション 7.5, *Recommended Operating Conditions*.

7.10.1 Thermal Resistance Characteristics for ALW and AMC Packages

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	ALW PACKAGE °C/W(1) (2)	AMC PACKAGE °C/W(1) (2)	AIR FLOW (m/s)(3)
T1	$R\Theta_{JC}$	Junction-to-case	3.7	1.2	N/A
T2	$R\Theta_{JB}$	Junction-to-board	8.3	3.9	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	22.3	13.3	0
T4		Junction-to-moving air	15.7	9.7	1
T5			14.5	8.7	2
T6			13.9	8.1	3
T7	Ψ_{JT}	Junction-to-package top	0.2	0.73	0
T8			0.3	0.75	1
T9			0.3	0.76	2
T10			0.3	0.77	3
T11	Ψ_{JB}	Junction-to-board	8.2	3.7	0
T12			7.7	3.4	1
T13			7.6	3.3	2
T14			7.5	3.3	3

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(3) m/s = meters per second.

7.11 Timing and Switching Characteristics

注

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

注

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

7.11.1 Timing Parameters and Information

The timing parameter symbols used in セクション 7.11, *Timing and Switching Characteristics* are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in 表 7-3:

表 7-3. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

7.11.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

注

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions* and *Pin Connectivity Requirements*.

7.11.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/µs. For instance, as shown in 図 7-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 µs.

図 7-2 describes the Power Supply Slew Rate Requirement in the device.

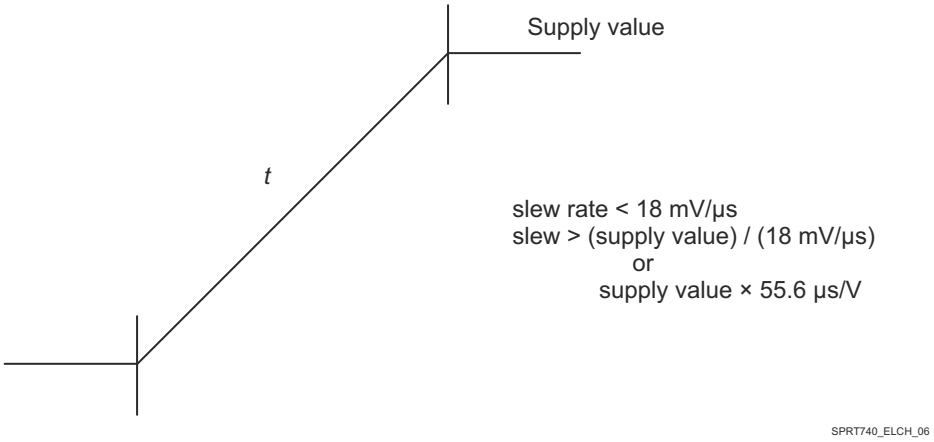


図 7-2. Power Supply Slew and Slew Rate

7.11.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in 図 7-3 and 図 7-4 along with their descriptions are provided to clarify what each transition regions represents.

図 7-3 defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.

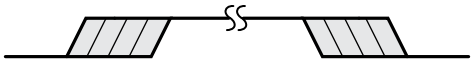


図 7-3. Multiple Power Supply Transition Legend

図 7-4 defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.

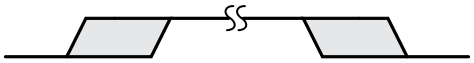


図 7-4. Single Common Power Supply Transition Legend

7.11.2.2.1 Power-Up Sequencing

表 7-4 and 図 7-5 describes the device power-up sequencing.

注

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See セクション 7.11.2.2.3, *Partial IO Power Sequencing* for more information on power supply sequence requirements when entering or exiting low power modes.

表 7-4. Power-Up Sequencing – Supply / Signal Assignments

See: 図 7-5

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_VSYS(2)
B	VDDSHV_CANUART(3), VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VDDA_3P3_USB, VMON_3P3_SOC(4)
C	VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSIRX0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC(6)
D	VDDSHV4(7), VDDSHV5(7), VDDSHV6(7)
E	VDDS_DDR(8), VDDS_DDR_C(8)
F	VDD_CANUART(9)
G	VDD_CANUART(10), VDD_CORE(10) (12), VDDA_CORE_CSIRX0(10), VDDA_CORE_USB0(10), VDDA_DDR_PLL0(10)
H	VDD_CANUART(11), VDD_CORE(11) (12), VDDA_CORE_CSIRX0(11), VDDA_CORE_USB0(11), VDDA_DDR_PLL0(11), VDDR_CORE(12)
I	VPP(13)
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see the *System Power Supply Monitor Design Guidelines*.

(3) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 3.3V, it shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 1.8V, it shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV4, VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(8) VDDS_DDR and VDDS_DDR_C are expected to be powered by the same source such that they ramp together.

(9) VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

When VDD_CANUART is connected to an always-on power source, the potential applied to VDD_CORE must never be greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down. This requires VDD_CANUART to ramp up before and ramp down after VDD_CORE. VDD_CANUART does not have any ramp requirements beyond the one defined for VDD_CORE.

(10) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(11) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(12) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(13) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

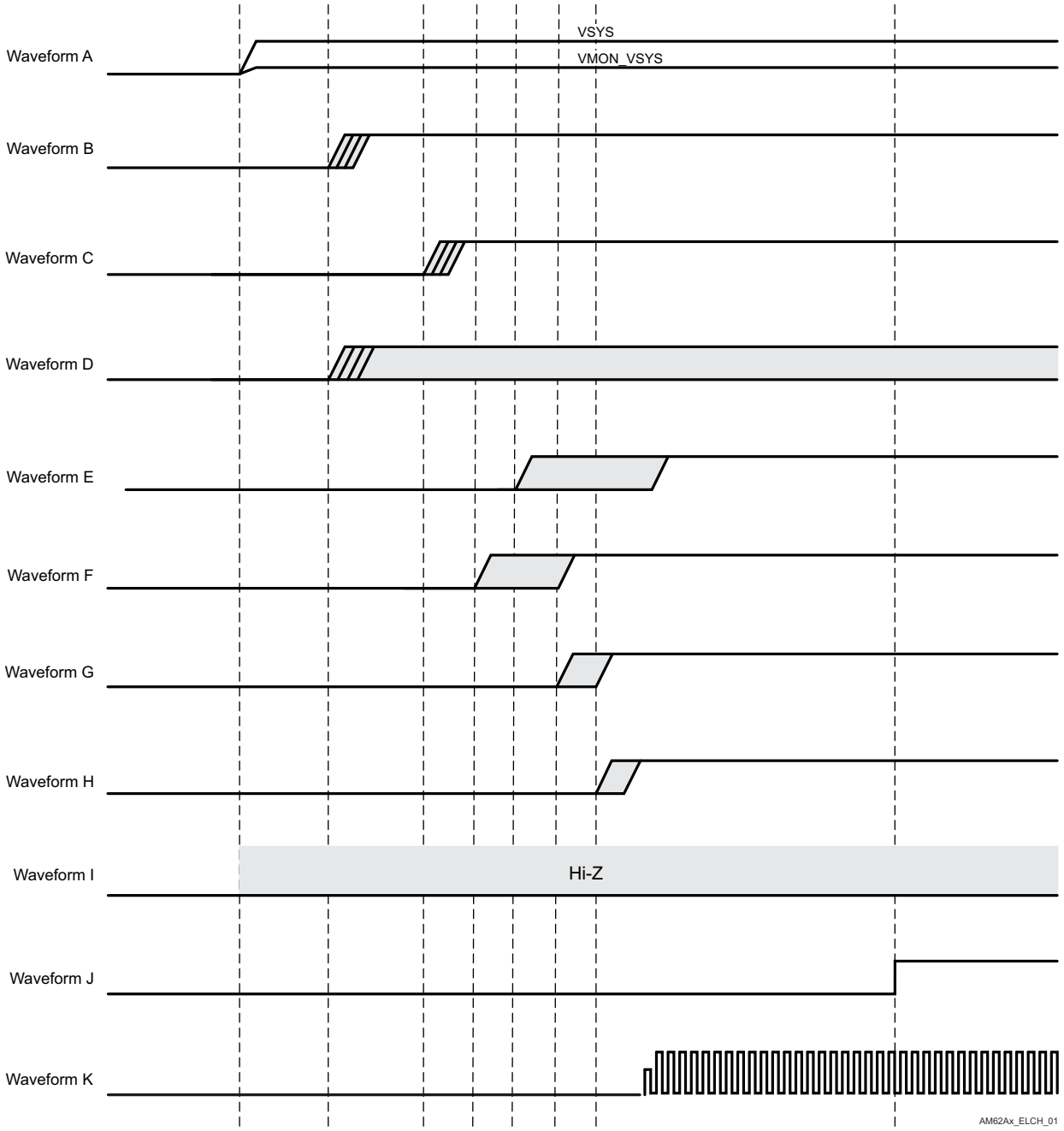


図 7-5. Power-Up Sequencing

7.11.2.2.2 Power-Down Sequencing

表 7-5 and 図 7-6 describes the device power-down sequencing.

注

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See セクション 7.11.2.2.3, *Partial IO Power Sequencing* for more information on power supply sequence requirements when entering or exiting low power modes.

表 7-5. Power-Down Sequencing – Supply / Signal Assignments

See: 図 7-6

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS, VMON_VSYS
B	VDDSHV_CANUART(1), VDDSHV_MCU(1), VDDSHV0(1), VDDSHV1(1), VDDSHV2(1), VDDSHV3(1), VDDA_3P3_USB, VMON_3P3_SOC
C	VDDSHV_CANUART(2), VDDSHV_MCU(2), VDDSHV0(2), VDDSHV1(2), VDDSHV2(2), VDDSHV3(2), VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSIRX0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC
D	VDDSHV4(3), VDDSHV5(3), VDDSHV6(3)
E	VDDS_DDR, VDDS_DDR_C
F	VDD_CANUART(4)
G	VDD_CANUART(5), VDD_CORE(5), VDDA_CORE_CSIRX0(5), VDDA_CORE_USB0(5), VDDA_DDR_PLL0(5)
H	VDD_CANUART(6), VDD_CORE(6), VDDA_CORE_CSIRX0(6), VDDA_CORE_USB0(6), VDDA_DDR_PLL0(6), VDDR_CORE
I	VPP
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 3.3V.
(2) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 1.8V.
(3) VDDSHV4, VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.
(4) VDDSHV_CANUART when connected to an always-on power source for Partial IO low power mode.
(5) VDD_CANUART, VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.75V
(6) VDD_CANUART, VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.85V

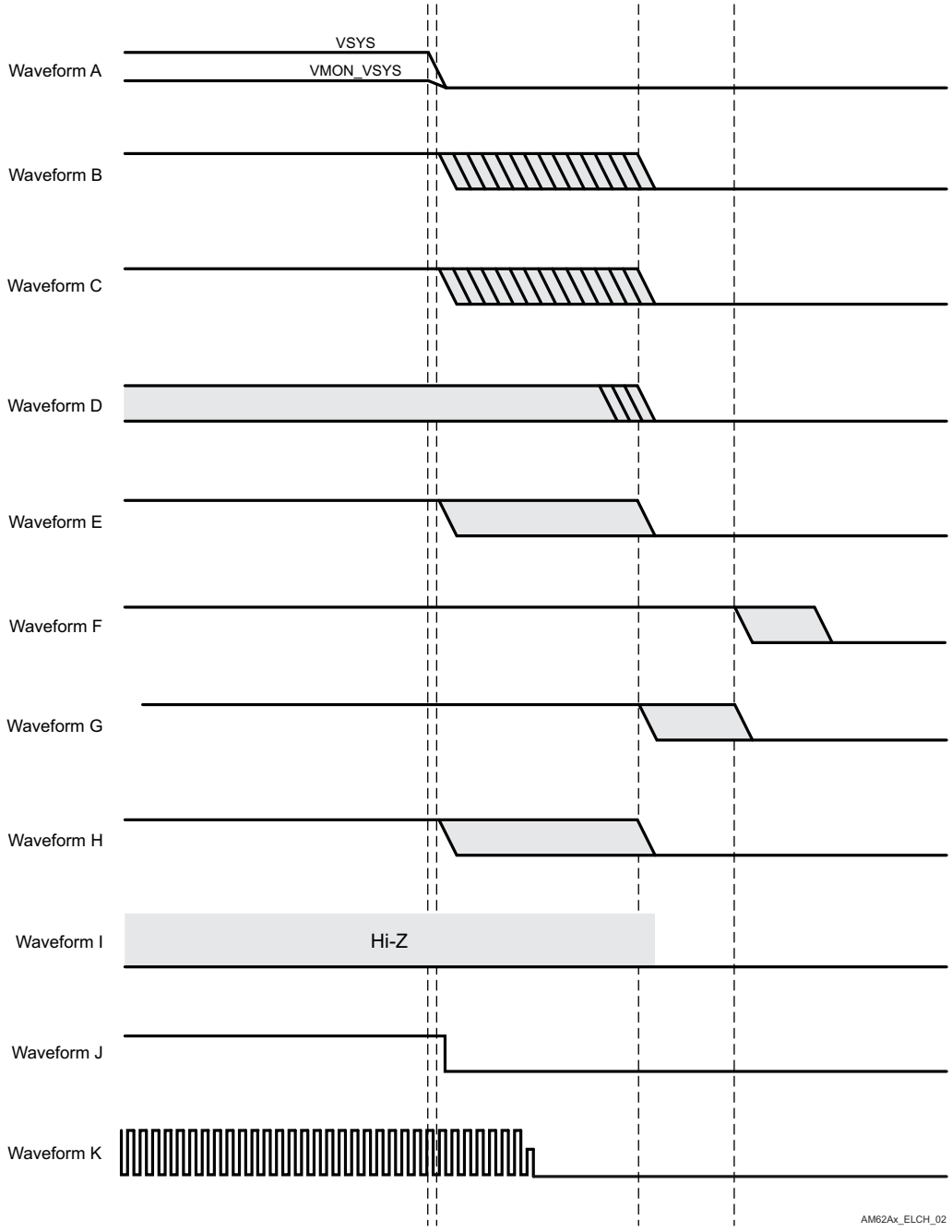


図 7-6. Power-Down Sequencing

7.11.2.2.3 Partial IO Power Sequencing

This section describes power supply sequence requirements when entering or exiting low power modes.

For more information on low power modes supported by this device and the names assigned to each low power mode, see the Power Modes section in the Device Configuration chapter of the Technical Reference Manual.

Partial IO is the only low power mode that requires power supply changes to the device power rails. All power supply rails except VDD_CANUART and VDDSHV_CANUART are turned off when operating in Partial IO mode. The power sequence required to enter Partial IO is the same sequence defined in セクション 7.11.2.2.2, *Power-Down Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which remain powered. The power sequence required to exit Partial IO is the same sequence defined in セクション 7.11.2.2.1, *Power-Up Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which are already powered.

7.11.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.11.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

表 7-6. Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.0033		V/ns
		VDD(1) = 3.3V	0.0018		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance			30	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

表 7-7. MCU_PORz Timing Requirements

see 図 7-7

NO.	PARAMETER		MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID - MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS clock source)	1200		ns
RST3	$t_{w(MCU\_PORzL)}$	Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns

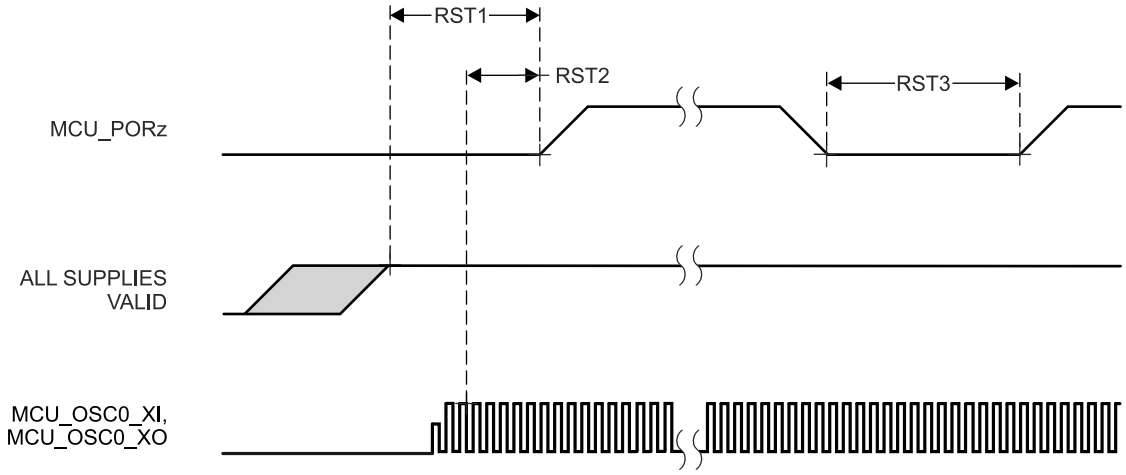


図 7-7. MCU_PORz Timing Requirements

表 7-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 7-8

NO.	PARAMETER		MIN	MAX	UNIT
RST4	$t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)	0		ns
RST5	$t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	6120*S(1)		ns
RST6	$t_{d(MCU\_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)	0		ns
RST7	$t_{d(MCU\_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)	9195*S(1)		ns
RST8	$t_{w(MCU\_RESETSTATzL)}$	Pulse Width, MCU_RESETSTATz low (SW_MCU_WARMRST)	966*S(1)		ns
RST9	$t_{w(RESETSTATzL)}$	Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)	4040*S		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

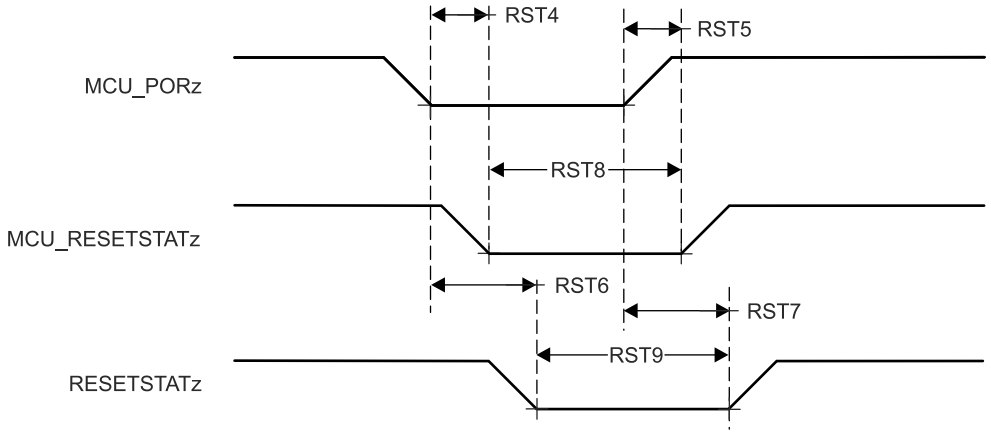


図 7-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

表 7-9. MCU_RESETz Timing Requirements

see 図 7-9

NO.	PARAMETER		MIN	MAX	UNIT
RST10	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width, MCU_RESETz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 7-10. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 7-9

NO.	PARAMETER		MIN	MAX	UNIT
RST11	$t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	0		ns
RST12	$t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	966*S(1)		ns
RST13	$t_{d(MCU\_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	960		ns
RST14	$t_{d(MCU\_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	4040*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

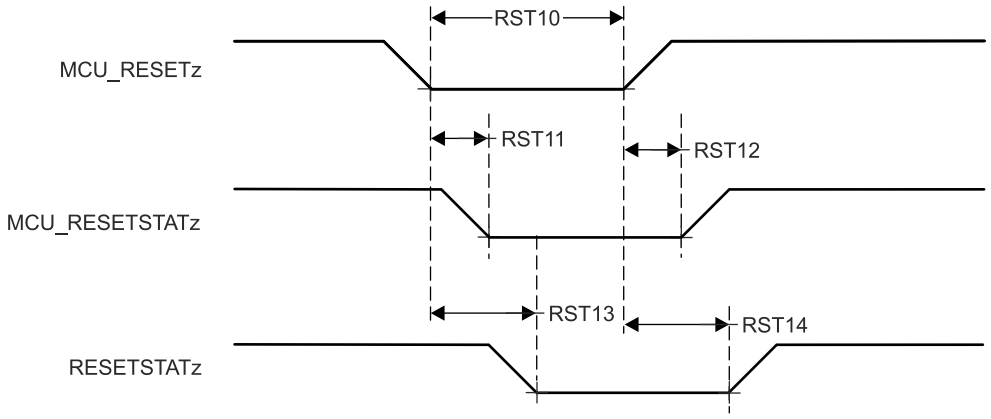


図 7-9. MCU_RESETz, MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

表 7-11. RESET_REQz Timing Requirements

see 図 7-10

NO.	PARAMETER		MIN	MAX	UNIT
RST15	$t_{w(RESET\_REQzL)}$ (1)	Pulse Width, RESET_REQz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 7-12. RESETSTATz Switching Characteristics

see 図 7-10

NO.	PARAMETER		MIN	MAX	UNIT
RST16	$t_{d(RESET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	900*T(1)		ns
RST17	$t_{d(RESET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)	4040*S(2)		ns

(1) T = Reset Isolation Time (Software Dependent)
(2) S = MCU_OSC0_XI/XO clock period in ns.

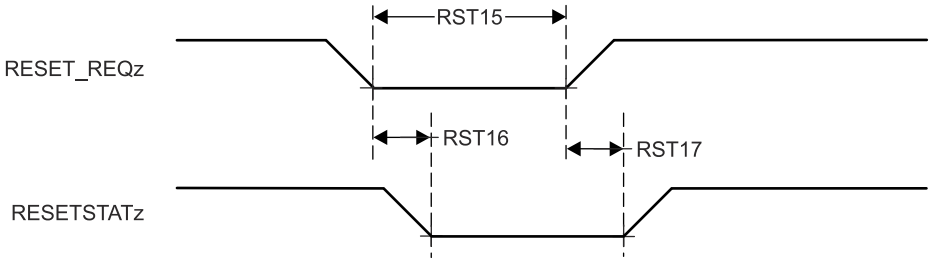


図 7-10. RESET_REQz and RESETSTATz Timing Requirements and Switching Characteristics

表 7-13. EMUx Timing Requirements

see 図 7-11

NO.	PARAMETER		MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST19	$t_{h(MCU\_PORz\ -\ EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

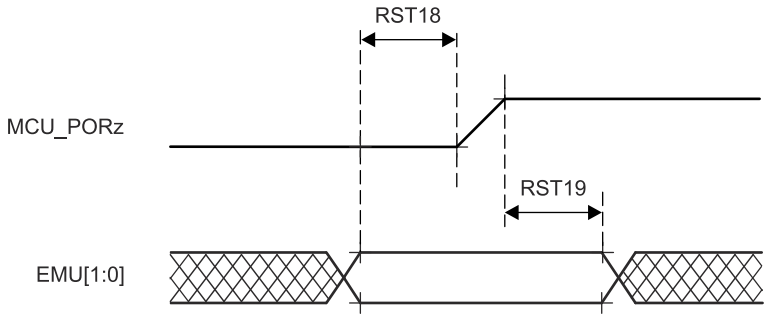


図 7-11. EMUx Timing Requirements

表 7-14. BOOTMODE Timing Requirements

see 図 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S(1)		ns
RST24	$t_{h(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, or Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

表 7-15. PORz_OUT Switching Characteristics

see 図 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST25	$t_{d(MCU\_PORzL-PORz\_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU\_PORzH-PORz\_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	1840		ns
RST27	$t_{w(PORz\_OUTL)}$	Pulse Width, PORz_OUT low (MCU_PORz or SW_MAIN_PORz)	1200		ns

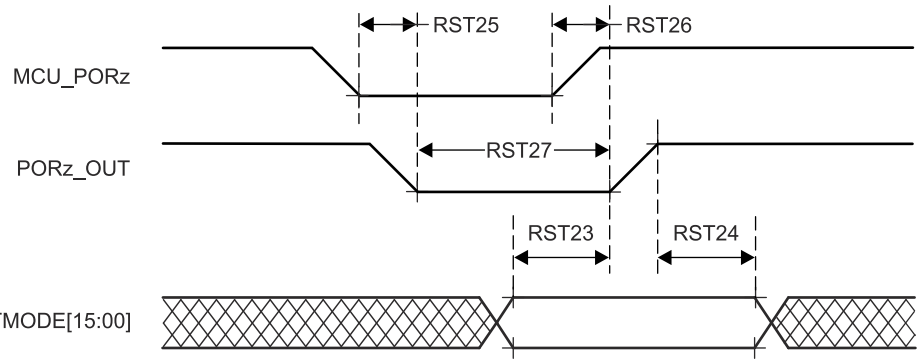


図 7-12. BOOTMODE Timing Requirements and PORz_OUT Switching Characteristics

7.11.3.2 Error Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU_ERRORn.

表 7-16. Error Signal Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance		30	pF

表 7-17. MCU_ERRORn Switching Characteristics

see 図 7-13

NO.	PARAMETER		MIN	MAX	UNIT
ERR1	$t_{c(MCU\_ERRORn)}$	Cycle time minimum, MCU_ERRORn (PWM mode enabled)	(P*H)+(P*L)(1) (3) (4)		ns
ERR2	$t_{w(MCU\_ERRORn)}$	Pulse width minimum, MCU_ERRORn active (PWM mode disabled)(5)	P*R(1) (2)		ns
ERR3	$t_{d\ (ERROR\_CONDITION-MCU\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_ERRORn active(5)	50*P(1)		ns

(1) P = ESM functional clock period in ns.
(2) R = Error Pin Counter Pre-Load Register count value.
(3) H = Error Pin PWM High Pre-Load Register count value.
(4) L = Error Pin PWM Low Pre-Load Register count value.
(5) When PWM mode is enabled, MCU_ERRORn stops toggling after ERR3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU_ERRORn is active low.

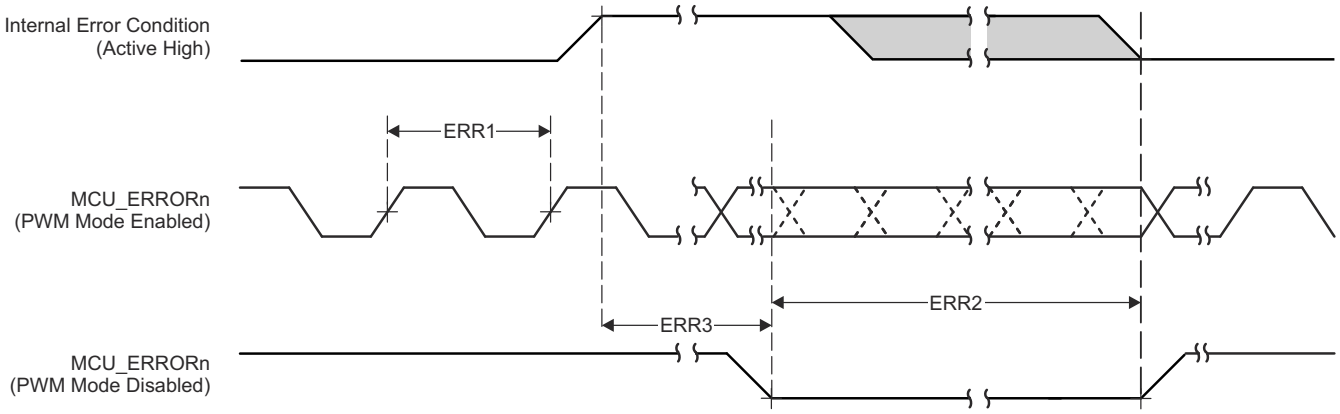


図 7-13. MCU_ERRORn Timing Requirements and Switching Characteristics

7.11.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements and switching characteristics for clock signals.

表 7-18. Clock Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		0.5		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	5 ns ≤ t_c < 8 ns		5	pF
		8 ns ≤ t_c < 20 ns		10	pF
		20 ns ≤ t_c		30	pF

表 7-19. Clock Timing Requirements

see 図 7-14

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns
CLK1	$t_{c(MCU\_EXT\_REFCLK0)}$	Cycle time minimum, MCU_EXT_REFCLK0	10		ns
CLK2	$t_{w(MCU\_EXT\_REFCLK0H)}$	Pulse Duration, MCU_EXT_REFCLK0 high	F*0.45(2)	F*0.55(2)	ns
CLK3	$t_{w(MCU\_EXT\_REFCLK0L)}$	Pulse Duration, MCU_EXT_REFCLK0 low	F*0.45(2)	F*0.55(2)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK0H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.45(3)	G*0.55(3)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK0L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.45(3)	G*0.55(3)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK1H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	H*0.45(4)	H*0.55(4)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK1L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	H*0.45(4)	H*0.55(4)	ns

(1) E = EXT_REFCLK1 cycle time in ns.
(2) F = MCU_EXT_REFCLK0 cycle time in ns.
(3) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(4) H = AUDIO_EXT_REFCLK1 cycle time in ns.

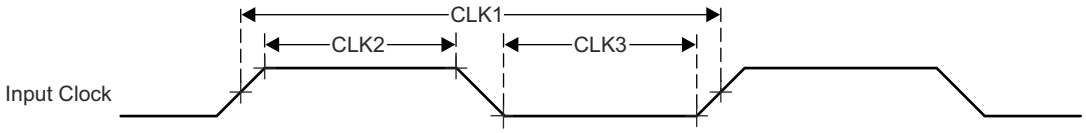


図 7-14. Clock Timing Requirements

表 7-20. Clock Switching Characteristics

see 図 7-15

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK4	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK5	$t_{w(OBSCLK0H)}$	Pulse Duration, OBSCLK0 high	B*0.45(2)	B*0.55(2)	ns
CLK6	$t_{w(OBSCLK0L)}$	Pulse Duration, OBSCLK0 low	B*0.45(2)	B*0.55(2)	ns
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration, CLKOUT0 high	C*0.4(3)	C*0.6(3)	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration, CLKOUT0 low	C*0.4(3)	C*0.6(3)	ns
CLK4	$t_{c(MCU\_SYSCLKOUT0)}$	Cycle time minimum, MCU_SYSCLKOUT0	10		ns
CLK5	$t_{w(MCU\_SYSCLKOUT0H)}$	Pulse Duration, MCU_SYSCLKOUT0 high	E*0.4(4)	E*0.6(4)	ns
CLK6	$t_{w(MCU\_SYSCLKOUT0L)}$	Pulse Duration, MCU_SYSCLKOUT0 low	E*0.4(4)	E*0.6(4)	ns
CLK4	$t_{c(MCU\_OBSCLK0)}$	Cycle time minimum, MCU_OBSCLK0	5		ns
CLK5	$t_{w(MCU\_OBSCLK0H)}$	Pulse Duration, MCU_OBSCLK0 high	D*0.45(5)	D*0.55(5)	ns
CLK6	$t_{w(MCU\_OBSCLK0L)}$	Pulse Duration, MCU_OBSCLK0 low	D*0.45(5)	D*0.55(5)	ns
CLK4	$t_{c(WKUP\_CLKOUT0)}$	Cycle time minimum, WKUP_CLKOUT0	5		ns
CLK5	$t_{w(WKUP\_CLKOUT0H)}$	Pulse Duration, WKUP_CLKOUT0 high	W*0.4(6)	W*0.6(6)	ns
CLK6	$t_{w(WKUP\_CLKOUT0L)}$	Pulse Duration, WKUP_CLKOUT0 low	W*0.4(6)	W*0.6(6)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK0\ )}$	Cycle time minimum, AUDIO_EXT_REFCLK0 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK0 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK0\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.4(7)	G*0.6(7)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK0\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.4(7)	G*0.6(7)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK1\ )}$	Cycle time minimum, AUDIO_EXT_REFCLK1 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK1 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK1\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	J*0.4(8)	J*0.6(8)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK1\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	J*0.4(8)	J*0.6(8)	ns

(1) A = SYSCLKOUT0 cycle time in ns.
(2) B = OBSCLK0 cycle time in ns.
(3) C = CLKOUT0 cycle time in ns.
(4) E = MCU_SYSCLKOUT0 cycle time in ns.
(5) D = MCU_OBSCLK0 cycle time in ns.
(6) W = WKUP_CLKOUT0 cycle time in ns.
(7) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(8) J = AUDIO_EXT_REFCLK1 cycle time in ns.

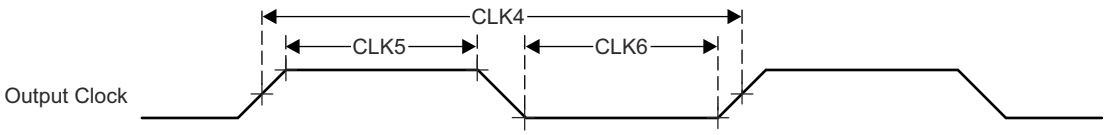


図 7-15. Clock Switching Characteristics

7.11.4 Clock Specifications

7.11.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins connected to the internal high-frequency oscillator (MCU_HFOSC0), which is the default clock source for internal reference clock HFOSC0_CLKOUT.
- WKUP_LFOSC0_XO/WKUP_LFOSC0_XI — external crystal interface pins connected to internal low-frequency oscillator (WKUP_LFOSC0), which sources optional 32768 Hz reference clock.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock.
  - EXT_REFCLK1 — optional external system clock.
- External CPTS reference clock input
  - CP_GEMAC_CPTS0_RFT_CLK — optional reference clock input for CPTS_RFT_CLK.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[1:0] — optional McASP high-frequency input clocks when configured to operate as an input.

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

7.11.4.1.1 MCU_OSC0 Internal Oscillator Clock Source

図 7-16 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins.

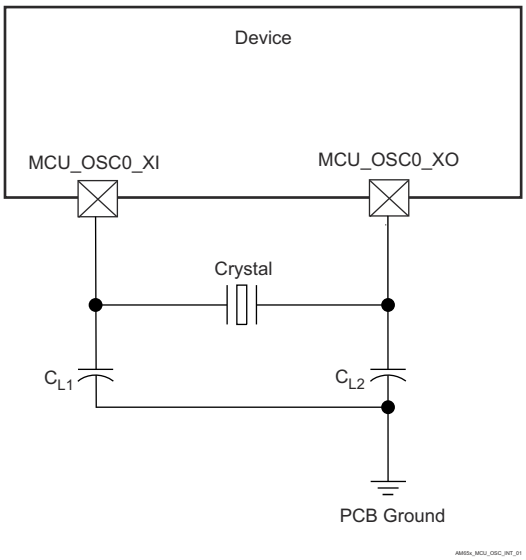


図 7-16. MCU_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 7-21 summarizes the required electrical constraints.

表 7-21. MCU_OSC0 Crystal Circuit Requirements

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				25		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	25 MHz			7	pF
		ESR_{xtal} = 40 Ω	25 MHz			5	pF
		ESR_{xtal} = 50 Ω	25 MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

表 7-22 details the switching characteristics of the oscillator.

表 7-22. MCU_OSC0 Switching Characteristics - Crystal Mode

PARAMETER		PACKAGE	MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance	ALW			0.812	pF
		AMC			1.635	pF

表 7-22. MCU_OSC0 Switching Characteristics - Crystal Mode (continued)

PARAMETER		PACKAGE	MIN	TYP	MAX	UNIT
C_{XO}	XO Capacitance	ALW			0.83	pF
		AMC			1.72	pF
C_{XIXO}	XI to XO Mutual Capacitance	ALW			0.0114	pF
		AMC			0.267	pF
t_s	Start-up Time			4		ms

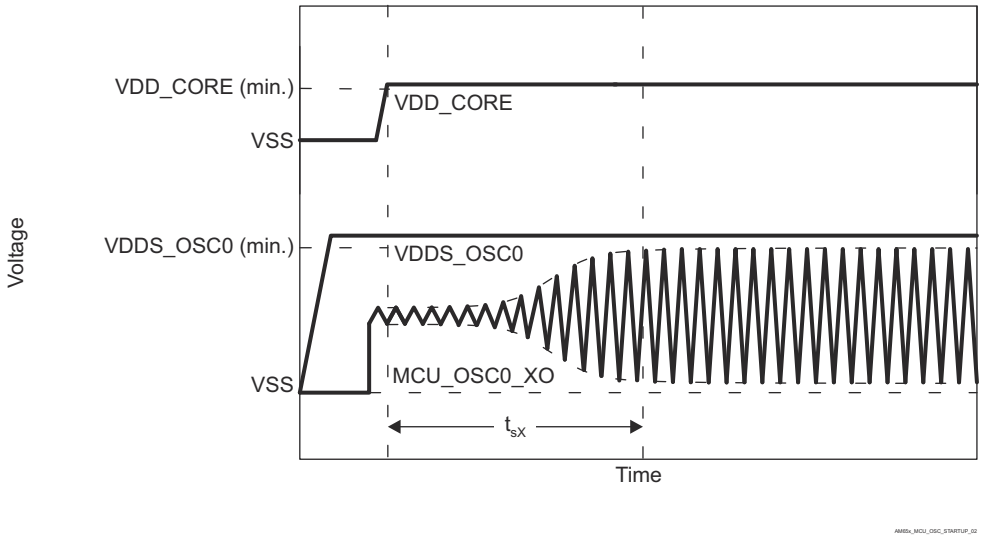


図 7-17. MCU_OSC0 Start-up Time

7.11.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0_XI and MCU_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in 表 7-22.

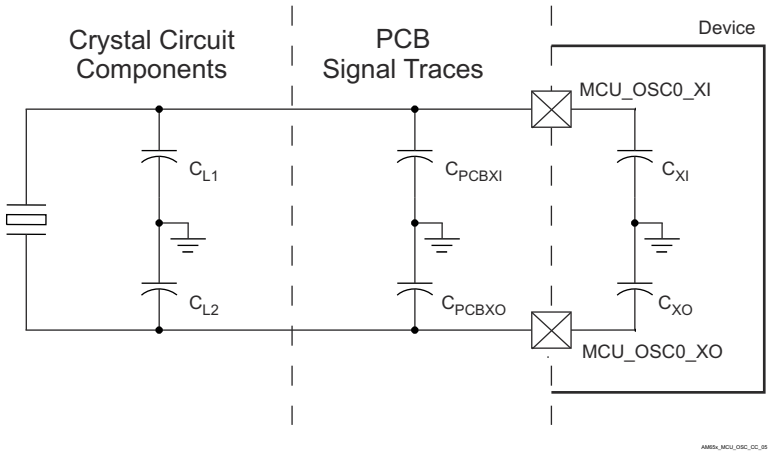


図 7-18. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in 図 7-16, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of C_{L1} = $[(2C_L) - (C_{PCBXI} + C_{XI})]$ = [(2 × 10 pF) - 2.9 pF - 0.5 pF)] = 16.6 pF and C_{L2} = $[(2C_L) - (C_{PCBXO} + C_{XO})]$ = [(2 × 10 pF) - 3.7 pF - 0.5 pF)] = 15.8 pF

7.11.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU_OSC0 operating conditions defined in 表 7-21. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in 表 7-22.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

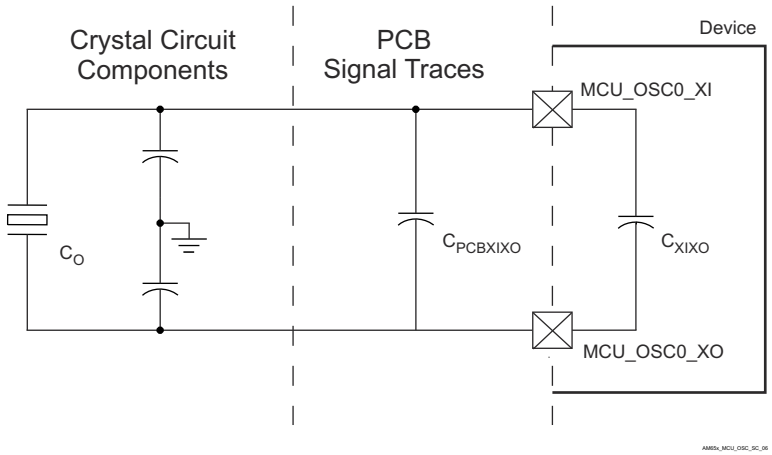


図 7-19. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

7.11.4.1.2 MCU_OSC0 LVCMOS Digital Clock Source

図 7-20 shows the recommended oscillator connections when MCU_OSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

注

A DC steady-state condition is not allowed on MCU_OSC0_XI when the oscillator is powered up. This is not allowed because MCU_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU_OSC0 any time MCU_OSC0_XI is not toggling between logic states.

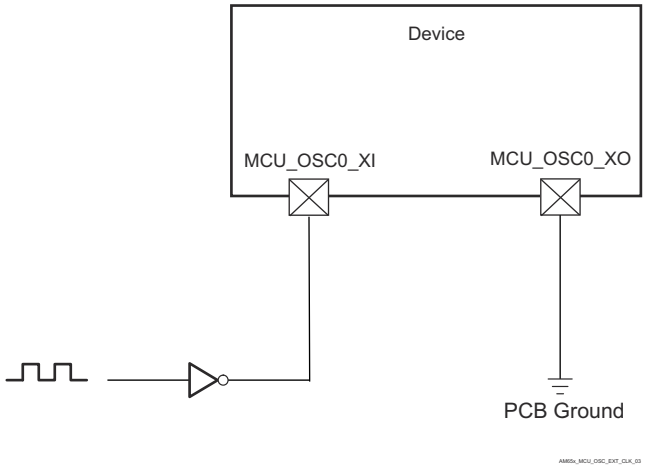


図 7-20. 1.8-V LVCMOS-Compatible Clock Input

7.11.4.1.3 WKUP_LFOSC0 Internal Oscillator Clock Source

図 7-21 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

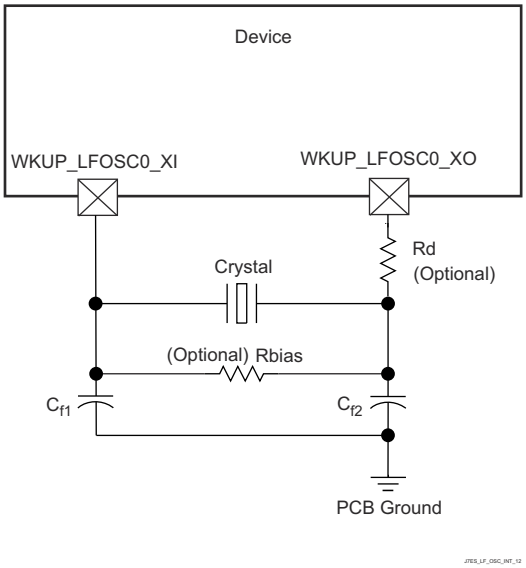


図 7-21. WKUP_LFOSC0 Crystal Implementation

表 7-23 presents LFXOSC modes of operation.

表 7-23. LFXOSC Modes of Operation

MODE	BP_C	PD_C	XI	XO	CLK_OUT	DESCRIPTION
ACTIVE	0	0	XTAL	XTAL	CLK_OUT	Active oscillator mode providing 32kHz
PWRDN	0	1	X	PD	LOW	Output will be pulled down to LOW. PAD to be tri-stated. Active mode disabled
BYPASS	1	0	CLK	PD	CLK	XI is driven by external clock source. XO is pulled down to LOW. Due to ESD diode to supply, XI should not be driven unless oscillator supply is present.

注

User should set CTRLMMR_WKUP_LFXOSC_TRIM[18:16] i_mult = 3b’001 for CL in the range 6pf to 9.5pf. CTRLMMR_WKUP_LFXOSC_TRIM [18:16] i_mult = 3b’010 for CL in the range 8.5pf to 12pf. Default setting is 3b’010.

注

The load capacitors, C_{f1} and C_{f2} in 図 7-22, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

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図 7-22. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 7-24 summarizes the required electrical constraints.

表 7-24. WKUP_LFOSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			32768		Hz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{shunt}	Shunt capacitance	ESRxtal – 40 kΩ			4	pF
		ESRxtal – 60 kΩ			3	pF
		ESRxtal – 80 kΩ			2	pF
		ESRxtal – 100 kΩ			1	pF
ESR	Crystal effective series resistance				(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 7-25 details the switching characteristics of the oscillator and the requirements of the input clock.

表 7-25. WKUP_LFOSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sX}	Start-up time			96.5	ms

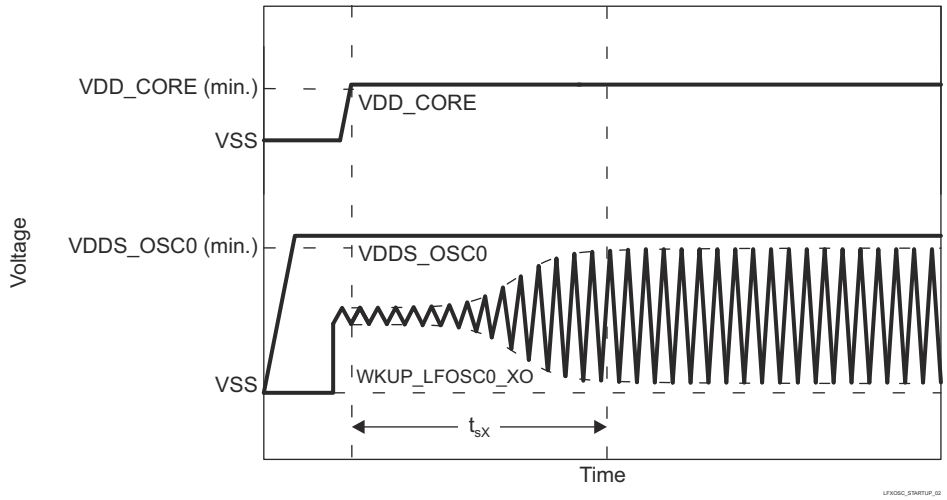


図 7-23. WKUP_LFOSC0 Start-up Time

7.11.4.1.4 WKUP_LFOSC0 LVCMOS Digital Clock Source

図 7-24 shows the recommended oscillator connections when WKUP_LFOSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

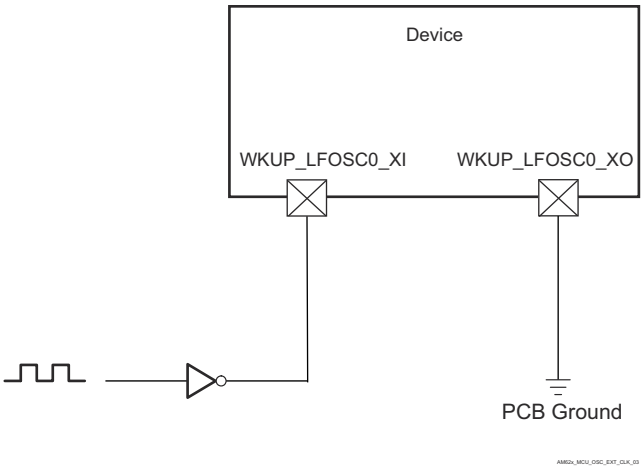


図 7-24. 1.8-V LVCMOS-Compatible Clock Input

7.11.4.1.5 WKUP_LFOSC0 Not Used

図 7-25 shows the recommended oscillator connections when WKUP_LFOSC0 is not used.

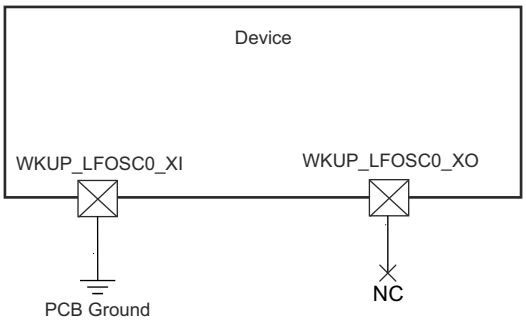


図 7-25. WKUP_LFOSC0 Not Used

7.11.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_SYSCLKOUT0**
  - MCU_PLL0_HSDIV0_CLKOUT (MCU_SYSCLKOUT0) divided by 4 and sent out of the device as MCU_SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **MCU_OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **WKUP_CLKOUT0**
  - WKUP domain CLKOUT0 output.
- **SYSCLKOUT0**
  - MAIN_PLL0_HSDIV0_CLKOUT (SYSCLKOUT0) divided by 4 and then sent out of the device as SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet subsystem clock (MAIN_PLL2_HSDIV1_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided as an optional source to the external PHY. When configured to operate as the RMII Clock source (50 MHz) the signal must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.
- **OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **AUDIO_EXT_REFCLK[1:0]**
  - Option of sourcing one of six McASP high-frequency audio reference clocks, MAIN_PLL1_HSDIV6_CLKOUT, or MAIN_PLL2_HSDIV8_CLKOUT when configured to operate as an output.

7.11.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU PLL

There are eight PLLs in the MAIN domain:

- MAIN PLL
- PER0 PLL
- PER1 PLL
- ARM0 PLL
- DDR PLL
- SMS_PLL
- DSS0 PLL
- DSS1 PLL

The system designer should consider the reference clock source start-up time and the PLL lock requirements before configuring and using any of the PLL outputs as clock sources. The device reference clock input requirements are defined in セクション 7.11.4.1, *Input Clocks / Oscillators*. PLL configuration details are described in the device TRM.

For more information on PLLs, see the *PLL* subsection in the *Clocking* subsection of the *Device Configuration* section in the device TRM.

7.11.4.4 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

7.11.5 Peripherals

7.11.5.1 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.11.5.1.1 CPSW3G MDIO Timing

表 7-26, 表 7-27, 表 7-28, and 図 7-26 present timing conditions, requirements, and switching characteristics for CPSW3G MDIO.

表 7-26. CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

表 7-27. CPSW3G MDIO Timing Requirements

see 図 7-26

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO\_MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(MDC\_MDIO)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

表 7-28. CPSW3G MDIO Switching Characteristics

see 図 7-26

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-150	150	ns

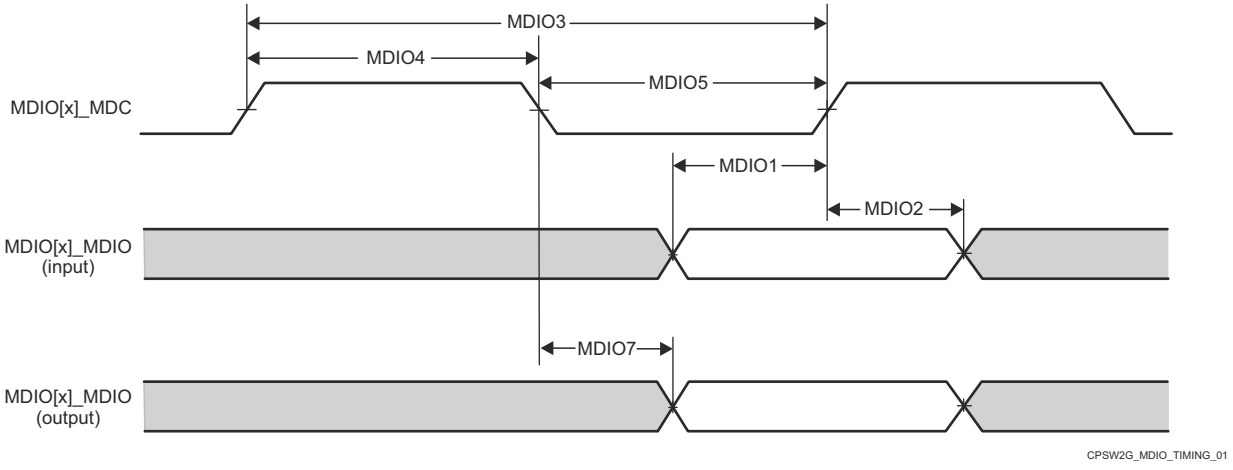


図 7-26. CPSW3G MDIO Timing Requirements and Switching Characteristics

7.11.5.1.2 CPSW3G RMII Timing

表 7-29, 表 7-30, 図 7-27, 表 7-31, 図 7-28, 表 7-32, and 図 7-29 present timing conditions, requirements, and switching characteristics for CPSW3G RMII.

表 7-29. CPSW3G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.18	0.54	V/ns
		VDD(1) = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

表 7-30. RMII[x]_REF_CLK Timing Requirements – RMII Mode

see 図 7-27

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse Duration, RMII[x]_REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse Duration, RMII[x]_REF_CLK Low	7	13	ns

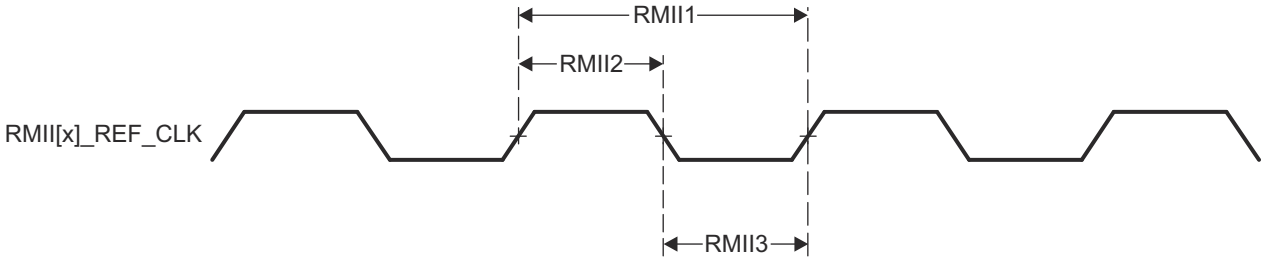


図 7-27. CPSW3G RMII[x]_REF_CLK Timing Requirements – RMII Mode

表 7-31. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

see 図 7-28

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK	4		ns
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK	2		ns

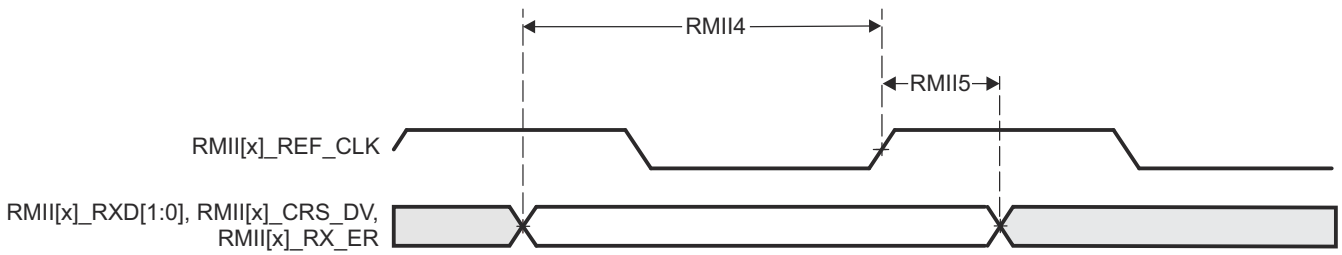


図 7-28. CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

表 7-32. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see 図 7-29

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TX\_EN)}$	Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid	2	10	ns

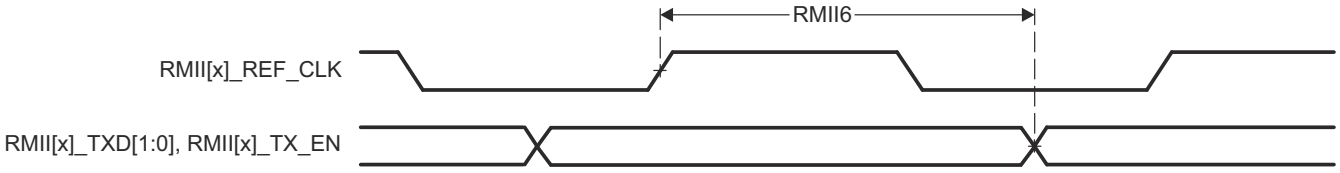


図 7-29. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

7.11.5.1.3 CPSW3G RGMII Timing

表 7-33, 表 7-34, 表 7-35, 図 7-30, 表 7-36, 表 7-37, and 図 7-31 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

表 7-33. CPSW3G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

表 7-34. RGMII[x]_RXC Timing Requirements – RGMII Mode

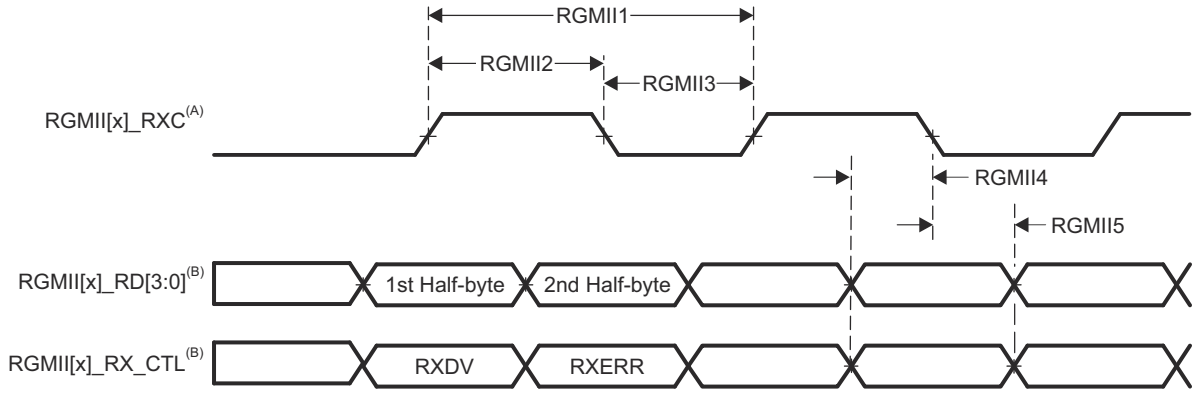
see 図 7-30

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

表 7-35. RGMII[x]_RD[3:0], and RGMII[x]_RX_CTL Timing Requirements – RGMII Mode

see 図 7-30

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

図 7-30. CPSW3G RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

表 7-36. RGMII[x]_TXC Switching Characteristics – RGMII Mode

see 図 7-31

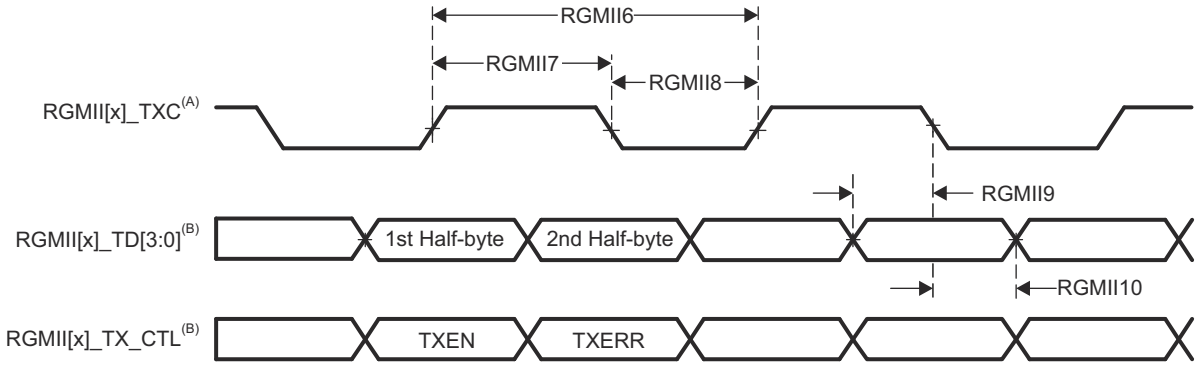
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

表 7-37. RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see 図 7-31

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time(1), RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time(1), RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time(1), RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time(1), RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns

(1) Output setup/hold times are defining a delay relationship of the transmit data and control outputs relative to the transmit clock output, but this output relationship is being presented as the minimum setup/hold times provided to the attached receiver. This approach matches how the output timing relationships are defined in the RGMII specification.



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

図 7-31. CPSW3G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

7.11.5.2 CPTS

表 7-38, 表 7-39, 図 7-32, 表 7-40, and 図 7-33 present timing conditions, requirements, and switching characteristics for CPTS.

表 7-38. CPTS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

表 7-39. CPTS Timing Requirements

see 図 7-32

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w(HWTSPUSHH)}$	Pulse duration, HWnTSPUSH high	12P(1) + 2		ns
T2	$t_{w(HWTSPUSHL)}$	Pulse duration, HWnTSPUSH low	12P(1) + 2		ns
T3	$t_{c(RFT\_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT\_CLKH)}$	Pulse duration, RFT_CLK high	0.45T(2)		ns
T5	$t_{w(RFT\_CLKL)}$	Pulse duration, RFT_CLK low	0.45T(2)		ns

(1) P = functional clock period in ns.
(2) T = RFT_CLK cycle time in ns.

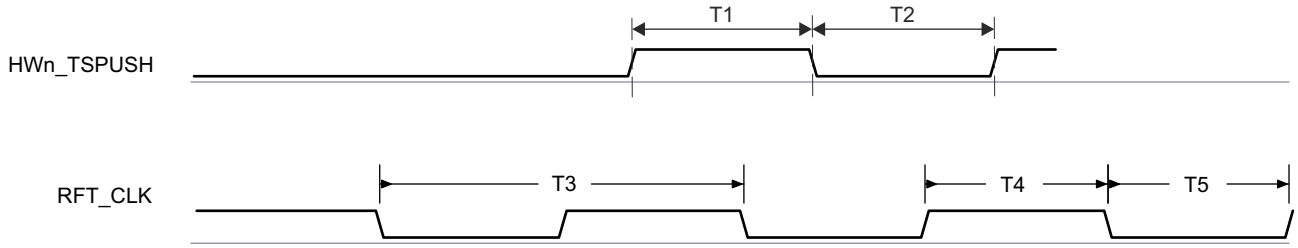


図 7-32. CPTS Timing Requirements

表 7-40. CPTS Switching Characteristics

see 図 7-33

NO.	PARAMETER	DESCRIPTION	SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS\_COMPH)}$	Pulse duration, TS_COMP high		36P(1) - 2		ns
T7	$t_{w(TS\_COMPL)}$	Pulse duration, TS_COMP low		36P(1) - 2		ns
T8	$t_{w(TS\_SYNCH)}$	Pulse duration, TS_SYNC high		36P(1) - 2		ns
T9	$t_{w(TS\_SYNCL)}$	Pulse duration, TS_SYNC low		36P(1) - 2		ns
T10	$t_{w(SYNC\_OUTH)}$	Pulse duration, SYNCn_OUT high	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns
T11	$t_{w(SYNC\_OUTL)}$	Pulse duration, SYNCn_OUT low	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns

(1) P = functional clock period in ns.

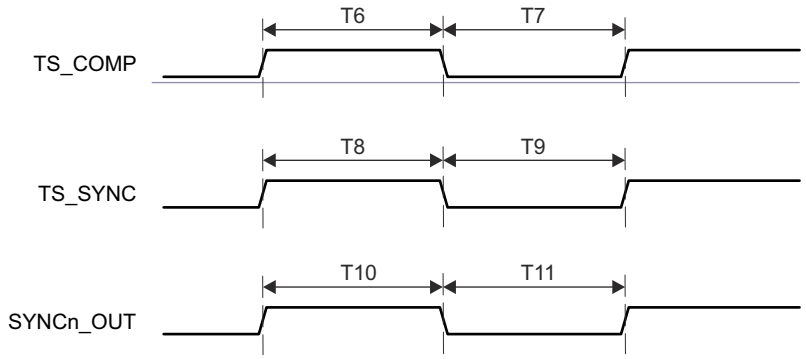


図 7-33. CPTS Switching Characteristics

For more information, see *Data Movement Architecture (DMA)* chapter in the device TRM.

7.11.5.3 CSI-2

注

For more information, see the *Camera Streaming Interface Receiver (CSI_RX_IF)* section in the device TRM.

The CSI_RX_IF deals with the processing of the pixel data coming from an external image sensor. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The CSI_RX_IF has a primary serial interface CSI-2 port (CSIRX0) compliant with the MIPI D-PHY RX specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane in synchronous mode, double data rate. Refer to the MIPI specifications for timing details.

- Support for 1,2,3 or 4 data lane mode up to 1.5Gbps

7.11.5.4 DDRSS

For more details about features and additional description information on the device (LP)DDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-41 and 図 7-34 present switching characteristics for DDRSS.

表 7-41. DDRSS Switching Characteristics

see 図 7-34

NO.	PARAMETER		DDR TYPE	MIN	MAX	UNIT
1	$t_{c(DDR\_CKP/DDR\_CKN)}$	Cycle time, DDR_CKP and DDR_CKN	LPDDR4	1.25(1)	20	ns
			DDR4	1.25(1)	1.6	ns

(1) Minimum DDR clock Cycle time will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

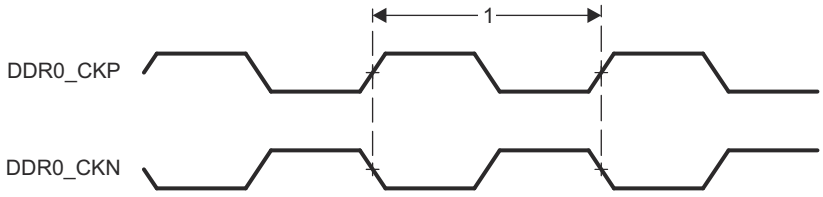


図 7-34. DDRSS Switching Characteristics

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

7.11.5.5 DSS

表 7-42, 表 7-43, 図 7-35, 表 7-44 and 図 7-36 present timing conditions, requirements, and switching characteristics for DSS.

表 7-42. DSS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.44	26.4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 7-43. DSS External Pixel Clock Timing Requirements

see 図 7-35

NO.			MIN	MAX	UNIT
D6	$t_{c(extpclkin)}$	Cycle time, VOUT(x)_EXTPCLKIN(2)	6.06		ns
D7	$t_{w(extpclkinL)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) low	0.475P(1)		ns
D8	$t_{w(extpclkinH)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) high	0.475P(1)		ns

(1) P = VOUT(x)_EXTPCLKIN cycle time in ns
(2) x in VOUT(x) = 0

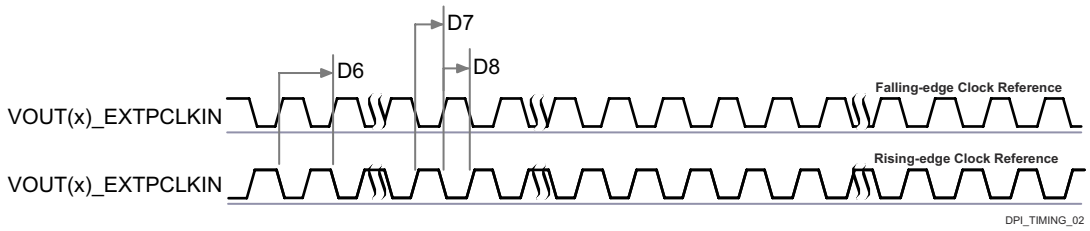


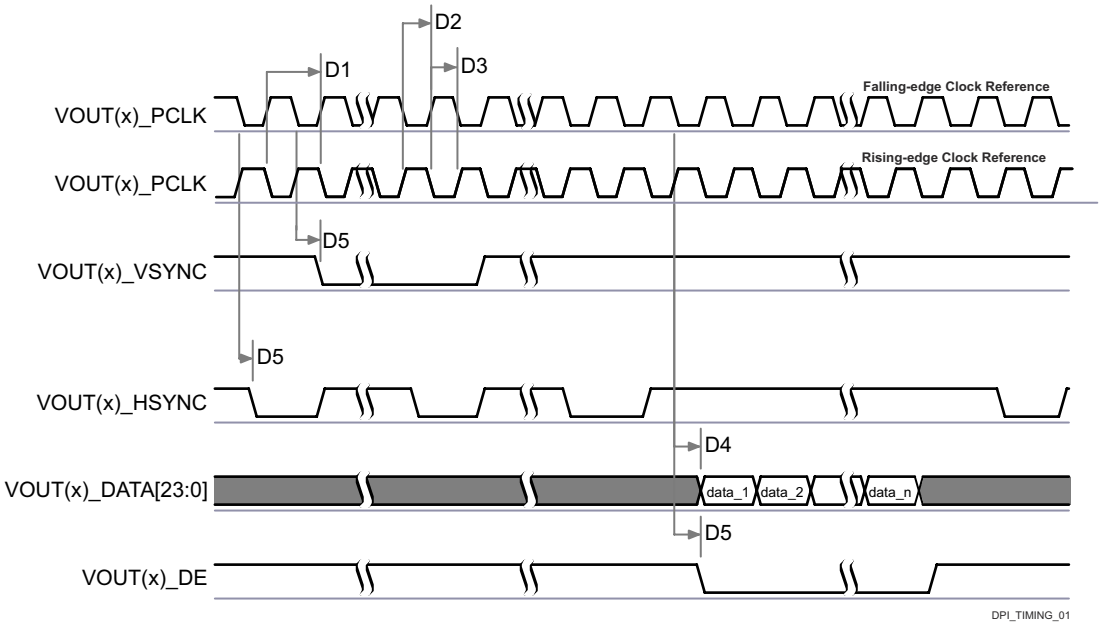
図 7-35. DSS External Pixel Clock Timing Requirements

表 7-44. DSS Switching Characteristics

see 図 7-36

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, VOUT(x)_PCLK(2)		6.06		ns
D2	$t_{w(pclkL)}$	Pulse duration, VOUT(x)_PCLK(2) low	Internal PLL	0.475P(1) - 0.3		ns
			EXTPCLKIN	Y(3) - 0.45		ns
D3	$t_{w(pclkH)}$	Pulse duration, VOUT(x)_PCLK(2) high	Internal PLL	0.475P(1) -0.3		ns
			EXTPCLKIN	Z(4) - 0.45		ns
D4	$t_{d(pclkV-dataV)}$	Delay time, VOUT(x)_PCLK(2) transition to VOUT(x)_DATA[23:0](2) transition	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns
D5	$t_{d(pclkV-ctrlL)}$	Delay time, VOUT(x)_PCLK(2) transition to control signals VOUT(x)_VSYNC(2), VOUT(x)_HSYNC(2), VOUT(x)_DE(2) falling edge	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns

(1) P = VOUT(x)_PCLK cycle time in ns
(2) x in VOUT(x) = 0
(3) Y = $t_{w(extpclkinL)}$, parameter D7 from 表 7-43, *DSS External Pixel Clock Timing Requirements*
(4) Z = $t_{w(extpclkinH)}$, parameter D8 from 表 7-43, *DSS External Pixel Clock Timing Requirements*



A. The assertion of data can be programmed to occur on the falling or rising edge of the pixel clock. Refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
B. The polarity and pulse width of VOUT(x)_HSYNC and VOUT(x)_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
C. The VOUT(x)_PCLK frequency is configurable, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.

図 7-36. DSS Switching Characteristics

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter of the device TRM.

7.11.5.6 ECAP

表 7-45, 表 7-46, 図 7-37, 表 7-47, and 図 7-38 present timing conditions, requirements, and switching characteristics for ECAP.

表 7-45. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 7-46. ECAP Timing Requirements

see 図 7-37

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Pulse duration, CAP (asynchronous)	2P(1) + 2		ns

(1) P = sysclk period in ns.

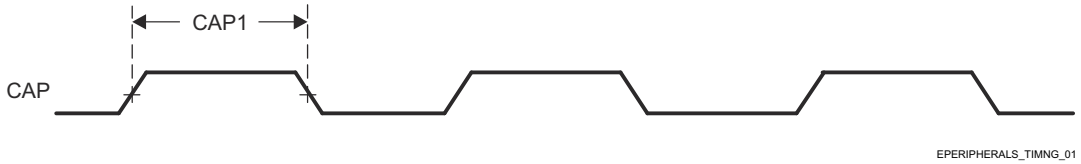


図 7-37. ECAP Timings Requirements

表 7-47. ECAP Switching Characteristics

see 図 7-38

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx high/low	2P(1) - 2		ns

(1) P = sysclk period in ns.

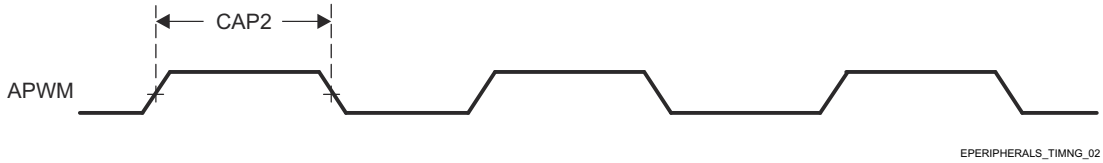


図 7-38. ECAP Switching Characteristics

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

7.11.5.7 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.11.5.7.1 Trace

表 7-48. Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces		200	ps

表 7-49. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.83		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.66		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.66		ns
DBTR4	$t_{osu(TRC\_DATAV\text{-}TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.85		ns
DBTR5	$t_{oh(TRC\_CLK\text{-}TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.85		ns
DBTR6	$t_{osu(TRC\_CTLV\text{-}TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.85		ns
DBTR7	$t_{oh(TRC\_CLK\text{-}TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.85		ns
3.3V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	8.78		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	3.64		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	3.64		ns
DBTR4	$t_{osu(TRC\_DATAV\text{-}TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.10		ns
DBTR5	$t_{oh(TRC\_CLK\text{-}TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.10		ns
DBTR6	$t_{osu(TRC\_CTLV\text{-}TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.10		ns
DBTR7	$t_{oh(TRC\_CLK\text{-}TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.10		ns

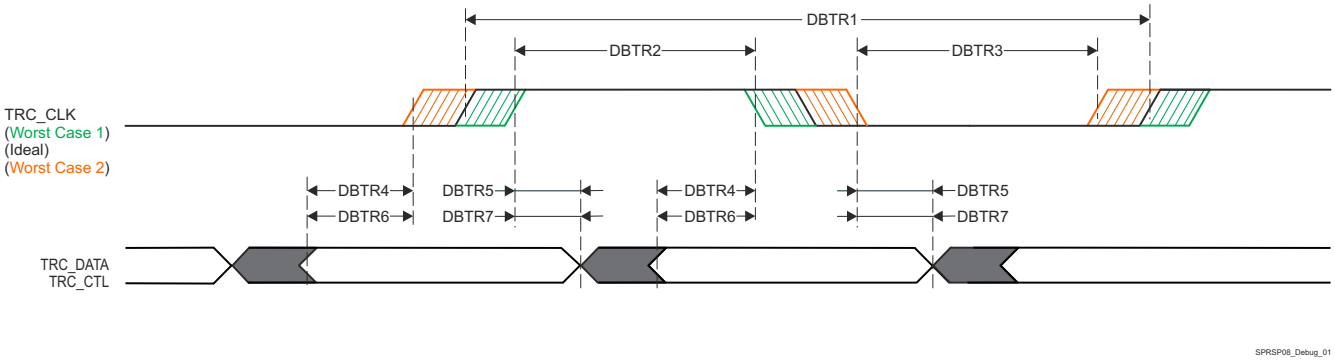


図 7-39. Trace Switching Characteristics

7.11.5.7.2 JTAG

表 7-50. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2.0	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

表 7-51. JTAG Timing Requirements

see 図 7-40

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	40(1)		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	0.4P(2)		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	0.4P(2)		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	2		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	3		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	3		ns

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristis for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 2 ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of -12.9 ns to 13.9 ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

表 7-52. JTAG Switching Characteristics

see 図 7-40

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		12	ns

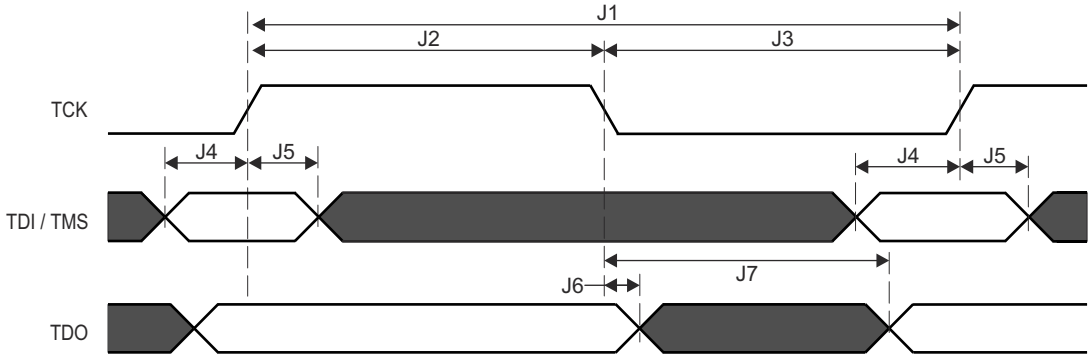


図 7-40. JTAG Timing Requirements and Switching Characteristics

7.11.5.8 EPWM

表 7-53, 表 7-54, 図 7-41, 表 7-55, 図 7-42, 図 7-43, and 図 7-44 present timing conditions, requirements, and switching characteristics for EPWM.

表 7-53. EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 7-54. EPWM Timing Requirements

see 図 7-41

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2P(1) + 2		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	3P(1) + 2		ns

(1) P = sysclk period in ns.

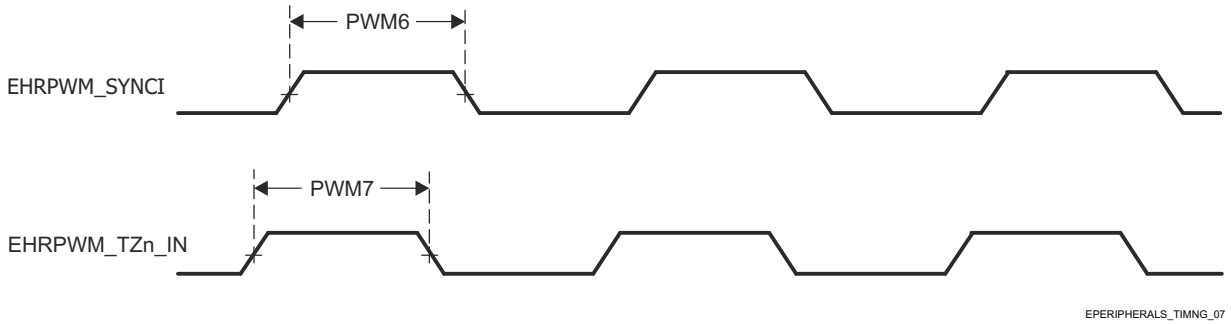


図 7-41. EPWM Timing Requirements

表 7-55. EPWM Switching Characteristics

see 図 7-42, 図 7-43, and 図 7-44

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	P(1) - 3		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	P(1) - 3		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	P(1) - 3		ns

(1) P = sysclk period in ns.

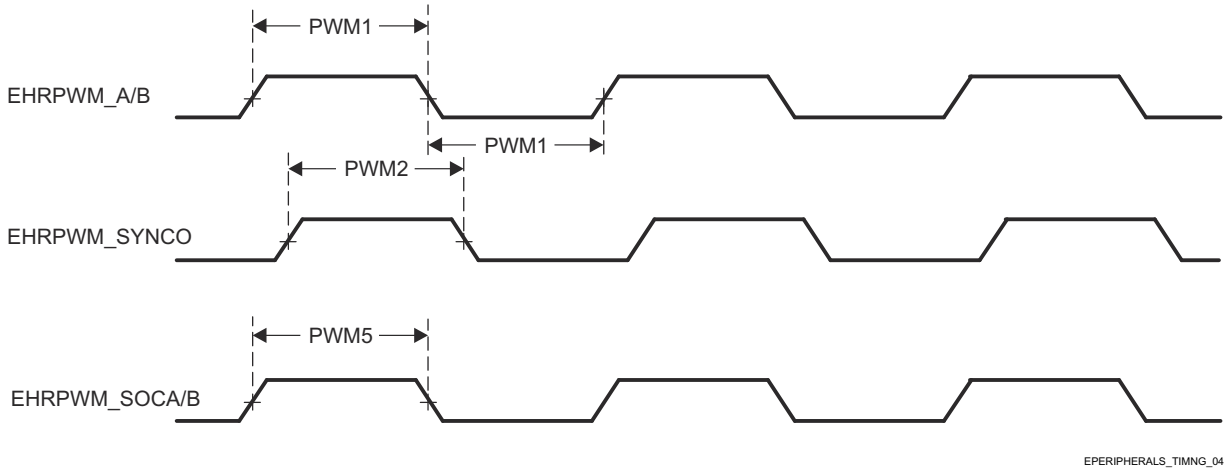


図 7-42. EHRPWM Switching Characteristics

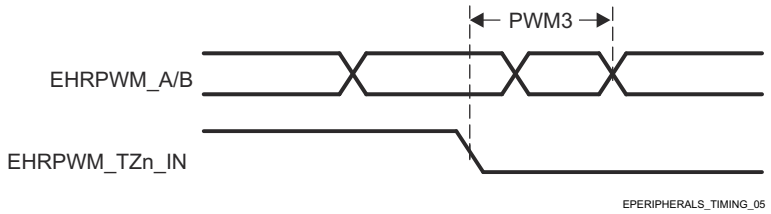


図 7-43. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

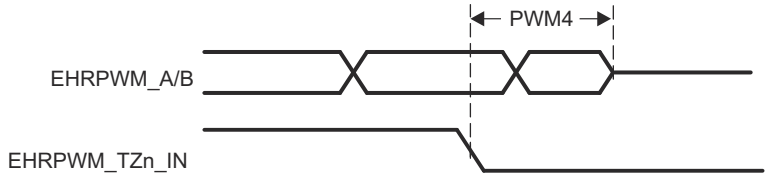


図 7-44. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

7.11.5.9 EQEP

表 7-56, 表 7-57, 図 7-45, and 表 7-58 present timing conditions, requirements, and switching characteristics for EQEP.

表 7-56. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 7-57. EQEP Timing Requirements

see 図 7-45

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	$t_{w(QEP)}$	Pulse duration, QEP_A/B	2P(1) + 2		ns
QEP2	$t_{w(QEPIH)}$	Pulse duration, QEP_I high	2P(1) + 2		ns
QEP3	$t_{w(QEPIL)}$	Pulse duration, QEP_I low	2P(1) + 2		ns
QEP4	$t_{w(QEPSH)}$	Pulse duration, QEP_S high	2P(1) + 2		ns
QEP5	$t_{w(QEPSL)}$	Pulse duration, QEP_S low	2P(1) + 2		ns

(1) P = sysclk period in ns

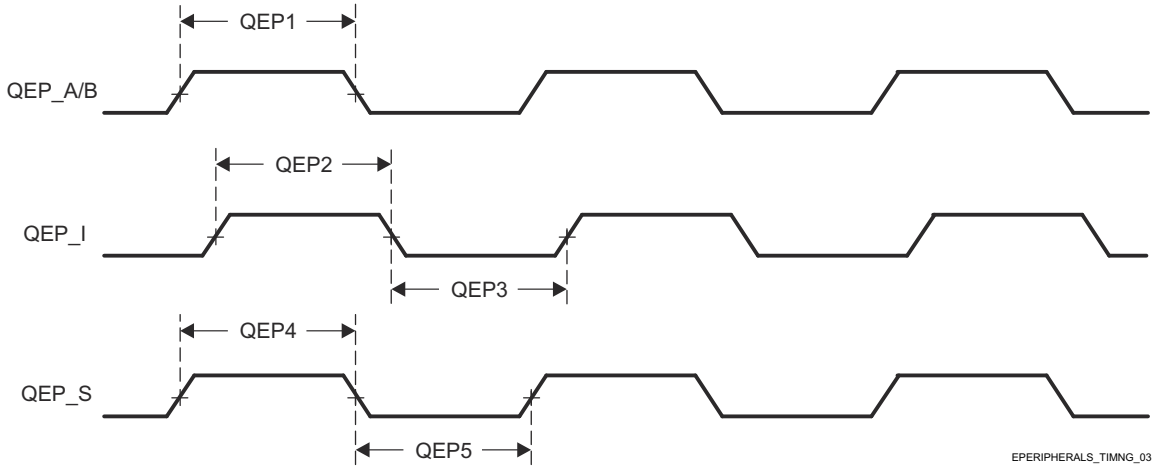


図 7-45. EQEP Timing Requirements

表 7-58. EQEP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

7.11.5.10 GPIO

表 7-59, 表 7-60, and 表 7-61 present timing conditions, requirements, and switching characteristics for GPIO.

The device has three instances of the GPIO module.

- MCU_GPIO0
- GPIO0
- GPIO1

注

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-59. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	LVCMOS	0.2	6.6	V/ns
		I2C OD FS	0.2	0.8	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

表 7-60. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
GPIO1	$t_{w(GPIO\_IN)}$	Pulse width, GPIOn_x	1.8 V	2P + 2.6(1)		ns
			3.3 V	2P + 3.5(1)		ns

(1) P = functional clock period in ns.

表 7-61. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	$t_{w(GPIO\_OUT)}$	Pulse width, GPIOn_x	LVCMOS	0.975P(1) - 3.6		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

7.11.5.11 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-62 presents timing conditions for GPMC.

表 7-62. GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

7.11.5.11.1 GPMC and NOR Flash — Synchronous Mode

表 7-63 and 表 7-64 present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

表 7-63. GPMC and NOR Flash Timing Requirements — Synchronous Mode

see 図 7-46, 図 7-47, and 図 7-50

NO.	PARAMETER	DESCRIPTION	MODE(4)	MIN MAX GPMC_FCLK = 100 MHz(1)	MIN MAX GPMC_FCLK = 133 MHz(1)	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j](2) (3) valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j](2) (3) valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns

(1) GPMC_FCLK select

- gpmc_fclk_sel[1:0] = 2b01 to select the 100MHz GPMC_FCLK
- gpmc_fclk_sel[1:0] = 2b00 to select the 133MHz GPMC_FCLK

(2) In GPMC_WAIT[j], j is equal to 0 or 1.

(3) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For not_div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 7-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode

see 図 7-46, 図 7-47, 図 7-48, 図 7-49, and 図 7-50

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F0	1 / tc(clk)	Period, output clock GPMC_CLK(15)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10.00		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3(14)		0.475P - 0.3(14)		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3(14)		0.475P - 0.3(14)		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	F - 2.2 (5)	F + 3.75	F - 2.2 (5)	F + 3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.2 (4)	E + 3.18	E - 2.2 (4)	E + 4.5	ns
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 4.5	B - 2.3 (2)	B + 4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-2.3	4.5	-2.3	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 1.9	B - 2.3 (2)	B + 1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3(3)	D + 1.9	D - 2.3 (3)	D + 1.9	ns

表 7-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see 図 7-46, 図 7-47, 図 7-48, 図 7-49, and 図 7-50

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100 MHz	MIN MAX 133 MHz	UNIT
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3) D + 1.9	D - 2.3 (3) D + 1.9	ns
F7	$t_{d(clkL-be[x]nIV).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3) D + 1.9	D - 2.3 (3) D + 1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	G - 2.3(6) G + 4.5	G - 2.3 (6) G + 4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	D - 2.3 (3) D + 4.5	D - 2.3 (3) D + 4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 (7) H + 3.5	H - 2.3 (7) H + 3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 (7) H + 3.5	H - 2.3 (7) H + 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	I - 2.3 (8) I + 4.5	I - 2.3 (8) I + 4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F15	$t_{d(clkL-do).}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns
F17	$t_{d(clkL-be[x]n).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read	A	A	ns
			Write	A	A	ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C	C	ns
			Write	C	C	ns

表 7-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see 図 7-46, 図 7-47, 図 7-48, 図 7-49, and 図 7-50

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100 MHz	MIN MAX 133 MHz	UNIT
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K	K	ns
			Write	K	K	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK(14)

(3) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(4) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(5) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(6) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)

- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(7) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK (14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) J = GPMC_FCLK(14)
(10) First transfer only for CLK DIV 1 mode.
(11) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(12) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
(14) P = GPMC_CLK period in ns
(15) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(16) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

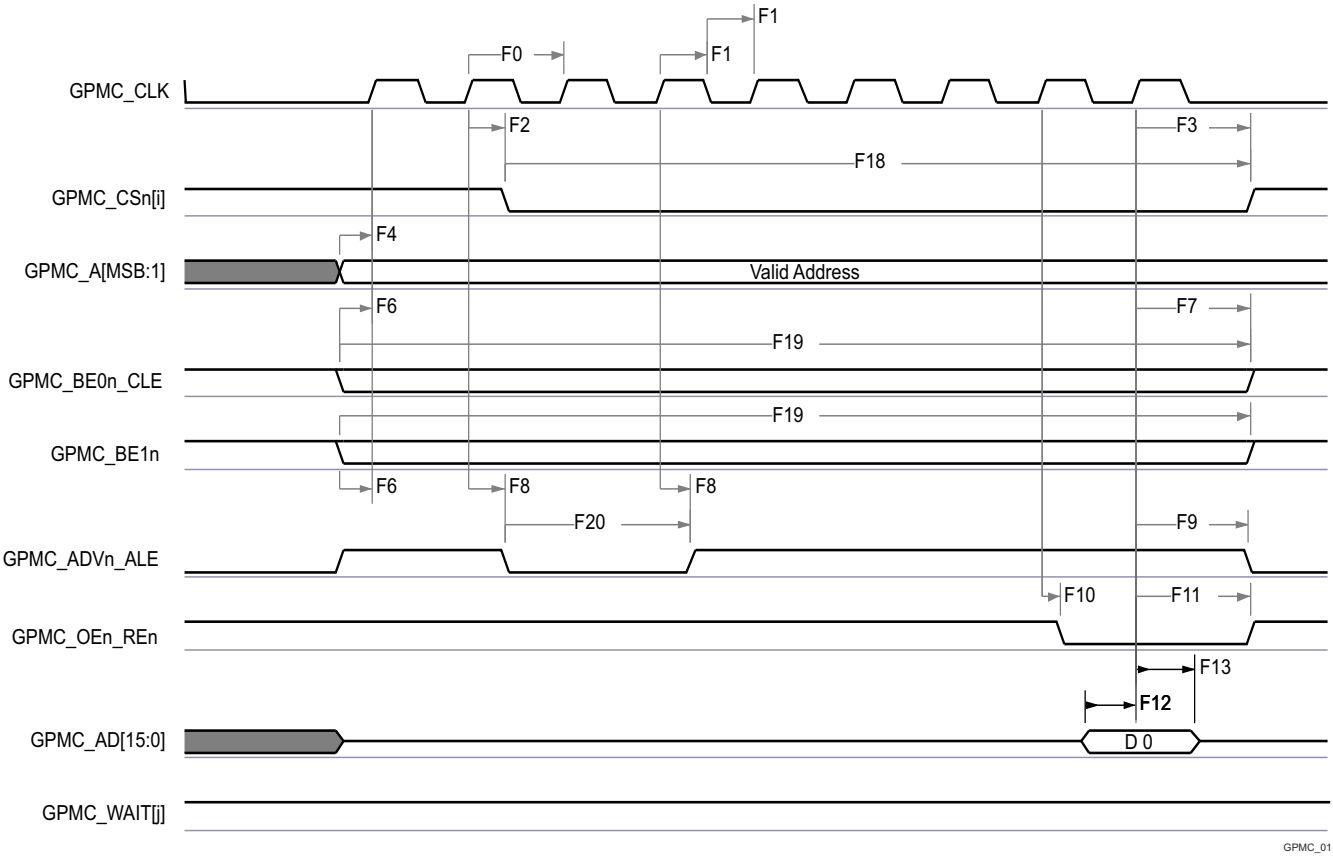
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

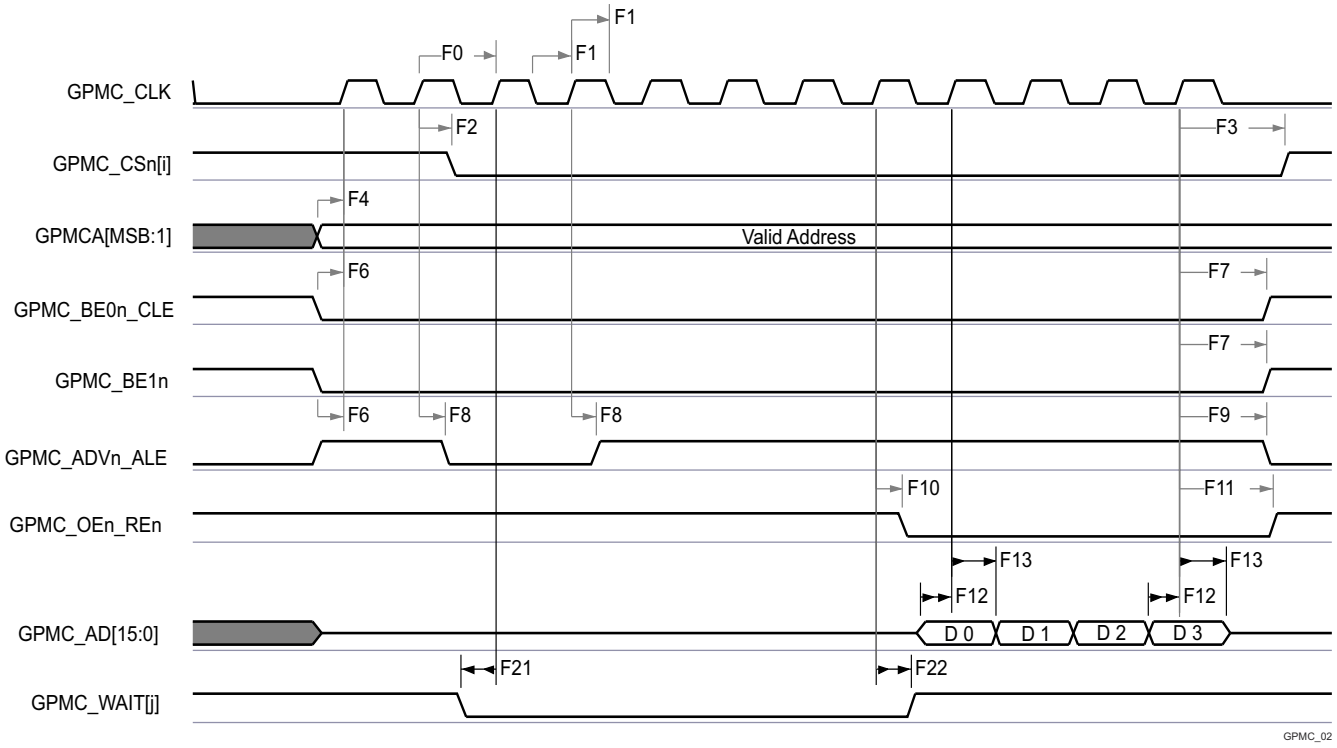
For no extra_delay:

- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



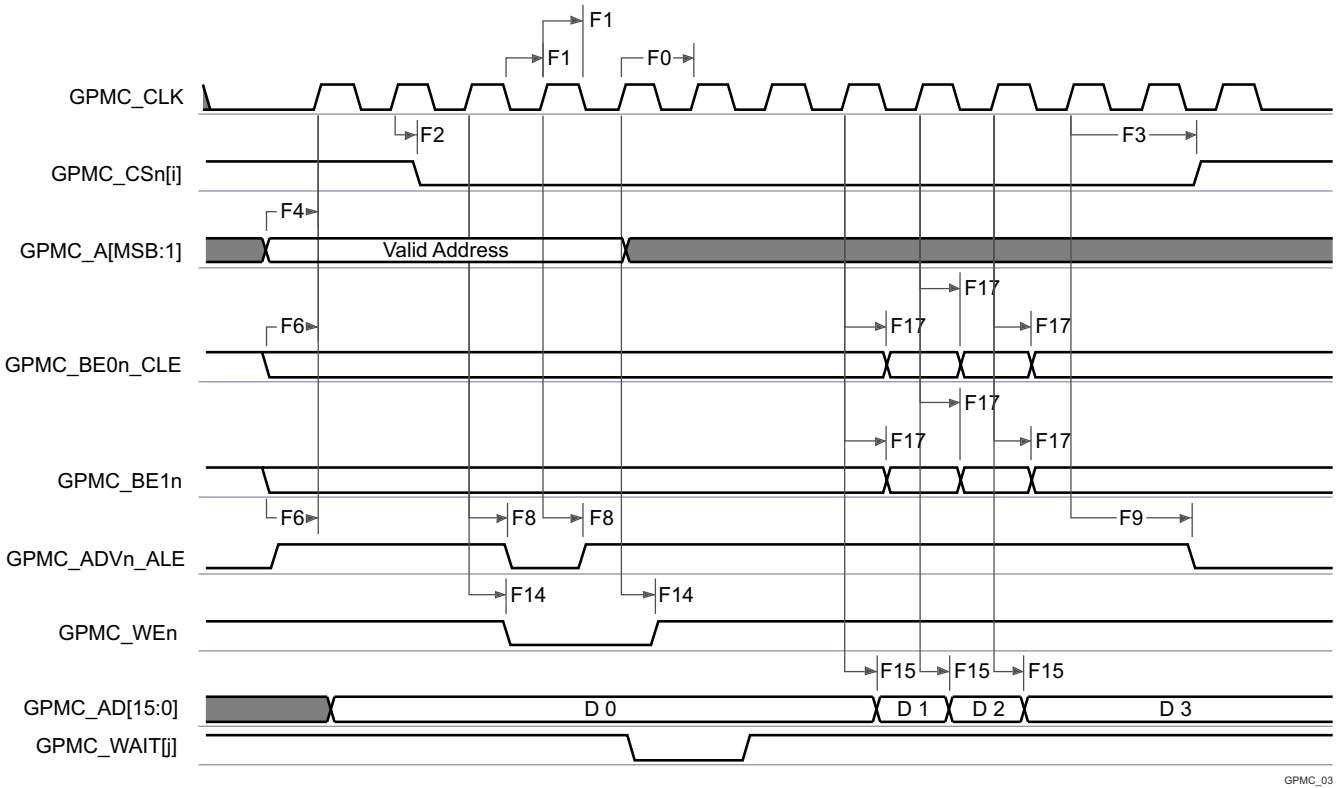
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-46. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

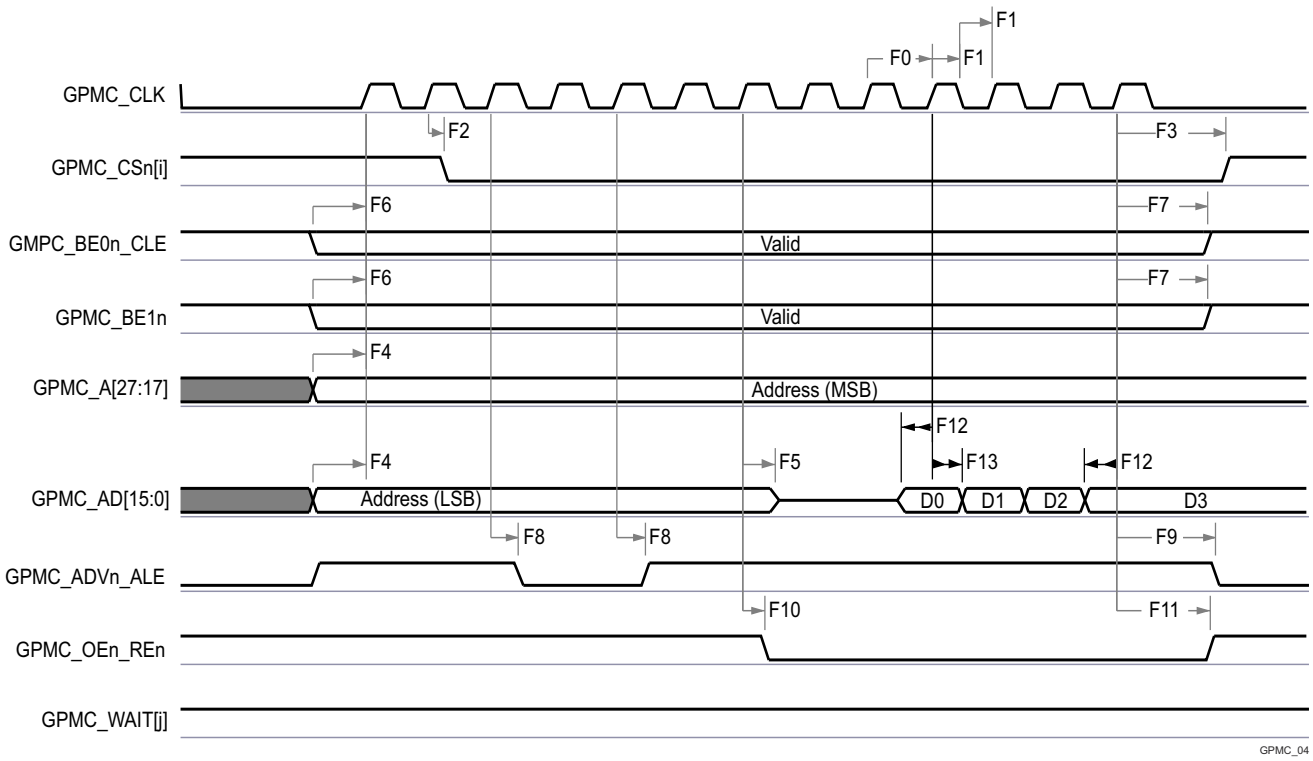
図 7-47. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

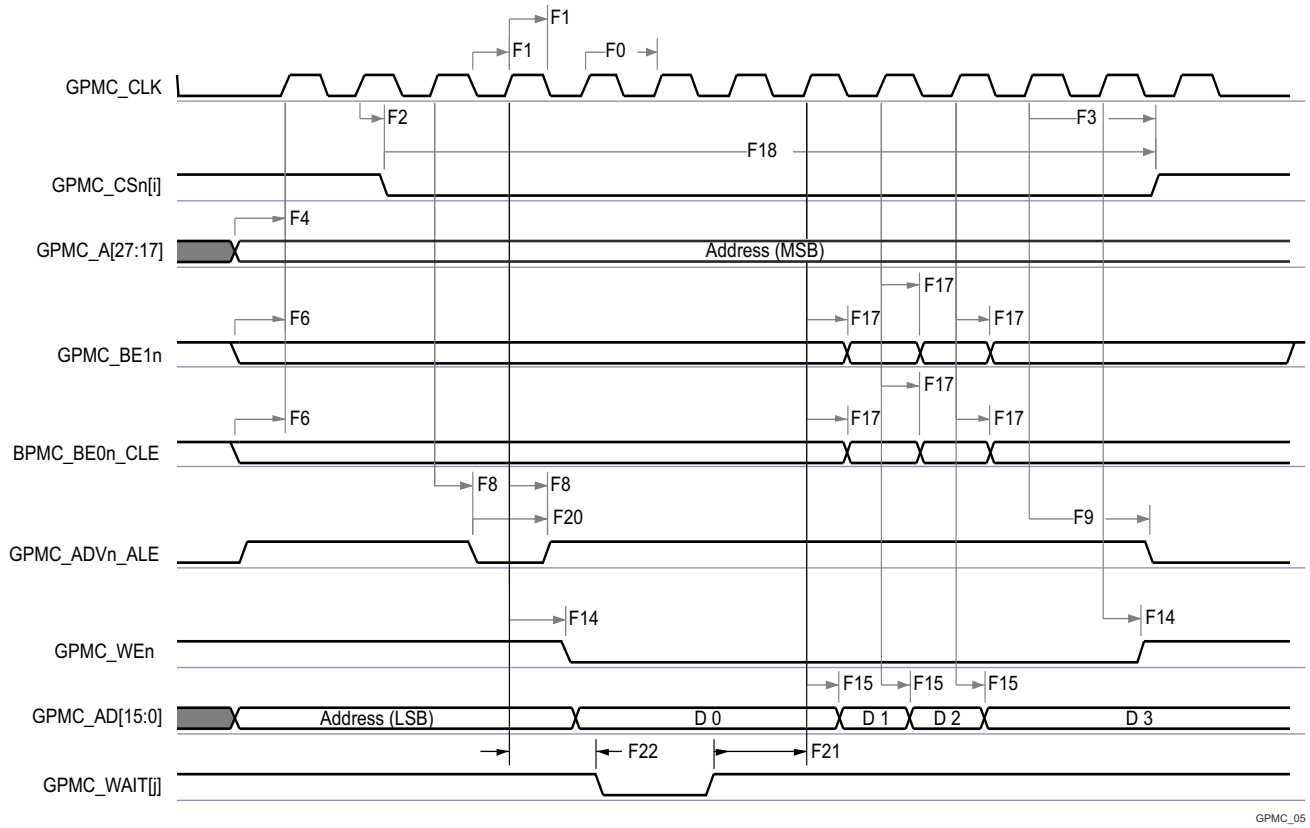
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-48. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-49. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-50. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

7.11.5.11.2 GPMC and NOR Flash — Asynchronous Mode

表 7-65 and 表 7-66 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

表 7-65. GPMC and NOR Flash Timing Requirements – Asynchronous Mode

see 図 7-51, 図 7-52, 図 7-53, and 図 7-55

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5[1]	$t_{acc(d)}$	Data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H[4]	ns
FA20[2]	$t_{acc1-pgmode(d)}$	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		P[3]	ns
FA21[1]	$t_{acc2-pgmode(d)}$	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H[4]	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[5]
(4) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[5]
(5) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

表 7-66. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

see 図 7-51, 図 7-52, 図 7-53, 図 7-54, 図 7-55, and 図 7-56

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN	MAX	UNIT
				133 MHz		
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read		N [12]	ns
			Write		N [12]	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i][13] low	Read		A [1]	ns
			Write		A [1]	
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B - 2 [2]	B + 2[2]	ns
			Write	B - 2[2]	B + 2[2]	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2[3]	C + 2[3]	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K - 2[10]	K + 2[10]	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L - 2[11]	L + 2[11]	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G [7]		ns

表 7-66. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (continued)

see 図 7-51, 図 7-52, 図 7-53, 図 7-54, 図 7-55, and 図 7-56

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN	MAX	UNIT
				133 MHz		
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2[8]	I + 2[8]	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D [4]		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2[5]	E + 2[5]	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2[6]	F + 2[6]	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(7) G = Cycle2CycleDelay × GPMC_FCLK[14]
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK[14]
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

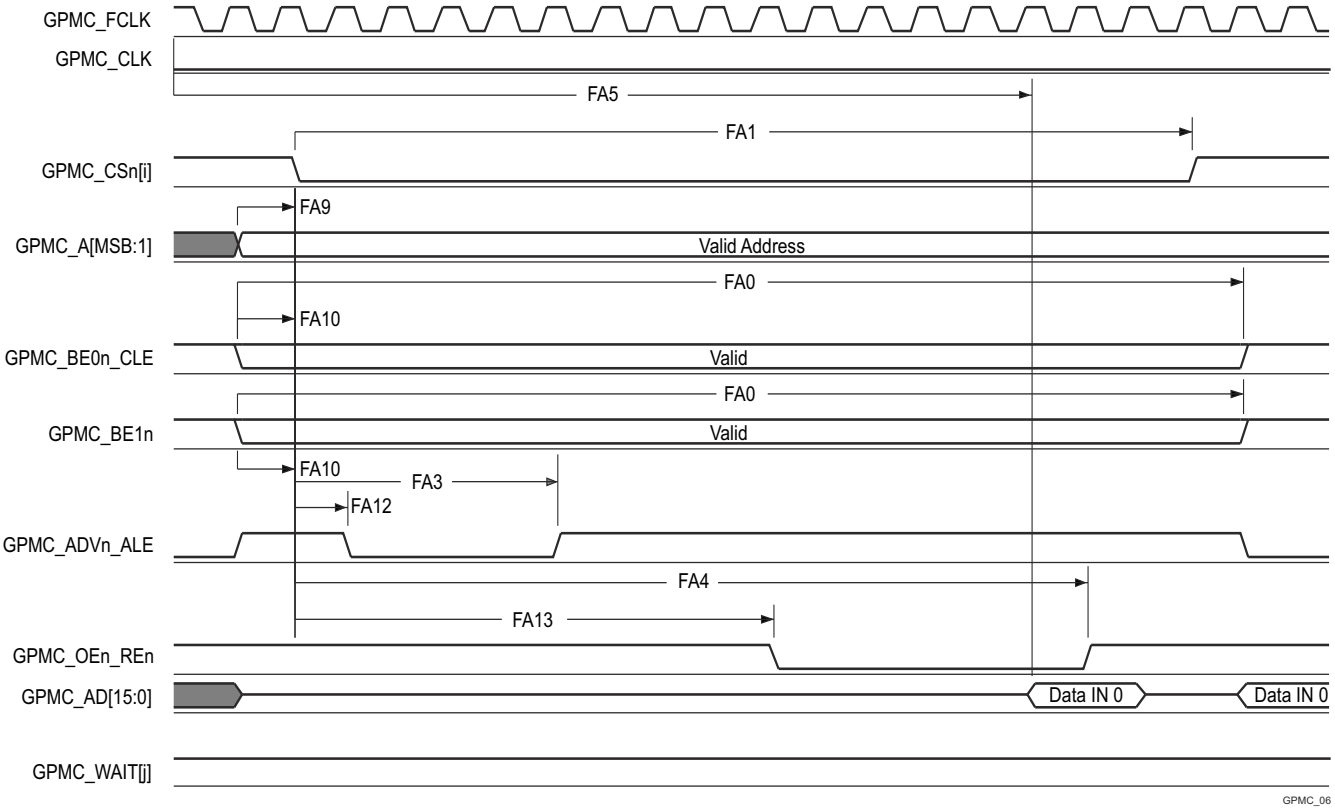
For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

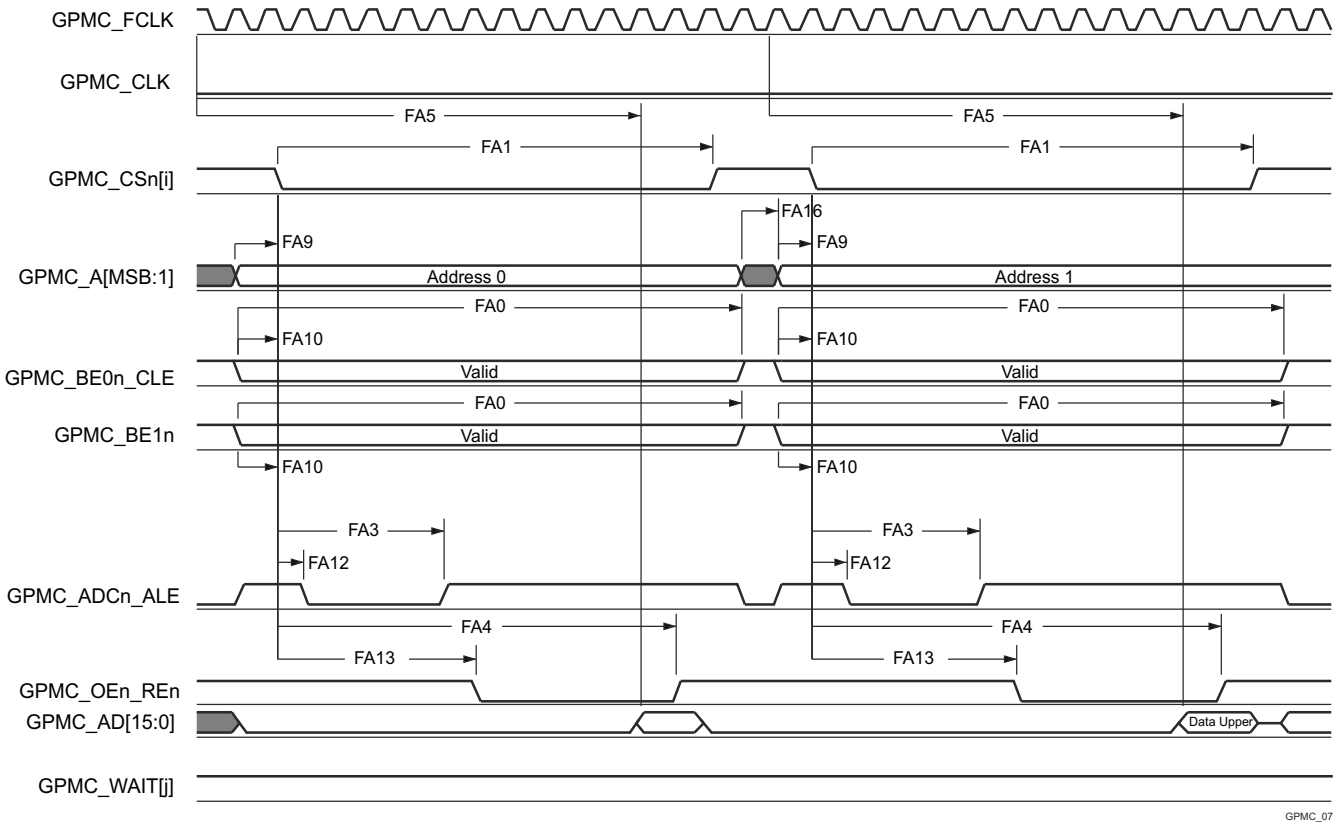
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME,

OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], jis equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 7-51. GPMC and NOR Flash — Asynchronous Read — Single Word

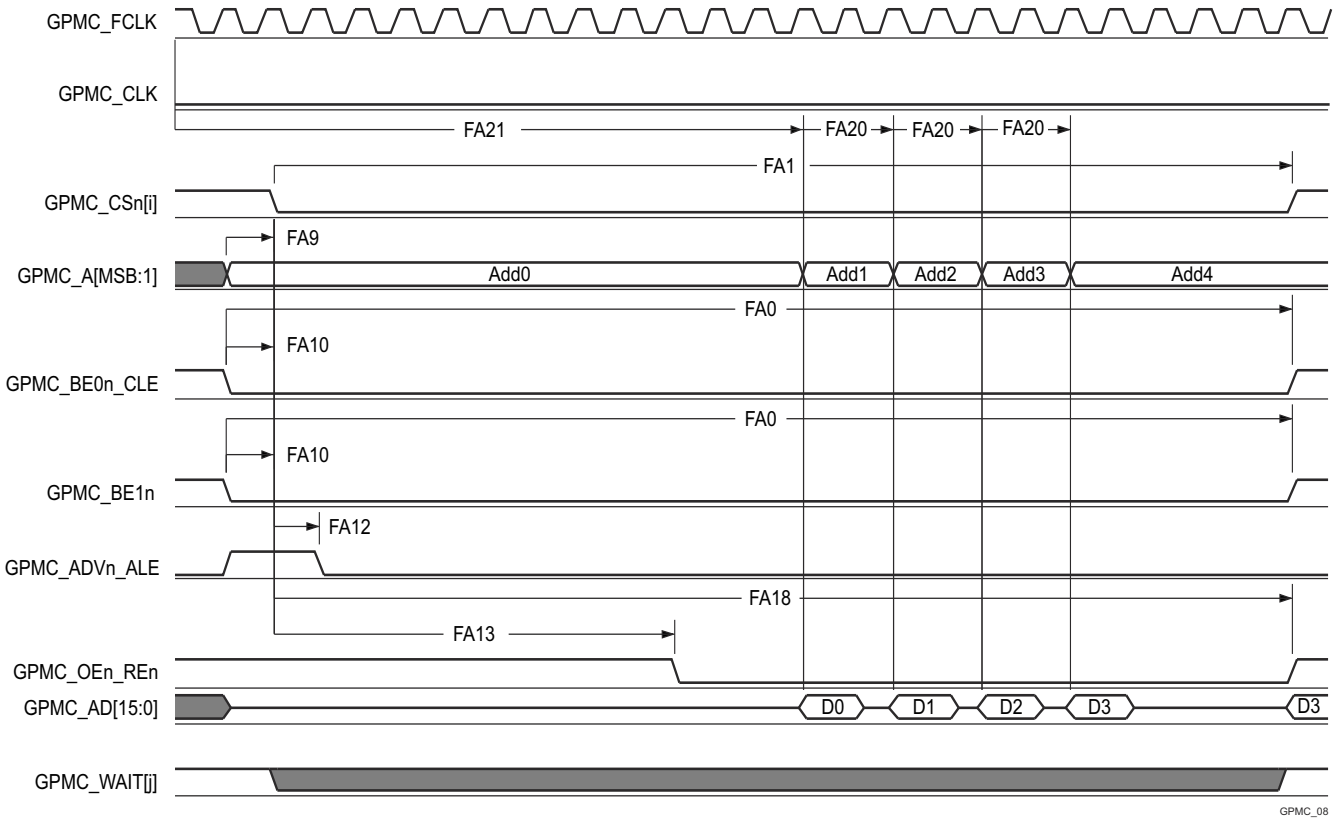


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 7-52. GPMC and NOR Flash — Asynchronous Read — 32–Bit



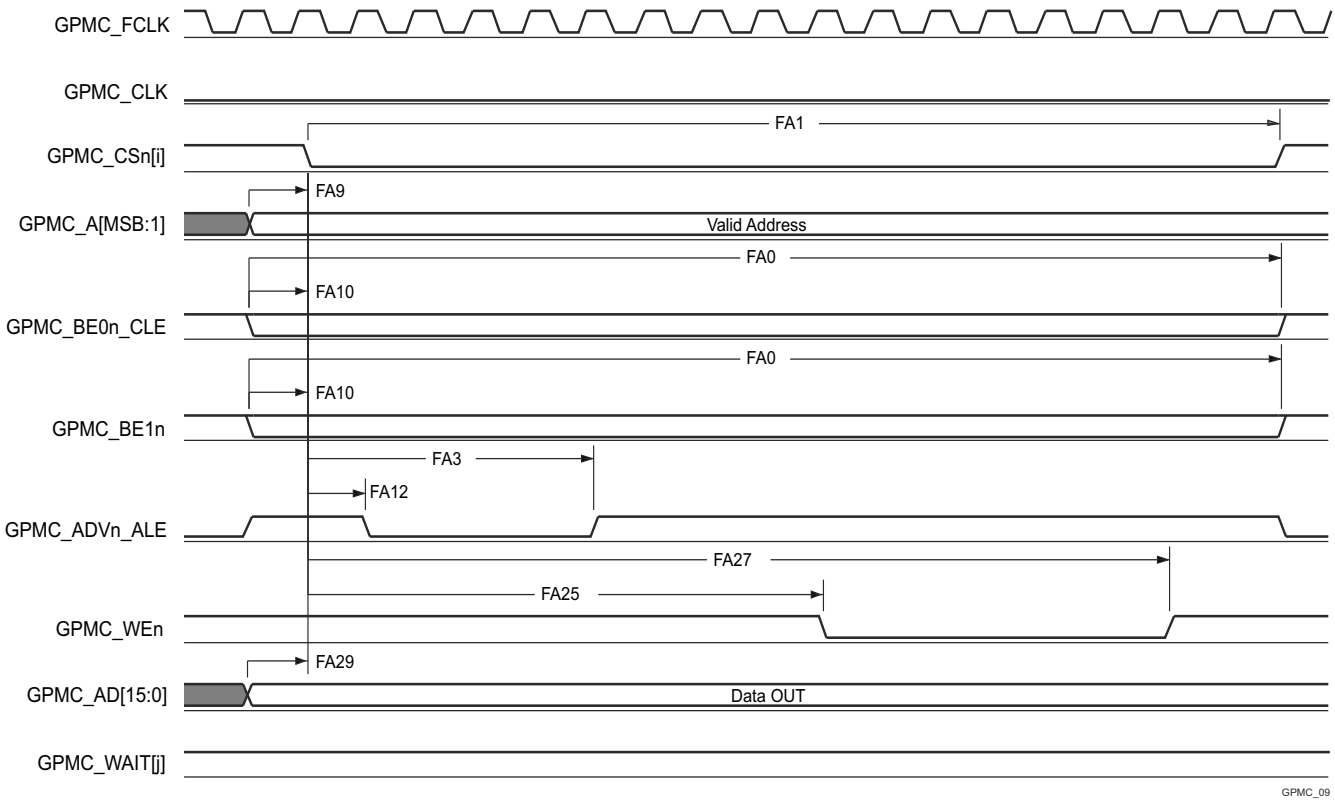
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

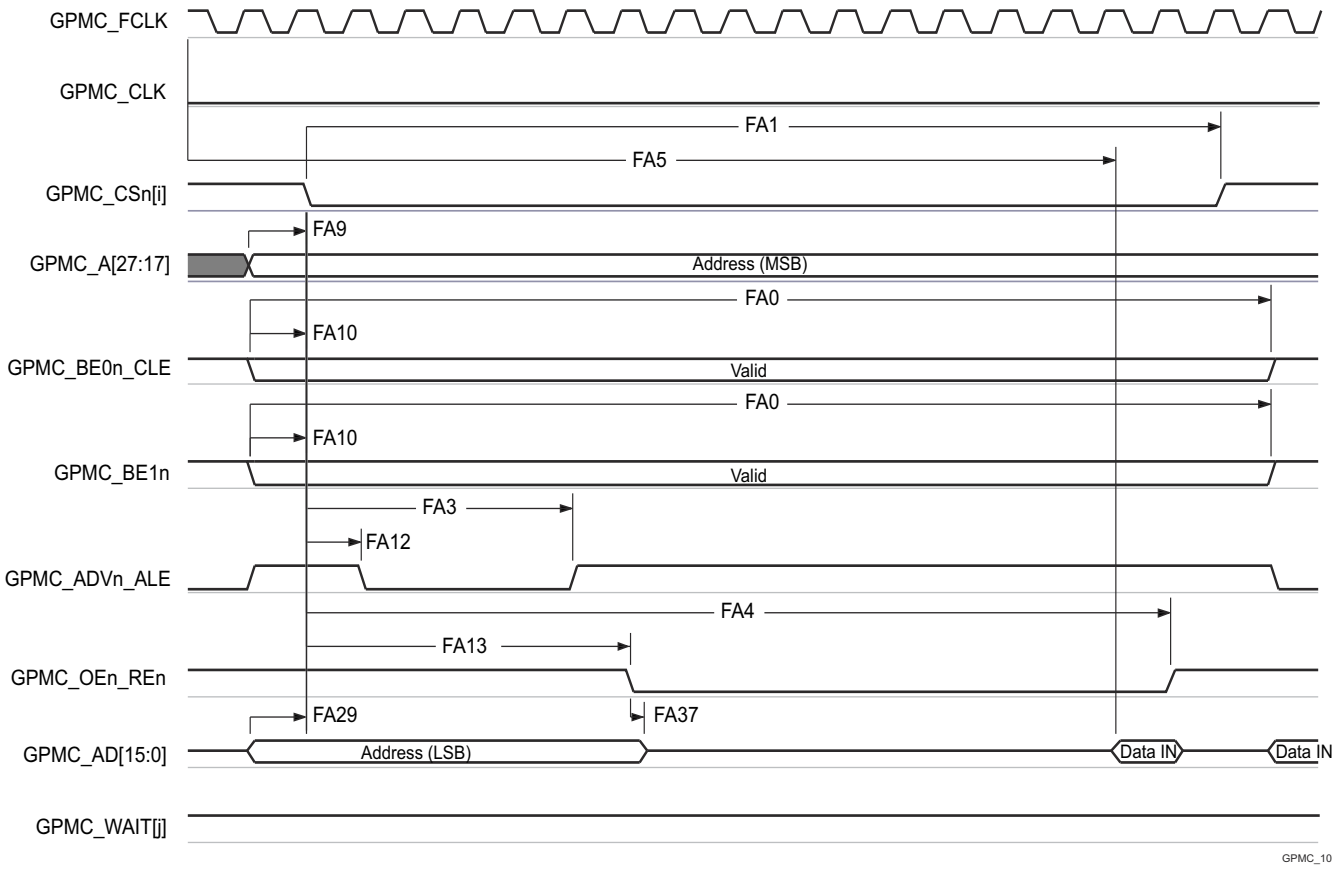
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 7-53. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



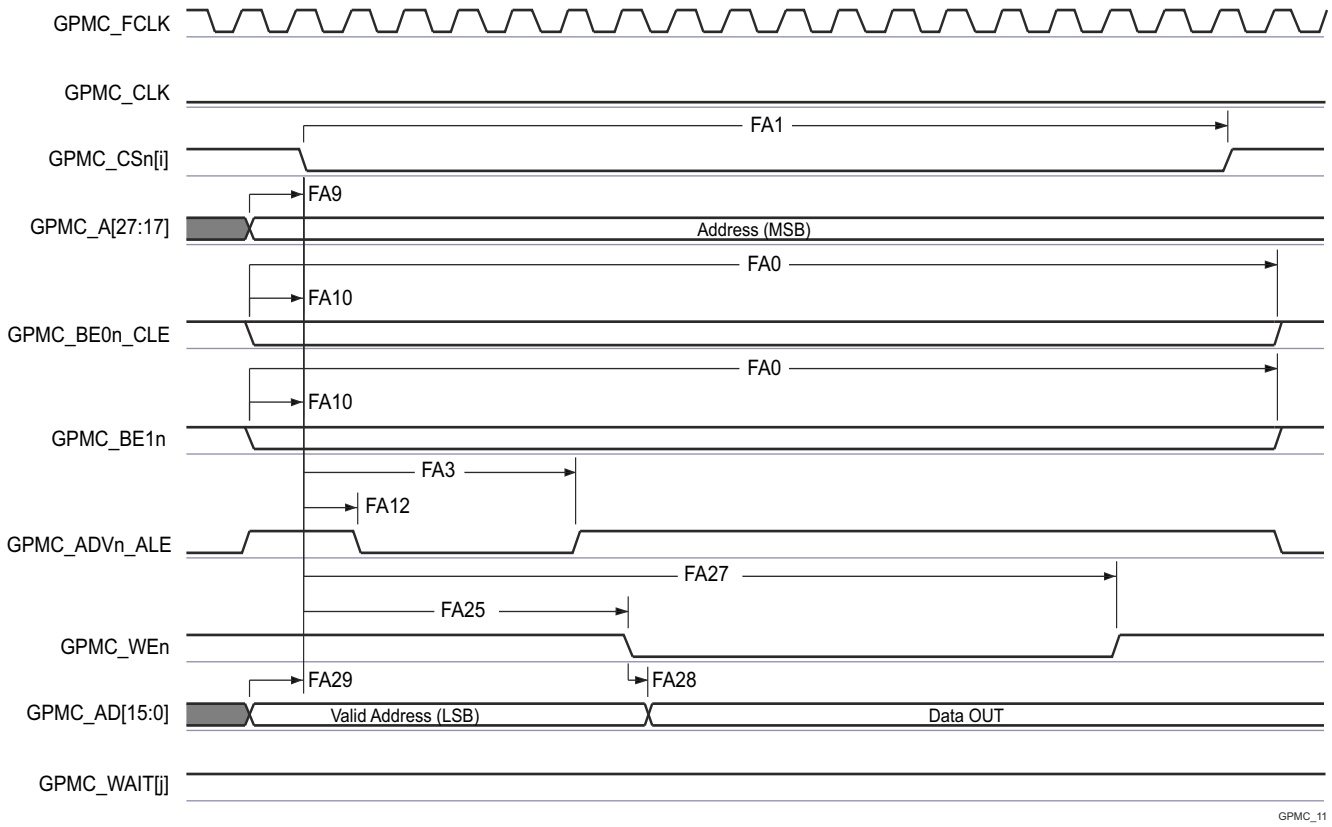
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-54. GPMC and NOR Flash — Asynchronous Write — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 7-55. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-56. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

7.11.5.11.3 GPMC and NAND Flash — Asynchronous Mode

表 7-67 and 表 7-68 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

表 7-67. GPMC and NAND Flash Timing Requirements – Asynchronous Mode

see 図 7-59

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN MAX 133 MHz	UNIT
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 7-68. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

see 図 7-57, 図 7-58, 図 7-59 and 図 7-60

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2	B + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2	D + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2	E + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G - 2	G + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns

表 7-68. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (continued)

see 図 7-57, 図 7-58, 図 7-59 and 図 7-60

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2	I + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	M - 2	M + 2	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(2) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

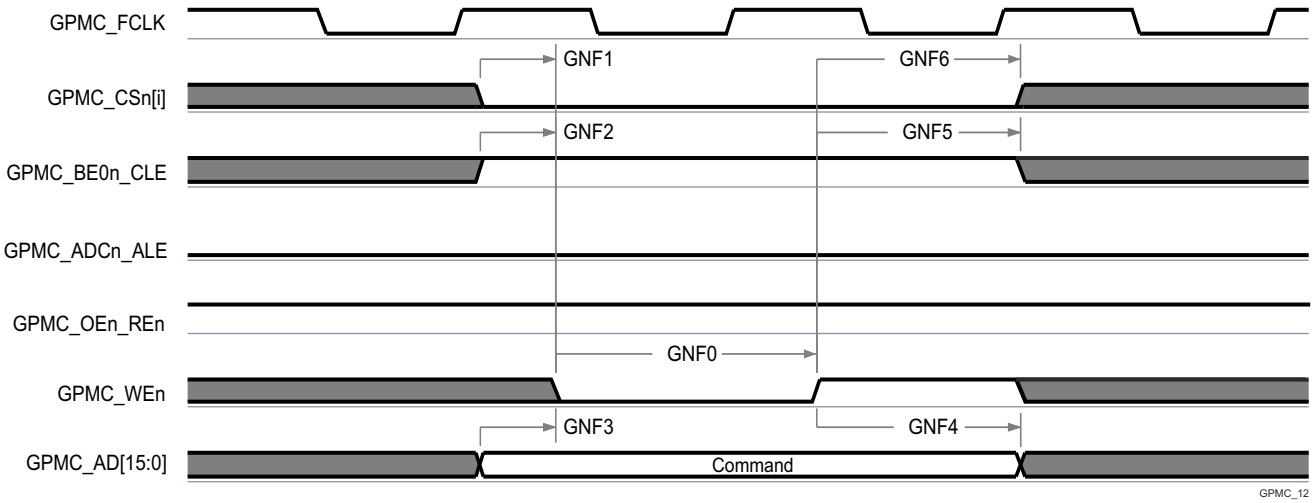
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

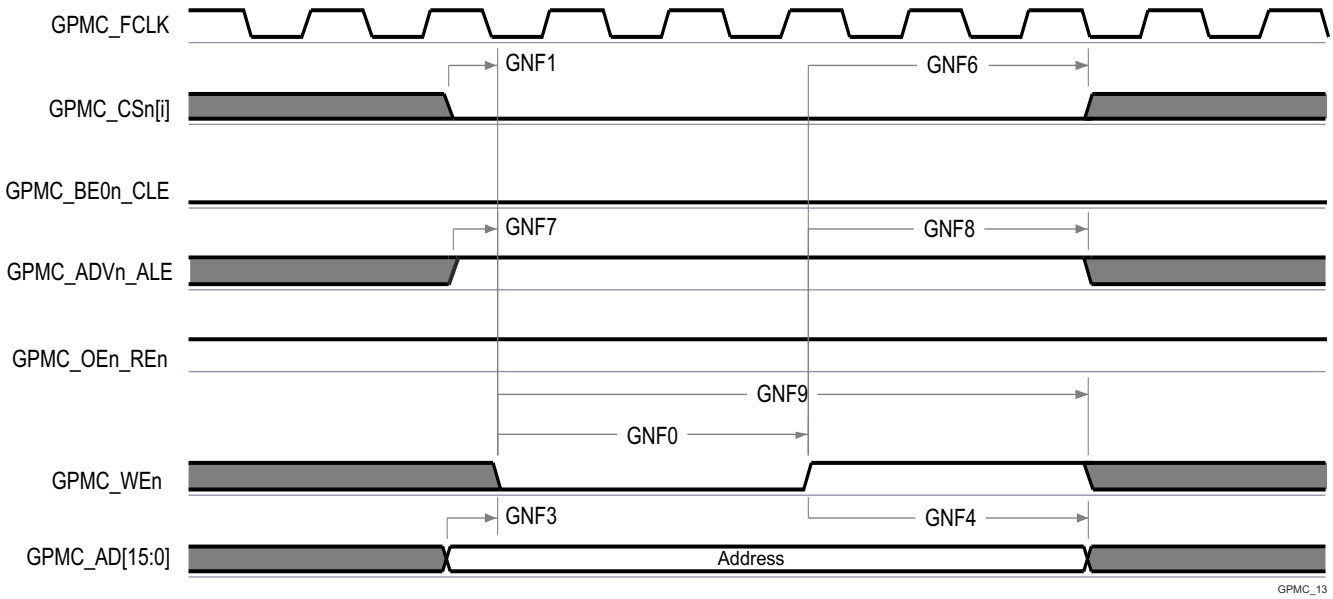
For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



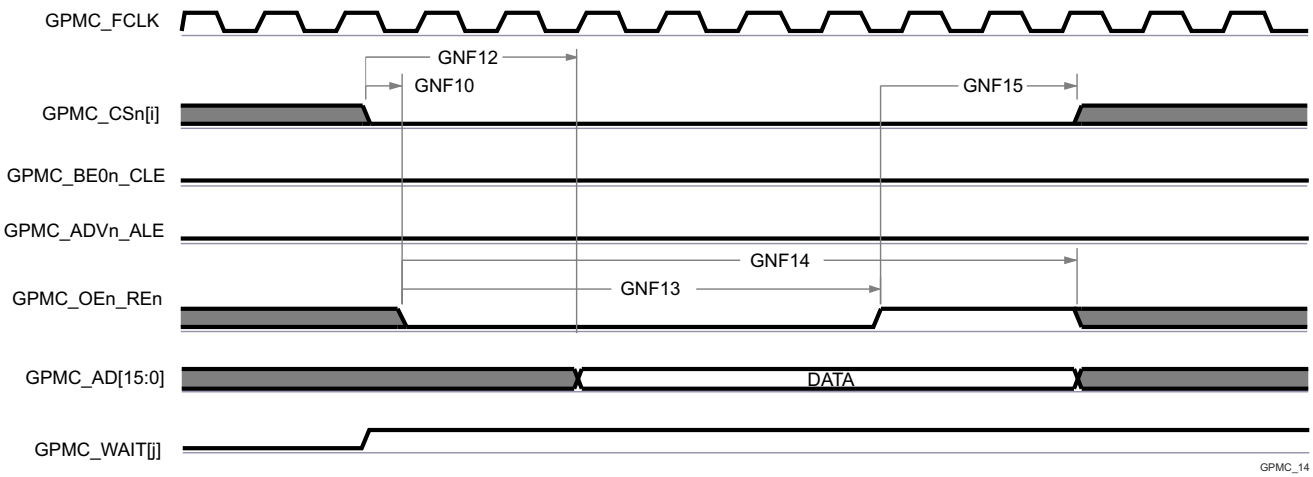
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 7-57. GPMC and NAND Flash — Command Latch Cycle



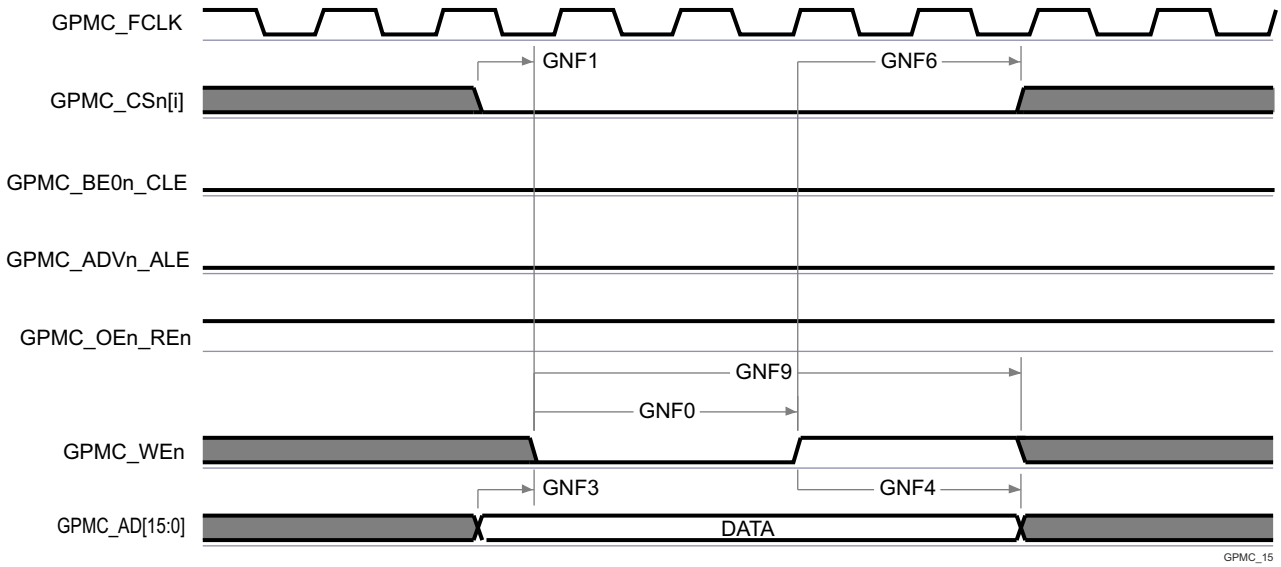
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 7-58. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

図 7-59. GPMC and NAND Flash — Data Read Cycle



A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 7-60. GPMC and NAND Flash — Data Write Cycle

7.11.5.12 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^2C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C0, I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- MCU_I2C0 and WKUP_I2C0
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Hs-mode (up to 3.4 Mbits/s)
      - 1.8 V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8 V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

注

I2C3 has one or more signals which can be multiplexed to more than one pin. Timing is only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.11.5.13 MCAN

表 7-69 and 表 7-70 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

注

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

表 7-69. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

表 7-70. MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MCAN1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX		10	ns
MCAN2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX to receive shift register		10	ns

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

7.11.5.14 MCASP

注

McASP has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

表 7-71, 表 7-72, 図 7-61, 表 7-73, and 図 7-62 present timing conditions, requirements, and switching characteristics for MCASP.

表 7-71. MCASP Timing Conditions

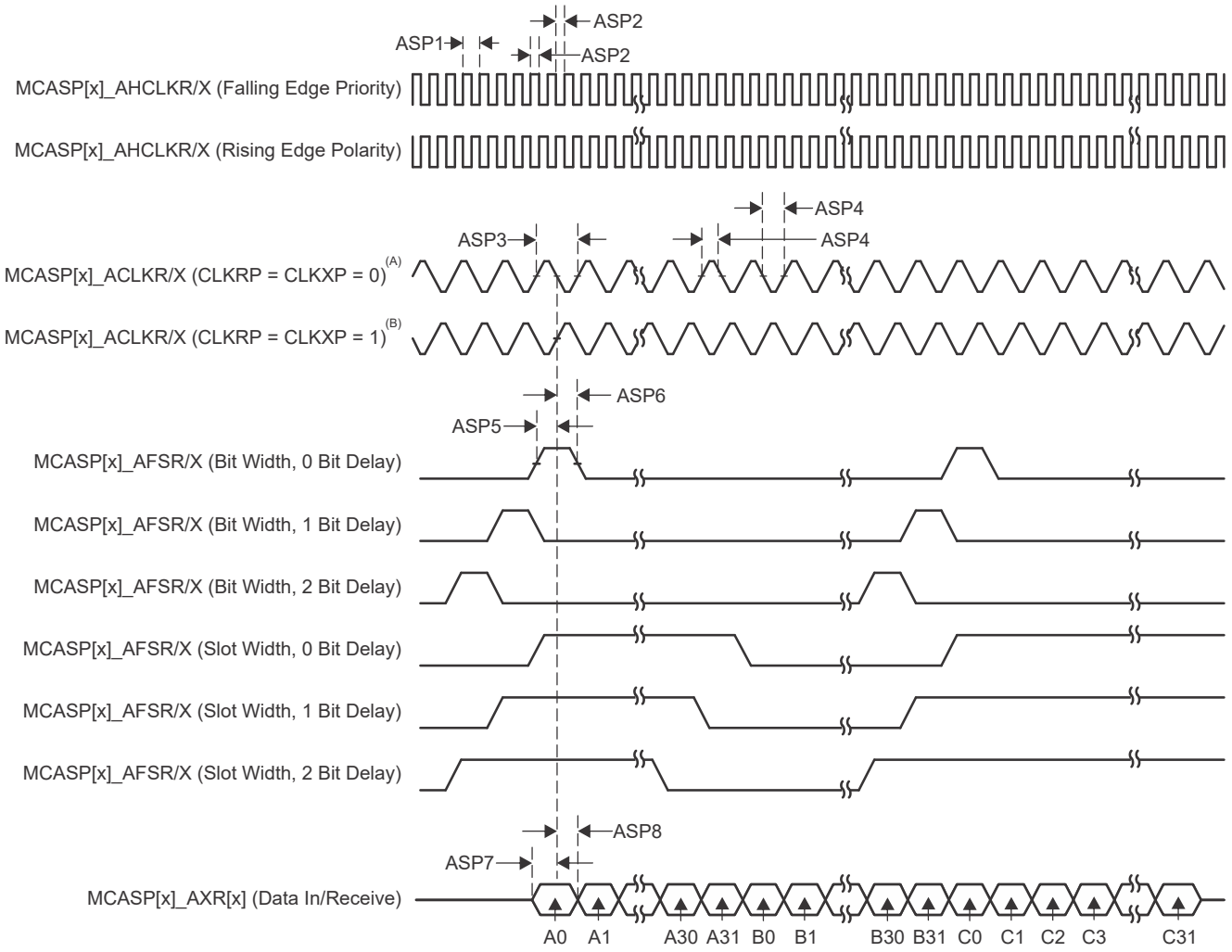
PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 7-72. MCASP Timing Requirements

see 図 7-61

NO.			MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2



A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

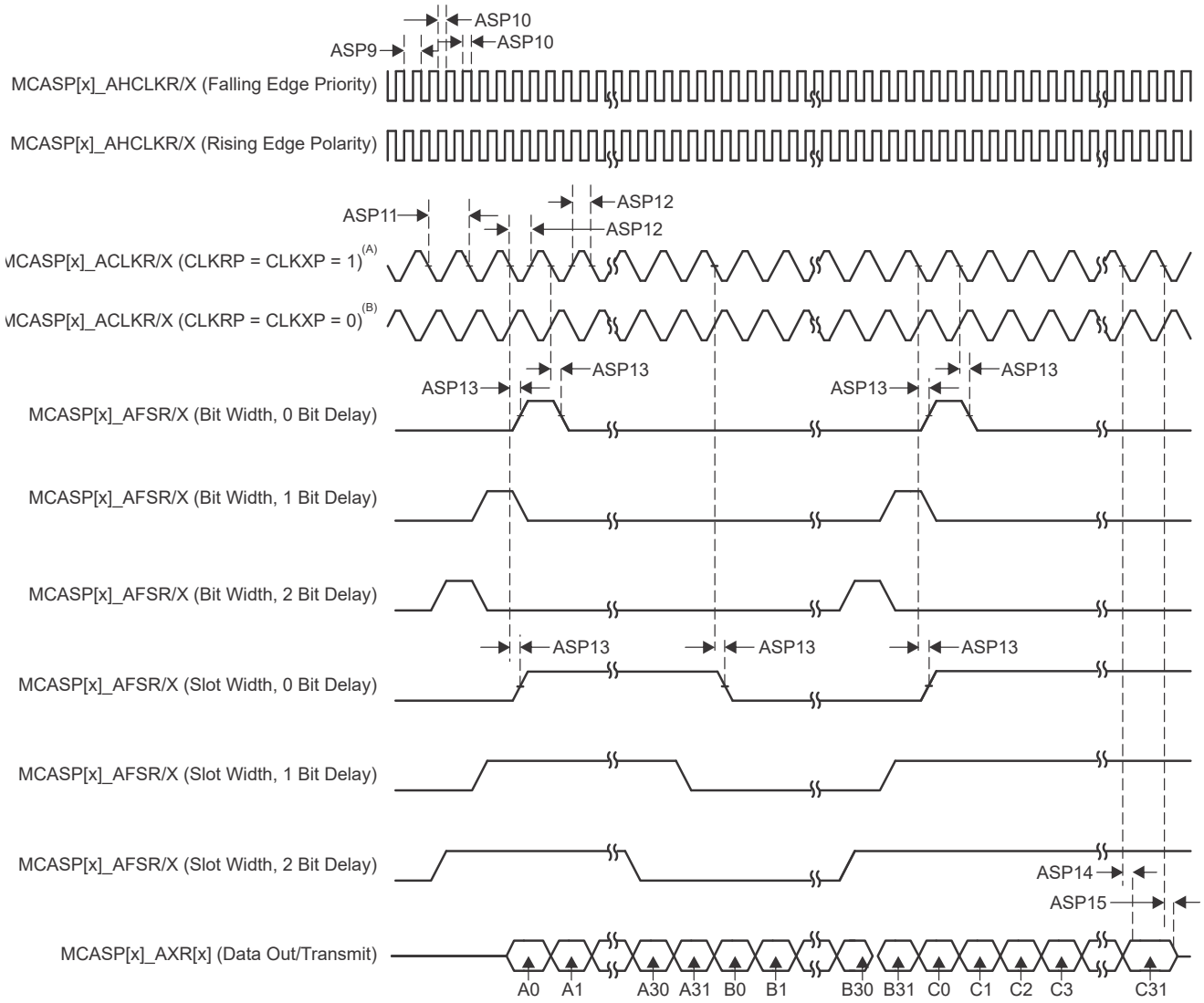
図 7-61. MCASP Timing Requirements

表 7-73. MCASP Switching Characteristics

see 図 7-62

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X(4) transmit edge to MCASP[x]_AFSR/X(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output high impedance	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-14.9	14	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2



A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

図 7-62. MCASP Switching Characteristics

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

7.11.5.15 MCSPI

注

McSPI has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-74 presents timing conditions for MCSPI.

表 7-74. MCSPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	6	12	pF

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

7.11.5.15.1 MCSPI — Controller Mode

表 7-75, 図 7-63, 表 7-76, and 図 7-64 present timing requirements and switching characteristics for SPI – Controller Mode.

表 7-75. MCSPI Timing Requirements – Controller Mode

see 図 7-63

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	$t_{su(POCI-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	$t_{h(SPICLK-POCI)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns

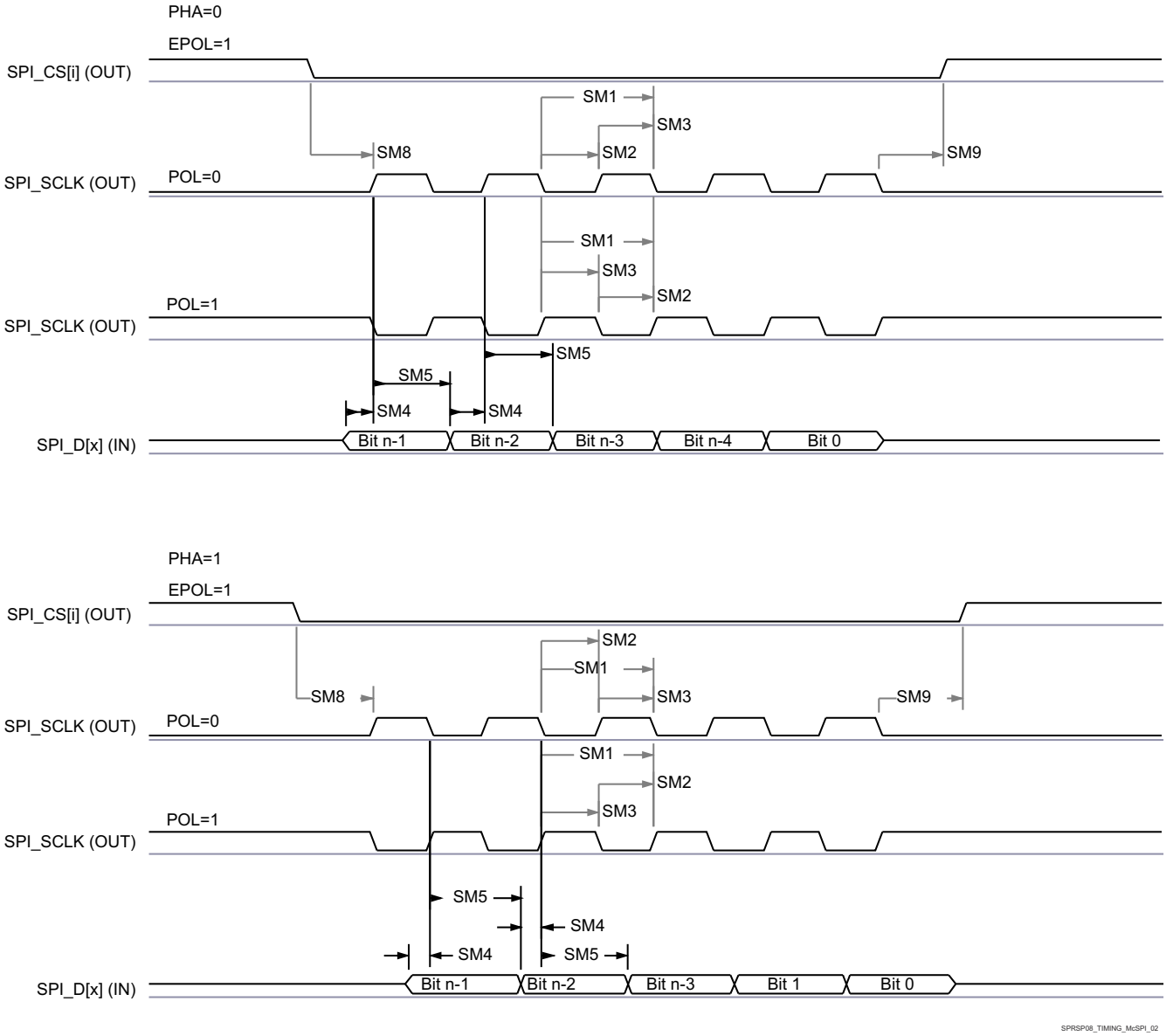


図 7-63. SPI Controller Mode Receive Timing

表 7-76. MCSPI Switching Characteristics - Controller Mode

see 図 7-64

NO.	PARAMETER			MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK		20		ns
SM2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low		0.5P - 1 (1)		ns
SM3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high		0.5P - 1 (1)		ns
SM6	$t_{d(SPICLK-PICO)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]		-3	2.5	ns
SM7	$t_{d(CS-PICO)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		5		ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, SPIn_CSi active to SPIn_CLK first edge	PHA = 0	B - 4 (3)		ns
			PHA = 1	A - 4 (2)		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPIn_CLK last edge to SPIn_CSi inactive	PHA = 0	A - 4 (2)		ns
			PHA = 1	B - 4 (3)		ns

(1) P = SPI_CLK period in ns.
(2) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(3) B = (TCS + .5) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even >= 2.

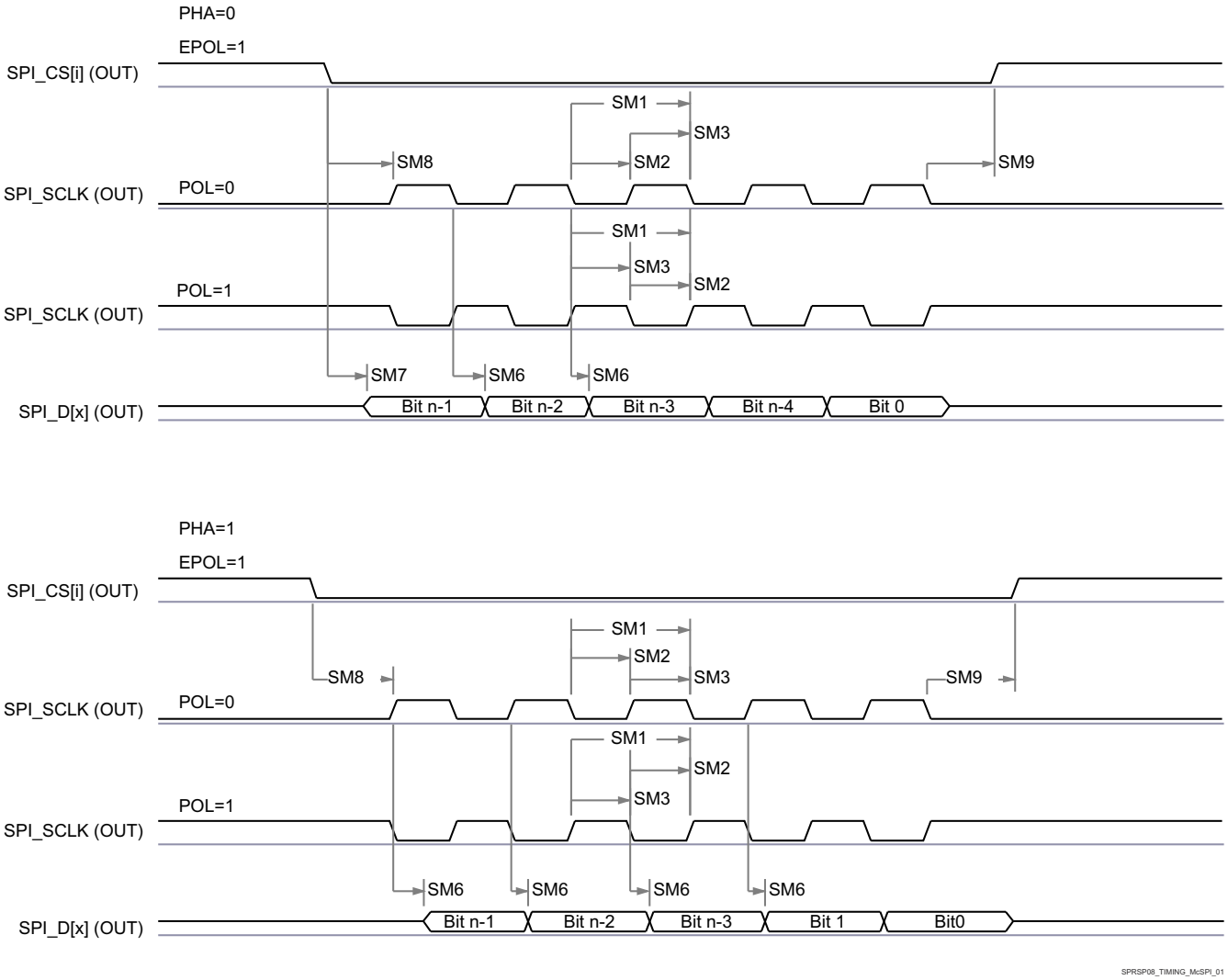


図 7-64. SPI Controller Mode Transmit Timing

7.11.5.15.2 MCSPI — Peripheral Mode

表 7-77, 図 7-65, 表 7-78, and 図 7-66 present timing requirements and switching characteristics for SPI – Peripheral Mode.

表 7-77. MCSPI Timing Requirements – Peripheral Mode

see 図 7-65

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK	20		ns
SS2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low	0.45P(1)		ns
SS3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high	0.45P(1)		ns
SS4	$t_{su(PICO-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns
SS5	$t_{h(SPICLK-PICO)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1) P = SPIn_CLK period in ns.

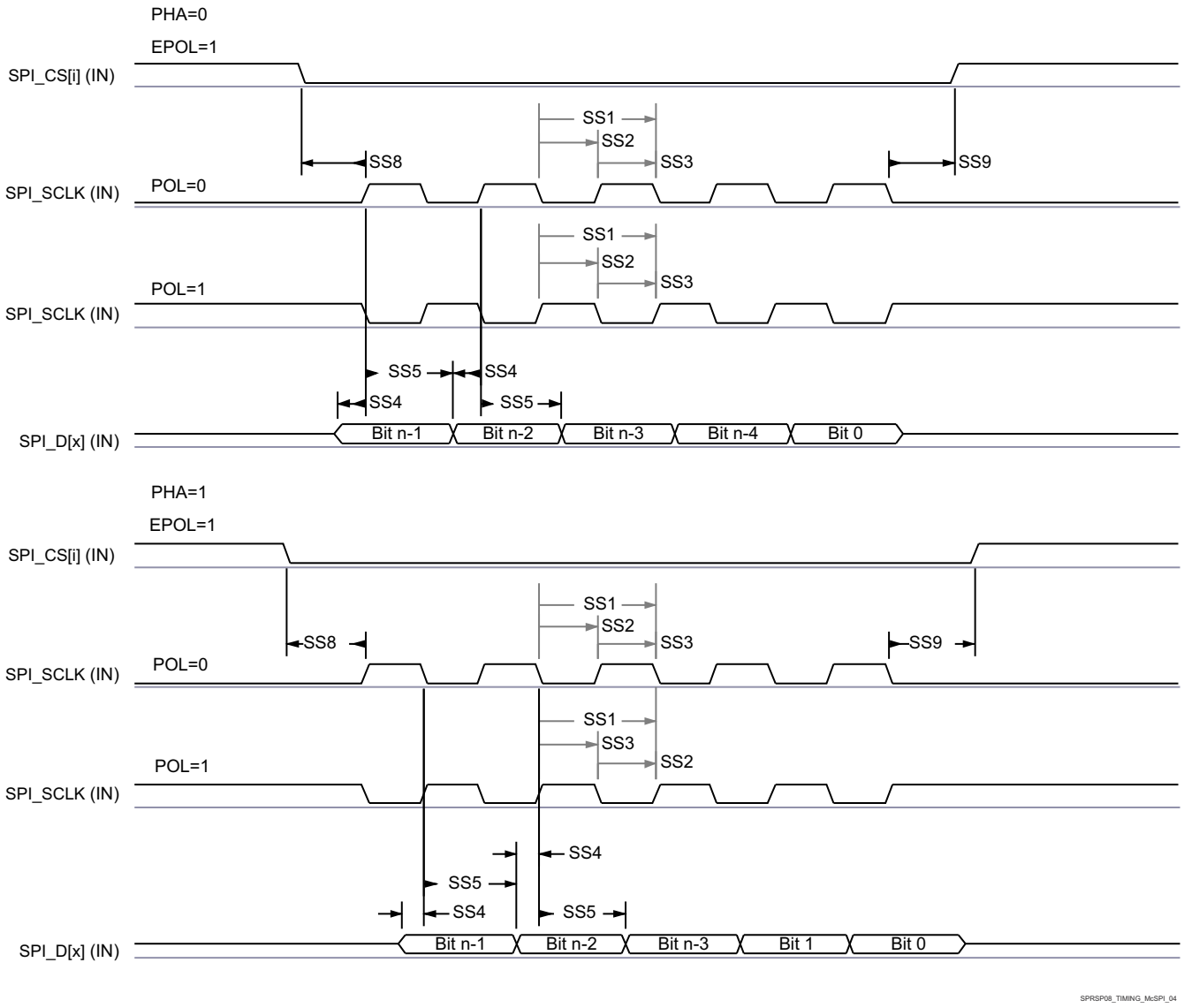


図 7-65. SPI Peripheral Mode Receive Timing

表 7-78. MCSPI Switching Characteristics – Peripheral Mode

see 図 7-66

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-POCI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	17.12	ns
SS7	$t_{sk(CS-POCI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]	20.95		ns

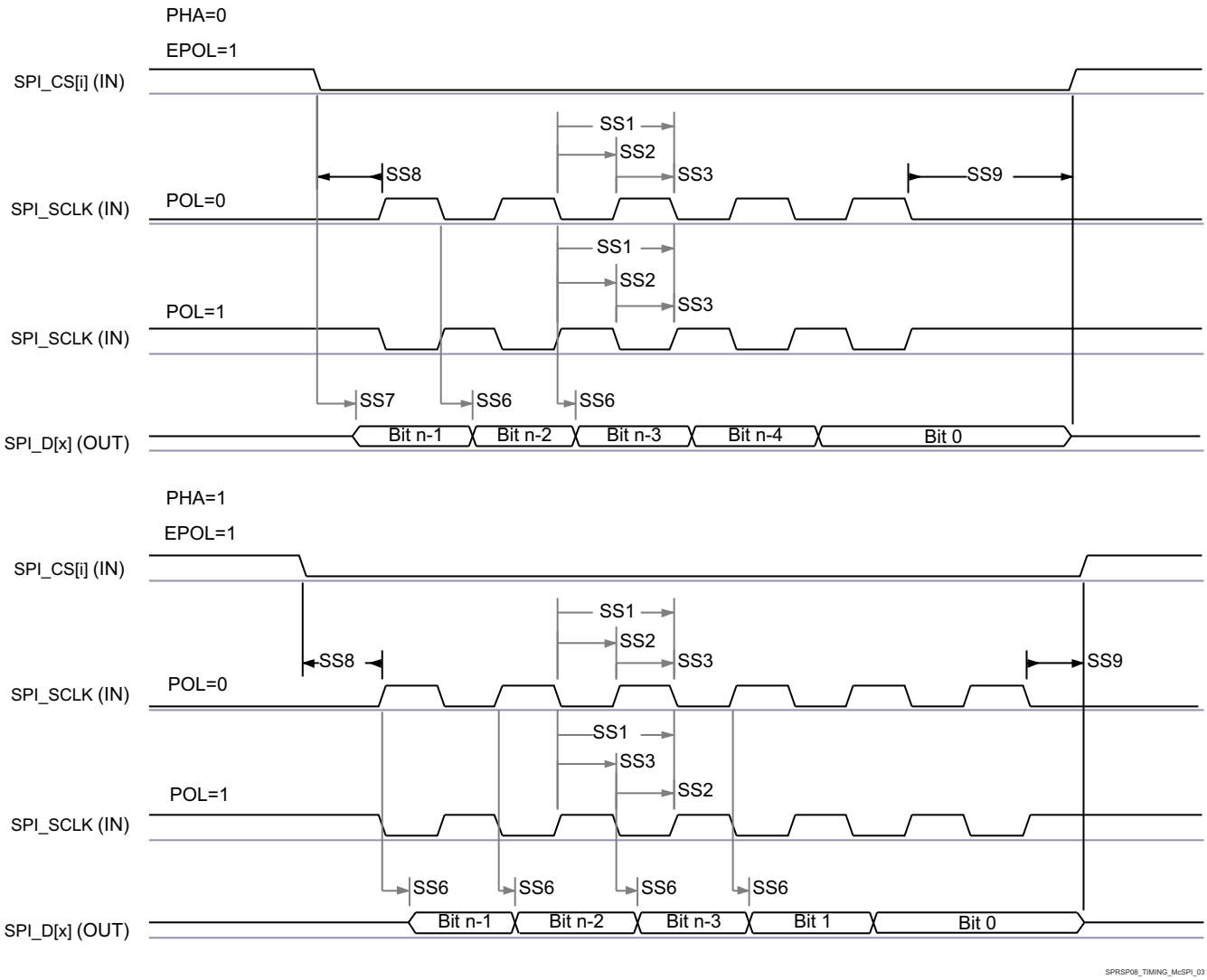


図 7-66. SPI Peripheral Mode Transmit Timing

7.11.5.16 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 subsections within *Signal Descriptions* and *Detailed Description* sections.

注

Some operating modes require software configuration of the MMC DLL delay settings, as shown in 表 7-79 and 表 7-97.

The modes which show a value of "Tuning" in the ITAPDLYSEL column of 表 7-79 and 表 7-97 require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSD Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

7.11.5.16.1 MMC0 - eMMC/SD/SDIO Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy SDR
- High Speed SDR
- HS200

MMC0 interface is also compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default Speed
- High Speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I DDR50
- UHS–I SDR104

表 7-79 presents the required DLL software configuration settings for MMC0 timing modes.

表 7-79. MMC0 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD0_SS_PHY_CTRL_4_REG				MMCSD0_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Legacy SDR	8-bit PHY operating 1.8 V, 25 MHz	0x1	0x0	0x0	NA(1)	0x7
	8-bit PHY operating 3.3 V, 25 MHz	0x1	0x0	0x0	NA(1)	0x7
High Speed SDR	8-bit PHY operating 1.8 V, 50 MHz	0x1	0x0	0x0	NA(1)	0x7
	8-bit PHY operating 3.3 V, 50 MHz	0x1	0x0	0x0	NA(1)	0x7
HS200	8-bit PHY operating 1.8 V, 200 MHz	0x1	0x6	0x1	Tuning(2)	0x7
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x1	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x1	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning(2)	0x7
UHS-I DDR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0x9	0x1	Tuning(2)	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x6	0x1	Tuning(2)	0x7

(1) NA means Not Applicable
(2) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

表 7-80 presents timing conditions for MMC0.

表 7-80. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR @ 3.3 V High Speed SDR@ 3.3V Default Speed High Speed	0.69	2.06	V/ns
		Legacy SDR @ 1.8 V UHS-I SDR12	0.14	1.44	V/ns
		High Speed SDR @ 1.8 V UHS-I SDR25	0.3	1.34	V/ns
		UHS-I DDR50	1	2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	HS200 UHS-I SDR104	1	10	pF
		All other modes	1	12	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	Legacy SDR High Speed SDR HS200	126	756	ps
		Default Speed High Speed UHS-I SDR12 UHS-I SDR25 UHS-I SDR50 UHS-I SDR104	126	1386	ps
		UHS-I DDR50	239	1134	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	High Speed SDR HS200 High Speed UHS-I SDR104		8	ps
		UHS-I DDR50		20	ps
		All other modes		100	ps

7.11.5.16.1.1 Legacy SDR Mode

表 7-81, 図 7-67, 表 7-82, and 図 7-68 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

表 7-81. MMC0 Timing Requirements – Legacy SDR Mode

see 図 7-67

NO.			IO Operating Voltage	MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.8 V	4.2		ns
			3.3 V	2.15		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.8 V	0.87		ns
			3.3 V	1.67		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.8 V	4.2		ns
			3.3 V	2.15		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	1.8 V	0.87		ns
			3.3 V	1.67		ns

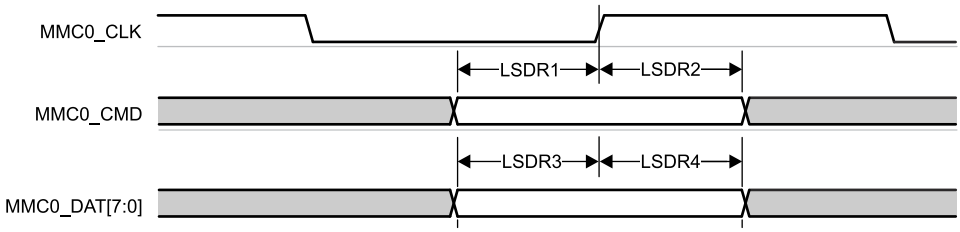


図 7-67. MMC0 – Legacy SDR – Receive Mode

表 7-82. MMC0 Switching Characteristics – Legacy SDR Mode

see 図 7-68

NO.	PARAMETER		IO Operating Voltage	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK			25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK		40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high		18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low		18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	1.8 V	-2.1	2.1	ns
			3.3 V	-1.8	2.2	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	1.8 V	-2.1	2.1	ns
			3.3 V	-1.8	2.2	ns

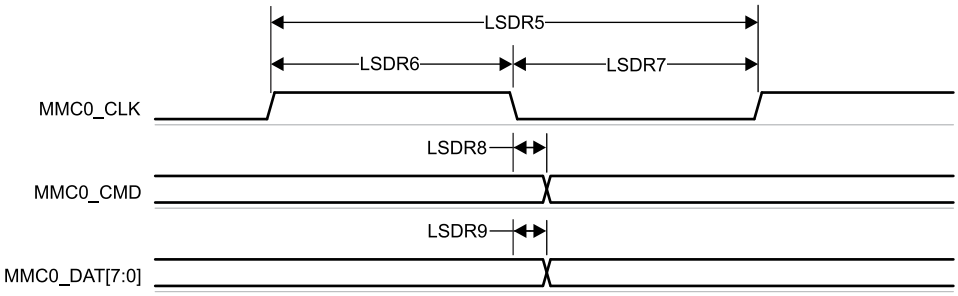


図 7-68. MMC0 – Legacy SDR – Transmit Mode

7.11.5.16.1.2 High Speed SDR Mode

表 7-83, 図 7-69, 表 7-84, and 図 7-70 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

表 7-83. MMC0 Timing Requirements – High Speed SDR Mode

see 図 7-69

NO.			IO Operating Voltage	MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.8 V	2.15		ns
			3.3 V	2.24		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.8 V	1.27		ns
			3.3 V	1.66		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.8 V	2.15		ns
			3.3 V	2.24		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	1.8 V	1.27		ns
			3.3 V	1.66		ns

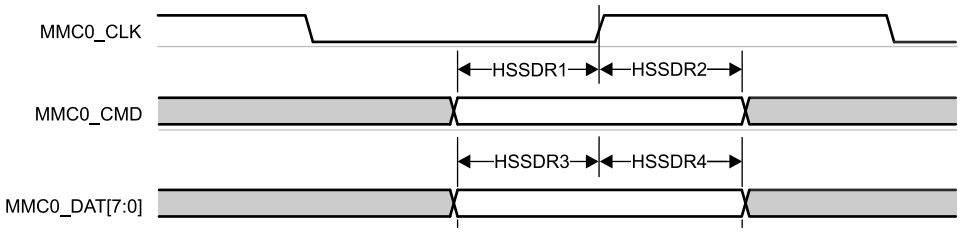


図 7-69. MMC0 – High Speed SDR Mode – Receive Mode

表 7-84. MMC0 Switching Characteristics – High Speed SDR Mode

see 図 7-70

NO.	PARAMETER		IO Operating Voltage	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK			50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK		20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high		9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low		9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	1.8 V	-1.55	3.05	ns
			3.3 V	-1.8	2.2	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	1.8 V	-1.55	3.05	ns
			3.3 V	-1.8	2.2	ns

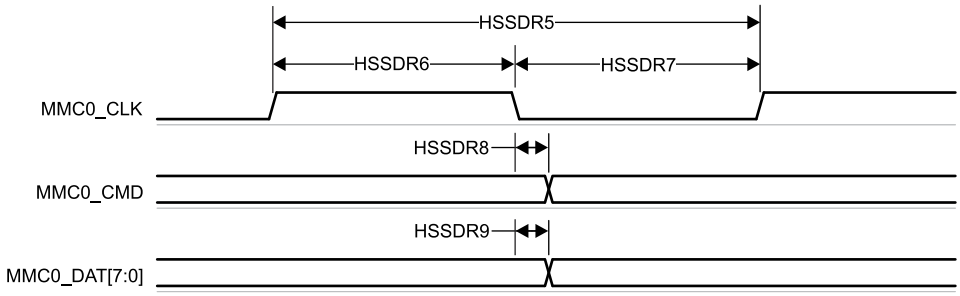


図 7-70. MMC0 – High Speed SDR Mode – Transmit Mode

7.11.5.16.1.3 HS200 Mode

表 7-85 and 図 7-71 present switching characteristics for MMC0 – HS200 Mode.

表 7-85. MMC0 Switching Characteristics – HS200 Mode

see 図 7-71

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.12		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.12		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.07	3.21	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	1.07	3.21	ns

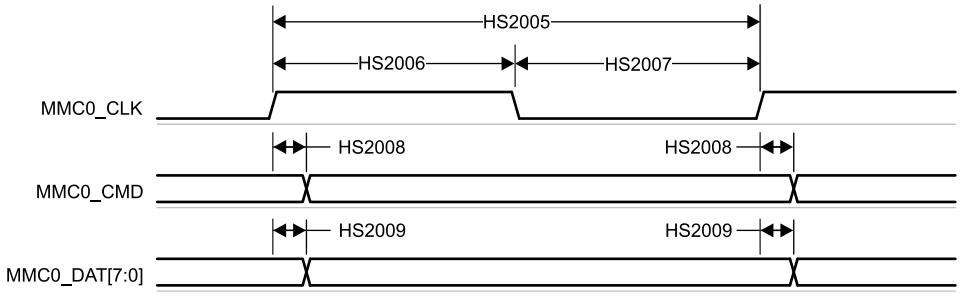


図 7-71. MMC0 – HS200 Mode – Transmit Mode

7.11.5.16.1.4 Default Speed Mode

表 7-86, 図 7-72, 表 7-87, and 図 7-73 present timing requirements and switching characteristics for MMC0 – Default Speed Mode.

表 7-86. Timing Requirements for MMC0 – Default Speed Mode

see 図 7-72

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	1.67		ns

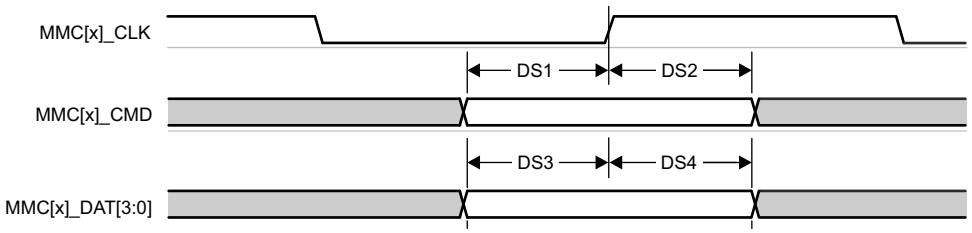


図 7-72. MMC0 – Default Speed – Receive Mode

表 7-87. Switching Characteristics for MMC0 – Default Speed Mode

see 図 7-73

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	- 1.8	2.2	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[3:0] transition	- 1.8	2.2	ns

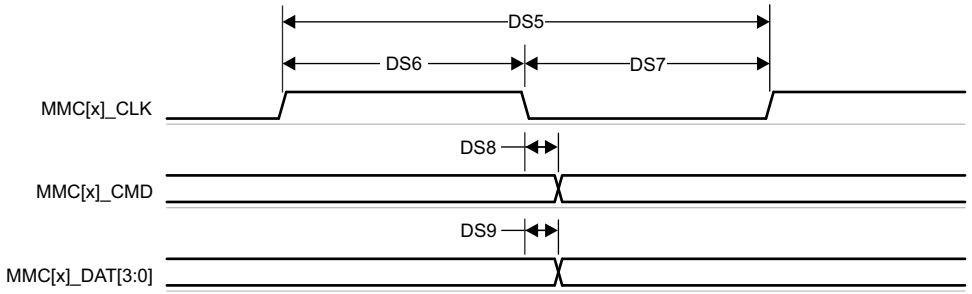


図 7-73. MMC0 – Default Speed – Transmit Mode

7.11.5.16.1.5 High Speed Mode

表 7-88, 図 7-74, 表 7-89, and 図 7-75 present timing requirements and switching characteristics for MMC0 – High Speed Mode.

表 7-88. Timing Requirements for MMC0 – High Speed Mode

see 図 7-74

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.24		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.66		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	2.24		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	1.66		ns

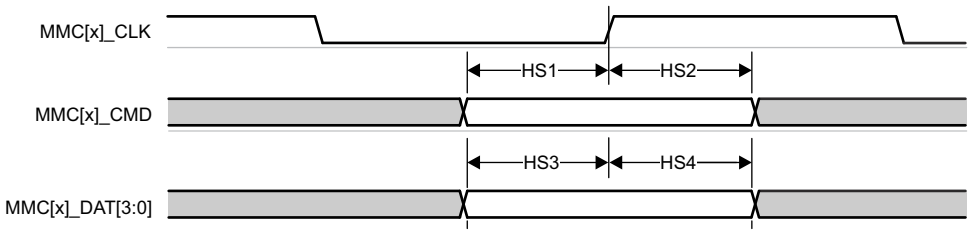


図 7-74. MMC0 – High Speed – Receive Mode

表 7-89. Switching Characteristics for MMC0 – High Speed Mode

see 図 7-75

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMC0_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-1.8	2.2	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[3:0] transition	-1.8	2.2	ns

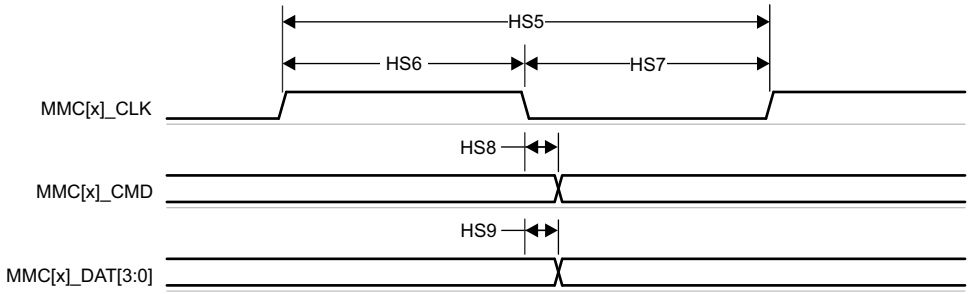


図 7-75. MMC0 – High Speed – Transmit Mode

7.11.5.16.1.6 UHS–I SDR12 Mode

表 7-90, 図 7-76, 表 7-91, and 図 7-77 present timing requirements and switching characteristics for MMC0 – UHS-I SDR12 Mode.

表 7-90. Timing Requirements for MMC0 – UHS-I SDR12 Mode

see 図 7-76

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	4.2		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	0.87		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	4.2		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	0.87		ns

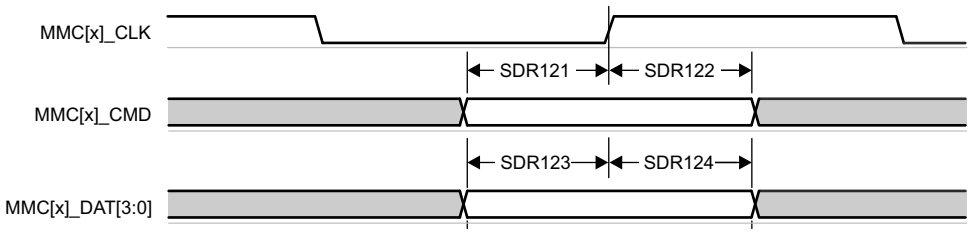


図 7-76. MMC0 – UHS-I SDR12 – Receive Mode

表 7-91. Switching Characteristics for MMC0 – UHS-I SDR12 Mode

see 図 7-77

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.5	8.6	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.5	8.6	ns

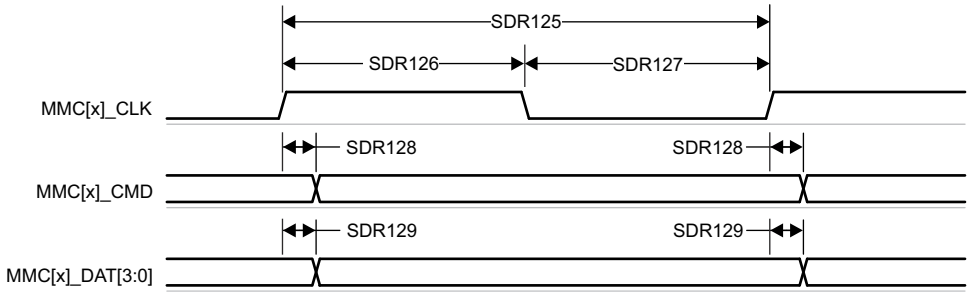


図 7-77. MMC0 – UHS-I SDR12 – Transmit Mode

7.11.5.16.1.7 UHS–I SDR25 Mode

表 7-92, 図 7-78, 表 7-93, and 図 7-79 present timing requirements and switching characteristics for MMC0 – UHS-I SDR25 Mode.

表 7-92. Timing Requirements for MMC0 – UHS-I SDR25 Mode

see 図 7-78

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	1.27		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[3:0] valid before MMC0_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[3:0] valid after MMC0_CLK rising edge	1.27		ns

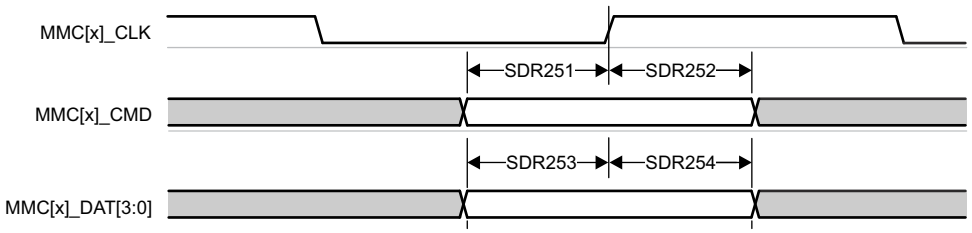


図 7-78. MMC0 – UHS-I SDR25 – Receive Mode

表 7-93. Switching Characteristics for MMC0 – UHS-I SDR25 Mode

see 図 7-79

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	2.4	8.1	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	2.4	8.1	ns

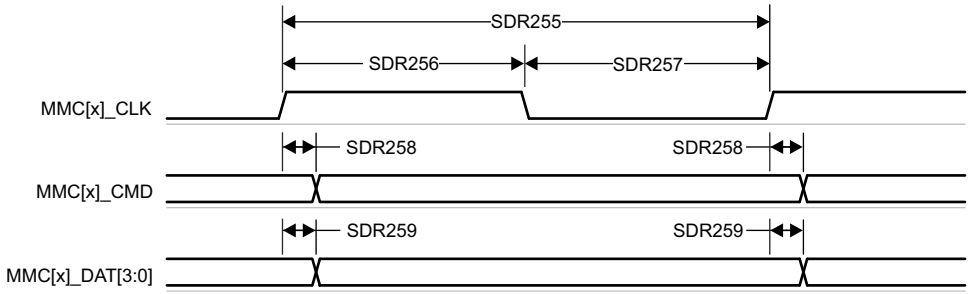


図 7-79. MMC0 – UHS-I SDR25 – Transmit Mode

7.11.5.16.1.8 UHS–I SDR50 Mode

表 7-94 and 図 7-80 presents switching characteristics for MMC0 – UHS-I SDR50 Mode.

表 7-94. Switching Characteristics for MMC0 – UHS-I SDR50 Mode

see 図 7-80

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMC0_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.2	6.35	ns

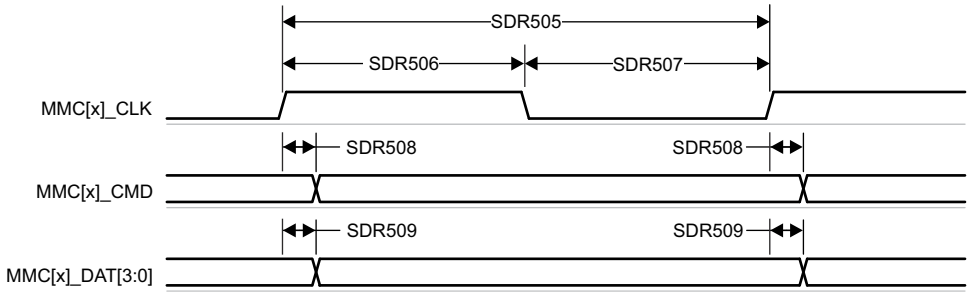


図 7-80. MMC0 – UHS-I SDR50 – Transmit Mode

7.11.5.16.1.9 UHS–I DDR50 Mode

表 7-95 and 図 7-81 present switching characteristics for MMC0 – UHS-I DDR50 Mode.

表 7-95. Switching Characteristics for MMC0 – UHS-I DDR50 Mode

see 図 7-81

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.12	6.43	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[3:0] transition	1.12	6.43	ns

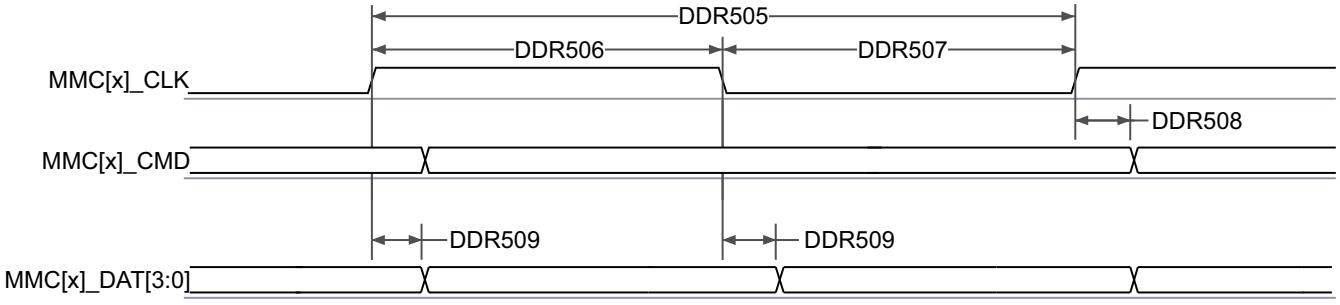


図 7-81. MMC0 – UHS-I DDR50 – Transmit Mode

7.11.5.16.1.10 UHS–I SDR104 Mode

表 7-96 and 図 7-82 present switching characteristics for MMC0 – UHS-I SDR104 Mode.

表 7-96. Switching Characteristics for MMC0 – UHS-I SDR104 Mode

see 図 7-82

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[3:0] transition	1.07	3.21	ns

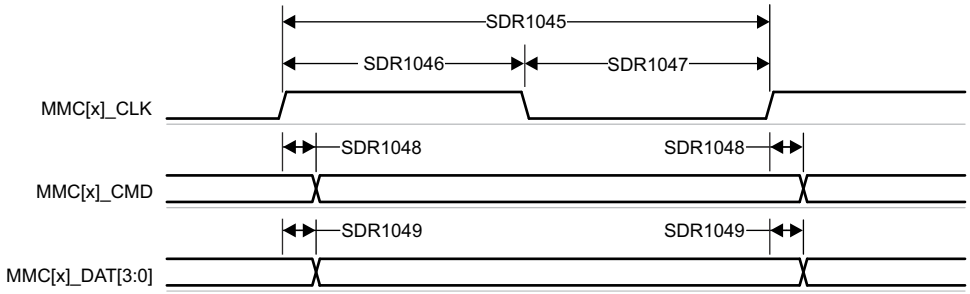


図 7-82. MMC0 – UHS-I SDR104 – Transmit Mode

7.11.5.16.2 MMC1/MMC2 - SD/SDIO Interface

MMC1/MMC2 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I DDR50
- UHS–I SDR104

表 7-97 presents the required DLL software configuration settings for MMC1/2 timing modes.

表 7-97. MMC1/MMC2 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG/ MMCSD2_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG/ MMCSD2_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x1	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x1	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning(1)	0x7
UHS-I DDR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0x9	0x1	Tuning(1)	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x6	0x1	Tuning(1)	0x7

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

表 7-98 presents timing conditions for MMC1.

表 7-98. MMC1/MMC2 Timing Conditions

PARAMETER			MIN	MAX	UNIT
Input Conditions					
SR_I	Input slew rate	Default Speed High Speed	0.69	2.06	V/ns
		UHS–I SDR12 UHS–I SDR25	0.34	1.34	V/ns
		UHS–I DDR50	1	2	V/ns
Output Conditions					
C_L	Output load capacitance	All modes	1	10	pF
PCB Connectivity Requirements					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	239	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	High Speed UHS–I SDR104		8	ps
		UHS–I DDR50		20	ps
		All other modes		100	ps

7.11.5.16.2.1 Default Speed Mode

表 7-99, 図 7-83, 表 7-100, and 図 7-84 present timing requirements and switching characteristics for MMC1/MMC2 – Default Speed Mode.

表 7-99. Timing Requirements for MMC1/MMC2 – Default Speed Mode

see 図 7-83

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.67		ns

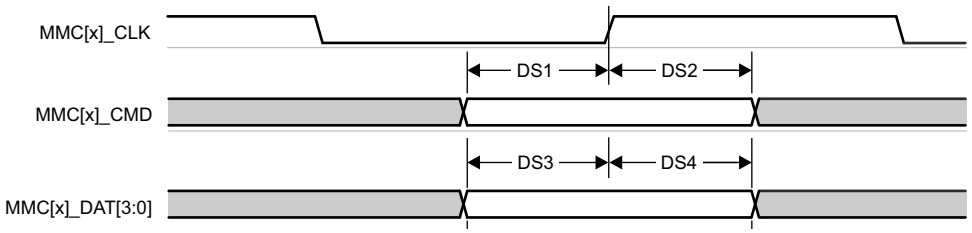


図 7-83. MMC1/MMC2 – Default Speed – Receive Mode

表 7-100. Switching Characteristics for MMC1/MMC2 – Default Speed Mode

see 図 7-84

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

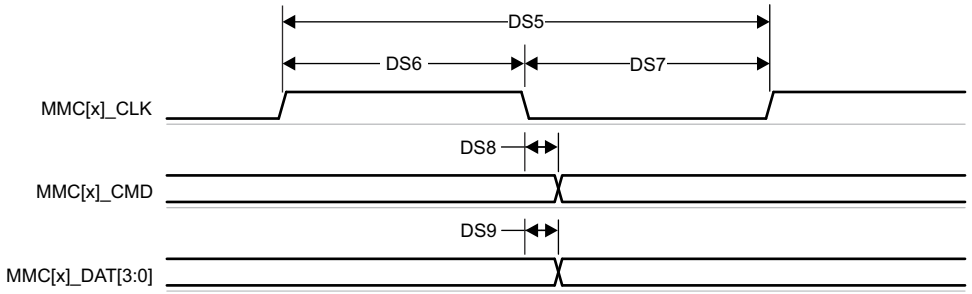


図 7-84. MMC1/MMC2 – Default Speed – Transmit Mode

7.11.5.16.2.2 High Speed Mode

表 7-101, 図 7-85, 表 7-102, and 図 7-86 present timing requirements and switching characteristics for MMC1/MMC2 – High Speed Mode.

表 7-101. Timing Requirements for MMC1/MMC2 – High Speed Mode

see 図 7-85

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.24		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.66		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.24		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.66		ns

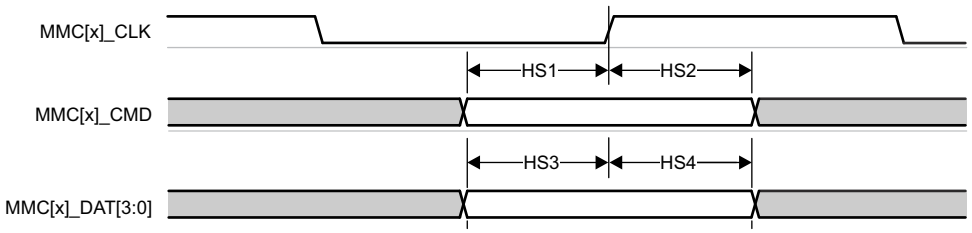


図 7-85. MMC1/MMC2 – High Speed – Receive Mode

表 7-102. Switching Characteristics for MMC1/MMC2 – High Speed Mode

see 図 7-86

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMCx_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

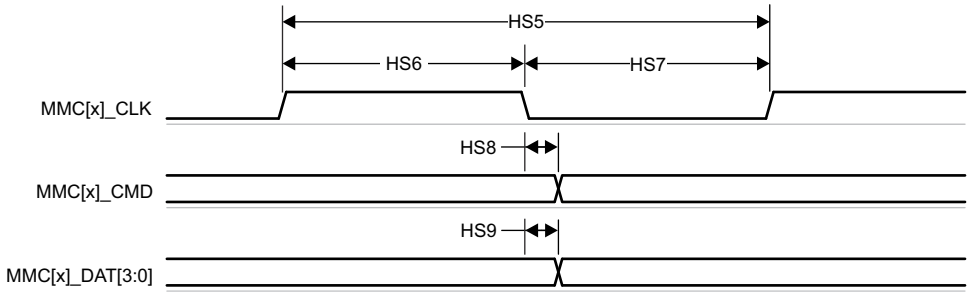


図 7-86. MMC1/MMC2 – High Speed – Transmit Mode

7.11.5.16.2.3 UHS–I SDR12 Mode

表 7-103, 図 7-87, 表 7-104, and 図 7-88 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR12 Mode.

表 7-103. Timing Requirements for MMC1/MMC2 – UHS-I SDR12 Mode

see 図 7-87

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	4.2		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	0.87		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	4.2		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	0.87		ns

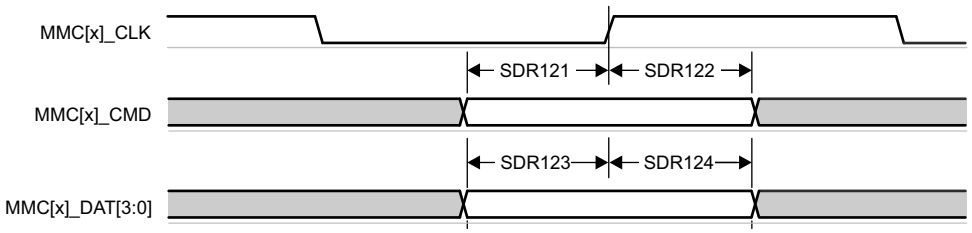


図 7-87. MMC1/MMC2 – UHS-I SDR12 – Receive Mode

表 7-104. Switching Characteristics for MMC1/MMC2 – UHS-I SDR12 Mode

see 図 7-88

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.5	8.6	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.5	8.6	ns

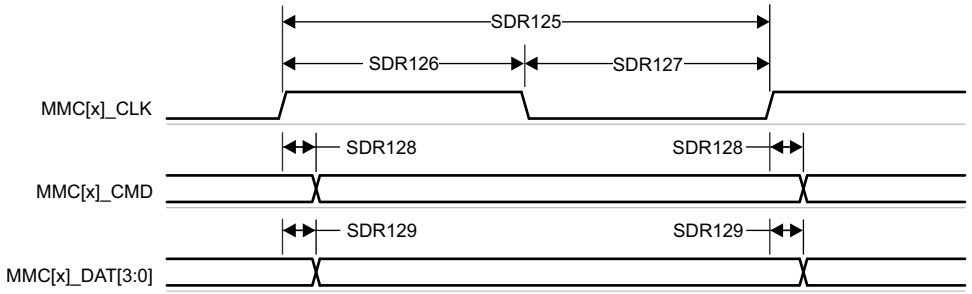


図 7-88. MMC1/MMC2 – UHS-I SDR12 – Transmit Mode

7.11.5.16.2.4 UHS–I SDR25 Mode

表 7-105, 図 7-89, 表 7-106, and 図 7-90 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR25 Mode.

表 7-105. Timing Requirements for MMC1/MMC2 – UHS-I SDR25 Mode

see 図 7-89

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.27		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.27		ns

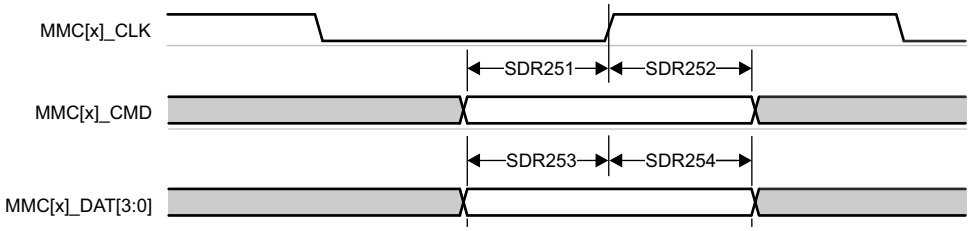


図 7-89. MMC1/MMC2 – UHS-I SDR25 – Receive Mode

表 7-106. Switching Characteristics for MMC1/MMC2 – UHS-I SDR25 Mode

see 図 7-90

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	2.4	8.1	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	2.4	8.1	ns

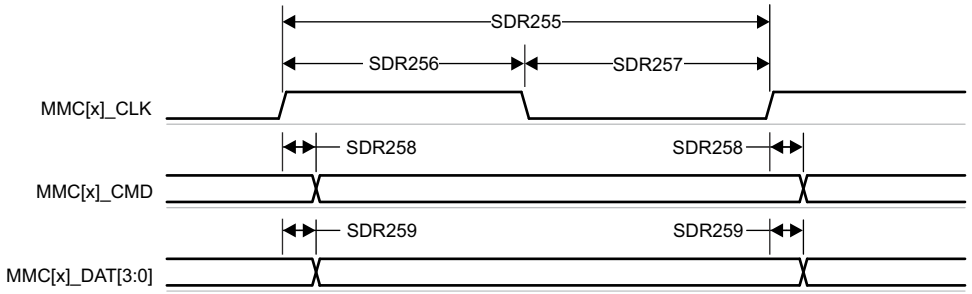


図 7-90. MMC1/MMC2 – UHS-I SDR25 – Transmit Mode

7.11.5.16.2.5 UHS–I SDR50 Mode

表 7-107 and 図 7-91 presents switching characteristics for MMC1/MMC2 – UHS-I SDR50 Mode.

表 7-107. Switching Characteristics for MMC1/MMC2 – UHS-I SDR50 Mode

see 図 7-91

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.2	6.35	ns

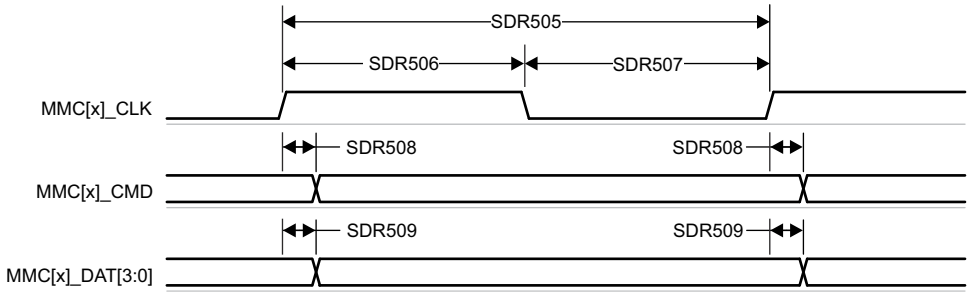


図 7-91. MMC1/MMC2 – UHS-I SDR50 – Transmit Mode

7.11.5.16.2.6 UHS–I DDR50 Mode

表 7-108 and 図 7-92 present switching characteristics for MMC1/MMC2 – UHS-I DDR50 Mode.

表 7-108. Switching Characteristics for MMC1/MMC2 – UHS-I DDR50 Mode

see 図 7-92

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.12	6.43	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMCx_CLK transition to MMCx_DAT[3:0] transition	1.12	6.43	ns

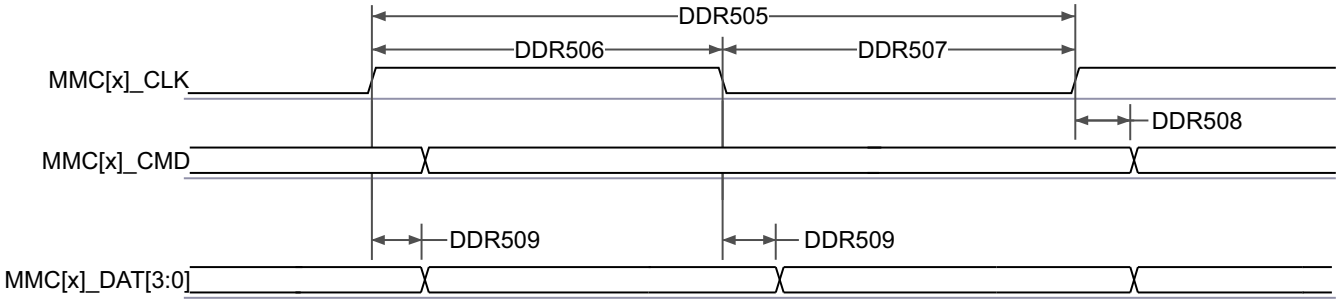


図 7-92. MMC1/MMC2 – UHS-I DDR50 – Transmit Mode

7.11.5.16.2.7 UHS–I SDR104 Mode

表 7-109 and 図 7-93 present switching characteristics for MMC1/MMC2 – UHS-I SDR104 Mode.

表 7-109. Switching Characteristics for MMC1/MMC2 – UHS-I SDR104 Mode

see 図 7-93

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMCx_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.07	3.21	ns

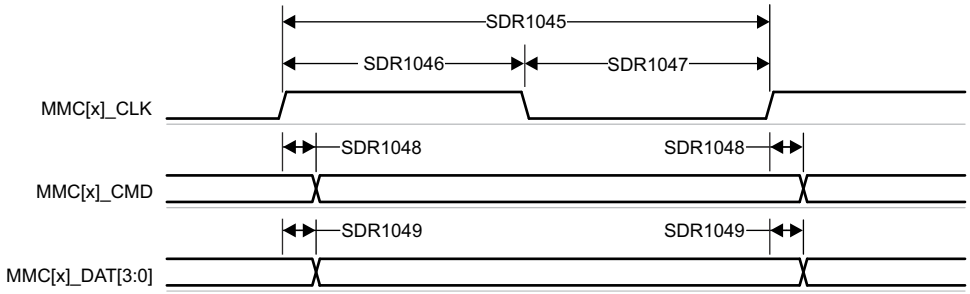


図 7-93. MMC1/MMC2 – UHS-I SDR104 – Transmit Mode

7.11.5.17 OLDI

7.11.5.17.1 OLDI0 Switching Characteristics

表 7-110 and 図 7-94 present switching characteristics for OLDI0.

表 7-110. OLDI0 Switching Characteristics

NO.	PARAMETER		MODE	MIN	TYP	MAX	UNIT
OLDI1	$t_{t(LHTT)}$	Rise time, OLDI0_CLK[1:0]P, OLDI0_CLK[1:0]N, OLDI0_A[7:0]P, and OLDI0_A[7:0]N	Slow(1)			0.5	ns
			Fast(2)			0.25	ns
OLDI2	$t_{t(HLTT)}$	Fall time, OLDI0_CLK[1:0]P, OLDI0_CLK[1:0]N, OLDI0_A[7:0]P, and OLDI0_A[7:0]N	Slow(1)			0.5	ns
			Fast(2)			0.25	ns
OLDI3	$t_{c(CLK)}$	Cycle time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N		6.06		110.01	ns
OLDI4	$t_{w(BIT)}$	Bit width, OLDI0_A[7:0]P and OLDI0_A[7:0]N			(1/7)OLDI3		ns
OLDI5	$t_{d(BIT1)}$	Bit 1 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		- (0.1)OLDI3		(0.1)OLDI3	ns
OLDI6	$t_{d(BIT0)}$	Bit 0 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(1/7)OLDI3 - (0.1)OLDI3		(1/7) OLDI3 + (0.1)OLDI3	ns
OLDI7	$t_{d(BIT6)}$	Bit 6 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(2/7)OLDI3 - (0.1)OLDI3		(2/7) OLDI3 + (0.1)OLDI3	ns
OLDI8	$t_{d(BIT5)}$	Bit 5 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(3/7)OLDI3 - (0.1)OLDI3		(3/7) OLDI3 + (0.1)OLDI3	ns
OLDI9	$t_{d(BIT4)}$	Bit 4 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(4/7)OLDI3 - (0.1)OLDI3		(4/7) OLDI3 + (0.1)OLDI3	ns
OLDI10	$t_{d(BIT3)}$	Bit 3 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(5/7)OLDI3 - (0.1)OLDI3		(5/7) OLDI3 + (0.1)OLDI3	ns
OLDI11	$t_{d(BIT2)}$	Bit 2 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(6/7)OLDI3 - (0.1)OLDI3		(6/7) OLDI3 + (0.1)OLDI3	ns
OLDI12	$t_{sk(TCCS)}$	Skew, OLDI0_A[7:0]P and OLDI0_A[7:0]N relative to any other OLDI0_A[7:0]P and OLDI0_A[7:0]N				50	ps

(1) Slow mode: TXDRV[3:0] = 0100b without back termination (RTERM_EN = 0b with 100Ω differential termination on far-end only)
(2) Fast mode: TXDRV[3:0] = 1000b with back termination (RTERM_EN = 1b with 100Ω differential termination on far-end only, or RTERM_EN = 0b with 100Ω differential termination on near-end and far-end)

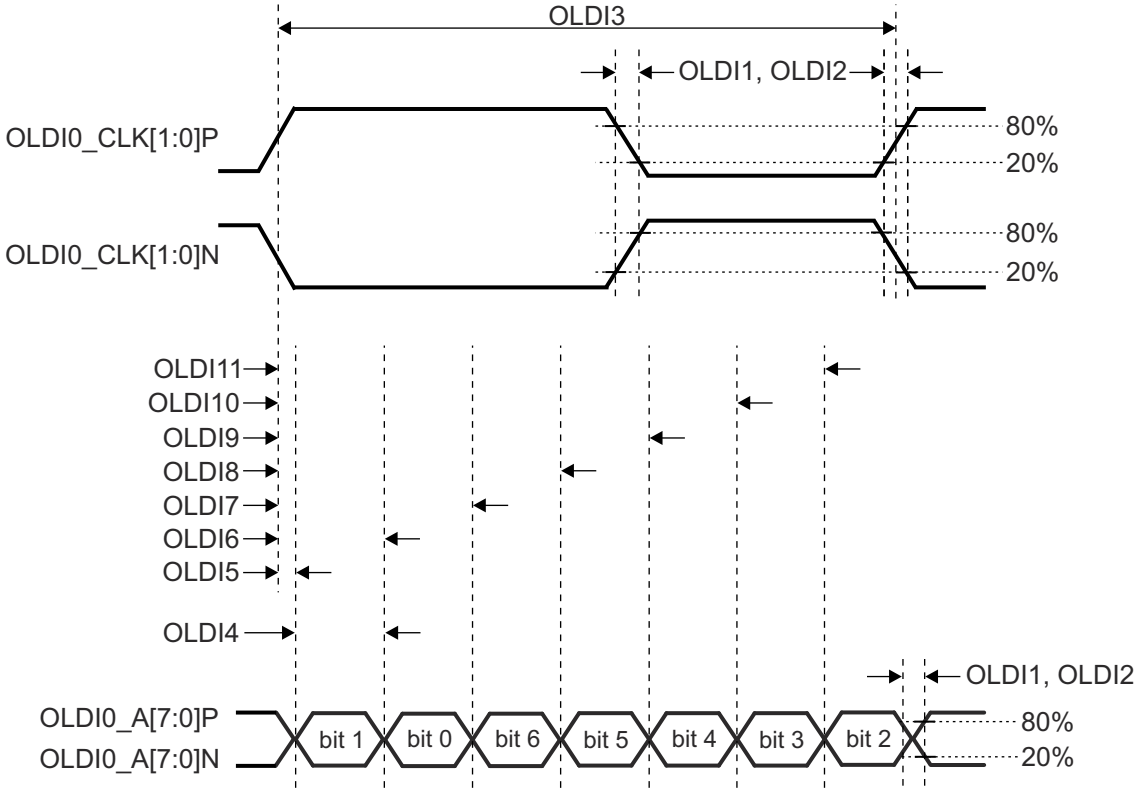


図 7-94. OLDI0 Switching Characteristics

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

7.11.5.18 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200 MHz, which produces an OSPI0_CLK rate up to 50 MHz for SDR mode or 25 MHz for DDR mode.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

セクション 7.11.5.18.1 defines timing requirements and switching characteristics associated with PHY mode and セクション 7.11.5.18.2 defines timing requirements and switching characteristics associated with Tap mode.

表 7-111 presents timing conditions for OSPI0.

表 7-111. OSPI0 Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

7.11.5.18.1 OSPI0 PHY Mode

7.11.5.18.1.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

表 7-112 defines DLL delays required for OSPI0 with Data Training. 表 7-113, 図 7-95, 表 7-114, and 図 7-96 present timing requirements and switching characteristics for OSPI0 with Data Training.

表 7-112. OSPI0 DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

表 7-113. OSPI0 Timing Requirements – PHY Data Training

see 図 7-95

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.

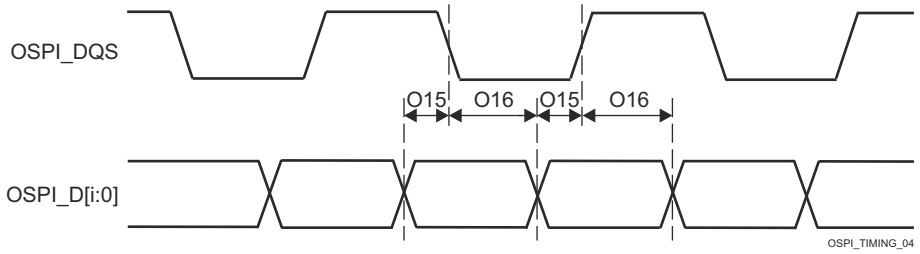


図 7-95. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

表 7-114. OSPI Switching Characteristics – PHY Data Training

See 図 7-96

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V, DDR	6.02	7.52	ns
			3.3V, DDR	7.52	7.52	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	DDR	((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	DDR	((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge	DDR	((0.475P(1)) + (0.975M(2)R(4)) + (0.04TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.11TD(5)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge	DDR	((0.475P(1)) + (0.975N(3)R(4)) - (0.04TD(5)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) - (0.11TD(5)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	DDR	(6)	(6)	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.

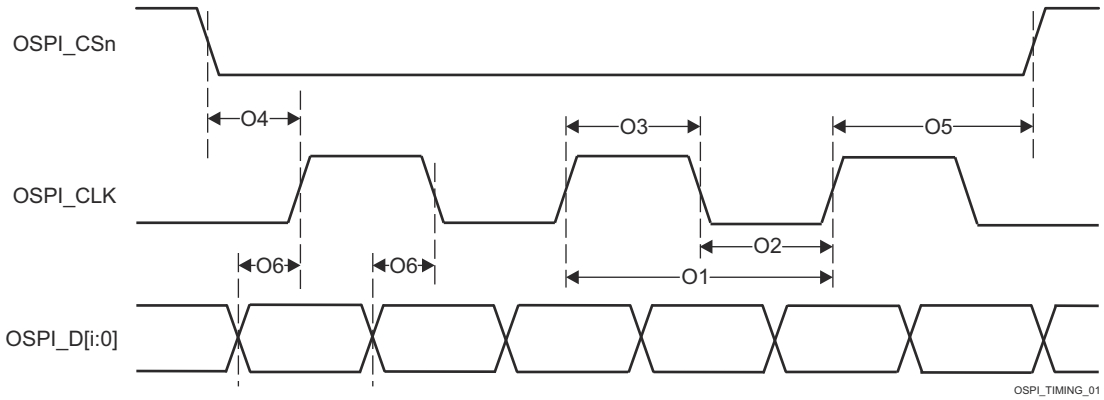


図 7-96. OSPI0 Switching Characteristics – PHY DDR Data Training

7.11.5.18.1.2 OSPI0 Without Data Training

注

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in 表 7-115 and 表 7-118.

7.11.5.18.1.2.1 OSPI0 PHY SDR Timing

表 7-115 defines DLL delays required for OSPI0 PHY SDR Mode. 表 7-116, 図 7-97, 図 7-98, 表 7-117, and 図 7-99 present timing requirements and switching characteristics for OSPI0 PHY SDR Mode.

表 7-115. OSPI0 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

表 7-116. OSPI0 Timing Requirements – PHY SDR Mode

see 図 7-97 and 図 7-98

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	4.8		ns
			3.3V, SDR with Internal PHY Loopback	5.19		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	-0.5		ns
			3.3V, SDR with Internal PHY Loopback	-0.5		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	0.6		ns
			3.3V, SDR with External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	1.7		ns
			3.3V, SDR with External Board Loopback	2.0		ns

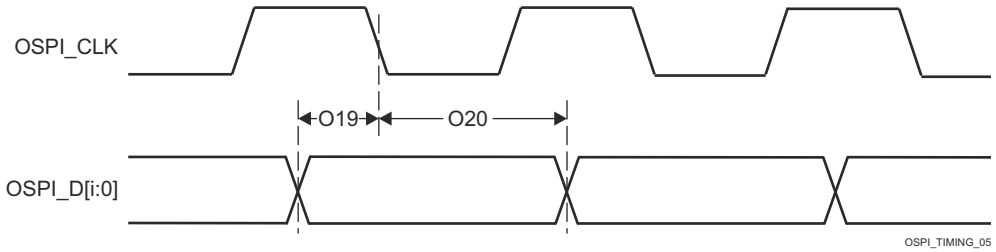


図 7-97. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

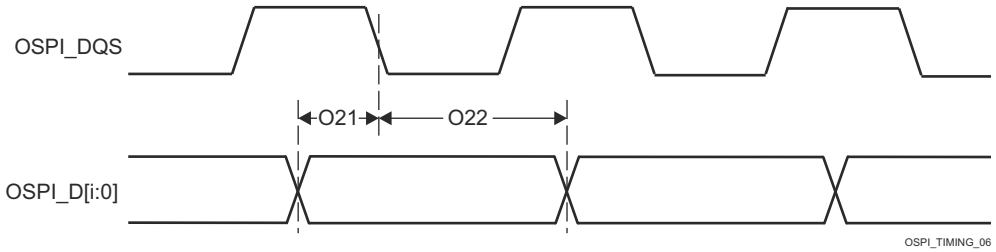


図 7-98. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

表 7-117. OSPI0 Switching Characteristics – PHY SDR Mode

see 図 7-99

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V	7		ns
			3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-1.16	1.25	ns
			3.3V	-1.33	1.51	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

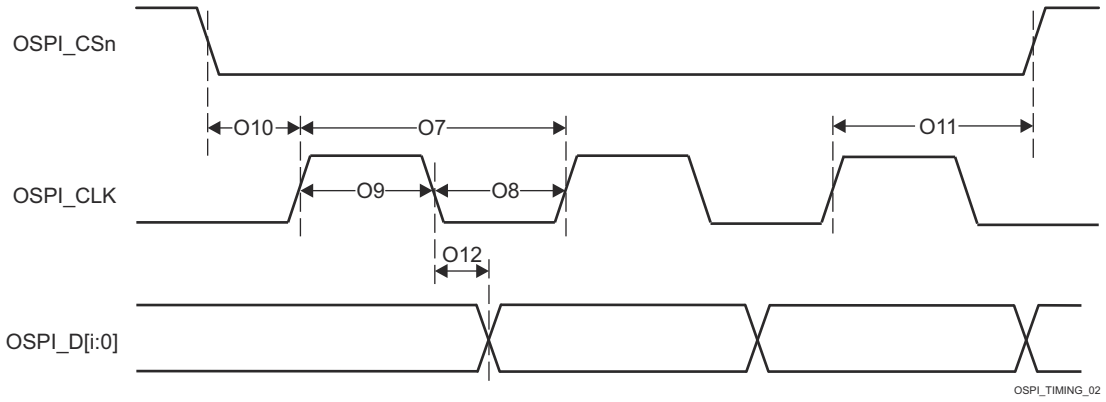


図 7-99. OSPI0 Switching Characteristics – PHY SDR

7.11.5.18.1.2.2 OSPI0 PHY DDR Timing

表 7-118 defines DLL delays required for OSPI0 PHY DDR Mode. 表 7-119, 図 7-100, 表 7-120, and 図 7-101 present timing requirements and switching characteristics for OSPI0 PHY DDR Mode.

表 7-118. OSPI0 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x46
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x43
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x15
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

表 7-119. OSPI0 Timing Requirements – PHY DDR Mode

see 図 7-100

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	0.53		ns
			1.8V, DDR with DQS	-0.46		ns
			3.3V, DDR with External Board Loopback	1.23		ns
			3.3V, DDR with DQS	-0.66		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	1.24(1)		ns
			1.8V, DDR with DQS	3.59		ns
			3.3V, DDR with External Board Loopback	1.44(1)		ns
			3.3V, DDR with DQS	7.92		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical OSPI/QSPI/SPI device. Therefore, the trace length between the SoC and attached OSPI/QSPI/SPI device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI0_LBCLKO to OSPI0_DQS) may need to be shortened to compensate.

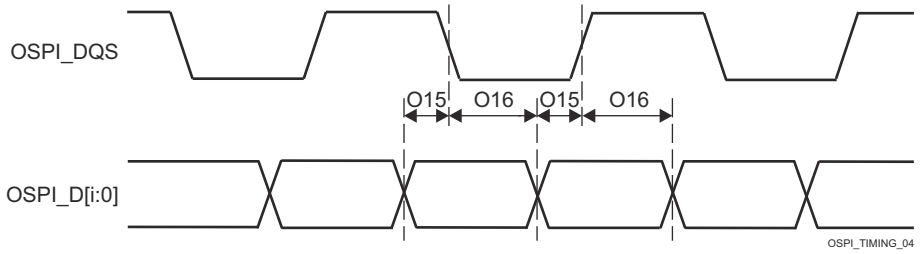


図 7-100. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS

表 7-120. OSPI0 Switching Characteristics – PHY DDR Mode

see 図 7-101

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		19		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) - (0.975M(2)R(4)))	((0.525P(1)) - (1.025M(2)R(4)) + 7)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 7)	((0.525P(1)) + (1.025N(3)R(4)))	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-7.71	-1.56	ns
			3.3V	-7.71	-1.56	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

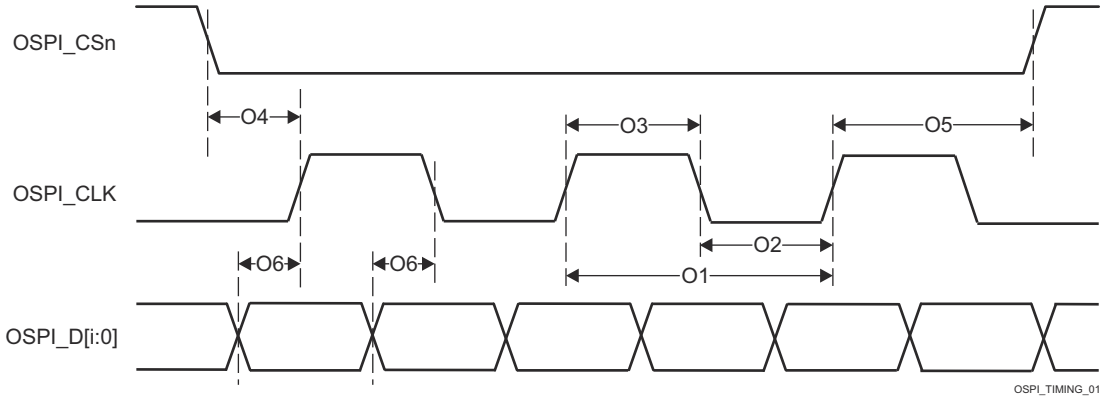


図 7-101. OSPI0 Switching Characteristics – PHY DDR

7.11.5.18.2 OSPI0 Tap Mode

7.11.5.18.2.1 OSPI0 Tap SDR Timing

表 7-121, 図 7-102, 表 7-122, and 図 7-103 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

表 7-121. OSPI0 Timing Requirements – Tap SDR Mode

see 図 7-102

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(15.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 4.3 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

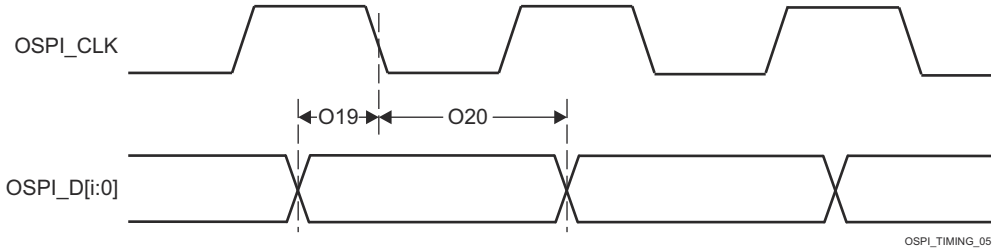


図 7-102. OSPI0 Timing Requirements – Tap SDR, No Loopback

表 7-122. OSPI0 Switching Characteristics – Tap SDR Mode

see 図 7-103

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		- 4.25	7.25	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

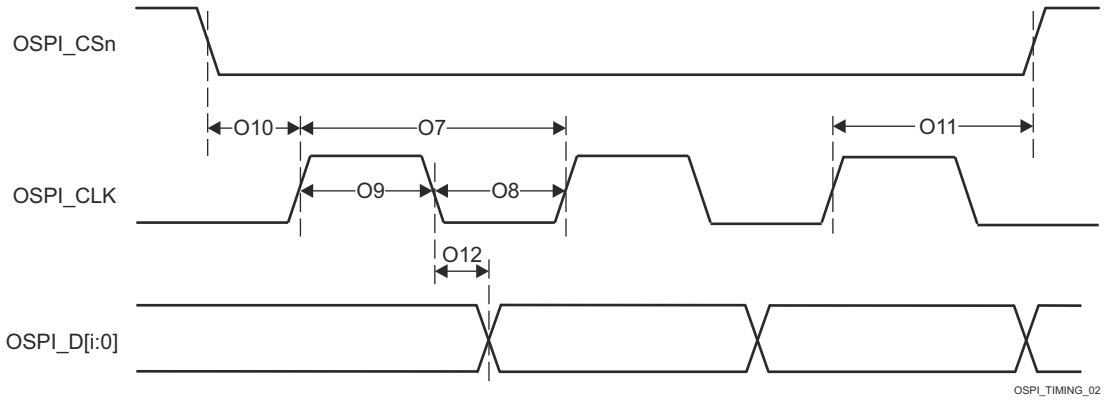


図 7-103. OSPI0 Switching Characteristics – Tap SDR, No Loopback

7.11.5.18.2.2 OSPI0 Tap DDR Timing

表 7-123, 図 7-104, 表 7-124, and 図 7-105 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

表 7-123. OSPI0 Timing Requirements – Tap DDR Mode

see 図 7-104

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(17.04 - (0.975T(1)R(2)))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 3.16 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

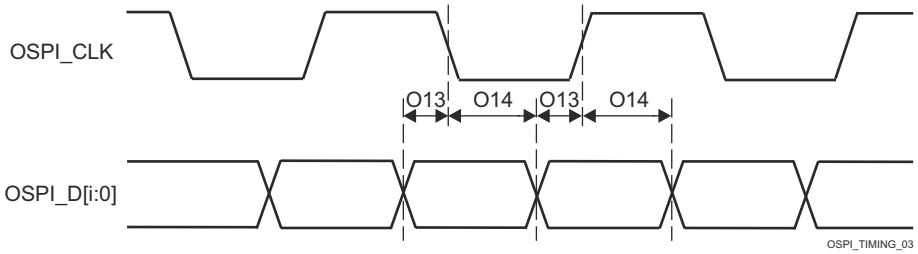


図 7-104. OSPI0 Timing Requirements – Tap DDR, No Loopback

表 7-124. OSPI0 Switching Characteristics – Tap DDR Mode

see 図 7-105

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + ((0.975M(2)R(5)) - 1)	((0.525P(1)) + (1.025M(2)R(5)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(5)) - 1)	((0.525P(1)) + (1.025N(3)R(5)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		(- 5.04 + (0.975(T(4) + 1)R(5)) - (0.525P(1)))	(3.64 + (1.025(T(4) + 1)R(5)) - (0.475P(1)))	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]
(5) R = reference clock cycle time in ns

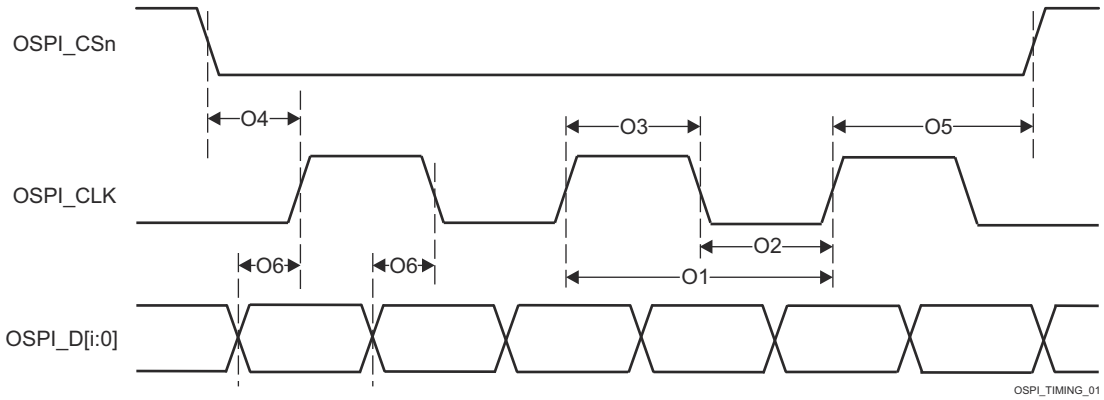


図 7-105. OSPI0 Switching Characteristics – Tap DDR, No Loopback

7.11.5.19 PRUSS

The device has a single Programmable Real-Time Unit Subsystem (PRUSS), which includes two PRU cores. The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and off-loading of tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRUSS, see the corresponding sections within *Signal Descriptions* and *Detailed Description*.

注

PRUSS contains a second layer of peripheral signal multiplexing to enable additional functionality on the PRU GPO and GPI signals. This peripheral multiplexing is described in the PRUSS chapter in the device TRM.

注

PRUSS has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

7.11.5.19.1 PRUSS Programmable Real-Time Unit (PRU)

注

PRUSS signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

表 7-125. PRUSS PRU Timing Conditions

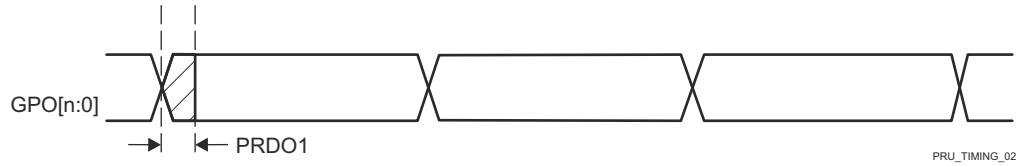
PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	30	pF

7.11.5.19.1.1 PRUSS PRU Direct Output Mode Timing

表 7-126. PRUSS PRU Switching Characteristics – Direct Output Mode

see 図 7-106

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	$t_{sk(GPO-GPO)}$	Skew, GPO to GPO		2	ns



A. n in GPO[n:0] = 19.

図 7-106. PRUSS PRU Direct Output Timing

7.11.5.19.1.2 PRUSS PRU Parallel Capture Mode Timing

表 7-127. PRUSS PRU Timing Requirements – Parallel Capture Mode

see 図 7-107 and 図 7-108

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	$t_{c(CLOCK)}$	Cycle time, CLOCKIN	20		ns
PRPC2	$t_{w(CLOCKL)}$	Pulse duration, CLOCKIN low	0.45P(1)		ns
PRPC3	$t_{w(CLOCKH)}$	Pulse duration, CLOCKIN high	0.45P(1)		ns
PRPC4	$t_{su(DATAIN-CLOCK)}$	Setup time, DATAIN valid before CLOCKIN active edge	4		ns
PRPC5	$t_{h(CLOCK-DATAIN)}$	Hold time, DATAIN valid after CLOCKIN active edge	0		ns

(1) P = CLOCKIN cycle time in ns

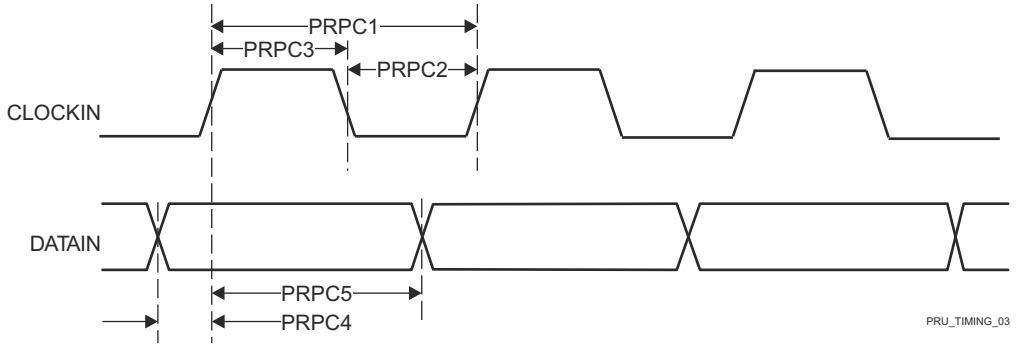


図 7-107. PRUSS PRU Parallel Capture Timing Requirements – Rising Edge Mode

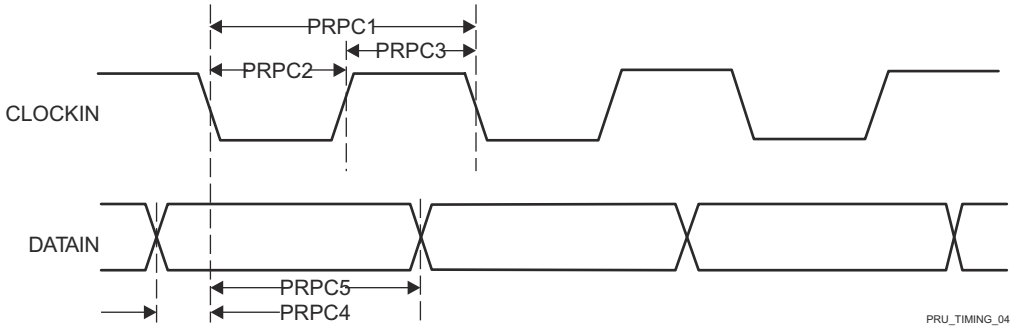


図 7-108. PRUSS PRU Parallel Capture Timing Requirements – Falling Edge Mode

7.11.5.19.1.3 PRUSS PRU Shift Mode Timing

表 7-128. PRUSS PRU Timing Requirements – Shift In Mode

see 図 7-109

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSI1	$t_{w(DATAINH)}$	Pulse duration, DATAIN high	2P(1) + 2		ns
PRSI2	$t_{w(DATAINL)}$	Pulse duration, DATAIN low	2P(1) + 2		ns

(1) P = Internal shift in clock period in ns, defined by PRUn_GPI_DIV0 and PRUn_GPI_DIV1 bit fields in the GPCFGn_REG register, where PRUn represents the respective PRU0 or PRU1 instance.

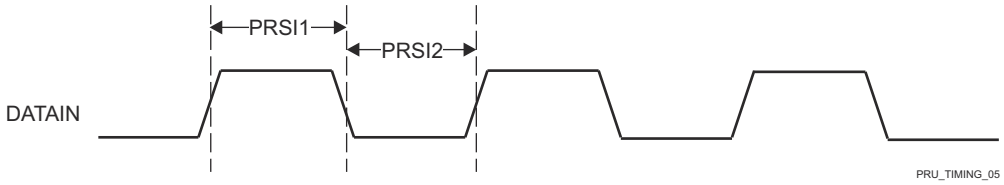


図 7-109. PRUSS PRU Shift In Timing

表 7-129. PRUSS PRU Switching Characteristics – Shift Out Mode

see 図 7-110

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_{c(CLOCKOUT)}$	Cycle time, CLOCKOUT	10		ns
PRSO2L	$t_{w(CLOCKOUTL)}$	Pulse duration, CLOCKOUT low	0.475P(1)Z(2) - 0.3		ns
PRSO2H	$t_{w(CLOCKOUTH)}$	Pulse duration, CLOCKOUT high	0.475P(1)Y(3) - 0.3		ns
PRSO3	$t_{d(CLOCKOUT-DATAOUT)}$	Delay time, CLOCKOUT to DATAOUT valid	0	3	ns

(1) P = Software programmable shift out clock period in ns, defined by PRUn_GPO_DIV0 and PRUn_GPO_DIV1 bit fields in the GPCFGn_REG register, where PRUn represents the respective PRU0 or PRU1 instance.

(2) The Z parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.

a. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are INTEGERS -or- if PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an EVEN INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1).

b. If PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an ODD INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.5).

c. If PRUn_GPI_DIV0 is an INTEGER and PRUn_GPI_DIV1 is a NON-INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.5 * PRUn_GPI_DIV0).

d. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are NON-INTEGERS then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.25 * PRUn_GPI_DIV0).

(3) The Y parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.

a. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are INTEGERS -or- if PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an EVEN INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1).

b. If PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an ODD INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.5).

c. If PRUn_GPI_DIV0 is an INTEGER and PRUn_GPI_DIV1 is a NON-INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.5 * PRUn_GPI_DIV0).

d. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are NON-INTEGERS then, Y1 equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.25 * PRUn_GPI_DIV0) and Y2 equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.25 * PRUn_GPI_DIV0), where Y1 is the first high pulse and Y2 is the second high pulse.

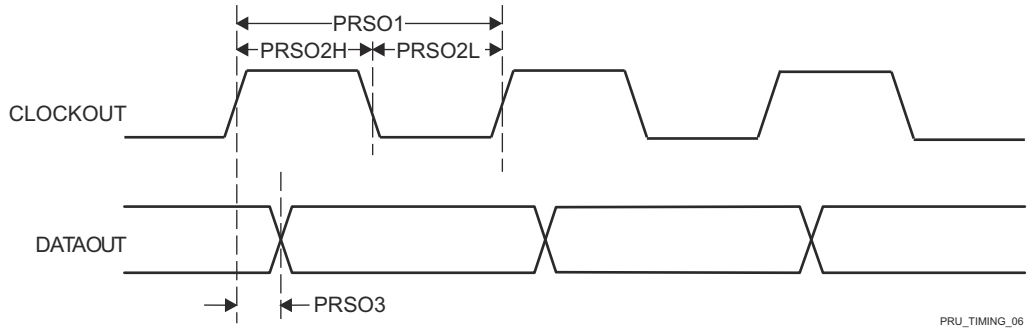


図 7-110. PRUSS PRU Shift Out Timing

7.11.5.19.2 PRUSS Industrial Ethernet Peripheral (IEP)

表 7-130. PRUSS IEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	10	pF

7.11.5.19.2.1 PRUSS IEP Timing

表 7-131. PRUSS IEP Switching Characteristics – Digital IOs

see 図 7-111

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO4	$t_{sk(EDIO\_DATA\_OUT)}$	EDIO_DATA_OUT skew		5	ns

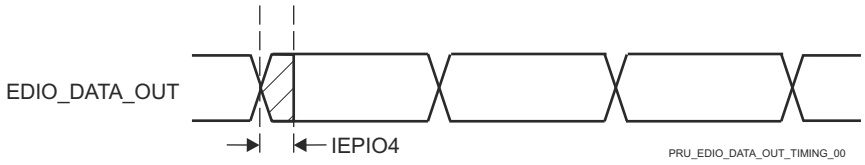


図 7-111. PRUSS IEP Digital IOs Timing Requirements

7.11.5.19.3 PRUSS Universal Asynchronous Receiver Transmitter (UART)

表 7-132. PRUSS UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

7.11.5.19.3.1 PRUSS UART Timing

表 7-133. PRUSS UART Timing Requirements

see 図 7-112

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

表 7-134. PRUSS UART Switching Characteristics

see 図 7-112

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	f(baud)	Programmed baud rate		12	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2	U(1) + 2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2	U(1) + 2	ns

(1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.

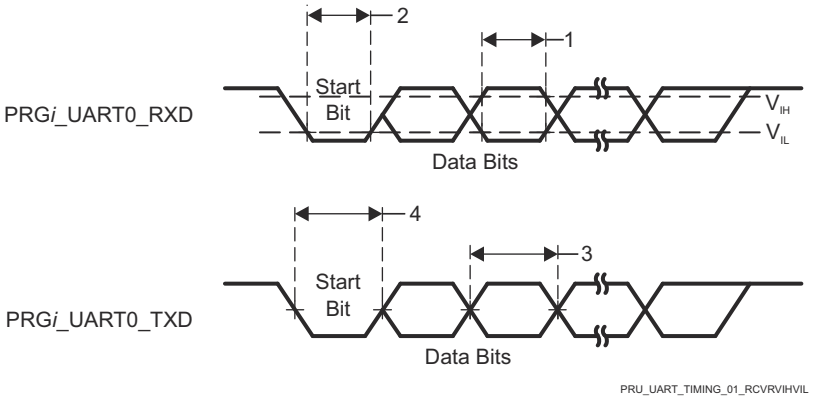


図 7-112. PRUSS UART Timing Requirements and Switching Characteristics

7.11.5.19.4 PRUSS Enhanced Capture Peripheral (ECAP)

表 7-135. PRUSS ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

7.11.5.19.4.1 PRUSS ECAP Timing

表 7-136. PRUSS ECAP Timing Requirements

see 図 7-113

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	$t_{w(CAP)}$	Pulse Duration, CAP (asynchronous)	2P(1) + 2		ns
PREP2	$t_{w(SYNCI)}$	Pulse Duration, SYNCI (asynchronous)	2P(1) + 2		ns

(1) P = CORE_CLK period in ns.

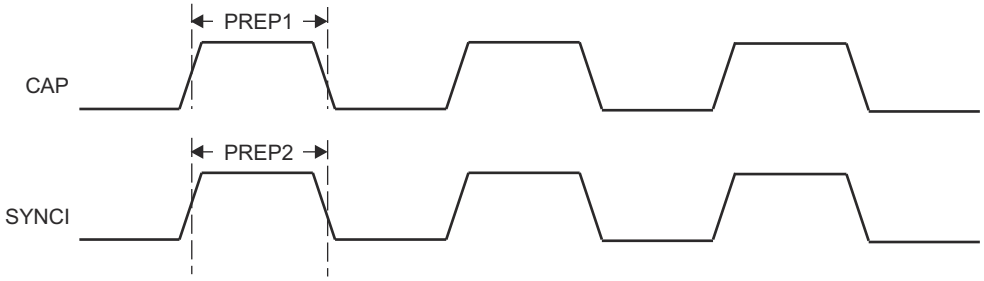


図 7-113. PRUSS ECAP Timing

表 7-137. PRUSS ECAP Switching Characteristics

see 図 7-114

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	$t_{w(APWM)}$	Pulse Duration, APWM high/low	2P(1) - 2		ns
PREP4	$t_{w(SYNCO)}$	Pulse Duration, SYNCO (asynchronous)	P(1) - 2		ns

(1) P = CORE_CLK period in ns.

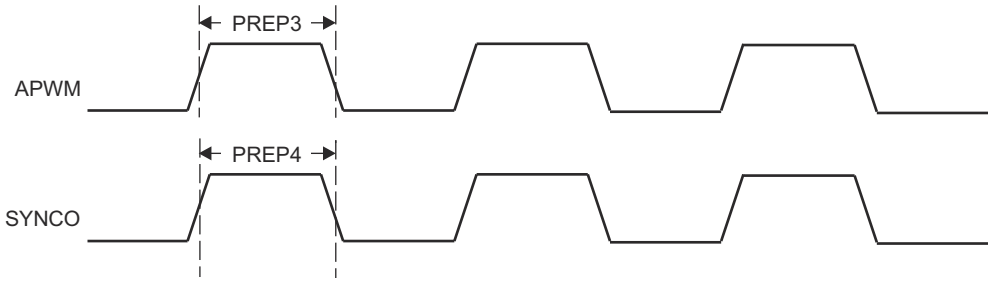


図 7-114. PRUSS ECAP Switching Characteristics

7.11.5.20 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-138. Timer Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

表 7-139. Timer Input Timing Requirements

see 図 7-115

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	4P(1)+ 2.5		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	4P(1)+ 2.5		ns

(1) P = functional clock period in ns.

表 7-140. Timer Output Switching Characteristics

see 図 7-115

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	4P(1) - 2.5		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	4P(1) - 2.5		ns

(1) P = functional clock period in ns.

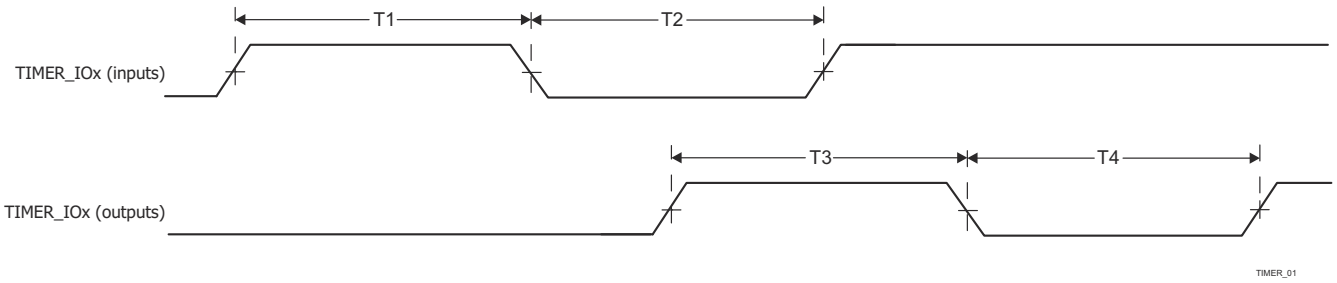


図 7-115. Timer Timing Requirements and Switching Characteristics

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

7.11.5.21 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 7-141. UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

表 7-142. UART Timing Requirements

see 図 7-116

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

表 7-143. UART Switching Characteristics

see 図 7-116

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate for Main Domain UARTs		12	Mbps
		Programmable baud rate for MCU and WKUP Domain UARTs		3.7	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2	U(1) + 2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2		ns

(1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.

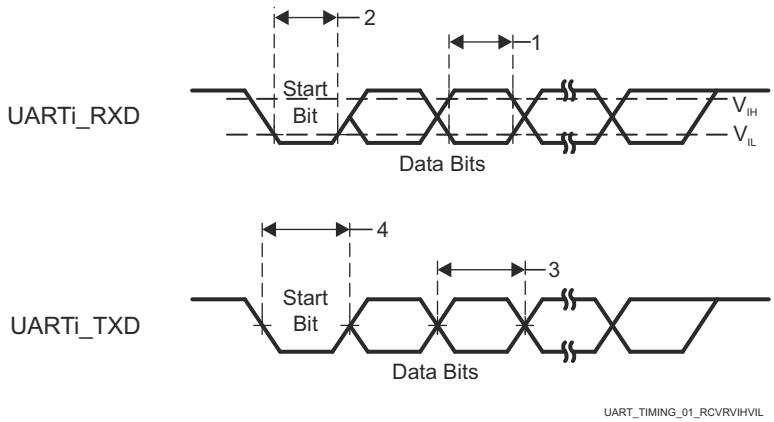


図 7-116. UART Timing Requirements and Switching Characteristics

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

7.11.5.22 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

8 Detailed Description

8.1 Overview

The low-cost AM62x Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance and embedded features, such as: dual-display support and 3D graphics acceleration, along with an extensive set of peripherals that make the AM62x device well-suited for a broad range of industrial and automotive applications while offering intelligent features and optimized power architecture as well.

Some of these applications include:

- Industrial HMI
- EV charging stations
- Touchless building access
- Driver monitoring systems

AM62x Sitara™ processors are industrial-grade in the 13 x 13 mm package (ALW) and can meet the AEC - Q100 automotive standard in the 17.2 x 17.2 mm package (AMC). Industrial and Automotive functional safety requirements can be addressed using the integrated Cortex-M4F cores and dedicated peripherals, which can all be isolated from the rest of the AM62x processor.

The 3-port Gigabit Ethernet switch has one internal port and two external ports with Time-Sensitive Networking (TSN) support. An additional PRU module on the device enables real-time I/O capability for customer's own use cases. In addition, the extensive set of peripherals included in AM62x enables system-level connectivity, such as: USB, MMC/SD, Camera interface, OSPI, CAN-FD and GPMC for parallel host interface to an external ASIC/FPGA. The AM62x device also supports secure boot for IP protection with the built-in Hardware Security Module (HSM) and employs advanced power management support for portable and power-sensitive applications

注

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

8.2 Processor Subsystems

8.2.1 Arm Cortex-A53 Subsystem

The SoC implements one cluster of quad-core Arm® Cortex®-A53 MPCore™, with 32KB L1 instruction, 32KB L1 data, per core and 512KB L2 shared cache.

The Cortex®-A53 cores are general-purpose processors that can be used for running customer applications.

注

Notes on references used in this document:

- A53SS is also referred to as Arm® CorePac.
- Cortex®-A53 is often shortened to A53.

The A53SS is built around the Cortex®-A53 MPCore™ (Arm®-A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus, it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

The Arm®v8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers. The A53 processor is Arm's first Arm®v8-A processor aimed at providing power-efficient 64-bit processing. It features an in-order, 8-stage, dual-issue pipeline, and improved integer, Arm® Neon™, Floating-Point Unit (FPU) and memory performance.

The A53 CPU supports two execution states: AArch32 and AArch64. The AArch64 state gives the A53 CPU its ability to execute 64-bit applications, while the AArch32 state allows the processor to execute existing Arm®v7-A applications.

For more information, see *Arm Cortex-A53 Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8.2.2 Device/Power Manager

The WKUP_R5FSS is a single-core implementation of the Arm® Cortex®-R5F processor that acts as the Device Manager responsible for boot, resource management, and power management functions. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ ™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

注

The Cortex-R5F processor is a Cortex-R5 processor that includes the optional floating point unit (FPU) extension. In this TRM, all references to the Cortex-R5 processor apply to the Cortex-R5F processor by default.

For more information, see *Device Manager Cortex R5F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8.2.3 Arm Cortex-M4F

The MCU_M4FSS is an Arm® Cortex®-M4F based subsystem that can run safety processing or be used as a general purpose MCU. During the boot process, the MCU_M4FSS will be configured by an initial software running on a different core. Following configuration, software will release the safety processor (M4F) out of reset, and at this point safety processor code or general purpose code can start execution.

注

The Cortex-M4F processor is a Cortex-M4 processor that includes the optional floating point unit (FPU) extension.

For more information, see *Cortex-M4F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8.3 Accelerators and Coprocessors

8.3.1 Graphics Processing Unit (GPU)

The GPU is an area optimized Graphics Core supporting OpenGL ES 3.1 and Vulkan 1.2.

For more information, see *Graphics Processing Unit* section in *Processors and Accelerators* chapter in the device TRM.

8.3.2 Programmable Real-Time Unit Subsystem (PRUSS)

The PRUSS consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Data RAMs per PRU core (DRAM)
- Instruction RAMs per PRU core (IRAM)
- Shared RAM (SRAM)
- Peripheral modules: UART0, ECAP0, IEP0, MDIO
- Interrupt Controller (INTC) per core

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

For more information, see *Programmable Real-Time Unit Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8.4 Other Subsystems

8.4.1 Dual Clock Comparator (DCC)

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator* section in *Peripherals* chapter in the device TRM.

8.4.2 Data Movement Subsystem (DMSS)

The DMSS module provides data movement (DMA) and bridges between the CBA switched interconnect and the packet streaming fabric (network on chip) on the device.

The Data Movement Subsystem (DMSS) consists of DMA/Queue Management components and Peripherals:

- Packet DMA
- Block Copy DMA
- Ring Accelerator
- Packet Streaming Interface (PSILSS)
- Infrastructure components such as CBASS, secure proxy, and an interrupt aggregator

8.4.3 Memory Cyclic Redundancy Check (MCRC)

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system.

For more information, see *Memory Cyclic Redundancy Check* section in *Peripherals* chapter in the device TRM.

8.4.4 Peripheral DMA Controller (PDMA)

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured transfer request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer DMSS destination channel which then performs the movement of the data into memory. Likewise, a remote DMSS source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (DMSS + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

8.4.5 Real-Time Clock (RTC)

The basic purpose for the RTC is to keep time of day. The other equally important purpose of RTC is for Digital Rights management. Some degree of tamper proofing is needed to ensure that simply stopping, resetting, or corrupting the RTC does not go unnoticed so that if this occurs, the application can re-acquire the time of day from a trusted source.

For more information, see *Real-Time Clock* section in *Peripherals* chapter in the device TRM.

8.5 Peripherals

8.5.1 Gigabit Ethernet Switch (CPSW3G)

The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

For more information, see *Gigabit Ethernet Switch* section in *Peripherals* chapter in the device TRM.

8.5.2 Camera Streaming Interface Receiver (CSI_RX_IF)

The integration of the CSI_RX_IF module allows the device to stream video inputs from multiple cameras to internal memory.

For more information, see *Camera Streaming Interface Receiver* section in *Peripherals* chapter in the device TRM.

8.5.3 DDR Subsystem (DDRSS)

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via CBASS0 interconnect.

For more information, see *DDR Subsystem* section in *Peripherals* chapter in the device TRM.

8.5.4 Display Subsystem (DSS)

The Display Subsystem (DSS) is a flexible, multi-pipeline subsystem that supports high-resolution display outputs. DSS includes input pipelines providing multi-layer blending with transparency to enable on-the-fly composition. Various pixel processing capabilities are supported, such as color space conversion and scaling, among others. DSS includes a DMA engine, which allows direct access to the frame buffer (device system memory). Display outputs can connect seamlessly to an Open LVDS Display Interface transmitter (OLDITX), or can directly drive device pads as a Display Parallel Interface (DPI).

For more information, see *Display Subsystem* section in *Peripherals* chapter in the device TRM.

8.5.5 Enhanced Capture (ECAP)

The ECAP module provides accurate timing of events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms.

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

For more information, see *Enhanced Capture* section in *Peripherals* chapter in the device TRM.

8.5.6 Error Location Module (ELM)

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

For more information, see *Error Location Module* section in *Peripherals* chapter in the device TRM.

8.5.7 Enhanced Pulse Width Modulation (EPWM)

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

For more information, see *Enhanced Pulse Width Modulation* section in *Peripherals* chapter in the device TRM.

8.5.8 Error Signaling Module (ESM)

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

For more information, see *Error Signaling Module* section in *Peripherals* chapter in the device TRM.

8.5.9 Enhanced Quadrature Encoder Pulse (EQEP)

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

For more information, see *Enhanced Quadrature Encoder Pulse* section in *Peripherals* chapter in the device TRM.

8.5.10 General-Purpose Interface (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface* section in *Peripherals* chapter in the device TRM.

8.5.11 General-Purpose Memory Controller (GPMC)

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller* section in *Peripherals* chapter in the device TRM.

8.5.12 Global Timebase Counter (GTC)

The GTC module provides a continuous running counter that can be used for time synchronization and debug trace time stamping.

For more information, see *Global Timebase Counter* section in *Peripherals* chapter in the device TRM.

8.5.13 Inter-Integrated Circuit (I2C)

The device contains multicontroller Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multicontroller I^2C module can be configured to act like a target or controller I^2C-compatible device.

I^2C instances may be implemented with dedicated, I^2C compliant, open-drain I/O buffers, or with standard LVCMOS I/O buffers. The I^2C instances associated with open-drain I/O buffers can support Hs-mode (up to 3.4 Mbps when the I/O buffers are operating at 1.8 V but limited to 400 kbps when the I/O buffers are operating at 3.3 V).

The I^2C instances associated with standard LVCMOS I/O buffers can support Fast-mode (up to 400 kbps). The LVCMOS I/O buffers being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.

For more information, see *Inter-Integrated Circuit* section in *Peripherals* chapter in the device TRM.

8.5.14 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

For more information, see *Modular Controller Area Network* section in *Peripherals* chapter in the device TRM.

8.5.15 Multichannel Audio Serial Port (MCASP)

This section introduces the Multichannel Audio Serial Port (MCASP) module and describes its main functions and connections in the device.

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port* section in *Peripherals* chapter in the device TRM.

8.5.16 Multichannel Serial Peripheral Interface (MCSPI)

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

For more information, see *Multichannel Serial Peripheral Interface* section in *Peripherals* chapter in the device TRM.

8.5.17 Multi-Media Card Secure Digital (MMCSD)

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded Multi-Media Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness

For more information, see *Multi-Media Card Secure Digital* section in *Peripherals* chapter in the device TRM.

8.5.18 Octal Serial Peripheral Interface (OSPI)

The Octal Serial Peripheral Interface (OSPI) module is a Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

8.5.19 Timers

All timers include specific functions to generate accurate tick interrupts to the operating system.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

8.5.20 Universal Asynchronous Receiver/Transmitter (UART)

The UART is a peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter* section in *Peripherals* chapter in the device TRM.

8.5.21 Universal Serial Bus Subsystem (USBSS)

USB (Universal Serial Bus) provides a low-cost connectivity solution for numerous consumer portable devices by implementing a mechanism for data transfer between USB devices.

The device instantiates two independent instances of a third-party USB subsystem (USB2SS) operating at up to USB2.0 speeds (480Mb/s), either of which can be independently configured to act as a USB Host or a USB Device.

For more information, see *Universal Serial Bus Subsystem* section in *Peripherals* chapter in the device TRM.

9 Applications, Implementation, and Layout

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Device Connection and Layout Fundamentals

9.1.1 Power Supply

9.1.1.1 Power Supply Designs

The TPS65219 Power Management IC (PMIC) is recommended for an integrated AM62x power solution. This cost and space optimized solution is designed to power the AM62 processor and its principal peripherals. For the full application note and operational details, refer to Powering the AM62x with the TPS65219 PMIC

List of benefits when using TPS65219 PMIC to power AM62x:

- Full device performance entitlement as validated on TI Evaluation boards
- Factory programmed configurations support power rail load steps, supply voltage accuracies and maximum load currents with margins
- Factory programmed configurations support LPDDR4 and DDR4 memory
- Meets all AM62x voltage and sequencing requirements, refer to セクション 7.5, *Recommended Operating Conditions* and セクション 7.11.2.2, *Power Supply Sequencing*

9.1.1.2 Power Distribution Network Implementation Guidance

The Sitara Processor Power Distribution Networks: Implementation and Analysis provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI *only* supports designs that follow the board design guidelines contained in the application report.

9.1.2 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

9.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

9.1.4 Reset

9.1.5 Unused Pins

For more information about Unused Pins, see セクション 6.4, *Pin Connectivity Requirements*

9.2 Peripheral- and Interface-Specific Design Information

9.2.1 DDR Board Design and Layout Guidelines

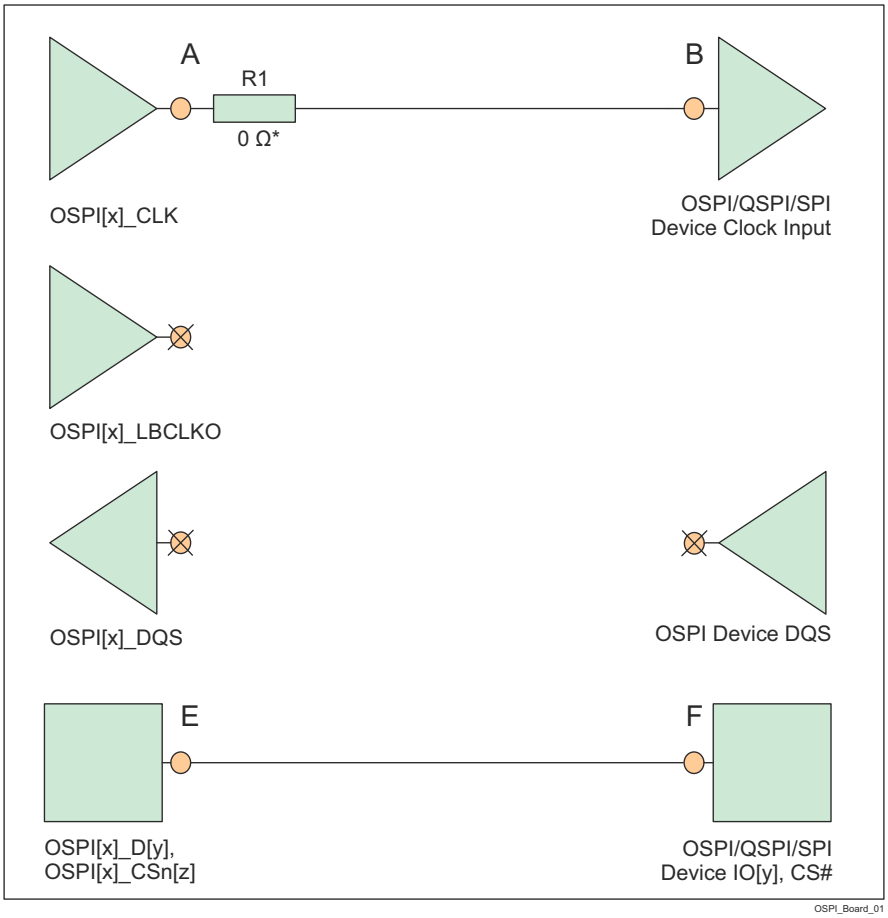
The goal of the **AM62x DDR Board Design and Layout Guidelines** is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 or LPDDR4 memories that follow the guidelines in this document.

9.2.2 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

9.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450 ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 9-1
- Propagation delays and matching:
  - (A to B) ≤ 450 ps
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

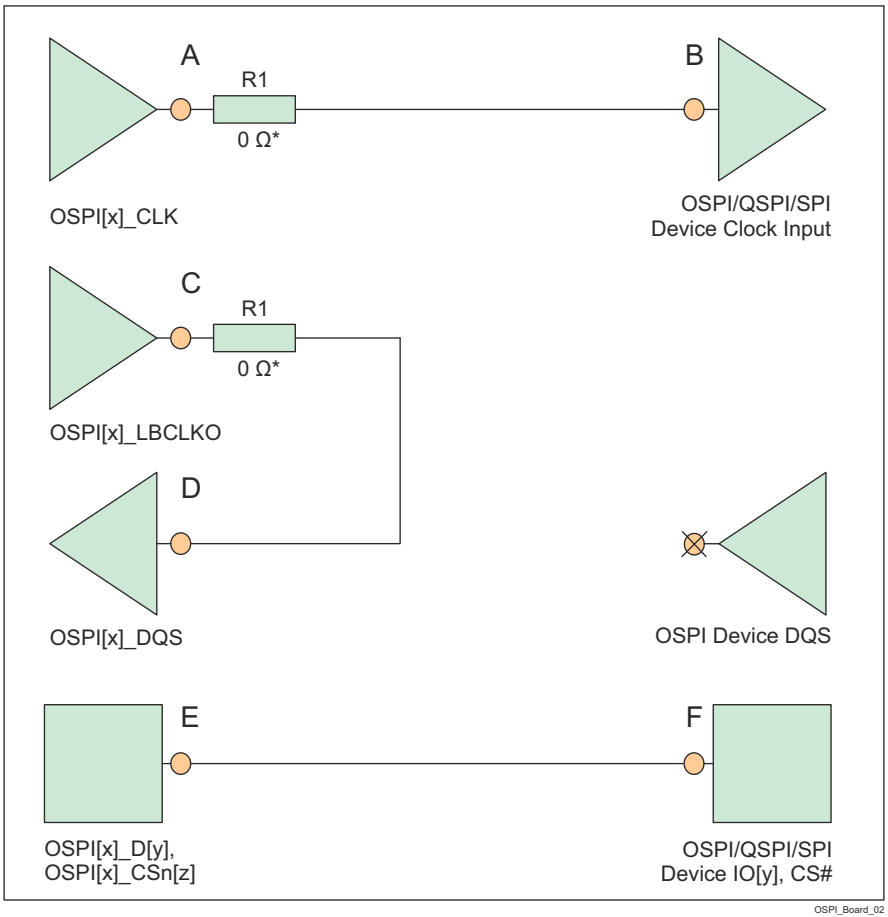
図 9-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

9.2.2.2 External Board Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]_LBCLKO output pin must be looped back to the OSPI[x]_DQS input pin
- The signal propagation delay of the OSPI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 9-2
- Propagation delays and matching:
  - (C to D) = 2 x ((A to B) ± 30 ps), see the exception note below.
  - (E to F, or F to E) = ((A to B) ± 60 ps)

注

The External Board Loopback hold time requirement (defined by parameter number O16 in 表 7-119, *OSPI0 Timing Requirements - PHY DDR Mode*) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OPSI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) can be reduced to provide additional hold time.

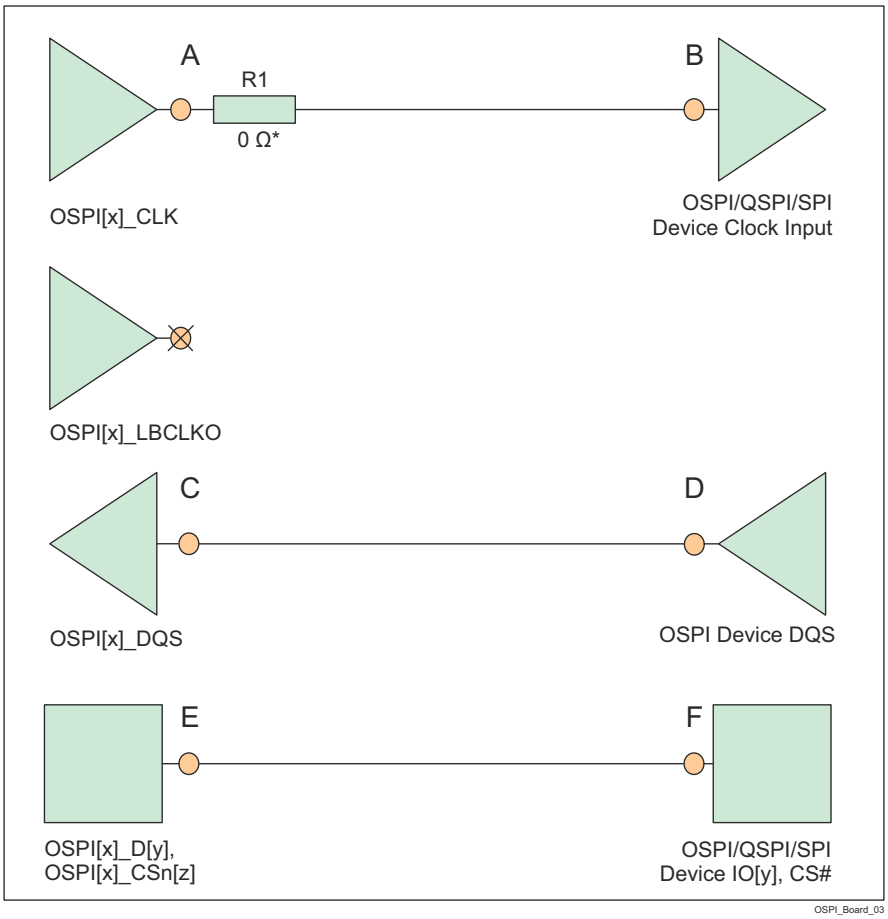


* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK and OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

図 9-2. OSPI Connectivity Schematic for External Board Loopback

9.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 9-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30 ps)
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

図 9-3. OSPI Connectivity Schematic for DQS

9.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the 図 9-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5 V should be less than 100 nA.

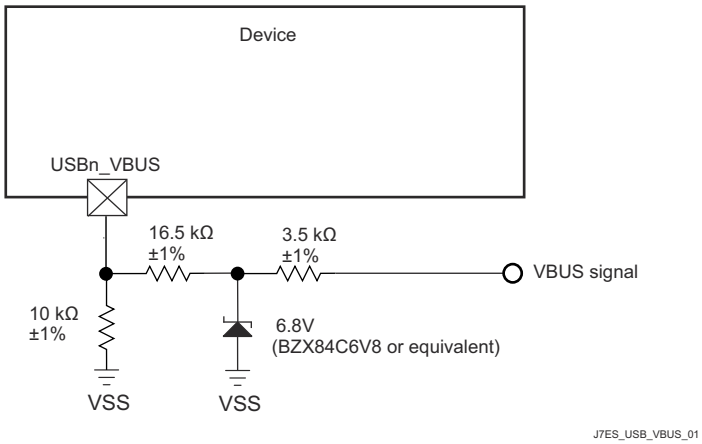


図 9-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in 図 9-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

9.2.4 System Power Supply Monitor Design Guidelines

The VMON_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON_VSYS pin via and external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When designing the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_VSYS input threshold which has a nominal value of 0.45 V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_VSYS input leakage current can be in the range of 10 nA to 2.5 µA when applying 0.45 V.

注

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

図 9-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_VSYS pin is 2.5 µA. When implementing a resistor divider where R1 = 4.81 KΩ and R2 = 40.2 KΩ, the result is a maximum trigger threshold of 4.517 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013 V to 4.517 V. Approximately 250 mV of this range is introduced by VMON_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100 mV of this range is introduced by loading error when VMON_VSYS input leakage current is 2.5 µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above can be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in 図 9-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

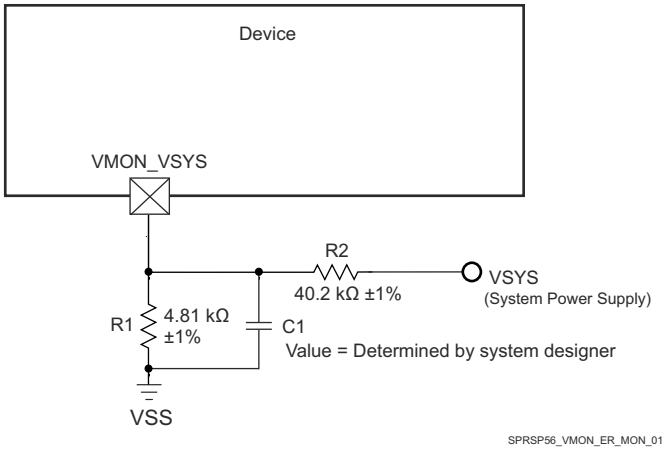


図 9-5. System Supply Monitor Voltage Divider Circuit

VMON_1P8_SOC pin provides a way to monitor external 1.8 V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON_3P3_SOC pin provides a way to monitor external 3.3 V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

9.2.5 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

9.2.6 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

10 Device and Documentation Support

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM6254ATCGGAALW). Texas Instruments recommends two of three possible prefix designators for related support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null (BLANK) Production version of the silicon die that is fully qualified and meets final electrical specifications.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM62x devices in the ALW or AMC package types, see the Package Option Addendum at the end of this document, the TI website (ti.com), or contact your TI sales representative.

10.1.1 Standard Package Symbolization

注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

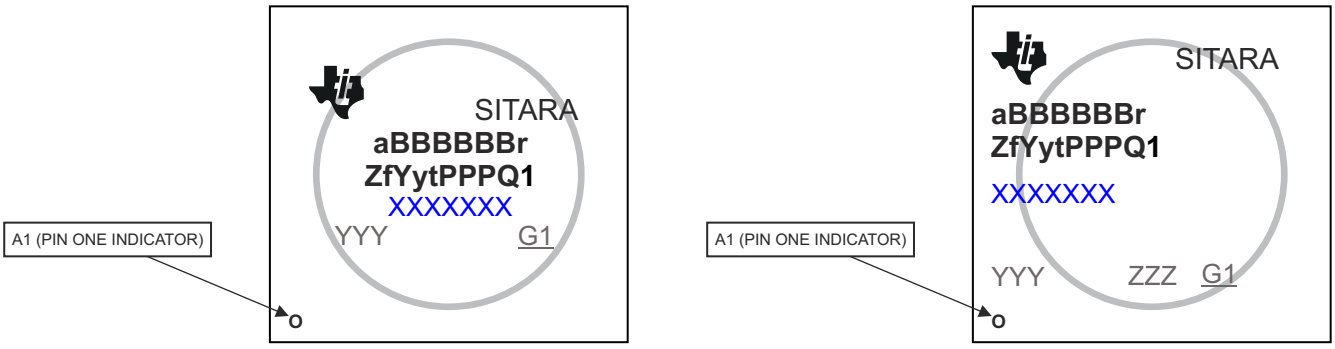


図 10-1. Printed Device Reference

10.1.2 Device Naming Convention

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK(1)	Production
BBBBBB	Base production part number	AM6254	See 表 5-1, Device Comparison
		AM6252	
		AM6251	
		AM6234	
		AM6232	
		AM6231	
		AM6204	
		AM6202	
		AM6201	
r	Device revision	A	SR1.0
Z	Device Speed Grade	G	See 表 7-1, Device Speed Grades
		K	
		S	
		T	
f	Features (see 表 5-1)	G	Base, no additional Features
		C	Base, plus PRU Subsystem (PRUSS) enabled
Y	Functional Safety	G	Non-Functional Safety
		F	Functional Safety
y	Security	G	Non-Secure
		Other	Secure
t	Temperature(2)	A	–40°C to 105°C - Extended Industrial (see セクション 7.5, *Recommended Operation Conditions*)
		H	0°C to 95°C - Commercial (see セクション 7.5, *Recommended Operation Conditions*)
		I	–40°C to 125°C - Automotive (see セクション 7.5, *Recommended Operation Conditions*)
PPP	Package Designator	ALW	FCCSP BGA (425-pin)
		AMC	FCBGA (441-pin)
Q1	Automotive Designator	Q1	Automotive Qualified (AEC - Q100)
		BLANK(1)	Standard
xxxxxxx			Lot Trace Code (LTC)
YYY			Production Code, For TI use only
ZZZ			Production Code, For TI use only
O			Pin one designator
G1			ECAT - Green package designator

(1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.
(2) Applies to device max junction temperature.

10.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM62x devices.

Technical Reference Manual

AM62x Sitara Processors Technical Reference Manual: Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM62x family of devices.

Errata

AM62x Sitara Processors Silicon Errata: Describes the known exceptions to the functional specifications for the device.

10.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.5 Trademarks

Sitara™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
MPCore™, Neon™, and CoreSight™ are trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Arm®, Cortex®, and TrustZone® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM6201ASGFHIAMCRQ1	ACTIVE	FCBGA	AMC	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	AM6201A SGFHIAMCQ1 131	Samples
AM6202ATGFHIAMCRQ1	ACTIVE	FCBGA	AMC	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	AM6202A TGFHIAMCQ1 131	Samples
AM6204ASGFHIAMCRQ1	ACTIVE	FCBGA	AMC	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	AM6204A SGFHIAMCQ1 131	Samples
AM6231AKGGHHALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	0 to 95	AM6231A KGGHHALW 131	Samples
AM6231ASGGGAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6231A SGGGAALW 131	Samples
AM6231ASGGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6231A SGGHAALW 131	Samples
AM6231ASGGHIALWR	PREVIEW	FCCSP	ALW	425	1000	TBD	Call TI	Call TI			
AM6231ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6231A TCGHAALW 131	Samples
AM6231ATGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6231ATGGHIALWR	PREVIEW	FCCSP	ALW	425	1000	TBD	Call TI	Call TI			
AM6232ASCGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6232ASGGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6232A SGGHAALW 131	Samples
AM6232ATCGGAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6232A TCGGAALW 131	Samples
AM6232ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6232A TCGHAALW	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										131	
AM6232ATGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6232A TGGHAALW 131	Samples
AM6232ATGGHIALWR	PREVIEW	FCCSP	ALW	425	1000	TBD	Call TI	Call TI			
AM6234ASCGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6234ASGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6234ATCGGAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6234A TCGGAALW 131	Samples
AM6234ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6234A TCGHAALW 131	Samples
AM6234ATGGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6234A TGGHAALW 131	Samples
AM6234ATGGHIALWR	PREVIEW	FCCSP	ALW	425	1000	TBD	Call TI	Call TI			
AM6251ASGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6251ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6251A TCGHAALW 131	Samples
AM6251ATGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6252ASGFHIAMCRQ1	ACTIVE	FCBGA	AMC	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	AM6252A SGFHIAMCQ1 131	Samples
AM6252ASGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	TBD	Call TI	Call TI	-40 to 105		Samples
AM6252ATCGGAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6252A TCGGAALW 131	Samples
AM6252ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6252A TCGHAALW 131	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM6252ATGGHAALWR	ACTIVE	FCCSP	ALW	425	1000	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6252A TGGHAALW 131	Samples
AM6254ASGGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6254A SGGHAALW 131	Samples
AM6254ATCGGAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6254A TCGGAALW 131	Samples
AM6254ATCGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6254A TCGHAALW 131	Samples
AM6254ATCGHIALWR	PREVIEW	FCCSP	ALW	425	1000	TBD	Call TI	Call TI			
AM6254ATGFHIAMCRQ1	ACTIVE	FCBGA	AMC	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 125	AM6254A TGFHIAMCQ1 131	Samples
AM6254ATGGHAALW	ACTIVE	FCCSP	ALW	425	119	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6254A TGGHAALW 131	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM625, AM625-Q1 :

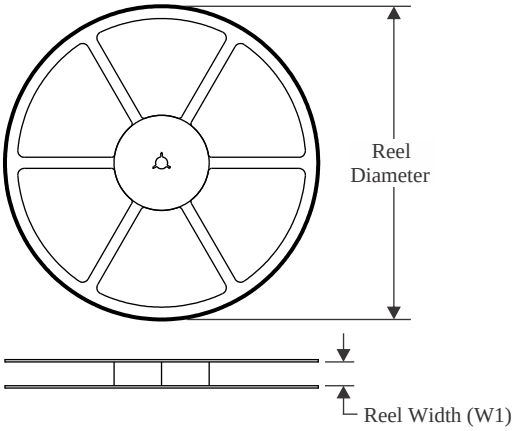
- Catalog : AM625
- Automotive : AM625-Q1

NOTE: Qualified Version Definitions:

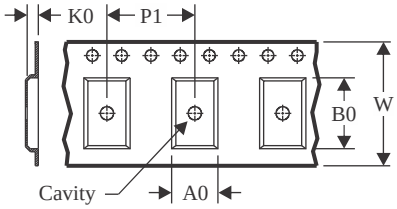
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

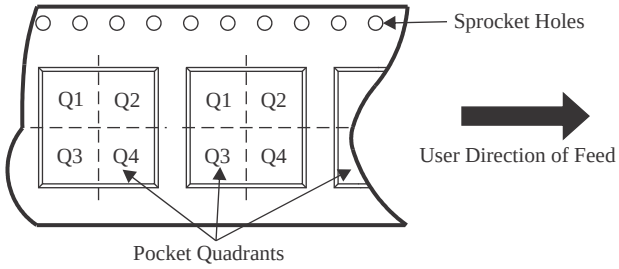


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

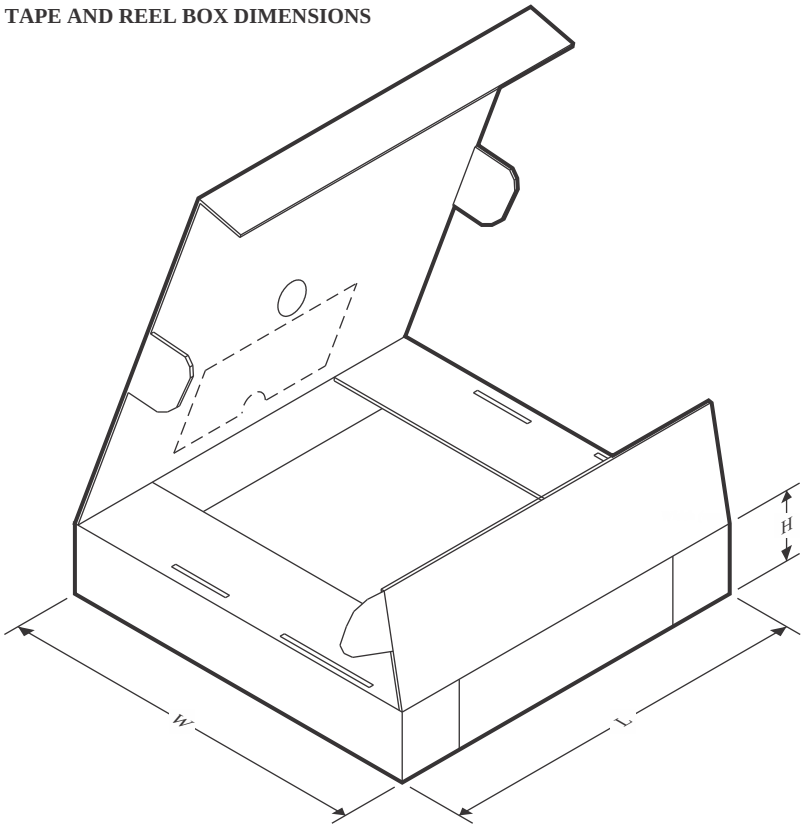
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM6201ASGFHIAMCRQ1	FCBGA	AMC	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6202ATGFHIAMCRQ1	FCBGA	AMC	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6204ASGFHIAMCRQ1	FCBGA	AMC	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6232ATGGHAALWR	FCCSP	ALW	425	1000	330.0	24.4	13.25	13.25	1.8	16.0	24.0	Q1
AM6252ASGFHIAMCRQ1	FCBGA	AMC	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6252ATGGHAALWR	FCCSP	ALW	425	1000	330.0	24.4	13.25	13.25	1.8	16.0	24.0	Q1
AM6254ATGFHIAMCRQ1	FCBGA	AMC	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1

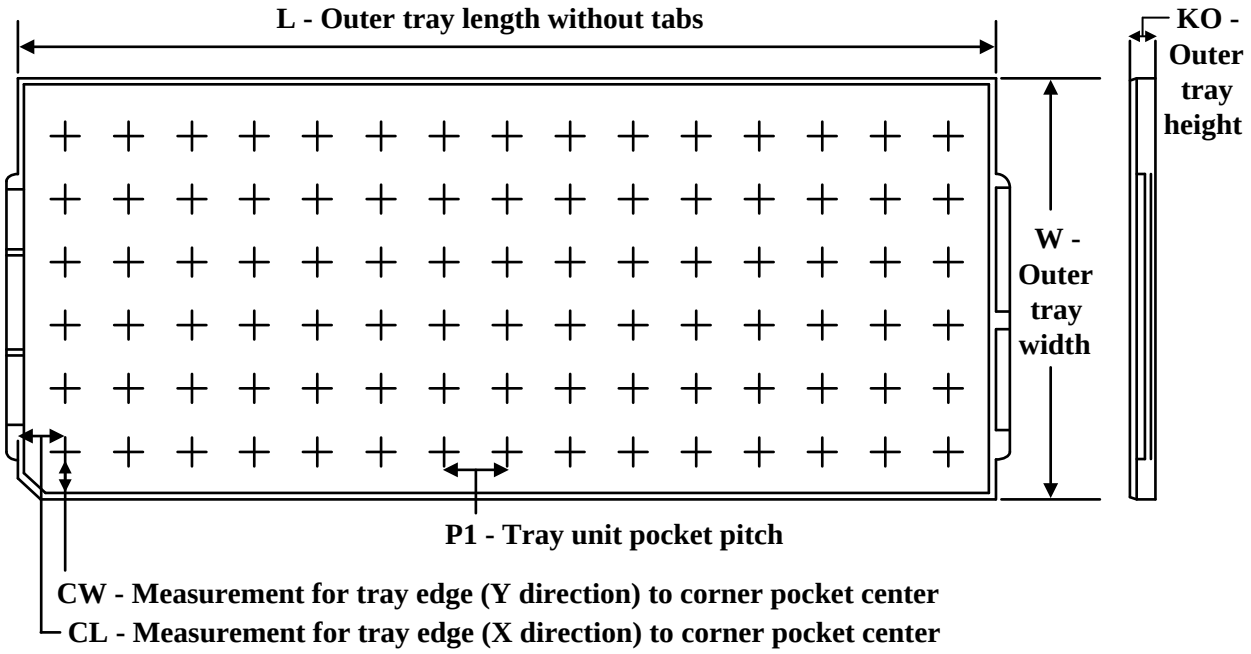
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM6201ASGFHIAMCRQ1	FCBGA	AMC	441	500	336.6	336.6	41.3
AM6202ATGFHIAMCRQ1	FCBGA	AMC	441	500	336.6	336.6	41.3
AM6204ASGFHIAMCRQ1	FCBGA	AMC	441	500	336.6	336.6	41.3
AM6232ATGGHAALWR	FCCSP	ALW	425	1000	336.6	336.6	41.3
AM6252ASGFHIAMCRQ1	FCBGA	AMC	441	500	336.6	336.6	41.3
AM6252ATGGHAALWR	FCCSP	ALW	425	1000	336.6	336.6	41.3
AM6254ATGFHIAMCRQ1	FCBGA	AMC	441	500	336.6	336.6	41.3

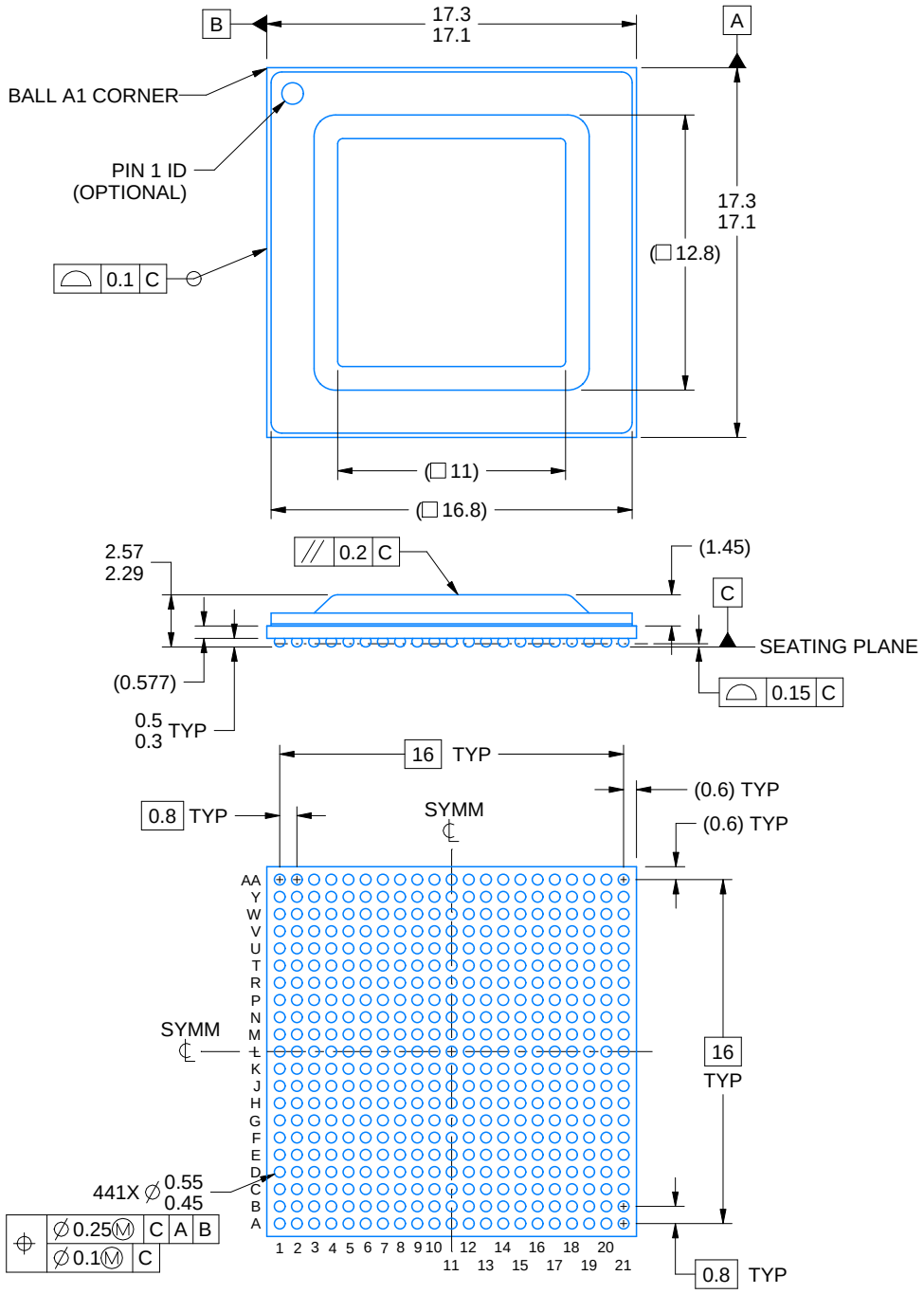
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

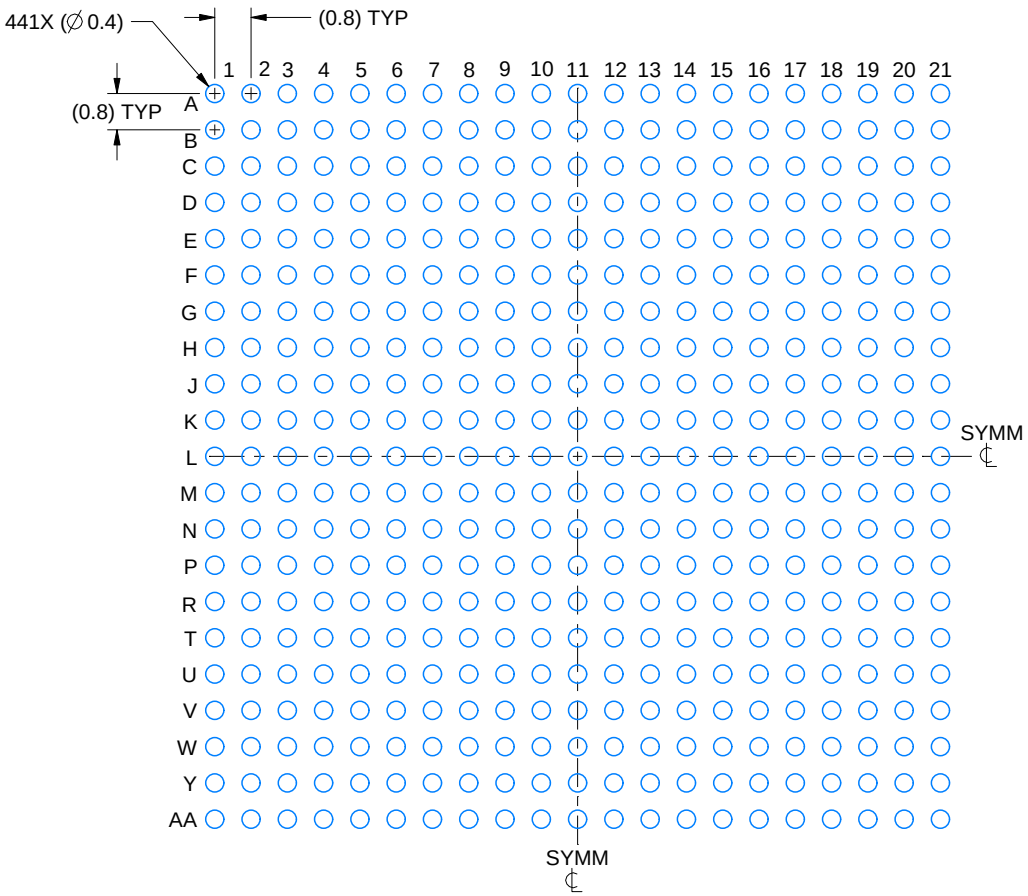
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AM6231AKGGHHALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6231ASGGGAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6231ASGGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6231ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6232ASGGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6232ATCGGAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6232ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6234ATCGGAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6234ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6234ATGGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6251ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6252ATCGGAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6252ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6254ASGGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6254ATCGGAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6254ATCGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9
AM6254ATGGHAALW	ALW	FCCSP	425	119	07x17	150	315	135.9	7620	18.1	12.7	12.9



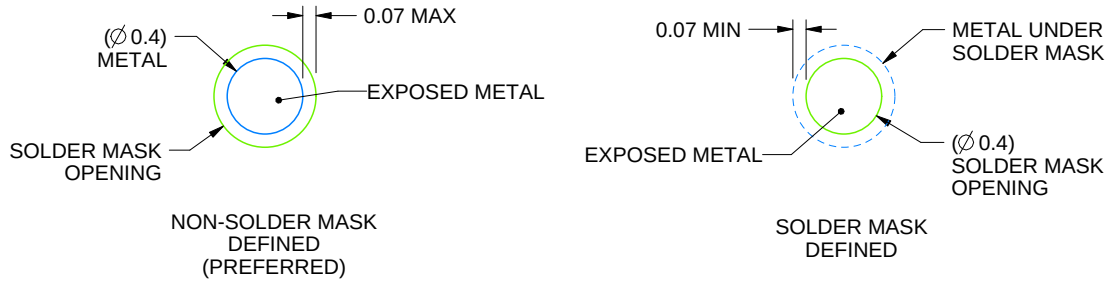
4228316/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X

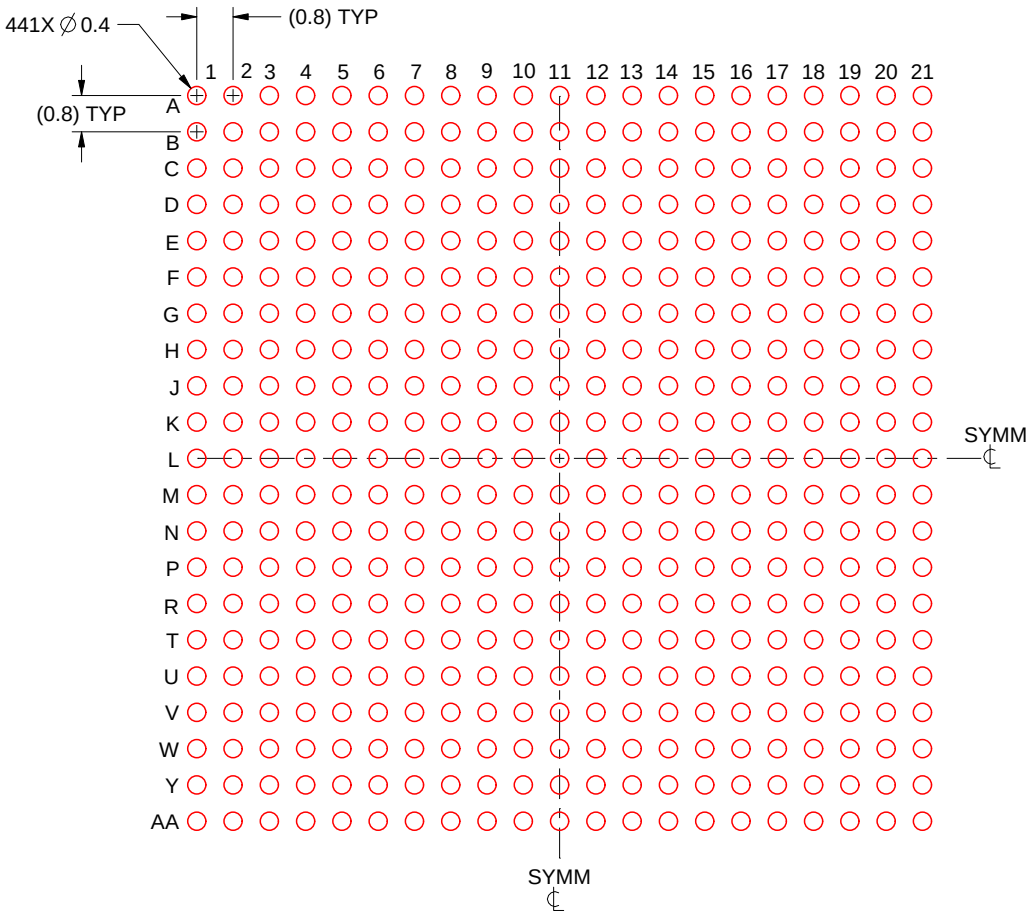


SOLDER MASK DETAILS
NOT TO SCALE

4228316/A 12/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4228316/A 12/2021

NOTES: (continued)

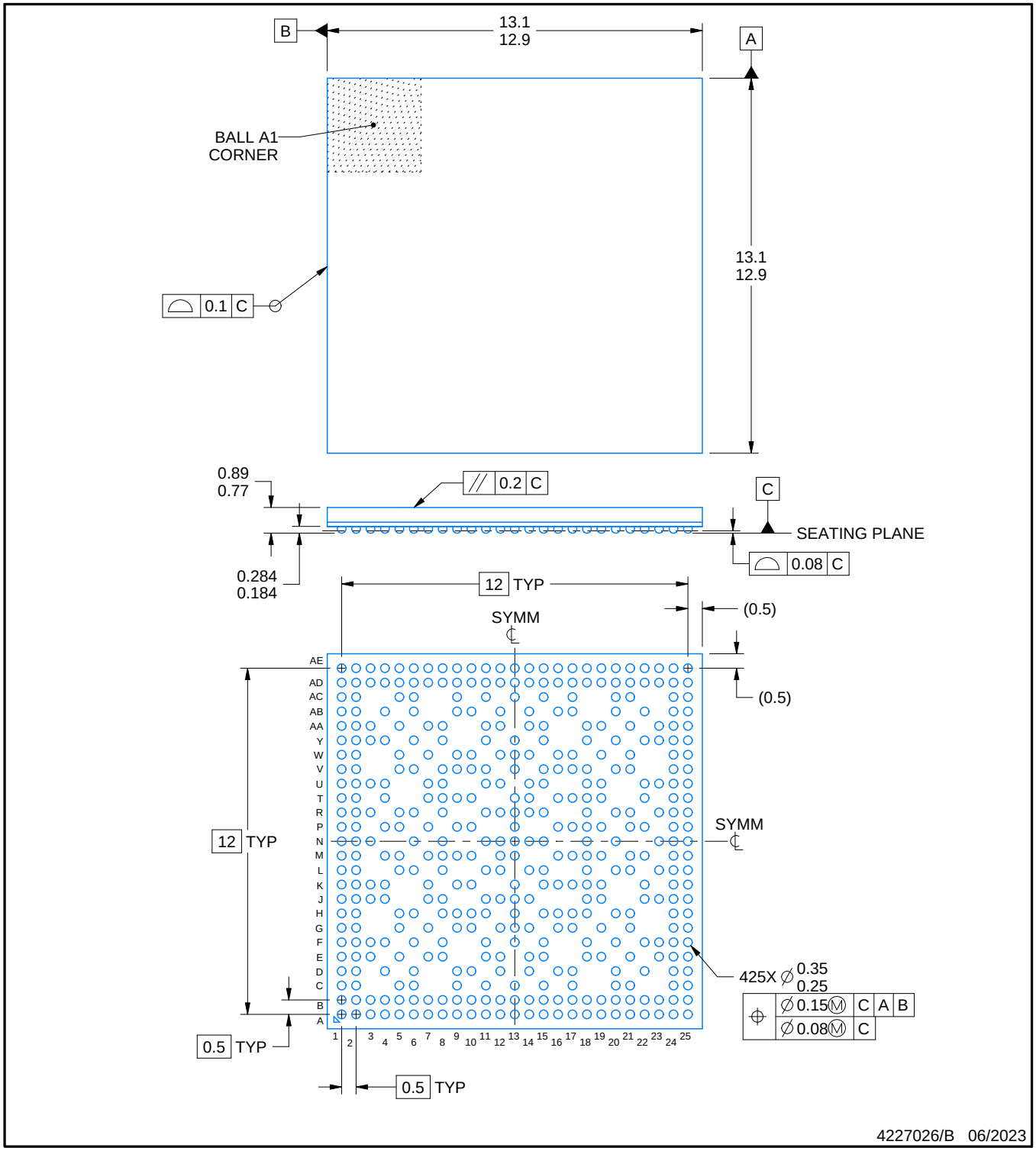
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ALW0425A

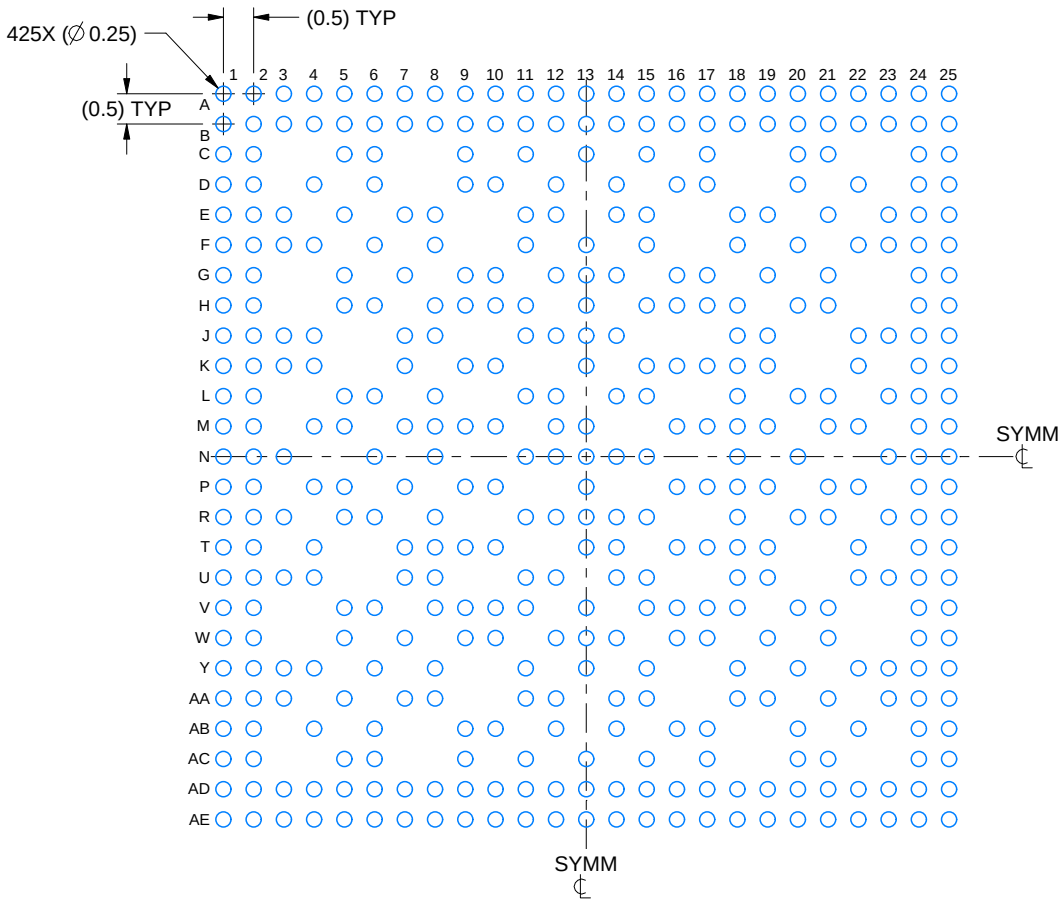
FCCSP - 0.89 mm max height

PLASTIC BALL GRID ARRAY

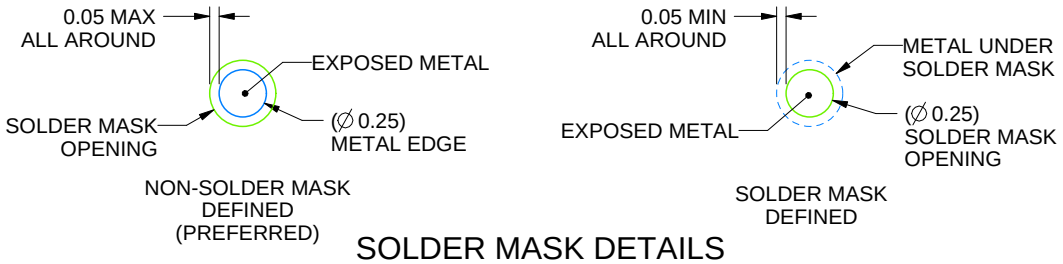


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4227026/B 06/2023

NOTES: (continued)

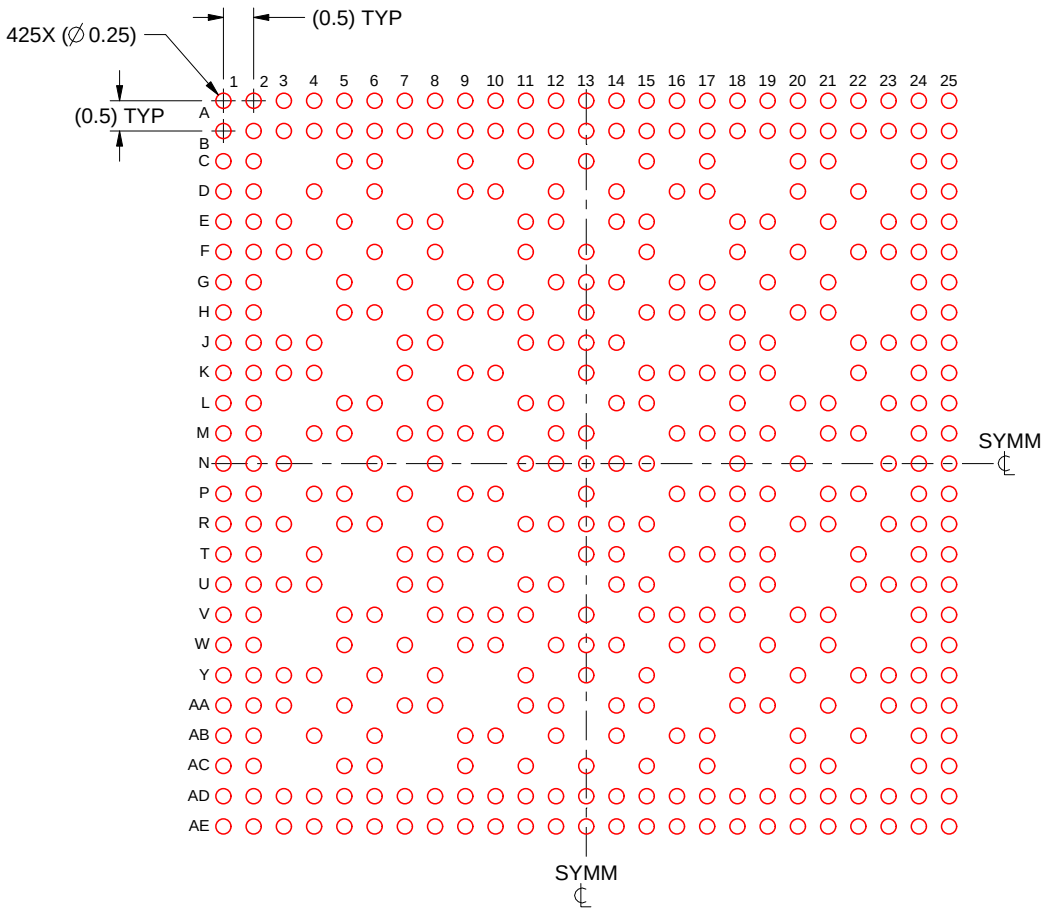
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ALW0425A

FCCSP - 0.89 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4227026/B 06/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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