AWR2544 ADAS アプリケーション向け、ローンチ オン パッケージ (LOP) 導波管インターフェイス搭載、シングルチップ 76～81GHz FMCW レーダー SoC

1 特長

- FMCW トランシーバ
  - PLL、トランスミッタ、レシーバ、ベースバンド、ADC を内蔵
  - 76～81GHz 帯で使用可能帯域幅 4GHz 超
  - アンテナに対する**ローンチ オン パッケージ (LOP) インターフェイス**を備えた、4 個の受信チャネルと 4 個の送信チャネル
  - 送信用位相シフタ
  - フラクショナル PLL を使用した超高精度のチャープ エンジン
  - TX 出力
    - +12.5dBm
  - RX ノイズ指数
    - +12.5 dB
  - 位相ノイズ (1MHz)
    - –96dBc/Hz (76GHz～77GHz)
    - –95dBc/Hz (76GHz～81GHz)
- 較正および自己テストを内蔵
  - 内蔵ファームウェア (ROM)
  - プロセスおよび温度の自己較正システム
- 処理部品
  - 300MHz で動作する Arm® Cortex-R5F® コア (ロック ステップ動作をサポート)
  - FFT、干渉軽減、メモリ圧縮などの動作向け、テキサス・インスツルメンツのレーダー ハードウェア アクセラレータ (HWA1.5)
  - データ移動用の複数の EDMA インスタンス
- ホスト インターフェイス
  - 10/100/1000Mbps RGMII/RMII/MII イーサネット
  - イーサネット PHY のクロック用 25MHz クロック出力
- シリアル フラッシュ メモリ インターフェイスをサポート (QSPI フラッシュ メモリからのユーザー アプリケーションのロード)
- ユーザー アプリケーションで利用可能なその他のインターフェイス
  - 最大 4 つの ADC チャネル
  - 1 SPI
  - 2 つの UART
  - I^2C
  - GPIO
  - 3 つの EPWM
  - 未加工 ADC データおよびデバッグ計測機器向け 2 レーン LVDS インターフェイス
- オンチップ RAM
  - 2MB
  - MCU、共有 L3 でメモリ空間を分割
- デバイスのセキュリティ (一部の型番のみ)
  - プログラム可能な組み込みハードウェア セキュリティ モジュール (HSM)
  - セキュア認証および暗号化ブートのサポート
  - 顧客がプログラム可能なルート キー、対称キー (256 ビット)、非対称キー (RSA-4K または ECC-512 まで)、キー失効機能付き
  - 暗号化ハードウェア アクセラレータ:ECC 付き PKA、AES (最大 256 ビット)、SHA (最大 512 ビット)、TRNG/DRBG
- 機能安全準拠製品向け
  - 機能安全アプリケーション向けに開発
  - ISO26262 機能安全システムの設計に役立つ資料を利用可能
  - ASIL B までを対象とするハードウェア インテグリティ
- AEC-Q100 認定済み
- 高度な機能
  - 外部プロセッサの関与を必要としない自己監視機能を内蔵
  - 干渉検出機能を内蔵
- パワー マネージメント
  - オンダイ LDO ネットワークにより PSRR の向上を実現
  - LVCMOS IO は 3.3V、1.8V のデュアル電圧に対応
- クロック ソース
  - 40MHz または 50MHz の水晶振動子と内部発振器
  - 40MHz または 50MHz の外部発振器 / 駆動クロックをサポート
- パワー マネージメント
  - 推奨される LP8772-Q1 パワー マネージメント IC (PMIC)
    - デバイスの電源要件を満たすように特別に設計されたコンパニオン PMIC
    - さまざまな使用事例をサポートするためのフレキシブルなマッピングと工場出荷時にプログラムされた構成
- コストを抑えたハードウェア設計
  - 0.65mm ピッチ、12.4mm × 12mm の FCCSP パッケージ
  - 小型サイズ
- 車載用動作温度範囲に対応

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

– 動作時の接合部温度範囲:-40℃ ～ +140℃

2 アプリケーション

- 車線変更支援
- 死角検出
- 自動緊急ブレーキ
- アダプティブ クルーズ コントロール
- クロストラフィック アラート
- 衛星

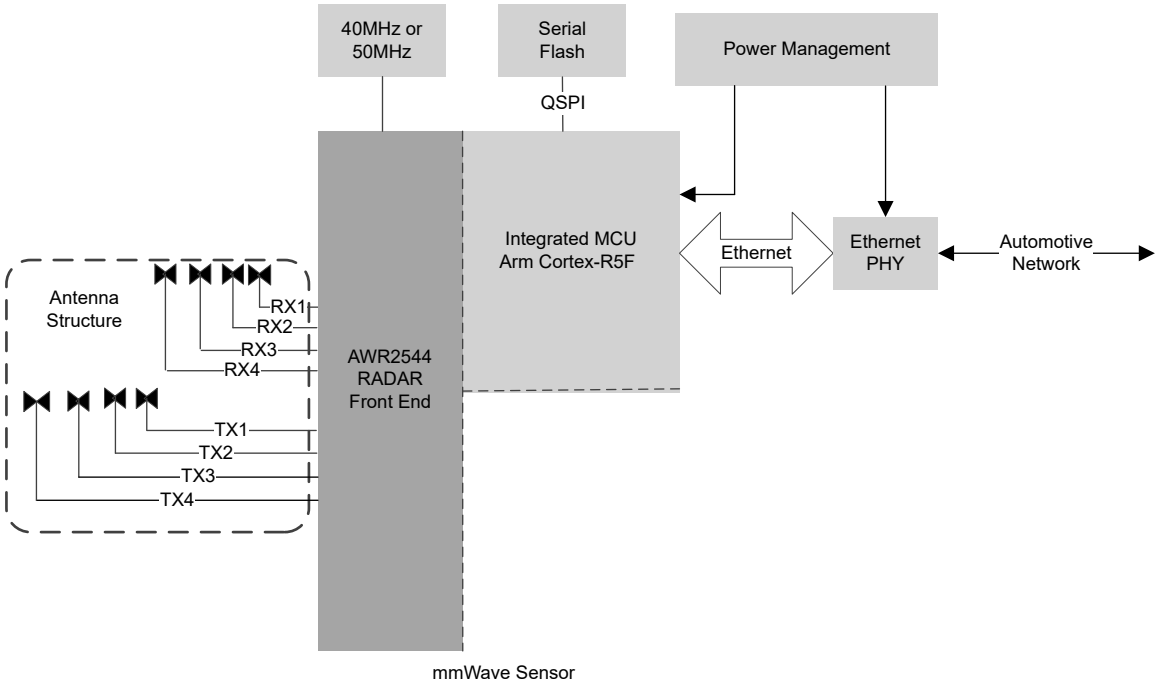

図 2-1. 車載アプリケーション用の自律レーダー センサ

3 概要

AWR2544 は、FMCW トランシーバで構成されるシングルチップのミリ波センサです。このデバイスは 76～81GHz (EHF) 帯域で動作可能で、レーダー データ処理部品と、車内ネットワーク用の豊富な周辺機器セットを備えています。AWR2544 は、パッケージにアンテナを容易に直接接続できるようにする、追加のローンチ オン パッケージ (LOP) アンテナ機能をお客様に提供します。AWR2544 は、テキサス・インスツルメンツの低消費電力 45nm RFCMOS プロセスで製造され、小さいフォーム ファクタと最小限の部品点数で、かつてないレベルの統合を実現しています。AWR2544 は、低消費電力で自己監視機能を備えた、超高精度の車載用レーダー システム向けに設計されています。

テキサス・インスツルメンツの低消費電力 45nm RFCMOS プロセスにより、PLL、VCO、ミキサ、ベースバンド ADC を内蔵し、4 個の TX、4 個の RX を備えたシステムのモノリシック実装が可能になります。このデバイスは、レーダー フロントエンドの構成、制御、較正を行う、無線プロセッサ サブシステムも備えています。メイン サブシステム (MSS) 内には、ユーザーによるプログラムが可能な Arm Cortex-R5F プロセッサが実装されており、カスタム制御アプリケーションや車載用インターフェイス アプリケーションに使用できます。ハードウェア アクセラレータ ブロック (HWA 1.5) は、FFT、スケーリング、圧縮などの一般的なレーダー処理を負荷分担して、MSS を補完します。これにより、外部プロセッサの MIPS が軽減され、カスタム アプリケーションや高度な後処理アルゴリズムの実装のためにリソースが使えるようになります。

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ハードウェア セキュリティ モジュール (HSM) もこのデバイスに用意されています (セキュア部品バリアントのみで使用可能)。HSM は、プログラム可能な Arm Cortex-M4 コアと、デバイス内でセキュアな動作ゾーンを実現するために必要なインフラで構成されます。

プログラミング モデルを変更するだけで、さまざまなセンサ (短距離、中距離、長距離) を実装でき、マルチモード センサの実装においては動的再構成にも対応します。

テキサス・インスツルメンツは AWR2544 を特にサテライト アーキテクチャ向けに設計しています。サテライト アーキテクチャは、センサ フュージョン アルゴリズムと集中型 ECU のより大きな計算能力を通じて付加価値を高めます。簡素化されたサテライト センサとソフトウェアによる差別化は、システムの複雑さを緩和し、価値を創造する新しい方法を実現するのに役立ちます。

サテライト レーダーを使用すると、自動車メーカーは無線ソフトウェア アップデートを使用してシステム性能の向上とセキュリティの強化を図ることができます。これらの性能、スケーラビリティ、簡素化といった複数の利点により、自動車業界でサテライト アーキテクチャが注目されるようになっています。

また、AWR2544 は、テキサス・インスツルメンツのハードウェアおよびソフトウェアのリファレンス デザイン、ソフトウェア ドライバ、構成例、API ガイド、ユーザー マニュアルを含む完全なプラットフォームとして提供しています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)	セキュリティ
AWR2544BGAMQQ1	AMQ (FCCSP、248)	12.4 mm × 12mm	全般
AWR2544BGAMQRQ1	AMQ (FCCSP、248)	12.4 mm × 12mm	全般
AWR2544BSAMQQ1	AMQ (FCCSP、248)	12.4 mm × 12mm	セキュアな機能
AWR2544BSAMQRQ1	AMQ (FCCSP、248)	12.4 mm × 12mm	セキュアな機能

(1) 詳細については、セクション 13 を参照してください。

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3.1 機能ブロック図

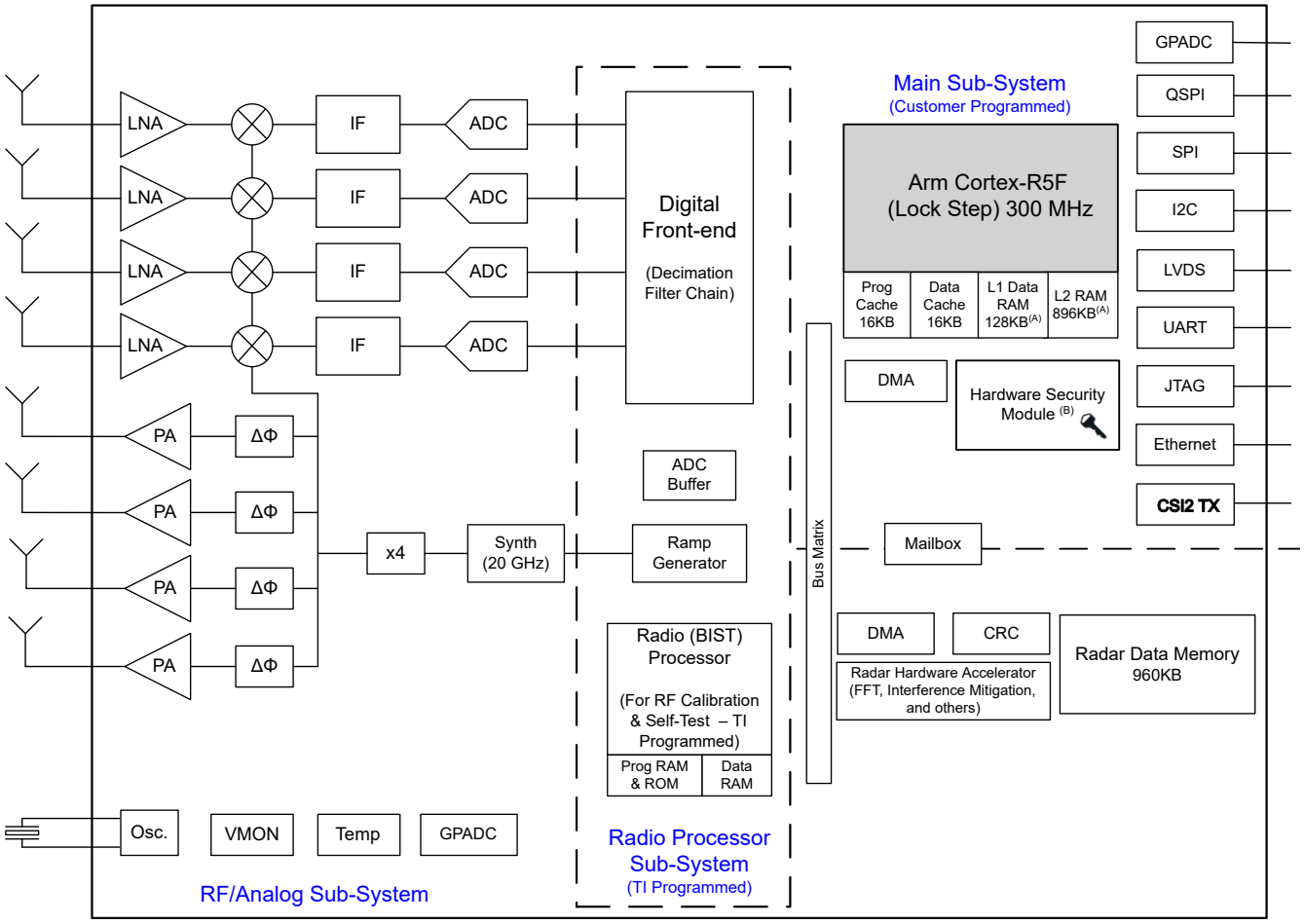

図 3-1. 機能ブロック図

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4 Device Comparison

表 4-1. Device Features Comparison

FUNCTION		AWR2544	AWR2944	AWR2243	AWR1843
Launch on Package (LOP) Antenna		Yes	—	—	—
Number of receivers		4	4	4	4
Number of transmitters		4	4	3(1)	3(1)
On-chip memory		2MB	4MB	—	2MB
Max I/F (Intermediate Frequency) (MHz)		20	15 (2)	20	10
Max real/complex 2x sampling rate (Msps)		45(2)	37.5	45	25
Max complex 1x sampling rate (Msps)		—(2)	—	22.5	12.5
Safety and Security (3)					
Hardware Security Module (HSM) (6)		Yes	Yes	—	—
Security Accelerators (6)		Yes	Yes	—	Yes
AEC-Q100 Qualified		Yes	Yes	Yes	Yes
Processor					
DSP (C6xx)		—	Yes	—	Yes
MCU (RxF)		Yes(4)	Yes(5)	—	Yes
Hardware accelerator		Yes(5)	Yes(6)	—	Yes
Peripherals					
Serial Peripheral Interface (SPI) ports		1	2	1	2
Quad Serial Peripheral Interface (QSPI)		1	Yes	—	Yes
LVDS/Debug		Yes	Yes	Yes	Yes
Aurora LVDS		—	Yes	—	—
Ethernet Interface		Yes	Yes	—	—
Inter-Integrated Circuit (I^2C) interface		1	1	1	1
Controller Area Network (DCAN) interface		—	—	—	Yes
CAN FD		—	2	—	1
Trace		Yes	Yes	—	Yes
EPWM		Yes	Yes	—	Yes
DMM Interface		—	Yes	—	Yes
GPADC		Yes	Yes(7)	Yes	Yes
CSI2 TX		Yes	—	Yes	—
CSI2 RX		—	Yes	—	—
Cascade (20-GHz sync)		—	—	Yes	—
JTAG		Yes	Yes	—	Yes
Per chirp configurable Tx phase shifter		Yes	Yes	Yes	Yes
Product status(7)	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	AI	PD	PD	PD

(1) 3 Tx Simultaneous operation in AWR1843 and AWR2243 is supported only with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. Please refer to the respective datasheets for more information.
(2) AWR2544 supports a real only receiver.
(3) Developed for Functional Safety applications, the AWR2544 device is targeted to support hardware integrity up to ASIL-B. For other devices, refer to the respective Datasheets.
(4) In AWR2544, Main-Subsytem Processing core is changed from ARM CR4F in AWR1843 to ARM CR5F.
(5) The hardware accelerator in AWR2544 is upgraded to HWA1.5 with additional features as compared to AWR1843.
(6) Only applicable for AWR2544 Secure Part Variant

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(7) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of allparameters.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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5 Related Products

For information about other devices in this family of products or related products see the links that follow.

mmWave Sensors	TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.
Automotive mmWave Sensors	TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.

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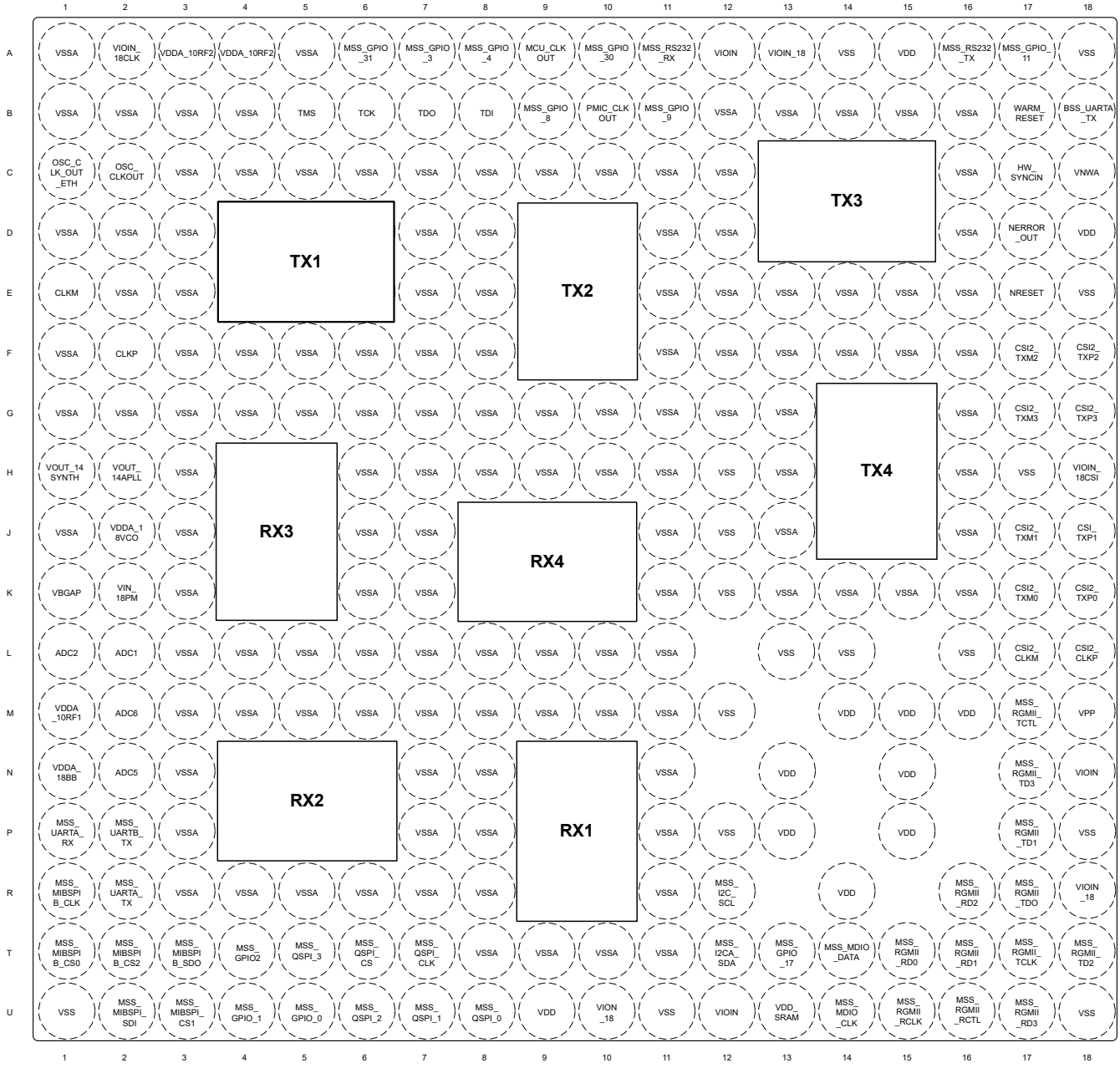
6 Pin Configurations and Functions

6.1 Pin Diagram

Pin Diagrams

Figure below show the pin locations for the 12.4mm x 12 mm FCCSP package. Following four figures show same pins, but split into four quadrants.



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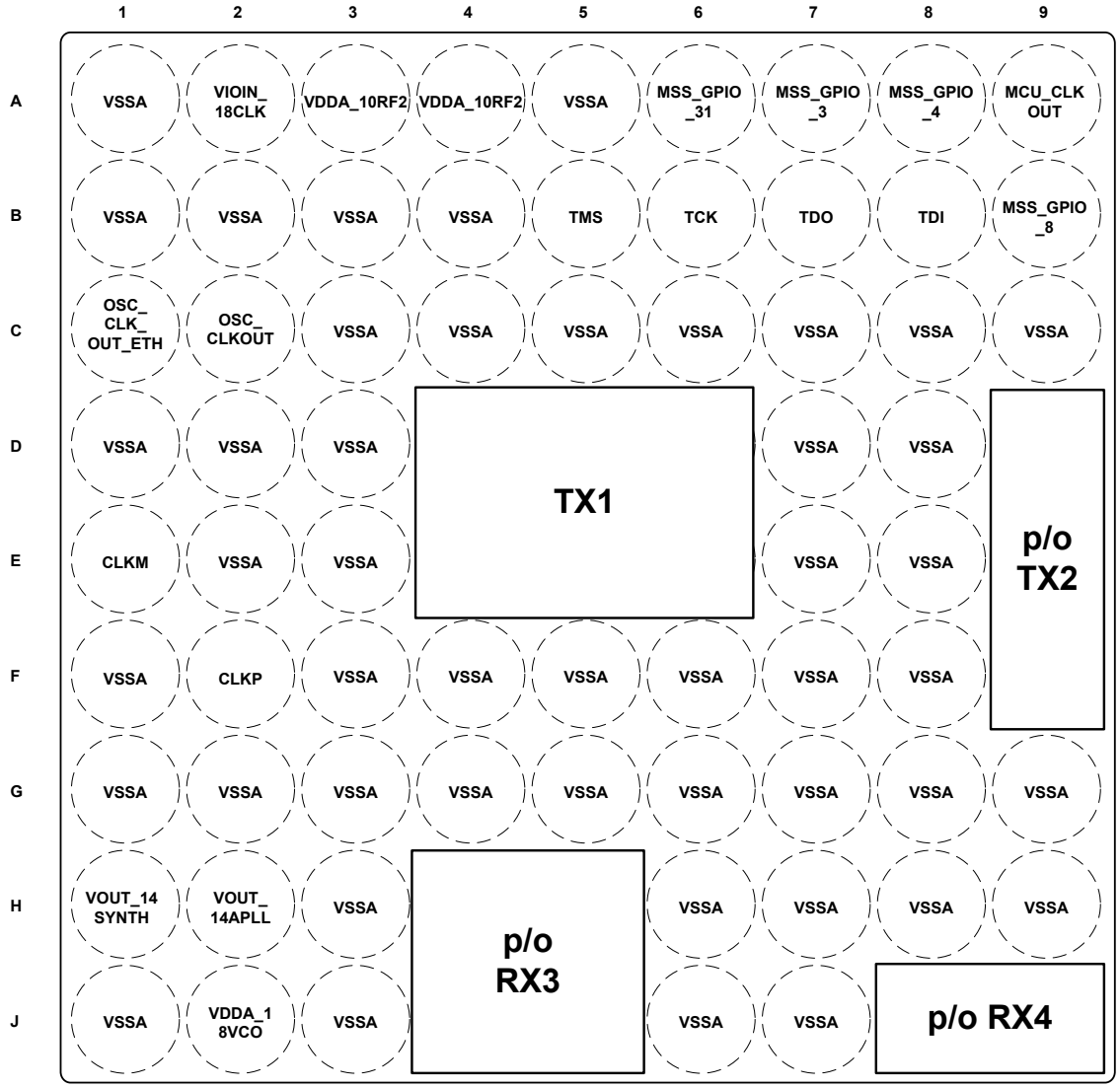

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1	2
3	4

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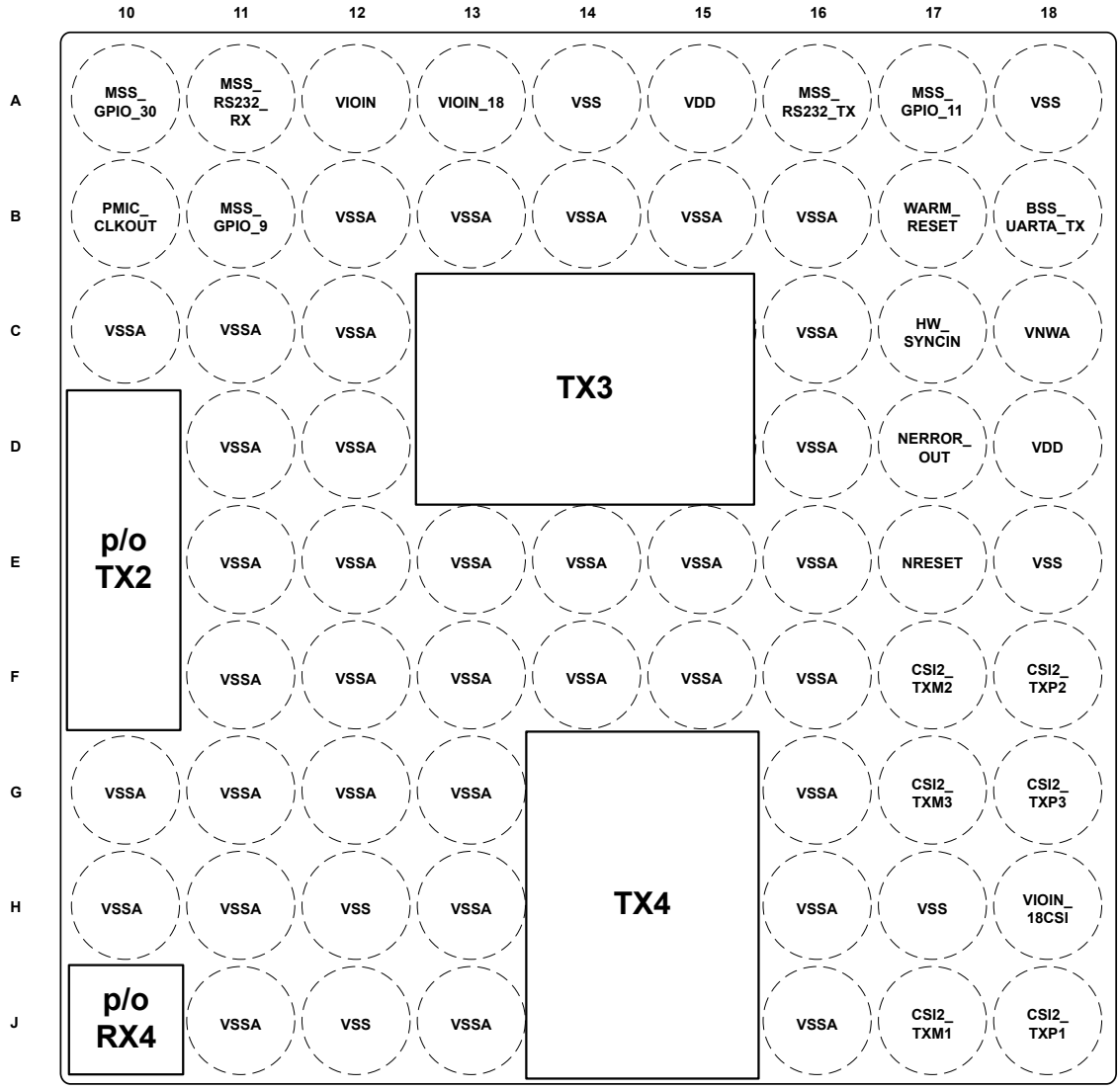
10 11 12 13 14 15 16 17 18
A
B
C
D
E
F
G
H
J
MSS_ GPIO_30
MSS_ RS232_ RX
VIOIN
VIOIN_18
VSS
VDD
MSS_ RS232_TX
MSS_ GPIO_11
VSS
PMIC_ CLKOUT
MSS_ GPIO_9
VSSA
WARM_ RESET
BSS_ UARTA_TX
HW_ SYNCIN
VNWA
TX3
NERROR_ OUT
p/o TX2
NRESET
CSI2_ TXM2
CSI2_ TXP2
CSI2_ TXM3
CSI2_ TXP3
TX4
VIOIN_ 18CSI
p/o RX4
CSI2_ TXM1
CSI2_ TXP1
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1
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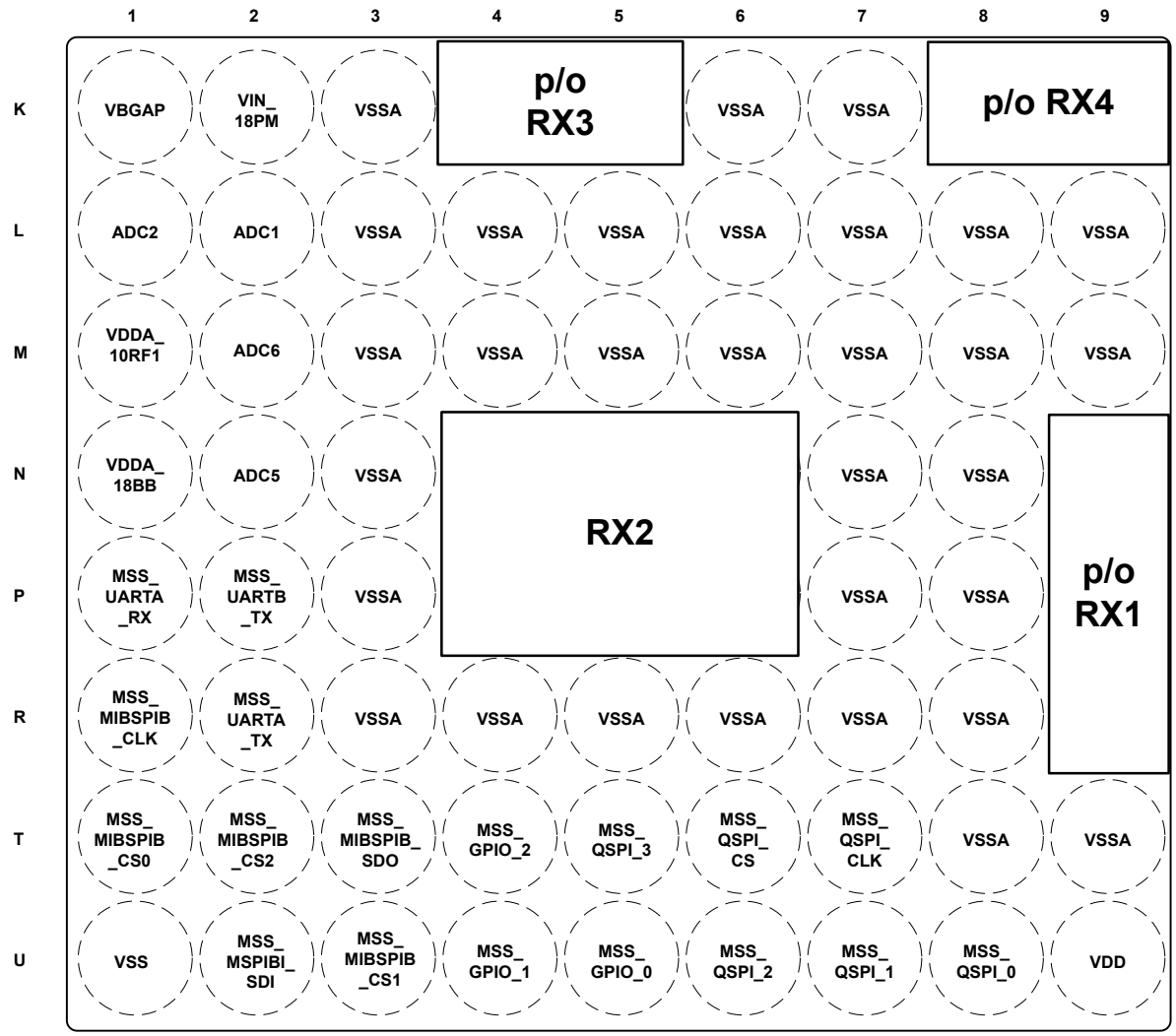

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3	4

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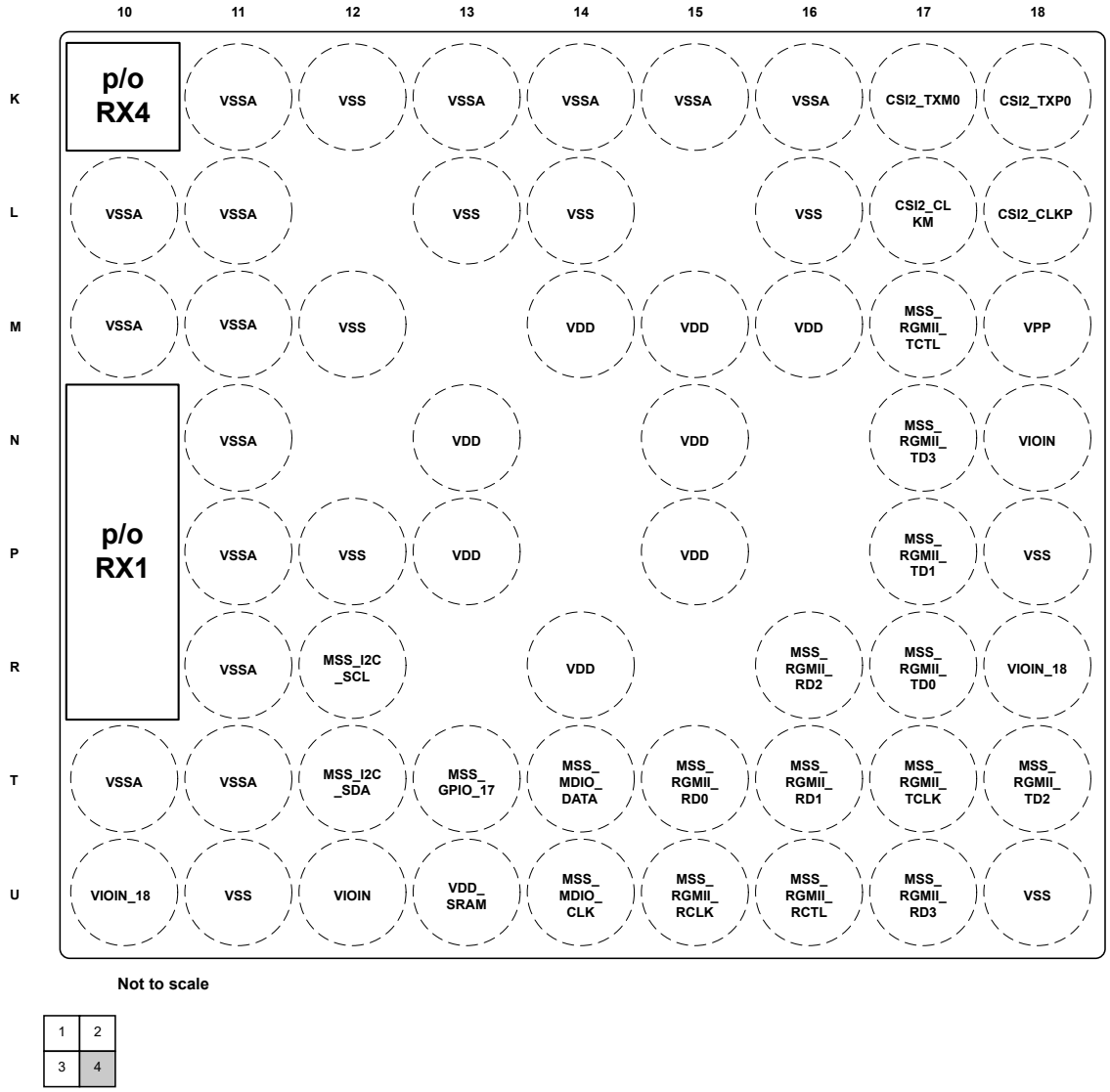

図 6-1. Pin Diagram

6.2 Pin Attributes

表 6-1. Pin Attributes (AMQ / FCCSP Package)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
U3	MSS_MIBSPIB_CS1	MSS_GPIO_12	0	IO	OUTPUT DISABLED	PD
		MSS_MIBSPIA_HOSTIRQ	1	O		
		ADC_VALID	2	O		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		MSS_MIBSPIB_CS1	6	IO		
U5	MSS_GPIO_0	MSS_GPIO_13	0	IO	OUTPUT DISABLED	PD
		MSS_GPIO_0	1	IO		
		PMIC_CLKOUT	2	O		
		MSS_EPWM_TZ2	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		
		RSVD	7	I		
		RSVD	8	O		
		RSVD	9	O		
		MSS_EPWMA1	10	O		
		MSS_EPWMB0	11	O		
		RSVD	12	IO		
U4	MSS_GPIO_1	MSS_GPIO_16	0	IO	OUTPUT DISABLED	PD
		MSS_GPIO_1	1	IO		
		SYNC_OUT	2	O		
		MSS_EPWM_TZ1	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		
		BSS_UARTA_TX	7	O		
		READY_INT	8	O		
		LVDS_VALID	9	O		
		RSVD	10	O		
		RSVD	11	O		
		RSVD	12	IO		
		MSS_MIBSPIB_CS1	13	IO		
		RSVD	14	IO		
		MSS_EPWMA_SYNCI	15	I		
T3	MSS_MIBSPIB_SDO	MSS_GPIO_21	0	IO	OUTPUT DISABLED	PU

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		MSS_MIBSPIB_SDO	1	IO		
		MSS_I2CA_SDA	2	IO		
		MSS_EPWMA0	3	O		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	I		
		RSVD	7	IO		
U2	MSS_MIBSPIB_SDI	MSS_GPIO_22	0	IO	OUTPUT DISABLED	PU
		MSS_MIBSPIB_SDI	1	IO		
		MSS_I2CA_SCL	2	IO		
		MSS_EPWMB0	3	O		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		
		RSVD	7	IO		
R1	MSS_MIBSPIB_CLK	MSS_GPIO_5	0	IO	OUTPUT DISABLED	PU
		MSS_MIBSPIB_CLK	1	IO		
		MSS_UARTA_RX	2	IO		
		MSS_EPWMC0	3	O		
		RSVD	4	O		
		RSVD	5	O		
		MSS_UARTB_TX	6	IO		
		BSS_UARTA_TX	7	O		
		RSVD	8	IO		
T1	MSS_MIBSPIB_CS0	MSS_GPIO_4	0	IO	OUTPUT DISABLED	PU
		MSS_MIBSPIB_CS0	1	IO		
		MSS_UARTA_TX	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		MSS_UARTB_TX	6	IO		
		BSS_UARTA_TX	7	O		
		RSVD	8	IO		
		RSVD	9	IO		
U8	MSS_QSPI_0	MSS_GPIO_8	0	IO	OUTPUT DISABLED	PD
		MSS_QSPI_0	1	IO		
		MSS_MIBSPIB_MISO	2	IO		
		RSVD	3	I		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	O		
		RSVD	7	O		
U7	MSS_QSPI_1	MSS_GPIO_9	0	IO	OUTPUT DISABLED	PD
		MSS_QSPI_1	1	I		
		MSS_MIBSPIB_MOSI	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	O		
		RSVD	7	O		
		MSS_MIBSPIB_CS2	8	IO		
U6	MSS_QSPI_2	MSS_GPIO_10	0	IO	OUTPUT DISABLED	PU
		MSS_QSPI_2	1	I		
		ADC_VALID	2	O		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	O		
		RSVD	7	O		
		RSVD	8	IO		
T5	MSS_QSPI_3	MSS_GPIO_11	0	IO	OUTPUT DISABLED	PU
		MSS_QSPI_3	1	I		
		ADC_VALID	2	O		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	O		
		RSVD	7	O		
		RSVD	8	IO		
T7	MSS_QSPI_CLK	MSS_GPIO_7	0	IO	OUTPUT DISABLED	PD
		MSS_QSPI_CLK	1	IO		
		MSS_MIBSPIB_CLK	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
T6	MSS_QSPI_CS	MSS_GPIO_6	0	IO	OUTPUT DISABLED	PU
		MSS_QSPI_CS	1	O		
		MSS_MIBSPIB_CS0	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
B17	WARM_RESET	WARM_RESET	0	IO	HI-Z (OPEN DRAIN)	
D17	NERROR_OUT	NERROR_OUT	0	IO	HI-Z (OPEN DRAIN)	
B6	TCK	MSS_GPIO_17	0	IO	OUTPUT DISABLED	PD
		TCK	1	I		
		MSS_UARTB_TX	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		BSS_UARTA_RX	6	I		
		RSVD	7	I		
		RSVD	8	IO		
B5	TMS	MSS_GPIO_18	0	IO	OUTPUT DISABLED	PU
		TMS	1	IO		
		BSS_UARTA_TX	2	O		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		
B8	TDI	MSS_GPIO_23	0	IO	OUTPUT DISABLED	PU
		TDI	1	I		
		MSS_UARTA_RX	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	I		
		RSVD	7	IO		
B7	TDO	MSS_GPIO_24	0	IO	OUTPUT DISABLED	HI-Z
		TDO	1	O		
		MSS_UARTA_TX	2	IO		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		MSS_UARTB_TX	6	IO		
		BSS_UARTA_TX	7	O		
		RSVD	8	O		
		RSVD	9	IO		
A9	MCU_CLKOUT	MSS_GPIO_25	0	IO	OUTPUT DISABLED	PD
		MCU_CLKOUT	1	O		
		TRACE_CLK	2	O		
		RSVD	3	I		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	I		
		FRAME_START	7	O		
		READY_INT	8	O		
		LVDS_VALID	9	O		
		BSS_UARTA_RX	10	I		
		RSVD	11	O		
		MSS_EPWMA0	12	O		
		RSVD	13	O		
		RSVD	14	IO		
		OBS_CLKOUT	15	O		
T4	MSS_GPIO_2	MSS_GPIO_26	0	IO	OUTPUT DISABLED	PD
		MSS_GPIO_2	1	IO		
		RSVD	2	O		
		RSVD	3	IO		
		RSVD	4	O		
		RSVD	5	O		
		RSVD	6	IO		
		MSS_UARTB_TX	7	IO		
		MSS_GPIO_2	8	IO		
		SYNC_OUT	9	O		
		PMIC_CLKOUT	10	O		
		CHIRP_START	11	O		
		CHIRP_END	12	O		
		FRAME_START	13	O		
		MSS_EPWM_TZ0	14	I		
		LVDS_VALID	15	O		
B10	PMIC_CLKOUT	MSS_GPIO_27	0	IO	OUTPUT DISABLED	HI-Z
		PMIC_CLKOUT	1	O		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		OBS_CLKOUT	2	O		
		TRACE_CTL	3	O		
		RSVD	4	O		
		RSVD	5	O		
		CHIRP_START	6	O		
		CHIRP_END	7	O		
		FRAME_START	8	O		
		READY_INT	9	O		
		LVDS_VALID	10	O		
		MSS_EPWMA1	11	O		
		MSS_EPWMB0	12	O		
		RSVD	13	IO		
C17	HW_SYNCIN	MSS_GPIO_28	0	IO	OUTPUT DISABLED	PD
		HW_SYNCIN	1	I		
		ADC_VALID	2	O		
		RSVD	3	IO		
		RSVD	4	O		
		RSVD	5	O		
		MSS_UARTB_RX	6	IO		
		RSVD	7	IO		
		RSVD	8	IO		
		SYNC_OUT	9	O		
T2	MSS_MIBSPIB_CS2	MSS_GPIO_29	0	IO	OUTPUT DISABLED	HI-Z
		SYNC_OUT	1	O		
		RCOSC_CLK	2	O		
		RSVD	3	IO		
		RSVD	4	O		
		RSVD	5	O		
		READY_INT	6	O		
		LVDS_VALID	7	O		
		RSVD	8	O		
		RSVD	9	IO		
		MSS_MIBSPIB_CS1	10	IO		
		MSS_MIBSPIB_CS2	11	IO		
		MSS_EPWMB0	12	O		
		MSS_EPWMB1	13	O		
A11	MSS_RS232_RX	MSS_GPIO_15	0	IO	OUTPUT DISABLED	PU
		MSS_RS232_RX	1	IO		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		MSS_UARTA_RX	2	IO		
		RSVD	4	O		
		RSVD	5	O		
		BSS_UARTA_TX	6	O		
		MSS_UARTB_RX	7	IO		
		RSVD	8	IO		
		MSS_I2CA_SCL	9	IO		
		MSS_EPWMB0	10	O		
		MSS_EPWMB1	11	O		
		MSS_EPWMC0	12	O		
A16	MSS_RS232_TX	MSS_GPIO_14	0	IO	OUTPUT DISABLED	PU
		MSS_RS232_TX	1	IO		
		RSVD	3	O		
		RSVD	4	O		
		MSS_UARTA_TX	5	IO		
		MSS_UARTB_TX	6	IO		
		BSS_UARTA_TX	7	O		
		READY_INT	8	O		
		LVDS_VALID	9	O		
		RSVD	10	IO		
		MSS_I2CA_SDA	11	IO		
		MSS_EPWMA0	12	O		
		MSS_EPWMA1	13	O		
		RSVD	14	IO		
		MSS_EPWMB0	15	O		
A6	MSS_GPIO_31	TRACE_DATA_0	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_31	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_UARTA_TX	4	IO		
		RSVD	5	I		
		MSS_GPIO_31	6	IO		
		RSVD	7	IO		
		RSVD	8	I		
		RSVD	9	I		
		MSS_I2CA_SDA	10	IO		
A10	MSS_GPIO_30	TRACE_DATA_1	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_30	1	IO		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		RSVD	2	IO		
		MSS_EPWMC_SYNCI	3	I		
		MSS_UARTA_RX	4	IO		
		RSVD	5	I		
		MSS_GPIO_0	6	IO		
		RSVD	7	IO		
		RSVD	8	I		
		RSVD	9	I		
		MSS_I2CA_SCL	10	IO		
B9	MSS_GPIO_8	TRACE_DATA_2	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_29	1	IO		
		RSVD	2	IO		
		MSS_EPWMB_SYNCI	3	I		
		RSVD	4	I		
		RSVD	5	I		
		MSS_GPIO_1	6	IO		
		MSS_GPIO_8	7	IO		
		MSS_EPWMA0	8	O		
		MSS_CPTS0_TS_GENF0	9	O		
		CHIRP_START	10	O		
		CHIRP_END	11	O		
		FRAME_START	12	O		
		READY_INT	13	O		
		ADC_VALID	14	O		
B11	MSS_GPIO_9	TRACE_DATA_3	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_28	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_EPWMC_SYNCO	4	O		
		RSVD	5	I		
		MSS_GPIO_2	6	IO		
		MSS_GPIO_9	7	IO		
		MSS_EPWMA1	8	O		
		MSS_CPTS0_TS_GENF1	9	O		
		CHIRP_START	10	O		
		CHIRP_END	11	O		
		FRAME_START	12	O		
		READY_INT	13	O		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		ADC_VALID	14	O		
A7	MSS_GPIO_3	TRACE_DATA_4	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_3	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_EPWMB_SYNCO	4	O		
		RSVD	5	I		
		MSS_GPIO_27	6	IO		
		MSS_EPWMB0	7	O		
		MSS_CPTS0_TS_GENF2	8	O		
		XREF_CLK1	9	I		
		MSS_CPTS0_TS_GENF1	10	O		
		MSS_CPTS0_HW1TSPUSH	11	I		
		ADC_VALID	12	O		
A8	MSS_GPIO_4	TRACE_DATA_5	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_4	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_EPWM_TZ2	4	I		
		MSS_UARTB_TX	5	IO		
		MSS_GPIO_26	6	IO		
		MSS_EPWMB1	7	O		
		MSS_CPTS0_TS_COMP	8	O		
		XREF_CLK0	9	I		
		MSS_CPTS0_HW2TSPUSH	10	I		
		READY_INT	11	O		
B18	BSS_UARTA_TX	TRACE_DATA_6	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_5	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_EPWM_TZ1	4	I		
		BSS_UARTA_TX	5	O		
		MSS_GPIO_25	6	IO		
		MSS_GPIO_10	7	IO		
		MSS_EPWMC0	8	O		
		MSS_CPTS0_TS_GENF2	9	O		
		MSS_CPTS0_HW1TSPUSH	10	I		
		CHIRP_START	11	O		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
A17	MSS_GPIO_11	TRACE_DATA_7	0	O	OUTPUT DISABLED	PD
		MSS_GPIO_6	1	IO		
		RSVD	2	IO		
		RSVD	3	I		
		MSS_EPWM_TZ0	4	I		
		RSVD	5	IO		
		MSS_GPIO_24	6	IO		
		MSS_GPIO_11	7	IO		
		MSS_EPWMC1	8	O		
		MSS_CPTS0_TS_COMP	9	O		
		MSS_CPTS0_TS_GENF0	10	O		
		MSS_CPTS0_HW2TSPUSH	11	I		
		CHIRP_END	12	O		
T13	MSS_GPIO_17	MSS_GPIO_17	0	IO	OUTPUT DISABLED	PD
		MSS_MII_COL	1	I		
		MSS_RMII_REFCLK	2	IO		
		RSVD	3	I		
		RSVD	4	IO		
		RSVD	5	I		
		MSS_EPWMA1	6	O		
T12	MSS_I2CA_SDA	MSS_GPIO_18	0	IO		HI-Z
		MSS_MII_CRS	1	I		
		MSS_RMII_CRS_DV	2	I		
		MSS_I2CA_SDA	3	IO		
		RSVD	4	IO		
		RSVD	5	I		
		MSS_EPWMB1	6	O		
R12	MSS_I2CA_SCL	MSS_GPIO_19	0	IO		HI-Z
		MSS_MII_RXER	1	I		
		MSS_RMII_RXER	2	I		
		MSS_I2CA_SCL	3	IO		
		RSVD	4	IO		
		RSVD	5	I		
		MSS_EPWMC1	6	O		
M17	MSS_RGMII_TCTL	MSS_GPIO_20	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXEN	1	O		
		MSS_RMII_TXEN	2	O		
		MSS_RGMII_TCTL	3	O		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		RSVD	4	IO		
		RSVD	5	I		
		MSS_EPWMA0	6	O		
U16	MSS_RGMII_RCTL	MSS_GPIO_21	0	IO		HI-Z
		MSS_MII_RXDV	1	I		
		RSVD	2	I		
		MSS_RGMII_RCTL	3	I		
		MSS_UARTB_RX	5	IO		
		MSS_EPWMB0	6	O		
N17	MSS_RGMII_TD3	MSS_GPIO_22	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXD3	1	O		
		RSVD	2	I		
		MSS_RGMII_TD3	3	O		
		RSVD	4	IO		
		MSS_UARTB_TX	5	IO		
		MSS_EPWMC0	6	O		
T18	MSS_RGMII_TD2	MSS_GPIO_23	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXD2	1	O		
		RSVD	2	I		
		MSS_RGMII_TD2	3	O		
P17	MSS_RGMII_TD1	MSS_GPIO_24	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXD1	1	O		
		MSS_RMII_TXD1	2	O		
		MSS_RGMII_TD1	3	O		
R17	MSS_RGMII_TD0	MSS_GPIO_25	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXD0	1	O		
		MSS_RMII_TXD0	2	O		
		MSS_RGMII_TD0	3	O		
T17	MSS_RGMII_TCLK	MSS_GPIO_26	0	IO	OUTPUT DISABLED	PD
		MSS_MII_TXCLK	1	I		
		RSVD	2	I		
		MSS_RGMII_TCLK	3	O		
U15	MSS_RGMII_RCLK	MSS_GPIO_27	0	IO	OUTPUT DISABLED	PD
		MSS_MII_RXCLK	1	I		
		RSVD	2	I		
		MSS_RGMII_RCLK	3	I		
U17	MSS_RGMII_RD3	MSS_GPIO_28	0	IO		HI-Z
		MSS_MII_RXD3	1	I		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		RSVD	2	I		
		MSS_RGMII_RD3	3	I		
R16	MSS_RGMII_RD2	MSS_GPIO_29	0	IO		HI-Z
		MSS_MII_RXD2	1	I		
		RSVD	2	I		
		MSS_RGMII_RD2	3	I		
T16	MSS_RGMII_RD1	MSS_GPIO_30	0	IO		HI-Z
		MSS_MII_RXD1	1	I		
		MSS_RMII_RXD1	2	I		
		MSS_RGMII_RD1	3	I		
T15	MSS_RGMII_RD0	MSS_GPIO_31	0	IO		HI-Z
		MSS_MII_RXD0	1	I		
		MSS_RMII_RXD0	2	I		
		MSS_RGMII_RD0	3	I		
T14	MSS_MDIO_DATA	MSS_GPIO_30	0	IO	OUTPUT DISABLED	PU
		MSS_MDIO_DATA	1	IO		
		RSVD	2	I		
		RSVD	3	I		
U14	MSS_MDIO_CLK	MSS_GPIO_31	0	IO	OUTPUT DISABLED	PU
		MSS_MDIO_CLK	1	O		
		RSVD	2	I		
		RSVD	3	I		
P1	MSS_UARTA_RX	MSS_GPIO_12	0	IO	OUTPUT DISABLED	PU
		MSS_CPTS0_TS_SYNC	1	O		
		RSVD	2	I		
		MSS_GPIO_8	3	IO		
		MSS_UARTB_RX	4	IO		
		MSS_UARTA_RX	5	IO		
		RSVD	6	IO		
R2	MSS_UARTA_TX	MSS_GPIO_13	0	IO		HI-Z
		MSS_CPTS0_HW2TSPUSH	1	I		
		RSVD	2	I		
		MSS_GPIO_9	3	IO		
		MSS_UARTB_TX	4	IO		
		MSS_UARTA_TX	5	IO		
		RSVD	6	IO		
P2	MSS_UARTB_TX	MSS_GPIO_0	0	IO		HI-Z
		RSVD	1	IO		

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表 6-1. Pin Attributes (AMQ / FCCSP Package) (続き)

BALL NUMBER	BALL NAME (DEFAULT)	MUX SIGNAL NAME	MODE	TYPE	BALL RESET STATE	PULL UP/DOWN TYPE
		RSVD	2	I		
		MSS_EPWMB_SYNCI	3	I		
		RSVD	4	IO		
		MSS_UARTA_TX	5	IO		
		MSS_UARTB_TX	6	IO		
		RSVD	7	I		
		LVDS_VALID	8	O		
		RSVD	9	I		
		RSVD	10	I		
		RSVD	11	I		
		MSS_GPIO_31	12	IO		

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6.3 Signal Descriptions - Digital

注

All digital IO pins of the device (except NERROR_OUT and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

注

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low , a tri-state buffer should be used to isolate the GPIO output from the radar device and a pull resister used to define the required state in the application. The NRESET signal to the radar device could be used to control the output enable (OE) of the tri-state buffer.

FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
SPI Interface	MSS_MIBSPIB_CLK	O	SPI Channel B - Clock	R1, T7
	MSS_MIBSPIB_SDO	O	SPI Channel B - Serial Data Out	T3
	MSS_MIBSPIB_SDI	I	SPI Channel B - Serial Data In	U2
	MSS_MIBSPIB_CS0	O	SPI Channel B - Chip Select 0	T1, T6
	MSS_MIBSPIB_CS1	O	SPI Channel B - Chip Select 1	U3, U4, T2
	MSS_MIBSPIB_CS2	O	PI Channel B - Chip Select 2	T2, U7
UART (MSS)	MSS_UARTA_RX	I	Main Subsystem - UART A Receive (For Flash programming)	P1, A10, A11, B8, R1
	MSS_UARTA_TX	IO	Main Subsystem - UART A Transmit (For Flash programming)	R2, A6, A16, B7, P2, T1
	MSS_UARTB_TX	IO	Main Subsystem - UART B Transmit	P2, A8, A16, B4, B6, N17, R1, R2, T1, T4
	MSS_UARTB_RX	I	Main Subsystem - UART B Receive	A11, C17, P1, U16
QSPI for Serial Flash	MSS_QSPI_0	IO	QSPI Data Line #0 (Used with Serial Data Flash)	U8
	MSS_QSPI_1	I	QSPI Data Line #1 (Used with Serial Data Flash)	U7
	MSS_QSPI_2	I	QSPI Data Line #2 (Used with Serial Data Flash)	U6
	MSS_QSPI_3	I	QSPI Data Line #3 (Used with Serial Data Flash)	T5
	MSS_QSPI_CLK	IO	QSPI clock (Used with Serial Data Flash)	T7
	MSS_QSPI_CS	O	QSPI chip select (Used with Serial Data Flash)	T6
I2C interface	MSS_I2C_SCL	IO	I2C Clock	R12, A10, A11, U2
	MSS_I2C_SDA	IO	I2C Data	T12, A6, A16, T3
RS232 UART	MSS_RS232_RX	IO	Debug UART (Operates as Bus Master) - Receive Signal	A11
	MSS_RS232_TX	IO	Debug UART (Operates as Bus Master) - Transmit Signal	A16

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
PWM Module	MSS_EPWMA0	O	PWM Module 1 - Output A0	A9, A16, B9, M17, T3
	MSS_EPWMA1	O	PWM Module 1 - Output A1	A16, B10, B11, U5, T13
	MSS_EPWMA_SYNCI	I	PWM Module 1 - Sync Input	U4
	MSS_EPWMA_SYNCO	O	PWM Module 1 - Sync Output	A7, B11
	MSS_EPWMB0	O	PWM Module 2 - Output B0	A7, A11, A16, B10, T2, U2, U5, U16
	MSS_EPWMB1	O	PWM Module 2 - Output B1	A8, A11, T2, T12
	MSS_EPWMB_SYNCI	I	PWM Module 2 - Sync Input	B9, P2
	MSS_EPWMB_SYNCO	O	PWM Module 2 - Sync Output	A7
	MSS_EPWMC0	O	PWM Module 3 - Output C0	A11, B18, N17, R1
	MSS_EPWMC1	O	PWM Module 3 - Output C1	A17, R12
	MSS_EPWMC_SYNCI	I	PWM Module 3 - Sync Input	A10
	MSS_EPWMC_SYNCO	O	PWM Module 3 - Sync Output	B11
	MSS_EPWM_TZ0	I	PWM module Trip Signal 0	A17, T4
	MSS_EPWM_TZ1	I	PWM module Trip Signal 1	B18, U4
	MSS_EPWM_TZ2	I	PWM module Trip Signal 2	A8, U5

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
RGMII/ RMII/MII Ethernet	MSS_MII_COL	I	MSS Ethernet MII Collision Detect	T13
	MSS_MII_CRS	I	MSS Ethernet MII Carrier Sense	T12
	MSS_MII_RXER	I	MSS Ethernet MII Receive Error	R12
	MSS_MII_TXEN	O	MSS Ethernet MII Transmit Enable	M17
	MSS_MII_RXDV	I	MSS Ethernet MII Receive Data Valid	U16
	MSS_MII_TXD3	O	MSS Ethernet MII Transmit Data 3	N17
	MSS_MII_TXD2	O	MSS Ethernet MII Transmit Data 2	T18
	MSS_MII_TXD1	O	MSS Ethernet MII Transmit Data 1	P17
	MSS_MII_TXD0	O	MSS Ethernet MII Transmit Data 0	R17
	MSS_MII_TXCLK	I	MSS Ethernet MII Transmit Clock	T17
	MSS_MII_RXCLK	I	MSS Ethernet MII Receive Clock	U15
	MSS_MII_RXD3	I	MSS Ethernet MII Receive Data 3	U17
	MSS_MII_RXD2	I	MSS Ethernet MII Receive Data 2	R16
	MSS_MII_RXD1	I	MSS Ethernet MII Receive Data 1	T16
	MSS_MII_RXD0	I	MSS Ethernet MII Receive Data 0	T15
	MSS_RMII_REFCLK	IO	MSS Ethernet RMII Clock Input	T13
	MSS_RMII_CRS_DV	I	MSS Ethernet RMII Carrier Sense/Receive Data Valid	T12
	MSS_RMII_RXER	I	MSS Ethernet RMII Receive Error	R12
	MSS_RMII_TXEN	O	MSS Ethernet RMII Transmit Enable	M17
	MSS_RMII_TXD1	O	MSS Ethernet RMII Transmit Data 1	P17
	MSS_RMII_TXD0	O	MSS Ethernet RMII Transmit Data 0	R17
	MSS_RMII_RXD1	I	MSS Ethernet MII Receive Data 1	T16
	MSS_RMII_RXD0	I	MSS Ethernet MII Receive Data 0	T15
	MSS_RGMII_TCTL	O	MSS Ethernet RGMII Transmit Control	M17
	MSS_RGMII_RCTL	I	MSS Ethernet RGMII Receive Control	U16
	MSS_RGMII_TD3	O	MSS Ethernet RGMII Transmit Data 3	N17
	MSS_RGMII_TD2	O	MSS Ethernet RGMII Transmit Data 2	T18
	MSS_RGMII_TD1	O	MSS Ethernet RGMII Transmit Data 1	P17
	MSS_RGMII_TD0	O	MSS Ethernet RGMII Transmit Data 0	R17
	MSS_RGMII_TCLK	O	MSS Ethernet RGMII Transmit Clock	T17
	MSS_RGMII_RCLK	I	MSS Ethernet RGMII Receive Clock	U15
	MSS_RGMII_RD3	I	MSS Ethernet RGMII Receive Data 3	U17
	MSS_RGMII_RD2	I	MSS Ethernet RGMII Receive Data 2	R16
	MSS_RGMII_RD1	I	MSS Ethernet RGMII Receive Data 1	T16
	MSS_RGMII_RD0	I	MSS Ethernet RGMII Receive Data 0	T15
	MSS_MDIO_DATA	IO	MSS Ethernet Manage Data Input/Output data	T14
	MSS_MDIO_CLK	O	MSS Ethernet Manage Data Input/Output Clock	U14
	MSS_CPTS0_TS_SYNC	O	Ethernet Timestamp SYNC output	P1
	MSS_CPTS0_HW2TSPUSH	I	Ethernet Hardware Timestamp Input Pin	A8, A17, R2
	MSS_CPTS0_HW1TSPUSH	I	Ethernet Hardware Timestamp Input Pin	A7, B18

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
Trace Signal	TRACE_DATA_0	O	Debug Trace Output - Data Line	A6
	TRACE_DATA_1	O	Debug Trace Output - Data Line	A10
	TRACE_DATA_2	O	Debug Trace Output - Data Line	B9
	TRACE_DATA_3	O	Debug Trace Output - Data Line	B11
	TRACE_DATA_4	O	Debug Trace Output - Data Line	A7
	TRACE_DATA_5	O	Debug Trace Output - Data Line	A8
	TRACE_DATA_6	O	Debug Trace Output - Data Line	B18
	TRACE_DATA_7	O	Debug Trace Output - Data Line	A17
	TRACE_CLK	O	Debug Trace Output - Clock	A9
	TRACE_CTL	O	Debug Trace Output - Control	B10

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
General-purpose I/Os	MSS_GPIO_0	IO	General-purpose I/O	U5, A10, P2
	MSS_GPIO_1	IO	General-purpose I/O	U4, B9
	MSS_GPIO_2	IO	General-purpose I/O	T4, B11
	MSS_GPIO_3	IO	General-purpose I/O	A7
	MSS_GPIO_4	IO	General-purpose I/O	A8, T1
	MSS_GPIO_5	IO	General-purpose I/O	B18, R1
	MSS_GPIO_6	IO	General-purpose I/O	A17, T6
	MSS_GPIO_7	IO	General-purpose I/O	T7
	MSS_GPIO_8	IO	General-purpose I/O	B9, P1, U8
	MSS_GPIO_9	IO	General-purpose I/O	B11, R2, U7
	MSS_GPIO_10	IO	General-purpose I/O	B18, U6
	MSS_GPIO_11	IO	General-purpose I/O	A17, T5
	MSS_GPIO_12	IO	General-purpose I/O	P1, U2
	MSS_GPIO_13	IO	General-purpose I/O	R2, U5
	MSS_GPIO_14	IO	General-purpose I/O	A16
	MSS_GPIO_15	IO	General-purpose I/O	A11
	MSS_GPIO_16	IO	General-purpose I/O	U4
	MSS_GPIO_17	IO	General-purpose I/O	T13, B6
	MSS_GPIO_18	IO	General-purpose I/O	B5, T12
	MSS_GPIO_19	IO	General-purpose I/O	R12
	MSS_GPIO_20	IO	General-purpose I/O	M17
	MSS_GPIO_21	IO	General-purpose I/O	U16, T3
	MSS_GPIO_22	IO	General-purpose I/O	N17, U2
	MSS_GPIO_23	IO	General-purpose I/O	B8, T18
	MSS_GPIO_24	IO	General-purpose I/O	A17, B7, P17
	MSS_GPIO_25	IO	General-purpose I/O	A9, B18, R17
	MSS_GPIO_26	IO	General-purpose I/O	A8, T4, T17
	MSS_GPIO_27	IO	General-purpose I/O	A7, B10, U15
	MSS_GPIO_28	IO	General-purpose I/O	B11, C17, U17
	MSS_GPIO_29	IO	General-purpose I/O	B9, R16, T2
	MSS_GPIO_30	IO	General-purpose I/O	A10, T14, T16
	MSS_GPIO_31	IO	General-purpose I/O	A6, P2, T15, U14
Chirp/Frame signals	ADC_VALID	O	When high, indicating valid ADC samples	A7, B9, B11, C17, T5, U3, U6
	CHIRP_START	O	Pulse signal indicating the start of each chirp	B9, B10, B11, B18, T4
	CHIRP_END	O	Pulse signal indicating the end of each chirp	A17, B9, B10, B11, T4
	FRAME_START	O	Pulse signal indicating the start of each frame	A9, B9, B10, B11, T4

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
LVDS_VALID	LVDS_VALID	O	When high, indicating valid LVDS data	A9, A16, B10, P2, T2, T4, U4
External clock out	MCU_CLKOUT	O	Programmable clock given out to external MCU or the processor	A9
	PMIC_CLKOUT	O	Output Clock from the device for PMIC	B10, T4, U5
System Synchronization	HW_SYNCIN	I	Low frequency Synchronization signal input	C17
	SYNC_OUT	O	Low Frequency Synchronization Signal output	C17, T2, T4, U4
Clock Output	OBS_CLKOUT	O	Debug Clock Output	A9, B10
	RCOSC_CLK	O	Debug Clock Output	T2
Reference Clock	XREF_CLK0	I	External reference input clock 0	A8
	XREF_CLK1	I	External reference input clock 1	A7
JTAG	TCK	I	JTAG Test Clock	B6
	TMS	IO	JTAG Test Mode Signal	B5
	TDI	I	JTAG Test Data Input	B8
	TDO	O	JTAG Test Data Output	B7
UART (BSS)	BSS_UARTA_TX	O	Debug UART Transmit [Radar Block]	B18, A16, A11, B5, B7, R1, T1, U4
	BSS_UARTA_RX	I	Debug UART Receive [Radar Block]	A9, B6
Reset	WARM_RESET	IO	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	B17
Safety	NERROR_OUT	O	Open drain fail safe output signal. Connected to PMIC/ Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	D17
Sense On power	SOP[0]	I	The SOP pins are driven externally (weak drive) and the mmWave device senses the state of these pins during bootup to decide the bootup mode. After boot the same pins have other functionality. • [SOP2 SOP1 SOP0] = [0 0 1] -> Functional QSPI load mode • [SOP2 SOP1 SOP0] = [1 0 1] -> UART load mode • [SOP2 SOP1 SOP0] = [0 1 1] -> debug and development mode • [SOP2 SOP1 SOP0] = [1 1 0] -> JTAG load mode for customer key provisioning The following configurations of SOP pins help decide the reference crystal frequency • [SOP4 SOP3] = [0 0] -> 40 MHz • [SOP4 SOP3] = [1 1] -> 50 MHz	B7
	SOP[1]	I		T2
	SOP[2]	I		B10
	SOP[3]	I		P2
	SOP[4]	I		R2

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FUNCTION	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
CSI2 / LVDS	CSI2_TXM0 / LVDS_TXM0	O	CSI2 / LVDS Transmitter, Differential Data Output, Lane 0	K17
	CSI2_TXP0 / LVDS_TXP0	O		K18
	CSI2_TXM4 / LVDS_CLKM	O	CSI2 / LVDS Differential Clock	L17
	CSI2_TXP4 / LVDS_CLKP	O		L18
	CSI2_CLKM / CSI2_TXM2 / LVDS_FRCLKM	O	CSI2 / LVDS Differential Frame Clock	F17
	CSI2_CLKP / CSI2_TXP2 / LVDS_FRCLKMP	O		F18
	CSI2_TXM1 / LVDS_TXM1	O	CSI2 / LVDS Transmitter, Differential Data Output, Lane 1	J17
	CSI2_TXP1 / LVDS_TXP1	O		J18
	CSI2_TXM3	0	CSI2 Transmitter - Differential Data Output	G17
	CSI2_TXP3	0	CSI2 Transmitter - Differential Data Output	G18

6.4 Signal Descriptions - Analog

INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
Waveguide Launches	Transmitter	O	Waveguide Launch for TX outputs	
	Receiver	I	Waveguide Launch for RX inputs	
Reset	NRESET	I	Power on reset for chip. Active low. The NRESET needs to be pulled low for a minimum of 20 µsec to ensure proper device reset.	E17
Reference Oscillator	CLKP	I	In XTAL mode: Input for the reference crystal In External clock mode: Single ended input reference clock port	F2
	CLKM	I	In XTAL mode: Feedback drive for the reference crystal In External clock mode: Connect this port to ground	E1
Reference Clock for Ethernet	OSC_CLK_OUT_ETH	O	Can be used to replace 25MHz crystal used with Ethernet PHY IC (OSC_CLK_OUT_25 on EVM). Please note that this is only useable when a 50MHz reference crystal is used with the device	C1
Reference clock	OSC_CLKOUT	O	Reference clock output from clocking subsystem after cleanup PLL (OSC_CLKTOP on EVM)	C2
Bandgap voltage	VBGAP	O	Device's Band Gap Reference Output	K1
Power supply	VDD	Power	1.2V digital power supply	A15,D18,M14,M15,M16, N13,N15,P13,P15,R14,U9
	VDD_SRAM	Power	1.2V power rail for internal SRAM	U13
	VNWA	Power	1.2V power rail for SRAM array back bias	C18
	VIOIN	Power	I/O Supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply	A12, N18, U12
	VIOIN_18	Power	1.8V supply for CMOS IO	A13, R18, U10
	VDDA_18CLK	Power	1.8V supply for clock module	A2
	VDDA_18PM	Power	1.8V supply for PM module	K2
	VIOIN_18CSI	Power	1.8V supply for CSI port	H18
	VPP	Power	Voltage supply for fuse chain	M18

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INTERFACE	SIGNAL NAME	PIN TYPE	DESCRIPTION	BALL NUMBER
Power supply	VDDA_10RF1	Power	1V Analog and RF supply,VDDA_10RF1 and VDDA_10RF2 could be shorted on the board	M1
	VDDA_10RF2	Power	1V Analog and RF supply	A3,A4
	VDDA_18BB	Power	1.8V Analog base band power supply	N1
	VDDA_18VCO	Power	1.8V RF VCO supply	J2
	VSS(2)	Ground	Digital ground	A14,A18,E18,H12,H17,J12,L14,L16,M12, P12,P18,U1, U11,U18
	VSSA(3)	Ground	Analog ground	A1,A5,B1,B2,B3,B4,B12, B13,B14,B15,B16,C3,C4,C5,C6,C7,C8,C 9,C10,C11,C12, C16,D1,D2,D3,D7,D8,D11, D12,D16,E2,E3,E7,E8,E11, E12,E13,E14,E15,E16,F1, F3,F4,F5,F6,F7,F8,F11,F12,F13,F14,F15 ,F16,G1,G2,G3,G4,G5,G6,G8,G9,G10,G 11, G12,G13,G16,H3,H6,H7,H8,H9,H10,H11, H13,H16,J1, J3,J6,J7,J11,J13,J16,K3,K6, K7,K11,K13,K14,K15,K16, L3,L4,L5,L6,L7,L8,L9,L10, L11,M3,M4,M5,M6,M7, M8,M9,M10,M11,N3,N7, N8,N11,P3,P7,P8,P11,R3, R4,R5,R6,R7,R8,R11, T8,T9,T10,T11
Internal LDO output/ inputs	VOUT_14APLL	O	Internal LDO output	H2
	VOUT_14SYNTH	O	Internal LDO output	H1
General purpose ADC inputs for external voltage monitoring(1)	ADC1	I	ADC Channel 1	L2
	ADC2	I	ADC Channel 2	L1
	ADC5	I	ADC Channel 5	N2
	ADC6	I	ADC Channel 6	M2

(1) For details, see セクション 8.4.3
(2) Corner BGAs are VSS and redundant, meaning if they fail, the device will still function.
(3) The VSSA BGAs around the launches are not redundant and are required for functionality.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETERS		MIN	MAX	UNIT
VDD	1.2V digital power supply	–0.5	1.4	V
VDD_SRAM	1.2V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8V supply for CMOS IO	–0.5	2	V
VDDA_18CLK	1.8V supply for clock module	–0.5	2	V
VDDA_18PM	1.8V supply for the PM Module	-0.5	2	V
VIOIN_18CSI	1.8V supply for CSI2 port	–0.5	2	V
VIOIN_18LVDS	1.8V supply for LVDS port	–0.5	2	V
VDDA_10RF1 VDDA_10RF2	1V Analog and RF supply, VDDA_10RF1 and VDDA_10RF2 could be shorted on the board.	–0.5	1.4	V
VDDA_18BB	1.8V Analog baseband power supply	–0.5	2	V
VDDA_18VCO supply	1.8V RF VCO supply	–0.5	2	V
RX1-4	Externally applied power on RF inputs		10	dBm
TX1-4	Externally applied power on RF outputs(3)		10	dBm
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 1.8V/3.3V (Transient Overshoot/Undershoot) or external oscillator input	VIOIN + 20% up to 20% of signal period		
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	140	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_J) (1) (2)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
–40°C	50% duty cycle	1.2	1440 (6%)
75°C			4800 (20%)
95°C			15600 (65%)
130°C			1920 (8%)
140°C			240 (1%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) The specified POH are applicable with max Tx output power settings using the default firmware gain tables. The specified POH would not be applicable, if the Tx gain table is overwritten using an API.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD	1.2V digital power supply	1.14	1.2	1.26	V
VDD_SRAM	1.2V power rail for internal SRAM	1.14	1.2	1.26	V
VNWA	1.2V power rail for SRAM array back bias	1.14	1.2	1.26	V
VIOIN	I/O supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8V supply for CMOS IO	1.71	1.8	1.89	V
VDDA_18CLK	1.8V supply for clock module	1.71	1.8	1.89	V
VDDA_18PM	1.8V supply for the PM module	1.71	1.8	1.89	V
VIOIN_18CSI	1.8V supply for CSI2 port	1.71	1.8	1.89	V
VIOIN_18LVDS	1.8V supply for LVDS port	1.71	1.8	1.89	V
VDDA_10RF1	1V Analog and RF supply. VDDA_10RF1 and VDDA_10RF2 could be shorted on the board	0.95	1	1.05	V
VDDA_10RF2					
VDDA_18BB	1.8V Analog baseband power supply	1.71	1.8	1.89	V
VDDA_18VCO	1.8V RF VCO supply	1.71	1.8	1.89	V
V_{IH}	Voltage Input High (1.8V mode)	1.17		0.3 + VIOIN	V
	Voltage Input High (3.3V mode)	2.25		0.3 + VIOIN	
V_{IL}	Voltage Input Low (1.8V mode)	-0.3		0.3*VIOIN	V
	Voltage Input Low (3.3V mode)	-0.3		0.62	
V_{OH}	High-level output threshold (I_{OH} = 6mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6mA)			450	mV
NRESET SOP[4:0]	V_{IL} (1.8V Mode)			0.45	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.65	
	V_{IH} (3.3V Mode)	1.57			
T_J	Operating junction temperature range	-40		140	℃

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7.5 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for high-security (AWR2544 HS) devices. During the process of writing the customer specific keys or other custom information in the eFuse, the user needs to provide the VPP supply.

7.5.1 Recommended Operating Conditions for OTP eFuse Programming

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VPP	Supply voltage range for the eFuse ROM domain during normal operation		NC		
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.65	1.7	1.75	V
Duration of VPP Supply	If VPP voltage is supplied for more than recommended Hours, it can cause reliability issue			24	hours
I(VPP)				50	mA

(1) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the external regulator attached to the VPP terminal.

7.5.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.

7.5.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, in these cases of faulty EFUSE programmability, TI WILL HAVE NO LIABILITY.

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7.6 Power Supply Specifications

表 7-1 describes the four required power rails which must be provided to the AWR2544 from an external power supply. In the case when 1.8V LVCMOS IO is utilized, VIOIN is powered from a 1.8V rail and the 3.3V rail can be omitted, so only three rails must be provided. Also, depending on the power topology utilized, additional power supply filtering can be required for the RF 1.0V and baseband, clock and VCO 1.8V supplies to meet the required ripple specifications. This additional filtering results in separate supply power nets being generated from these four basic rails.

表 7-1. Power Supply Rails Characteristics

SUPPLY VOLTAGE	DEVICE BLOCKS POWERED FROM THE SUPPLY	DEVICE POWER NETS
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, CSI2, LVDS, LVCMOS IO	Input: VDDA_18VCO, VDDA_18CLK, VDDA_18PM, VDDA_18BB, VIOIN_18CSI, VIOIN_18LVDS, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.0 V	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VDDA_10RF2, VDDA_10RF1
3.3 V (or 1.8 V for 1.8 V I/O mode)	LVCMOS IO	VIOIN
1.2 V	Core Digital and SRAM	VDD, VDD_SRAM, VNWA
1.7 V	Programming OTP eFuse (For secure devices)	VPP

The 1.0 V and 1.8 V power supply ripple specifications are mentioned in 表 7-2 The spur and ripple levels have a dB to dB relationship, for example, a 1dB increase in supply ripple leads to an approximately 1dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

表 7-2. Ripple Specifications

FREQUENCY (kHz)	Spur Level (dBc)	RF RAIL	VCO/IF RAIL
		1 V (μV_{RMS})	1.8 V (mV_{RMS})
10	-85	22	10.99
100	-95	8	1.42
200	-98	6	0.73
500	-102	4	0.45
1000	-105	3	0.30
2000	-105	3	0.08
5000	-105	3	0.06
10000	-105	3	0.06
15000	-105	2	0.04
20000	-105	2	0.04

Power Supply Guidelines

The LP8772-Q1 Power Management IC (PMIC) is recommended for an integrated AWR2544 power solution. This cost and space optimized solution is designed to power the AWR2544 radar sensor and its principal peripherals.

List of benefits when using LP8772-Q1 PMIC to power AWR2544:

1. Full device performance entitlement as validated on TI Evaluation boards
2. Noise/Ripple performance that meets AWR noise/ripple performance specification

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a. LP8772-Q1 has high switching frequency switching outside IF band & avoiding the LDOs helps with thermal performance at the system level and bypasses the need for 2nd stage LC filters to suppress the ripple and filter out the spurs.
b. Thermal dissipation does not affect RF performance

7.7 Power Consumption Summary

表 7-3 and 表 7-4 summarize the power consumption at the power terminals.

表 7-3. Maximum Current Ratings at Power Terminals

PARAMETER(1)	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption	VDD, VDD_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			2000	mA
	VDDA_10RF1, VDDA_10RF2	Total current drawn by all nodes driven by 1V rail when all 4 transmitters are used			2300	
	VIOIN_18, VDDA_18CLK, VDDA_18PM, VIOIN_18CSI, VIOIN_18LVDS, VDDA_18BB, VDDA_18VCO	Total current drawn by all nodes driven by 1.8V rail			600	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail			50	

(1) The specified current values are at Max supply voltage level (Recommended Operating Conditions).

表 7-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP(1)	MAX	UNIT
Average power consumption in single chip mode.	3TX, 4RX	25% duty cycle	Use Case: 76-77GHz chirps; Regular mode, 45 Msps sampling rate, 25.6 ms frame periodicity, 256 chirps/ frame, 2-µs idle time, 50-µs ramp end time, 7us ADC start time and excess ramp time Activity of cores : • 70% MSS R5F • 50% Arm M4F All the above cores under-clocked/ clock-gated during idle times); Ethernet is enabled for data transfer		1350		mW
		50% duty cycle			2000		
	4TX, 4RX	25% duty cycle			1400		
		50% duty cycle			2100		

(1) The Power consumption numbers are for a typical usecase i.e. for a Nominal device at 25C ambient temperature and nominal voltage conditions.

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7.8 RF Specifications

over recommended operating conditions and with run time calibrations enabled (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure			12.5		dB
	1dB compression point (Out Of Band)(1)			-8		dBm
	Maximum gain			44		dB
	Gain range			20		dB
	Gain step size			2		dB
	IF bandwidth(2)				20	MHz
	ADC sampling rate				45	Msps
	ADC resolution			12		Bits
	Return loss (S11)			-10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	Idle Channel Spurs			-90		dBFS
Transmitter	Output power			+12.5		dBm
	Phase shifter accuracy			±5		°
	Temperature sensor accuracy			±5		℃
	Amplitude noise			-145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				250(3)	MHz/µs
	Phase noise at 1-MHz offset	76 to 77GHz (VCO1)		-96		dBc/Hz
		76 to 81GHz (VCO2)(4)		-95		

(1) 1-dB Compression Point (Out Of Band) is measured by feeding a continuous wave tone at 5% of the programmed HPF cut-off frequency (i.e. blocker tone). The compression point is determined by the blocker power that results in a 1dB compression of the blocker tone at the RX ADC.

(2) The analog IF stages include a second order high pass filter that can be configured to the following -6dB corner frequencies:

Available HPF Corner Frequencies (kHz)
HPF
300, 350, 700, 1400,

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5dB pass-band ripple/droop, and
- Better than 60dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

(3) The max ramp rate depends on the PLL bandwidth configuration set using the"AWR_APLL_SYNTH_BW_CONTROL_SB" API. For more details, refer to the mmWave Radar Interface Control document.

(4) VCO2 supports a maximum continuous range of 4.5GHz. The supported range can span 76-80.5GHz or 76.5-81GHz through VCO2_RANGE_CONFIG in AWR_ CAL_MON_FREQUENCY_* API.

図 7-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed

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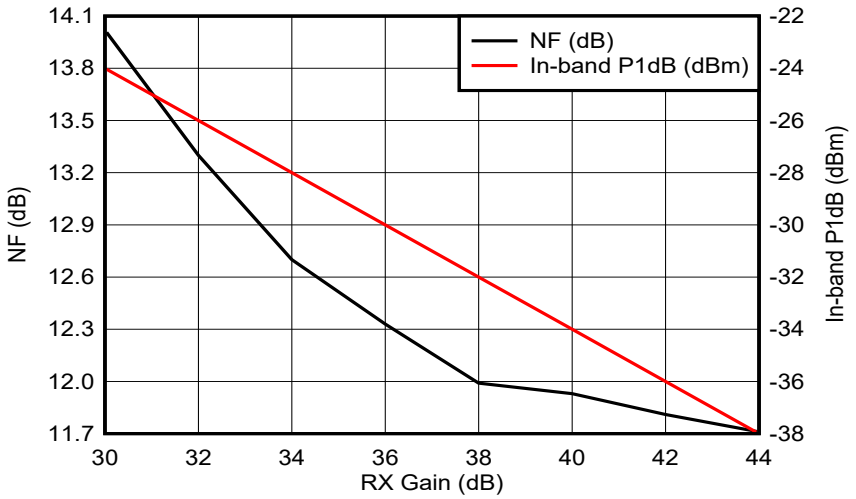

図 7-1. Noise Figure, In-band P1dB vs Receiver Gain

7.9 Thermal Resistance Characteristics

THERMAL METRICS(1) (4)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	3.36
$R\Theta_{JB}$	Junction-to-board	5.0
$R\Theta_{JA}$	Junction-to-free air	17.3
Ψ_{JT}	Junction-to-top	0.12
Ψ_{JB}	Junction-to-board	4.9

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

A junction temperature of 140°C is assumed.
(4) Air flow = 0m/s

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7.10 Power Supply Sequencing and Reset Timing

The AWR2544 device expects all external 1.2V, 1.8V and 3.3V voltage rails as well as all SOP[4:0] lines to be stable before NRESET is deasserted for a successful device bootup. IO state is not guaranteed until the VIOIN and VIOIN_18 supplies are available. 図 7-2 describes the device wake-up sequence.

注

Hardware platform must support supplying 1.7V on the VPP pin only during OTP eFuse programming.

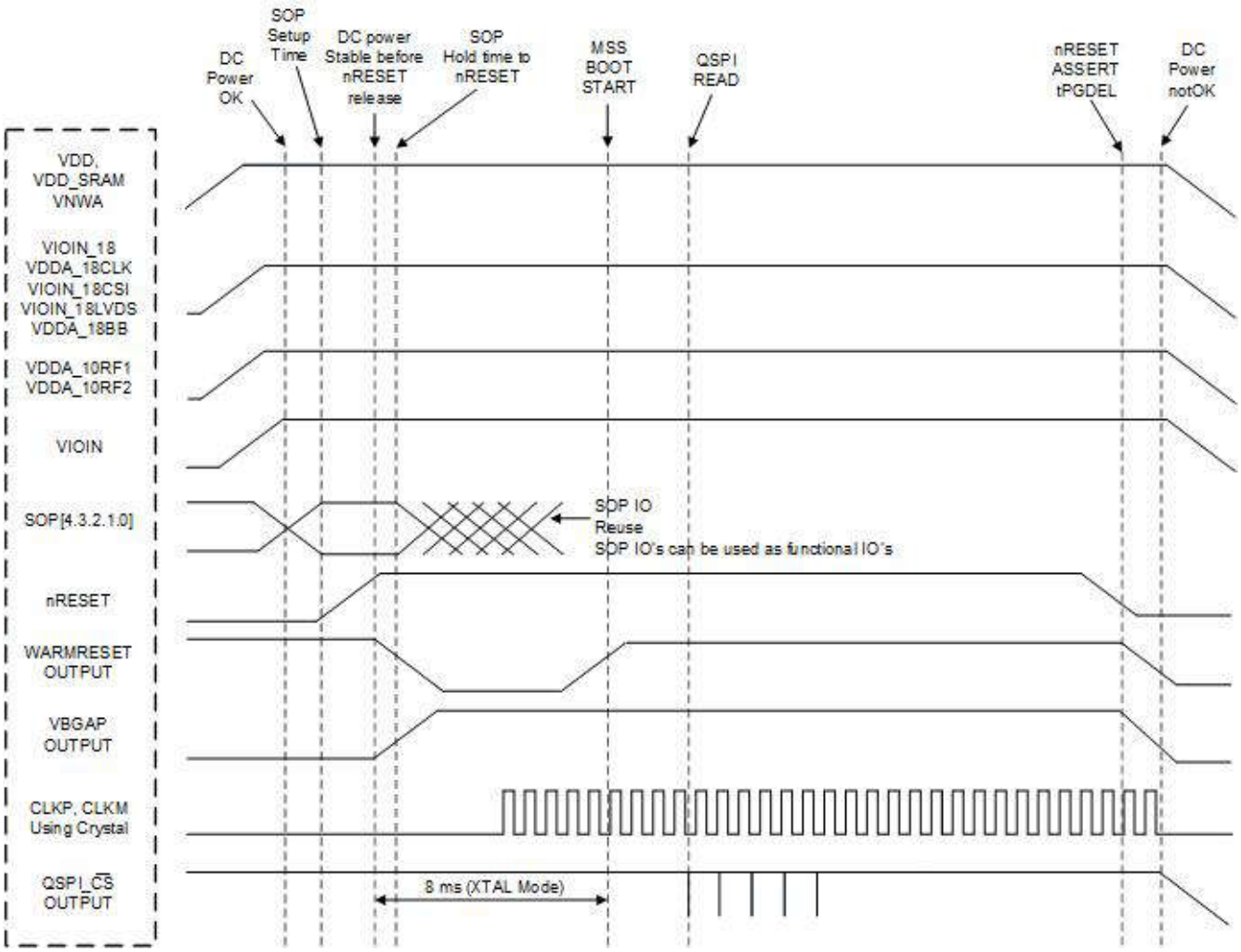

図 7-2. Device Wake-up Sequence

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7.11 Input Clocks and Oscillators

7.11.1 Clock Specifications

An external crystal is connected to the device pins. 図 7-3 shows the crystal implementation.

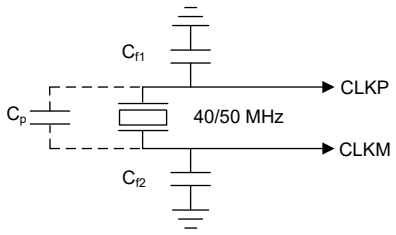

図 7-3. Crystal Implementation

注

The load capacitors, C_{f1} and C_{f2} in 図 7-3, can be chosen such that 式 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit can be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

注

The board routing parasitics between CLKP/CLKM pins also need to be included in the estimates of C_P

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

表 7-5 lists the electrical characteristics of the clock crystal.

表 7-5. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		50		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	-40		140	℃
Frequency tolerance	Crystal frequency tolerance(1) (2)	-100		100(3)	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) For Ethernet operation, tighter specifications of less than 100PPM frequency error is required. If the Ethernet interface is not used , a PPM error up to 200PPM can be tolerated.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 50MHz clock is fed externally. 表 7-6 lists the electrical characteristics of the external clock signal.

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表 7-6. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 50 MHz	Frequency		50		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-trise/fall			10	ns
	Phase Noise at 1 kHz			-132	dBc/Hz
	Phase Noise at 10kHz			–143	dBc/Hz
	Phase Noise at 100kHz			–152	dBc/Hz
	Phase Noise at 1MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	-100		100	ppm

7.12 Peripheral Information

Initial peripheral descriptions and features are provided in the following sections. Additional peripheral details and interface timing information shall be provided in a later product preview or datasheet release.

7.12.1 QSPI Flash Memory Peripheral

The device includes a Quad-Serial Peripheral Interface for external flash memory access. Flash memory can be utilized for many purposes including: Secondary boot-loader memory, application program memory, security keys storage, and long-term data logs for security and error conditions.

Following features are supported by the QSPI Interface on the device:

- Loopback skew cancellation for clock signal to supported faster flash interface clock rates
- Two chip-select signals to connect two external flash devices
- Memory mapped 'direct' mode and software triggered 'indirect' mode of operation for performing flash data transfers

7.12.1.1 QSPI Timing Conditions

PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	5		15	pF

7.12.1.2 QSPI Timing Requirements (1) (2)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, D[3:0] valid before falling SCLK edge (Q12)	5			ns
$t_{h(SCLK-D)}$	Hold time, D[3:0] valid after falling SCLK edge (Q13)	1			ns

(1) Clock Mode 0 (clock polarity = 0 ; clock phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although nonstandard, The falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.

7.12.1.3 QSPI Switching Characteristics (1) (2)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(SCLK)}$	Cycle time, sclk	12.5			ns
$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 0.625			ns
$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 0.625			ns

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PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1		–M*P + 2.5	ns
$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	–2		4	ns
$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–2– P		4 – P	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

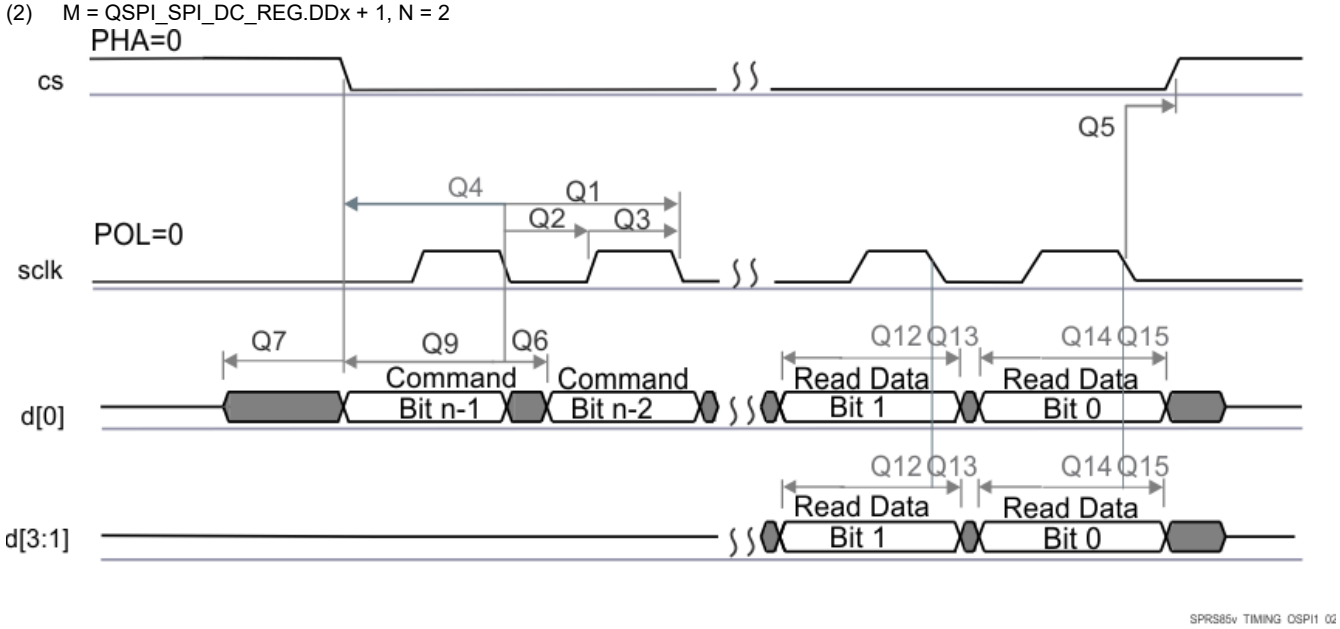

図 7-4. QSPI Read (Clock Mode 0)

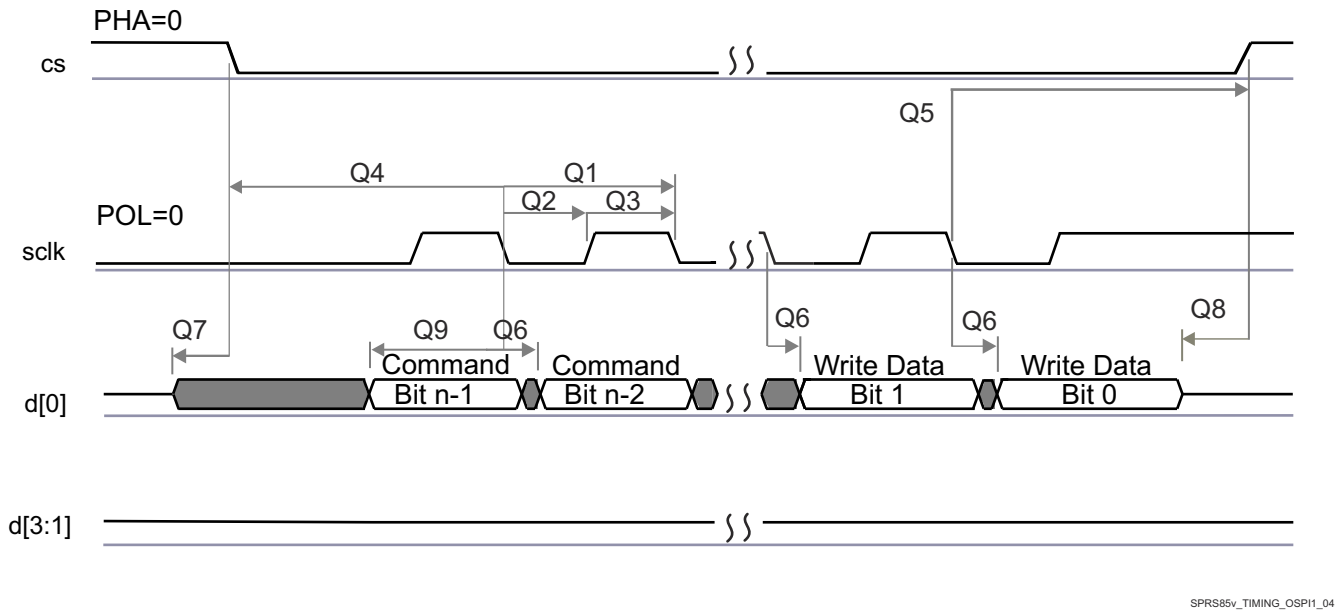

図 7-5. QSPI Write (Clock Mode 0)

7.12.2 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

7.12.2.1 MibSPI Peripheral Description

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The device includes one Multi-Buffered Serial Peripheral Interface (MibSPI) in the Main Sub-System (MSS). This is intended for external MCU, PMIC, EEPROM and Watchdog communication.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (Controller mode) or received from an external clock source (Peripheral mode)
- Maximum clock rate supported over each MIBSPI module shall be 40MHz.
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

7.12.2.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

セクション 7.12.2.2.2 and セクション 7.12.2.2.3 assume the operating conditions stated in セクション 7.12.2.2.1.

7.12.2.2.1 SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

7.12.2.2.2 SPI Controller Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input) (1) (2) (3)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{c(SPC)M}$	Cycle time, SPICLK(4)	20		$256t_{c(VCLK)}$	ns
$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 7$			ns
$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 7$			
$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 8$			ns
$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 8$			

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PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	(C2TDELAY+2)*$t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	ns
		CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
	Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	(C2TDELAY+2)*$t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	
		CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
	Hold time, SPICLK high until CS inactive (clock polarity = 1)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	
$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		2			ns
$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		2			

(1) The Controller bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(3) When the SPI is in controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25ns$.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

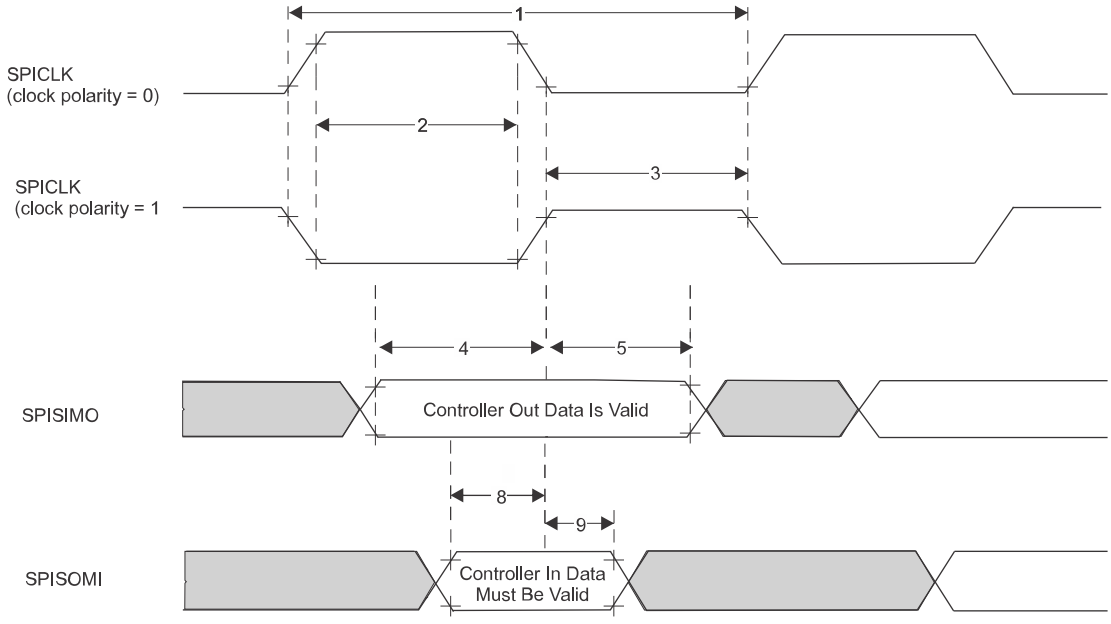

図 7-6. SPI Controller Mode External Timing (CLOCK PHASE = 0)

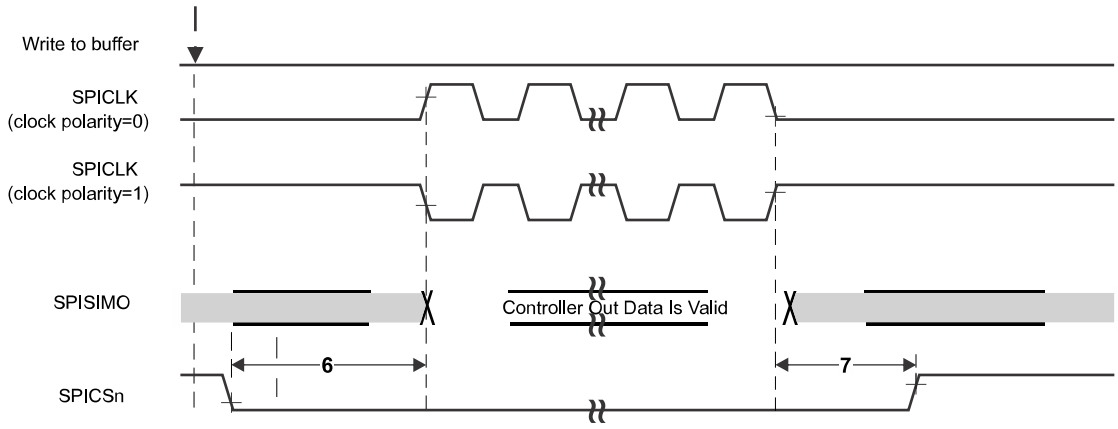

図 7-7. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 0)

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7.12.2.2.3 SPI Controller Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input) (1) (2) (3)

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{c(SPC)M}$	Cycle time, SPICLK(4)		20		$256t_{c(VCLK)}$	ns
$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	ns
$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 2$		$0.5t_{c(SPC)M} + 2$	
$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 7$			ns
$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 7$			
$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 8$			ns
$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 8$			
$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
		CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
	Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	
$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
	Hold time, SPICLK high until CS inactive (clock polarity = 1)		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	
$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		2			ns
$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		2			

(1) The Controller bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(3) When the SPI is in Controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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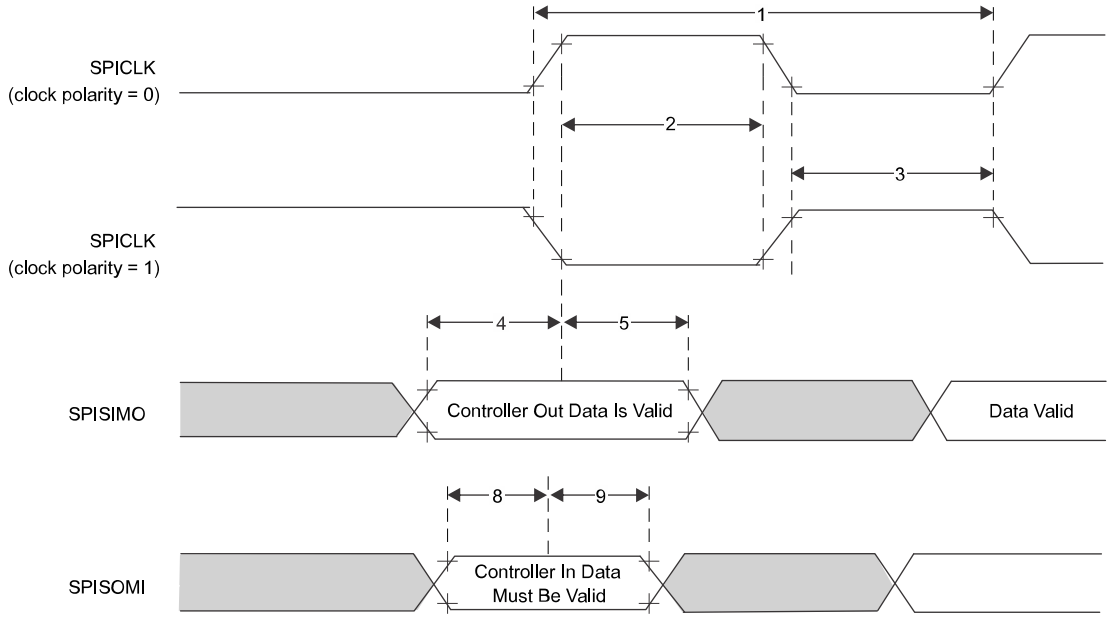

図 7-8. SPI Controller Mode External Timing (CLOCK PHASE = 1)

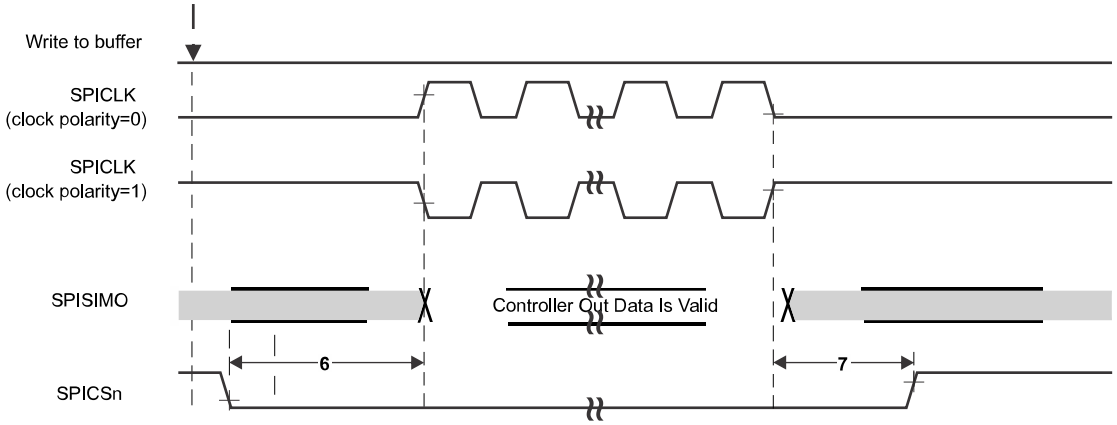

図 7-9. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 1)

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7.12.2.3 SPI Peripheral Mode I/O Timings

7.12.2.3.1 SPI Peripheral Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) (1) (2) (3)

PARAMETER(5)	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{c(SPC)S}$	Cycle time, SPICLK (4)	20			ns
$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	8			ns
$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	8			
$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	8			ns
$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	8			
$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			14	ns
$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			14	
$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			
$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2.1			ns
$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2.1			
$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The Controller bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS_VCLK)}$. For more details, refer to the device Technical Reference Manual.
(4) When the SPI is in Peripheral mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(MSS_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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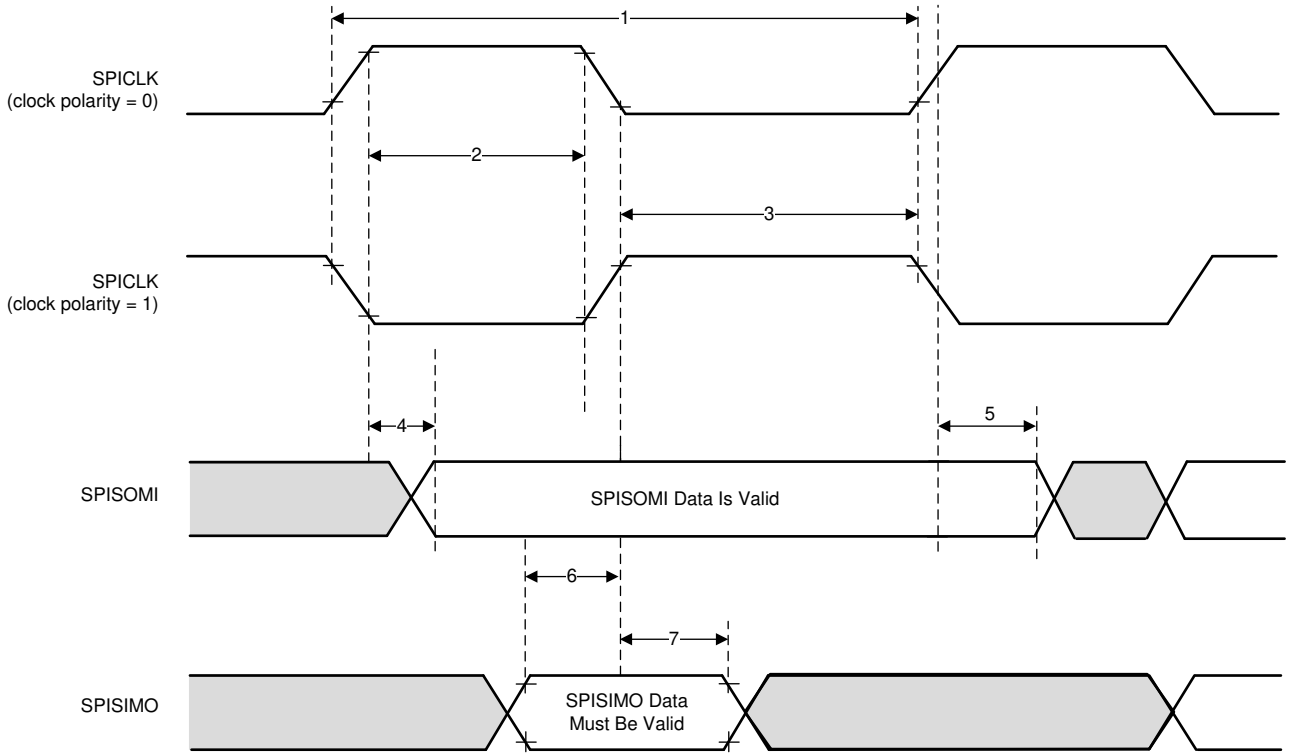

図 7-10. SPI Peripheral Mode External Timing (CLOCK PHASE = 0)

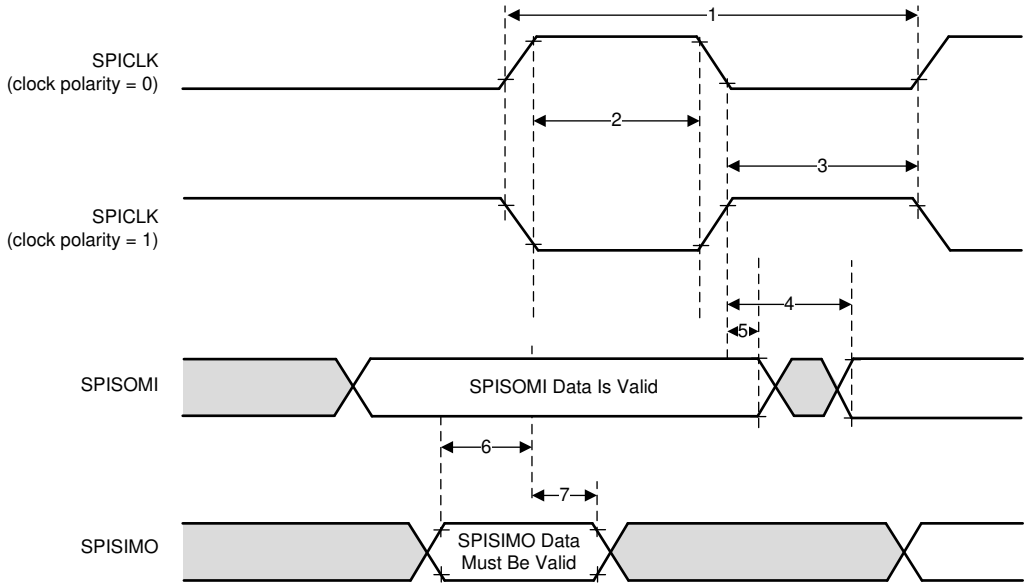

図 7-11. SPI Peripheral Mode External Timing (CLOCK PHASE = 1)

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7.12.3 Ethernet Switch (RGMII/RMII/MII) Peripheral

The device integrates a two port Ethernet with one external RGMII/RMII/MII port and another port servicing the Main Sub-System (MSS). This interface is intended to operate primarily as a 1Gbps ECU interface. It can also be used as an instrumentation interface.

- Full Duplex 10Mbps/100Mbps/1Gbps wire rate interface to Ethernet PHY over RGMII, RMII, or MII parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support
- CPTS based radar frame triggering, allowing Ethernet to trigger radar frames

7.12.3.1 RGMII/RMII/MII Timing Conditions

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
	Input Conditions					
1	SR_I	Input Slew Rate	2.64		5	V/ns
	Output Conditions					
3	C_{LOAD}	Output load capacitance	2		20	pF

7.12.3.2 RGMII Transmit Clock Switching Characteristics

PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
$t_{c(TXC)}$	Cycle time, rgmiin_txc	10Mbps	360	440	ns
		100Mbps	36	44	ns
		1Gbps	7.6	8.4	ns
$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10Mbps	160	240	ns
		100Mbps	16	24	ns
		1Gbps	3.6	4.4	ns
$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10Mbps	160	240	ns
		100Mbps	16	24	ns
		1Gbps	3.6	4.4	ns
$t_{t(TXC)}$	Transition time, rgmiin_txc	10Mbps		1.4	ns
		100Mbps		1.4	ns
		1Gbps		0.75	ns

7.12.3.3 RGMII Transmit Data and Control Switching Characteristics

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10M/100M/1G	1.2		ns
$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10M/100M/1G	1.2		ns

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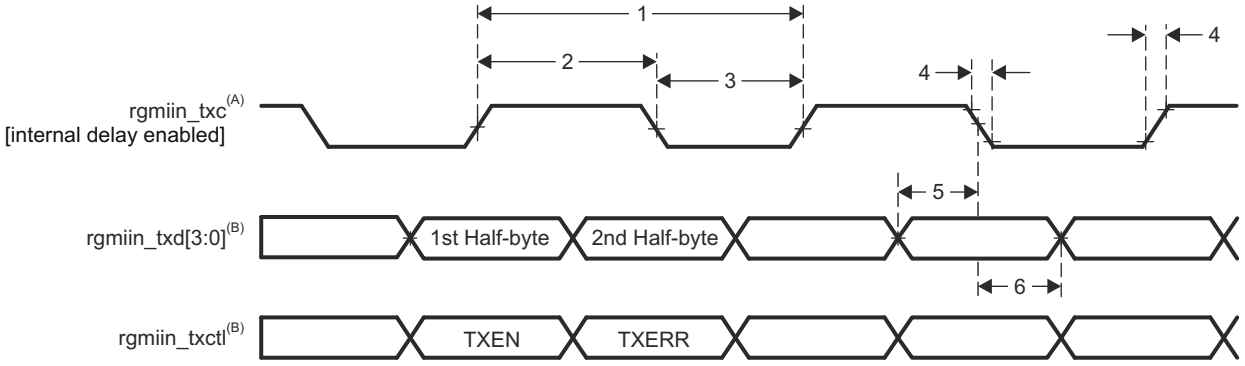

A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

図 7-12. RGMII Transmit Interface Switching Characteristics

7.12.3.4 RGMII Receive Clock Timing Requirements

PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10Mbps	360	440	ns
		100Mbps	36	44	ns
		1Gbps	7.6	8.4	ns
$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10Mbps	160	240	ns
		100Mbps	16	24	ns
		1Gbps	3.6	4.4	ns
$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10Mbps	160	240	ns
		100Mbps	16	24	ns
		1Gbps	3.6	4.4	ns
$t_{t(RXC)}$	Transition time, rgmiin_rxc	10Mbps		1.4	ns
		100Mbps		1.4	ns
		1Gbps		0.75	ns

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7.12.3.5 RGMII RX and TX Timing Diagrams

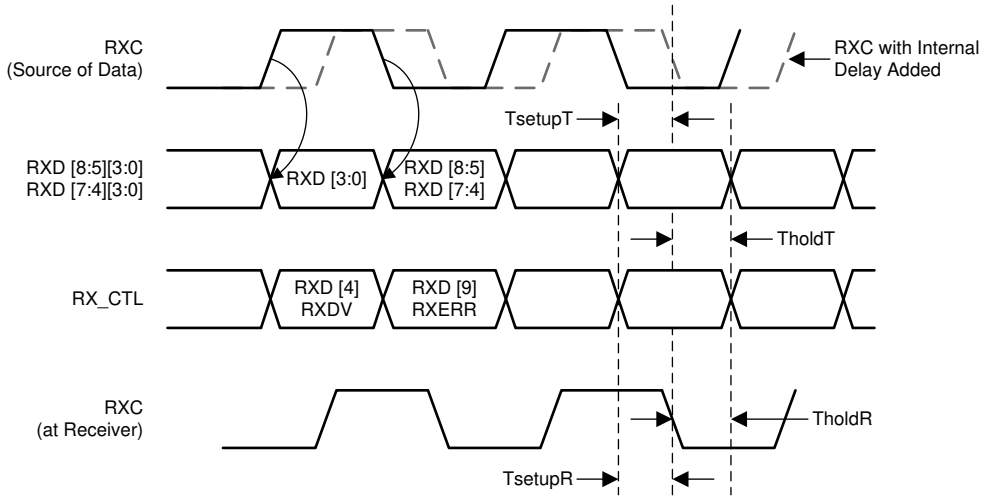

図 7-13. RGMII RX Timing Diagram

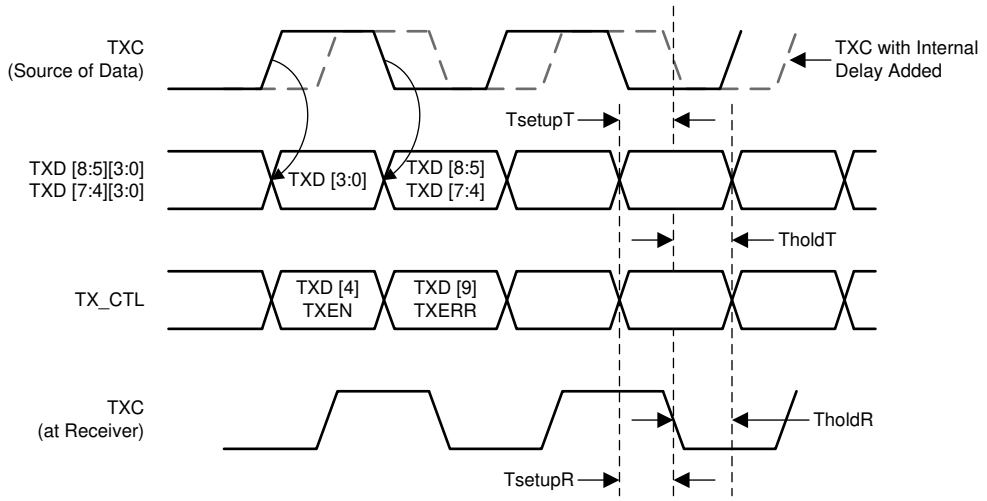

図 7-14. RGMII TX Timing Diagram

表 7-7.

TX Mode	RX Mode	TX Delay	RX Delay	Loopback Testcase	Comment
Aligned	Aligned	0.250 ns	0.250 ns	RXCRC errors, RXAlignCode Errors at MAC port	
Aligned	Aligned	0.500 ns	0.500 ns	RXCRC errors, RXAlignCode Errors at MAC port	
Aligned	Shift	0.250 ns	0.250 ns	Passed: No Packet drops at MAC port	
Aligned	Shift	0.250 ns	2 ns	Passed: No packet drops at MAC port.	This is the TI recommended settings
Aligned	Aligned	0.250 ns	0.500 ns	RXCRC errors, RXAlignCode Errors at MAC port	

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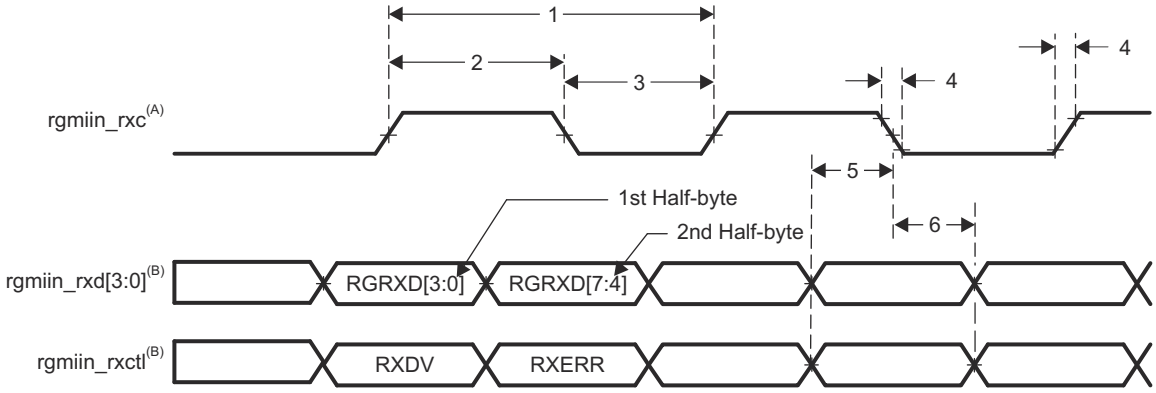
7.12.3.6 RGMII Receive Data and Control Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before MSS_RGMII_RCLK high/low	1.25		ns
$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after MSS_RGMII_RCLK high/low	1.25		ns



A. rgmiin_rxc must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. MSS_RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

図 7-15. MAC Receive Interface Timing, RGMIIn operation

7.12.3.7 RMII Transmit Clock Switching Characteristics

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
$t_{t(REF_CLK)}$	Transition time, REF_CLK		3	ns

7.12.3.8 RMII Transmit Data and Control Switching Characteristics

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	2	14.2	ns
$t_{dd(REF_CLK-TXEN)}$				

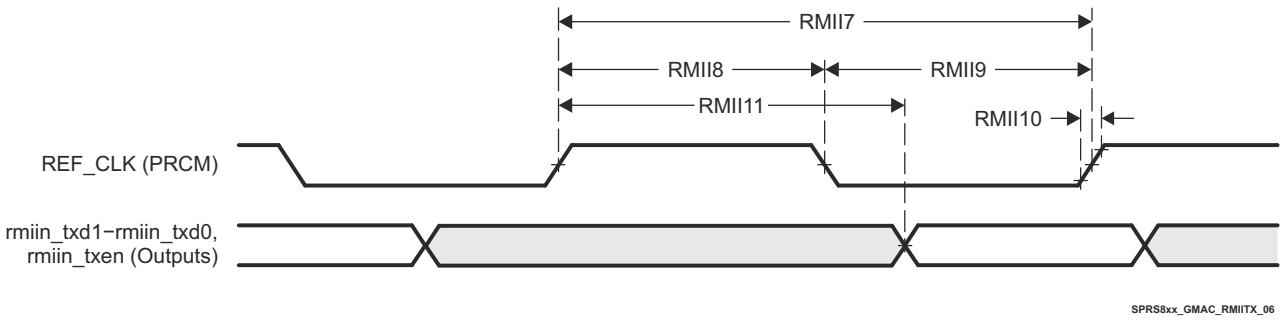


図 7-16. MAC Transmit Interface Timing, RMIIn Operation

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7.12.3.9 RMII Receive Clock Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{c(REF_CLK)}$	Cycle time, REF_CLK	20		ns
$t_{w(REF_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
$t_{w(REF_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
$t_{tt(REF_CLK)}$	Transistion time, REF_CLK		3	ns

7.12.3.10 RMII Receive Data and Control Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{su(RXD-REF_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
$t_{su(CRS_DV-REF_CLK)}$				
$t_{su(RX_ER-REF_CLK)}$				
$t_{h(REF_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
$t_{h(REF_CLK-CRS_DV)}$				
$t_{h(REF_CLK-RX_ER)}$				

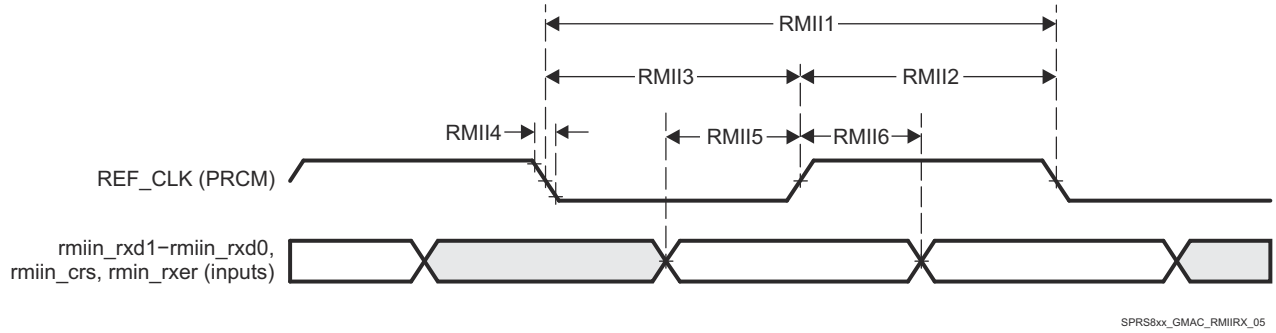

図 7-17. MAC Receive Interface Timing, RMIIn operation

7.12.3.11 MII Transmit Switching Characteristics

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{d(TX_CLK-TXD)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
$t_{d(TX_CLK-TX_EN)}$				
$t_{d(TX_CLK-TX_ER)}$				

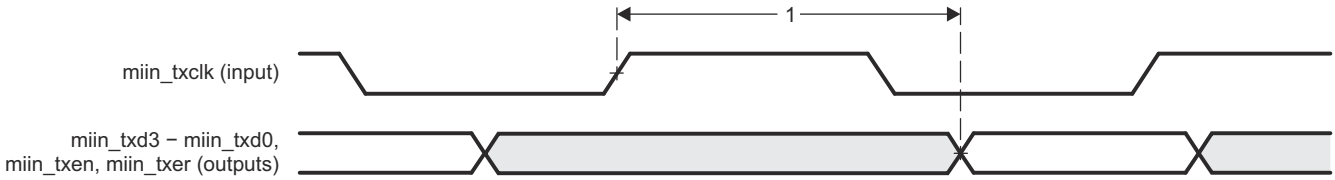

図 7-18. MAC Transmit Interface Timing, MIIn operation

7.12.3.12 MII Receive Clock Timing Requirements

PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
$t_{c(RX_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
		100 Mbps	40		ns
$t_{w(RX_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
		100 Mbps	14	26	ns

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PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
$t_{w(RX_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
		100 Mbps	14	26	ns
$t_{t(RX_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
		100 Mbps		3	ns

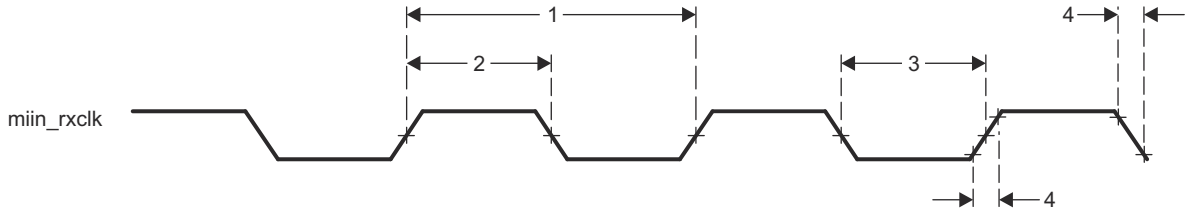

図 7-19. Clock Timing (MAC Receive) - MIIn operation

7.12.3.13 MII Receive Timing Requirements

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{su(RXD-RX_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
$t_{su(RX_DV-RX_CLK)}$				
$t_{su(RX_ER-RX_CLK)}$				
$t_{h(RX_CLK-RXD)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns
$t_{h(RX_CLK-RX_DV)}$				
$t_{h(RX_CLK-RX_ER)}$				

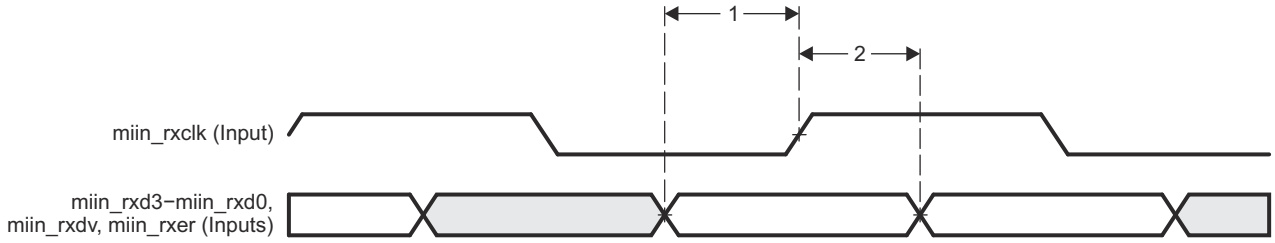

図 7-20. MAC Receive Interface Timing, MIIn operation

7.12.3.14 MII Transmit Clock Timing Requirements

PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
$t_{c(TX_CLK)}$	Cycle time, miin_txclk	10Mbps	400		ns
		100Mbps	40		ns
$t_{w(TX_CLKH)}$	Pulse duration, miin_txclk high	10Mbps	140	260	ns
		100Mbps	14	26	ns
$t_{w(TX_CLKL)}$	Pulse duration, miin_txclk low	10Mbps	140	260	ns
		100Mbps	14	26	ns
$t_{t(TX_CLK)}$	Transition time, miin_txclk	10Mbps		3	ns
		100Mbps		3	ns

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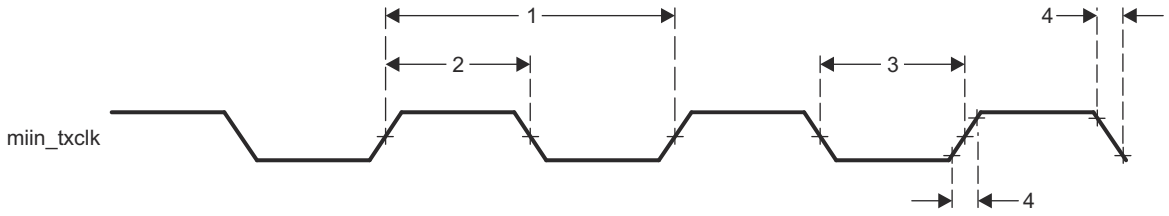

図 7-21. Clock Timing (MAC Transmit) - MIIn operation

7.12.3.15 MDIO Interface Timings

> **注意**
>
> The IO Timings provided in this section are only valid for some MAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

表 7-8, 表 7-9 and 図 7-22 present switching characteristics and timing requirements for the MDIO interface.

表 7-8. Timing Requirements for MDIO Input

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{c(MDC)}$	Cycle time, MDC	40		ns
$t_{w(MDCH)}$	Pulse Duration, MDC High	16		ns
$t_{w(MDCL)}$	Pulse Duration, MDC Low	16		ns
$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	9		ns
$t_{h(MDIO_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

表 7-9. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{t(MDC)}$	Transition time, MDC		3	ns
$t_{d(MDC-MDIO)}$	Delay time, MDC low to MDIO valid	10	(P * 0.5) - 10	ns

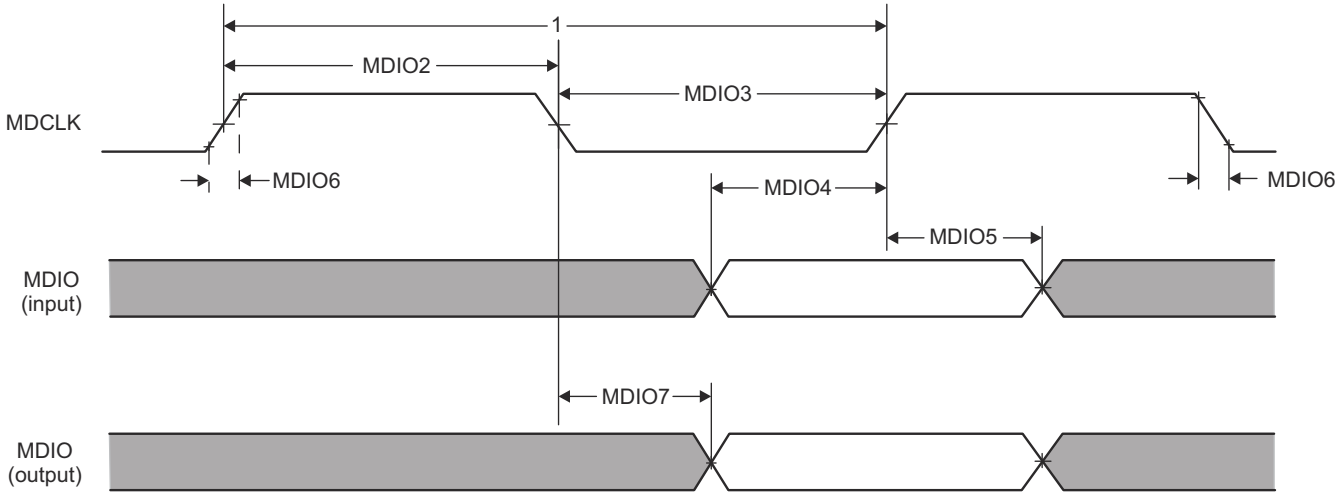

図 7-22. MAC MDIO diagrams

7.12.4 LVDS Instrumentation and Measurement Peripheral

The device supports a set of LVDS interfaces in two different modes.

- Legacy LVDS mode

The LVDS IO are shared between the above two measurement interface options.

Following features are supported :

- 2-data lane LVDS interface (two additional lanes for Data Clock and Frame Clock)

Please see the device TRM for information regarding programming options for LVDS interface.

7.12.4.1 LVDS Interface Configuration

The supported LVDS lane configuration is 2-data lane (LVDS_TXP/M), one Bit Clock lane (LVDS__TXxx_CLKP/M) and one Frame clock lane (LVDS_TXxx_FRCLKP/M). The LVDS interface supports programmable data rates with the maximum being 900 Mbps (450 MHz DDR Clock).

Note that the bit clock is in DDR format and hence the number of toggles in the clock is equivalent to data.

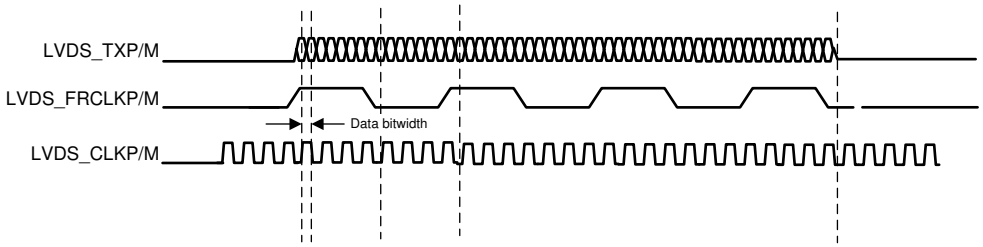

図 7-23. LVDS Interface Lane Configuration And Relative Timings

7.12.4.2 LVDS Interface Timings

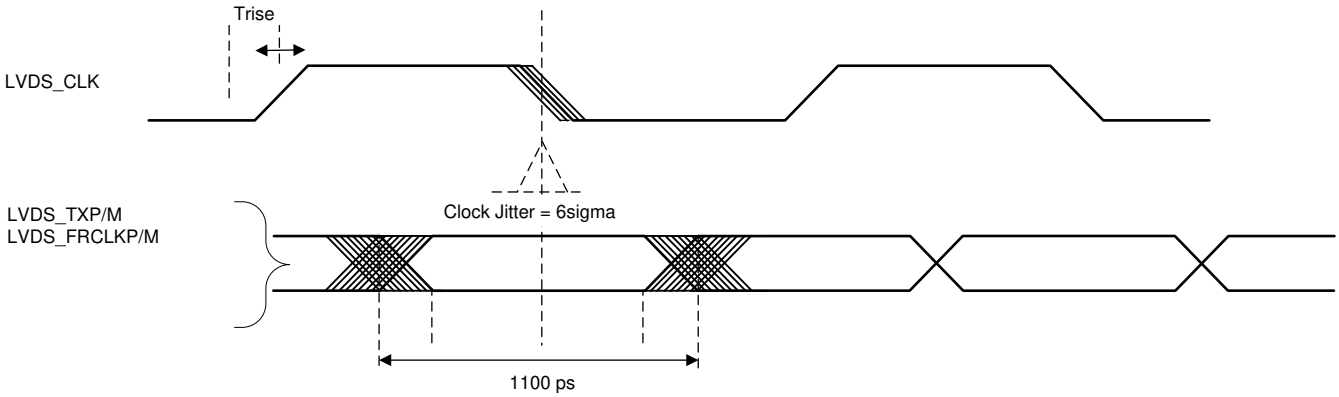

図 7-24. Timing Parameters

表 7-10. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

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7.12.5 UART Peripheral

The device includes two UART interfaces. One UART is intended as a secondary boot loader source and the other one is intended for use as a register debug interface (with XDS110 emulator).

- Maximum baud-rate supported shall be at least 1536kBaud in all the different clock frequency modes
- UART interfaces multiplexed with other I/O to allow for widest peripheral use flexibility

7.12.5.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20pF		921.6		kHz

7.12.6 Inter-Integrated Circuit Interface (I2C)

The device supports one Controller/Target Inter-integrated Circuit interface and is intended to be connected to an external PMIC or EEPROM device (alternative control SPI).

The I2C has the following features:

- Standard/fast mode I2C interface compliant with I2C bus specification (UM10204)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-controller transmitter/ target receiver mode
  - Multi-controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates up to 400kbps
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

注

This I2C module does not support:

- Fast-mode Plus or High speed (Hs)mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

7.12.6.1 I2C Timing Requirements (1)

PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs

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PARAMETER	DESCRIPTION	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$(1)	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

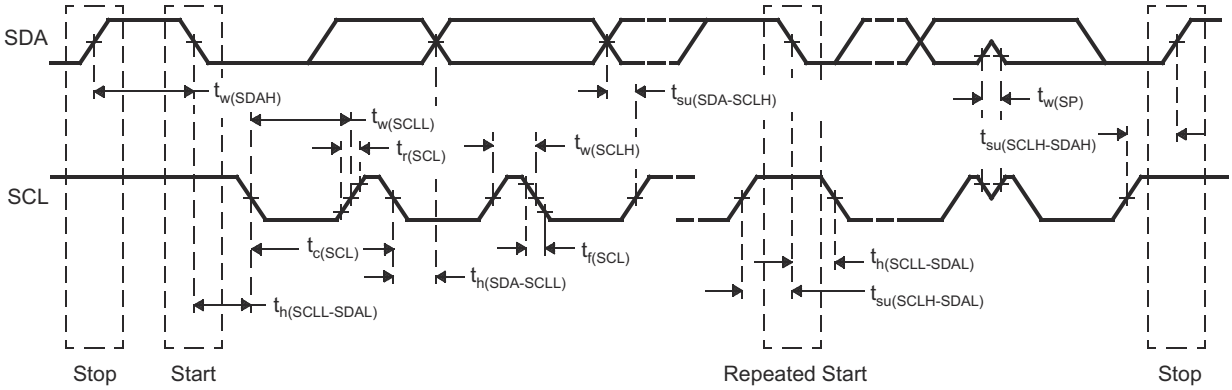

図 7-25. I2C Timing Diagram

注

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

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7.12.7 Enhanced Pulse-Width Modulator (ePWM)

The device includes three Enhanced Pulse-Width Modulation (ePWM) modules. These modules can be used to generate duty-cycled controlled waveforms for a power regulator, or a power management systems, or more complex waveforms for motor control applications.

The module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control for each PWM module
- Each module contains two PWM outputs (EPWMxA and EPWMxB) that shall be usable in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation

7.12.8 General-Purpose Input/Output

セクション 7.12.8.1 lists the switching characteristics of output timing relative to load capacitance.

7.12.8.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L) (1) (2)

PARAMETER	DESCRIPTION	TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

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7.13 Emulation and Debug

7.13.1 Emulation and Debug Description

7.13.2 JTAG Interface

The JTAG interface implements the IEEE1149.1 standard interface for processor debug and boundary scan testing.

セクション 7.13.2.1 and セクション 7.13.2.2 assume the operating conditions stated in 図 7-26.

7.13.2.1 Timing Requirements for IEEE 1149.1 JTAG

表 7-11. JTAG Timing Conditions

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
C_{LOAD}	Output load capacitance	2		15	pF

表 7-12. JTAG Timing Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{c(TCK)}$	Cycle time TCK	33.33			ns
$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	13.33			ns
$t_{w(TCKL)}$	Pulse duration TCK low (40% of tc)	13.33			ns
$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

7.13.2.2 Switching Characteristics for IEEE 1149.1 JTAG

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		21	ns

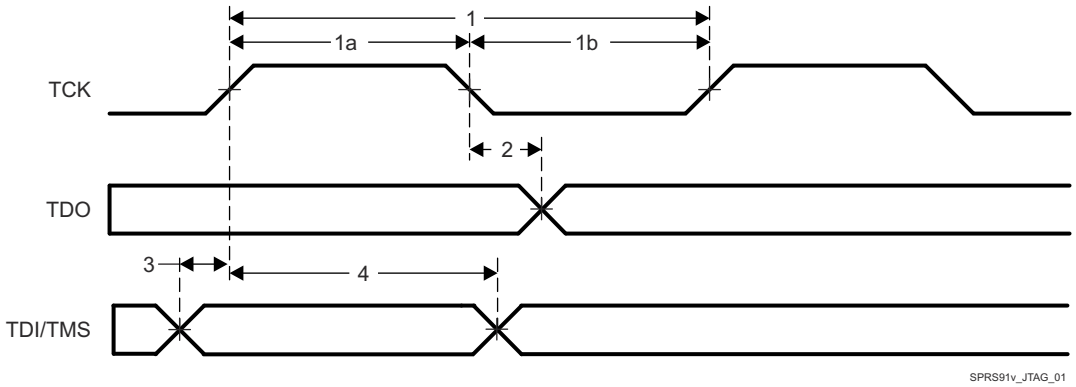

図 7-26. JTAG Timing

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7.13.3 ETM Trace Interface

The ETM Trace interface provides a means of exporting real time processor debug information to a host PC through a compatible emulator toolset.

セクション 7.13.3.1 and セクション 7.13.3.2 describe the operating conditions shown in 図 7-27 and 図 7-28.

7.13.3.1 ETM TRACE Timing Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
C_{LOAD}	Output load capacitance	2		20	pF

7.13.3.2 ETM TRACE Switching Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{cyc(ETM)}$	Cycle time, TRACECLK period	16			ns
$t_{h(ETM)}$	Pulse Duration, TRACECLK High	7			ns
$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	7			ns
$t_{r(ETM)}$	Clock and data rise time			3.3	ns
$t_{f(ETM)}$	Clock and data fall time			3.3	ns
$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		14.5	ns
$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		14.5	ns

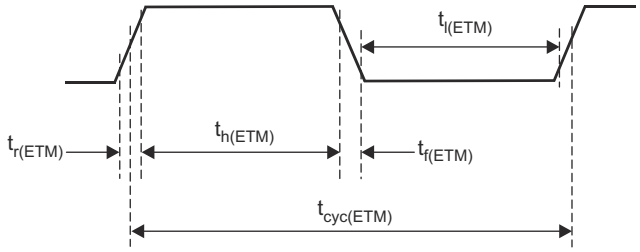

図 7-27. ETMTRACECLKOUT Timing

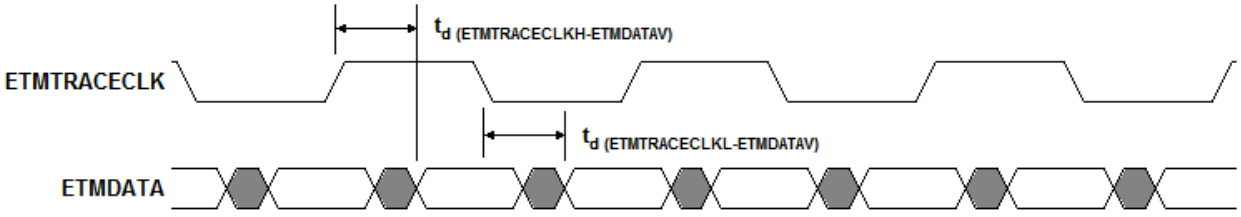

図 7-28. ETMDATA Timing

8 Detailed Description

8.1 Overview

The AWR2544 device includes the entire Millimeter Wave blocks, and analog baseband signal chain, for four transmitters and four receivers, as well as a customer-programmable MCU. The device comes with an additional Launch on package (LOP) antenna feature which facilitates the attachment of antennas directly on to the package..

8.2 Functional Block Diagram

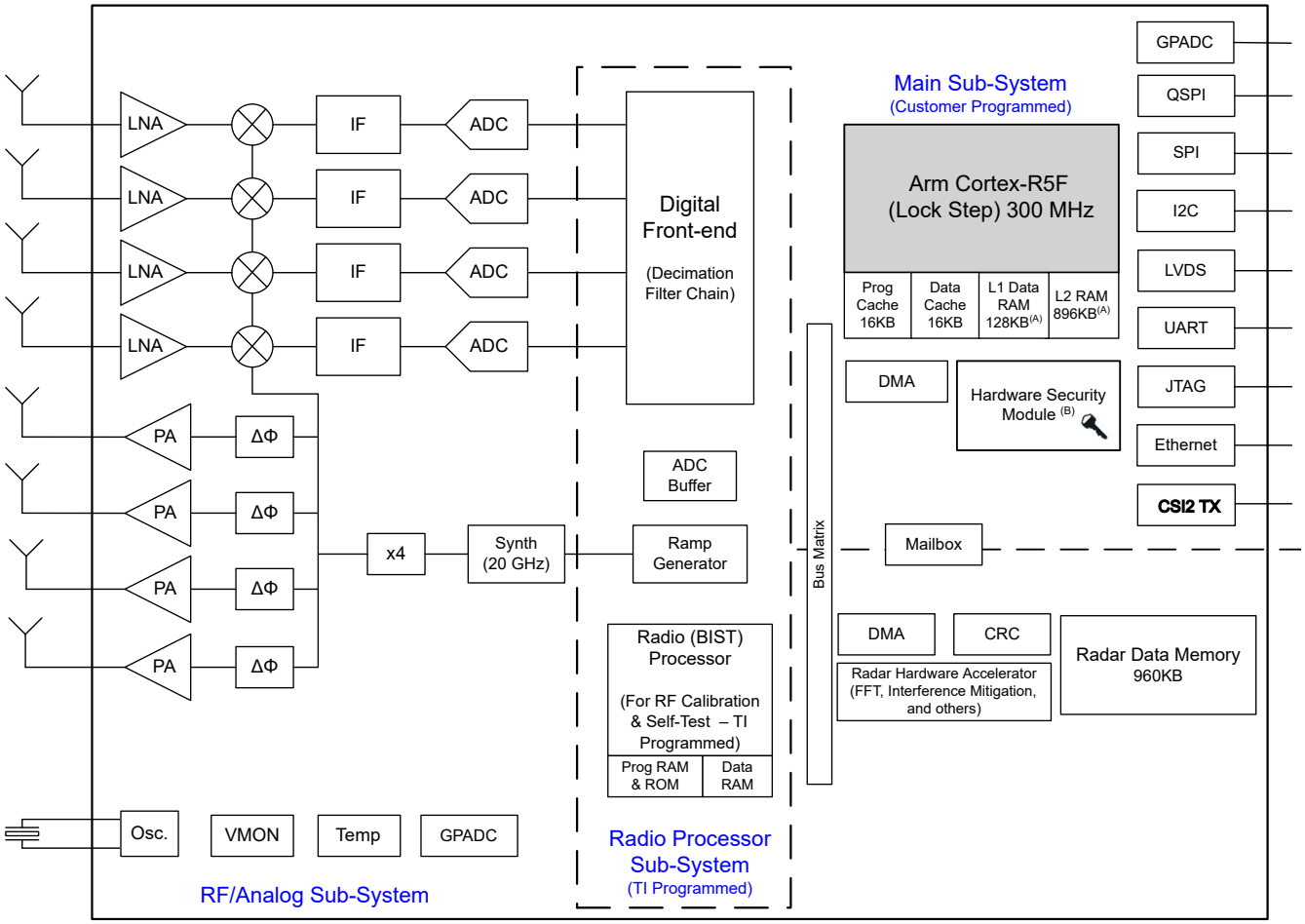

図 8-1. Functional Block Diagram

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8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The four transmit and the receive channels can all be operated simultaneously for transmit beamforming purpose and receiving data as required.

8.3.1.1 RF Clock Subsystem

The device clock subsystem generates 76 to 81GHz from an input reference of 50-MHz crystal. It has a built-in oscillator circuit followed by an Analog PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an x4 multiplier to create the required frequency in the 76 to 81GHz spectrum. The RF synthesizer output can be modulated by the timing engine block to create the required waveforms for effective sensor operation or it can input a fixed signal of 1GHz directly from APLL.

The Analog PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

図 8-2 describes the clock subsystem.

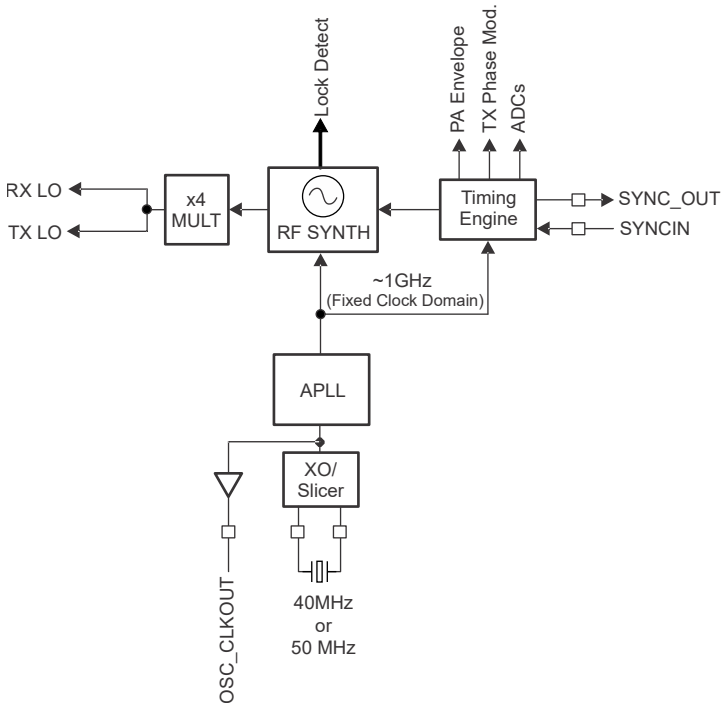

図 8-2. RF Clock Subsystem

8.3.1.2 Transmit Subsystem

The device transmit subsystem consists of four parallel transmit chains, each with independent phase and amplitude control. All four transmitters can be used simultaneously or in time-multiplexed fashion. The device supports binary phase modulation and a 6 bit programmable phase shifter for beamforming control on a per chirp basis for each channel as indicated in the figure below. The transmit chains also support programmable backoff for system optimization.

図 8-3 describes the transmit subsystem.

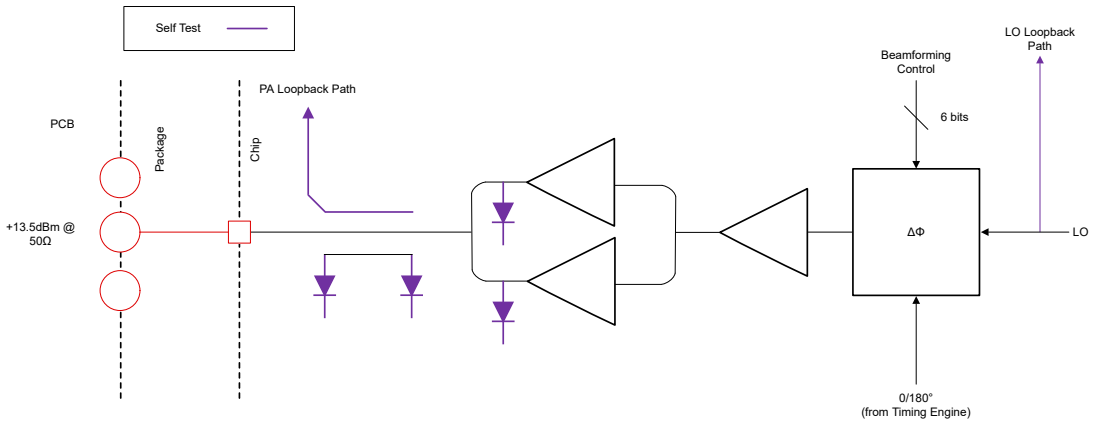

図 8-3. Transmit Subsystem (Per Channel)

8.3.1.3 Receive Subsystem

The device receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can be operational at the same time. An individual power-down option is also available for system optimization.

The device supports a real-only receiver. The band-pass IF chain has configurable cutoff frequencies above 350 kHz and can support bandwidths up to 20MHz.

図 8-4 describes the receive subsystem.

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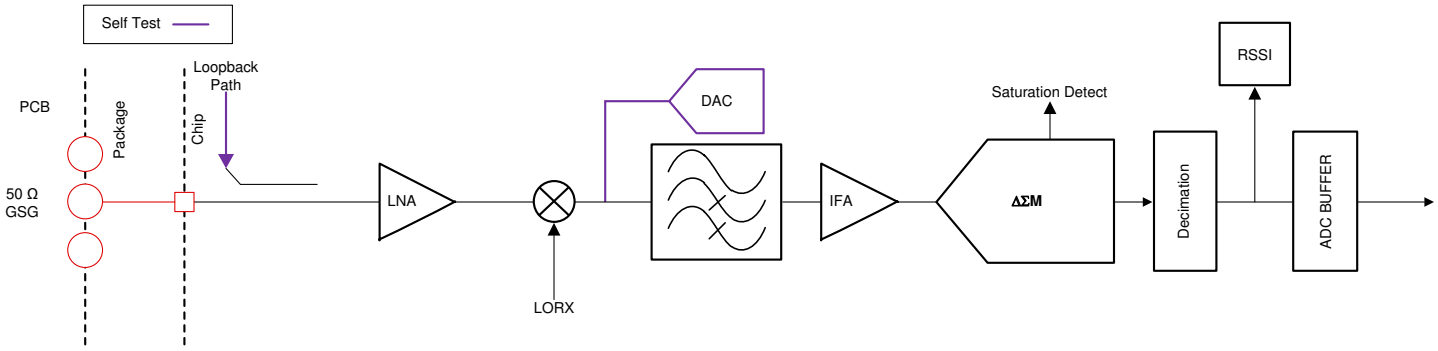

図 8-4. Receive Subsystem (Per Channel)

8.3.2 Processor Subsystem

At a high level there is one customer programmable subsystem. The left hand side shows TI's high performance HWA 1.5, a high-bandwidth interconnect for high performance (128-bit, 150 MHz), and associated peripherals – LVDS interface for Measurement data output, L3 Radar data cube memory, ADC buffers, CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Main subsystem (MSS). The Main subsystem, as the name suggests, is the primary controller of the device and controls all the device peripherals and house-keeping activities of the device. The Main subsystem contains a Cortex-R5F (MSS R5F) processor and associated peripherals and housekeeping components such as EDMAs, CRC, and peripherals (I^2C, UART, SPI, EPWM, and others) connected to the primary interconnect through the Peripheral Central Resource (PCR interconnect).

The Radio Processing Subsystem or the BIST Subsystem (RSS) is responsible for initializing and calibrating the Analog/RF modules. RSS periodically monitors the Analog/RF functionality such that all the Analog/RF modules work in their defined limits.

General-Purpose ADC (GPADC), Fast Fourier Transformation engine (FFT engine) and other modules are provided to monitor the signal from different points in the transmitter and receiver chains. Digital front-end filters (DFE), Ramp Generation module and Analog/DFE registers, which are mainly under the control of BSS, can be indirectly controlled through the API calls from the Main Subsystem.

Refer to the AWR2544 TRM (Technical Reference Manual) for MSS Cortex-R5F.

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8.3.3 Automotive Interfaces

The device communicates with the automotive network over the following main interface:

- Ethernet

8.4 Other Subsystems

8.4.1 Hardware Accelerator Subsystem

The device incorporates Radar Hardware Accelerators (HWA1.5) to compress range FFT data for efficient Ethernet transfer and to offload the central radar processor.

To understand the capabilities offered by the Radar Hardware Accelerator 1.5 so as to achieve the desired functionality, please refer to the Hardware Accelerator 1.5 section in the Device Technical Reference Manual.

8.4.2 Security – Hardware Security Module

A Hardware Security Module (HSM), which performs a secure zone operation, is provisioned in the device (*operational only in select part variants*). A programmable Arm Cortex-M4 core is available to implement the crypto-agility requirements.

The cryptographic algorithms can be accelerated using the hardware modules in the HSM. Functions include acceleration of AES, SHA, and public key accelerator (PKA) to perform math operations for asymmetric key cryptographic requirements and true random number generation.

The Main subsystem (MSS) Cortex-R5F processor interfaces with the HSM subsystem to perform the cryptographic operations required for the secure boot and secure runtime communications.

Further details on Security can be found in the concerned collaterals. Please reach out to your local TI sales representative for more information.

8.4.3 ADC Channels (Service) for User Application

The device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to nine external and internal voltages. The ADC1, ADC2, ADC5, and ADC6 pins are used for this purpose.

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GPADC structures are also used for measuring the output of internal temperature sensors.

GPADC Specifications:

- 625 Ksps SAR ADC
- 0 to 1.8V input range
- 10-bit resolution

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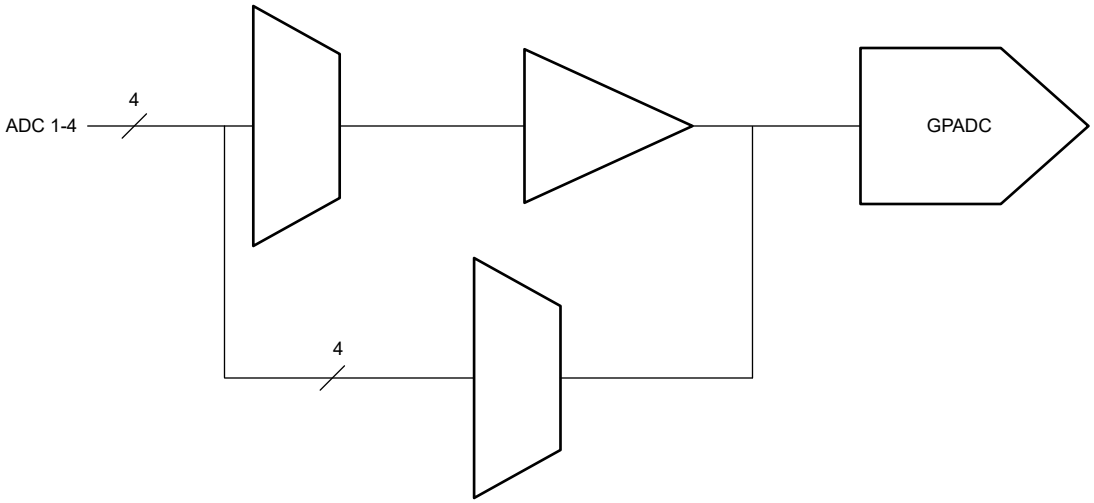

表 8-1. GP-ADC Parameter

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate	625	Ksps
ADC sampling time	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.

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9 Monitoring and Diagnostics

9.1 Monitoring and Diagnostic Mechanisms

表 9-1 is a list of the main monitoring and diagnostic mechanisms available in the device.

表 9-1. Monitoring and Diagnostic Mechanisms for AWR2544

FEATURE	DESCRIPTION
MAIN SUBSYSTEM	
Lockstep operation of MSS R5F Core	Device architecture supports lockstep operation of the MSS R5F core that is the operating core in the Main subsystem that is provisioned as the safety island in the device.
Boot time LBIST For MSS R5F Core and associated VIM	Device architecture supports hardware logic BIST (LBIST) engine self-test Controller (STC). This logic is used to provide a very high diagnostic coverage (>90%) on the MSS R5F CPU core and Vectored Interrupt Module (VIM) at a transistor level. LBIST for the CPU and VIM need to be triggered by application code before starting the functional safety application. A reset of the CPU is initiated at the end of the STC operation and the reset cause register captures the status of reset. The STC registers can then be read out to identify the status of the STC execution to determine if there were any errors. CPU stays there in while loop and does not proceed further if a fault is identified. There can be a fault injection test also performed which leads to a reset of the CPU with the error status signaled in the STC registers.
Boot time PBIST for MSS R5F Memories	MSS R5F has tightly coupled memories (TCM) Level 1 (L1) memories TCMA, TCMB0 and TCMB1 as well as the level 2 (L2) memories. Device architecture supports a hardware programmable memory BIST (PBIST) engine. This logic is used to provide a very high diagnostic coverage (March-13n) on the implemented MSS R5F TCMs at a transistor level. PBIST for L1 and L2 memories is triggered by the bootloader at the boot time before starting download of application from flash or a peripheral interface. The CPU is in a while loop and does not proceed further if a fault is identified.
End to End ECC for MSS R5F Memories	The TCMs and L2 memory diagnostic support a single error correction, double error detection (SECDED) ECC diagnostic. For L2 memory, an 8-bit code word is used to store the ECC data as calculated over the 64-bit data bus. For TCMs, a 7-bit code word is used to store the ECC data for a 32-bit data bus. ECC evaluation for TCMs is done by the ECC control logic inside the CPU. This scheme provides end-to-end diagnostics on the transmissions between CPU and TCM. CPU can be configured to have predetermined response (ignore or abort generation) to single and double bit error conditions.
MSS R5F bit multiplexing	Logical TCM and L2 memory word and the associated ECC code is split and stored in two physical SRAM banks. This scheme provides an inherent diagnostic mechanism for address decode failures in the physical SRAM banks. Faults in the bank addressing are detected by the CPU as an ECC fault. Further, bit multiplexing scheme is implemented such that the bits accessed to generate a logical (CPU) word are not physically adjacent. This scheme helps to reduce the probability of physical multi-bit faults resulting in logical multi-bit faults; rather the faults manifest as multiple single bit faults. As the SECDED TCM ECC can correct a single bit fault in a logical word, this scheme improves the usefulness of the TCM ECC diagnostic. Both these features are hardware features and cannot be enabled or disabled by application software.
Clock Monitor	Device architecture supports four digital clock comparators (EDCCs) and an internal RCOSC. Dual functionality is provided by these modules – clock detection and clock monitoring. EDCCA is dedicated for ADPLL/APLL lock detection monitoring, comparing the ADPLL/APLL output divided version with the Reference input clock of the device. Failure detection for EDCCA can be programmed to cause the device to go into limp mode. Additionally, there is a provision to feed an external reference clock to monitor the internal clock using the EDCCA. EDCCB, EDCCC, EDCCD module is one which is available for user software. Any two clocks can be compared. One example is to compare the CPU clock with the reference or internal RCOSC clock source. Failure detection is indicated to the MSS R5F CPU through the Error Signaling Module (ESM).

表 9-1. Monitoring and Diagnostic Mechanisms for AWR2544 (続き)

FEATURE	DESCRIPTION
RTI/WDT for MSS R5F	Device architecture supports the use of an internal watchdog that is implemented in the real-time interrupt (RTI) module. The internal watchdog has two modes of operation: digital watchdog (DWD) and digital windowed watchdog (DWWD). The modes of operation are mutually exclusive; the designer can elect to use one mode or the other but not both at the same time. Watchdog can issue either an internal (warm) system reset or a CPU non-mask able interrupt upon detection of a failure. The Watchdog is enabled by the bootloader in DWD mode at boot time to track the boot process. When the application code takes control, the watchdog can be configured again for the mode and timings based on the application requirements.
MPU for MSS R5F	The Cortex-R5F CPU includes an MPU. The MPU logic can be used to provide spatial separation of software tasks in the device memory. The Cortex-R5F MPU supports 16 regions. The operating system controls the MPU and changes the MPU settings based on the needs of each task. A violation of a configured memory protection policy results in a CPU abort.
PBIST for Peripheral interface SRAMs - SPI, Ethernet, EDMA, Mailbox	Device architecture supports a hardware programmable memory BIST (PBIST) engine for Peripheral SRAMs as well. PBIST for peripheral SRAM memories can be triggered by the application. User can elect to run the PBIST on one SRAM or on groups of SRAMs based on the execution time, which can be allocated to the PBIST diagnostic. The PBIST tests are destructive to memory contents, and as such are typically run only at boot time. However, the user has the freedom to initiate the tests at any time if peripheral communication can be hindered. Any fault detected by the PBIST results in an error indicated in PBIST status registers.
ECC for Peripheral interface SRAMs – SPI, Ethernet, EDMA, Mailbox	Peripheral interface SRAMs diagnostic is supported by Single error correction double error detection (SECDED) ECC diagnostic. When a single or double bit error is detected, the MSS R5F is notified via ESM (Error Signaling Module). This feature is disabled after reset. Software must configure and enable this feature in the peripheral and ESM module. ECC failure (both single bit corrected and double bit uncorrectable error conditions) is reported to the MSS R5F as an interrupt via ESM module.
Configuration registers protection for Main SS peripherals	All the Main SS peripherals (SPI, Ethernet, I2C, DMAs, RTI/WD, DCCs, EDMA, IOMUX etc.) are connected to interconnect via Peripheral Central resource (PCR). This provides two diagnostic mechanisms that can limit access to peripherals. Peripherals can be clock gated per peripheral chip select in the PCR. This can be utilized to disable unused features such that the features cannot interfere. In addition, each peripheral chip select can be programmed to limit access based on privilege level of transaction. This feature can be used to limit access to entire peripherals to privileged operating system code only. These diagnostic mechanisms are disabled after reset. Software must configure and enable these mechanisms. Protection violation also generates an error that result in abort to MSS R5F or error response to other hosts such as DMAs.
Cyclic Redundancy Check–Main SS	Device architecture supports hardware CRC engine on Main SS implementing the below polynomials. • CRC16 CCITT – 0x10 • CRC32 Ethernet – 0x04C11DB7 • CRC64 • CRC 32C – CASTAGNOLI – 0x1EDC6F4 The read operation of the SRAM contents to the CRC can be done by CPU or by DMA. The comparison of results, indication of fault, and fault response are the responsibility of the software managing the test.
MPU	Device architecture supports MPUs on certain peripheral ports in the Main SS that include L2 Memory, PCR peripheral access, QSPI access, R5F AXI-peripheral access. This allows configuring access permissions to these key regions in the Main SS. By default, this control resides with the HSM.
MPU for DMAs	Device architecture supports MPUs on Main SS EDMAs. EDMAs also includes MPUs on both read and writes host ports. EDMA MPUs supports 8 regions. Failure detection by MPU is reported to the core as an interrupt via local ESM.
Interconnect ECC	Device architecture supports hardware based ECC protection mechanisms for transfers over the system interconnect. Since code execution includes instruction fetches from memories hosted on the interconnect, the transfers over the interconnect are designed to be safe by a combination of ECC and redundancy based mechanisms. Any failures detected in the transfers are reported over the ESM interface. This mechanism is enabled by default in HW, for R5F CPU SS only.

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表 9-1. Monitoring and Diagnostic Mechanisms for AWR2544 (続き)

FEATURE	DESCRIPTION
Error Signaling Module	When a diagnostic detects a fault, the error must be indicated. The Device architecture provides aggregation of fault indication from internal monitoring/diagnostic mechanisms using a peripheral logic known as the Error Signaling Module (ESM). The ESM provides mechanisms to classify errors by severity and to provide programmable error response. ESM module is configured by customer application code and specific error signals can be enabled or masked to generate an interrupt (Low/High priority) for the MSS R5F CPU. Device supports Nerror output signal (IO) which can be monitored externally to identify any kind of high severity faults in the design which are not be handled by the R5F.
Temperature Sensor	Device architecture supports various temperature sensors at temperature hotspots in digital across the device that can be monitored by the application using an internal GPADC channel.
Voltage Monitors	Device architecture supports monitoring the supply rails connected to the chip, in conjunction with external voltage monitors.
BIST (Within RADAR SUB-SYSTEM)	
NOTE: BIST is handled by the TI firmware. Refer to the mmWave Interface Control Document (as a part of mmWave-MCUPLUS-SDK package) and safety manual for information on safety mechanisms.	

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Refer to the Device Safety Manual or other relevant collaterals for more details on applicability of all diagnostics mechanisms.

10 Applications, Implementation, and Layout

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Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Key device features driving the following applications are:

- Integration of Radar Front End and Programmable MCU
- Launch on Package (LOP) Antenna Interface
- Flexible boot modes: Autonomous application boot using a serial flash or external boot over SPI
- Hardware Security Module
- High speed up to 1Gbps Fast Ethernet Support

10.2 Short and Medium Range Radar

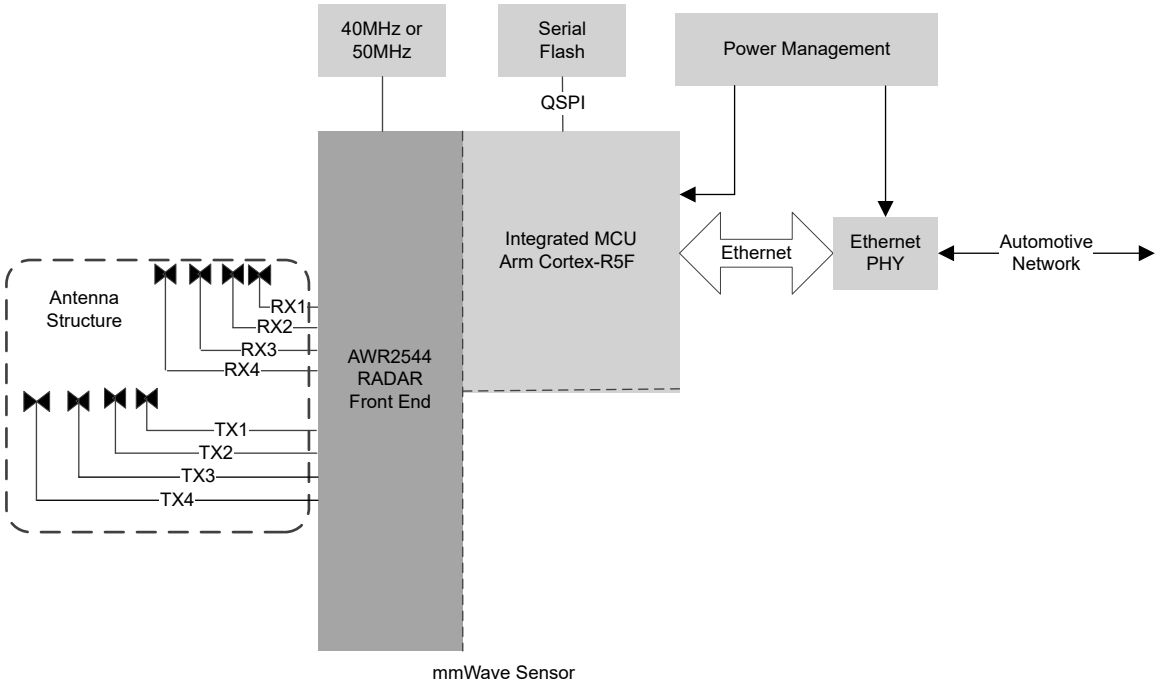

図 10-1. Short- and Medium-Range Radar

10.3 Reference Schematic

For reference schematics and power supply information, please contact TI Representative for access.

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *XA2944PBDALT*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *your package*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *your device speed range*). Figure x provides a legend for reading the complete device name for any *your device* device.

For orderable part numbers of *your device* devices in the *your package* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

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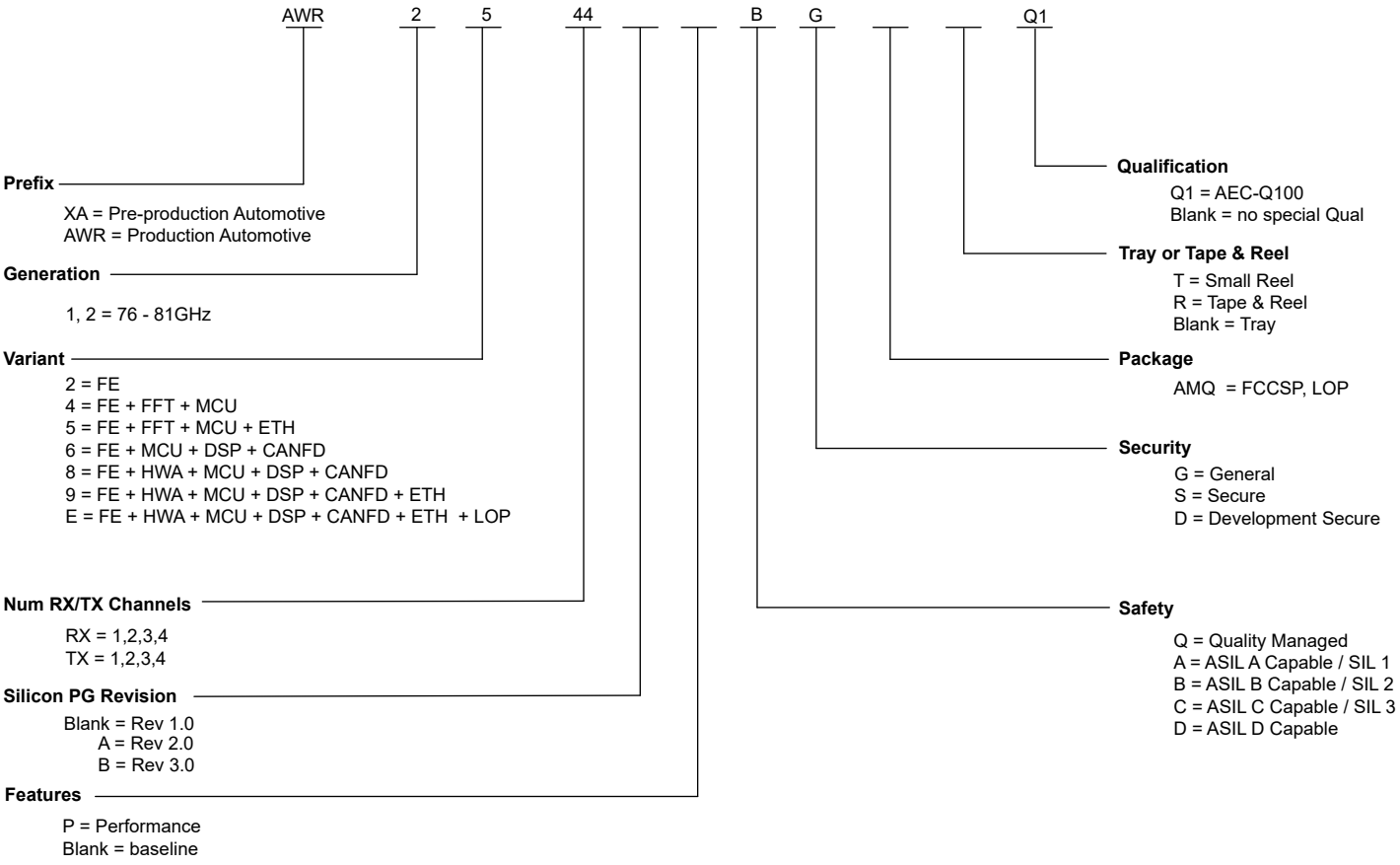

図 11-1. Device Nomenclature

11.3 Tools and Software

The contents in this section will be updated in subsequent versions.

11.4 Documentation support

The contents in this section will be updated in subsequent versions.

11.5 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

Changes from November 30, 2024 to December 30, 2024 (from Revision A (November 2024) to Revision B (December 2024)) **Page**

- *(概要) :*デバイスの説明の表から x マークが付いた OPN を削除 ... 2
- *(Signal Descriptions - Digital) :* Add A7 and B11 to MSS_EPWMA_SYNCO table entry ... 27
- *(Recommended Operating Conditions for OTP eFuse Programming) :* Updated with information on maximum duration of VPP supply ... 37
- *(Power Consumption Summary_LOP) :* Updated TBD values ... 39
- *(RF Specifications) :* Updated Noise Figure, In-band P1dB vs Receiver Gain ... 40
- *(RGMII RX and TX Timing Diagrams) :* Added RGMII RX and TX Timing Diagrams Section ... 55
- *(RGMII RX and TX Timing Diagrams) :* Updated table with RX and TX delay information ... 55
- *(RGMII Receive Data and Control Timing Requirements):* Updated from 1ns to 1.25ns hold and setup time 56
- *(Device Nomenclature) :* Updated Device Nomenclature ... 77

Changes from January 1, 2024 to November 30, 2024 (from Revision * (January 2024) to Revision A (November 2024)) **Page**

- (特長):パワー マネージメント ソリューションに関する推奨事項を追加 ... 1
- *(概要) :*ES2.0 シリコンの受注可能な部品番号 (OPN) を更新。 ... 2
- *(概要) :*デバイスの説明の表から x マークが付いた OPN を削除 ... 2
- *(機能ブロック図) :*図を更新し、脚注を削除。 ... 4
- *(Device Comparison) :* Updated the table for AWR2243. ... 6
- *(Signal Descriptions - Digital) :* Corrected descriptions for MSS_RGMII_RDx pins ... 27
- *(Signal Descriptions - Digital) :* Added a table-note for usage of MSS_MIBSPIB signals ... 27
- *(Signal Descriptions - Digital) :* Removed pins C20 and B20 from TRACE_CLK and TRACE_CTL ... 27
- *(Recommended Operating Conditions) :* Updated MAX values for 1.2V digital and SRAM supply; and 1.8V supply ... 36
- *(VPP Specifications) - Warranty Impact :* Rephrased section ... 37
- *(Power Supply Specification)* : Added Supply Ripple specs ... 38
- *(Power Supply Specification)* : Added recommendations on power management solutions ... 38
- *(Power Consumption Summary) :* Updated the Max peak current numbers for 1.2V and 1.8V respectively from 2100mA and 600mA to 2000mA and 550mA in Table - *Maximum Current Ratings at Power Terminals* for ES2.0 silicon ... 39
- *(Power Consumption Summary) :* Updated the Description conditions and power numbers in Table - *Average Power Consumption at Power Terminals* for ES2.0 silicon ... 39
- *(RF Specifications) :* Improved Typical 1-dB compression point (Out Of Band) from -11dBm to -8dBm in ES2.0 silicon ... 40
- *(RF Specifications) :* Updated table-notes for 1-dB compression point (Out Of Band) measurement technique and a new note added for VCO2 range ... 40

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- *(RF Specifications) :* Updated Noise Figure, In-band P1dB vs Receiver Gain figure in the section.....40
- *(RF Specifications) :*Corrected IF BW to 20MHz.....40
- *(Clock Specifications):* Updated/Changed "Crystal Electrical Characteristics (Oscillator Mode)" to reflect correct device operating temperature range.....43
- *(QSPI Timing Conditions) :* Updated the Output load capacitance from 2pF to 5pF.....44
- *(QSPI Timing Requirements) :* Updated the Setup time (Q12 and Q14) from 13.2ns to 5 ns.....44
- *(QSPI Switching Characteristics):* Updated/Changed *Cycle time, sclk* from 15ns to 12.5ns; 44
- *(QSPI Switching Characteristics):* Updated/Changed *Pulse duration, sclk i.e. [Q2, Q3]* from 0.5*P – 1.5 to 0.5*P – 0.625 (Min). 44
- *(QSPI Switching Characteristics):* Updated/Changed *Delay time, sclk falling edge to d[0] transition i.e. [Q6, Q9]* from 5.5ns to 2ns (Max) and -2.5ns to -4.5ns (Min). 44
- *(SPI Timing Conditions):* Updated/Changed C_{LOAD}*, Output load capacitance* from 15pF to 20pF (Max). 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =0):* Updated/Changed *Cycle time, SPICLK* from 40ns to 20ns; 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =0):* Updated/Changed *Pulse duration, SPICLK i.e. [Q2, Q3]* from $0.5t_{c(SPC)M}$ +- 4 to $0.5t_{c(SPC)M}$ +- 2(Min/Max). 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =0):* Updated/Changed *Delay time, SPISIMO valid before SPICLK low, i.e. [Q4]* from $0.5t_{c(SPC)M}$ – 14 to $0.5t_{c(SPC)M}$ – 7 (Min). 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =0):* Updated/Changed *Valid time, SPISIMO data valid after SPICLK low, i.e. [Q5]* from $0.5t_{c(SPC)M}$ – 18 to $0.5t_{c(SPC)M}$ – 8 (Min). 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =0):* Updated/Changed *Hold time, SPISOMI data valid after SPICLK i.e. [Q9]* from 3ns to 2ns (Min). 46
- *(SPI Controller Mode Switching Parameters, Clock Phase =1):* Updated/Changed *Cycle time, SPICLK* from 40ns to 20ns; 49
- *(SPI Controller Mode Switching Parameters, Clock Phase =1):* Updated/Changed *Pulse duration, SPICLK i.e. [Q2, Q3]* from $0.5t_{c(SPC)M}$ +- 4 to $0.5t_{c(SPC)M}$ +- 2(Min/Max). 49
- *(SPI Controller Mode Switching Parameters, Clock Phase =1):* Updated/Changed *Delay time, SPISIMO valid before SPICLK low, i.e. [Q4]* from $0.5t_{c(SPC)M}$ – 14 to $0.5t_{c(SPC)M}$ – 7 (Min). 49
- *(SPI Controller Mode Switching Parameters, Clock Phase =1):* Updated/Changed *Valid time, SPISIMO data valid after SPICLK low, i.e. [Q5]* from $0.5t_{c(SPC)M}$ – 18 to $0.5t_{c(SPC)M}$ – 8 (Min). 49
- *(SPI Controller Mode Switching Parameters, Clock Phase =1):* Updated/Changed *Hold time, SPISOMI data valid after SPICLK i.e. [Q9]* from 3ns to 2ns (Min). 49
- *(SPI Peripheral Mode Switching Parameters):* Updated/Changed *Cycle time, SPICLK* from 50ns to 20ns; .51
- *(SPI Peripheral Mode Switching Parameters):* Updated/Changed *Pulse duration, SPICLK i.e. [Q2, Q3]* from 20ns to 8ns (Min). 51
- *(SPI Peripheral Mode Switching Parameters):* Updated/Changed *Setup time, SPISIMO before SPICLK i.e. [Q6]* from 6ns to 2.1ns (Min). 51
- Updated RGMII/RMII/MII Timing Conditions.....53
- *(RGMII Receive Data and Control Timing Requirements):* Updated/Changed *Hold time, i.e. [No. 6]* from 4.5ns to 1ns (Min). 56
- *(RMII Transmit Data and Control Switching Characteristics):* Updated/Changed *Delay time, REF_CLK high to selected transmit signals valid, i.e. [RMII 11]* from 3ns to 2ns (Min). 56
- *(MII Transmit Switching Characteristics):* Updated/Changed *Delay time, miin_txclk to transmit selected signals valid, i.e. [No. 1]* from 3ns to 0ns (Min). 57
- *(LVDS Interface Configuration) :* Corrected a typo for the number of data lanes in LVDS from '4' to '2'.....60
- *(Switching Characteristics for IEEE 1149.1 JTAG):* Updated/Changed *Delay time, TCK low to TDO valid, i.e. [No. 2]* from 27.1ns to 21ns (Max). 64
- Updated BW to 20MHz.....68
- *(ADC Channels (Service) for User Application)*: Added a figure in the section.....71
- *(Monitoring and Diagnostic Mechanisms)*: Updated the section and added a note for reference to safety related collateral. 73
- *(Monitoring and Diagnostic Mechanisms)*: Removed CRC-8 support since polynomials are not supported in the Design.....73

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- Added package to device nomenclature..... 77

DATE	REVISION	NOTES
January 2024	*	Initial Release

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

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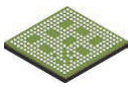
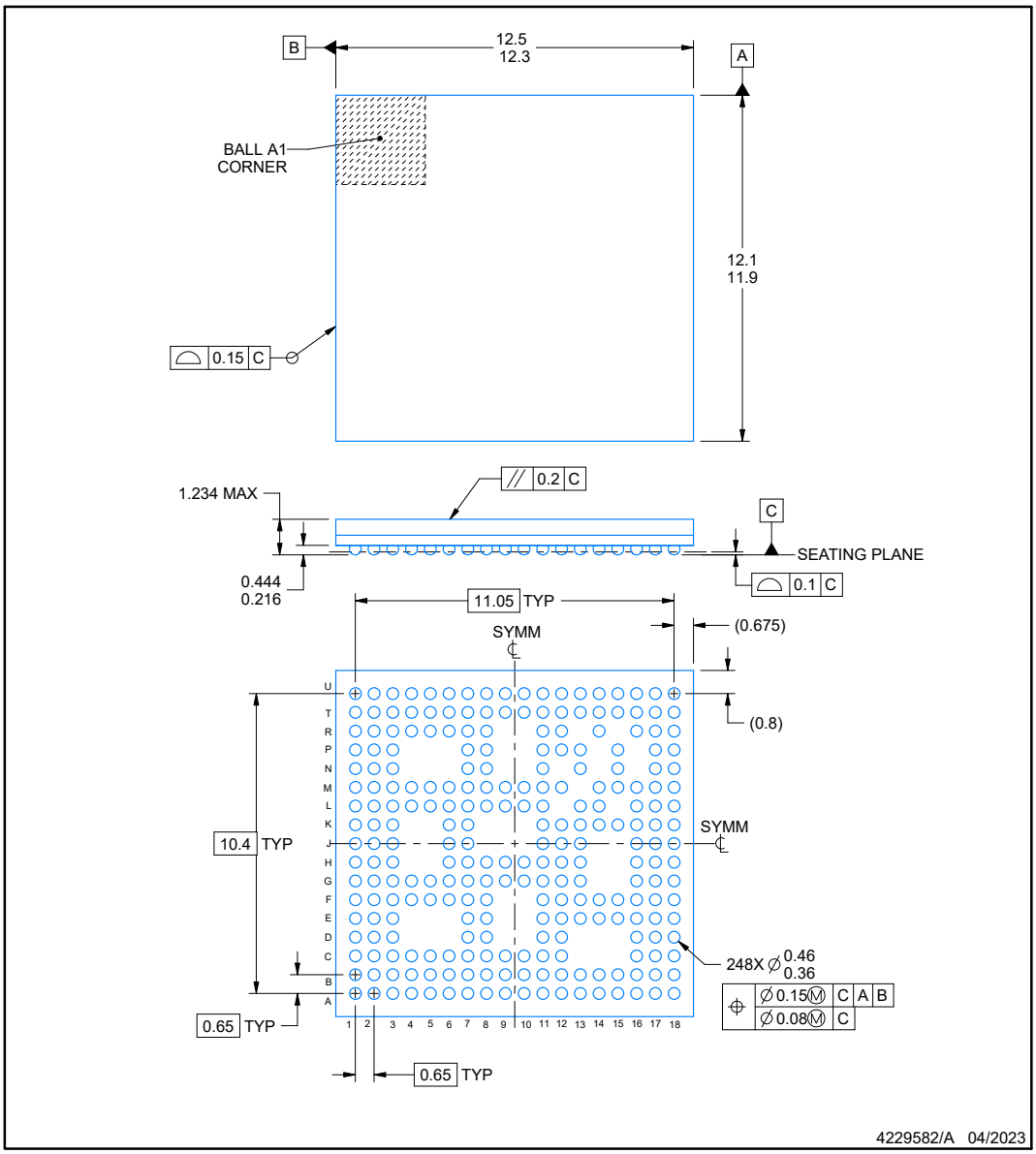
PACKAGE OUTLINE

AMQ0248A



FCCSP - 1.234 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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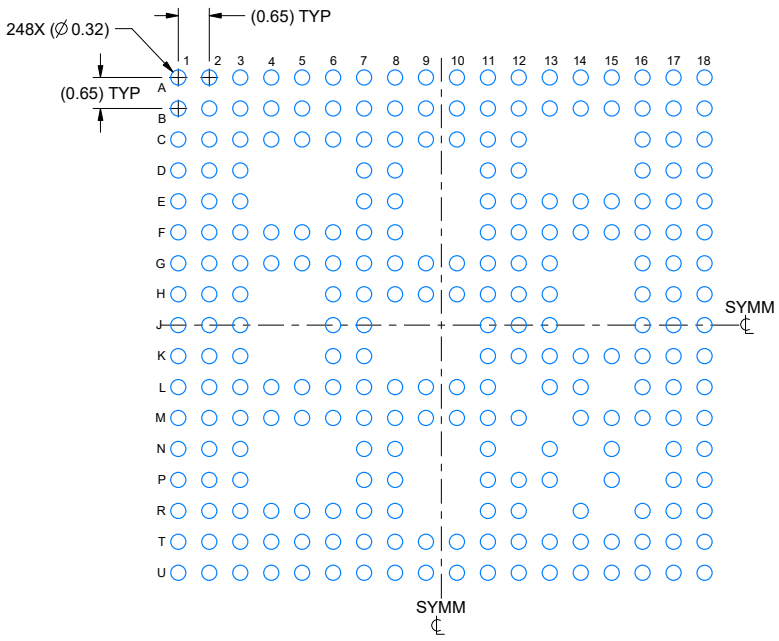
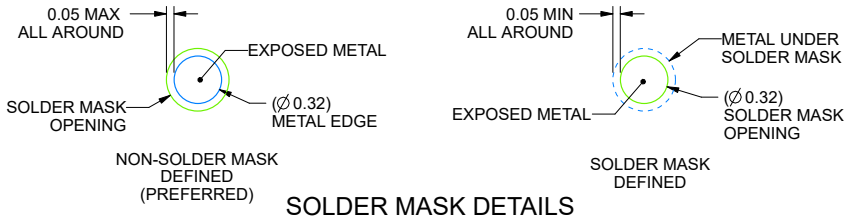
EXAMPLE BOARD LAYOUT

AMQ0248A — **FCCSP - 1.234 mm max height**

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

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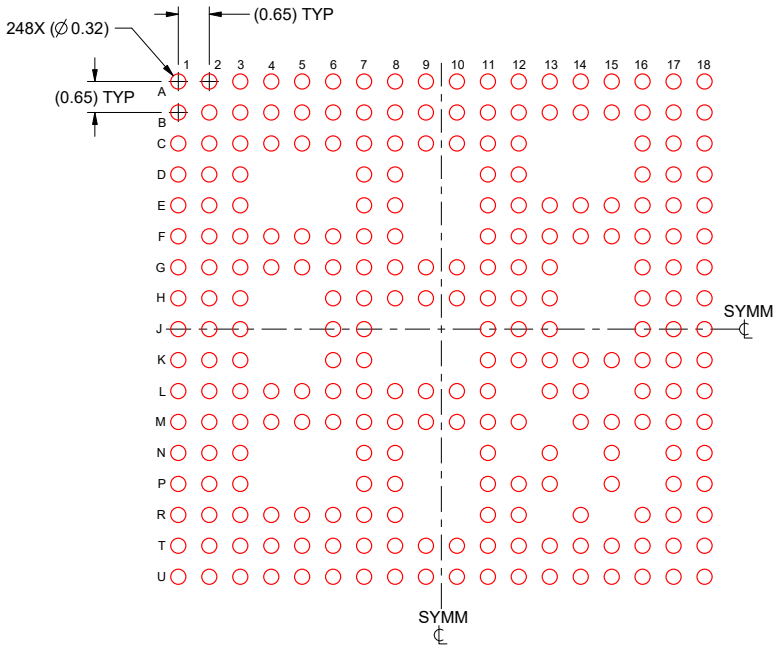
EXAMPLE STENCIL DESIGN

AMQ0248A — **FCCSP - 1.234 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AWR2544BGAMQQ1	Active	Production	FCCSP (AMQ) | 248	147 | JEDEC TRAY (5+1)	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2544 BG 585
AWR2544BGAMQRQ1	Active	Production	FCCSP (AMQ) | 248	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2544 BG 585
AWR2544BGAMQRQ1.B	Active	Production	FCCSP (AMQ) | 248	1000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 140	AWR2544 BG 585

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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最終更新日：2025 年 10 月