UNITRODE

bq2011

Gas Gauge IC for High Discharge Rates

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011 Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011 is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and selfdischarge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the PFC and MODE pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

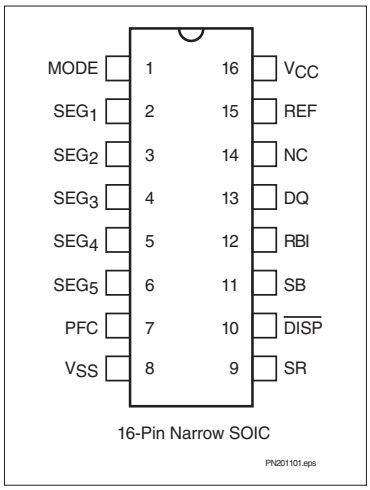
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to indicate graphically the nominal available charge.

The bq2011 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011 outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011 gas gauge data registers.

The bq2011 may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



Pin Names

MODE	Display mode output	NC	No connect
SEG_1	LED segment 1	DQ	Serial communications input/output
SEG_2	LED segment 2	RBI	Register backup input
SEG_3	LED segment 3	SB	Battery sense input
SEG_4	LED segment 4	$\overline{DISP}$	Display control input
SEG_5	LED segment 5	SR	Sense resistor input
PFC	Programmed full count selection input	V_{CC}	3.0–6.5V
REF	Voltage reference output	V_{SS}	Negative battery terminal

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Pin Descriptions

MODE **Display mode output**

When left floating, this output selects relative mode for capacity display. If connected to the anode of the LEDs to source current, absolute mode is selected for capacity display. See Table 1.

SEG_1–SEG_5 **LED display segment outputs**

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

PFC **Programmed full count selection input**

This three-level input pin defines the programmed full count (PFC) thresholds and scale selections described in Table 1. The state of the PFC pin is only read immediately after a reset condition.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011 is $V_{SR} + V_{OS}$ (see Table 3).

NC **No connect**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI **Register backup input**

This input is used to provide backup potential to the bq2011 registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2011 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011 using the LED display with absolute mode as a charge-state indicator. The bq2011 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

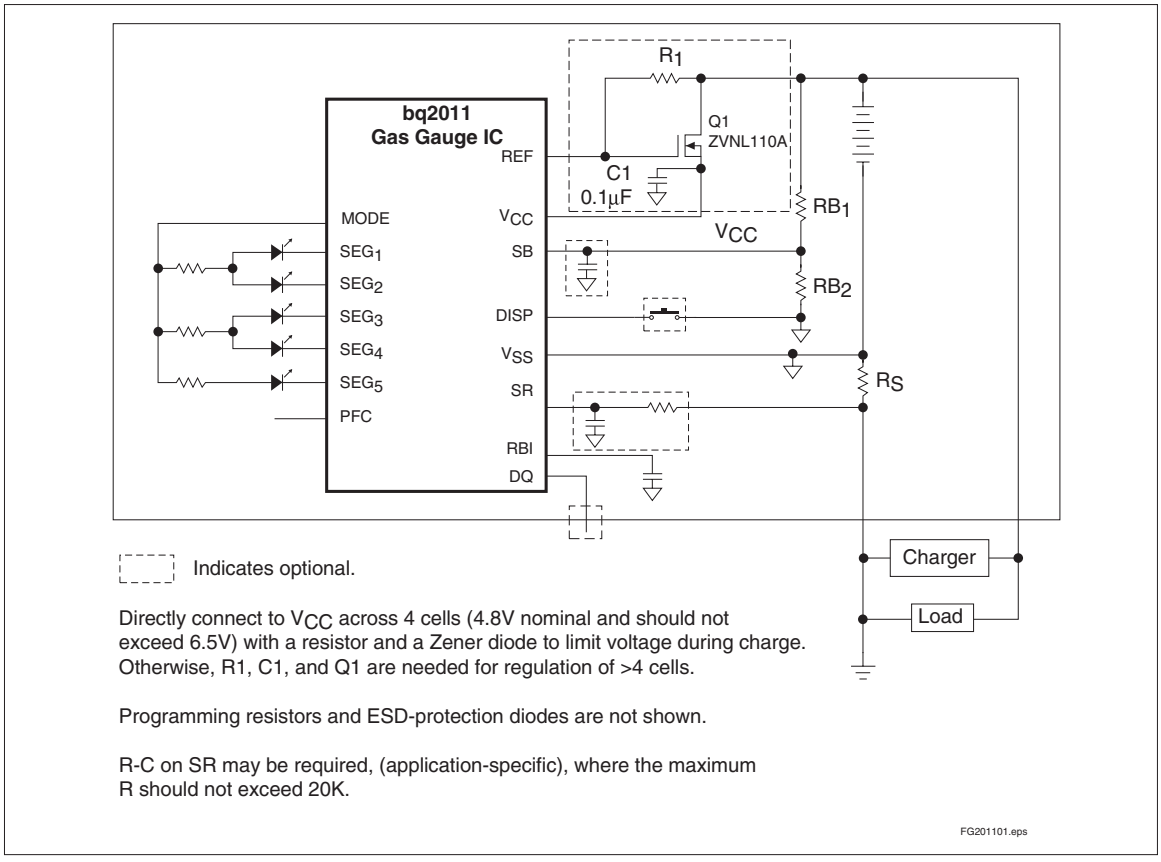


Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011 RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011 registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011 checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011 are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

During discharge and charge, the bq2011 monitors V_{SR} for various thresholds, V_{SR1}–V_{SR4}. These thresholds are used to compensate the charge and discharge rates. Refer to the discharge compensation section for details. EDV monitoring is disabled if $V_{SR} \geq V_{SR1}$ (50mV typical) and resumes 1 second after V_{SR} drops back below V_{SR1}.

Reset

The bq2011 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2011 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011. The bq2011 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011 is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) $*$ sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

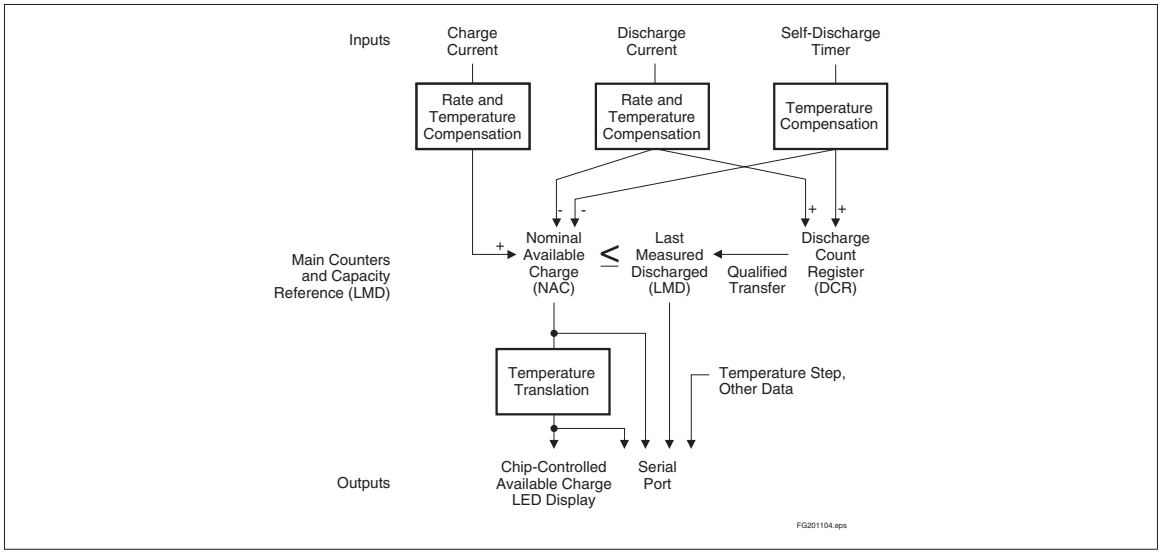


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.005Ω
Number of cells = 6
Capacity = 1300mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = $\frac{6}{64}$
Voltage drop over sense resistor = 5mV to 400mV

Therefore:

1300mAh ∗ 0.005Ω = 6.5mVh

Select:

PFC = 34304 counts or 6.5mVh
PFC = Z (float)
MODE = not connected

The initial full battery capacity is 6.5mVh (1300mAh) until the bq2011 "learns" a new capacity with a qualified discharge from full to EDV.

Table 1. bq2011 Programmed Full Count mVh Selections

PFC	Programmed Full Count (PFC)	mVh	Scale	MODE Pin	Display Mode
H	27648	10.5	$\frac{1}{2640}$	Floating	Relative
Z	34304	6.5	$\frac{1}{5280}$		
L	44800	8.5	$\frac{1}{5280}$		
H	42240	8.0	$\frac{1}{5280}$	Connected to LEDs	Absolute
Z	31744	6.0	$\frac{1}{5280}$		
L	23808	4.5	$\frac{1}{5280}$		

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

   Note: NAC is set to the value in LMD when SEG_5 is pulled low during a reset.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   - No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011 determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{80}$ * NAC rate per day. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2011 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<40°C	0.80	0.95
≥ 40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} < 50 mV	1.00	100%
V_{SR1} > 50 mV	1.05	95%
V_{SR2} > 100 mV	1.15	85%
V_{SR3} > 150 mV	1.25	75%
V_{SR4} > 253 mV	1.25	75%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and V_{SR} < 50mV.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/80$ * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 2

Table 2. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	$NAC/320$
10–20°C	$NAC/160$
20–30°C	$NAC/80$
30–40°C	$NAC/40$
40–50°C	$NAC/20$
50–60°C	$NAC/10$
60–70°C	$NAC/5$
> 70°C	$NAC/2.5$

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 3. bq2011 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Communicating with the bq2011

The bq2011 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011. The command directs the bq2011 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011 NAC register.

bq2011 Registers

The bq2011 command and status registers are listed in Table 4 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

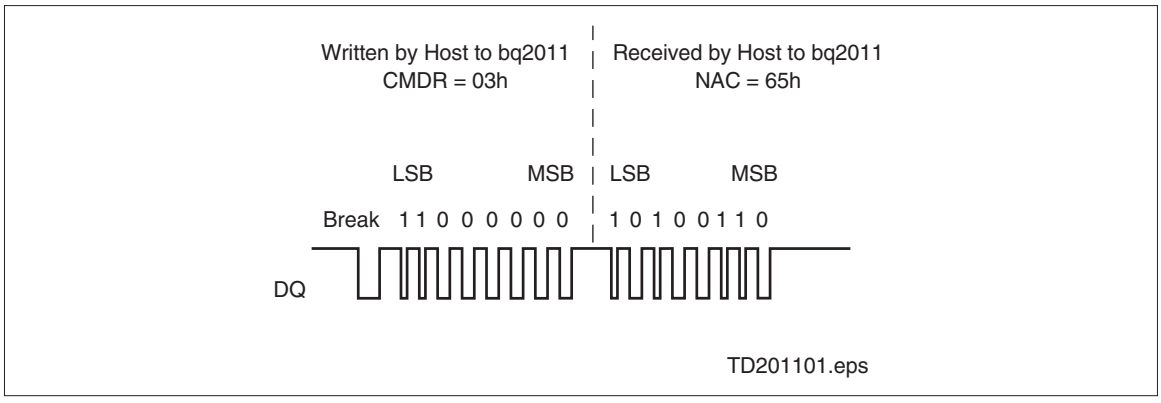


Figure 3. Typical Communication with the bq2011

Table 4. bq2011 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
FULCNT	Full count register	0bh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than-400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011 is reset (see the RST register description). BRP is latched until either the bq2011 is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011 is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge or the bq2011 is reset

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2011 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with V_{SRO} < -400µV.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if $V_{SR} > V_{SR1}$. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that $V_{SR} < V_{SR1}$

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 ∗ NAC / "Full Reference"
< -20°C	0.5 ∗ NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, the NACH and NACL registers are cleared to zero. NACL stops counting when NACH reaches zero. When the bq2011 detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011 gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011 uses as a measured full reference. The bq2011 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011 updates the capacity of the battery. LMD is set to PFC during a bq2011 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} < 50mV
0	0	1	50mV < V_{SR} < 100mV (overload, OVLD=1)
0	1	0	100mV < V_{SR} < 150mV
0	1	1	150mV < V_{SR} < 253mV
1	0	0	V_{SRD} > 253mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SRD} > 50mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SRD} < 50mV.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits $OC_{5–1}$ of the OCTL register (see Table 4 on page 10 for details) is output onto the segment pins, $SEG_{5–1}$, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011 to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011 as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2011.*

Resetting the bq2011 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and OCE = 0 or NAC = LMD when SEG5 = L
- CI and BRP = 1

Display

The bq2011 can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011.

The bq2011 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the $SEG_{1–5}$ outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011 can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011 can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SR1}	Discharge compensation threshold	20	50	75	mV	SR (see note)
V_{SR2}	Discharge compensation threshold	70	100	125	mV	SR (see note)
V_{SR3}	Discharge compensation threshold	120	150	175	mV	SR (see note)
V_{SR4}	Discharge compensation threshold	220	253	275	mV	SR (see note)
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = V_{CC}
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{MODE}	MODE input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data-retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} > V_{SS} = discharge; V_{SR} < V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	PFC logic input high	V_{CC} - 0.2	-	-	V	PFC
V_{ILPFC}	PFC logic input low	-	-	V_{SS} + 0.2	V	PFC
V_{IZPFC}	PFC logic input Z	float	-	float	V	PFC
I_{IHPFC}	PFC input high current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
I_{ILPFC}	PFC input low current	-	1.2	-	µA	V_{PFC} = V_{CC}/2
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	MODE output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHMODE} = -5.25mA
V_{OHMH}	MODE output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHMODE} = -33.0mA
I_{OHMODE}	MODE source current	-33	-	-	mA	At V_{OHMODE} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	PFC

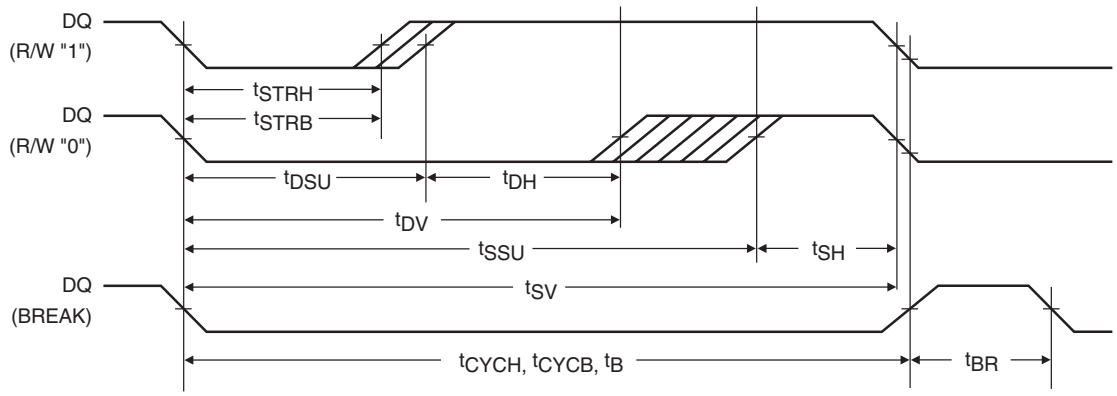
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

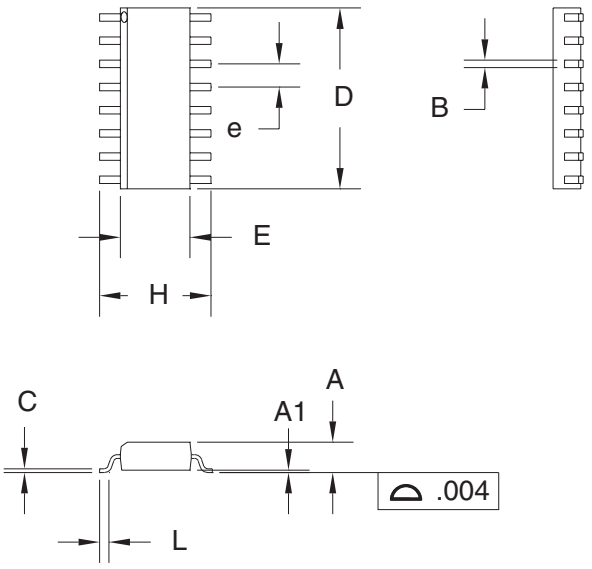
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011	5	-	-	ns	
t_{STRB}	Start hold, bq2011 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

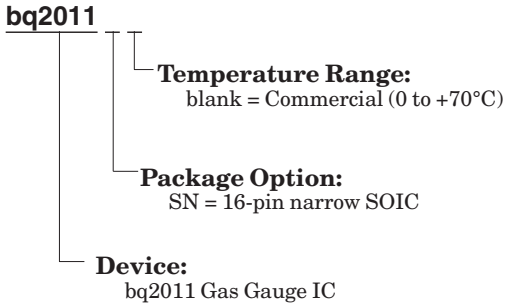
All dimensions are in inches.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	7	Self-discharge count rate	Was: $\frac{1}{64}$ * NAC rate per day Is: $\frac{1}{80}$ * NAC rate per day
3	7	Compensation factor 30–40°C	Was: 0.90 Is: 0.95
3	7	Compensation factor >40°C	Was: 0.80 Is: 0.90
4	7	Charge compensation	Changed compensation factor variation with temperature
4	8	Self-discharge compensation	Changed self-discharge compensation rate variation with temperature

Notes: Changes 1 and 2 = See the *1995 Data Book*.
Change 3 = Jan. 1996 D changes from July 1994 C.
Change 4 = Feb. 1996 E changes from Jan. 1996 D.

Ordering Information



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2011SN-D118TR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2011 D118	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

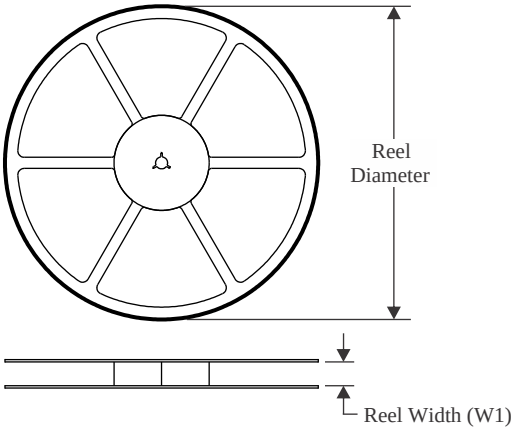
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

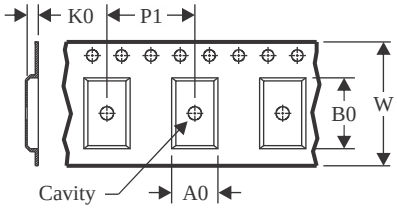
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

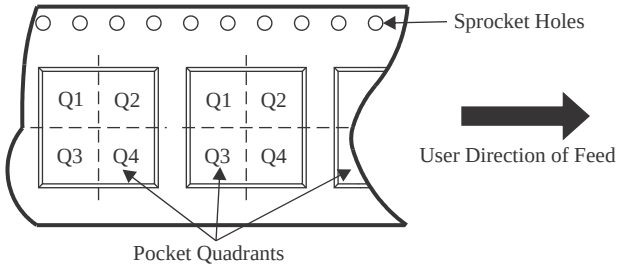


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

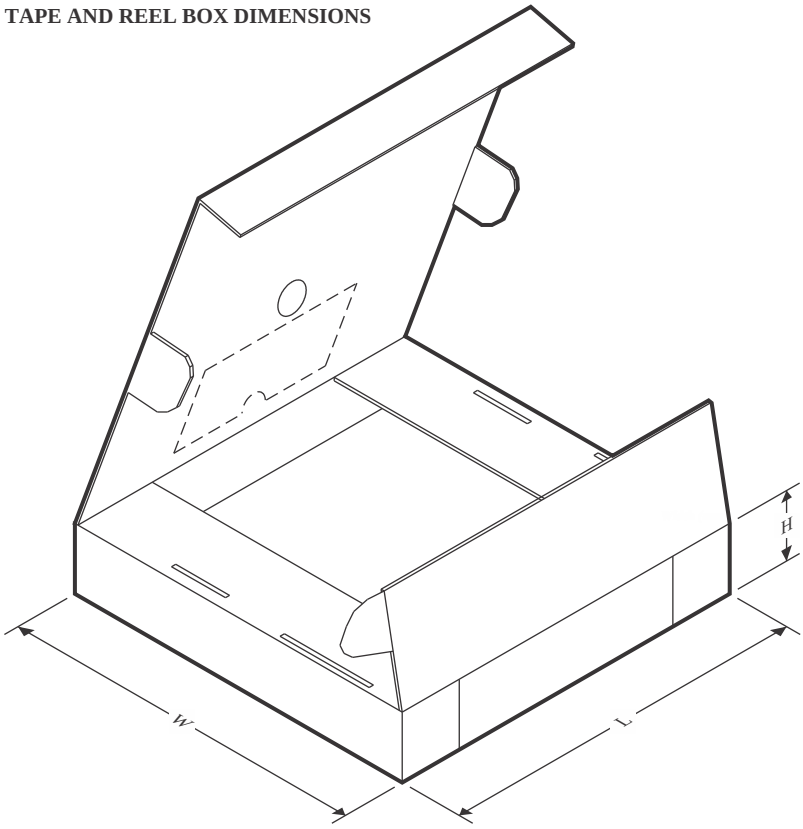
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2011SN-D118TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

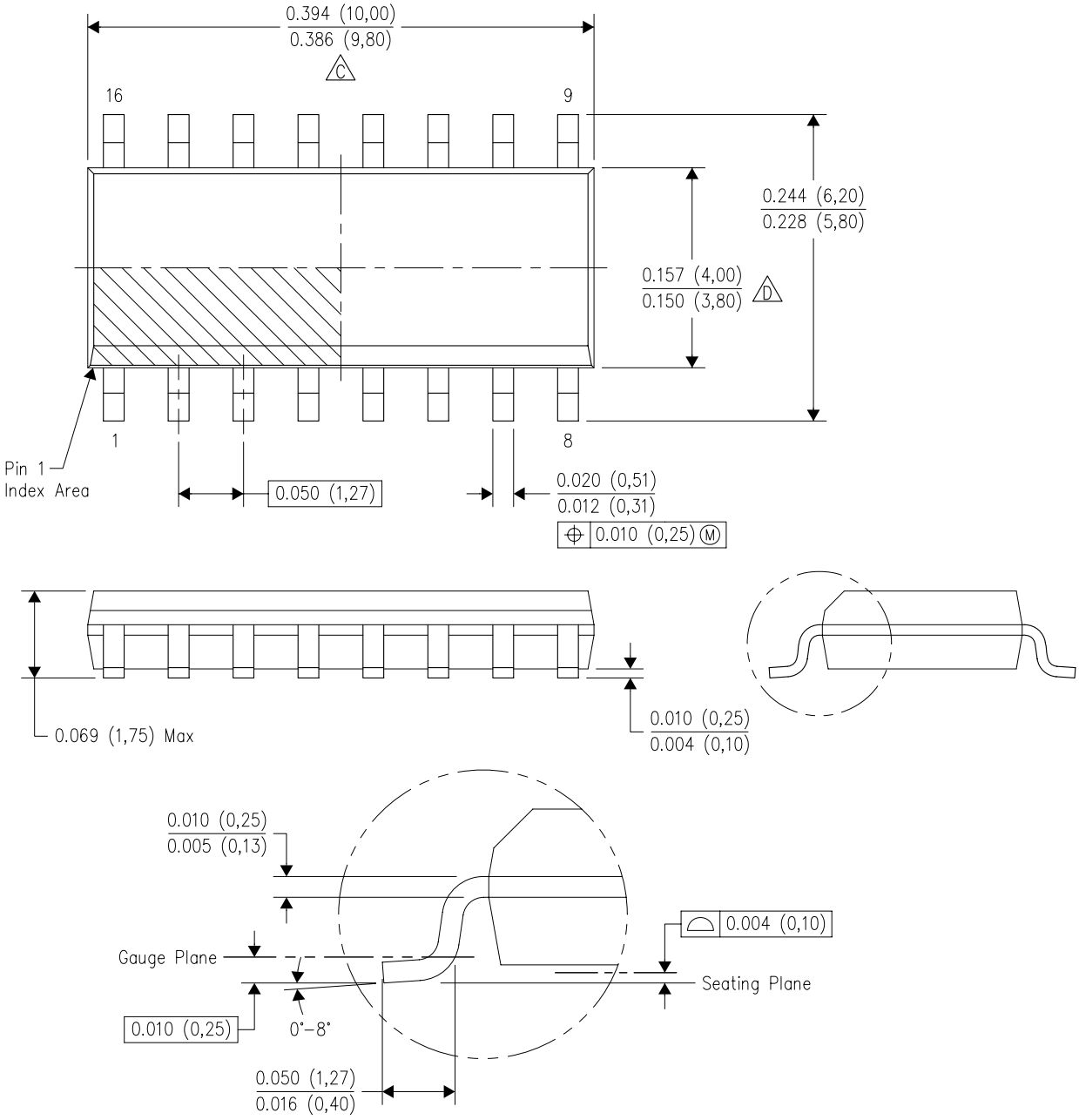
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2011SN-D118TR	SOIC	D	16	2500	356.0	356.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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