TEXAS INSTRUMENTS
BQ24296, BQ24297
JAJSJW8D – SEPTEMBER 2013 – REVISED APRIL 2023

BQ2429x I²C 制御、3A シングル・セル USB チャージャ、Narrow VDC パワー・パス管理および可変電圧 USB OTG 付き

1 特長

- 90% の高効率スイッチ・モード 3A チャージャ
- 6.4V 過電圧保護機能搭載、3.9V～6.2V、シングル入力、USB 準拠チャージャ
  - USB ホストまたは充電ポート D+/D- 検出、USB バッテリ・チャージャ仕様 (BC1.2) に準拠
  - 非標準の 2A/1A アダプタ検出 (BQ24297) をサポート
  - 入力電圧および電流制限は、USB 2.0 および USB 3.0 をサポート
  - 入力電流制限：100mA、150mA、500mA、900mA、1A、1.5A、2A、3A
- 1A または 1.5A で 4.55V～5.5V の出力を調整可能な USB OTG
  - 高速 OTG スタートアップ (標準 22ms)
  - 5V 昇圧モードで 90% の効率
  - 正確な ±15% のヒカップ・モード過電流保護
- Narrow VDC (NVDC) パワー・パス管理
  - バッテリ未接続または深放電状態でもシステムを即時オン
  - バッテリ補助モードで理想ダイオード動作
- 低プロファイルの 1.2mm インダクタ用の 1.5MHz のスイッチング周波数
- 最適なシステム性能とステータス・レポートのための I²C ポート
- ホスト管理あり / なしでの自律的なバッテリ充電
  - バッテリ充電のイネーブルとプリコンディショニング
  - 充電の終了と再充電
- 高精度
  - ±0.5% の充電電圧レギュレーション
  - ±7% の充電電流レギュレーション
  - ±7.5% の入力電流レギュレーション
  - USB OTG 昇圧モードで ±3% の出力電圧レギュレーション
- 高集積
  - パワー・パス管理
  - 同期スイッチング MOSFET
  - 電流センス機能内蔵
  - ブートストラップ・ダイオード
  - ループ補償内蔵
- 安全
  - OTG モードでの充電および放電用のバッテリ温度センシング
  - バッテリ充電安全タイマ
  - サーマル・レギュレーションおよびサーマル・シャットダウン
  - 入力およびシステムの過電圧保護
  - MOSFET の過電流保護
- LED またはホスト・コンピュータ用の充電ステータス出力
- 入力電圧レギュレーションによる最大電力追従機能
- 20µA の小さいバッテリ・リーク電流で出荷モードをサポート
- 4.00mm × 4.00mm の VQFN-24 パッケージ
- 安全関連認証：
  - TUV IEC 62368 認証 (BQ24297)

2 アプリケーション

- タブレット PC、スマートフォン、インターネット・デバイス
- 携帯用オーディオ・スピーカ
- ハンドヘルド・コンピュータ、PDA、POS

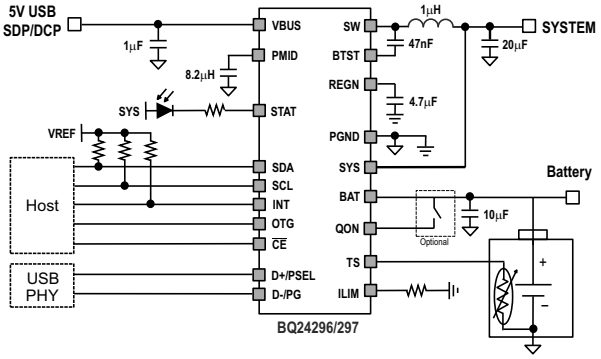
3 概要

BQ24296/BQ24297 は、スマートフォンやタブレットの幅広いアプリケーションで使用される 1 セルのリチウムイオンおよびリチウムポリマ・バッテリ用の、高度に統合されたスイッチモード・バッテリ・チャージャ管理およびシステム・パワー・パス管理デバイスです。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
BQ24296/7	VQFN (24)	4.00mm × 4.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Description (continued) ... 4
6 Device Comparison Table ... 5
7 Pin Configuration and Functions ... 6
8 Specifications ... 8
8.1 Absolute Maximum Ratings(1) ... 8
8.2 ESD Ratings ... 8
8.3 Recommended Operating Conditions ... 8
8.4 Thermal Information ... 9
8.5 Electrical Characteristics ... 9
8.6 Timing Requirements ... 13
8.7 Typical Characteristics ... 13
9 Detailed Description ... 16
9.1 Overview ... 16
9.2 Functional Block Diagram ... 17
9.3 Feature Description ... 18
9.4 Device Functional Modes ... 30
9.5 Programming ... 31
9.6 Register Map ... 35
10 Application and Implementation ... 43
10.1 Application Information ... 43
10.2 Typical Application ... 43
11 Power Supply Recommendations ... 48
12 Layout ... 49
12.1 Layout Guidelines ... 49
12.2 Layout Example ... 50
13 Device and Documentation Support ... 51
13.1 Device Support ... 51
13.2 Documentation Support ... 51
13.3 ドキュメントの更新通知を受け取る方法 ... 51
13.4 サポート・リソース ... 51
13.5 Trademarks ... 51
13.6 静電気放電に関する注意事項 ... 51
13.7 用語集 ... 51
14 Mechanical, Packaging, and Orderable Information ... 52

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (December 2016) to Revision D (April 2023)	Page
• TUV IEC 62368 認証機能を追加	1
• Changed BTST from anode to cathode and REGN from cathode to anode in descriptions	6
• Updated inclusive terminology throughout data sheet	31

Changes from Revision B (November 2014) to Revision C (December 2016)	Page
• Changed CE to $\overline{CE}$ for BQ24297 in Pin Functions	6
• Changed VREF to V_{REGN} in 図 9-8	25
• Changed 20°C to –20°C and VREF to V_{REGN} in 図 9-9	25
• Changed 式 1	25
• Changed Bit 3 RESET from 1 to 0 in 表 9-11	38
• Changed Bit 2 RESET from 1 to 0 in 表 9-11	38
• Changed 0 to 1 for REG05 Bit 2 Reset in 表 9-12	38
• Changed 1 to 0 for REG05 Bit 1 Reset in 表 9-12	38
• Changed DPDM_EN to IINDET_EN in 表 9-14	41
• Changed D+/D– to Input current limit in 表 9-14	41
• Added note to 図 10-1	43
• Added note to 図 10-2	43
• Changed last paragraph in セクション 10.2.2.3 section	45

Changes from Revision A (October 2013) to Revision B (November 2014)	Page
• 「取り扱い定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 先頭ページの回路図を変更	1
• Changed REG01[4] = 1 to REG01[5] = 1 in OTG description	6
• Added (10kΩ NTC thermister only) to QON description	6

Copyright © 2023 Texas Instruments Incorporated

- Added ESD information to Handling Ratings 8
- Changed I_{CHG} = 1792 mA in $I_{ICHG_REG_ACC}$ test conditions..... 9
- Changed falling to rising in V_{HTF} 9
- Changed V_{HTF} TYP to 47.2% 9
- Changed Input high threshold (OTG) MIN to 1.1 V..... 9
- Changed 表 9-2 19
- Changed 図 9-5 24
- Changed RT1 = 5.25 kΩ 25
- Deleted and LSFET from *Voltage and Current Monitoring in Buck Mode* description..... 29
- Deleted HSFET and from *Voltage and Current Monitoring in Boost Mode* description..... 30
- Changed text in セクション 9.3.5.4.1 30
- Changed REG09[5] to REG09[3] in *Battery Over-Voltage Protection (BATOVP)* section..... 30
- Changed REG09 Bit 3 description 1 – Battery OVP 42

Changes from Revision * (September 2013) to Revision A (October 2013)	Page
• BQ24297 部品番号から H を削除	1

Copyright © 2023 Texas Instruments Incorporated

5 Description (continued)

Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charge time and extends battery life during discharging phase. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports 3.9-V to 6.2-V USB input sources, including standard USB host port and USB charging port with 6.4-V over-voltage protection. The device is compliant with USB 2.0 and USB 3.0 power specifications with input current and voltage regulation. To set the default input current limit, the BQ24296 takes the result from the detection circuit in the system, such as USB PHY device and the BQ24297 detects the input source through D+/D- detection following the USB battery charging spec 1.2. In addition, the BQ24297 detects non-standard 2-A/1-A adapters. The device also supports USB On-the-Go operation by providing fast startup and supplying adjustable voltage 4.55-V to 5.5-V (default 5 V) on the VBUS with an accurate current limit up to 1.5 A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5-V minimum system voltage (programmable). With this feature, the system keeps operating even when the battery is completely depleted or removed. When the input source current or voltage limit is reached, the power path management automatically reduces the charge current to zero and then starts discharges the battery until the system power requirement is met. This supplement mode operation keeps the input source from getting overloaded.

The device initiates and completes a charging cycle when host control is not available. It automatically charges the battery in three phases: pre-conditioning, constant current, and constant voltage. In the end, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. Later on, when the battery voltage falls below the recharge threshold, the charger automatically starts another charging cycle.

The charge device provides various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer, and over-voltage/over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable).

The STAT output reports the charging status and any fault conditions. The INT immediately notifies the host when a fault occurs.

The BQ24296 and BQ24297 are available in a 24-pin, 4.00 x 4.00 mm^2 thin VQFN package.

Copyright © 2023 Texas Instruments Incorporated

6 Device Comparison Table

	BQ24296	BQ24297
I^2C Address	6BH	6BH
USB OTG	Yes Adjustable 4.5 V to 5.5 V at 1.5 A (max)	Yes Adjustable 4.5 V to 5.5 V at 1.5 A (max)
USB Detection	PSEL	D+/D–
Default Battery Voltage	4.208 V	4.208 V
Default Charge Current	2.048 A	2.048 A
Default Adapter Current Limit	3 A	3 A
Default Pre-Charge Current / Max Pre-Charge Current	256 mA / 2.048 A	256 mA / 2.048 A
Default Termination Current	256 mA	256 mA
Charging Temperature Profile	Cold/Hot	Cold/Hot
Status Output	STAT, $\overline{PG}$	STAT
STAT During Fault	Blinking at 1 Hz	Blinking at 1 Hz
Default Safety Timer	12 hr	12 hr
Default VINDPM	4.36 V	4.36 V
Default Pre-charge Timer	4 hr	4 hr

Copyright © 2023 Texas Instruments Incorporated

7 Pin Configuration and Functions

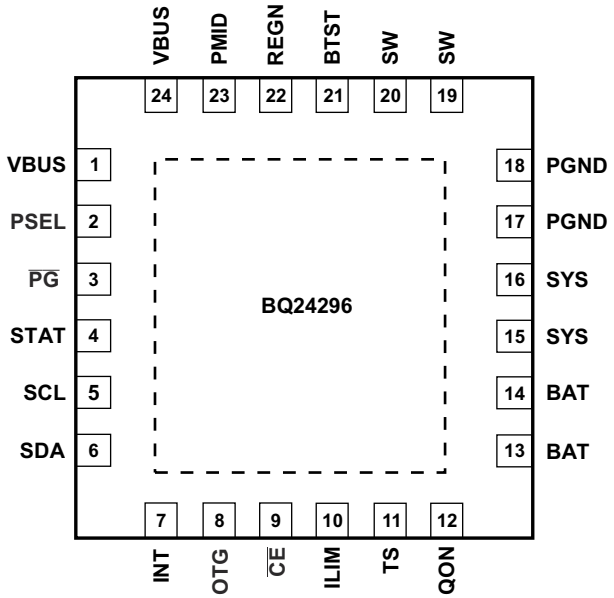


図 7-1. 24-Pin VQFN RGE Package (Top View)

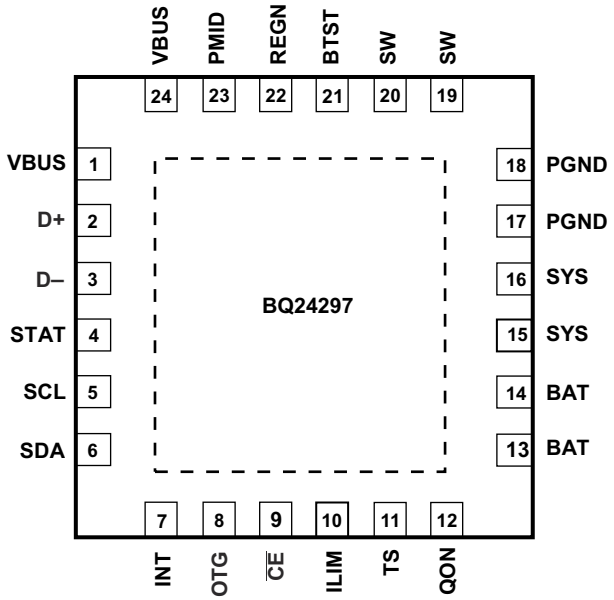


図 7-2. 24-Pin VQFN RGE Package (Top View)

表 7-1. Pin Functions

PIN		NUMBER	TYPE	DESCRIPTION
BQ24296	BQ24297			
VBUS	VBUS	1,24	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
PSEL	PSEL	2	I	Power source selection input. High indicates a USB host source and Low indicates an adapter source.
–	D+	2	I Analog	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary detection in bc1.2, and non-standard adapters.

Copyright © 2023 Texas Instruments Incorporated

表 7-1. Pin Functions (continued)

PIN		NUMBER	TYPE	DESCRIPTION
BQ24296	BQ24297			
$\overline{PG}$	–	3	O	Open drain active low power good indicator. Connect to the pull up rail via 10-kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
–	D–	3	I Analog	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary detection in bc1.2, and non-standard adapters.
STAT	STAT	4	O	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin in the charge blinks at 1 Hz.
SCL	SCL	5	I	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	SDA	6	I/O	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	INT	7	O	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
OTG	OTG	8	I Digital	USB current limit selection pin during buck mode, and active high enable pin during boost mode. For BQ24296, when in buck mode with USB host (PSEL = High), when OTG = High, IIN limit = 500 mA and when OTG = Low, IIN limit = 100 mA. For BQ24297, when in buck mode with USB host, when OTG = High, IIN limit = 500 mA and when OTG = Low, IIN limit = 100 mA. The boost mode is activated when the REG01[5] = 1 and OTG pin is High.
$\overline{CE}$	$\overline{CE}$	9	I	Active low Charge Enable pin. Battery charging is enabled when REG01[5:4] = 01 and $\overline{CE}$ pin = Low. $\overline{CE}$ pin must be pulled high or low.
ILIM	ILIM	10	I	ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = (1V/R_{ILIM}) \times K_{ILIM}$. The actual input current limit is the lower one set by ILIM and by I^2C REG00[2:0]. The minimum input current programmed on ILIM pin is 500 mA.
TS	TS	11	I Analog	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends or Boost disable when TS pin is out of range. A 103AT-2 thermistor is recommended.
QON	QON	12	I	BATFET enable control in shipping mode. A logic low to high transition on this pin with minimum 2-ms high level turns on BATFET to exit shipping mode. It has internal 1-MΩ (Typ) pull down. For backward compatibility, when BATFET enable control function is not used, the pin can be no connect or tied to TS pin (10-kΩ NTC thermister only). (Refer to *セクション 9.3.1.2.2* for detail description).
BAT	BAT	13,14	P	Battery connection point to the positive pin of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10 µF closely to the BAT pin.
SYS	SYS	15,16	I	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage.
PGND	PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	SW	19,20	O	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
BTST	BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
REGN	REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PMID	PMID	23	O	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Given the total input capacitance, connect a 1-µF capacitor on VBUS to PGND, and the recommended 8.2 µF or more on PMID to PGND.
Thermal Pad	Thermal Pad	–	P	Exposed pad beneath the IC for heat dissipation. Always solder thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter.

Copyright © 2023 Texas Instruments Incorporated

8 Specifications

8.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage (with respect to GND)	VBUS (converter not switching)	–2	15(2)	V
	PMID (converter not switching)	–0.3	15(2)	V
	STAT, $\overline{PG}$	–0.3	12	V
	BTST	–0.3	12	V
	SW	–2	7 8 (Peak for 20ns duration)	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, ILIM, REGN, TS, QON , $\overline{CE}$, D+, D–, PSEL	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
Output sink current	INT, STAT, $\overline{PG}$		6	mA
Junction temperature		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground pin unless otherwise noted.
(2) VBUS is specified up to 16 V for a maximum of 24 hours under no load conditions.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.9	6.2(1)	V
I_{IN}	Input current (VBUS)		3	A
I_{SYS}	Output current (SYS)		3.5	A
V_{BAT}	Battery voltage		4.4	V
I_{BAT}	Fast charging current		3	A
	Discharging current with internal MOSFET		5.5	A
T_A	Operating free-air temperature range	–40	85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

Copyright © 2023 Texas Instruments Incorporated

8.4 Thermal Information

THERMAL METRIC(1)		BQ2429x RGE (VQFN) 24 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS)	$V_{VBUS} < V_{UVLO}$, VBAT = 4.2 V, leakage between BAT and VBUS		5		µA
		High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1), –40°C – 85°C		16	20	µA
		High-Z Mode, or no VBUS, BATFET enabled (REG07[5] = 0), –40°C – 85°C		32	55	µA
I_{VBUS}	Input supply current (VBUS)	V_{VBUS} = 5 V, High-Z mode, No battery		15	30	µA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0 A		4		mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, charge disable, V_{BAT} = 3.8 V, I_{SYS} = 100 µA		3.5		mA
I_{BOOST}	Battery discharge current in boost mode	VBAT = 4.2 V, Boost mode, I_{VBUS} = 0 A, converter switching		3.5		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating voltage		3.9		6.2	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery	V_{VBUS} rising	3.6			V
V_{SLEEP}	Sleep mode falling threshold	V_{VBUS} falling, $V_{VBUS-VBAT}$	35	80	120	mV
V_{SLEEPZ}	Sleep mode rising threshold	V_{VBUS} rising, $V_{VBUS-VBAT}$	170	250	350	mV
V_{ACOV}	VBUS over-voltage rising threshold	V_{VBUS} rising	6.2	6.4	6.6	V
V_{ACOV_HYST}	VBUS over-voltage falling hysteresis	V_{VBUS} falling		250		mV
V_{BAT_UVLOZ}	Battery for active I^2C, no VBUS	V_{BAT} rising	2.3			V
V_{BAT_DPL}	Battery depletion threshold	V_{BAT} falling		2.4	2.6	V
$V_{BAT_DPL_HY}$	Battery depletion rising hysteresis	V_{BAT} rising		200		mV
$V_{VBUSMIN}$	Bad adapter detection threshold	V_{VBUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
POWER PATH MANAGEMENT						
V_{SYS_MAX}	Typical system regulation voltage	Isys = 0 A, BATFET (Q4) off, V_{BAT} up to 4.2 V, REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.5		4.35	V
V_{SYS_MIN}	System voltage outpu	REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.5	3.65		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMIID			28	41	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance between PMID and SW	T_J = –40°C – 85°C		39	51	mΩ
		T_J = -40°C – 125°C		39	58	

Copyright © 2023 Texas Instruments Incorporated

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between SW and PGND	T_J = –40°C – 85°C		61	82	mΩ
		T_J = -40°C – 125°C		61	90	
V_{FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10mA		30		mV
V_{SYS_BAT}	SYS/BAT comparator	V_{SYS} falling		70		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising		3.55		V
V_{BATGD_HYST}	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
$V_{BAT_REG_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.112 V and 4.208 V	–0.5%		0.5%	
$I_{ICHG_REG_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.8 V, I_{CHG} = 1024 mA, T_J = 25°C	-4%		4%	
		V_{BAT} = 3.8 V, I_{CHG} = 1024 mA, T_J = -20°C – 125°C	-7%		7%	
		V_{BAT} = 3.8 V, I_{CHG} = 1792 mA, T_J = -20°C – 125°C	–10%		10%	
I_{CHG_20pct}	Charge current with 20% option on	V_{BAT} = 3.1 V, I_{CHG} = 104 mA, REG02 = 03 and REG02[0] = 1	75		175	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV_HYST}$	Battery LOWV rising threshold	Precharge to fast charge, REG04[1] = 1 (Typical 200-mV hysteresis)	2.8	3.0	3.1	V
I_{PRECHG_ACC}	Precharge current regulation accuracy	VBAT = 2.6 V, I_{CHG} = 256 mA	–20%		20%	
$I_{TYP_TERM_ACC}$	Typical termination current	I_{TERM} = 256 mA, I_{CHG} = 2048 mA		265		mA
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 256 mA, I_{CHG} = 2048 mA	–22.5%		22.5%	
V_{SHORT}	Battery short voltage	VBAT falling		2.0		V
V_{SHORT_HYST}	Battery Short Voltage hysteresis	VBAT rising		200		mV
I_{SHORT}	Battery short current	VBAT < 2.2 V		100		mA
V_{RECHG}	Recharge threshold below VBAT_REG	VBAT falling, REG04[0] = 0		100		mV
t_{RECHG}	Recharge deglitch time	VBAT falling, REG04[0] = 0		20		ms
R_{ON_BATFET}	SYS-BAT MOSFET on-resistance	T_J = 25°C		24	28	mΩ
		T_J = –40°C – 125°C		24	35	
INPUT VOLTAGE/CURRENT REGULATION						
$V_{INDPM_REG_ACC}$	Input voltage regulation accuracy		-2%		2%	
I_{USB_DPM}	USB Input current regulation limit, VBUS = 5V, current pulled from SW	USB100	85		100	mA
		USB150	125		150	mA
		USB500	440		500	mA
		USB900	750		900	mA
I_{ADPT_DPM}	Input current regulation accuracy	IADP = 1.5 A, REG00[2:0] = 101	1.3		1.5	A
I_{IN_START}	Input current limit during system start up	VSYS < 2.2 V		100		mA
K_{ILIM}	I_{IN} = K_{ILIM}/R_{ILIM}	IINDPM = 1.5 A	395	435	475	A x Ω
D+/D- DETECTION (BQ24297)						
V_{D+_SRC}	D+ voltage source		0.5		0.7	V
I_{D+_SRC}	D+ connection check current source		7		14	μA
I_{D-_SINK}	D– current sink		50	100	150	μA
I_{D_LKG}	Leakage current into D+/D–	D–, switch open	–1		1	μA
		D+, switch open	–1		1	μA
V_{D+_LOW}	D+ low comparator threshold				0.8	V
$V_{D-_LOWdatref}$	D– low comparator threshold		250		400	mV
R_{D-_DWN}	D– pulldown for connection check		14.25		24.8	kΩ
$t_{SDP_DEFAULT}$	Charging timer with 100mA USB host in default mode				45	mins

Copyright © 2023 Texas Instruments Incorporated

8.5 Electrical Characteristics (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{adpt1_lo}	D+ low comparator threshold for non-standard adapter Divider-1	As percentage of REGN, 0°C – 85°C(1)	46.5%	48%	49.5%	
V_{adpt1_hi}	D+ low comparator threshold for non-standard adapter divider-1	As percentage of REGN, 0°C – 85°C(1)	58.5%	60%	61.5%	
V_{adpt2_lo}	D+ low comparator threshold for non-standard adapter divider-2	As percentage of REGN, 0°C – 85°C(1)	15.5%	17%	18.5%	
V_{adpt2_hi}	D+ low comparator threshold for Non-standard adapter divider-2	As percentage of REGN, 0°C – 85°C(1)	28.5%	30%	31.5%	
V_{adpt3_lo}	D- low comparator threshold for non-standard adapter divider-3	As percentage of REGN, 0°C – 85°C(1)	46.5%	48%	49.5%	
V_{adpt3_hi}	D- high comparator threshold for non-standard adapter divider-3	As percentage of REGN, 0°C – 85°C(1)	58.5%	60%	61.5%	
BAT OVER-VOLTAGE PROTECTION						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%		
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{Junction_REG}$	Junction temperature regulation accuracy	REG06[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		160		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			30		°C
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
COLD/HOT THERMISTER COMPARATOR						
V_{LTF}	Cold temperature threshold, TS pin voltage rising threshold	Charger suspends charge. as percentage to V_{REGN}	73%	73.5%	74%	
V_{LTF_HYS}	Cold temperature hysteresis, TS pin voltage falling	As percentage to V_{REGN}		0.4%		
V_{HTF}	Hot temperature TS pin voltage rising threshold	As percentage to V_{REGN}	46.6%	47.2%	48.8%	
V_{TCO}	Cut-off temperature TS pin voltage falling threshold	As percentage to V_{REGN}	44.2%	44.7%	45.2%	
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		10		ms
VBCOLD0	Cold temperature threshold, TS pin voltage rising threshold	As percentage to V_{REGN} REG02[1] = 0 (Approx. -10°C w/ 103AT)	75.5%	76%	76.5%	
VBCOLD0_HYS		As percentage to V_{REGN} REG02[1] = 0 (Approx. 1°C w/ 103AT)		1%		
VBCOLD1	Cold temperature threshold 1, TS pin voltage rising threshold	As percentage to V_{REGN} REG02[1] = 1 (Approx. -20°C w/ 103AT)	78.5%	79%	79.5%	
VBCOLD1_HYS		As percentage to V_{REGN} REG02[1] = 1 (Approx. 1°C w/ 103AT)		1%		
VBHOT0	Hot temperature threshold, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 01 (Approx. 55°C w/ 103AT)	35.5%	36%	36.5%	
VBHOT0_HYS		As percentage to V_{REGN} REG06[3:2] = 01 (Approx. 3°C w/ 103AT)		3%		
VBHOT1	Hot temperature threshold 1, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 00 (Approx. 60°C w/ 103AT)	32.5%	33%	33.5%	
VBHOT1_HYS		As percentage to V_{REGN} REG06[3:2] = 00 (Approx. 3°C w/ 103AT)		3%		
VBHOT2	Hot temperature threshold 2, TS pin voltage falling threshold	As percentage to V_{REGN} REG06[3:2] = 10 (Approx. 65°C w/ 103AT)	29.5%	30%	30.5%	
VBHOT2_HYS		As percentage to V_{REGN} REG06[3:2] = 10 (Approx. 3°C w/ 103AT)		3%		
CHARGE OVER-CURRENT COMPARATOR						

Copyright © 2023 Texas Instruments Incorporated

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HSFET_OCP}	HSFET cycle by cycle over-current threshold		5.3	7.5		A
I_{BATFET_OCP}	System over load threshold		5.5	6.6		A
V_{LSFET_UCP}	LSFET charge under-current falling threshold	From sync mode to non-sync mode		100		mA
F_{SW}	PWM Switching frequency, and digital clock		1300	1500	1700	kHz
D_{MAX}	Maximum PWM duty cycle			97%		
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold	VBTST-VSW when LSFET refresh pulse is requested, VBUS = 5 V		3.6		V
BOOST MODE OPERATION						
$V_{OTG_REG_ACC}$	OTG output voltage	I(VBUS) = 0, REG06[7:4] = 0111 (4.998 V)		5		V
$V_{OTG_REG_ACC}$	OTG output voltage accuracy	I(VBUS) = 0, REG06[7:4] = 0111 (4.998 V)	-3%		3%	
V_{OTG_BAT}	Battery voltage exiting OTG mode	BAT falling, REG04[1] = 1	2.9			V
I_{OTG}	OTG mode output current	REG01[0] = 0	1			A
		REG01[0] = 1	1.5			A
V_{OTG_OVP}	OTG over-voltage threshold	Rising threshold	5.8	6		V
$V_{OTG_OVP_HYS}$	OTG over-voltage threshold hysteresis	Falling threshold		300		mV
I_{OTG_LSOCP}	LSFET cycle by cycle current limit		5			A
I_{OTG_HSZCP}	HSFET under current falling threshold			100		mA
I_{RBFET_OCP}	RBFET over-current threshold	REG01[0] = 0	1.00	1.15	1.30	A
		REG01[0] = 1	1.50	1.70	1.90	
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 6 V, I_{REGN} = 40 mA	4.8	5	5.5	V
		V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.7	4.8		V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5 V, V_{REGN} = 3.8 V	50			mA
LOGIC I/O PIN CHARACTERISTICS (OTG, $\overline{CE}$, STAT, QON , PSEL, $\overline{PG}$)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold ($\overline{CE}$, STAT, QON , PSEL, $\overline{PG}$)		1.3			V
V_{IH_OTG}	Input high threshold (OTG)		1.1			V
V_{OUT_LO}	Output low saturation voltage	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current (OTG, $\overline{CE}$, STAT , PSEL, $\overline{PG}$)	Pull-up rail 1.8 V			1	µA
I_{BIAS}	High level leakage current (QON)	Pull-up rail 3.6 V			8	µA
I^2C INTERFACE (SDA, SCL, INT)						
V_{IH}	Input high threshold level	VPULL-UP = 1.8 V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	VPULL-UP = 1.8 V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS}	High-level leakage current	VPULL-UP = 1.8 V, SDA and SCL			1	µA
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{HIZ}	Digital crude clock	REGN LDO disabled	15	35	50	kHz
f_{DIG}	Digital clock	REGN LDO enabled	1300	1500	1700	kHz

(1) REGN LDO is configured in drop-out mode. VBUS is close to REGN when I_{REGN} = 0 mA.

Copyright © 2023 Texas Instruments Incorporated

8.6 Timing Requirements

			MIN	TYP	MAX	UNIT
VBUS/BAT POWER UP						
t_{BADSRC}	Bad source detection duration			30		ms
BOOST MODE OPERATION						
$t_{OTG_OCP_OFF}$	OTG mode over-current protection off cycle time			32		ms
$t_{OTG_OCP_ON}$	OTG mode over-current protection on cycle time			260		µs
QON TIMING						
t_{QON}	QON pin high time to turn on BATFET		2			ms
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[5:4] = 11	REGN LDO disabled	112	160		s
		REGN LDO enabled	136	160		

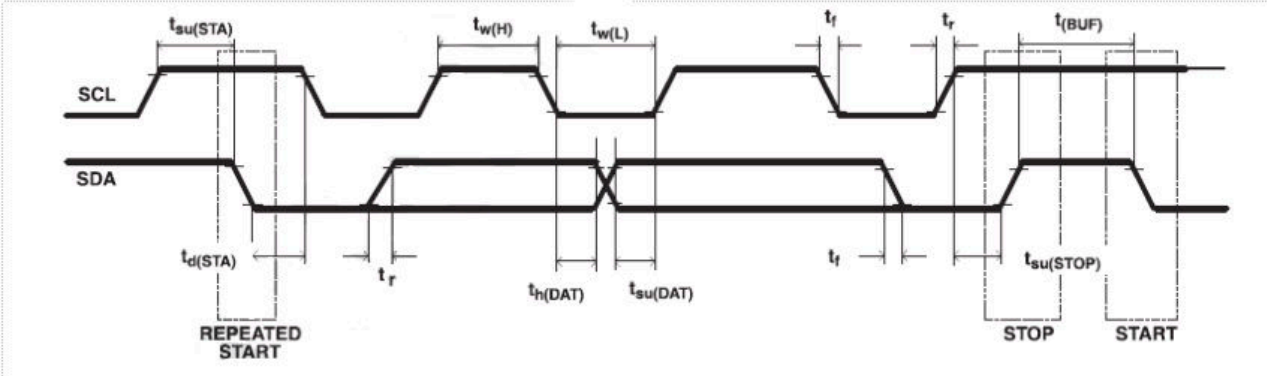


図 8-1. I²C-Compatible Interface Timing Diagram

8.7 Typical Characteristics

表 8-1. Table of Figures

	FIGURE
Charging Efficiency vs Charging Current (DCR = 10 mΩ)	図 8-2
System Efficiency vs System Load Current (DCR = 10 mΩ)	図 8-3
Boost Mode Efficiency vs VBUS Load Current (DCR = 10 mΩ)	図 8-4
SYS Voltage Regulation vs System Load Current	図 8-5
Boost Mode VBUS Voltage Regulation (Typical Output = 4.998 V, REG06[7:4] = 0111) vs VBUS Load Current	図 8-6
SYS Voltage vs Temperature	図 8-7
BAT Voltage vs Temperature	図 8-8
Input Current Limit vs Temperature	図 8-9
Charge Current vs Package Temperature	図 8-10

Copyright © 2023 Texas Instruments Incorporated

8.7 Typical Characteristics (continued)

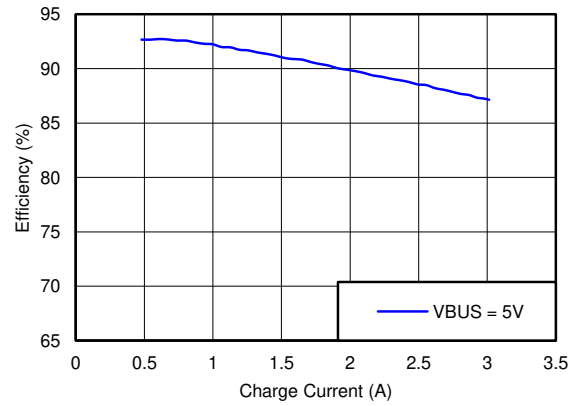


図 8-2. Charge Efficiency vs Charge Current

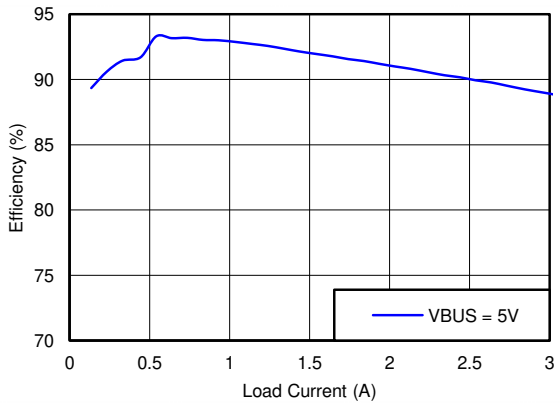


図 8-3. System Efficiency vs System Load Current

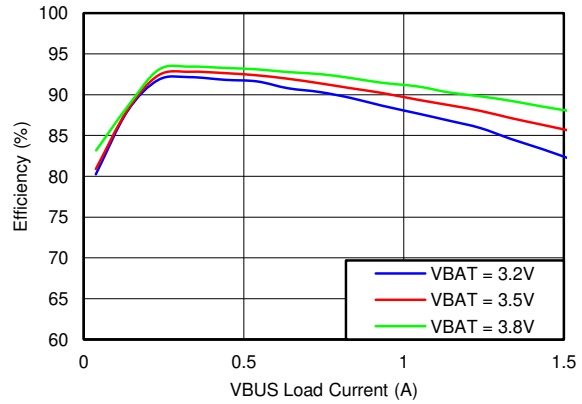


図 8-4. Boost Mode Efficiency vs VBUS Load Current

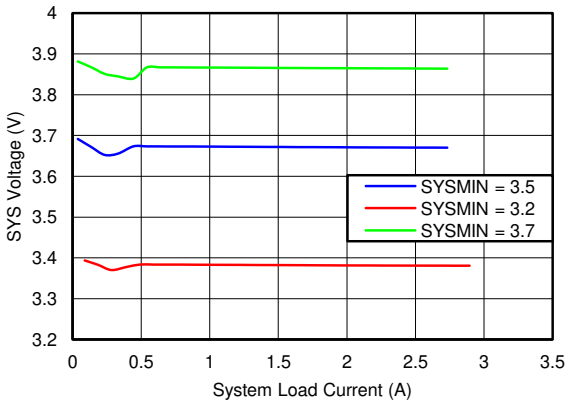
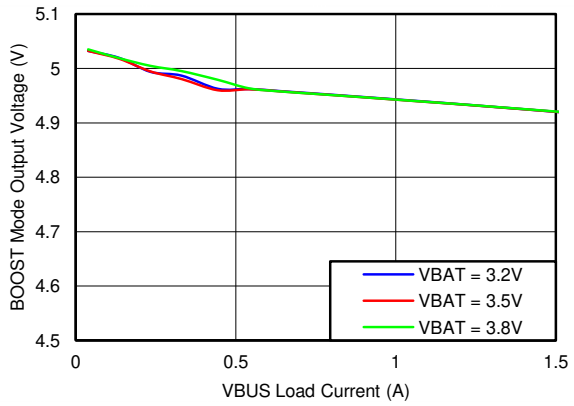


図 8-5. SYS Voltage Regulation vs System Load Current



Typical Output = 4.998 V, REG06[7:4] = 0111

図 8-6. Boost Mode VBUS Voltage Regulation vs VBUS Load Current

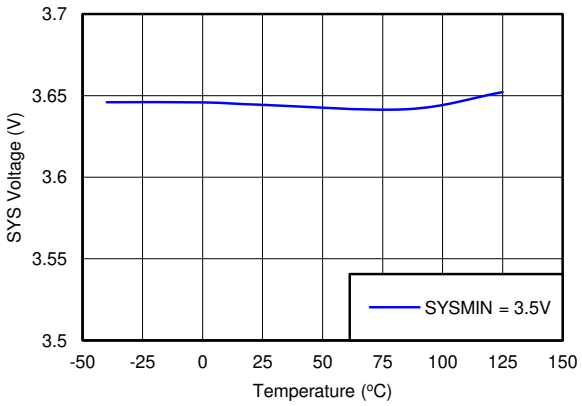


図 8-7. SYS Voltage vs Temperature

Copyright © 2023 Texas Instruments Incorporated

8.7 Typical Characteristics (continued)

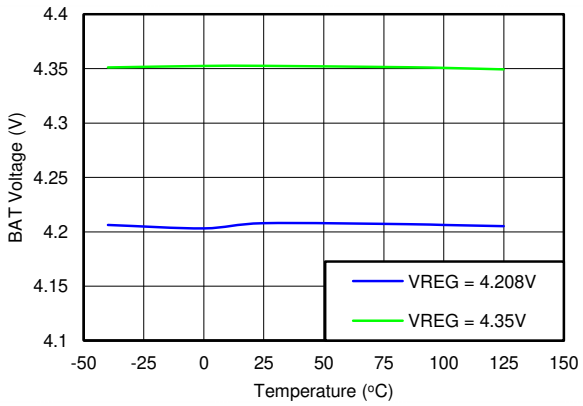


図 8-8. BAT Voltage vs Temperature

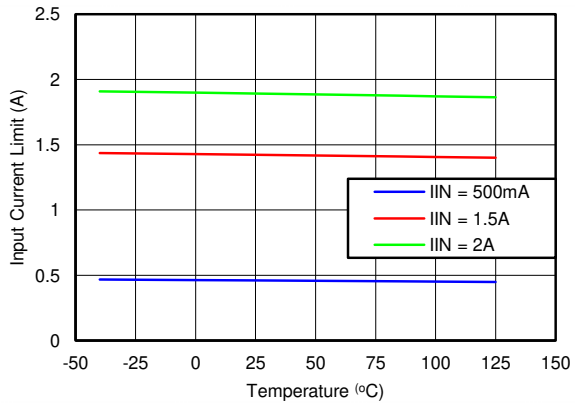


図 8-9. Input Current Limit vs Temperature

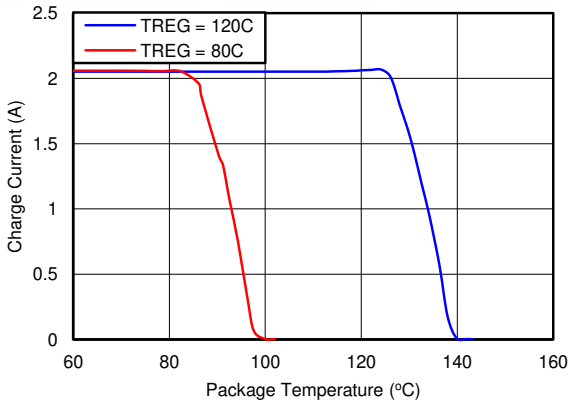


図 8-10. Charge Current vs Package Temperature

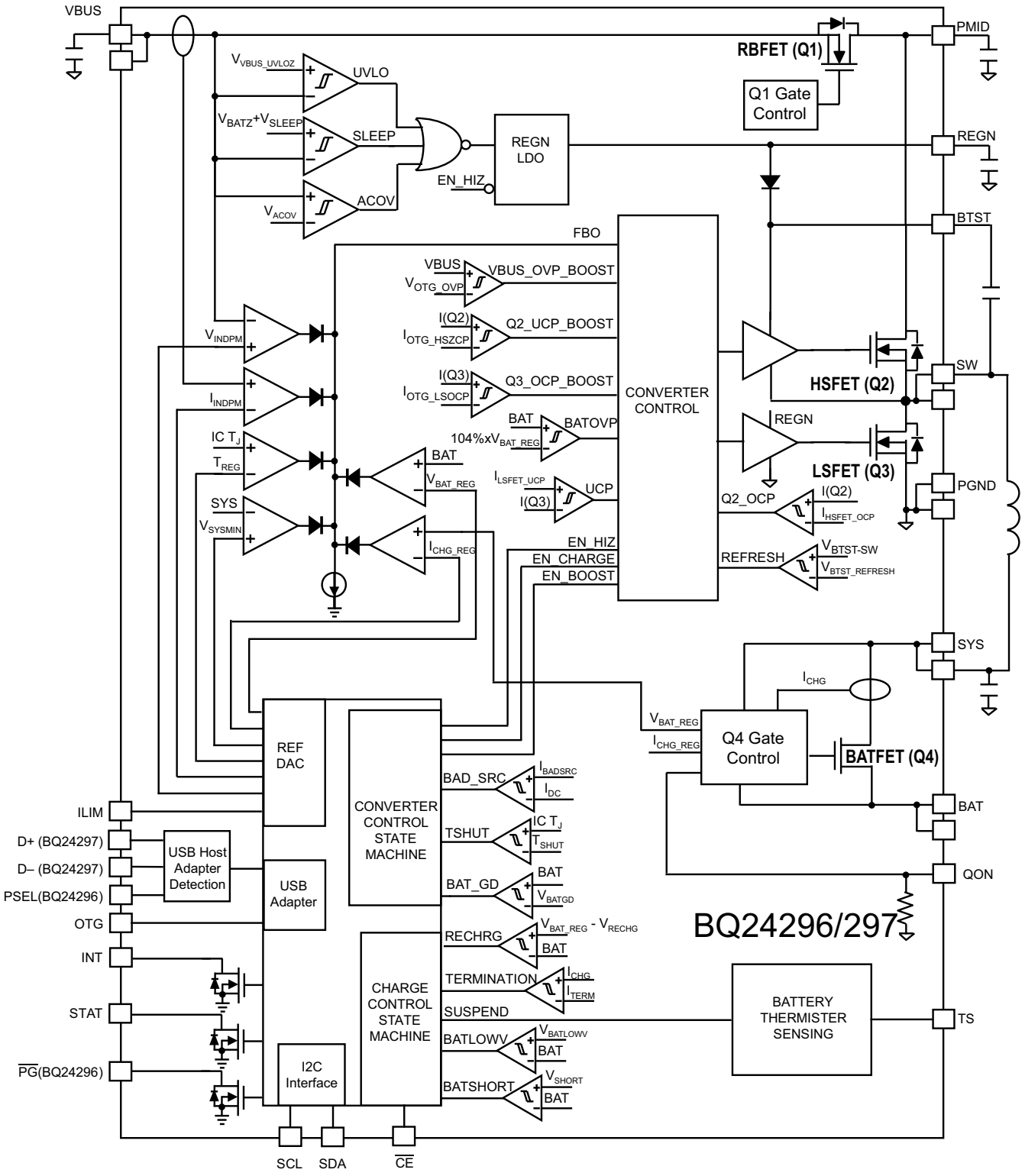
9 Detailed Description

9.1 Overview

The BQ24296, BQ24297 is an I^2C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

Copyright © 2023 Texas Instruments Incorporated

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Power Up

9.3.1.1 Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

9.3.1.2 Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DEPL}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. During both boost and charge mode, the device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

9.3.1.2.1 BATFET Turn Off

The BATFET can be forced off by the host through I^2C REG07[5] . This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery. When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

9.3.1.2.2 Shipping Mode

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage. The BATFET can be turned off by setting REG07[5] (BATFET_DISABLE) bit.

In order to keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4] = 00) and disable BATFET (REG07[5] = 1) at the same time. Once the BATFET is disabled, one of the following events can turn on BATFET and clear REG07[5] (BATFET_DISABLE) bit.

1. Plug in adapter
2. Write REG07[5] = 0
3. watchdog timer expiration
4. Register reset (REG01[7] = 1)
5. A logic low to high transition on QON pin (refer to 図 9-1 for detail timing)

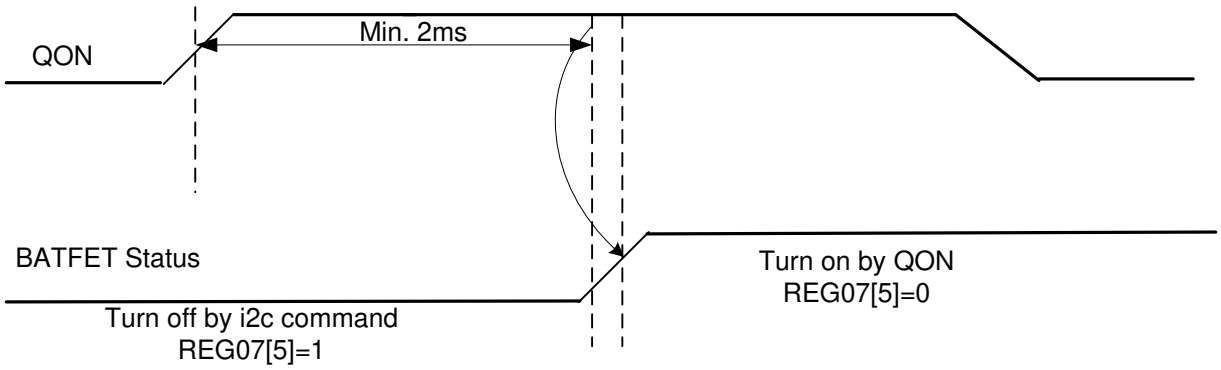


図 9-1. QON Timing

9.3.1.3 Power Up from DC Source

When the DC source plugs in, the charger device checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

Copyright © 2023 Texas Instruments Incorporated

9.3.1.3.1 REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT and $\overline{PG}$ (BQ24296) can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.

1. VBUS above V_{VBUS_UVLOZ}
2. VBUS above V_{BAT} + V_{SLEEPZ} in buck mode or VBUS below V_{BAT} + V_{SLEEP} in boost mode
3. After typical 220-ms delay (100 ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS} (15 μA typical) from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

9.3.1.3.2 Input Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below V_{ACOV} (not in VBUS over-voltage)
2. VBUS voltage above V_{BADSRC} (3.8 V typical) when pulling I_{BADSRC} (30 mA typical) (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high and the $\overline{PG}$ pin (BQ24296) goes low. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

9.3.1.3.3 Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100 mA/500 mA in USB 2.0, and 150 mA/900 mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 3 A.

After the $\overline{PG}$ is LOW (BQ24296) or REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The BQ24297 follows Battery Charging Specification 1.2 (BC1.2) to detect input source through USB D+/D- lines. The BQ24296 sets input current limit through PSEL and OTG pins. After the input current limit detection is done, the detection result is reported in VBUS_STAT registers (REG08[7:6]) and input current limit is updated in IINLIM register (REG00[2:0]). In additon, host can write to REG00[2:0] to change the input current limit.

9.3.1.3.4 D+/D– Detection Sets Input Current Limit (BQ24297)

The BQ24297 contains a D+/D– based input source detection to program the input current limit. The D+/D- detection has three steps: data contact detect (DCD), primary detection, and non-standard adapter detection. When the charging source passes data contact detect, the device would proceed to run primary detection. Otherwise the charger would proceed to run non-standard adapter detection.

Copyright © 2023 Texas Instruments Incorporated

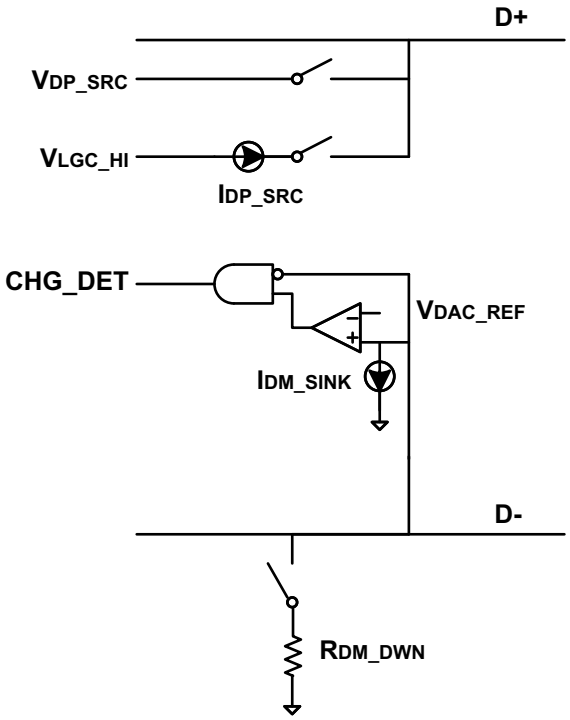


図 9-2. USB D+/D- Detection

DCD (Data Contact Detection) uses a current source to detect when the D+/D– pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and REG08[2] = 1 (power good)
- Turn on D+ I_{DP_SRC} and the D– pull-down resistor R_{DM_DWN} for 40 ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec.
- Turn off I_{DP_SRC} and disconnect R_{DM_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V_{DP_SRC} on D+ and I_{DM_SINK} on D– for 40 ms
- If PD is attached to a USB host (SDP), the D– is low. If PD is attached to a charging port (CDP or DCP), the D– is high
- Turn off V_{DP_SRC} and I_{DM_SINK}

表 9-1 shows the input current limit setting after D+/D– detection.

表 9-1. BQ24297 USB D+/D– Detection

D+/D– DETECTION	OTG	INPUT CURRENT LIMIT	REG08[7:6]
0.5 sec timer expired in DCD (D+/D- floating)	—	Proceed to non-standard adapter detection	00
USB host	LOW	100 mA	01
USB host	HIGH	500 mA	01
Charging port	—	3 A	10

When DCD 0.5 sec timer expires, the non-standard adapter detection is used to distinguish three different divider bias conditions on D+/D- pins. When non-standard adapter is detected, the input current limit (REG0[2:0]) is set based on the table shown below and REG08[7:6] is set to 10 (Adapter port). If non-standard adapter is not detected, REG08[7:6] is set to 00 (Unknown) and the input current limit is set in REG0[2:0] to 500 mA by default.

Copyright © 2023 Texas Instruments Incorporated

表 9-2. BQ24297 Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	$V_{adpt1_lo} < V_{D+} < V_{adpt1_hi}$ For VBUS = 5 V, typical range 2.4 V < V_{D+} < 3.1 V	$V_{D-} < V_{adpt1_lo}$ or $V_{D-} > V_{adpt1_hi}$ For VBUS = 5 V, typical range V_{D-} < 2.4 V or V_{D-} > 3.1 V	2.0A
Divider 2	$V_{adpt2_lo} < V_{D+} < V_{adpt2_hi}$ For VBUS = 5 V, typical range 0.85 V < V_{D+} < 1.5 V	NA	2.0A
Divider 3	$V_{D+} < V_{adpt3_lo}$ or $V_{D+} > V_{adpt3_hi}$ For VBUS = 5 V, typical range V_{D+} < 2.4 V or V_{D+} > 3.1 V	$V_{adpt3_lo} < V_{D-} < V_{adpt3_hi}$ For VBUS = 5 V, typical range 2.4 V < V_{D-} < 3.1 V	1A

After D+/D- detection is completed with an input source already plugged in, the input current limit is not changed unless DPDM_EN (REG07[7]) bit is set to force detection.

9.3.1.3.5 PSEL/OTG Pins Set Input Current Limit

The BQ24296 has PSEL instead of D+/D-. It directly takes the USB PHY device output to decide whether the input is USB host or charging port.

表 9-3. BQ24296 Input Current Limit Detection

PSEL	OTG	INPUT CURRENT LIMIT	REG08[7:6]
HIGH	LOW	100 mA	01
HIGH	HIGH	500 mA	01
LOW	—	3 A	10

9.3.1.3.6 HIZ State with 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100-mA USB host, and the battery is above bat-good threshold (V_{BATGD}), the device follows battery charging spec and enters high impedance state (HIZ). In HIZ state, the device is in the lowest quiescent state with REGN LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be less than 30 µA. The system is supplied by the battery.

Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7] = 0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.

In default mode, the charger IC will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

9.3.1.3.7 Force Input Current Limit Detection

While adapter is plugged-in, the host can force the charger device to run input current limit detection by setting REG07[7] = 1 or when watchdog timeout. During the forced detection, the input current limit is set to 100 mA. After the detection is completed, REG07[7] will return to 0 by itself and new input current limit is set based on D+/D- (BQ24297) or PSEL/OTG (BQ24296).

9.3.1.4 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when ramp up the system rail. When the system rail is below 2.2 V, the input current limit is forced to 100mA. After the system rises above 2.2 V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

Copyright © 2023 Texas Instruments Incorporated

As a battery charger, the charger deploys a 1.5-MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

9.3.1.5 Boost Mode Operation from Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 1-A output requirement. The maximum output current is 1.5 A. The boost operation can be enabled if the following conditions are valid:

1. BAT above BATLOWV threshold ($V_{BATLOWV}$ set by REG04[1])
2. VBUS less than V_{BAT} + V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4] = 10)
4. Thermistor Temperature is within boost mode temperature monitor threshold unless BHOT[1:0] is set to 11 (REG06[1:0]) to disable this monitor function
5. After 30ms delay from boost mode enable

In boost mode, the device employs a 1.5-MHz step-up switching regulator. Similar to buck operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

During boost mode, the status register REG08[7:6] is set to 11, the VBUS output is 5 V and the output current can reach up to 1 A or 1.5 A, selected via I^2C (REG01[0]). In addition, the device provides adjustable boost voltage from 4.55 V to 5.5 V by changing BOOSTV bits in REG06[7:4]

Any fault during boost operation, including VBUS over-voltage or over-current, sets the fault register REG09[6] to 1 and an INT is asserted.

9.3.2 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

9.3.2.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150 mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

Copyright © 2023 Texas Instruments Incorporated

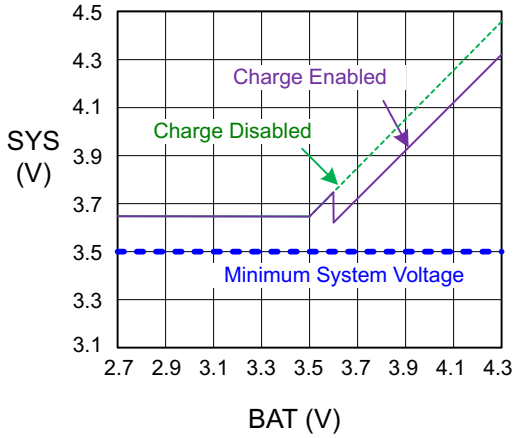


図 9-3. V(SYS) vs V(BAT)

9.3.2.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

図 9-4 shows the DPM response with 5-V/1.2-A adapter, 3.2-V battery, 2.0-A charge current and 3.4-V minimum system voltage setting.

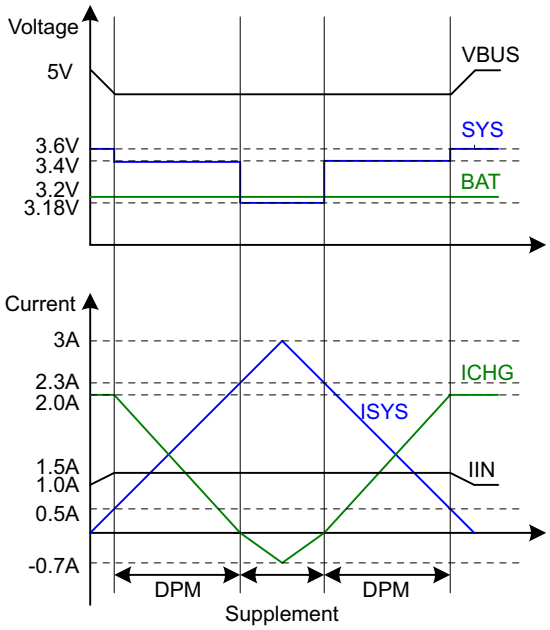


図 9-4. DPM Response

9.3.2.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. 図 9-5 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

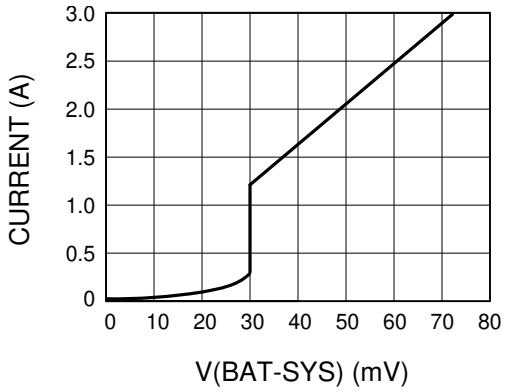


図 9-5. BATFET V-I Curve

9.3.3 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3-A charge current for high capacity tablet battery. The 24-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

9.3.3.1 Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4] = 01), the charger device complete a charging cycle without host involvement. The device default charging parameters are listed in the following table.

表 9-4. Charging Parameter Default Setting

DEFAULT MODE	BQ24296 / BQ24297
Charging voltage	4.208 V
Charging current	2.048 A
Pre-charge current	256 mA
Termination current	256 mA
Temperature profile	Hot/Cold
Safety timer	12 hours(1)

(1) See *Charging Safety Timer* for more information.

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by I^2C register bit (REG01[5:4]) = 01 and $\overline{CE}$ is low
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the device automatically starts another charging cycle. After the charge done, either toggle $\overline{CE}$ pin or REG01[5:4] will initiate a new charging cycle.

Copyright © 2023 Texas Instruments Incorporated

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

9.3.3.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

表 9-5. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
$V_{BAT} < V_{SHORT}$ (Typical 2 V)	100 mA	–	01
$V_{SHORT} \le V_{BAT} < V_{BATLOWV}$ (Typical 2 V ≤ V_{BAT} < 3 V)	REG03[7:4]	256 mA	01
$V_{BAT} \ge V_{BATLOWV}$ (Typical V_{BAT} ≥ 3 V)	REG02[7:2]	2048 mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

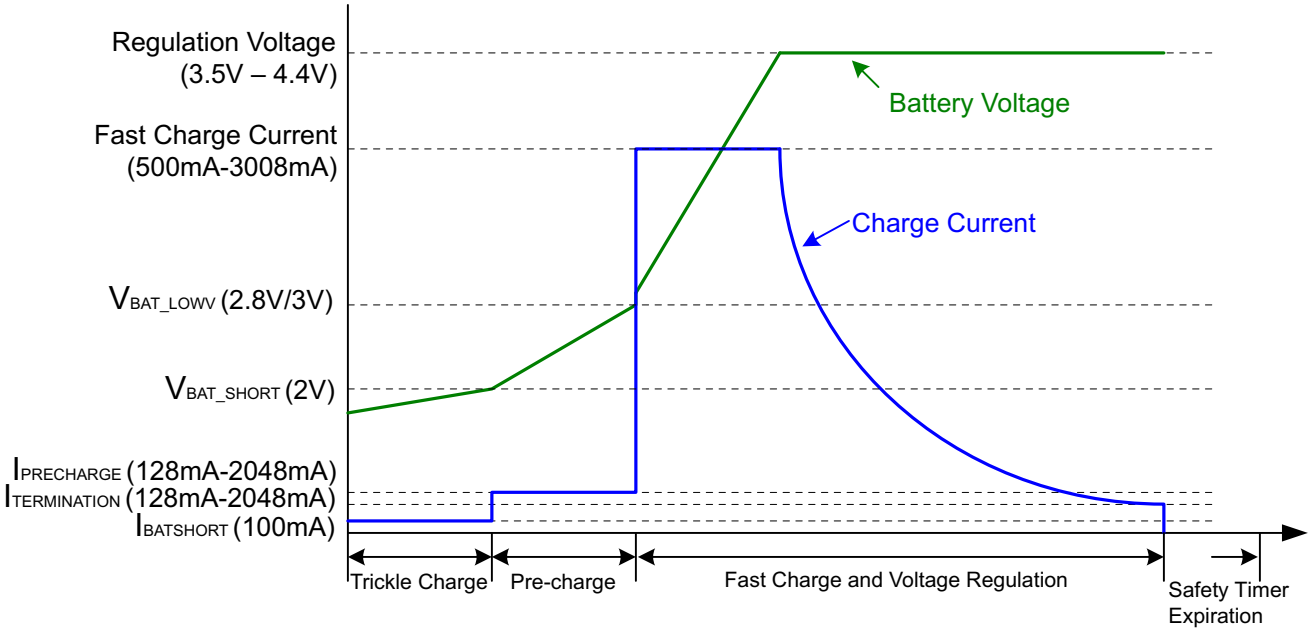


図 9-6. Battery Charging Profile

9.3.3.3 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

9.3.3.3.1 Cold/Hot Temperature Window

The device continuously monitors battery temperature by measuring the voltage between the TS pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charge or boost is allowed.

Copyright © 2023 Texas Instruments Incorporated

To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLDx to VBHOTx thresholds unless boost mode temperature is disabled by setting BHOT bits (REG06[3:2]) to 11. When temperature is outside of the temperature thresholds, the boost mode is suspended and REG08[7:6] bits (VBUS_STAT) are set to 00. Once temperature returns within thresholds, the boost mode is recovered.

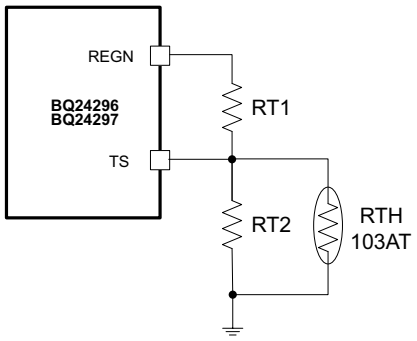


図 9-7. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

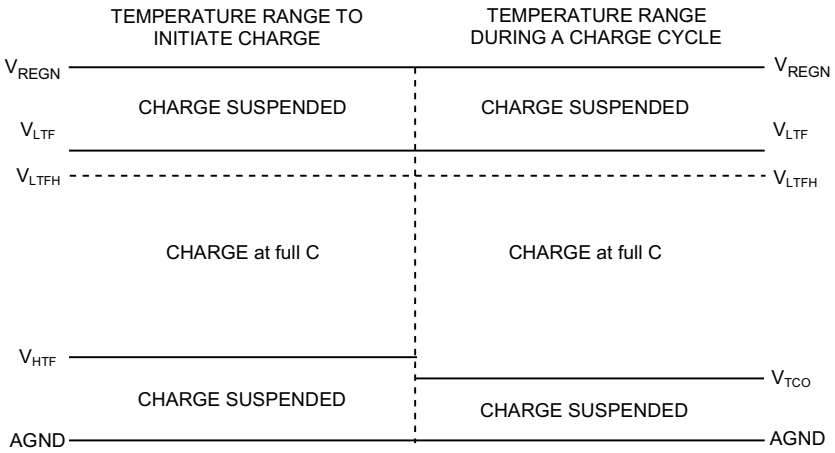


図 9-8. TS Pin Thermistor Sense Thresholds in Charge Mode

Copyright © 2023 Texas Instruments Incorporated

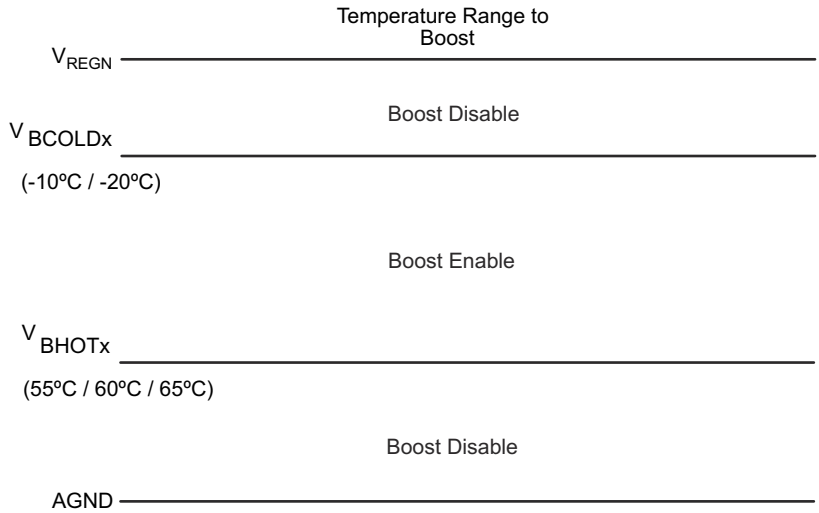


図 9-9. TS Pin Thermistor Sense Thresholds in Boost Mode

Assuming a 103AT NTC thermistor is used on the battery pack 図 9-8, the value RT1 and RT2 can be determined by using the following equation:

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{REGN}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{REGN}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (1)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.25 kΩ
RT2 = 31.23 kΩ

9.3.3.4 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

9.3.3.4.1 Termination When REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through $\overline{CE}$ pin or REG01[5:4].

9.3.3.5 Charging Safety Timer

The device has safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 4 hours when the battery is below batlowv threshold. The user can program fast charge safety timer (default 12 hours) through I^2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I^2C (REG05[3]).

The following actions restart the safety timer after safety timer expires:

- Toggle the $\overline{CE}$ pin HIGH to LOW to HIGH (charge enable)
- Write REG01[5:4] from 00 to 01 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)

During input voltage/current regulation, thermal regulation, or FORCE_20PCT bit (REG02[0]) is set , the safety timer counting at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

9.3.3.5.1 Safety Timer Configuration Change

When safety timer value needs to be changed, it is recommended that the timer is disabled first before new configuration is written to REG05[2:1]. The safety timer can be disable by writing 1 to REG05[3]. This ensures the safety timer restart counting after new value is configured.

9.3.3.6 USB Timer When Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

9.3.4 Status Outputs ($\overline{PG}$, STAT, and INT)

9.3.4.1 Power Good Indicator ($\overline{PG}$) (BQ24296)

In BQ24296, $\overline{PG}$ goes LOW to indicate a good input source when:

1. VBUS above V_{BUS_UVLO}
2. VBUS above battery (not in sleep)
3. VBUS below V_{ACOV} threshold
4. VBUS above V_{BUS_MIN} when I_{BADSRC} current is applied (not a poor source)

9.3.4.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

表 9-6. STAT Pin State

CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault, input or system over-voltage)	blinking at 1Hz

9.3.4.3 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate a 256-µs INT pulse.

1. USB/adapter source identified (through PSEL or DPDM detection, and OTG pin)
2. Good input source detected
   - not in sleep

Copyright © 2023 Texas Instruments Incorporated

- VBUS below V_{ACOV} threshold
- current limit above I_{BADSRC}

3. Input removed or VBUS above V_{ACOV} threshold
4. Charge Complete
5. Any FAULT event in REG09

For the first four events, INT pulse is always generated. For the last event, when a fault occurs, the charger device sends out INT and latches the fault state in REG09 until the host reads the fault register. If a prior fault exists, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last read and the 2nd reads the current fault register status.

9.3.5 Protections

9.3.5.1 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times K_{LIM} \quad (2)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3 A, and ILIM has a 316-Ω resistor to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1 V. If ILIM voltage exceeds 1 V, the device enters input current regulation (Refer to *Dynamic Power Path Management* section).

The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following 式 3:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (3)$$

For example, if ILIM pin sets 2 A, and the ILIM voltage is 0.75 V, the actual input current 1.5 A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1 V. If ILIM pin is short, the input current limit is set by the register.

9.3.5.2 Thermal Regulation and Thermal Shutdown

During charge operation, the device monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

9.3.5.3 Voltage and Current Monitoring in Buck Mode

The device closely monitors the input and system voltage, as well as HSFET current for safe buck mode operation.

Copyright © 2023 Texas Instruments Incorporated

9.3.5.3.1 Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

9.3.5.3.2 System Over-Voltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. When SYSOVP is detected, the converter stops immediately to clamp the overshoot.

9.3.5.4 Voltage and Current Monitoring in Boost Mode

The charger device closely monitors the VBUS voltage, as well as LSFET current to ensure safe boost mode operation.

9.3.5.4.1 Over-Current Protection

The charger device closely monitors the RBFET (Q1) and LSFET (Q3) current to ensure safe boost mode operation. During over-current condition, the device will operate in hiccup mode for protection. While in hiccup mode cycle, the device turns off RBFET for $t_{OTG_OCP_OFF}$ (32 ms typical) and turns on RBFET for $t_{OTG_OCP_ON}$ (260 us typical) in an attempt to restart. If the over-current condition is removed, the boost converter will maintain the RBFET on state and the VBUS OTG output will operate normally. When over-current condition continues to exist, the device will repeat the hiccup cycle until over-current condition is removed. When over-current condition is detected, the fault register bit BOOST_FAULT (REG09[6]) is set high to indicate fault in boost operation. An INT is asserted to the host.

9.3.5.4.2 VBUS Over-Voltage Protection

When an adapter plugs in during boost mode, the VBUS voltage will rise above regulation target. Once the VBUS voltage exceeds V_{OTG_OVP}, the device stops switching and the device exits boost mode. During the over-voltage, the fault register bit BOOST_FAULT (REG09[6]) is set high to indicate fault in boost operation. An INT is asserted to the host.

9.3.5.5 Battery Protection

9.3.5.5.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at V_{BAT_OVP} (4% nominal) above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[3] goes high and an INT is asserted to the host.

9.3.5.5.2 Battery Short Protection

If the battery voltage falls below V_{short} (2V typical), the device immediately turns off BATFET to disable the battery charging or supplement mode. 1ms later, the BATFET turns on and charge the battery with 100-mA current. The device does not turn on BATFET to discharge a battery that is below 2.5 V.

9.3.5.5.3 System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the device latches off BATFET. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.

9.4 Device Functional Modes

9.4.1 Host Mode and Default Mode

The device is a host controlled device, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings. The device keeps charging the battery by default with 12-hour fast charging safety timer. At

Copyright © 2023 Texas Instruments Incorporated

the end of the 12 hours, the charging is stopped and the buck converter continues to operate to supply system load.

Any write command to device transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4] = 00.

When the host changes watchdog timer configuration (REG05[5:4]), it is recommended to first disable watchdog by writing 00 to REG05[5:4] and then change the watchdog to new timer values. This ensures the watchdog timer is restarted after new value is written.

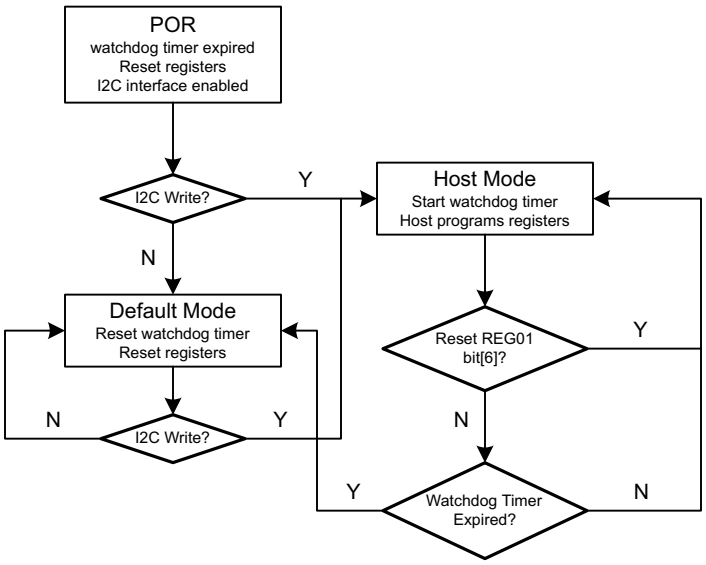


図 9-10. Watchdog Timer Flow Chart

9.4.1.1 Plug in USB100mA Source with Good Battery

When the input source is detected as 100mA USB host, and the battery voltage is above batgood threshold (V_{BATGD}), the charger device enters HIZ state to meet the battery charging spec requirement.

If the charger device is in host mode, it will stay in HIZ state even after the USB100mA source is removed, and the adapter plugs in. During the HIZ state, REG00[7] is set HIGH and the system load is supplied from battery. It is recommended that the processor host always checks if the charger IC is in HIZ state when it wakes up. The host can write REG00[7] to 0 to exit HIZ state.

If the charger is in default mode, when the DC source is removed, the charger device will get out of HIZ state automatically. When the input source plugs in again, the charger IC runs detection on the input source and update the input current limit.

9.4.1.2 USB Timer When Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

9.5 Programming

9.5.1 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as hosts or targets when performing data transfers. A host is the device which initiates a data

Copyright © 2023 Texas Instruments Incorporated

transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with address 6BH, receiving control inputs from the host device like microcontroller or a digital signal processor. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

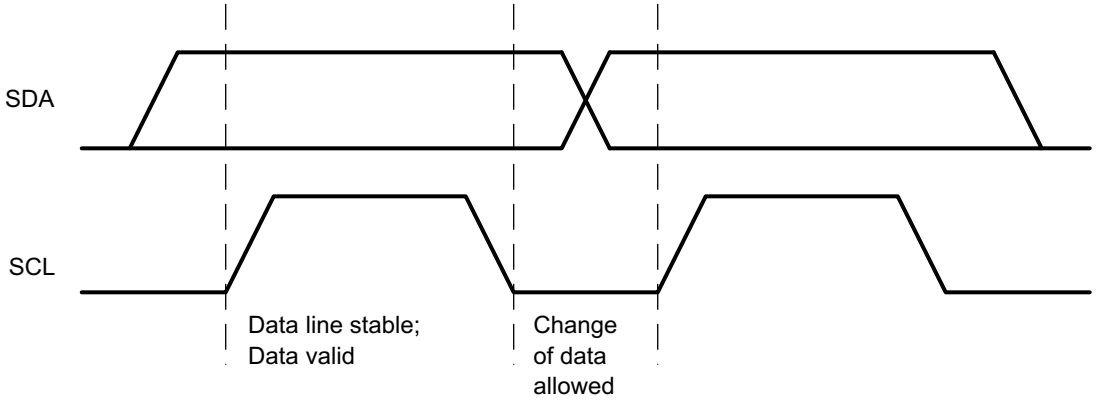


図 9-11. Bit Transfer on the I^2C Bus

9.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

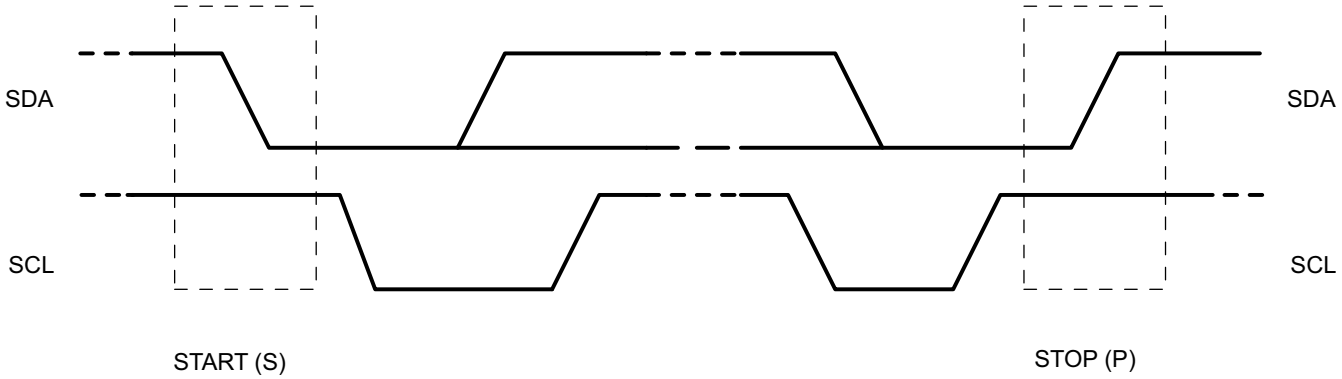


図 9-12. START and STOP Conditions

9.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some

Copyright © 2023 Texas Instruments Incorporated

other function, it can hold the clock line SCL low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

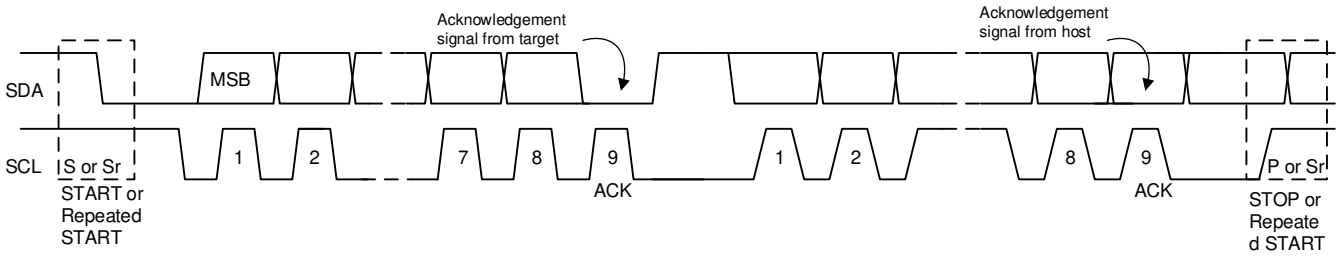


図 9-13. Data Transfer on the I²C Bus

9.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.5.1.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

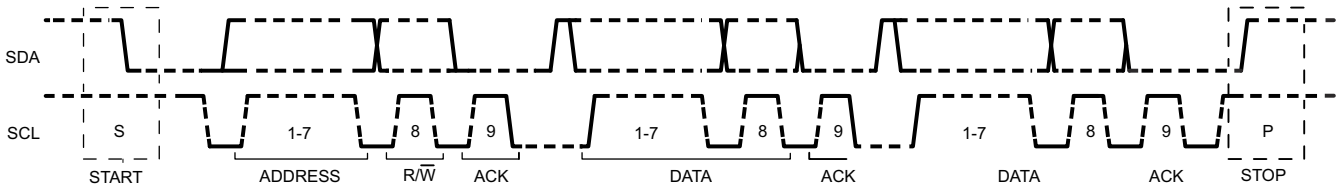


図 9-14. Complete Data Transfer

9.5.1.5.1 Single Read and Write

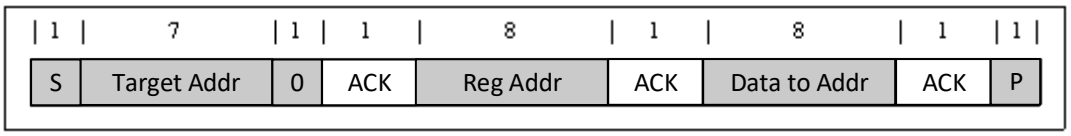


図 9-15. Single Write

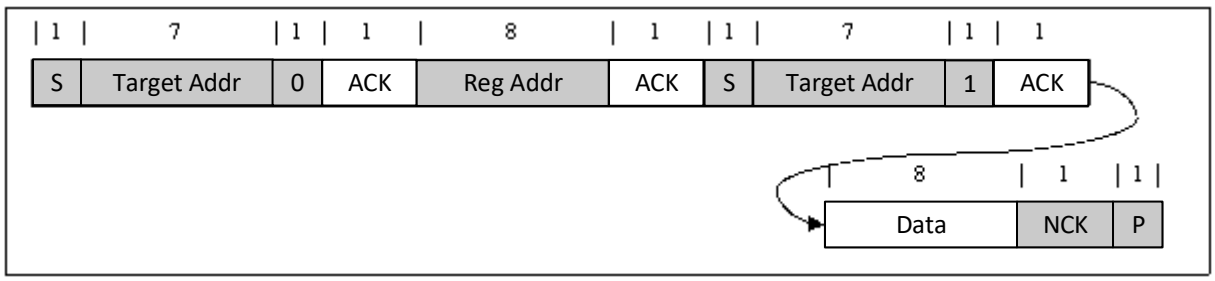


図 9-16. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.5.1.5.2 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

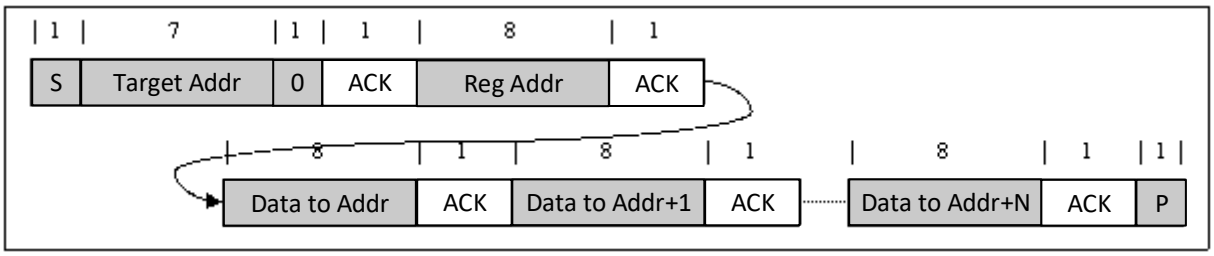


図 9-17. Multi-Write

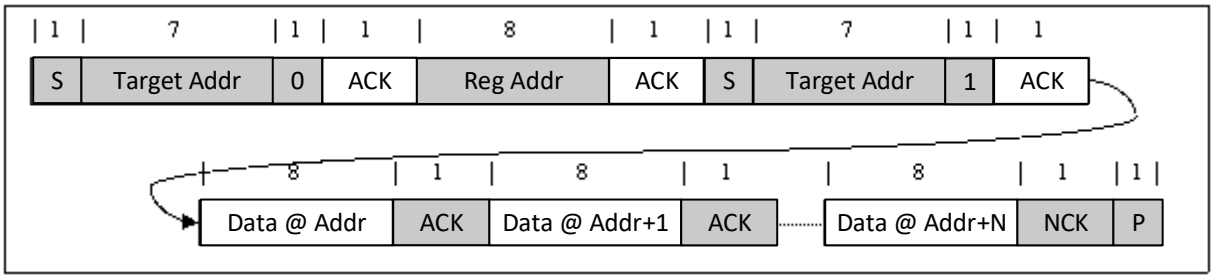


図 9-18. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if there is a TS fault but gets recovered immediately, the host still sees TS fault during the first read. In order to get the fault information at present, the host has to read REG09 for the second time. REG09 does not support multi-read and multi-write.

Copyright © 2023 Texas Instruments Incorporated

9.6 Register Map

9.6.1 I²C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are Read only.

9.6.1.1 Input Source Control Register REG00 [reset = 00110xxx, or 3x]

図 9-19. Input Source Control Register REG00 Format

7	6	5	4	3	2	1	0
EN_HIZ	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]	IINLIM[2]	IINLIM[1]	IINLIM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-7. Input Source Control Register REG00 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	EN_HIZ	R/W	0	0 – Disable, 1 – Enable	Default: Disable (0)
Input Voltage Limit					
Bit 6	VINDPM[3]	R/W	0	640 mV	Offset 3.88 V, Range: 3.88 V – 5.08 V Default: 4.36 V (0110)
Bit 5	VINDPM[2]	R/W	1	320 mV	
Bit 4	VINDPM[1]	R/W	1	160 mV	
Bit 3	VINDPM[0]	R/W	0	80 mV	
Input Current Limit (Actual input current limit is the lower of I²C and ILIM)					
Bit 2	IINLIM[2]	R/W	x	000 – 100 mA, 001 – 150 mA, 010 – 500 mA, 011 – 900 mA, 100 – 1 A, 101 – 1.5 A, 110 – 2 A, 111 – 3A	BQ24296 PSEL = Lo : 3 A (111) PSEL = Hi : 100 mA (000) (OTG pin = Lo) or 500 mA (OTG pin = Hi) BQ24297 Default SDP : 100 mA (000) (OTG pin = Lo) or 500 mA (OTG pin = Hi) Default DCP/CDP: 3 A (111) Default Divider 1 and 2 : 2 A (110) Default Divider 3 : 1 A (100)
Bit 1	IINLIM[1]	R/W	x		
Bit 0	IINLIM[0]	R/W	x		

Copyright © 2023 Texas Instruments Incorporated

9.6.1.2 Power-On Configuration Register REG01 [reset = 00011011, or 0x1B]

図 9-20. Power-On Configuration Register REG01 Format

7	6	5	4	3	2	1	0
Register Reset	I^2C Watchdog Timer Reset	OTG_CONFIG	CHG_CONFIG	SYS_MIN[2]	SYS_MIN[1]	SYS_MIN[0]	BOOST_LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-8. Power-On Configuration Register REG01 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	Register Reset	R/W	0	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Note: Register Reset bit does not reset device to default mode
Bit 6	I^2C Watchdog Timer Reset	R/W	0	0 – Normal ; 1 – Reset	Default: Normal (0) Note: Consecutive I^2C watchdog timer reset requires minimum 20-µs delay
Charger Configuration					
Bit 5	OTG_CONFIG	R/W	0	0 – OTG Disable; 1 – OTG Enable(1)	Default: OTG disable (0) Note: OTG_CONFIG would over-ride Charge Enable Function in CHG_CONFIG
Bit 4	CHG_CONFIG	R/W	1	0- Charge Disable; 1- Charge Enable(1)	Default: Charge Battery (1)
Minimum System Voltage Limit					
Bit 3	SYS_MIN[2]	R/W	1	0.4 V	Offset: 3.0 V, Range 3.0 V – 3.7 V Default: 3.5 V (101)
Bit 2	SYS_MIN[1]	R/W	0	0.2 V	
Bit 1	SYS_MIN[0]	R/W	1	0.1 V	
Boost Mode Current Limit					
Bit 0	BOOST_LIM	R/W	1	0 – 1 A, 1 – 1.5 A	Default: 1.5 A (1)

(1) The CHG_CONFIG and OTG_CONFIG bits cannot be set at the same time.

Copyright © 2023 Texas Instruments Incorporated

9.6.1.3 Charge Current Control Register REG02 [reset = 01100000, or 60]

図 9-21. Charge Current Control Register REG02 Format

7	6	5	4	3	2	1	0
ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]	BCOLD	FORCE_20PCT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-9. Charge Current Control Register REG02 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Fast Charge Current Limit					
Bit 7	ICHG[5]	R/W	0	2048 mA	Offset: 512 mA Range: 512 – 3008 mA (000000 – 100111) Default: 2048 mA (011000) Note: ICHG higher than 3008mA is not supported
Bit 6	ICHG[4]	R/W	1	1024 mA	
Bit 5	ICHG[3]	R/W	1	512 mA	
Bit 4	ICHG[2]	R/W	0	256 mA	
Bit 3	ICHG[1]	R/W	0	128 mA	
Bit 2	ICHG[0]	R/W	0	64 mA	
Bit 1	BCOLD	R/W	0	Set Boost Mode temperature monitor threshold voltage to disable boost mode 0 – V_{bcold0} (Typ. 76% of REGN or -10°C w/ 103AT thermistor) 1 – V_{bcold1} (Typ. 79% of REGN or -20°C w/ 103AT thermistor)	Default: V_{bcold0} (0)
Bit 0	FORCE_20PCT	R/W	0	0 – ICHG as Fast Charge Current (REG02[7:2]) and IPRECH as Pre-Charge Current (REG03[7:4]) programmed 1 – ICHG as 20% Fast Charge Current (REG02[7:2]) and IPRECH as 50% Pre-Charge Current (REG03[7:4]) programmed	Default: ICHG as Fast Charge Current (REG02[7:2]) and IPRECH as Pre-Charge Current (REG03[7:4]) programmed (0)

9.6.1.4 Pre-Charge/Termination Current Control Register REG03 [reset = 00010001, or 0x11]

図 9-22. Pre-Charge/Termination Current Control Register REG03 Format

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-10. Pre-Charge/Termination Current Control Register REG03 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Pre-Charge Current Limit					
Bit 7	IPRECHG[3]	R/W	0	1024 mA	Offset: 128 mA, Range: 128 mA – 2048 mA Default: 256 mA (0001)
Bit 6	IPRECHG[2]	R/W	0	512 mA	
Bit 5	IPRECHG[1]	R/W	0	256 mA	
Bit 4	IPRECHG[0]	R/W	1	128 mA	
Termination Current Limit					

Copyright © 2023 Texas Instruments Incorporated

表 9-10. Pre-Charge/Termination Current Control Register REG03 Field Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 3	ITERM[3]	R/W	0	1024 mA	Offset: 128 mA Range: 128 mA – 2048 mA Default: 256 mA (0001)
Bit 2	ITERM[2]	R/W	0	512 mA	
Bit 1	ITERM[1]	R/W	0	256 mA	
Bit 0	ITERM[0]	R/W	1	128 mA	

9.6.1.5 Charge Voltage Control Register REG04 [reset = 10110010, or 0xB2]

図 9-23. Charge Voltage Control Register REG04 Format

7	6	5	4	3	2	1	0
VREG[5]	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	BATLOWV	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-11. Charge Voltage Control Register REG04 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charge Voltage Limit					
Bit 7	VREG[5]	R/W	1	512 mV	Offset: 3.504 V Range: 3.504 V – 4.400 V Default: 4.208 V (101100)
Bit 6	VREG[4]	R/W	0	256 mV	
Bit 5	VREG[3]	R/W	1	128 mV	
Bit 4	VREG[2]	R/W	1	64 mV	
Bit 3	VREG[1]	R/W	0	32 mV	
Bit 2	VREG[0]	R/W	0	16 mV	
Bit 1	BATLOWV	R/W	1	0 – 2.8 V, 1 – 3.0 V	Default: 3.0 V (1) (pre-charge to fast charge)
Battery Recharge Threshold (below battery regulation voltage)					
Bit 0	VRECHG	R/W	0	0 – 100 mV, 1 – 300 mV	Default: 100 mV (0)

9.6.1.6 Charge Termination/Timer Control Register REG05 [reset = 10011010, or 0x9A]

図 9-24. Charge Termination/Timer Control Register REG05 Format

7	6	5	4	3	2	1	0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER[1]	CHG_TIMER[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-12. Charge Termination/Timer Control Register REG05 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charging Termination Enable					
Bit 7	EN_TERM	R/W	1	0 – Disable, 1 – Enable	Default: Enable termination (1)
Bit 6	Reserved	R/W	0	0 - Reserved	
I2C Watchdog Timer Setting					
Bit 5	WATCHDOG[1]	R/W	0	00 – Disable timer, 01 – 40 s, 10 – 80 s, 11 – 160 s	Default: 40 s (01)
Bit 4	WATCHDOG[0]	R/W	1		
Charging Safety Timer Enable					
Bit 3	EN_TIMER	R/W	1	0 – Disable, 1 – Enable	Default: Enable (1)
Fast Charge Timer Setting					

Copyright © 2023 Texas Instruments Incorporated

表 9-12. Charge Termination/Timer Control Register REG05 Field Description (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 2	CHG_TIMER[1]	R/W	1	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 12 hrs (10) (See *Charging Safety Timer* for details)
Bit 1	CHG_TIMER[0]	R/W	0		
Bit 0	Reserved	R/W	0	0 - Reserved	

Copyright © 2023 Texas Instruments Incorporated

9.6.1.7 Boost Voltage/Thermal Regulation Control Register REG06 [reset = 01110011, or 0x73]

図 9-25. Boost Voltage/Thermal Regulation Control Register REG06 Format

7	6	5	4	3	2	1	0
BOOSTV[3]	BOOSTV[2]	BOOSTV[1]	BOOSTV[0]	BHOT[1]	BHOT[0]	TREG[1]	TREG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-13. Boost Voltage/Thermal Regulation Control Register REG06 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	BOOSTV[3]	R/W	0	512 mV	Offset: 4.55 V Range: 4.55 V – 5.51 V Default:4.998 V (0111)
Bit 6	BOOSTV[2]	R/W	1	256 mV	
Bit 5	BOOSTV[1]	R/W	1	128 mV	
Bit 4	BOOSTV[0]	R/W	1	64 mV	
Bit 3	BHOT[1]	R/W	0	Set Boost Mode temperature monitor threshold voltage to disable boost mode Voltage to disable boost mode 00 – V_{bhot1} (33% of REGN or 55°C w/ 103AT thermistor) 01 – V_{bhot0} (36% of REGN or 60°C w/ 103AT thermistor) 10 – V_{bhot2} (30% of REGN or 65°C w/ 103AT thermistor) 11 – Disable boost mode thermal protection.	Default: V_{bhot1} (00) Note: For BHOT[1:0] = 11, boost mode operates without temperature monitor and the NTC_FAULT is generated based on V_{bhot1} threshold
Bit 2	BHOT[0]	R/W	0		
Thermal Regulation Threshold					
Bit 1	TREG[1]	R/W	1	00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C	Default: 120°C (11)
Bit 0	TREG[0]	R/W	1		

Copyright © 2023 Texas Instruments Incorporated

9.6.1.8 Misc Operation Control Register REG07 [reset = 01001011, or 4B]

図 9-26. Misc Operation Control Register REG07 Format

7	6	5	4	3	2	1	0
DPDM_EN	TMR2X_EN	BATFET_Disable	Reserved	Reserved	Reserved	INT_MASK[1]	INT_MASK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

表 9-14. Misc Operation Control Register REG07 Field Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Force DPDM detection					
Bit 7	IINDET_EN	R/W	0	0 – Not in Input current limit detection; 1 – Force Input current limit detection when VBUS power is presence	Default: Not in Input current limit detection (0), Back to 0 after detection complete
Safety Timer Setting during Input DPM and Thermal Regulation					
Bit 6	TMR2X_EN	R/W	1	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
Force BATFET Off					
Bit 5	BATFET_Disable	R/W	0	0 – Allow BATFET (Q4) turn on, 1 – Turn off BATFET (Q4)	Default: Allow BATFET (Q4) turn on(0)
Bit 4	Reserved	R/W	0	0 - Reserved	
Bit 3	Reserved	R/W	1	1 - Reserved	
Bit 2	Reserved	R/W	0	0 - Reserved	
Bit 1	INT_MASK[1]	R/W	1	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	R/W	1	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

9.6.1.9 System Status Register REG08

図 9-27. System Status Register REG08 Format

7	6	5	4	3	2	1	0
VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	DPM_STAT	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 9-15. System Status Register REG08 Field Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	VBUS_STAT[1]	R	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	R	
Bit 5	CHRG_STAT[1]	R	00 – Not Charging, 01 – Pre-charge (<$V_{BATLOWV}$), 10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	R	
Bit 3	DPM_STAT	R	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	R	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	R	0 – Normal, 1 – In Thermal Regulation

Copyright © 2023 Texas Instruments Incorporated

表 9-15. System Status Register REG08 Field Description (continued)

BIT	FIELD	TYPE	DESCRIPTION
Bit 0	VSYS_STAT	R	0 – Not in VSYSMIN regulation (BAT > VSYSMIN), 1 – In VSYSMIN regulation (BAT < VSYSMIN)

9.6.1.10 New Fault Register REG09

図 9-28. New Fault Register REG09 Format

7	6	5	4	3	2	1	0
WATCHDOG_FAULT	OTG_FAULT	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	Reserved	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 9-16. New Fault Register REG09 Field Description(1) (2) (3)

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	WATCHDOG_FAULT	R	0 – Normal, 1- Watchdog timer expiration
Bit 6	OTG_FAULT	R	0 – Normal, 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that cannot start boost function)
Bit 5	CHRG_FAULT[1]	R	00 – Normal, 01 – Input fault (OVP or bad source), 10 - Thermal shutdown, 11 – Charge Timer Expiration
Bit 4	CHRG_FAULT[0]	R	
Bit 3	BAT_FAULT	R	0 – Normal, 1 – Battery OVP
Bit 2	Reserved	R	Reserved – 0
Bit 1	NTC_FAULT[1]	R	0-Normal 1–Cold Note: Cold temperature threshold is different based on device operates in buck or boost mode
Bit 0	NTC_FAULT[0]	R	0-Normal 1–Hot Note: Hot temperature threshold is different based on device operates in buck or boost mode

(1) REG09 only supports single byte I^2C read.
(2) All register bits in REG09 are latched fault. First time read of REG09 clears the previous fault and second read updates fault register to any fault that still presents.
(3) When adapter is unplugged, input fault (bad source) in CHRG_FAULT bits[5:4] is set to 01 once.

9.6.1.11 Vender / Part / Revision Status Register REG0A

図 9-29. Vender / Part / Revision Status Register REG0A Format

7	6	5	4	3	2	1	0
PN[2]	PN[1]	PN[0]	Reserved	Reserved	Rev[2]	Rev[1]	Rev[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only

表 9-17. Vender / Part / Revision Status Register REG0A Field Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	PN[2]	R	001 (BQ24296) 011 (BQ24297)
Bit 6	PN[1]	R	
Bit 5	PN[0]	R	
Bit 4	Reserved	R	0 – Reserved
Bit 3	Reserved	R	0 – Reserved
Bit 2	Rev[2]	R	000
Bit 1	Rev[1]	R	
Bit 0	Rev[0]	R	

Copyright © 2023 Texas Instruments Incorporated

10 Application and Implementation

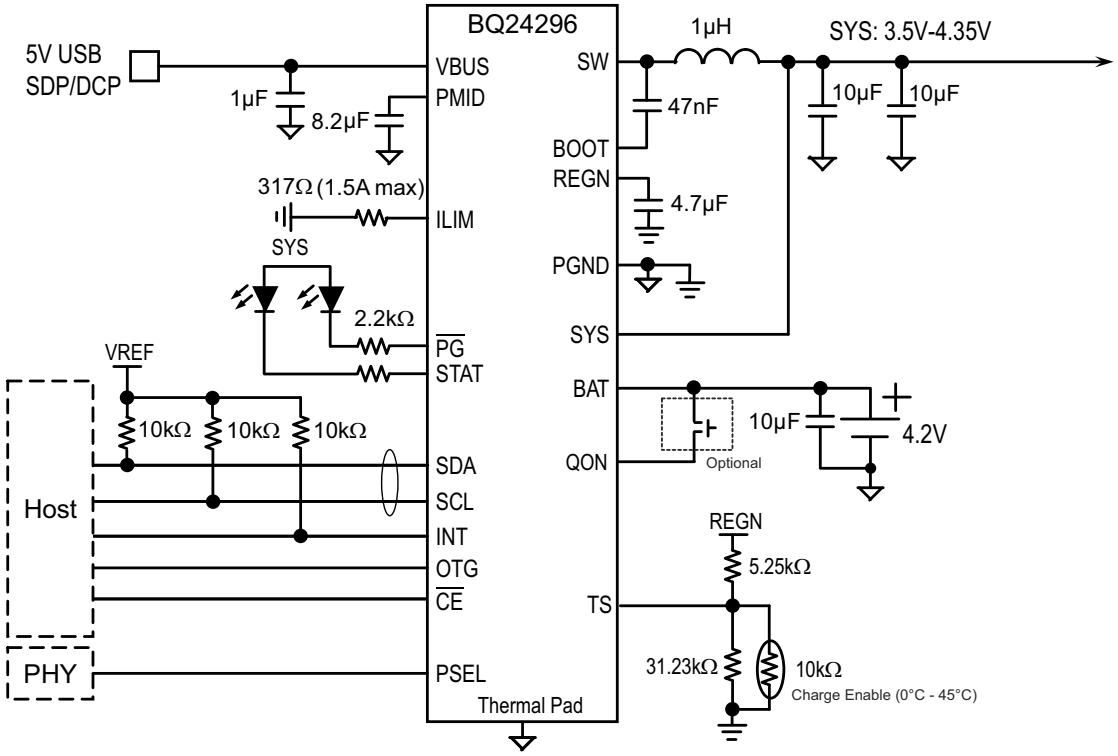
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

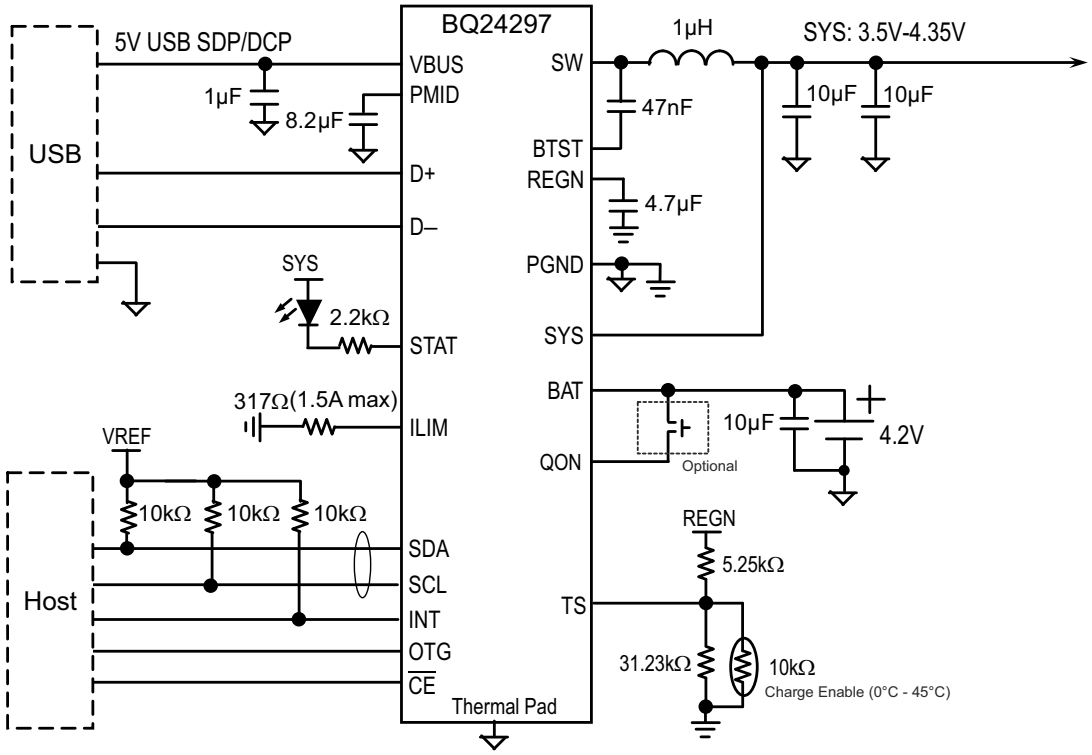
The BQ24296 and BQ24297 evaluation module (EVM) PWR021 is a complete charger module for evaluating the BQ24296 and BQ24297. The application curves were taken using the BQ24296/297 VM-021.

10.2 Typical Application



VREF is the pull up voltage of I2C communication interface.

図 10-1. BQ24296 with PSEL from PHY, Charging from SDP/DCP, and Optional BATFET Enable Interface



VREF is the pull up voltage of I2C communication interface.

図 10-2. BQ24297 with USB D+/D- Detection, USB On-The-Go (OTG) and Optional BATFET Enable Interface

10.2.1 Design Requirements

表 10-1. Design Requirements

DESIGN PARAMATER	EXAMPLE VALUE
Input voltage range	3.9 V to 6.2 V
Input current limit	3000 mA
Fast charge current	3000 mA
Boost mode output current	1.5 A

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The device has 1.5-MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (VBUS), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

Copyright © 2023 Texas Instruments Incorporated

10.2.2.2 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{6}$$

For best performance, VBUS should be decouple to PGND with 1-µF capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for 15-V input voltage. 22-µF capacitance is suggested for typical of 3-A to 4-A charging current.

10.2.2.3 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

The output capacitor voltage ripple can be calculated as follows:

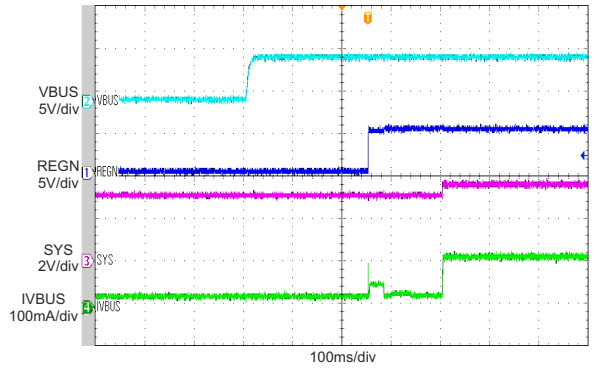
$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{8}$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 36 kHz. The preferred ceramic capacitor is 6 V or higher rating, X7R or X5R.

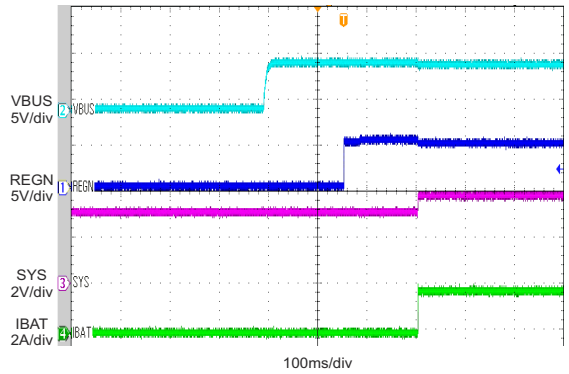
Copyright © 2023 Texas Instruments Incorporated

10.2.3 Application Performance Plots



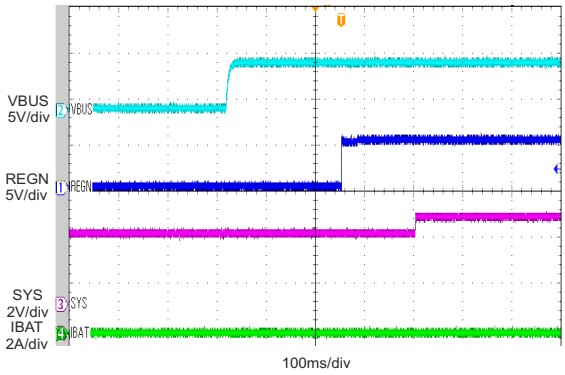
VBAT = 3.2 V

図 10-3. BQ24296 Power Up with Charge Enabled



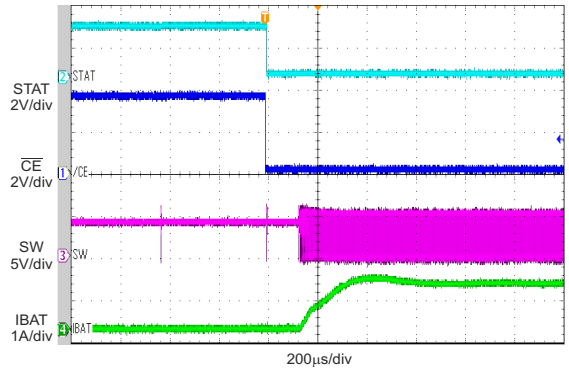
VBAT = 3.2 V

図 10-4. BQ24297 Power Up with Charge Enabled



VBAT = 3.2 V

図 10-5. BQ24297 Power Up with Charge Disabled



VBAT = 5 V

図 10-6. Charge Enable

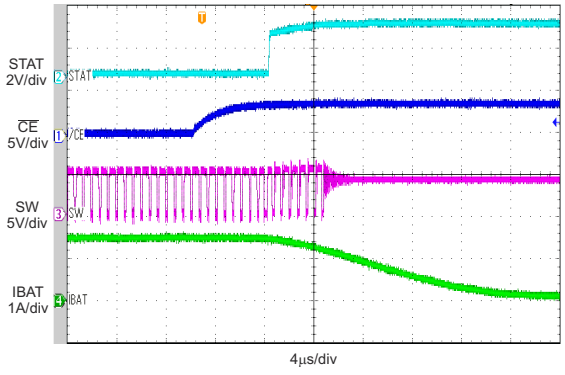
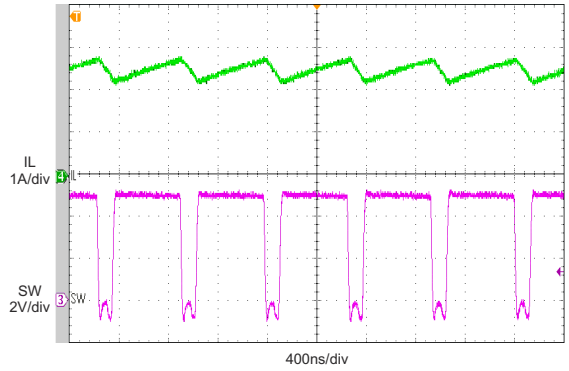


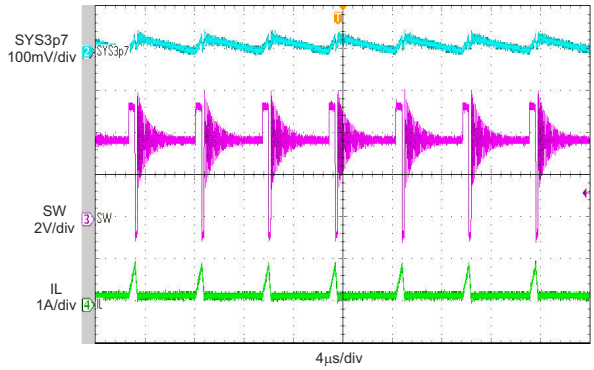
図 10-7. Charge Disable



VBUS = 5 V, No Battery, ISYS = 40 mA, Charge Disable

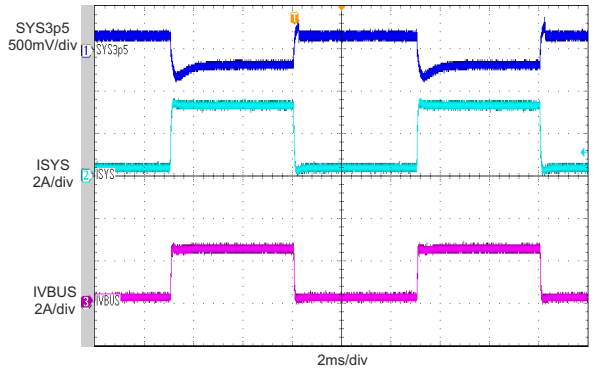
図 10-8. PWM Switching in Buck Mode

Copyright © 2023 Texas Instruments Incorporated



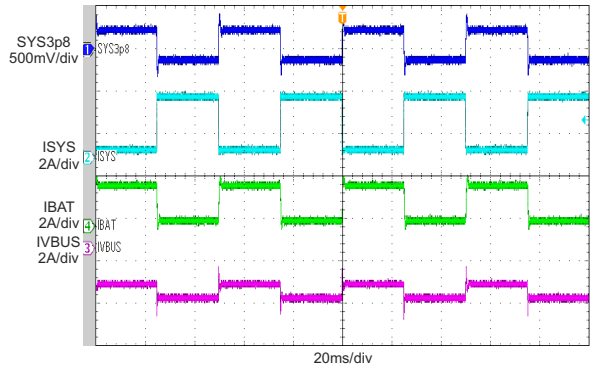
VBUS = 5 V, VBAT = 3.6 V, ICHG = 2.5 A

図 10-9. PFM Switching in Buck Mode



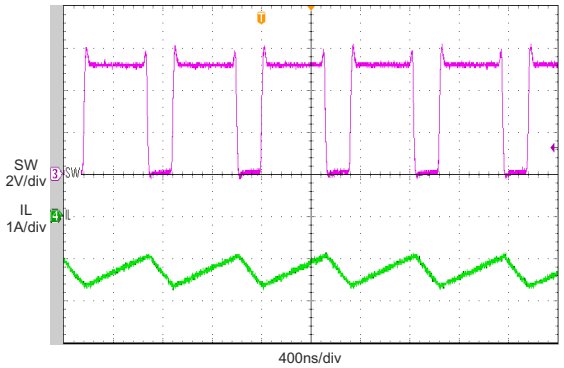
VBUS = 5 V, IIN = 3 A, No Battery, Charge Disable

図 10-10. Input Current DPM Response without Battery



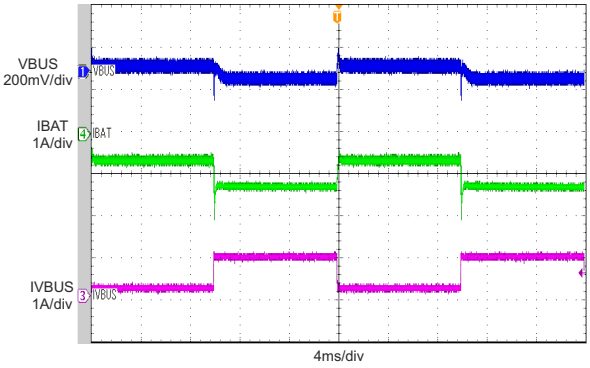
VBUS = 5 V, IIN = 1.5 A, VBAT = 3.8 V

図 10-11. Load Transient During Supplement Mode



VBAT = 3.8 V, ILOAD = 1 A

図 10-12. Boost Mode Switching



VBAT = 3.8 V

図 10-13. Boost Mode Load Transient

Copyright © 2023 Texas Instruments Incorporated

11 Power Supply Recommendations

In order to provide an output voltage on SYS, the BQ24296/297 require a power supply between 3.9 V and 6.2 V input with at least 100-mA current rating connected to V_{BUS}; or, a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

Copyright © 2023 Texas Instruments Incorporated

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 図 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the VQFN information, refer to *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

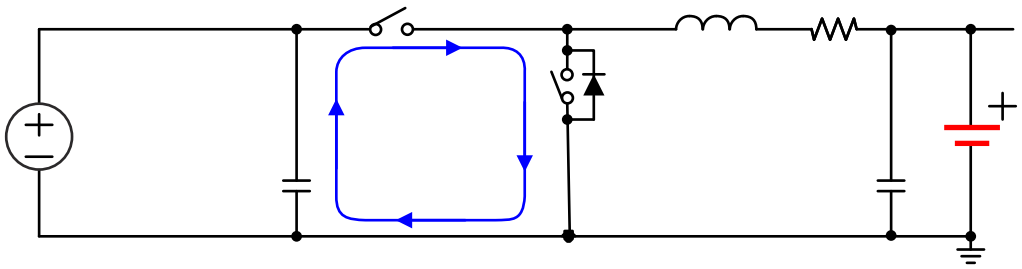


図 12-1. High Frequency Current Path

12.2 Layout Example

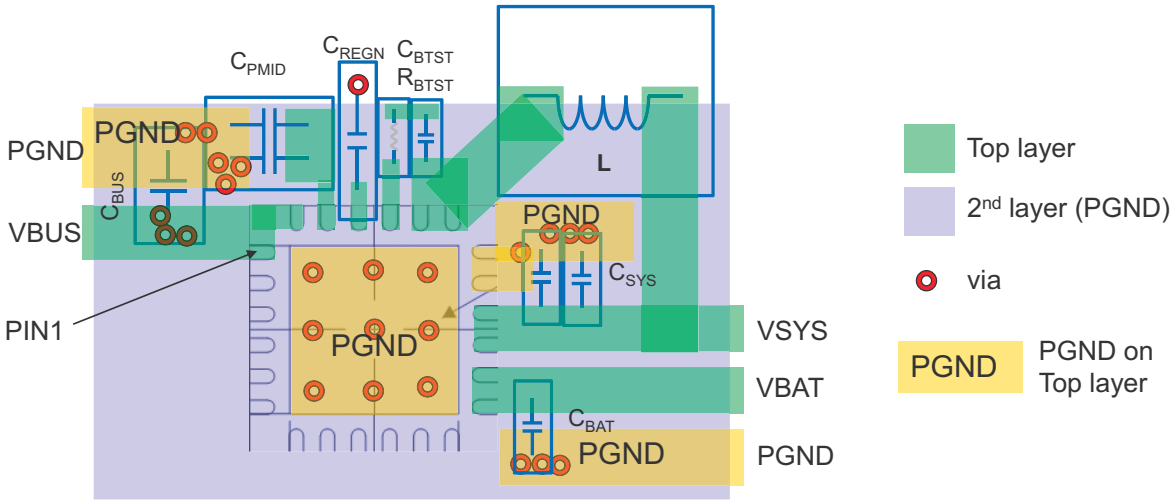


図 12-2. Layout Example

Copyright © 2023 Texas Instruments Incorporated

13 Device and Documentation Support

13.1 Device Support

13.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

13.2 Documentation Support

13.2.1 Related Documentation

BQ24296/7 EVM (PWR021) User's Guide

Quad Flatpack No-Lead Logic Packages Application Report

QFN/SON PCB Attachment Application Report

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2023 Texas Instruments Incorporated

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24296RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24296RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24296RGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24296RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24296RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24296RGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24296
BQ24297RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297
BQ24297RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297
BQ24297RGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297
BQ24297RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297
BQ24297RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297
BQ24297RGET.B	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24297

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

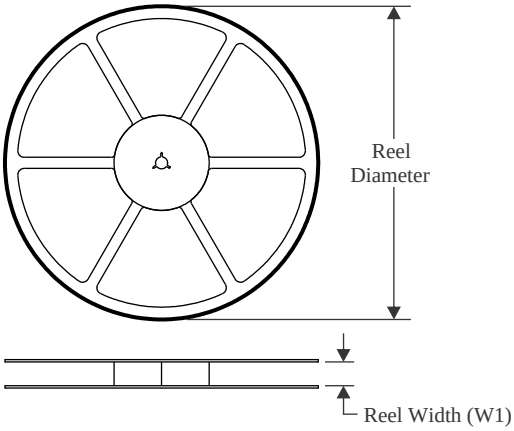
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

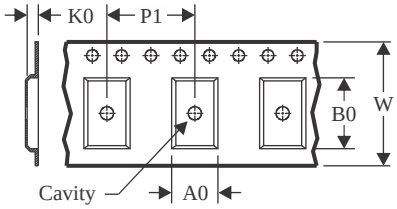
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

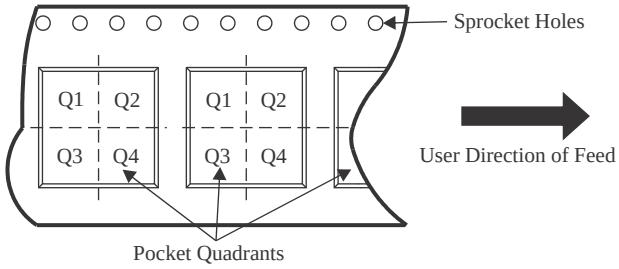


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

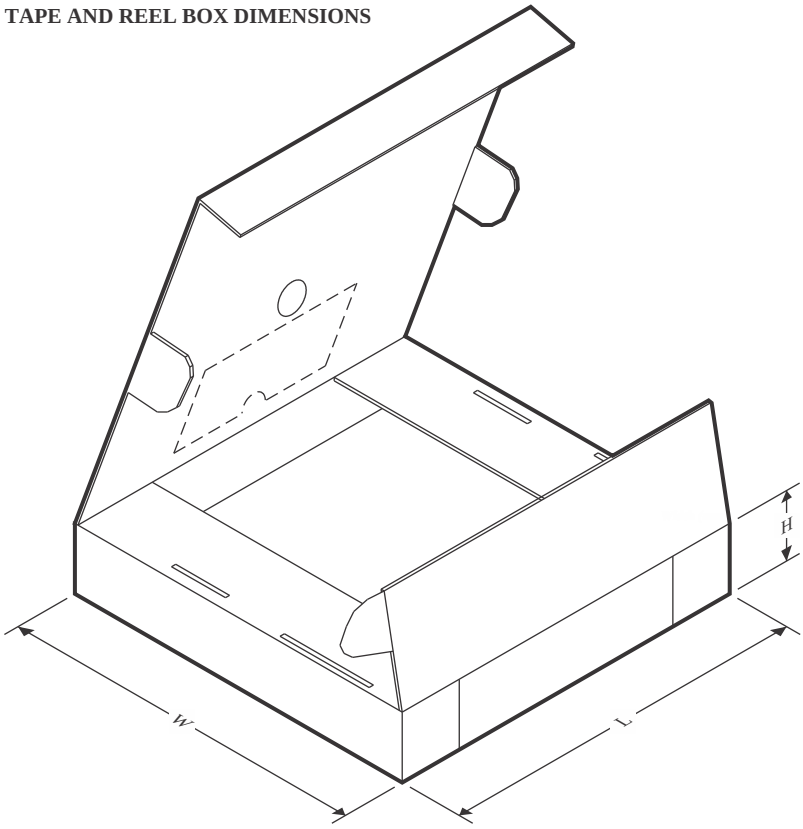
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24296RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24296RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24297RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24297RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



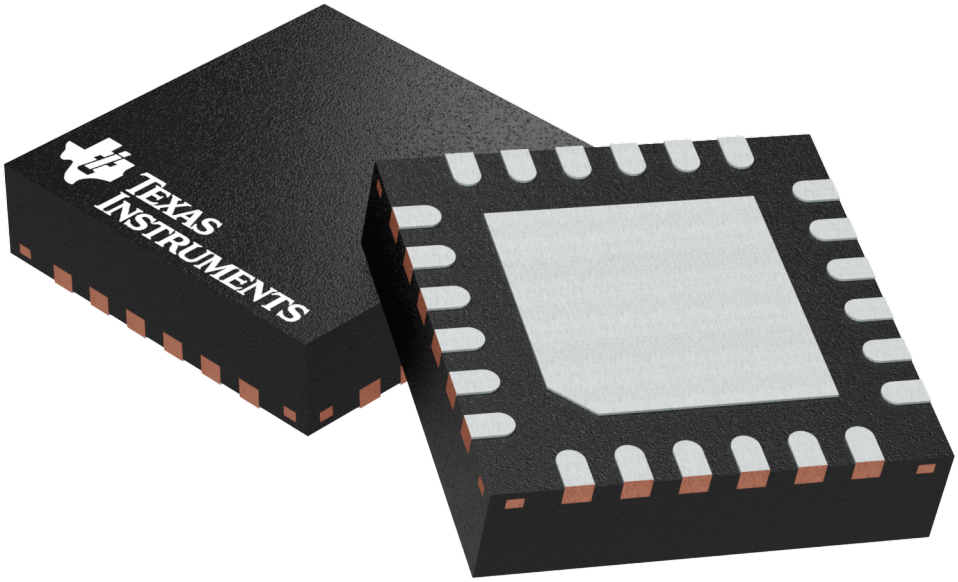
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24296RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
BQ24296RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24297RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
BQ24297RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



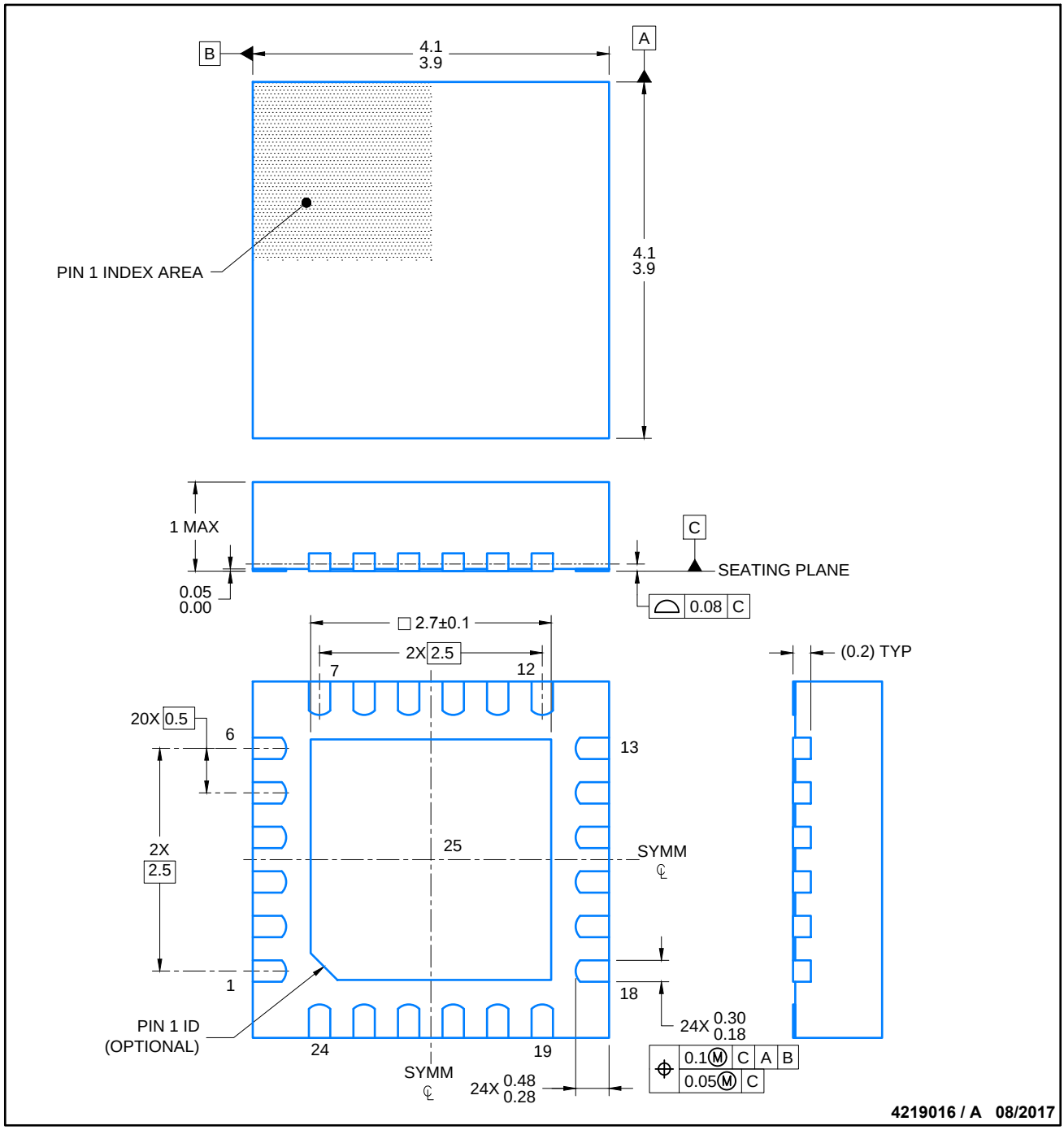
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

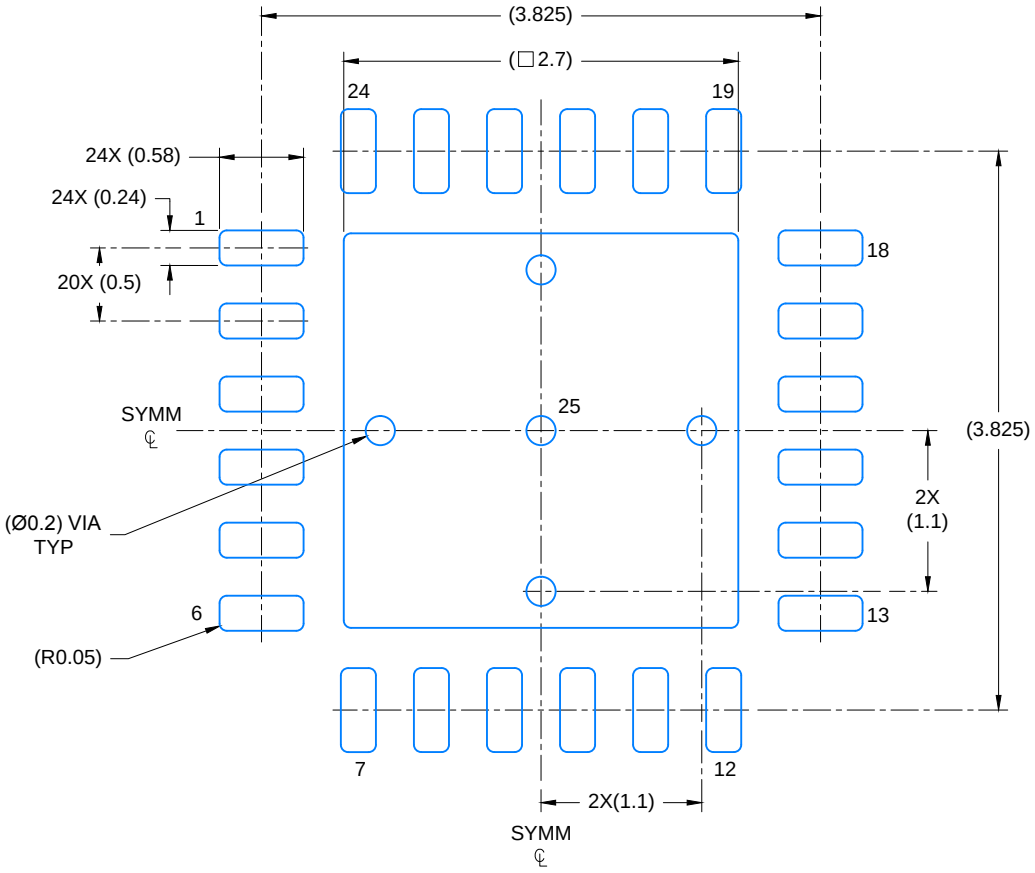
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



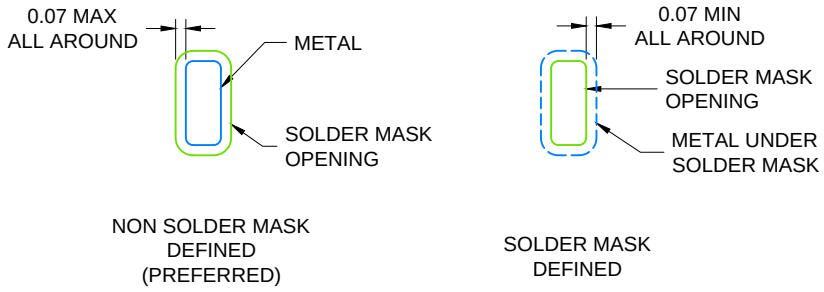
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

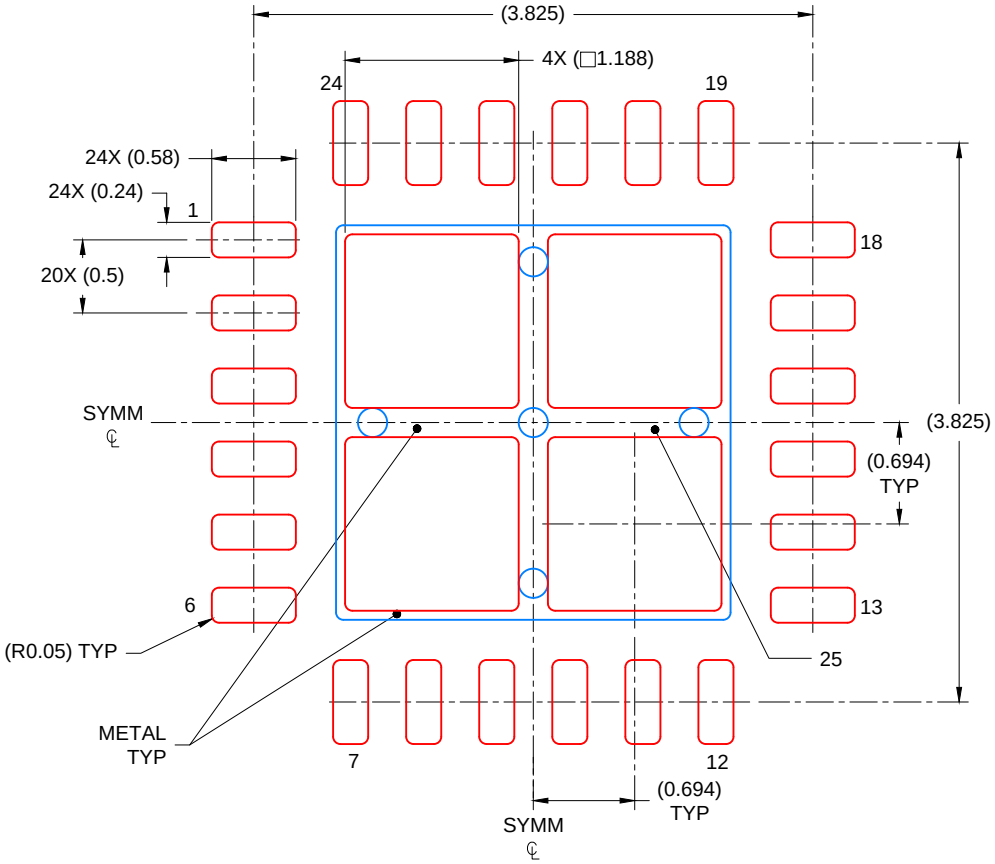


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月