BQ25185 パワー・パス、ファクトリ・モード、バッテリ・トラッキング VINDPM 付き 1 セル、1A スタンドアロン・リニア・バッテリ・チャージャ

1 特長

- 1A リニア・バッテリ・チャージャ
  - 3.0V ~ 18V の入力電圧動作範囲
  - 許容入力電圧 25V
  - 外付け抵抗でプログラム可能な動作：
    - ILIM/VSET でバッテリ・レギュレーション電圧を 3.6V、3.65V、4.02V、4.1V、4.2V、4.35V、4.4V に設定
    - ILIM/VSET で入力電流制限を 100mA、500mA、1100mA に設定
    - ISET による充電電流の設定 (5mA ~ 1A)
  - リチウムイオン電池、リチウムポリマー電池、LiFePO4 電池をサポート
  - 115mΩ バッテリ FET オン抵抗
  - 最大 3.125A の放電電流で高いシステム負荷に対応
- システム電源およびバッテリ充電用のパワー・パス管理
  - 4.5V でレギュレートされたシステム電圧 (SYS)
  - 設定可能な入力電流制限
  - USB サスペンドモードをサポート
  - ハイ・インピーダンス入力ソース用のバッテリ・トラッキング入力電圧ダイナミック・パワー・マネージメント (VINDPM)
  - 動的なパワー・パス管理により、弱いアダプタからの充電を最適化
- 非常に低い静止電流
  - 4μA バッテリ単独モード
  - 30μA 入力アダプタ Iq (スリープ・モード)
  - 出荷モードで 3.2μA のバッテリ放電電流
- フォルト保護機能内蔵
  - 入力過電圧保護 (VIN_OVP)
  - バッテリ低電圧保護 (BUVLO)
  - バッテリ短絡保護 (BATSC)
  - バッテリ過電流保護 (BATOCP)
  - 入力電流制限保護 (ILIM)
  - サーマル・レギュレーション (TREG) およびサーマル・シャットダウン (TSHUT)
  - バッテリ過熱フォルト保護 (TS)
  - 安全タイマ・フォルト
  - ISET および ILIM/VSET ピンの短絡 / 開放保護。

2 アプリケーション

- TWS ヘッドセットと充電ケース
- スマート眼鏡、AR、VR
- スマート・ウォッチ、その他のウェアラブル・デバイス
- リテール・オートメーションおよびペイメント
- ビル・オートメーション

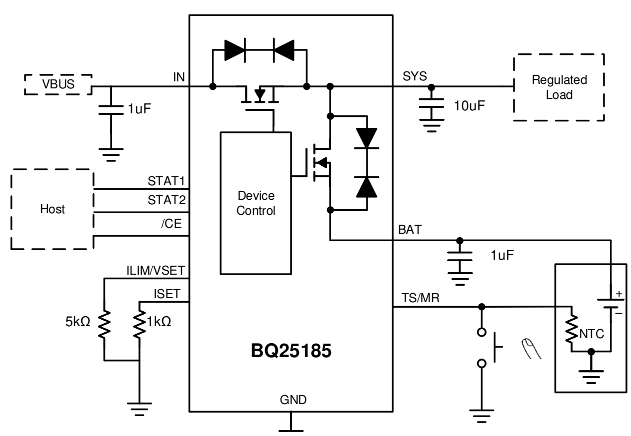
3 概要

BQ25185 は、小さなソリューション・サイズと、バッテリ寿命を延長するための低い静止電流に重点を置いたリニア・バッテリ・チャージャ IC です。このデバイスは、放熱性能を高めるサーマル・パッド付きのリードレス小型パッケージで供給されます。このデバイスは、最大 1A の充電および最大 3.125A のシステム負荷をサポートできます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ(2)	本体サイズ (公称)
BQ25185	DLH (WSON、10)	2.2mm × 2.0mm	2.2mm × 2.0mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 概要 (続き)

バッテリは、標準のリチウムイオンまたは LiFePO4 充電プロファイルを使用して、プリチャージ、定電流、定電圧の 3 つのフェーズで充電されます。サーマル· レギュレーションにより、デバイス温度を管理しながら最大充電電流を供給できます。また、このチャージャは、3V の最小入力電圧で動作するバッテリ間充電に最適化されており、25V の絶対最大ライン過渡電圧に耐えられます。このデバイスには、1 つの押しボタン入力が内蔵されているため、ソリューション全体の占有面積を減らすことができます。

6 Pin Configuration and Functions

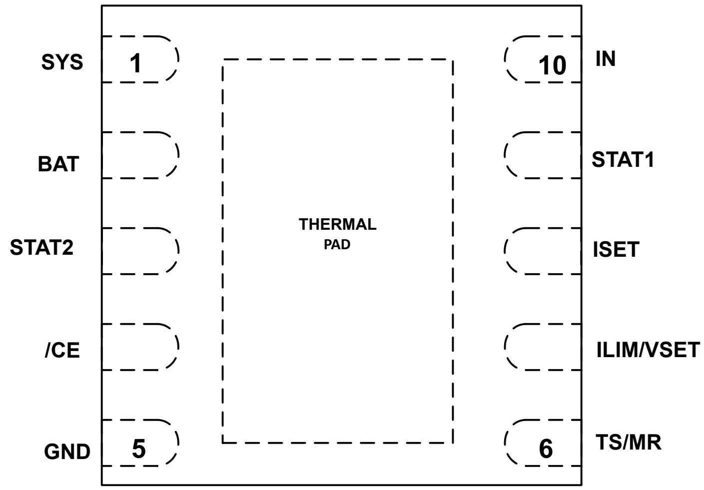


図 6-1. DLH Package 10-Pin (top view)

表 6-1. Pin Functions

Pin Name	Pin NO.	I/O[1]	Description
IN	10	P	DC input power supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1 uF of capacitance using a ceramic capacitor.
SYS	1	P	Regulated system output. Connect at least 10uF ceramic capacitor (at least 1uF of ceramic capacitance with DC bias de-rating) from SYS to GND as close to the SYS and GND pins as possible.
BAT	2	P	Battery connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1uF of ceramic capacitance.
GND	5	-	Ground connection. Connect to the ground plane of the circuit.
ILIM/VSET	7	I/O	Input current limit and battery regulation voltage program input. Refer to ILIM/VSET Control
ISET	8	I/O	Fast charge current program input. We recommend an RC for small charge current values. Prefer to work only with one resistor.
STAT1	9	O	Open drain status output. Can be pulled up to 1- 20kohm resistor. Typical pull up voltage = 1.8V, Max pull up voltage = 5V. Refer to the Status Pins section for more details.
TS/MR	6	I/O	Manual reset input/ NTC thermistor pin. TS/MR is a general purpose input that must be held low for greater than t_{LPRESS} to go into Factory mode. TS/MR may be driven by a momentary push-button or a MOS switch. The TS/MR pin can also have an NTC thermistor connected on to it. Refer to External NTC Montitoring Section (TS) section.
$\overline{CE}$	4	I	Charge enable active-low input. Connect $\overline{CE}$ to a high logic level to disable charging. Connect to a low logic level to enable charging.
STAT2	3	O	Open drain status output. Can be pulled up to 1- 20kohm resistor. Typical pull up voltage = 1.8V, Max pull up voltage = 5V. Refer to the Status Pins section for more details.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input Voltage	IN	-0.3	25	V
Voltage	All other pins	-0.3	5.5	V
Input Current (DC)	IN		1.1	A
SYS Discharge Current(DC)	SYS		3.125	A
Outut Sink Current	STAT1, STAT2		20	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC[1]		BQ25185 DLH 10	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	68.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBAT	Battery Voltage Range	2.2		4.6	V
VIN	Input Voltage Range	2.7		5.5	V
IIN	Input Current Range (IN to SYS)			1.1	A
IBAT	Battery Discharge Current (BAT to SYS)			3.125	A

7.4 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
TJ	Operating Junction Temperature Range	-40		125	°C

7.5 Electrical Characteristics

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{Q_IN}	Input supply quiescent current	VBAT = 3.6V, VIN = 5V, Charge enabled, ICHG = 0mA, SYSREG = 4.5V		0.75	1	mA
I_{SLEEP_IN}	SLEEP input current	VIN = 3.6V, VBAT = 3.7V		30		µA
I_{Q_BAT}	Battery quiescent current	V_{IN} <V_{UVLO} , VBAT =3.6V, 0°C < T_J < 85°C		4	5	µA
I_{BAT_FACT}	Battery discharge current in Factory Mode	VBAT = 3.6 V, 0°C < T_J < 85°C		3.2	5	µA
POWER-PATH MANAGEMENT AND INPUT						
V_{IN_OP}	Input voltage operating range		3.6		18	V
V_{IN_UVLOZ}	Exit IN undervoltage lock-out	IN rising			3	V
V_{IN_UVLO}	Enter IN undervoltage lock-out	IN falling			2.7	V
V_{IN_LOWV}	IN voltage to start charging	IN rising		3	3.15	V
V_{IN_LOWVZ}	IN voltage to stop charging	IN falling		2.95	3.1	V
V_{IN_PORZ}	IN voltage threshold to enter Factory Mode	IN falling	1.09	1.3	1.66	V
V_{SLEEPZ}	Exit sleep mode threshold	IN rising, VIN - VBAT, VBAT= 4V, VINDPM_ACTIVE = 1	122	152	188	mV
V_{SLEEPZ}	Exit sleep mode threshold	IN rising, VIN - VBAT, VBAT= 4V, VINDPM_ACTIVE = 0	168	208	262	mV
V_{SLEEP}	Enter sleep mode threshold	IN falling, VIN - VBAT, VBAT= 4V, VINDPM_ACTIVE = 1		82		mV
V_{SLEEP}	Enter sleep mode threshold	IN falling, VIN - VBAT, VBAT= 4V, VINDPM_ACTIVE = 0		82		mV
V_{SLEEP}	Enter sleep mode threshold	IN falling, VIN - VBAT, VBAT = 4V		82		mV
V_{SLEEPZ}	Exit sleep mode threshold	IN rising, VIN - VBAT, VBAT = 4V	168	208	262	mV
V_{IN_OVP}	VIN overvoltage rising threshold	IN rising	18	18.5	19	V
$V_{IN\_OVP\_HYS}$	IN overvoltage hysteresis	IN falling		500		mV
I_{BAT_OCP}	BATOCP (Reverse OCP only)	VBAT = 4V		3.13		A
I_{BAT_OCPACC}	Battery OCP Accuracy	IBAT= 3.125 A, TJ = 27C			18	%
VBSUP1	Enter supplement mode threshold	VBAT = 3.6V, VBAT > V_{BUVLO}, VSYS< VBAT-VBSUP1		40		mV
VBSUP2	Exit supplement mode threshold	V_{BAT} > V_{BUVLO}, VSYS>VBAT-VBSUP2		20		mV
ILIM	Input Current Limit	VIN = 5V, ILIM=100 mA	80	90	98	mA
		VIN = 5V, ILIM=500 mA	450	475	498	mA
		VIN = 5V, ILIM=1050mA	995	1050	1100	mA
V_{INDPM}	Input voltage threshold when input current is reduced			VBAT + V_{INDPM_TRACK}		V
V_{INDPM_TRACK}	Input voltage threshold offset for when input current is reduced and when VBAT > 3.5 V	VINDPM taget = VBAT + V_{INDPM_TRACK}		330		mV

7.5 Electrical Characteristics (続き)

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DPPM}	SYS voltage threshold when charge current is reduced	VBAT = 3.6V, VSYS = V_{DPPM} + VBAT before charge current is reduced.		0.1		V
V_{SYS_REG}	SYS Regulation Voltage	VIN = 5V, VBATREG <= 4.3 V		4.5		V
$V_{SYS\_REG\_ACC}$	SYS Regulation Accuracy	VIN = 5V, VBAT = 3.6V, RSYS = 100 ohm	-2		2	%
V_{MINSYS}	Minimum SYS voltage when in battery tracking mode	VBAT < 3.6V		3.8		V
R_{SYS_PD}	SYS pull down resistance	V_{SYS} = 3.6V		20		Ω
V_{SYS_SHORT}	Voltage threshold for detecting SYS_SHORT condition has occured	200mV hysteresis		1.6		V
BATTERY CHARGER						
R_{ON_BAT}	Battery FET on-resistance	VBAT = 4.5V, IBAT = 400 mA		115	140	mΩ
R_{ON_IN}	Input FET on-resistance	IN = 5V, IIN = 1A		330	470	mΩ
V_{REG_RANGE}	Typical BAT charge voltage regulation range		3.6		4.4	V
V_{REG_ACC}	BAT charge voltage accuracy, summary for all settings	All VBATREG settings, typical measurement at VBATREG = 4.2V	–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range	V_{BAT} > V_{LOWV}	5		1000	mA
V_{ISET}	ISET pin voltage when in regulation	IBAT = ICHG		1		V
K_{ISET}	Charge current setting factor, I_{CHG} = K_{ISET} / R_{ISET}	10mA < ICHG < 1000mA	285	300	315	AΩ
I_{CHG_ACC}	Charge current accuracy	VIN = 5V, Fastcharge >=40mA	–10		10	%
I_{CHG}	Charge current accuracy at 800 mA	R_{ISET} = 375Ω, OUT = 3.8V	720	800	880	mA
	Charge current accuracy at 500 mA	R_{ISET} = 600Ω, OUT = 3.8V	450	500	550	mA
	Charge current accuracy at 150 mA	R_{ISET} = 2.0kΩ, OUT = 3.8V	135	150	165	mA
	Charge current accuracy at 10 mA	R_{ISET} = 30kΩ, OUT = 3.8V	9	10	11	mA
I_{PRECHG}	Typical pre-charge current, as percentage of ICHG	V_{OUT} < V_{LOWV}		20		%
I_{PRECHG_ACC}	Precharge current accuracy	Fastcharge current >=40mA	–10		10	%
I_{PRECHG_ACC}	Precharge current accuracy at ICHG = 800 mA	R_{ISET} = 375Ω, OUT = 2.5V	144	160	176	mA
I_{PRECHG_ACC}	Precharge current accuracy at ICHG = 500 mA	R_{ISET} = 600Ω, OUT = 2.5V	90	100	110	mA
I_{PRECHG_ACC}	Precharge current accuracy at ICHG = 150 mA	R_{ISET} = 2.0kΩ, OUT = 2.5V	26.5	30	34.5	mA
I_{PRECHG_ACC}	Precharge current accuracy at ICHG = 10 mA	R_{ISET} = 30kΩ, OUT = 2.5V	1.6	2	2.4	mA
I_{TERM}	Typical termination current, as percentage of ICHG	V_{OUT} = VBATREG		10		%
I_{TERM_ACC}	Termination current accuracy	IBAT = 3mA (ICHG= 30mA) Tj = 25°C	–10		10	%
V_{LOWV}	Pre-charge to fast-charge transition threshold	VBAT rising	2.9	3	3.1	V
V_{LOWV_HYS}	Battery LOWV hysteresis			100		mV
V_{BUVLO}	Battery UVLO, VBAT falling			3		V
V_{BUVLO_HYS}	Battery UVLO hysteresis, VBAT rising	VIN = 5V	110	150	190	mV
V_{BUVLO_HYS}	Battery UVLO hysteresis, VBAT rising	VIN = 0V	90	150	210	mV
V_{RCH}	Battery Recharge Threshold	VIN = 5V, Charge Enabled, VBAT falling from VBATREG		100		mV

7.5 Electrical Characteristics (続き)

VIN = 5V, VBAT = 3.6V. -40°C < TJ < 125°C unless otherwise noted. Typical data at TJ = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATSC}	Short on battery threshold for trickle charge, VBAT rising		1.6	1.8	2.0	V
V_{BATSC_HYS}	Battery short circuit voltage hysteresis			200		mV
I_{BATSC}	Trickle Charge Current	VBAT<V_{BATSC}		7		mA
R_{ISET_SHORT}	Resistor value considered short	R_{ISET} below this range at startup, charger does not initiate charge, power cycle or /CE toggle to reset			264	Ω
TERMPERATURE REGULATION AND TEMPERATURE SHUTDOWN						
T_{REG}	Typical junction temperature regulation			100		°C
T_{SHUT_RISING}	Thermal shutdown rising threshold	Temperature increasing		150		°C
$T_{SHUT\_FALLING}$	Thermal shutdown falling threshold	Temperature decreasing		135		°C
BATTERY NTC MONITOR						
V_{HOT_ENTRY}	High Temperature trip point	Battery Charging, $V_{TS/MR}$ falling	0.1050	0.1150	0.1250	V
V_{COLD_ENTRY}	Low Temperature trip point	Battery Charging, $V_{TS/MR}$ rising	0.9575	1.0075	1.0575	V
V_{HOT_EXIT}	Hysteresis on high trip point	Battery Charging, $V_{TS/MR}$ rising from V_{HOT_ENTRY}	0.1250	0.1350	0.1450	V
V_{COLD_EXIT}	Hysteresis on low trip point	Battery Charging, $V_{TS/MR}$ falling from V_{COLD_ENTRY}	0.7775	0.8200	0.8600	V
PUSH BUTTON TIMERS AND THRESHOLDS						
I_{TSMR}	Adapter present		36.5	38	39.5	µA
V_{TSMR}	TSMR voltage to detect a button press event, adapter present				90	mV
t_{LPRESS}	Long Press timer. Time from button press detection to long press action.			10		s
BATTERY CHARGING TIMERS						
t_{MAXCHG}	Charge safety timer			720		min
t_{PRECHG}	Precharge safety timer			0.25 * t_{MAXCHG}		
LOGIC PINS						
V_{IL}	Input low threshold level	VPULLUP = 1.8V, /CE pin			0.4	V
V_{IH}	Input high threshold level	VPULLUP = 1.8V, /CE pin	1.3			V
V_{OL}	Output low threshold level	IL = 5mA, sink current, V_{PULLUP} =3.3V, STAT1, STAT2 pins			0.4	V
I_{LKG}	High-Level leakage current	V_{PULLUP} = 3.3V, STAT1, STAT2 pins			1	µA

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
INPUT					
$t_{VIN\_OVPZ\_DGL}$	VIN_OVP deglitch, VIN falling		30		ms
BATTERY CHARGER					
t_{REC_SC}	Recovery time, BATOCP during Discharge Mode		250		ms
t_{RETRY_SC}	Retry window for SYS or BAT short circuit recovery(BATOCP)		2		s
t_{BUVLO}	Deglitch time to disconnect the BATFET when VBAT < V_{BUVLO} setting		60		µs

7.7 Typical Characteristics

VIN = 5 V, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, C_{BAT} = 1 µF (unless otherwise specified)

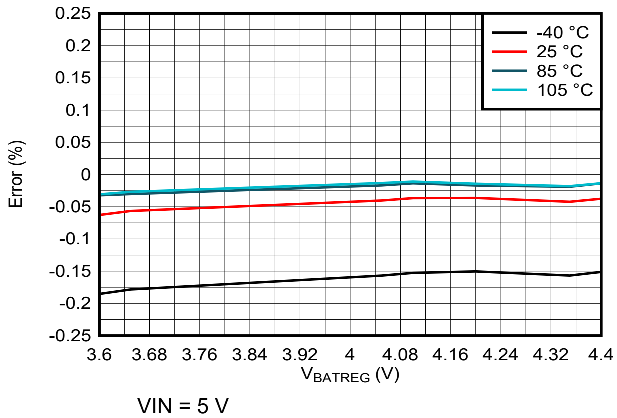


図 7-1. Battery Regulation Voltage Accurary vs. VBATREG Setting

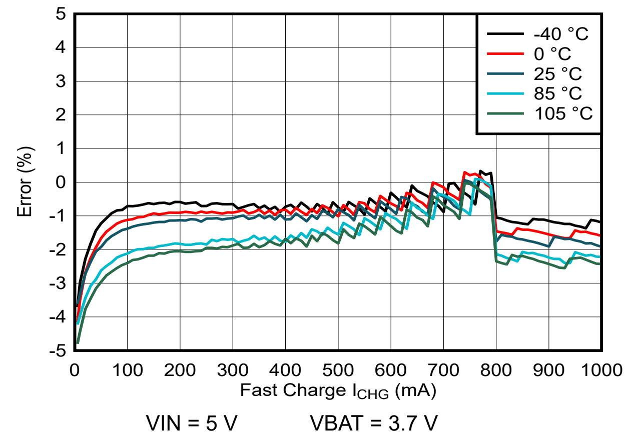


図 7-2. Charge Current Accuracy vs. ICHARGE Setting

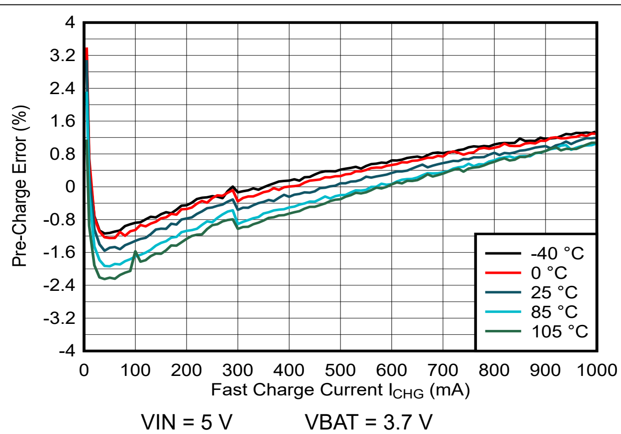


図 7-3. Precharge Accuracy vs Battery Voltage

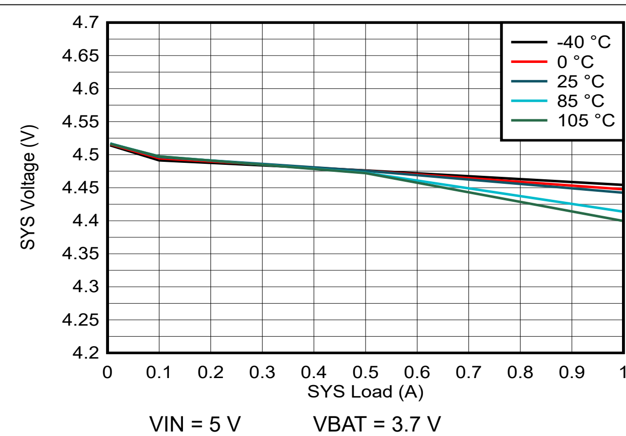


図 7-4. SYS Load Regulation

8 Detailed Description

8.1 Overview

The BQ25185 integrates a linear charger that allows the battery to be charged with a resistor configurable charge current of up to 1 A. In addition to the charge current, other charging parameters can be programmed through external resistors such as battery regulation voltage and input current limit.

The power path allows the system to be powered from a regulated output, SYS, even when the battery is empty or charging, by drawing power from IN pin. It also prioritizes the system load in SYS, reducing the charging current, if necessary, in order support the load when input power is limited. If the input supply is removed and the battery voltage level is above V_{BUVLO}, SYS will automatically and seamlessly switch to battery power.

Charging is done through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, thermal regulation, VDPPM, and VINDPM. During the charging process, all loops are enabled and the one that is dominant takes control.

The device supports multiple battery chemistries for single-cell applications, through adjustable battery regulation voltage regulation (V_{BATREG}) and charge current (I_{CHG}) options.

8.1.1 Battery Charging Process

When a valid input source is connected ($V_{IN} > V_{INDPM}$ and $V_{BAT} + V_{SLEEP} < V_{IN} < V_{IN\_OVP}$), the state of the $\overline{CE}$ pin and the TS/MR pin determines whether a charge cycle is initiated. When the $\overline{CE}$ pin is set to disable charging, $V_{HOT} < V_{TS/MR} < V_{COLD}$ and a valid input source is connected, the battery FET is turned off, preventing any kind of charging of the battery. Note that supplement behavior is independent of the $\overline{CE}$ pin. The device will be able to charge a battery as long as VIN voltage is higher than the V_{INDPM} threshold. This threshold is present as the VIN can be considered "powergood" with a very low battery voltage or a 0-V battery.

The following figure illustrates a typical charge cycle.

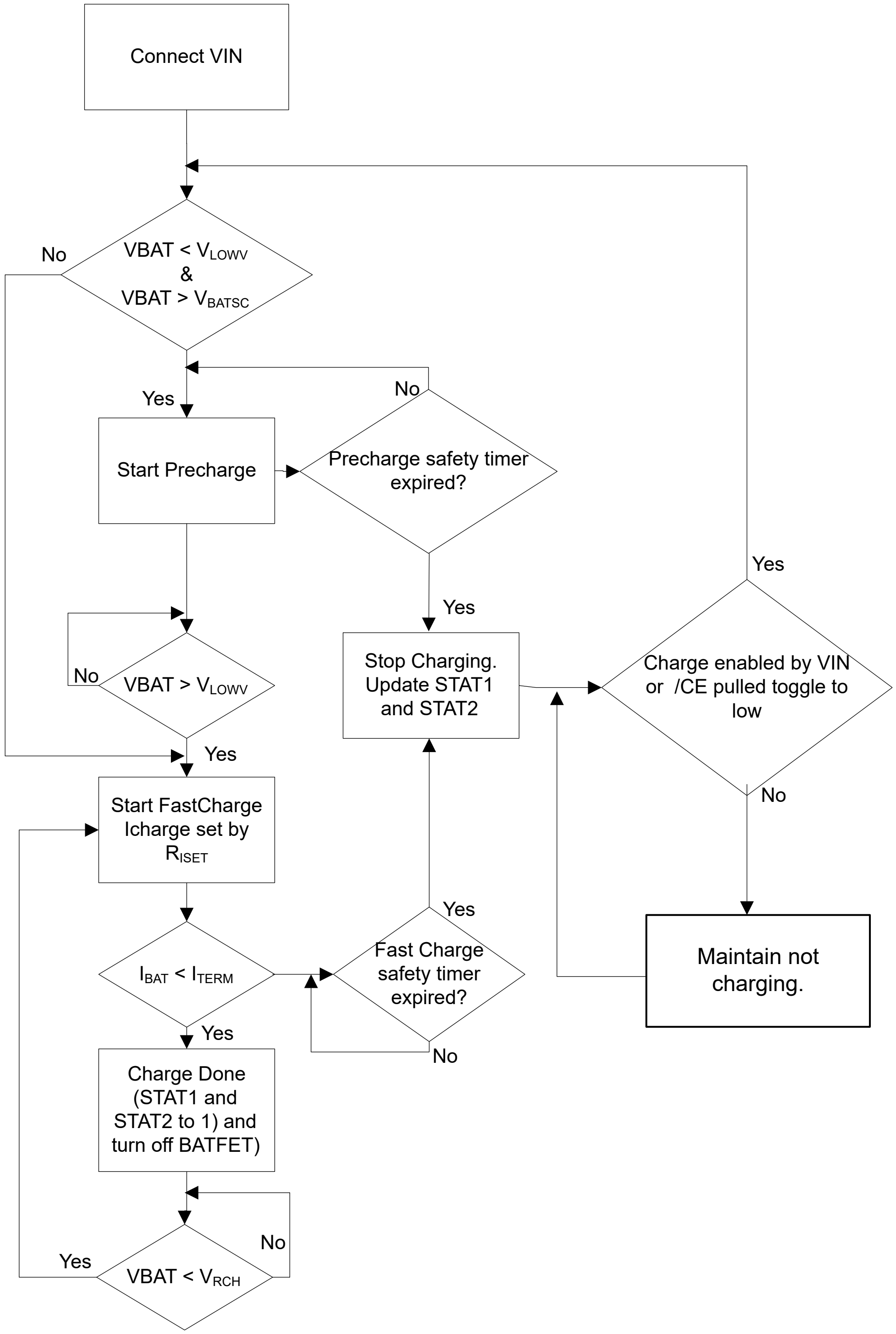


図 8-1. Charger Flow Diagram

8.1.1.1 Trickle Charge

In order to prevent damage to the battery, the device will charge the battery at a much lower current level known as trickle charge (I_{BATSC}) when the battery voltage (VBAT) is below the V_{BATSC} threshold. During trickle charge, the device still counts against the precharge safety timer. Rather trickle charge and precharge are counting against the same duration of 25% of the fast charge timer.

8.1.1.2 Pre-Charge

When battery voltage is above the V_{BATSC} but lower than V_{LOWV} threshold, the battery is charged with the pre-charge current (I_{PRECHG}). Pre-charge current is 2x the termination current (Section 8.1.1.5 Termination). As a result, the pre-charge current is 20 % of the fast charge current (I_{CHG}).

When the battery voltage reaches the precharge to fast charge transition threshold (V_{LOWV}), the device charges the battery at the fast charge current. If the device does not exit pre-charge within 25% of the fast charge safety timer, the device will stop charging. For more information on safety timers, see Section 8.3.7.7. Safety Timer.

8.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the Constant Current (CC) and Constant Voltage (CV) loops. When the CC loop is dominant, typically when $V_{BAT} < V_{BATREG} – V_{RCH}$, the battery is charged at the maximum charge current level I_{CHG}, unless there is a TS fault condition, VINDPM is active, thermal regulation or DPPM is active. (See respective sections for details on these modes of operation). Once the battery voltage approaches the V_{BATREG} level, the CV loops becomes more dominant and the charging current starts tapering off as shown in Typical Charging Profile of a Battery. Once the charging current reaches the termination current (I_{TERM}) the charge is done, then the STAT1 and STAT2 pins change to indicate a charge complete .

8.1.1.4 ISET Pin Detection

After valid VIN is plugged in and $\overline{CE}$ pin is pulled LOW, the device checks the resistor on the ISET pin for shortcircuit ($R_{ISET} < R_{ISET\_SHORT}$). If the condition is detected, charger remains in the FAULT state until the input or $\overline{CE}$ pin are toggled. If the ISET pin is open-circuit, the charger will charge with very low charging current in the order of 1.5 mA. This pin is monitored while charging, and changes in R_{ISET} while the charger is operating will immediately translate to changes in charge current. An external pull-down resistor (±1% or better recommended to minimize charge current error) from ISET pin to GND sets the charge current as:

$$I_{CHG} = (K_{ISET}) / (R_{ISET}) \tag{1}$$

- I_{CHG} is the desired fast charge current
- K_{ISET} is a gain factor found in the electrical specification (typically 300 AΩ)
- R_{ISET} is the pull-down resistor from ISET pin to GND

For charge currents below 50 mA, an extra RC circuit using a 50 pF capacitance is recommended on ISET to achieve more stable current signal. The ISET pin can also be used to monitor device current when the device is not in ICHG regulation. The voltage on the ISET pin is proportional to the device charging current. To measure the charge current when the device is charging, the following formula can be used:

$$I_{CHG}=(K_{ISET}\ V_{ISET}) / (R_{ISET}) \tag{2}$$

- V_{ISET} is the measured voltage at the ISET pin in volts.
- I_{CHG} is the calculated measured charge current

8.1.1.5 Termination

As the device CV loop becomes more dominate than the CC loop in fast charge operation, the charge current will taper and approach the I_{TERM} threshold. The device terminates at 10 % of I_{CHG}.

Once the I_{TERM} threshold is met during the CV phase, the device automatically terminates charge current by disabling the BATFET (disconnects the battery from SYS) to enter high impedeance mode. If there is a regulation loop such as VINDPM, DPPM, or a thermal regulation loop that affects the charge current while the CV loop is tapering the charge current, termination will not occur. Charge current will continue to taper due to the active current affecting regulation loops and CV but the device will not terminate the charge current.

Termination only occurs when the CV loop is operating without any other regulation loops in effect that could reduce the charge current further. Post termination, the battery FET is disabled and the device monitors the BAT pin voltage. If the BAT pin voltage has dropped lower than the battery regulation voltage (V_{BATREG}) by the recharge threshold (V_{RCH}), a new charge cycle is started and safety timers are reset.

During charging or even when charge done, a higher SYS load will be supported through the supplement operation.

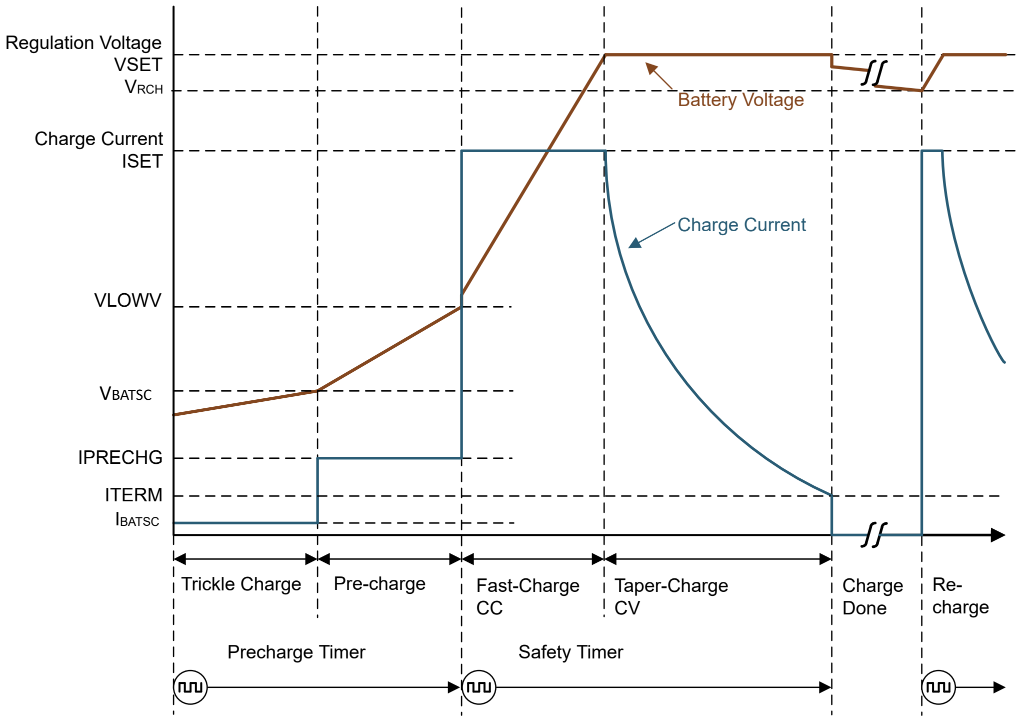
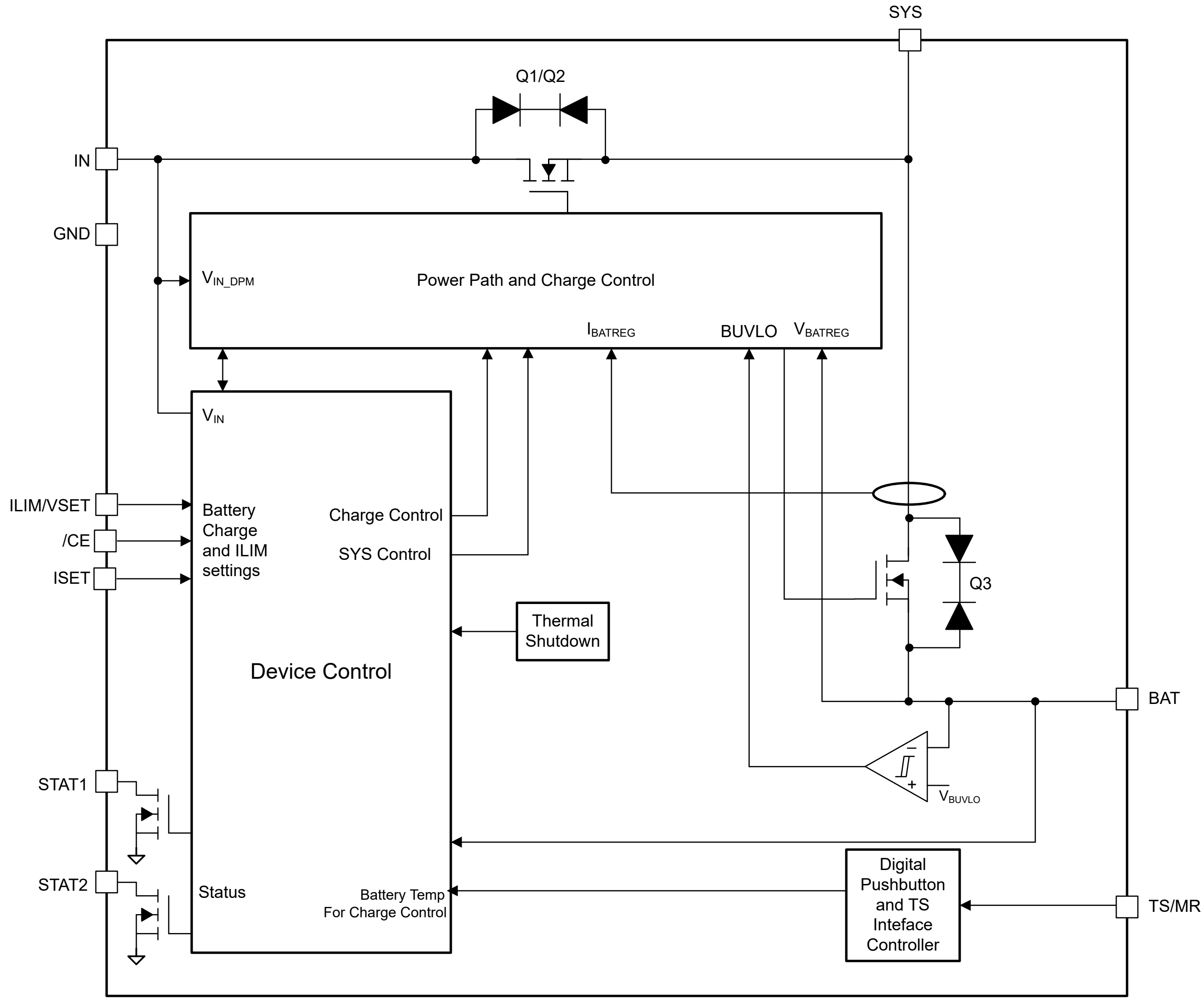


図 8-2. Typical Charging Profile of a Battery

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a point where charging would be interrupted. This is done by reducing the current drawn by charger enough to keep the input voltage above the VINDPM threshold (V_{INDPM}).

During the normal charging process, if the input power source is not able to support the programmed or default charging current and System load, the supply voltage decreases. Once the supply drops to the V_{INDPM} threhold, the input DPM current and voltage loops will reduce the input current through the blocking FETs to prevent the further drop of the supply.

The VINDPM threshold is typically 300 mV above VBAT. If the device is not operating in battery tracking VINDPM due to battery voltage, it will regulate the input to 3.6 V. Additionally, termination is disabled when VINDPM is active.

8.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared at SYS between charging the battery and powering the system load at SYS. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces input current. If SYS drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET. If SYS falls below the supplement mode threshold after BATFET charging current is reduced to zero, the part will enter supplement mode. SYS voltage is maintained above battery voltage when the DPPM loop is in control. Battery termination is disabled when the DPPM loop is active.

The VDPPM threshold is typically 100 mV above VBAT.

8.3.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at SYS reduces further. When the SYS voltage drops below the battery voltage to V_{BSUP1}, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the SYS pin rises within the battery voltage to V_{BSUP2}. During supplement mode, the battery supplement current is not regulated, however, the BATOCP protection circuit is active . Battery termination is disabled while in supplement mode. Battery voltage has to be higher than battery undervoltage lockout threshold (V_{BUVLO}) to be able to supplement the system.

8.3.4 Sleep Mode

The device enters the low-power sleep mode if V_{IN} falls below the sleep-mode entry threshold and V_{IN} is higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery during the absence of V_{IN}. Once V_{IN} > V_{BAT} + V_{SLEEP} and V_{IN} exceeeds the VINDPM threshold, the device initiates a new charge cycle.

8.3.5 SYS Regulation

The BQ25185 includes a SYS voltage regulation loop. By regulating the SYS voltage the device prevents downstream devices connected to SYS from being exposed to voltages as high as VIN_OVP. SYS regulation is only active when V_{IN} > V_{UVLO}, V_{IN} > V_{BAT} + V_{SLEEP} and V_{IN} < VIN_OVP .

For the BQ25185, if the ILIM/VSET is configured for a VBATREG setting higher than 4.3 V, the device regulates the SYS voltage in battery tracking mode. As battery voltage increases, VSYS is regulated to 225 mV above the battery. If the battery is less than 3.6 V, the VSYS will be regulated to V_{MINSYS}. This regulation occurs to ensure proper termination of the battery even if VDDPM is active.

8.3.6 ILIM/VSET Control

The input current limit can be controlled the external programmable resistor as indicated below.

The ILIM/VSET pin will be checked in the following conditions:

- Valid adapter present on V_{IN} (V_{IN} is considered power good)
- Charge Enable pin state is changed to enable.
  - Toggle the /CE pin when the TS/MR pin is not pressed to avoid charging during pin detection.
- TS/MR push button is not pressed.

If an Open is detected on the ILIM/VSET pin- the device will disable charging but regulate the SYS pin and limit the ILIM current to 500mA.

If a Short is detected on the ILIM/VSET pin, the device will stay in battery only mode.

表 8-1. ILIM and VBATREG Resistor Map

RESISTOR (kOhm)	CURRENT LIMIT	V_{BATREG} (V)	V_{LOWV} (V)
> 180	Charge Diabled, ILIM 500		
130	ILIM500	4.1	3.0
100	ILIM1100		
75	ILIM500	4.4	
56	ILIM1100		
43	ILIM500	4.35	
33	ILIM1100		
24	ILIM100	4.2	
18	ILIM500		
13	ILIM1100		
9.1	ILIM500	4.05	
6.8	ILIM1100		
5.1	ILIM1100	3.65	2.0
3.6	ILIM500	3.6	
2.4	ILIM1100		
<1.5	Battery Only Mode		

8.3.7 Protection Mechanisms

8.3.7.1 Input Overvoltage Protection

The input overvoltage protection protects the device and downstream components connected to SYS, and BAT against damage from overvoltage on the input supply. When VIN > V_{IN_OVP}, a VIN overvoltage condition is determined to exist. During the VIN overvoltage condition, the device turns the battery discharge FET on,the STAT1 and STAT2 pins update to reflect a recoverable fault (STAT1 = LOW, STAT2 = HIGH). Once the VIN overvoltage condition is removed, the STAT1 and STAT2 pins update to normal operation once the startup routine has finished due to a power good VIN detection. Thereafter VIN powergood condition is determined if VIN > VBAT + VSLEEP.

8.3.7.2 Battery Undervoltage Lockout

To prevent deep discharge of the battery, the device integrates a battery undervoltage lockout feature that disengages the BAT to SYS path when voltage at the battery drops below the BUVLO voltage.

8.3.7.3 Battery Overcurrent Protection

In order to protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the current on the battery FET exceeds IBAT_OCP. If the BATOCP limit is reached, the battery discharge FET is turned off and the device starts operating in hiccup mode, re-enabling the BATFET t_{REC_SC} (250 ms) after being turned OFF by the over current condition. If the overcurrent condition is triggered upon retry for 4 to 7 consecutive times in a 2-s window, the BATFET shall then remain off until valid VIN is connected (VIN = VIN_POWERGOOD). If the overcurrent condition and hiccup operation occurs while in supplement mode where VIN is already present, VIN must be toggled in order for BATFET to be enabled and start another detection cycle.

8.3.7.4 System Overvoltage Protection

The system overvoltage protection is to prevent the SYS from overshooting to a high voltage due to the input supply. The SYS_OVP will momentarily disconnect the blocking FETs and re-engage when the thresholds have dropped to less than SYS_OVP_FALLING threshold.

SYS_OVP_RISING threshold is 104 to 106% of target SYS voltage and SYS_OVP_FALLING threshold is 101.5 to 103.5% of the target SYS voltage.

8.3.7.5 System Short Protection

System short protection kicks in when the following conditions are met - the adapter connected the device turns ON the input FET for 5 ms and it detects the SYS pin to be shorted (voltage on SYS <V_{SYS_SHORT}). In this scenario, the device will turn OFF the input FET for 200 µs and turn it back ON for 5 ms for SYS to rise above the $V_{SYSSHORT}$ threshold. If after 10 tries, the voltage at SYS does not rise above the $V_{SYSSHORT}$ threshold, the device will disable both the input and BATFET paths and wait on adapter insertion before turning the paths ON again. A 2s timer is implemented to refresh the retry counter. After 2s, the device will check for system short again repeating the 10 attempts if there is a system short.

8.3.7.6 Thermal Protection and Thermal Regulation

During operation, to protect the device from damage due to overheating, the junction temperature of the die, T_J, is monitored. When T_J reaches T_{SHUT_RISING} the device stops charging operation and VSYS is shutdown. If In the case where $T_J > T_{SHUT\_RISING}$ prior to power being applied to the device (either battery or adapter), the input FET or BATFET will not turn ON, regardless of TSMR pin. Thereafter if temperature falls below $T_{SHUT\_FALLING}$ the device will automatically power up if VIN is present or if in Battery Only mode.

During the charging process, to prevent overheating in the device, the device monitors the junction temperature of the die and reduces the charging current once T_J reaches the thermal regulation threshold (T_{REG}). If the charge current is reduced to 0, the battery supplies the current needed to supply the SYS output.

To ensure that the system power dissipation is under the limit of the device. The power dissipated by the device can be calculated using the following equation:

$P_{DISS} = P_{SYS} + P_{BAT}$ Where:

$P_{SYS} = (V_{IN} – V_{SYS}) * I_{IN}$

$P_{BAT} = (V_{SYS} – V_{BAT}) * I_{BAT}$

The die junction temperature, T_J, can be estimated based on the expected board performance using the following equation:

$T_J = T_A + \theta_{JA} * P_{DISS}$

The θ_{JA} is largely driven by the board layout, board layers, copper thickness and the layout. . For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*. Under typical conditions, the time spent in this state is very short.

8.3.7.7 Safety Timer

At the beginning of each charge cycle mode (Precharge or Fast Charge), the device starts the respective mode safety timer. If charging has not terminated before the programmed safety time, t_{MAXCHG} expires or the device does not exit the precharge mode before t_{PRECHG} expires, charging is disabled. The precharge safety timer, t_{PRECHG}, is 25% of t_{MAXCHG}. When a safety timer fault occurs For the device, the STATx pins update to show a non-recoverable fault. The /CE pin or the input power must be toggled in order to clear the safety timer.

8.3.8 Pushbutton Wake and Reset Input

The pushbutton function implemented through TS/MR pin has two main functions. First, it serves as a means to wake the device from ultra-low power modes like Factory mode. Second, it serves as a mean to get device into Factory mode after detecting a long button press.

8.3.8.1 Pushbutton Long Button Press Function - Factory mode

The device will perform factory mode entry when the pushbutton is pressed (TS/MR is held low) for a time t_{LPRESS} while a valid input is present, then removing VIN once the duration is met. Factory Mode is a low I_Q state that turns off the SYS regulation to minimize battery consumption Toggling the /CE pin will restart the timer for the long press button when VIN is present.

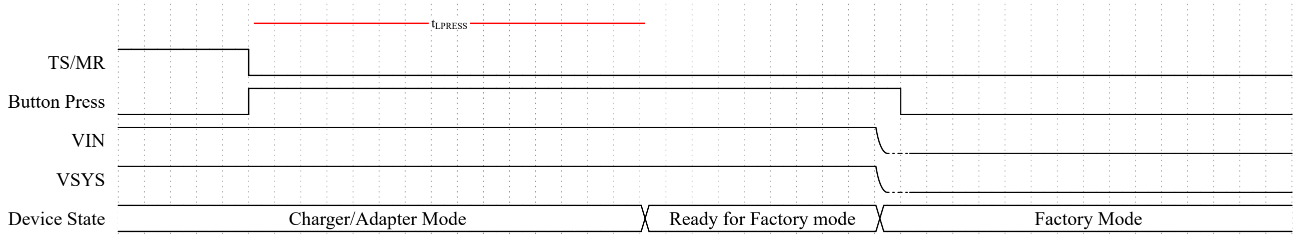


図 8-3. Enter Factory Mode

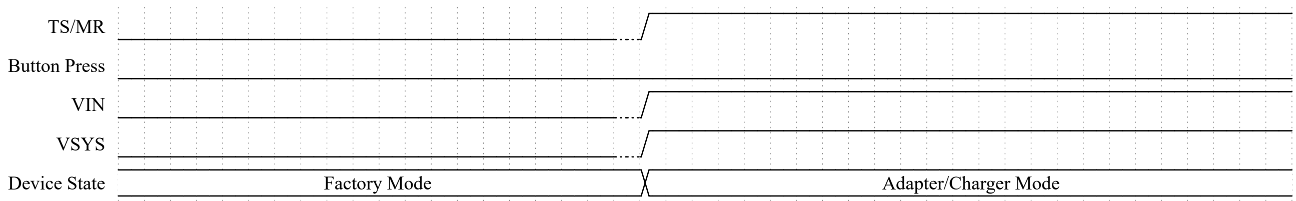


図 8-4. Exit Factory Mode - VIN Insertion

To wake up the device from factory mode, insert a valid VIN. The TS/MR push button cannot be used to wake from Factory Mode.

8.3.9 External NTC Monitoring (TS)

8.3.9.1 TS Biasing and Function

The device is configured to a simpler HOT/COLD function only. Two temperature thresholds are monitored: the cold battery threshold, and the hot battery threshold. These temperatures correspond to the V_{COLD} and V_{HOT} thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$.

For devices where the TS function is not needed, tie a 10-kΩ resistor to the TS/MR pin.

There is an active voltage clamp present on this device which will prevent the voltage on TS/MR pin from rising above the VTS_CLAMP threshold. This will particularly be ON when the TS/MR pin is floating.

When the button is detected as a “press” during the charging process, charging will be momentarily suspended till the button is high again. When charging is disabled in any of the TS faults, the trickle charging is also disabled.

8.3.10 Status Pins

The device has two open drain configuration status pins (STAT1 and STAT2) which can be externally pulled up and either be connected to an LED or an IO pin of an MCU to be able to inform the host or the user on the charger status.

When there is no battery present, the device will charge the capacitor on the BAT pin and toggle between charging done, charge completed. So STAT1 pin will be stable where as STAT2 pin will toggle between HIGH and LOW.

表 8-2. Status Pins State Table

CHARGING STATE	STAT1 PIN STATE	STAT2 PIN STATE
Charge completed, charger in sleep mode or charge disabled (including VBAT >VRCH)	HIGH	HIGH

表 8-2. Status Pins State Table (続き)

CHARGING STATE	STAT1 PIN STATE	STAT2 PIN STATE
Normal Charge in progress (including automatic recharge)	HIGH	LOW
Recoverable fault (VIN_OVP, TS HOT, TS COLD, TSHUT, System Short protection)	LOW	HIGH
Non-recoverable or latch-off fault (ILIM/ISET pin short, BATOCP, Safety TMR_EXP for charging)	LOW	LOW

8.4 Device Functional Modes

The BQ25185 has three main modes of operation: Charger/Adapter Mode (when a supply is connected to IN), Battery Mode (when only battery is connected), and Factory Mode (when battery only but VSYS is turned off). The table below summarizes the functions that are active for each operation mode.

FUNCTION	CHARGER/ADAPTER MODE	BATTERY MODE	FACTORY MODE
Input Overvoltage	Yes	Yes	No
Input Undervoltage	Yes	Yes	Yes
Battery Overcurent	Yes	Yes	Yes
Input DPM	Yes	No	Yes
Dynamic Power Path Management	Yes	No	No
BATFET	Yes	Yes	No
TS Measurement	Yes	No	No
Battery Charging	Yes	No	No
Input Current Limit	Yes (Selected by $R_{ILIM/VSET}$)	No	No
Pushbutton Input	Yes	No	No
Status Pin	Yes	Yes	No

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application of the BQ25185 consists of the device configured as a standalone single cell Li-ion battery charger and power path manager or battery applications such as smart-watches and wireless headsets. A battery thermistor may be connected to the TS pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the TS/MR pin input to a push-button to send interrupts to the host as a button is pressed or to allow the application end user to reset the system.

9.2 Typical Application

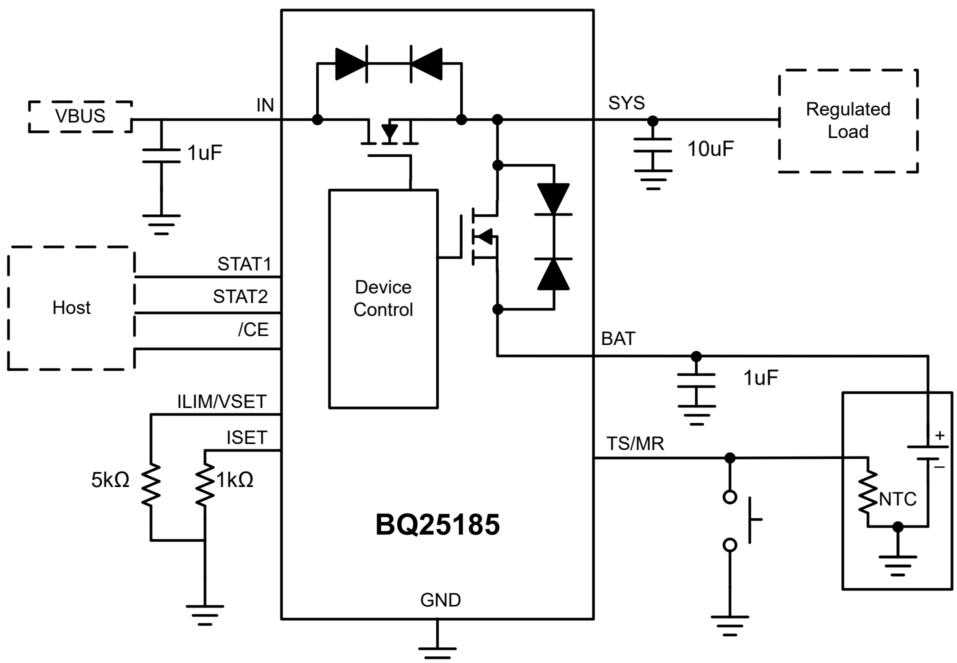


図 9-1. Typical Application

9.2.1 Design Requirements

The design requirements for the following design example are shown in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
IN Supply Voltage	5 V
Battery Regulation Voltage	4.2 V
Fast Charge Current	300 mA
Input Current Limit	500 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Input Current and Battery Regulation Voltage - ILIM/VSET

To configure the device for 4.2 V V_{BATREG} and an input current limit of 500 mA, the $R_{ILIM/VSET}$ resistor is set to 18 kOhm. The resistor value is found in the ILIM Control section.

9.2.2.2 Fast Charge Current- ISET

To configure the device for 300 mA of fast charge current, the R_{ISET} resistor is set to 1 kΩ. The resistor value is calculated based on the equations found in ISET Pin Detection.

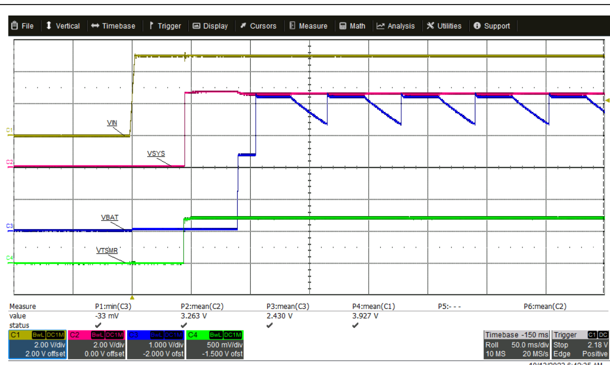
9.2.2.3 Recommended Passive Components

Low ESR ceramic capacitors such as X7R or X5R are preferred for input decoupling capacitors and should be placed as close as possible to the supply and ground pins for the IC. Due to the voltage derating of the capacitors, it is recommended that 25-V rated capacitors are used for the IN and SYS pins which can normally operate at 5 V. After derating the minimum capacitance must be higher than 1 µF.

		MIN	NOM	MAX	UNIT
C_{SYS}	Capacitance on SYS pin	1	10	100	µF
C_{BAT}	Capacitance on BAT pin	1	1	-	µF
C_{IN}	Capacitance on IN pin ($t_{VIN\_PRESENT}$ > 25 ms)	1			µF

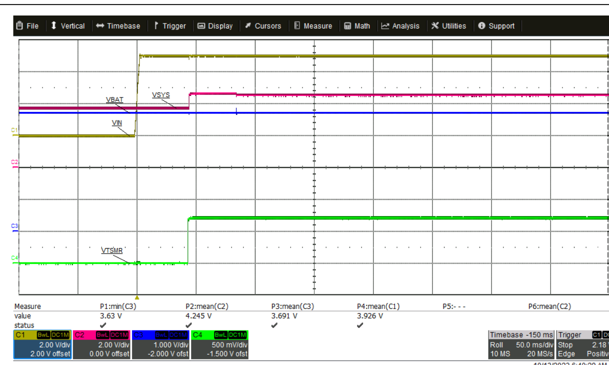
9.2.3 Application Curves

C_{IN} = 1 µF, C_{OUT} = 10 µF, V_{IN} = 5 V, V_{OUT} = 3.7 V, I_{CHG} = 100 mA (unless otherwise specified)



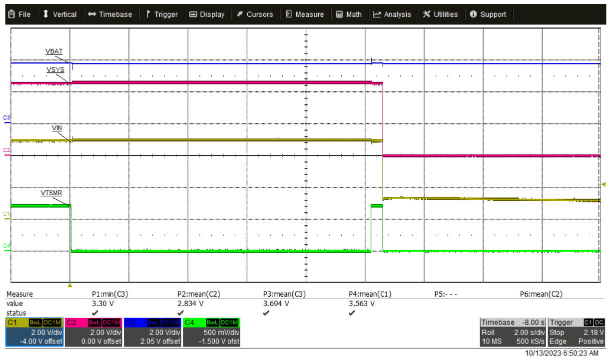
VIN = 5 V VBAT = Floating

図 9-2. Power Up with IN Supply Insertion with No Battery



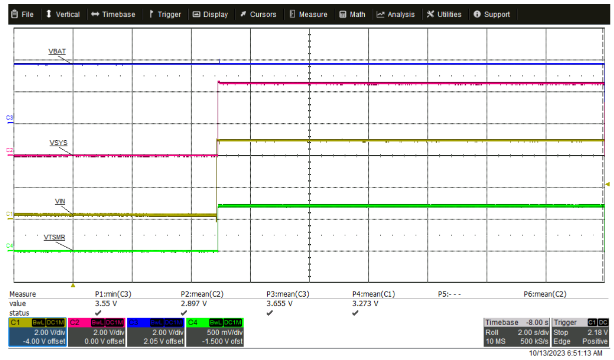
VIN = 5 V VBAT = 3.7 V

図 9-3. Power Up with IN Supply Insertion with Battery



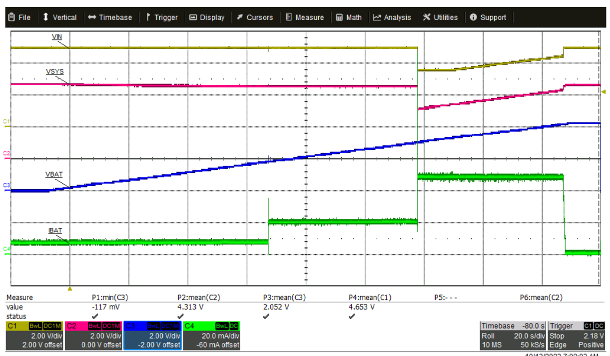
VIN = 5 V → 0V VBAT = 3.7 V

図 9-4. Enter Factory Mode



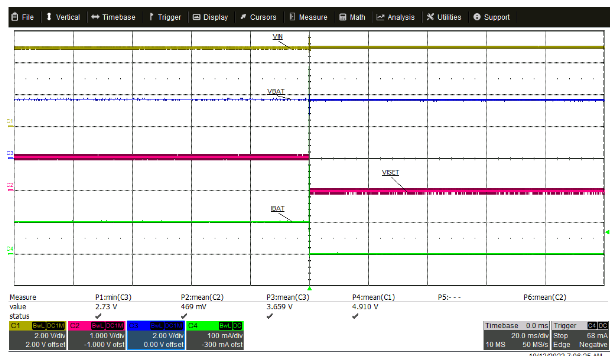
VIN = 0 V → 5 V VBAT = 3.7 V

図 9-5. Wake up from Factory Mode with Adapter Insertion



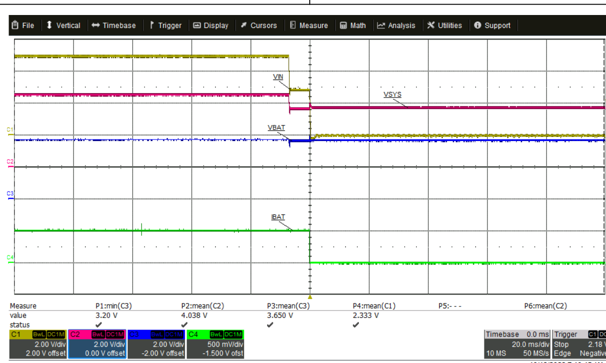
VIN = 5 V VBAT = 3.7 V ICHG = 100 mA
Input Source Current Limit = 50 mA

図 9-6. Battery Tracking VINDPM



ISET Short while charging

図 9-7. ISET Short Protection



VIN = 5V → 0V
VBAT = 3.7 V

図 9-8. VIN Power Down with VBAT Present

9.3 Power Supply Recommendations

The BQ25185 requires the adapter or IN supply to be between 3.3 V and 18 V. The battery voltage must be higher than 3.15 V or $V_{BATUVLO}$ to ensure proper operation.

9.4 Layout

9.4.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND, the capacitor from SYS to GND, and the BAT to GND capacitor should be placed as close as possible to the device.
- A solid ground plane should be used that is tied to the GND pin and thermal pad
- The pushbutton GND should be connected as close to the device as possible
- The high current charge paths into IN, SYS, and BAT must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces

9.4.2 Layout Example

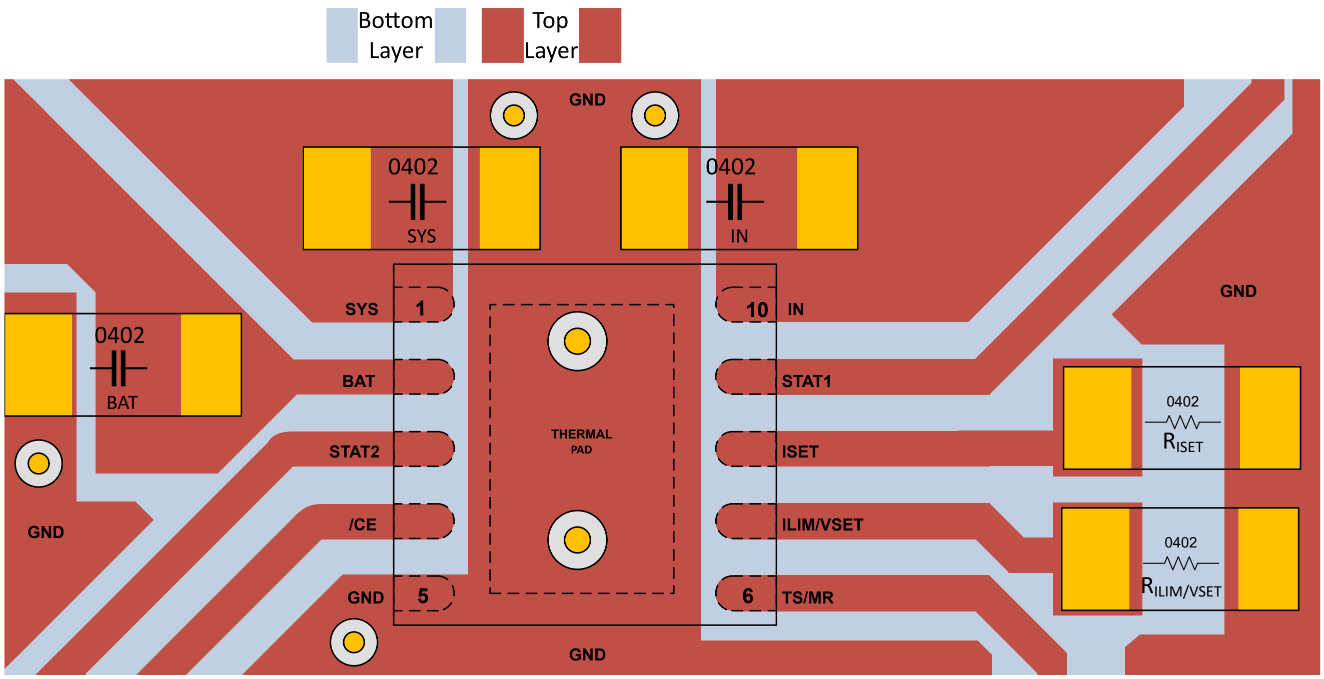


図 9-9. Board Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25185DLHR	Active	Production	WSON (DLH) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B185
BQ25185DLHR.A	Active	Production	WSON (DLH) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B185

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

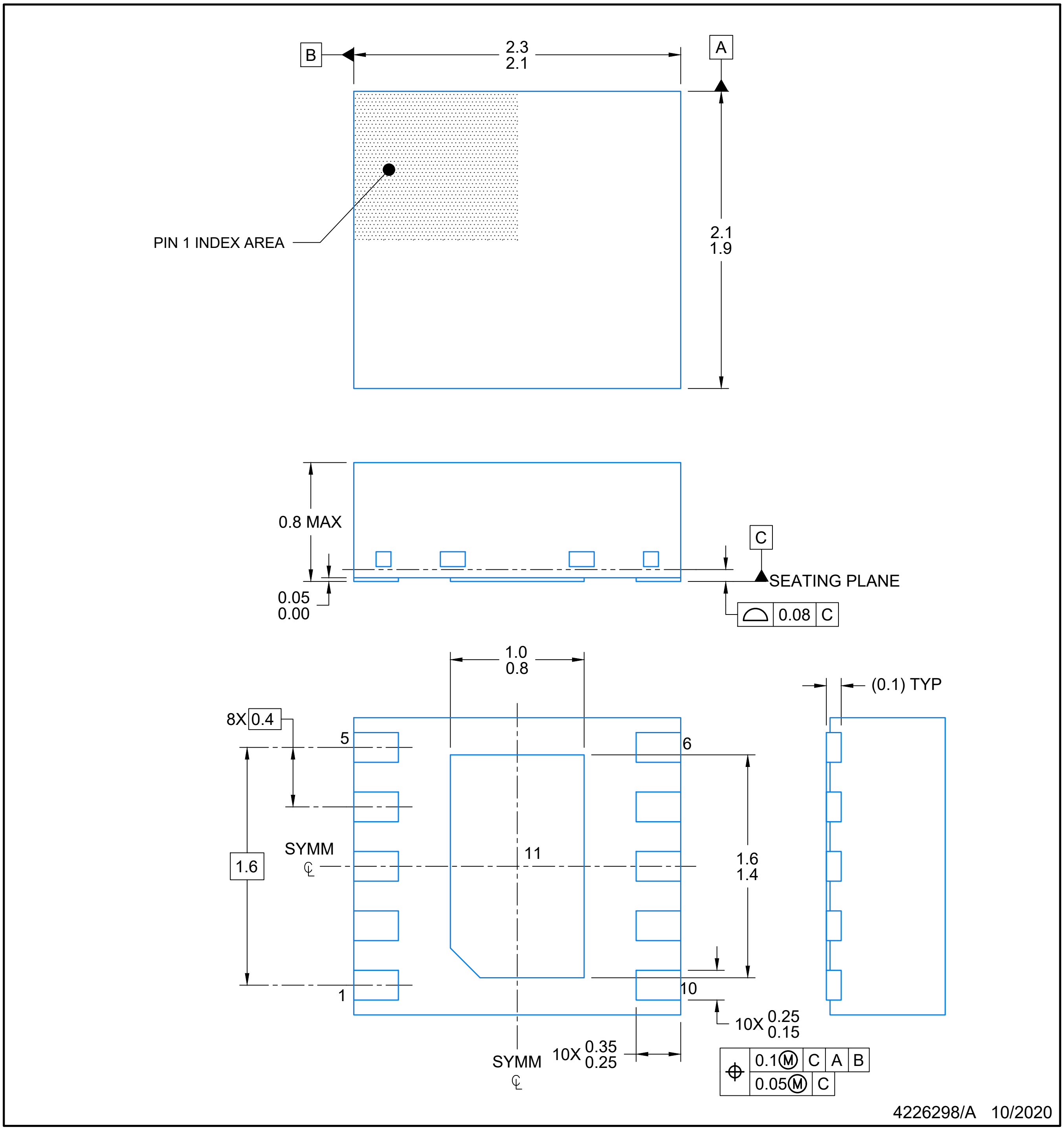
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

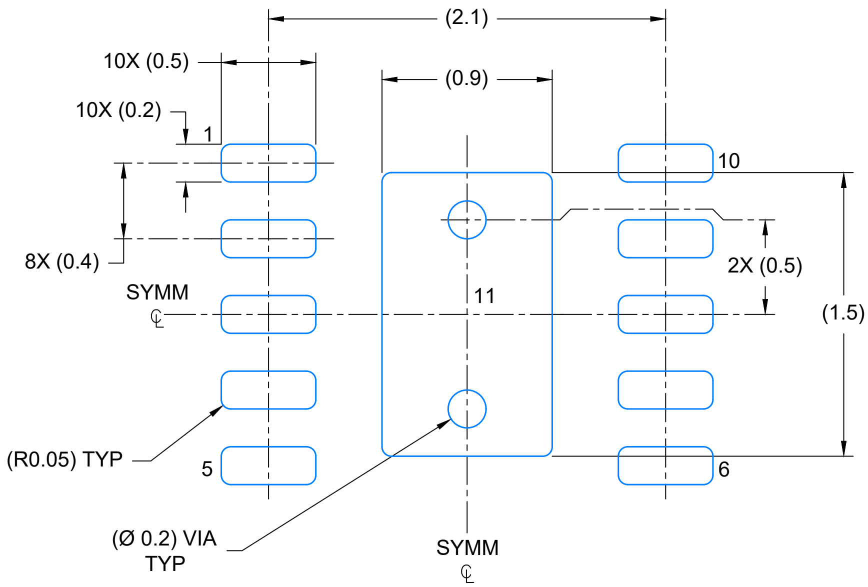
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

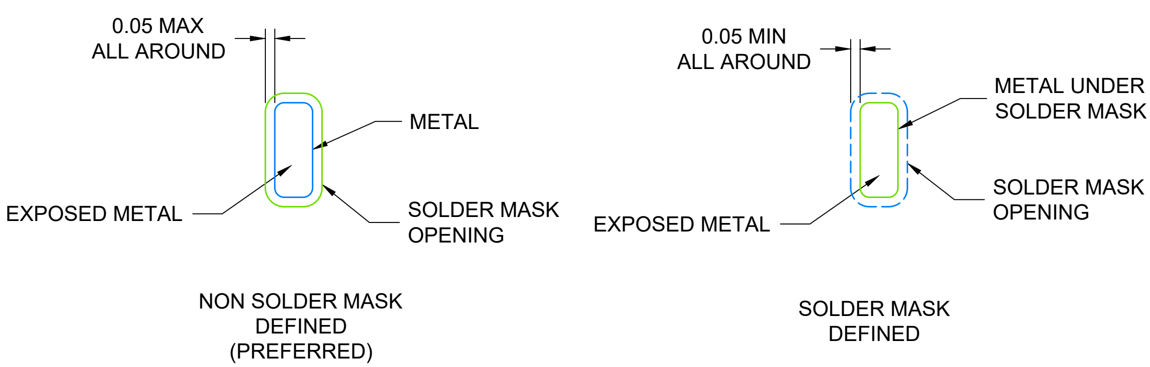


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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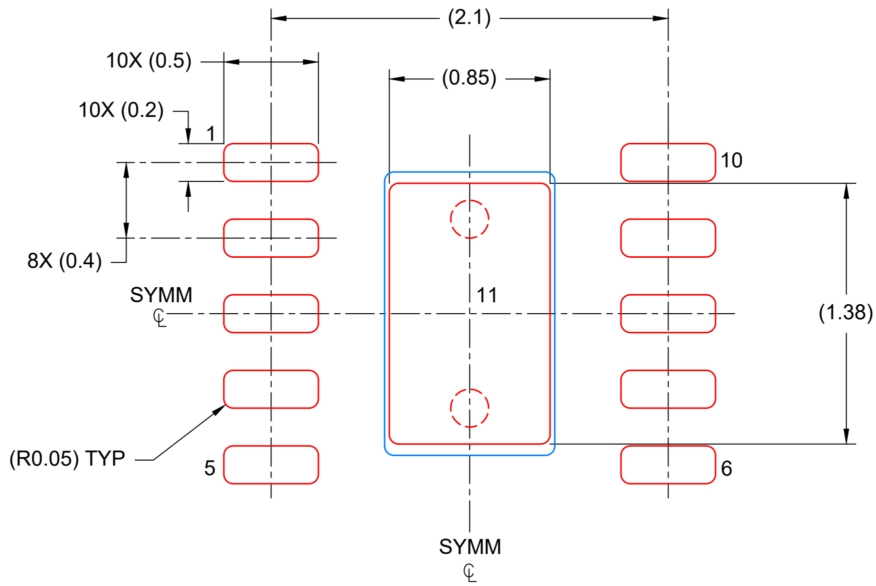
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.