BQ25672 デュアル入力セレクタ、ソーラー・パネル用 MPPT、ADC 内蔵、I²C 制御、1～4 セル、3A 降圧バッテリ充電器

1 特長

- 1～4 セル・バッテリ向け高電力密度、高集積降圧チャージャ
  - スイッチング MOSFET (BATFET) を内蔵
  - 入力および充電電流検出機能を内蔵
- 高効率
  - 750kHz または 1.5MHz のスイッチング周波数
  - 3A の充電電流 (分解能 10mA)
    - 96.5% の効率：20V 入力から 3A で 16V バッテリを充電する場合
- 幅広い入力電源をサポート
  - 太陽光発電パネルから充電するための自律サンプリング型開路電圧 (V_{OC}) 最大電力点トラッキング (MPPT)
  - 3.6V～24V の広い入力動作電圧範囲、30V の絶対最大定格
  - 最大 22V の入力電圧ダイナミック・パワー・マネージメント (VINDPM) と最大 3.3A の入力電流ダイナミック・パワー・マネージメント (IINDPM) に対応した最大電力トラッキング
  - USB BC1.2、HVDCP、非標準アダプタを検出
- 電源を選択するためのデュアル入力電源マルチプレクサ・コントローラ (オプション)
- Narrow VDC (NVDC) パワー・パス
- バッテリから USB ポートへの電源供給 (USB OTG)
  - 5V～12V の OTG 昇降圧出力電圧 (分解能 10mV)
  - 最大 2A の OTG 出力電流レギュレーション (分解能 40mA)
- 柔軟性の高い、自律および I²C モードにより最適なシステム性能を実現
- 電圧、電流、温度を監視するための 16 ビット ADC を内蔵
- 小さいバッテリ静止電流
  - 17μA (バッテリのみの動作)
  - 500nA (チャージャ・シャットダウン・モード)
- 高い精度
  - 2S バッテリで -0.25%～+0.65% の充電電圧レギュレーション
  - ±5% の充電電流レギュレーション
  - ±5% の入力電流レギュレーション
- 安全性
  - サーマル・レギュレーションおよびサーマル・シャットダウン
  - 入力 / バッテリの OVP と OCP
  - コンバータ MOSFET の OCP
  - 充電安全タイマ
- パッケージ
  - 29 ピン、4mm × 4mm QFN

2 アプリケーション

- ビデオ・ドアベル、スマート・ホーム・コントロール
- データ・コンセントレータ、ロボット芝刈り機、ロボット掃除機
- アセット・トラッキング、モバイル POS
- マルチパラメータ・メディカル・モニタ、心電図 (ECG)、超音波スマート・プローブ

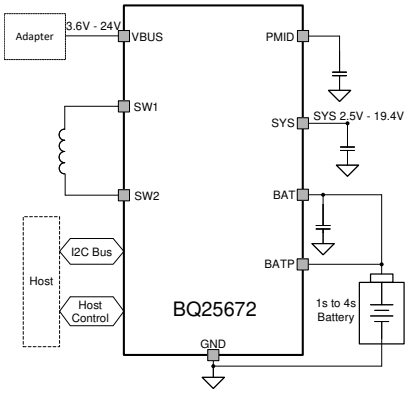
3 概要

BQ25672 は、1～4 セル・リチウムイオン・バッテリおよびリチウムポリマ・バッテリ用の完全統合型スイッチ・モード降圧チャージャです。BQ25672 は、OTG モードで動作している場合、VBUS 上に 5V～12V の昇降圧出力電圧を生成することもできます。つのスイッチング MOSFET 、入力および充電電流検出回路、バッテリ FET 、コンバータのすべてのループ補償が統合されています。システム電圧が設定可能な最小値を下回らないように、本デバイスは NVDC パワー・パス・マネージメント機能を使用して、システム電圧をレギュレートします。システム電圧が入力電源定格を上回った場合、入力電源に過剰な負荷が掛からないように、バッテリ補完モードがシステムを補助します。 は、内蔵の V_{OC} スケーリング MPPT アルゴリズムを使って、太陽光発電パネルからの電力を最大化することも行います。

デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
BQ25672	QFN (29)	4.0mm × 4.0mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2021) to Revision B (July 2023)	Page
• Corrected common drain to common source in ACDRVx pin function in セクション 6	4
• Clarified /QON pull up voltage in セクション 6	4
• Deleted SDRV connected to BAT when shipFET disabled as an option in セクション 6	4
• Updated: $V_{SYSMIN_REG_ACC}$	8
• Updated V_{OTG_ACC}	8
• Changed Functional Block Diagram	23
• Corrected default charge current to 1 A in セクション 8.3.2	24
• Clarified PFM peak inductor current in セクション 8.3.6.4	33
• Added charge current clamp during SYSMIN operation in セクション 8.3.9.2	38
• Clarified trickle to precharge regulation in セクション 8.3.9.2	38
• Added SDRV typical output voltage and current to セクション 8.3.12	45
• Updated I2C terminology in text and figures in セクション 8.3.14	48
• Corrected REG0x03 default charge current to 1A and max charge current to 3 A in セクション 8.5.1	53
• Changed REG0x09 bit5 from RESERVED to STOP_WD_CHG in セクション 8.5.1	53
• Added REG0x10 bits5-4 in セクション 8.5.1	53
• Clarified REG0x14 and REG0x33 regarding reporting IBAT discharge current in セクション 8.5.1	53
• Changed REG0x2E to no longer recommend 12-bit ADC setting in セクション 8.5.1	53
• Changed REG0x2E to Running average (not available for IBAT discharge) in セクション 8.5.1	53
• Corrected PN and DEV_REV naming in REG0x48 in セクション 8.5.1	53
• Added optional input snubber/TVS to application diagrams in セクション 9.2	126

Changes from Revision * (December 2020) to Revision A (May 2021)	Page
• 事前情報から量産データに変更	1

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5 概要 (続き)

この充電器は NVDC パワー・パス管理をサポートしています。この機能を使うと、システム電圧はバッテリ電圧よりわずかに高い値にレギュレートされますが、最小システム電圧を下回ることはありません。バッテリが完全に放電した場合や取り外された場合でも、システムは動作を続けられます。負荷電力が入力電源の定格を超過すると、バッテリが補完モードに移行し、入力電源の過負荷とシステムの故障を防止します。

入力電流オプティマイザ (ICO) を使うと、未知の入力源の最大電力点を検出できます。

I^2C ホスト制御充電モード以外に、この充電器は自律充電モードもサポートしています。電源投入後、充電はデフォルトのレジスタ設定を使って有効化されます。本デバイスは、ソフトウェアがまったく関与しなくても充電サイクルを完了できます。本デバイスは、各段階 (トリクル充電、プリチャージ、定電流 (CC) 充電、定電圧 (CV) 充電) でバッテリ電圧を検出しバッテリを充電します。定電圧フェーズにおいて、充電サイクルの終わりに、充電電流があらかじめ設定された制限値 (終了電流) を下回ると、充電器は自動的に停止します。十分に充電されたバッテリが再充電スレッショルドを下回ると、充電器は自動的にまた充電サイクルを開始します。

入力電源が存在しない場合、このデバイスは、VBUS 上に 5V ~ 12V の可変昇降圧出力電圧を 10mV 刻みで生成するためにバッテリを放電することで USB OTG (On-the-Go) 機能に対応します。

この充電器は、バッテリ温度の NTC サーミスタ監視、トリクル充電、プリチャージおよび高速充電タイマ、バッテリと入力の過電圧 / 過電流保護など、バッテリ充電とシステム動作のための各種安全機能を備えています。サーマル・レギュレーションにより、接合部温度がプログラム可能なスレッショルドを超えると充電電流が低減されます。本デバイスの STAT 出力は、充電ステータスとすべてのフォルト状態を報告します。フォルトが発生すると、$\overline{\text{INT}}$ ピンにより即座にホストへ通知されます。

このデバイスには、充電電流と入力 / バッテリ / システム (VAC、VBUS、BAT、SYS、TS) 電圧を監視するための、16 ビットのアナログ / デジタル・コンバータ (ADC) も搭載されています。

本デバイスは 29 ピンの 4mm × 4mm QFN パッケージで供給されます。

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6 Pin Configuration and Functions

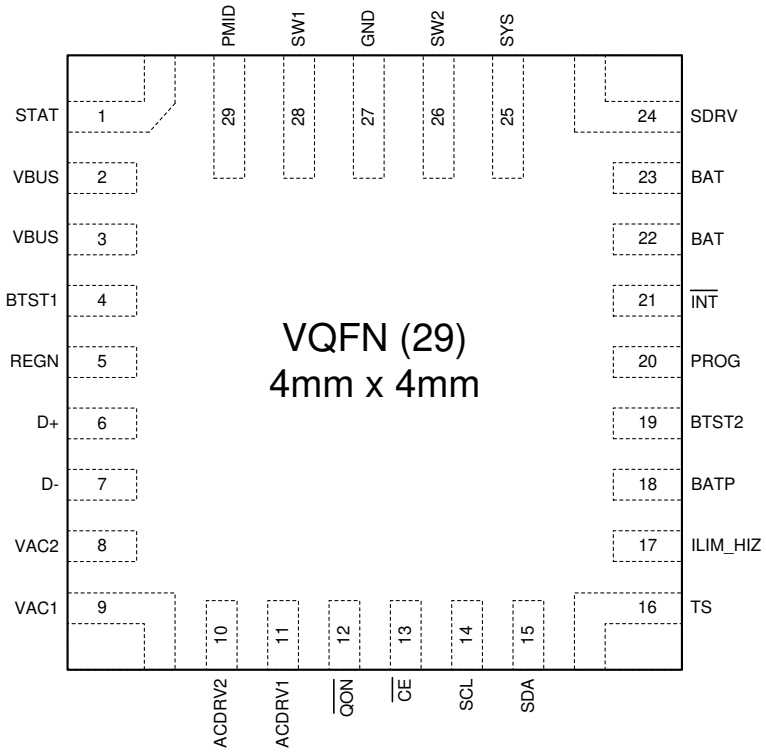

図 6-1. RQM Package 29-Pin VQFN Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
STAT	1	DO	**Open Drain Charge Status Output –** It indicates various charger operations. Connect to the pull up rail via a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT bit is set to 1.
VBUS	2-3	P	**Charger Input Voltage –** The power input terminal of the charger. An input current sensing circuit is connected between VBUS and PMID. The recommended capacitors at VBUS are 2 pieces of 10µF and one piece of 0.1µF ceramic capacitors. Place the 0.1µF ceramic capacitor as close as possible to the charger IC.
BTST1	4	P	**Input High Side Power MOSFET Gate Driver Power Supply –** Connect a 10V or higher rating, 47nF ceramic capacitor between SW1 and BTST1 as the bootstrap capacitor for driving high side switching MOSFET (Q1).
REGN	5	P	**The Charger Internal Linear Regulator Output –** It is supplied from either VBUS or BAT dependent on which voltage is higher. Connect a 10V, 4.7µF ceramic capacitor from REGN to power ground. The REGN LDO output is used for the internal MOSFETs gate driving voltage and the voltage bias for TS pin resistor divider.
D+	6	AIO	**Positive Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.
D-	7	AIO	**Negative Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.
VAC2	8	P	**VAC2 Input Detection –** When a voltage between 3.6V and 24V is applied on VAC2, it represents a valid input being plugged into port #2. Connect to VBUS if the ACFET2 and RBFET2 are not installed.
VAC1	9	P	**VAC1 Input Detection –** When a voltage between 3.6V and 24V is applied on VAC1, it represents a valid input being plugged into port #1. Connect to VBUS if the ACFET1 and RBFET1 are not installed.

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表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ACDRV2	10	P	**Input FETs Driver Pin 2 –** The charge pump output to drive the port #2 input N-channel MOSFET (ACFET2) and the reverse blocking N-channel MOSFET (RBFET2). The charger turns on the back-to-back MOSFETs by increasing the ACDRV2 voltage 5V above the common source connection of the ACFET2 and RBFET2 when the turn-on condition is met. Tie ACDRV2 to GND if no ACFET2 and RBFET2 installed.
ACDRV1	11	P	**Input FETs Driver Pin 1 –** The charge pump output to drive the port #1 input N-channel MOSFET (ACFET1) and the reverse blocking N-channel MOSFET (RBFET1). The charger turns on the back-to-back MOSFETs by increasing the ACDRV1 voltage 5V above the common source connection of the ACFET1 and RBFET1 when the turn-on condition is met. Tie ACDRV1 to GND if no ACFET1 and RBFET1 installed.
$\overline{QON}$	12	DI	**Ship FET Enable or System Power Reset Control Input –** When the device is in ship mode or in the shutdown mode, the SDRV turns off the external ship FET to minimize the battery leakage current. A logic low on this pin with t_{SM_EXIT} duration turns on ship FET to force the device to exit the ship mode. A logic low on this pin with t_{RST} duration resets system power by turning off the ship FET for t_{RST_SFET} (also setting the charger in HIZ mode when VBUS is high) and then turning on ship FET (also disabling the charger HIZ mode) to provide full system power reset. During t_{RST_SFET} when the ship FET is off, the charger applies a 30mA discharging current on SYS to discharge system voltage. The pin contains an internal pull-up through a R_{QON} resistor. The typical output voltage is 3.6 V-3.8 V with VBUS and VBAT > 5V.
$\overline{CE}$	13	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.
SCL	14	DI	**I^2C Interface Clock –** Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	15	DIO	**I^2C Interface Data –** Connect SDA to the logic rail through a 10 kΩ resistor.
TS	16	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10kΩ thermistor.
ILIM_HIZ	17	AI	**Input Current Limit Setting and HIZ Mode Control Pin –** Program ILIM_HIZ voltage by connecting a resistor divider from pull up rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: V_{ILIM_HIZ} = 1V + 800mΩ × IINDPM, in which IINDPM is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and the IINDPM register. When the pin voltage is below 0.75V, the buck converter enters non-switching mode, similar to HiZ mode using EN_HIZ bit, but with REGN on. When the pin voltage is above 1V, the converter resumes switching. Connect ILIM_HIZ to REGN to set the maximum input current limit.
BATP	18	P	**Positive Input for Battery Voltage Sensing –** Connect to the positive terminal of battery pack. Place 100Ω series resistance between this pin and the battery positive terminal.
BTST2	19	P	**Output High Side Power MOSFET Gate Driver Power Supply –** Connect a 10V or higher rating, 47nF ceramic capacitor between SW2 and BTST2 as the bootstrap capacitor for driving high side switching MOSFET (Q4).
PROG	20	AI	**Charger POR Default Settings Program –** At power up, the charger detects the resistance tied to PROG pin to determine the default switching frequency and the default battery charging profile. The surface mount resistor with ±1% or ±2% tolerance is recommended. Please refer to more details in the section of PROG Pin Configuration.
$\overline{INT}$	21	DO	**Open Drain Interrupt Output. –** Connect the $\overline{INT}$ pin to a logic rail via a 10kΩ resistor. The $\overline{INT}$ pin sends an active low, 256μs pulse to the host to report the charger device status and faults.
BAT	22-23	P	**The Battery Charging Power Connection –** Connect to the positive terminal of the battery pack. The internal charging current sensing circuit is connected between SYS and BAT. The recommended capacitors at BAT are 2 pieces of 10μF ceramic capacitors.
SDRV	24	P	**External N-channel Ship FET (SFET) Gate Driver Output –** The driver pin of the external ship FET. The ship FET is always turned on when the ship mode is disabled, and it keeps off when the charger is in ship mode or shutdown mode. Connect a 1nF, 50V rated, 0402 package, ceramic capacitor from SDRV to GND when the ship FET is not used.
SYS	25	P	**The Charger Output Voltage to System –** The internal N-channel high side MOSFET (Q4) is connected between SYS and SW2 with drain on SYS and source on SW2. The recommended capacitors at SYS are 5 pieces of 10μF and one piece of 0.1μF ceramic capacitors. Place the 0.1μF ceramic capacitor as close as possible to the charger IC.
SW2	26	P	**Boost Side Half Bridge Switching Node** Inductor connection to mid point of Q3 and Q4 switches.

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表 6-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	27	P	**Ground Return**
SW1	28	P	**Buck Side Half Bridge Switching Node** Inductor connection to mid point of Q1 and Q2 switches.
PMID	29	P	**Q1 MOSFET Drain Connection –** An internal N-channel high side MOSFET (Q1) is connected between PMID and SW1 with drain on PMID and source on SW1. The recommended capacitors at PMID are 3 pieces of 10µF and one piece of 0.1µF ceramic capacitors. Place the 0.1µF ceramic capacitor as close as possible to the charger IC.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VAC1, VAC2	-2	30	V
	VBUS (converter not switching)	-2	30	V
	PMID (converter not switching)	-0.3	30	V
	ACDRV1, ACDRV2, BTST1	-0.3	32	V
	SYS (converter not switching)	-0.3	23	V
	BATP, BAT	-0.3	20	V
	BTST2	-0.3	29	V
	SDRV	-0.3	26	V
	SW1	-2 (50ns)	30	V
	SW2	-2 (50ns)	23	V
	$\overline{QON}$, D+, D-, $\overline{CE}$, STAT, SCL, SDA, $\overline{INT}$, ILIM_HIZ, PROG, TS, REGN	-0.3	6	V
Output Sink Current	$\overline{INT}$, STAT		6	mA
Differential Voltage	BTST1-SW1, BTST2-SW2	-0.3	6	V
	PMID-VBUS	-0.3	6	V
	SYS-BAT	-0.3	16	V
	SDRV-BAT	-0.3	6	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.6		24	V
V_{BAT}	Battery voltage			18.8	V
I_{VBUS}	Input current			3.3	A
I_{SW}	Output current (SW)			5	A
I_{BAT}	Fast charging current			3	A
	RMS discharge current (continuously)			6	A
	Peak discharge current (upto 1 sec)			10	A
T_A	Ambient temperature	-40		85	°C

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7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature	-40		125	°C
C_{VBUS}	Effective VBUS capacitance		2		µF
C_{PMID}	Effective PMID capacitance		4		µF
C_{SYS}	Effective SYS capacitance		6		µF
C_{BAT}	Effective BAT capacitance		3		µF

7.4 Thermal Information

THERMAL METRIC(1)		BQ25672 RQM (QFN) 29-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
$I_{Q_BAT_ON}$	Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is disabled	VBAT = 8V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, not in ship mode or shut down mode, system is powered by battery. T_J < 85 °C		17	24	µA
$I_{Q_BAT_OFF}$	Quiescent battery current (BATP) for when the charger is in ship mode.	VBAT = 8V, No VBUS, I2C enabled, ADC disabled, in ship mode, T_J < 85 °C		11	16	µA
I_{SD_BAT}	Shutdown battery current (BATP) when charger is in shut down mode.	VBAT = 8V, No VBUS, I2C disabled, ADC disabled, in shut down mode, T_J < 85 °C		0.5	0.7	µA
$I_{Q_BAT_ON}$	Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is enabled	VBAT = 8V, No VBUS, I2C enabled, ADC enabled, not in ship mode or shut down mode, T_J < 85 °C		540		µA
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA disabled		3		mA
		VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA enabled		5		mA
I_{SD_VBUS}	Shutdown input current (VBUS) in HIZ	VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV disabled		386		µA
		VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV enabled		590		µA

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_OTG}	Quiescent battery current (BATP, BAT, SYS) in OTG	VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, OOA disabled		3		mA
		VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, OOA enabled		5		mA
VBUS / VBAT SUPPLY						
$V_{VAC_PRESENT}$	VAC present rising threshold to turn on the ACFET-RBFET	For both VAC1 and VAC2		3.4	3.5	V
	VAC present falling threshold to turn off the ACFET-RBFET	For both VAC1 and VAC2	3.1	3.2		V
V_{VAC_OVP}	VAC overvoltage rising threshold, when VAC_OVP[1:0]=00	For both VAC1 and VAC2	25.2	26	26.8	V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=00	For both VAC1 and VAC2	24.4	25.2	26.0	V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=01	For both VAC1 and VAC2	17.4	18.0	18.6	V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=01	For both VAC1 and VAC2	16.9	17.5	18.1	V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=10	For both VAC1 and VAC2	11.6	12	12.4	V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=10	For both VAC1 and VAC2	11.2	11.6	12.0	V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=11	For both VAC1 and VAC2	6.7	7	7.3	V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=11	For both VAC1 and VAC2	6.5	6.8	7.1	V
V_{VBUS_OP}	VBUS operating range		3.6		24	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising	3.25	3.4	3.55	V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling	3.05	3.2	3.35	V
$V_{VBUS_PRESENT}$	VBUS to start switching	VBUS rising	3.3	3.4	3.5	V
$V_{VBUS_PRESENTZ}$	VBUS to stop switching	VBUS falling	3.1	3.2	3.3	V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising	25.2	25.7	26.2	V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling	24.0	24.4	24.8	V
I_{BUS_OCP}	IBUS over-current rising threshold		7.0	8.0	9.0	A
I_{BUS_OCPZ}	IBUS over-current falling threshold		6.5	7.5	8.5	A
V_{BAT_UVLOZ}	BAT voltage for active I2C, no VBUS, no VAC	VBAT rising, with the ship FET (SFET) installed	3.25	3.40	3.55	V
		VBAT rising, without the ship FET (SFET) installed	2.50	2.60	2.71	V

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_UVLO}	BAT voltage to turn off I2C, no VBUS, no VAC	VBAT rising, with the ship FET (SFET) installed	3.05	3.20	3.31	V
		VBAT falling, without the ship FET (SFET) installed	2.30	2.40	2.50	V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising	2.7	2.8	2.9	V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling	2.4	2.5	2.6	V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.3	3.4	3.5	V
$V_{POORSRC}$	Bad adapter detection threshold hysteresis	VBUS rising above $V_{POORSRC}$	150	200	250	mV
$I_{POORSRC}$	Bad adapter detection current source		7	12	20	mA
R_{VBUS_PD}	VBUS pull down resistance			6		kΩ
R_{VAC_PD}	VAC pull down resistance	For both VAC1 and VAC2		60		Ω
V_{VINDPM_MPPT}	VINDPM as set by the MPPT algorithm	VOC_PCT = 000 (0.5625), VOC = 18.0V		10.125		V
		VOC_PCT = 001 (0.625), VOC = 18.0V		11.25		V
		VOC_PCT = 010 (0.6875), VOC = 18.0V		12.375		V
		VOC_PCT = 011 (0.75), VOC = 18.0V		13.5		V
		VOC_PCT = 100 (0.8125), VOC = 18.0V		14.625		V
		VOC_PCT = 101 (0.875), VOC = 18.0V		15.75		V
		VOC_PCT = 110 (0.9375), VOC = 18.0V		16.875		V
		VOC_PCT = 111 (1.0), VOC = 18.0V		18.0		V
POWER-PATH MANAGEMENT						
$V_{SYSMAX_REG_RNG}$	System voltage regulation range, measured on SYS		3.2		19	V
$V_{SYSMAX_REG_ACC}$	System voltage regulation accuracy (when V_{BAT}>V_{SYSMIN}, charging disabled, PFM disabled)	V_{BAT} = 16.8V (4s default)	16.82	17.00	17.25	V
		V_{BAT} = 12.6V (3s default)	12.62	12.80	13.04	V
		V_{BAT} = 8.4V (2s default)	8.44	8.60	8.77	V
		V_{BAT} = 4.2V (1s default)	4.268	4.40	4.550	V
$V_{SYSMIN_REG_RNG}$	V_{SYSMIN} regulation range, measured on SYS		2.5		16	V
$V_{SYSMIN_REG_STEP}$	V_{SYSMIN} regulation step size			250		mV
$V_{SYSMIN_REG_ACC}$	System voltage regulation accuracy (when V_{BAT}<V_{SYSMIN})	4s battery	11.9	12.2	12.75	V
		3s battery	9.0	9.2	9.55	V
		2s battery	7.12	7.2	7.52	V
		1s battery	3.5	3.7	4.1	V
V_{SYS_OVP}	VSYS overvoltage rising threshold	As a percentage of the system regulation voltage, to turnoff the converter.	105.5	110.0	112.3	%
	VSYS overvoltage falling threshold	As a percentage of the system regulation voltage, to re-enable the converter.	95.5	100	102	%
V_{SYS_SHORT}	VSYS short voltage falling threshold		2.1	2.2	2.3	V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3		18.8	V
V_{REG_STEP}	Typical charge voltage step			10		mV

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG_ACC}	Charge voltage accuracy, T_J = –40°C - 85°C	V_{REG} = 16.8V	-0.65		0.55	%
		V_{REG} = 12.6V	-0.85		0.65	%
		V_{REG} = 8.4V	-0.25		0.65	%
		V_{REG} = 4.2V	-0.45		0.95	%
I_{CHG_RANGE}	Typical charge current regulation range		0.05		3	A
I_{CHG_STEP}	Typical charge current regulation step			10		mA
I_{CHG_ACC}	Typical buck mode PWM charge current accuracy, VBUS > VBAT, T_J = –40°C - 85°C	ICHG = 2A; VBAT=8V	-6.5		3.5	%
		ICHG = 1A; VBAT=8V	-5		5	%
		ICHG = 0.5A; VBAT=8V	-7.5		7.5	%
I_{PRECHG_RANGE}	Typical pre-charge current range		40		2000	mA
I_{PRECHG_STEP}	Typical pre-charge current step			40		mA
I_{PRECHG_ACC}	Typical LDO mode charge current accuracy when V_{BATP} below V_{BAT_LOWV}, VBUS > VBAT, T_J = –40°C - 85°C	IPRECHG = 1000mA, VBAT = 6.5V	-4.5		3.5	%
		IPRECHG = 480mA, VBAT = 6.5V	-8		8	%
		IPRECHG = 200mA, VBAT = 6.5V	-20		20	%
		IPRECHG = 120mA, VBAT = 6.5V	-30		30	%
I_{TERM_RANGE}	Typical termination current range		40		1000	mA
I_{TERM_STEP}	Typical termination current step			40		mA
I_{TERM_ACC}	Termination current accuracy, T_J = –40°C - 85°C	ITERM = 120mA, ICHG < 1000mA	-20		20	%
		ITERM = 480mA, ICHG > 1000mA	-14		14	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling		2.06		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}		100		mA
$V_{BAT_LOWV_RISE}$	Battery voltage rising threshold to start fast-charge, as percentage of V_{REG}	VBAT_LOWV_1:0=00	13	15	17	%
		VBAT_LOWV_1:0=01	61.5	63.0	64.5	%
		VBAT_LOWV_1:0=10	67.0	68.0	69.0	%
		VBAT_LOWV_1:0=11	71.0	72.5	74.0	%
$V_{BAT_LOWV_HYS}$	Battery voltage threshold hysteresis to stop fast-charge on falling edge	VBAT falling, as percentage of VREG, VBAT_LOWV_1:0=11		1.4		%
V_{RECHG}	Battery recharge threshold	VBAT falling, VRECHG=0011, VREG=8.4V		200		mV
		VBAT falling, VRECHG=0111, VREG=16.8V		400		mV
I_{BAT_LOAD}	Battery discharge load current			30		mA
I_{SYS_LOAD}	System discharge load current			30		mA
R_{BATP}	BATP Input Resistance			2.5		MΩ
BATFET						
R_{BATFET}	MOSFET on resistance from SYS to BAT			11		mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage threshold	VBAT rising, as percentage of VREG	103	104	105	%
		VBAT falling, as percentage of VREG	101	102	103	%

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_SHORT}	Battery short voltage	VBAT falling, to clamp the charging current as trickle charging current.		2.06		V
		VBAT rising, to release the trickle charging current clamp		2.25		V
I_{BAT_OCP}	Battery discharging over-current rising threshold		9.3			A
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.6		22	V
V_{INDPM_STEP}	Typical input voltage regulation step			100		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=18.6V	-2		2	%
		VINDPM=10.6V	-3		3	%
		VINDPM=4.3V	-5		5	%
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.3	A
I_{INDPM_STEP}	Typical input current regulation step			10		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, VBUS=9V, T_J > -20°C	415	460	500	mA
		IINDPM = 1000mA, VBUS=9V, T_J > -20°C	880	940	1000	mA
		IINDPM = 2000mA, VBUS=9V, T_J > -20°C	1800	1880	1960	mA
		IINDPM = 3000mA, VBUS=9V, T_J > -20°C	2720	2820	2920	mA
$V_{ILIM_REG_RNG}$	Voltage range for input current regultion at ILIM_HIZ pin		1		4	V
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current	V_{ILIM_HIZ} = 4V	-1.5		1.5	µA
D+ / D- DETECTION						
$V_{D+_600MVSRC}$	D+ voltage source (600 mV)		500	600	700	mV
$I_{D+_10UASRC}$	D+ current source (10 µA)	V_{D+} = 200 mV,	7	10	14	µA
$I_{D+_100UASNK}$	D+ current sink (100 µA)	V_{D+} = 500 mV,	50	90	150	µA
V_{D+_0P325}	D+ comparator threshold for Secondary Detection	D+ pin rising	250		400	mV
V_{D+_0P8}	D+ comparator threshold for Data Contact Detection	D+ pin rising	775	850	925	mV
I_{D+_LKG}	Leakage current into D+	HIZ mode	-1		1	µA
$V_{D-_600MVSRC}$	D- voltage source (600 mV)		500	600	700	mV
$I_{D-_100UASNK}$	D- current sink (100 µA)	V_{D-} = 500 mV,	50	90	150	µA
V_{D-_0P325}	D- comparator threshold for Primary Detection	D- pin Rising	250		400	mV
I_{D-_LKG}	Leakage current into D-	HIZ mode	-1		1	µA
R_{D-_19K}	D- resistor to ground (19 kΩ)	V_{D-} = 500mV	14.25		24.8	kΩ
V_{D+_2p8}	D+ comparator threshold for non-standard adapter	(combined $V_{D+_2p8_hi}$ and $V_{D+_2p8_lo}$)	2.55		2.85	V
V_{D-_2p8}	D- comparator threshold for non-standard adapter	(combined VD-_2p8_hi and VD-_2p8_lo)	2.55		2.85	V
V_{D+_2p0}	D+ comparator threshold for non-standard adapter	(combined $V_{D+_2p0_hi}$ and $V_{D+_2p0_lo}$)	1.85		2.15	V

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{D-_2p0}	D- comparator threshold for non-standard adapter	(combined $V_{D-_2p0_hi}$ and $V_{D-_2p0_lo}$)	1.85		2.15	V
V_{D+_1p2}	D+ comparator threshold for non-standard adapter	(combined $V_{D+_1p2_hi}$ and $V_{D+_1p2_lo}$)	1.05		1.35	V
V_{D-_1p2}	D- comparator threshold for non-standard adapter	(combined $V_{D-_1p2_hi}$ and $V_{D-_1p2_lo}$)	1.05		1.35	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 120°C		120		°C
		TREG = 100°C		100		°C
		TREG = 80°C		80		°C
		TREG = 60°C		60		°C
T_{SHUT}	Thermal shutdown rising threshold	Temperature increasing (TSHUT[1:0]=00)		150		°C
		Temperature increasing (TSHUT[1:0]=01)		130		°C
		Temperature increasing (TSHUT[1:0]=10)		120		°C
		Temperature increasing (TSHUT[1:0]=11)		85		°C
T_{SHUT_HYS}	Thermal shutdown falling hysteresis	Temperature decreasing by T_{SHUT_HYS}		30		°C
JEITA THERMISTOR COMPARATOR (CHARGE MODE)						
V_{T1_RISE}	T1 comparator rising threshold. Charge is suspended above this voltage.	As Percentage to REGN (0°C w/ 103AT)	72.4	73.3	74.2	%
V_{T1_FALL}	T1 comparator falling threshold. Charge is re-enabled below this voltage.	As Percentage to REGN (3°C w/ 103AT)	71.5	72	72.5	%
V_{T2_RISE}	T2 comparator rising threshold.	As Percentage of REGN, JEITA_T2=5°C w/ 103AT	70.6	71.1	71.6	%
		As Percentage of REGN, JEITA_T2=10°C w/ 103AT	67.9	68.4	68.9	%
		As Percentage of REGN, JEITA_T2=15°C w/ 103AT	65.0	65.5	66.0	%
		As Percentage of REGN, JEITA_T2=20°C w/ 103AT	61.9	62.4	62.9	%
V_{T2_FALL}	T2 comparator falling threshold.	As Percentage of REGN, JEITA_T2=5°C w/ 103AT	69.3	69.8	70.3	%
		As Percentage of REGN, JEITA_T2=10°C w/ 103AT	66.6	67.1	67.6	%
		As Percentage of REGN, JEITA_T2=15°C w/ 103AT	63.7	64.2	64.7	%
		As Percentage of REGN, JEITA_T2=20°C w/ 103AT	60.6	61.1	61.6	%
V_{T3_RISE}	T3 comparator rising threshold.	As Percentage of REGN, JEITA_T3=40°C w/ 103AT	49.2	49.7	50.2	%
		As Percentage of REGN, JEITA_T3=45°C w/ 103AT	45.6	46.1	46.6	%
		As Percentage of REGN, JEITA_T3=50°C w/ 103AT	42.0	42.5	43.0	%
		As Percentage of REGN, JEITA_T3=55°C w/ 103AT	38.5	39	39.5	%

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T3_FALL}	T3 comparator falling threshold.	As Percentage of REGN, JEITA_T3=40°C w/ 103AT	47.9	48.4	48.9	%
		As Percentage of REGN, JEITA_T3=45°C w/ 103AT	44.3	44.8	45.3	%
		As Percentage of REGN, JEITA_T3=50°C w/ 103AT	40.7	41.2	41.7	%
		As Percentage of REGN, JEITA_T3=55°C w/ 103AT	37.2	37.7	38.2	%
V_{T5_FALL}	T5 comparator falling threshold. Charge is suspended below this voltage.	As Percentage of REGN (60°C w/ 103AT)	33.7	34.2	34.7	%
V_{T5_RISE}	T5 comparator rising threshold. Charge is re-enabled above this voltage.	As Percentage of REGN (58°C w/ 103AT)	35	35.5	36	%
COLD / HOT THERMISTOR COMPARATOR (OTG MODE)						
V_{BCOLD_RISE}	TCOLD comparator rising threshold.	As Percentage of REGN (–20°C w/ 103AT)	79.5	80.0	80.5	%
		As Percentage of REGN (–10°C w/ 103AT)	76.6	77.1	77.6	%
V_{BCOLD_FALL}	TCOLD comparator falling threshold.	As Percentage of REGN (–20°C w/ 103AT)	78.2	78.7	79.2	%
		As Percentage of REGN (–10°C w/ 103AT)	75.3	75.8	76.3	%
V_{BHOT_FALL}	THOT comparator falling threshold.	As Percentage of REGN, (55°C w/ 103AT)	37.2	37.7	38.2	%
		As Percentage of REGN, (60°C w/ 103AT)	33.9	34.4	34.9	%
		As Percentage of REGN, (65°C w/ 103AT)	30.8	31.3	31.8	%
V_{BHOT_RISE}	THOT comparator rising threshold.	As Percentage of REGN, (55°C w/ 103AT)	38.8	39.3	39.8	%
		As Percentage of REGN, (60°C w/ 103AT)	35.2	35.7	36.2	%
		As Percentage of REGN, (65°C w/ 103AT)	32.0	32.5	33.0	%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency		1.5		MHz
				750		kHz
SENSE RESISTANCE AND MOSFET RDSON						
R_{SNS}	VBUS to PMID input sensing resistance	T_j = -40°C-85°C (typical value is under 25°C)		8		mΩ
R_{Q1_ON}	Buck high-side switching MOSFET turnon resistance between PMID and SW1	T_j = -40°C-85°C (typical value is under 25°C)		24		mΩ
R_{Q2_ON}	Buck low-side switching MOSFET turnon resistance between SW1 and PGND	T_j = -40°C-85°C (typical value is under 25°C)		35		mΩ
R_{Q3_ON}	Boost low-side switching MOSFET turnon resistance between SW2 and PGND	T_j = -40°C-85°C (typical value is under 25°C)		28		mΩ

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{Q4_ON}	Boost high-side switching MOSFET turnon resistance between SW2 and SYS	T_j = -40°C-85°C (typical value is under 25°C)		17		mΩ
OTG MODE CONVERTER						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		5		12	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			10		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 20V	-3.5		3	%
		IVBUS = 0A, VOTG = 12V	-3.5		3	%
		IVBUS = 0A, VOTG = 5V	-3.5		3	%
I_{OTG_RANGE}	Typical OTG mode current regulation range		0.12		3.32	A
I_{OTG_STEP}	Typical OTG mode current regulation step			40		mA
I_{OTG_ACC}	OTG mode current regulation accuracy	VBUS = 9V, IOTG = 3.0A	-2.2		2.2	%
		VBUS = 9V, IOTG = 1.52A	-5		3	%
		VBUS = 9V, IOTG = 0.52A	-15		8	%
V_{OTG_UVP}	OTG mode under voltage falling threshold		2.1	2.2	2.3	V
V_{OTG_OVP}	OTG mode overvoltage rising threshold	As percentage of VOTG regulation, OTG mode OOA disabled.	104	113	120	%
	OTG mode overvoltage falling threshold	As percentage of VOTG regulation	90	98	104	%
I_{OTG_BAT}	Battery current regulation in OTG mode	IBAT_REG_1:0 = 00, VBAT=8V, VOTG=9V	2.8	3	3.2	A
		IBAT_REG_1:0 = 01, VBAT=8V, VOTG=9V	3.8	4	4.2	A
		IBAT_REG_1:0 = 10, VBAT=8V, VOTG=9V	4.8	5	5.3	A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.6	4.8	5	V
		V_{VBUS} = 15V, I_{REGN} = 20mA	4.8	5	5.2	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5V, V_{REGN} = 4.5V	30			mA
I2C INTERFACE (SCL, SDA)						
V_{IH_SDA}	Input high threshold level, SDA	Pull up rail 1.8V	1.3			V
V_{IL_SDA}	Input low threshold level	Pull up rail 1.8V			0.4	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS_SDA}	High-level leakage current	Pull up rail 1.8V			1	µA
V_{IH_SCL}	Input high threshold level, SDA	Pull up rail 1.8V	1.3			V
V_{IL_SCL}	Input low threshold level	Pull up rail 1.8V			0.4	V
I_{BIAS_SCL}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC I PIN ($\overline{CE}$, ILIM_HIZ, $\overline{QON}$)						
V_{IH_CE}	Input high threshold level, $\overline{CE}$		1.3			V
V_{IL_CE}	Input low threshold level, $\overline{CE}$				0.4	V
$I_{IN_BIAS_CE}$	High-level leakage current, $\overline{CE}$	Pull up rail 1.8V			1	µA
V_{IH_QON}	Input high threshold level, $\overline{QON}$		1.3			V
V_{IL_QON}	Input low threshold level, $\overline{QON}$				0.4	V

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7.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{QON}	Internal $\overline{QON}$ pull up	$\overline{QON}$ is pulled up internally		3.2		V
R_{QON}	Internal $\overline{QON}$ pull up resistance			200		kΩ
$V_{IH_ILIM_HIZ}$	Input high threshold level, ILIM_HIZ		1			V
$V_{IL_ILIM_HIZ}$	Input low threshold level, ILIM_HIZ				0.75	V
LOGIC O PIN ($\overline{INT}$, STAT)						
V_{OL_INT}	Output low threshold level, $\overline{INT}$	Sink current = 5mA			0.4	V
$I_{OUT_BIAS_INT}$	High-level leakage current, $\overline{INT}$	Pull up rail 1.8V			1	µA
V_{OL_STAT}	Output low threshold level, STAT	Sink current = 5mA			0.4	V
$I_{OUT_BIAS_STAT}$	High-level leakage current, STAT	Pull up rail 1.8V			1	µA
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion time, each measurement	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		ms
		ADC_SAMPLE[1:0] = 10		6		ms
		ADC_SAMPLE[1:0] = 11 (Not recommended)		3		ms
ADC_{RES}	Effective resolution	ADC_SAMPLE[1:0] = 00	14	15		bits
		ADC_SAMPLE[1:0] = 01	13	14		bits
		ADC_SAMPLE[1:0] = 10	12	13		bits
		ADC_SAMPLE[1:0] = 11 (Not recommended)	10	11		bits
ADC MEASUREMENT RANGE AND LSB						
IBUS_ADC	ADC VBUS current reading (forward and OTG)	Range	0		5	A
		LSB		1		mA
VBUS_ADC	ADC VBUS voltage reading	Range	0		30	V
		LSB		1		mV
VAC_ADC	ADC VAC voltage reading	Range	0		30	V
		LSB		1		mV
VBAT_ADC	ADC BAT voltage reading	Range	0		20	V
		LSB		1		mV
VSYS_ADC	ADC SYS voltage reading	Range	0		24	V
		LSB		1		mV
IBAT_ADC	ADC BAT current reading	Range	0		8	A
		LSB		1		mA
TS_ADC	ADC TS voltage reading range	Range	0		99.9	%
		LSB		0.098		%
TDIE_ADC	ADC die temperature reading range	Range	-40		150	°C
		LSB		0.5		°C

7.6 Timing Requirements

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
BATTERY CHARGER					

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7.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{TOP_OFF}	Top-off timer accuracy	TOPOFF_TMR[1:0] = 01	12	15	18	min
		TOPOFF_TMR[1:0] = 10	24	30	36	min
		TOPOFF_TMR[1:0] = 11	36	45	54	min
t_{SAFETY_TRKCHG}	Charge safety timer in trickle charge		0.9	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer in pre-charge	PRECHG_TMR = 0	1.8	2	2.2	hr
t_{SAFETY}	Charge safety timer accuracy	CHG_TMR[1:0] = 00	4.5	5	5.5	hr
		CHG_TMR[1:0] = 01	7.2	8	8.8	hr
		CHG_TMR[1:0] = 10	10.8	12	13.2	hr
		CHG_TMR[1:0] = 11	21.6	24	26.4	hr
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1000	kHZ
WATCHDOG TIMER						
t_{LP_WDT}	Watchdog reset time	EN_HIZ = 1, WATCHDOG = 160s	100	160		s
t_{WDT}	Watchdog reset time	EN_HIZ = 0, WATCHDOG = 160s	136	160		s

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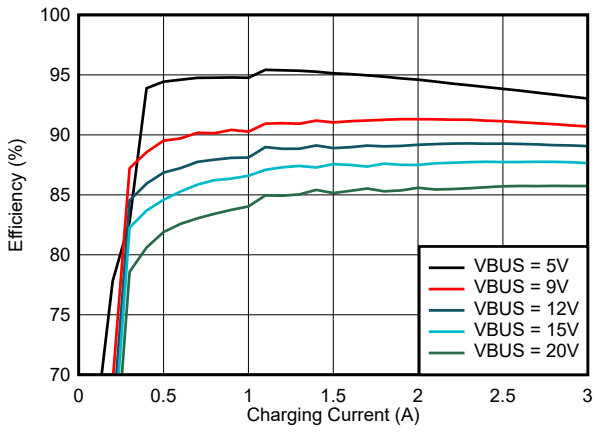
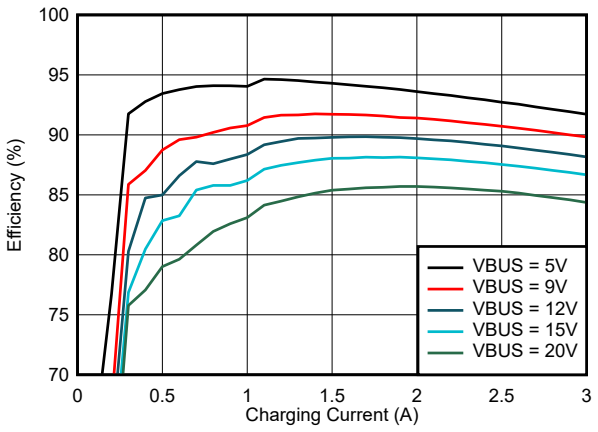
7.7 Typical Characteristics

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120) and L2 = 2.2µH (WE-LHMI-74437346022)



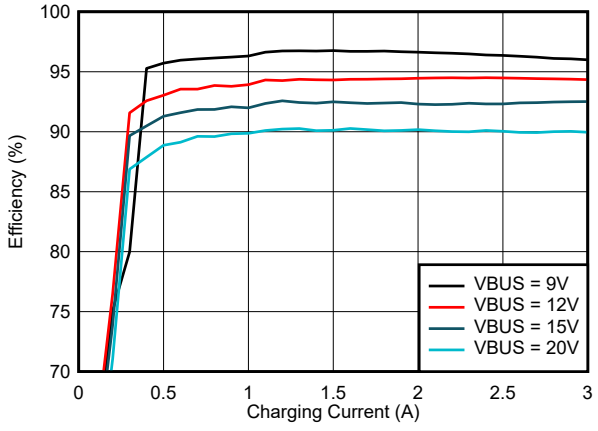
VBAT = 4V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-1. 1s Battery Charge Efficiency, 750 kHz



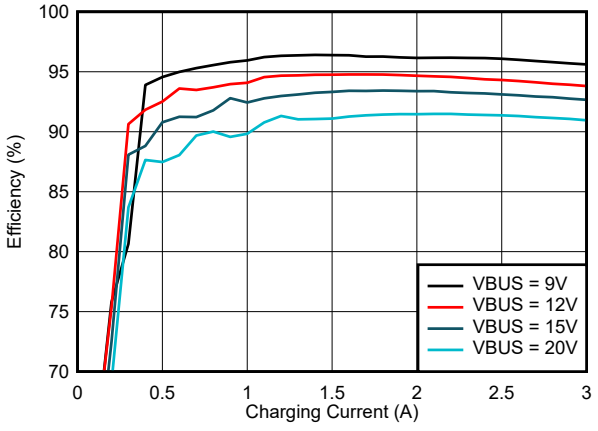
VBAT = 4V, Fsw = 1.5 MHz with L1 = 1.0 µH, PFM disabled

図 7-2. 1s Battery Charge Efficiency, 1.5 MHz



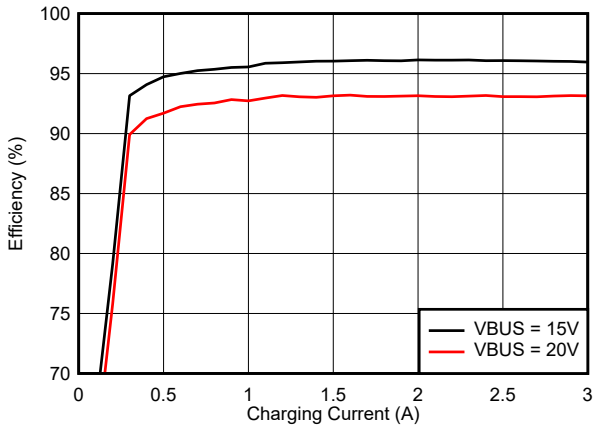
VBAT = 8V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-3. 2s Battery Charge Efficiency, 750 kHz



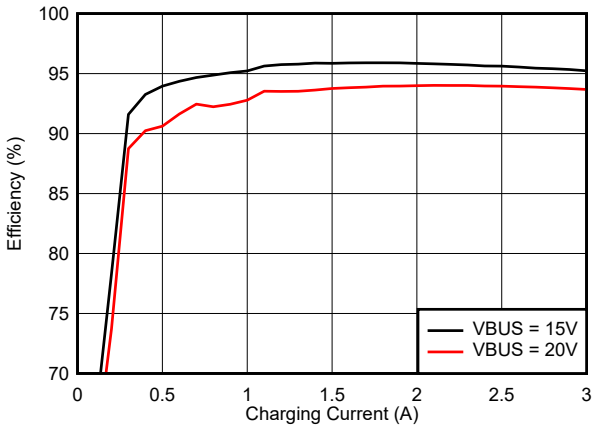
VBAT = 8V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-4. 2s Battery Charge Efficiency, 1.5 MHz



VBAT = 12V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-5. 3s Battery Charge Efficiency, 750 kHz



VBAT = 12V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-6. 3s Battery Charge Efficiency, 1.5 MHz

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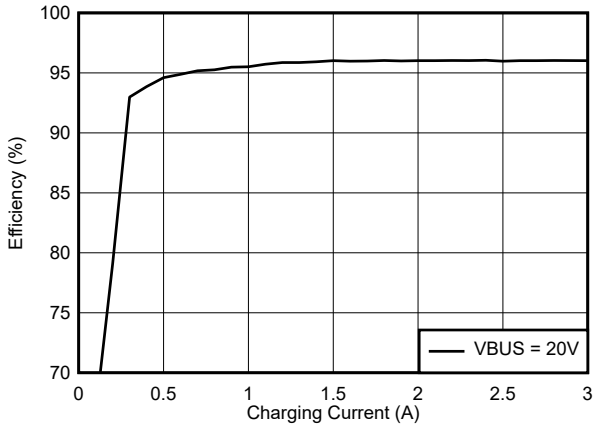
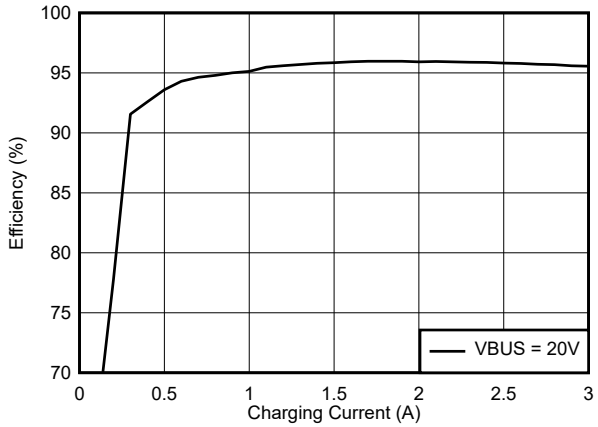
7.7 Typical Characteristics (continued)

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120) and L2 = 2.2µH (WE-LHMI-74437346022)



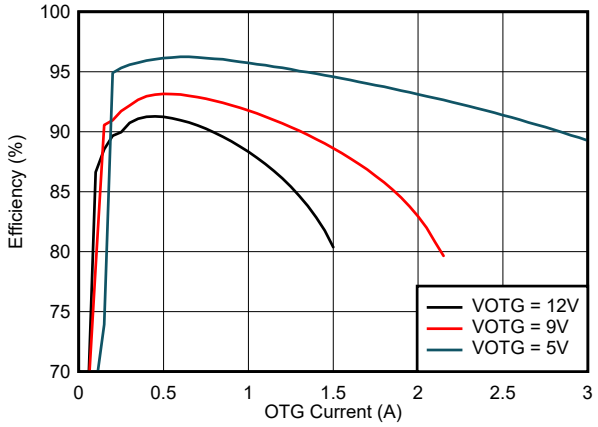
VBAT = 16V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-7. 4s Battery Charge Efficiency, 750 kHz



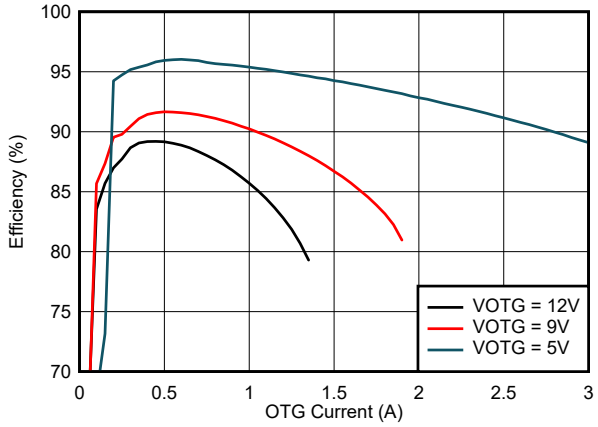
VBAT = 16V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-8. 4s Battery Charge Efficiency, 1.5 MHz



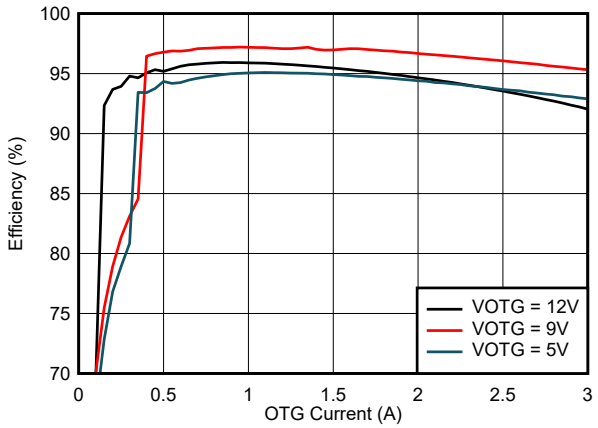
VBAT = 4.2V, Fsw = 750 kHz with L2 = 2.2 µH, PFM disabled

図 7-9. 1s Battery OTG Efficiency, 750 kHz



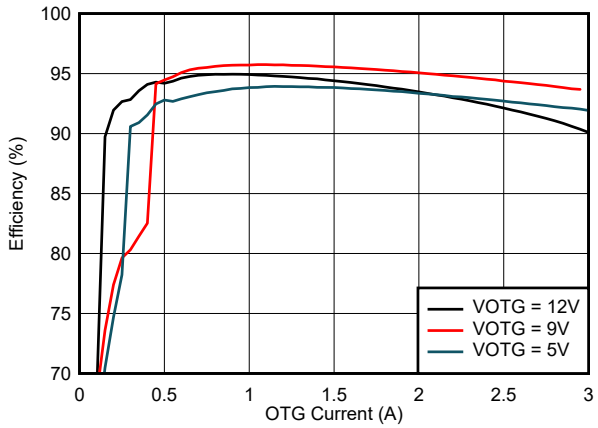
VBAT = 4.2V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-10. 1s Battery OTG Efficiency, 1.5 MHz



VBAT = 8.4V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-11. 2s Battery OTG Efficiency, 750 kHz



VBAT = 8.4V, Fsw = 1.5MHz with L1 = 1µH, PFM disabled

図 7-12. 2s Battery OTG Efficiency, 1.5 MHz

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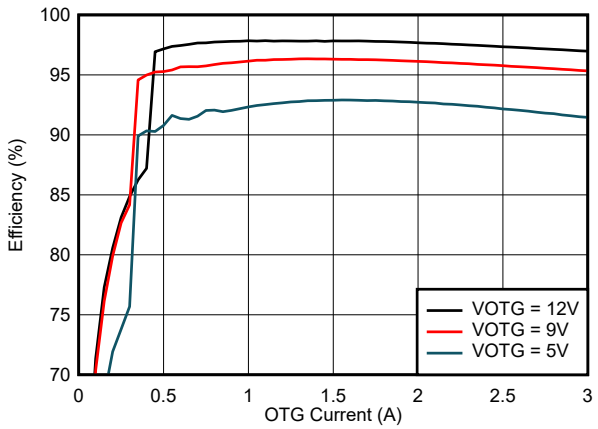
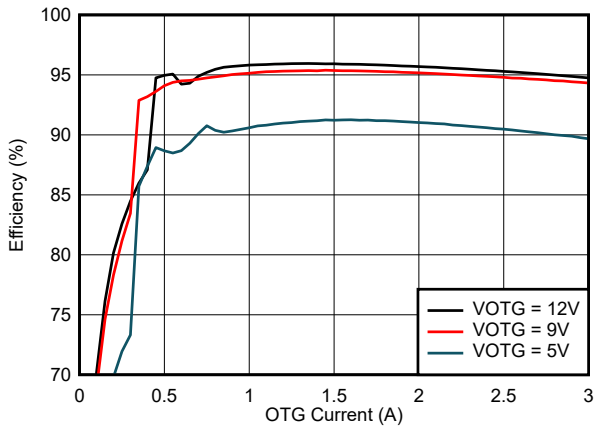
7.7 Typical Characteristics (continued)

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120) and L2 = 2.2µH (WE-LHMI-74437346022)



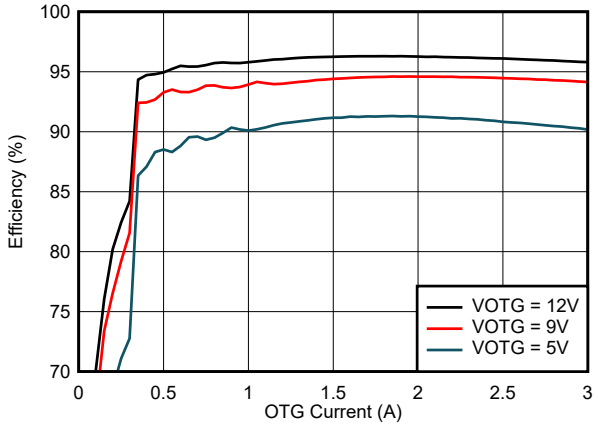
VBAT = 12.6V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-13. 3s Battery OTG Efficiency, 750 kHz



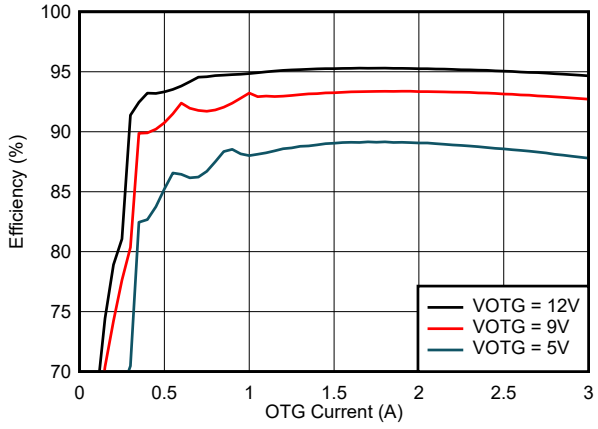
VBAT = 12.6V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-14. 3s Battery OTG Efficiency, 1.5 MHz



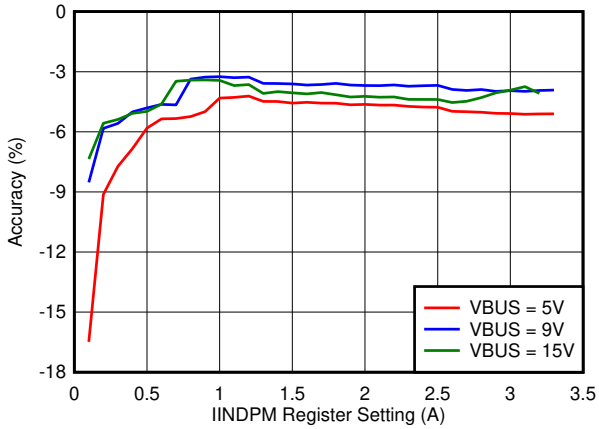
VBAT = 16.8V, Fsw = 750 kHz with L2 = 2.2µH, PFM disabled

図 7-15. 4s Battery OTG Efficiency, 750 kHz



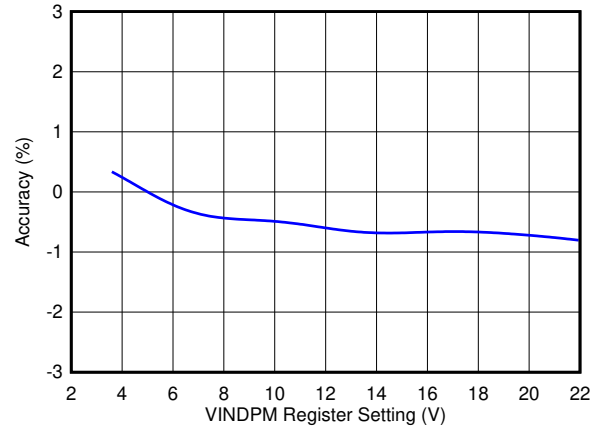
VBAT = 16.8V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

図 7-16. 4s Battery OTG Efficiency, 1.5 MHz



VBAT = 8V, Fsw = 1.5MHz with L1 = 1µH

図 7-17. Input Current Regulation (IINDPM) Accuracy



VBAT = 8V, Fsw = 1.5MHz with L1 = 1µH

図 7-18. Input Voltage Regulation (VINDPM) Accuracy

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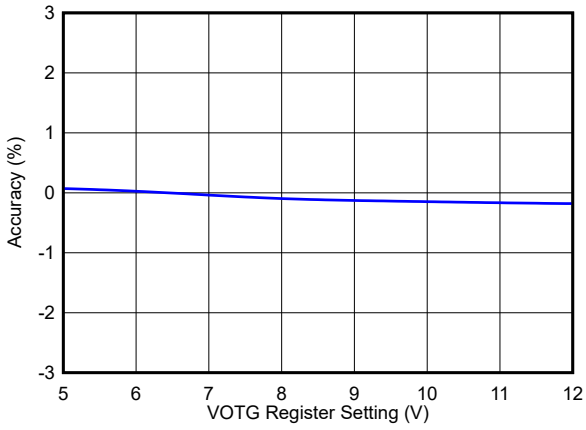
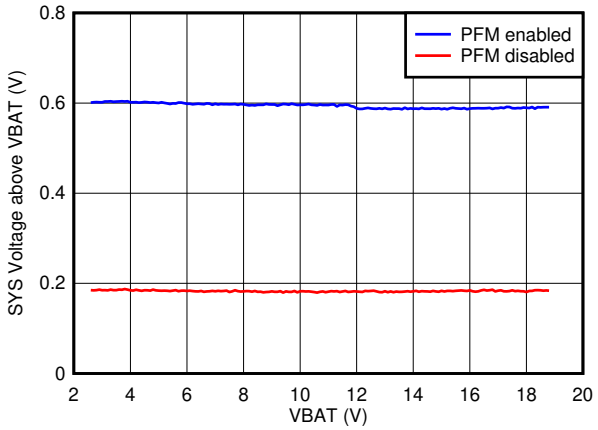
7.7 Typical Characteristics (continued)

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120) and L2 = 2.2µH (WE-LHMI-74437346022)



VBAT = 8.4V, Fsw = 1.5MHz with L1 = 1µH

図 7-19. OTG Voltage Regulation (VOTG) Accuracy



VBUS = 9V, Fsw = 1.5MHz with L1 = 1µH, ISYS = 0A, Charge Disabled

図 7-20. Offset Voltage of SYS Regulation above VBAT

8 Detailed Description

8.1 Overview

The BQ25672 is a fully integrated switch-mode buck charger for 1 cell to 4 cell Li-ion battery and Li-polymer battery. For compact design and minimum components count, the charger integrates the switching MOSFETs, input and charging current sensing circuits, the battery FET (BATFET) and all the loop compensation of the buck converter.

The charger supports narrow VDC (NVDC) power path management, in which the system is regulated at a voltage slightly higher than the battery voltage, but not drop below the minimum system voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds the input source rating, the battery gets into supplement mode and prevents the input source from being overloaded and the system from crashing.

The optional dual-input source selector manages the power flowing from two different input sources. The host controls the input source selection through I^2C with prioritizing the first available input source.

To support fast charging using adjustable high voltage adapter (HVDCP), the device provides D+/D- handshake. The device is compliant with USB 2.0 and USB 3.0 power delivery specification with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) allows the detection of maximum power point of an unknown input source. The BQ25672 also features a Maximum Power Point Tracking (MPPT) algorithm to optimize the energy drawn from a low-power photovoltaic panel. This MPPT algorithm measures the open-circuit voltage of the panel on a user-configurable period, then adjusts the VINDPM using the VOC_PCT setting to calculate the maximum power point as a percentage of the measured open-circuit voltage.

Besides the I^2C host controlled charging mode, BQ25672 also supports autonomous charging mode. After power up, the charging is defaulted enabled with all the registers default settings. The device can complete a charging cycle without any software engagements. It detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

In the absence of input sources, BQ25672 supports USB On-the-Go (OTG) function, discharging the battery to generate an adjustable, buck-boost, 5V to 12V output voltage on VBUS with 10mV step size.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor (NTC) monitoring, trickle charge, pre-charge and fast charge timers and over-voltage/over-current protections on the battery and the charger power input pin. The thermal regulation reduces charge current when the die temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The $\overline{INT}$ pin immediately notifies host when fault occurs.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring charge current and input/ battery/system voltages, the TS pin voltage and the die temperature. It is available in a QFN 4mm x 4mm, 29 pin package.

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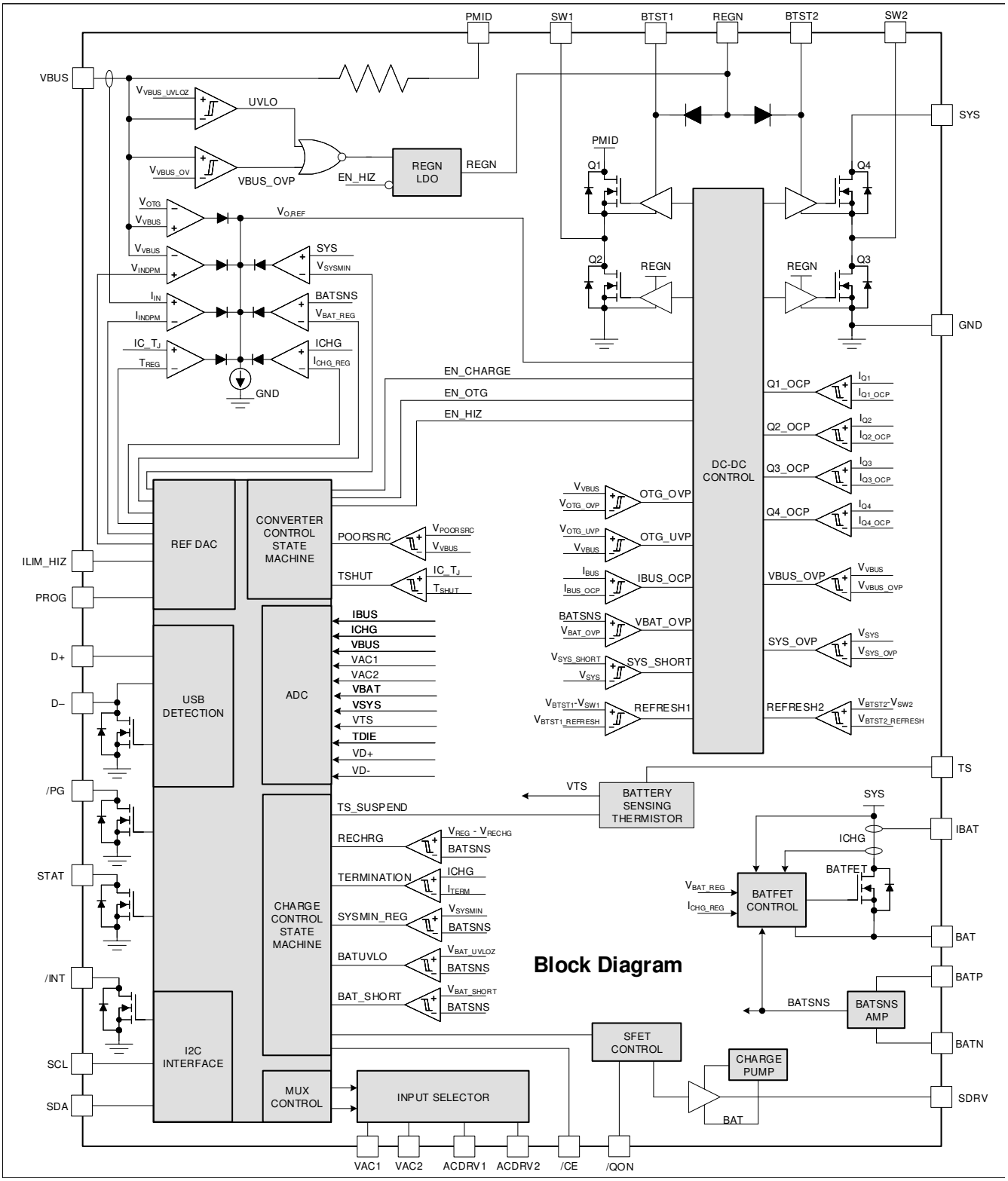
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power-On-Reset

The internal bias circuits are powered from the higher voltage, whichever V_{VBUS} or V_{BAT} through an integrated power selector. The valid voltage to power up the device has to be greater than either V_{VBUS_UVLOZ} or V_{BAT_UVLOZ} thresholds. When V_{VBUS} < V_{VBUS_UVLOZ}, V_{BAT} < V_{BAT_UVLOZ} and a voltage higher than $V_{AC_PRESENT}$ is present at either VAC1 or VAC2, the device will be powered from V_{AC1} or V_{AC2}, depending on which comes first.

Typically 5 ms after a valid voltage is first present at either V_{BAT}, V_{BUS} or V_{AC1} / V_{AC2}, the charger wakes up, starts the ACFET-RBFET detection, reading the resistance at PROG pin, then configures the charger power on reset (POR) register setting accordingly. Approximately 20ms after input voltage presence, the I^2C registers become accessible to the host.

8.3.2 PROG Pin Configuration

At POR, the charger detect the PROG pin pull down resistance, then sets the charger default POR switching frequency and the battery cell count. Please follow the resistance list in the table below to set the desired POR switching frequency and battery cell count. The surface mount resistor with ±1% or ±2% tolerance is recommended.

表 8-1. PROG Pin Resistance to Set Default Switching Frequency and Battery Cell Count

SWITCHING FREQUENCY	CELL COUNT	TYPICAL RESISTANCE AT PROG PIN
1.5 MHz	1s	3.0 kΩ
750 kHz	1s	4.7 kΩ
1.5 MHz	2s	6.04 kΩ
750 kHz	2s	8.2 kΩ
1.5 MHz	3s	10.5 kΩ
750 kHz	3s	13.7 kΩ
1.5 MHz	4s	17.4 kΩ
750 kHz	4s	27.0 kΩ

Some of the charging parameters default values are determined by the battery cell count identified by PROG pin configuration, which are summarized in the table below.

表 8-2. Charging Parameters Dependent on Battery Cell Count

CELL (REG0x0A[7:6])	1s	2s	3s	4s
ICHG (REG0x03/04)	1 A	1 A	1 A	1 A
VSYSMIN (REG0x00[5:0])	3.5 V	7 V	9 V	12 V
VREG (REG0x01/02)	4.2 V	8.4 V	12.6 V	16.8 V
VREG Range	3 V - 4.99 V	5 V - 9.99 V	10 V - 13.99 V	14 V - 18.8 V

After POR, the host can program the ICHG and VSYSMIN registers to any values within the ranges defined in the register tables. However, when programming the battery charging voltage (VREG), the host must ensure the VREG value falling into the right range associated with the CELL register (REG0x0A[7:6]) setting defined in the table above. When the CELL register is changed, the ICHG, VSYSMIN and VREG registers are reset to the POR default values associated with the CELL setting.

For example, if the PROG pin resistance is a 2s battery configuration, the default POR CELL, ICHG, VSYSMIN and VREG settings will be 2s, 1 A, 7 V and 8.4 V respectively. After POR, the host can change ICHG and VSYSMIN to any other values, and change VREG to any other values between 5V and 9.99V. With the CELL bits stay at 2s battery configuration, when REG_RST bit or watchdog timer expired, the registers are reset to default values with ICHG, VSYSMIN and VREG automatically return to 1 A, 7V, 8.4V respectively.

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When the CELL register is 2s battery configuration, any write out of the range of VREG (5 V - 9.99 V) is ignored by the charger. If VREG needs to be programmed out of the 5 V - 9.9 V range, like 11 V, the CELL bits have to be changed to 3s setting. The ICHG, VSYSMIN and VREG registers are reset to the 3s POR default values first, which are 1 A, 9 V and 12.6 V. After that, the host can program VREG in the range of 10 V - 13.99 V. In addition, when the CELL setting is changed to 3s, ICHG, VSYSMIN and VREG return to 1 A, 9 V and 12.6 V, when the registers are reset to the default values by REG_RST bit or the watchdog timer expiration.

8.3.3 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above UVLO threshold (V_{BAT_UVLOZ}), the BATFET turns on and connects the battery to the system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The POR sequence when the charger is powered from V_{BAT} is described as below:

1. 5 ms (typical) after $V_{BAT} > V_{BAT_UVLOZ}$, the charger starts ACFET-RBFET detection, reads the resistance at the PROG pin, and then configures the charger POR register set accordingly.
2. 20 ms (typical) after $V_{BAT} > V_{BAT_UVLOZ}$, the I^2C registers become accessible to the host..
3. The charger turns the battery FET on to allow the battery to power the system.

8.3.4 Device Power Up from Input Source

When an input source is present at VBUS, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck-boost converter is started. The power up sequence from input source is as listed below:

1. The device begins the POR sequence when $V_{VBUS} > V_{VBUS_UVLOZ}$ if there is a direct path from input to VBUS, or otherwise when V_{AC1} or $V_{AC2} > V_{AC_PRESENT}$.
2. 5 ms (typical) after a valid voltage is first present at either VBUS or VAC1/VAC2 pins, the charger starts the ACFET-RBFET detection, reads the resistance at PROG pin, and then configures the charger power on reset (POR) default register settings accordingly.
3. If ACFET-RBFET are detected on the input source pathway, the corresponding ACDRV turns on the pair.
4. 20 ms (typical) after valid voltage voltage presence, the I^2C registers become accessible to the host.
5. As soon as $V_{VBUS} > V_{VBUS_UVLOZ}$ (in step 1 or after step 3), VBUS_PRESENT_STAT is set to 1. 150 ms (typical) later, REGN is turned on.
6. Once REGN is on, the charger starts the poor source detection. After a good input source is detected (typically 30 ms if there is no retry), PG_STAT is set to 1, then the ADC reads the ILIM_HIZ pin voltage and VBUS voltage and updates the IINDPM and VINDPM registers accordingly.
7. When the poor source detection completes, the charger performs D+/D- detection and updates the VBUS_STAT and IINDPM registers accordingly.
8. 30 ms (typical) after the D+/D- detection completes, the converter starts switching to power SYS and charge the battery.

8.3.4.1 Power Up REGN LDO

When the device is powered up from VBUS, the LDO is turned on when $V_{VBUS_PRESENT} < VBUS < V_{VBUS_OVP}$. When the device is powered up from battery only condition, the LDO is turned on at either one of the following conditions:

- The charger is operated in the OTG mode
- VBAT is higher than 3.2V, and ADC TS channel is on (ADC_EN = 1 and TS_ADC_DIS = 0)

The REGN LDO supplies internal bias circuits and the MOSFETs gate drivers. The pull-up rails of ILIM_HIZ, TS, and STAT can be connected to REGN. The $\overline{INT}$ pin pull-up rail is recommended to be an external 1.8V or 3.3V voltage source, rather than REGN, because at battery only condition, the REGN might not be available. Except the charger related pull up rails, the REGN is not recommended to source any other external circuit. The REGN has to power the internal MOSFETs gate drivers, which is very critical for the charger normal operation.

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8.3.4.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$

Once the conditions are met, the status register bit PG_STAT is set high and the $\overline{INT}$ pin is pulsed to signal the host.

If VBUS_OVP is detected (failing condition 1 above), an $\overline{INT}$ pulse is asserted to alert the host if the VBUS_OVP_MASK = 0 or the PG_MASK = 0. The VBUS_OVP_STAT and VBUS_OV_FLAG fault registers get set, and the PG_STAT bit remains low. The device automatically retries input source qualification once the over-voltage fault goes away.

If a poor source is detected (when pulling $I_{POORSRC}$, the VBUS voltage drops below $V_{POORSRC}$), the EN_HIZ bit is set to 1, PG_STAT bit remains low, PG_FLAG will be set to 1, and an $\overline{INT}$ pulse will be asserted if PG_MASK = 0. The device will repeat the poor source qualification routine every 7 minutes until either the adapter is removed or the source is qualified. Each failed poor source qualification will cause EN_HIZ and PG_FLAG to be set to 1, and an $\overline{INT}$ pulse will be asserted if PG_MASK = 0. In the 7 minute interim between poor source qualification attempts, the host may set EN_HIZ = 0 to force an immediate retry of the poor source qualification. The EN_HIZ bit is cleared automatically when the adapter is plugged in, so cycling the adapter will also force an immediate retry of the poor source qualification.

8.3.4.3 ILIM_HIZ Pin

At POR, before the charger converter starts switching, the charger ADC reads the ILIM_HIZ pin voltage, and calculates the input current limit (ILIM) set by this ILIM_HIZ pin, according to:

$$V_{ILIM_HIZ} = 1V + 800\ m\Omega \times ILIM \quad (1)$$

The ILIM_HIZ pin sets a high clamp for the IINDPM register. If the IINDPM setting from the D+/D- detection or the POR default 3A IINDPM setting is higher than the ILIM clamp, the IINDPM register stays at this ILIM clamp. In addition, the host cannot program the IINDPM register to any values higher than this ILIM clamp after POR, unless the register bit EN_EXTILIM is set to 0.

The ILIM_HIZ pin can be biased from a resistor voltage divider tied to either REGN or another external voltage source. For both the forward charging mode and the OTG mode, when the ILIM_HIZ pin is pulled lower than 0.75V, the charger stops switching and REGN stays on. The charger resumes switching if the ILIM_HIZ pin voltage becomes higher than 1V.

If the ADC reads the ILIM_HIZ pin voltage is lower than 1.08V (1V + 800 mΩ × 100 mA), the charger considers the ILIM clamp to be 100mA, which is the minimal setting of the IINDPM register.

8.3.4.4 Default VINDPM Setting

In the POR sequence, right after the D+/D- detection, the charger initiates an ADC reading on the VBUS pin voltage without any load current (VBUS at no load condition, $VBUS_0$) before the converter starts switching. The default VINDPM threshold is set to be $VBUS_0$ - 1.4 V ($VBUS_0$ >= 7 V) or $VBUS_0$ - 0.7V ($VBUS_0$ < 7 V).

The $VBUS_0$ can be remeasured at any time by setting the register bit FORCE_VINDPM_DET=1. The converter stops switching, the ADC measures the VBUS voltage, the VINDPM register field is updated, and then the FORCE_VINDPM_DET bit returns to 0. The force VINDPM detection only can be done when VSYS_STAT = 0 (VBAT > VSYSMIN), otherwise stopping the converter would cause VSYS to drop below VSYSMIN. If VSYS_STAT = 1 (VBAT < VSYSMIN), $VBUS_0$ measurement does not start, the FORCE_VINDPM_DET bit resets to 0 and the VINDPM register retains its current value. The host must ensure there is a battery present prior to setting FORCE_VINDPDM_DET = 1, or to allow system to be supported by the battery during detection.

When the measured $VBUS_0$ is out of the VINDPM register range, the changer sets the VINDPM register to the minimum value (3.6V) or maximum (22V) value as appropriate.

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8.3.4.5 Input Source Type Detection

After the input source is qualified, the charger runs Input Source Type Detection if AUTO_INDET_EN bit is set (default enabled).

The charger follows the USB Battery Charging Specification 1.2 (BC1.2) to detect SDP/CDP/DCP/HVDC input sources and the non-standard adapters through the USB D+/D- lines. After BC1.2 detection is completed, the BC1.2_DONE_STAT bit is set to 1, and an $\overline{\text{INT}}$ pulse and BC1.2_DONE_FLAG are asserted if BC1.2_DONE_MASK = 0. In addition, when USB DCP is detected, the charger initiates adjustable high voltage adapter handshake on D+/D- if HVDCP detection is enabled by the host. The input type might be changed after HVDCP detection is completed.

After input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits change to reflect the detected source

After detection is completed, the host can over-write IINDPM registers to change the input current limit if necessary. The charger input current is limited by the lower of IINDPM register or ILIM_HIZ pin (when EN_EXTILIM = 1) regardless of Input Current Optimizer (ICO) setting. When AUTO_INDET_EN is disabled, the Input Source Type Detection is bypassed, and the Input Current Limit (IINDPM) register remains unchanged from its previous value.

8.3.4.5.1 D+/D– Detection Sets Input Current Limit

The device contains a D+/D- based input source detection to set the input current limit. The D+/D- detection has four major steps: Data Contact Detect (DCD), Primary Detection, Secondary Detection and High Voltage DCP (HVDCP) detection.

The D+/D- Primary Detection includes standard USB BC1.2 and non-standard adapters. When an input source is plugged in, the device starts standard USB BC1.2 detection first. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The non-standard detection is used to distinguish vendor specific adapters based on the unique dividers they apply to the D+/D- pins. The secondary detection is used to distinguish two types of charging ports, CDP and DCP.

A CDP usually requires the attached device to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port will power cycle back to SDP even the D+/D- detection indicates CDP. This enumeration must be handled externally to the charger.

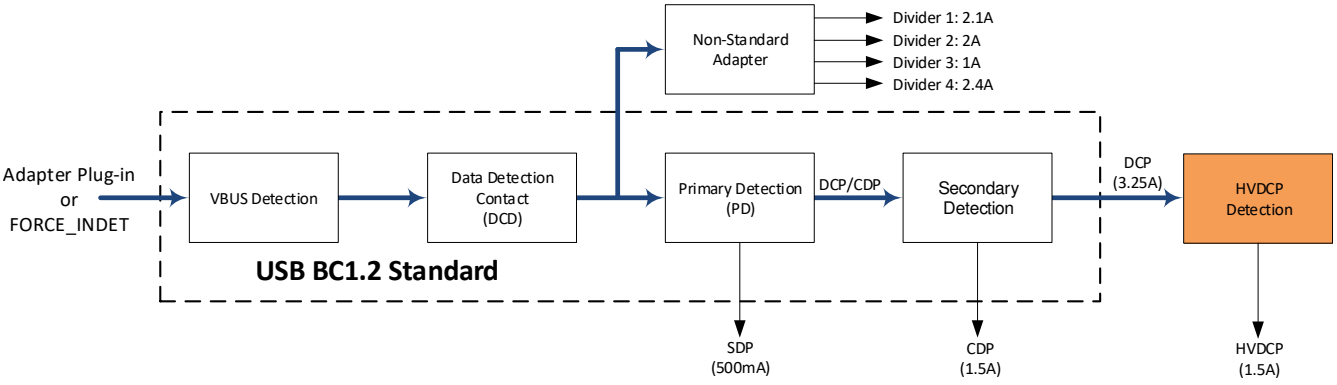

図 8-1. D+/D– Detection Flow

表 8-3. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1 A
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D+} within V_{1P2_VTH}	2A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1 A

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表 8-3. Non-Standard Adapter Detection (continued)

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT
Divider 4	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4 A

When a Dedicated Charging Port (DCP) is detected, the charger initiates two high voltage adapter (HVDCP) handshakes to enable the corresponding adapter to output a higher voltage for fast charging. The HVDCP detection can be enabled by setting EN_HVDCP=1 and then setting either EN_9V=1 to increase the input voltage to 9V or EN_12V=1 to increase the input voltage to 12V. When EN_12V and EN_9V are both set to 1, the charger starts 12V first.

After the input source type detection is done, the DPDM_STAT bit is set to 0, an $\overline{INT}$ pulse and DPDM_DONE_FLAG are asserted if DPDM_DONE_MASK = 0. In addition, REG06_Input_Current_Limit and VBUS_STAT are updated as shown in 表 8-4.

表 8-4. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINDPM)	VBUS_STAT_3:0
USB SDP	500 mA	0001
USB CDP	1.5 A	0010
USB DCP	3.25 A	0011
Adjustable High Voltage DCP (HVDCP)	1.5A	0100
Unknown Adapter	3 A	0101
Non-Standard Adapter, Divider 1	2.1 A	0110
Non-Standard Adapter, Divider 2	2 A	0110
Non-Standard Adapter, Divider 3	1 A	0110
Non-Standard Adapter, Divider 4	2.4 A	0110

8.3.4.5.2 HVDCP Detection Procedure

図 8-1 shows that an HVDCP source is first qualified as a DCP source in the USB BC1.2 standard detection stage, then qualified in the following HVDCP detection stage as an HVDCP source. When the HVDCP is first qualified as a DCP, the charger sets an IINDPM limit of 3.25A. The IIDPM is then updated to the HVDCP limit of 1.5A after the HVDCP handshake completes. In some cases the higher IINDPM limit of 3.25A may interfere with the source's ability to transition to 9V or 12V if the transition is attemped before the IINDPM is updated to 1.5A.

The recommended procedure for enabling detection of HVDCP sources is completed in the following steps:

- Before adapter insertion, the charger is configured with AUTO_INDET_EN = 1 and HVDCP_EN = 0. EN_12V and EN_9V are set as desired for the system.
- When an adapter is inserted, it will be detected as SDP, CDP, DCP or a Non-Standard adapter and an I^2C interrupt is sent to the host. If any detection other than DCP is made, the host proceeds as usual.
- If the adapter is detected as DCP (VBUS_STAT[3:0] = 0011), the host first changes the Input Current Limit register to 1.5A and then changes HVDCP_EN = 1.
- After HVDCP detection is complete, the host sets HVDCP_EN = 0 to disable HVDCP support in preparation for the next input source detection sequence.

8.3.4.5.3 Connector Fault Detection

The host can apply different status on D+ pin including HIZ, 0V, 0.6V, 1.2V, 2.0V, 2.7V, 3.3V or "short to D-", and different status on D- pin including HIZ, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V. The device also provides ADC readings of the D+ and D- pin voltages. The host can use the information to determine if connector is normal or in any faults. The voltage values are set using the DPLUS_DAC and DMINUS_DAC register. The D+/D- pins are only applied at the VAC1 input source. If the DPLUS_DAC or DMINUS_DAC are programmed when the adapter is plugged in and the D+/D- detection is in process, the device will ignore the register programming.

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8.3.5 Dual-Input Power Mux

The BQ25672 has two ACDRV drivers to control two optional sets of back-to-back power N-FETs, selecting and managing the power from two different input sources. In the POR sequence, the charger detects whether the ACFETs-RBFETs are present, then updates the ACRB1_STAT or ACRB2_STAT status bits accordingly. The ACFET1-RBFET1 or ACFET2-RBFET2 can be controlled by setting the register bit EN_ACDRV1 or EN_ACDRV2. If the external ACFET-RBFET is not present, then tie VAC1 / VAC2 to VBUS and connect ACDRV1 / ACDRV2 to GND. The power MUX drivers support three different application cases, which are elaborated in detail below.

8.3.5.1 VBUS Input Only

In this scenario, only single input is connected to VBUS directly, no back-to-back power MOSFETs are required. VAC1 and VAC2 are recommended to be shorted to VBUS. Both ACDRV1 and ACDRV2 need to be pulled down to GND, as shown in the figure below.

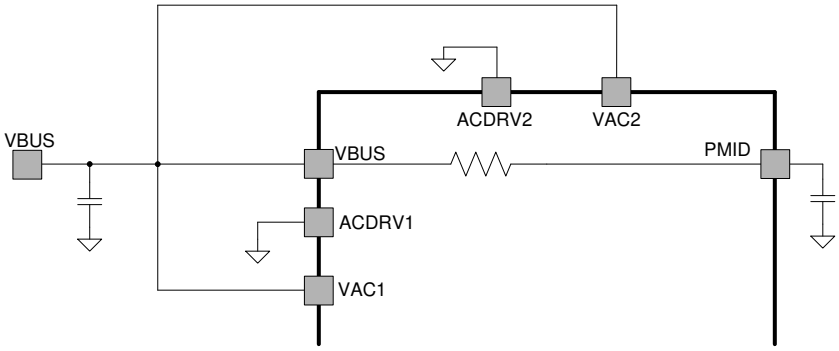

図 8-2. Single Input Connected to VBUS Directly Without ACFET-RBFET

- At POR, the charger detects no ACFETs-RBFETs are present by sensing that the ACDRV1 and ACDRV2 pins both shorted to GND.
- The charger updates the status bits ACRB1_STAT and ACRB2_STAT to 0, and locks EN_ACDRV1 = 0 and EN_ACDRV2 = 0.
- VAC1 and VAC2 are connected to VBUS directly. The ACDRV1 and ACDRV2 pins always stay low.

8.3.5.2 One ACFET-RBFET

In this configuration, only ACFET1-RBFET1 is present, ACFET2-RBFET2 is not. VAC1 is tied to the drain of ACFET1, ACDRV1 is connected to the gate of ACFET1. VAC2 is shorted to VBUS, ACDRV2 is pulled down to GND. This structure is illustrated in the figure below, which is able to support either single input (one from VAC1 to VBUS through ACFET1-RBFET1, or one to VBUS directly) or dual-input (one from VAC1 to VBUS through ACFET1-RBFET1, the other one connected to VBUS directly) applications.

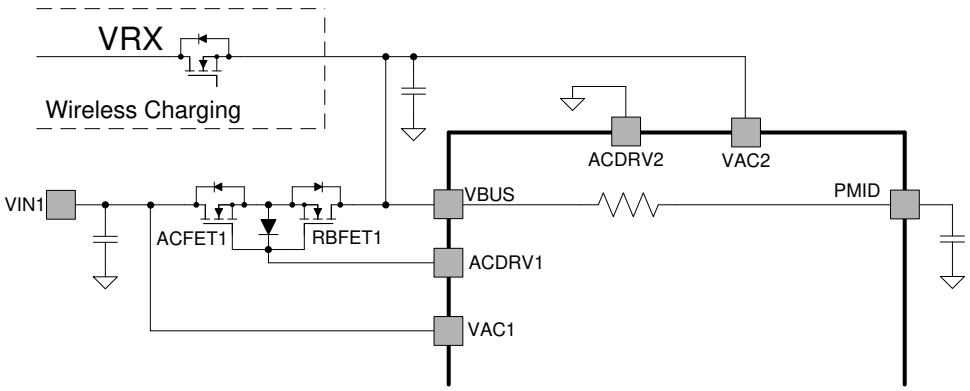

図 8-3. One ACFET-RBFET Structure Supporting One Input at VAC1 and/or One Input at VBUS

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- At POR, the charger detects only ACFET1-RBFET1 presented, updates ACRB1_STAT to 1 and keeps ACRB2_STAT as 0.
- The charger locks the register bit EN_ACDRV2 at 0, and the ACDRV2 pin will always stay low.
- When a valid input is presented at VAC1, the charger will set EN_ACDRV1 = 1 and turn ACFET1-RBFET1 on.
- To swap from the input at VAC1 to the input at VBUS, the host has to turn off the ACFET1-RBFET1 first by setting DIS_ACDRV=1 (forcing EN_ACDRV1 = 0), then enable the other input source which is connected to VBUS directly.
- In contrast, to swap from the input at VBUS to the input at VAC1, the host has to disable the input source connected to VBUS first, then turn on the ACFET1-RBFET1 by setting DIS_ACDRV = 0.

8.3.5.3 Two ACFETs-RBFETs

In this scenario, both ACFET1-RBFET1 and ACFET2-RBFET2 are present. VAC1 / VAC2 is tied to the drain of ACFET1 / ACFET2, ACDRV1 / ACDRV2 is connected to the gate of ACFET1 / ACFET2. This structure is developed to support dual-input connected at VA1 and VAC2.

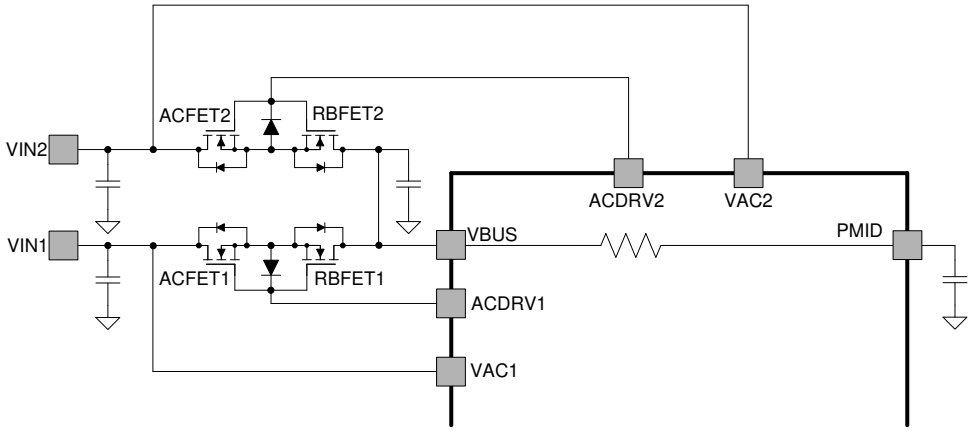

図 8-4. Two ACFETs-RBFETs Structure Supporting One Input at VAC1 and One Input at VAC2

- At POR, the charger detects both ACFET1-RBFET1 and ACFET2-RBFET2 presented, then updates ACRB1_STAT and ACRB2_STAT to 1.
- EN_ACDRV1 and EN_ACDRV2 are programmable in this case.
- The ACDRV turns on the ACFET-RBFET of the port with a valid input presented first. The other ACFET-RBFET stays off, even if there is an adapter being plugged in later.
- Programming EN_ACDRV1 = 1, EN_ACDRV2 = 1 at the same time to turn on both ACFET1-RBFET1 and ACFET2-RBFET2 is not allowed, which will be ignored by the charger.
- Assuming two valid voltages are presented at VAC1 and VAC2, ACFET1-RBFET1 turns on, connecting the input source at VAC1 to VBUS. If the voltage at VAC1 becomes invalid because of VAC_UVLO, VAC_OV or IBUS_OC, the charger swaps the input from VAC1 to VAC2, by turning off ACFET1-RBFET1 and then turning on ACFET2-RBFET2, without any host engagement. Swapping the input from VAC1 to VAC2 also can be controlled by the host. For example, to swap VAC1 to VAC2, the host can program REG0x13[7:6] (EN_ACDRV2, EN_ACDRV1) from 01b to 10b. The same control logic is applied to the input swapping from VAC2 to VAC1.

The waveforms below show the charger input transition from VAC1 to VAC2 when VAC1 is disconnected. At the beginning, VAC1 = 12V and VAC2 = 8V are both present. When VAC1 = 12V is gone, the charger accomplishes the input source auto transition from VAC1 to VAC2 without host control.

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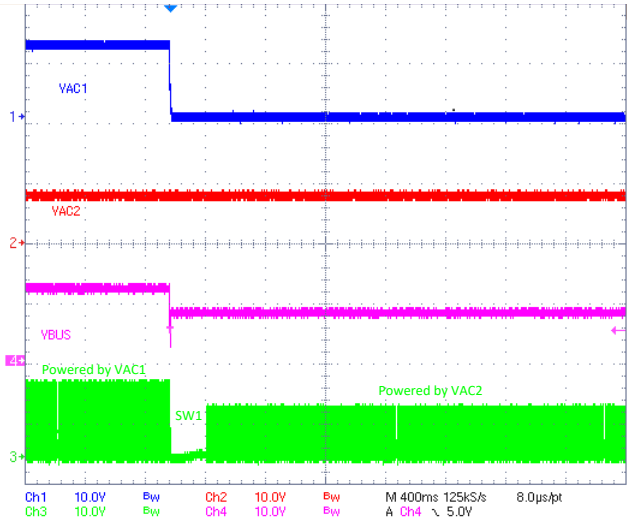

図 8-5. Input Source Auto Transition from VAC1 to VAC2 when VAC1 is Gone

When VAC2 has been connected, even if VAC1 is re-plugged in again later, the charger still stays connecting VAC2 as the input source, which is illustrated as the waveforms below. The host has to be involved to swap the input source from VAC2 back to VAC1 if necessary.

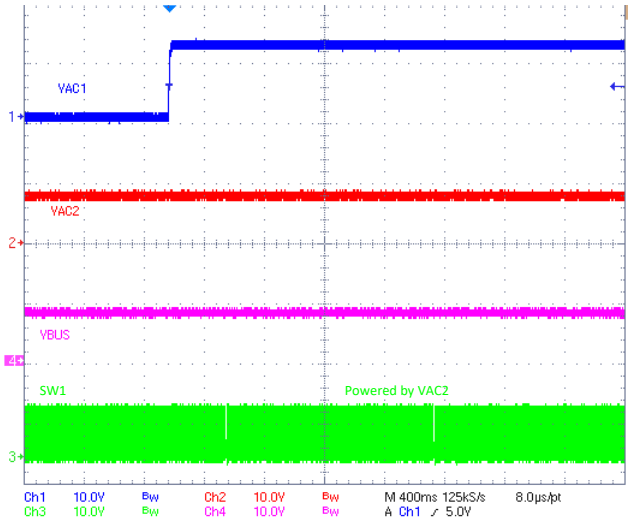

図 8-6. VAC1 Re-Plugged in When VAC2 Connected as the Charger Input

Some other critical notes for the application of this dual input power MUX are list below:

- The register bits, EN_ACDRV1 and EN_ACDRV2, are not only to control the turning on / off of ACFETs-RBFETs but also to indicate the on / off status of the FETs.
- The charger also provides the fault protection by turning ACFETs-RBFETs off, such as VAC_OVP and IBUS_OCP.
- With only one valid input presented at either VAC1 or VAC2, the ACFET1-RBFET1 and ACFET2-RBFET2 can not be both turned off by setting REG0x13[7:6] = 00b, because the charger is always trying to connect the only one input voltage available to power the charger. At this condition, the host has to set DIS_ACDRV = 1 to force both two ACFETs-RBFETs off. With two input sources presented at both VAC1 and VAC2, the host can turn of the two ACFETs-RBFETs by setting either REG0x13[7:6] = 00 or DIS_ACDRV = 1.
- In the transition from one input to the other one, after one ACFET-RBFET is turned off, the other one turns on until the VBUS voltage drops lower than $V_{BUS_PRESENT}$. The converter stops switching for a short time period.

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When no battery presented or battery depleted, the system output would fall. The user has to be aware of this and avoid the input source swap when the battery voltage is too low.

8.3.6 Buck Converter Operation

The charger employs a synchronous buck converter that allows charging the 1s to 4s battery from an input power source.

With a battery attached at BAT and input power at VBUS, the charger can provide at least the MINSYS voltage at SYS and charge current for the battery at BAT. Once the battery voltage reaches the MINSYS voltage, the SYS voltage follows the BAT voltage up. With no battery attached to BAT and input power at VBUS, the voltages at SYS and BAT vary depending on the whether or not charge is enabled as explained below.

1. No battery or battery removed and charge disabled by CE pin or EN_CHG register or thermistor removed from TS pin - The charger keeps the BAT pin voltage at low-level, steady-state voltage and regulates SYS pin to MINSYS. The host can monitor the ADC BAT pin voltage and TS fault register to determine when a valid battery is attached.
2. No battery or battery removed while charge enabled and TS pin function is disabled - The charger continuously tries to charge the BAT capacitance, typically resulting in the BAT voltage alternating between a low level and BATOVP fault. The SYS voltage follows the battery voltage up, potentially reaching SYSOVP fault. In order to determine if a battery is attached, the host must periodically disable charge, force IBAT discharge current and then read the ADC BAT pin voltage. Alternatively, the host can monitor the INT pin for rapid interrupts and then read the charge status bits for fast (<1 s for typical BAT pin capacitance) toggling between charging, taper and termination.

8.3.6.1 Force Input Current Limit Detection

In host mode, the host can force the device to run Input Current Limit Detection by setting FORCE_INDET bit to 1. After the detection is completed, FORCE_INDET bit automatically returns to 0. After the detection is completed, the input REG06_Input_Current_Limit (IINDPM), and the VBUS_STAT bits may be changed by the device according to the detection result.

8.3.6.2 Input Current Optimizer (ICO)

The device provides Input Current Optimizer (ICO) to identify maximum power point in order to avoid overloading the input source. The algorithm automatically identifies maximum input current limit of an unknown power source and sets the charger IINDPM register properly, in order to prevent from entering the charger input voltage (VINDPM) regulation. This feature is disabled by default at POR (EN_ICO = 0) and only activates when EN_ICO bit is set to 1.

After DCP type input source is detected based on the procedures described in セクション 8.3.4.5, the algorithm runs automatically if EN_ICO bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected. Please note that EN_ICO = 1 is required for FORCE_ICO to work.

The actual input current limit used by the Dynamic Power Management is reported in the ICO_ILIM register whether set by ICO if enabled or IINDPM register if not. In addition, the current limit is clamped by the ILIM_HIZ pin unless EN_EXT_ILIM bit is 0 to disable the ILIM_HIZ pin function.

When V(BAT) > VMINSYS, the ICO algorithm starts with the maximum allowed input current as reported in ICO_ILIM register as 500 mA then continually increases this limit until the optimal limit is found. When VBAT < VSYSMIN, the battery voltage can be too low to supplement a large system load if the charger buck converter is limited to 500 mA and then ramped up by the ICO algorithm. Therefore, when a VBAT < VSYSMIN, the ICO algorithm starts with the maximum allowed input current as reported in ICO_ILIM register to the input current-limit register value in REG0x06 and then continually decreses this limit until the optimal limit is found.

Once the optimal input current is identified, the ICO_STAT[1:0] and ICO_FLAG bits are set. The actual input current is reported in the ICO_ILIM register and does not change unless the algorithm is triggered again by the following events :

1. A new input source is plugged-in, or EN_HIZ bit is toggled
2. IINDPM register is changed

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3. VINDPM register is changed
4. FORCE_ICO bit is set to 1
5. VBUS_OVP event

These events also reset the ICO_STAT[1:0] bits to 01

8.3.6.3 Maximum Power Point Tracking for Small PV Panel

The device implements a simple algorithm to track the maximum power point (MPP) when the input source is a solar panel. The I-V and P-V curves of a solar panel are most strongly dependent on irradiation and temperature. The MPP is most commonly located between 70%~90% of the Open Circuit Voltage (VOC) of the solar panel. The algorithm automatically and periodically detects the charger input source VOC, and sets the VINDPM to be a ratio of the measured VOC. It is recommended to set the charging current to the maximum value, so that the VINDPM is always triggered and activated. The MPPT algorithm is disabled by default at POR (EN_MPPT = 0). The algorithm runs automatically when EN_MPPT bit is set to 1.

Similar to the FORCE_VINDPM_DET feature, when the battery voltage is lower than VSYSMIN (VSYS_STAT = 1), the MPPT algorithm can not be enabled. The EN_MPPT bit will be reset back to 0 if it is written to 1. In the MPPT process, the buck-boost charger stops switching and keeps in the non-switching status for a time period programmed by VOC_DLY[1:0]. When the charger stops switching, the system is powered by the battery discharging. Then the charger measures the open-circuit voltage of the input soruce attached at VBUS and updates the VINDPM to be VOC_PCT[2:0]*VOC. The converter starts up again for the VOC_RATE[1:0] time interval, stops switching for another VOC_DLY[1:0], measures VOC, and updates the VINDPM register to complete the next cycle. When VBUS goes below $V_{BUS_PRESENT}$, the EN_MPPT bit will be reset to 0, and forced to be 0 even if the host writes it to 1.

For the EN_ICO, FORCE_VINDPM_DET and EN_MPPT three register bits, only one of them can be set to 1 at a given time. If one of them is enabled, the charger will block the host from enabling the other two features until the first is disabled.

8.3.6.4 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly as load current decreases. The PFM operation can be disabled by setting PFM_FWD_DIS = 1. With PFM disabled, the converter stays at the PWM mode switching frequency and transitions into DCM operation at light load condition. The minimum effective switching frequency in PFM can be limited to 25 kHz to eliminate the audible noise concern if the out of audio (OOA) feature is enabled by setting DIS_FWD_OOA = 0. The host can disable the OOA by setting DIS_FWD_OOA = 1, which may result in the converter effective switching frequency dropping below 25 kHz at extremely light load. The PFM operation of OTG mode can be independently controlled using the PFM_OTG_DIS and DIS_OTG_OOA bits. In PFM mode, the converter limits peak inductor current to 2 A, when OOA is enabled, and 3.3 A if OOA is disabled or if the load has increased close to the point of exiting PFM.

8.3.6.5 Device HIZ State

The charger enters HIZ mode when EN_HIZ bit is set to 1. The HIZ mode refers to a charger state, in which the REGN LDO is off, and the converter stops switching even if the adapter is present. Similar to the battery only condition, the charger is in a low quiescent current mode, turns off the ADC and turns on the BATFET to support the system load. The ADC can be re-enabled during HIZ by setting EN_ADC =1.

Some of the faults, such as VBUS_OVP, VSYS_OVP, VBAT_OVP and OTG_OVP, force the converter to stop switching but keep the REGN and other internal circuits powered on. Alternatively, some of the faults, like VSYS_SHORT and IBUS_OCP, force the charger into HIZ mode by setting EN_HIZ=1. More details could be found in the セクション 8.3.13.

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8.3.7 USB On-The-Go (OTG)

8.3.7.1 OTG Mode to Power External Devices

The device supports the OTG operation to deliver power from the battery to other external devices through the USB ports. The OTG voltage regulation is set in VOTG[10:0] register bits. The OTG current regulation is set in IOTG[6:0] register bits. To enable the OTG operation, the following conditions have to be valid:

- The battery voltage is higher than V_{BAT_OTG} rising threshold, and not trigger the VBAT_OVP protection.
- The VBUS is below V_{VBUS_UVLO}.
- The voltage at TS pin is within the range configured by BHOT and BCOLD register bits

If the ACFET1-RBFET1 and the ACFET2-RBFET2 are not detected (ACRB1_STAT = 0 and ACRB2_STAT = 0) at POR, the converter starts up with typical 5ms delay after the EN_OTG bit is set to 1, then the VBUS voltage ramps up to the VOTG register setting.

The following cases explain the charger OTG mode behaviors when the ACFET1-RBFET1 or/and ACFET2-RBFET2 are present.

- If only ACRB1_STAT=1 OR only ACRB2_STAT = 1, which means only one input ACFET-RBFET is present, the converter stays in the non-switching mode after the EN_OTG bit is set, until the host writes EN_ACDRV1 = 1 (when only ACRB1_STAT = 1) or EN_ACDRV2 = 1 (when only ACRB2_STAT = 1). The converter starts up with 5ms delay after the EN_ACDRV1 or EN_ACDRV2 bit is set to 1, then VBUS voltage ramps up to the VOTG register setting.
- If both ACRB1_STAT = 1 AND ACRB2_STAT = 1, which means two input ACFET-RBFET are present, the converter stays in the non-switching mode after the EN_OTG bit is set, until the host writes either EN_ACDRV1 = 1 or EN_ACDRV2 = 1. The converter starts up with 5ms delay after the EN_ACDRV1 or EN_ACDRV2 bit is set to 1, then VBUS voltage ramps up to the VOTG register setting.
- Regardless of ACRB1_STAT and ACRB2_STAT, if DIS_ACDRV = 1, the ACDRV is disabled. The converter starts up with 5ms delay after the EN_OTG bit is set to 1, then VBUS voltage ramps up to the VOTG register setting. The operation is the same as that when ACFET1-RBFET1 and ACFET2-RBFET2 are not detected.
- For swapping the OTG output from port 1 to port 2, assuming EN_ACDRV2 is already 0, the host has to set EN_ACDRV1 = 0 to turn off ACFET1_RBFET1 first, which causes the converter to stop switching and VBUS to drop below $V_{BUS_PRESENT}$. The host sets EN_ACDRV2 = 1, the converter starts switching again and ACDRV2 turns on ACFET2-RBFET2, which allows VBUS to ramp up. The similar procedure can be applied to the case of swapping the OTG output from port 2 to port 1.

In OTG mode, the converter PFM operation can be disabled by setting PFM_OTG_DIS = 1 and the OOA can be disabled by setting DIS_OTG_OOA = 1.

The simplified application diagram for the OTG mode operation is shown as the figure above, in which the power flow is illustrated by the blue arrows.

The charger is also monitoring the battery discharging current in OTG mode. When IBAT rises higher than the IBAT_REG[1:0] register setting, the charger reduces the OTG output current and prioritizes the system load current if there is any. The IBAT_REG_STAT bit is set to 1 and an $\overline{INT}$ pulse is asserted and the IBAT_REG_FLAG is set to 1, if IBAT_REG_MASK = 0. If the OTG output current is decreased to zero and the system load pulls even more current, the charger can no longer limit the battery discharging current.

8.3.8 Power Path Management

The device accommodates a wide range of input voltages ranging from 3.6V to 24V covering the legacy 5V USB, HVDCP, USB-PD and the wall adapters. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT) or both.

8.3.8.1 Narrow Voltage DC Architecture

The device deploys the NVDC architecture with a BATFET separating the system from the battery. Even with a fully depleted battery, the system is regulated above the minimum system voltage. The minimum system voltage is set by VSYSMIN bits. The default minimum system voltage at POR is determined according to different battery cell settings.

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The NVDC architecture also provides the charging termination when the battery is fully charged. By turning off the BATFET, the adapter power is prioritized to support the system, which avoid the battery being continuously charged and discharged by the system load even if the adapter is present. This is very important to keep the battery in a healthy condition and extend the battery life time.

When the battery voltage is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at around 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the Rdson of BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above the minimum system voltage setting or charging is terminated, the system is always regulated at typically 200mV (PFM disabled) or typical 600mV (PFM enabled) above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

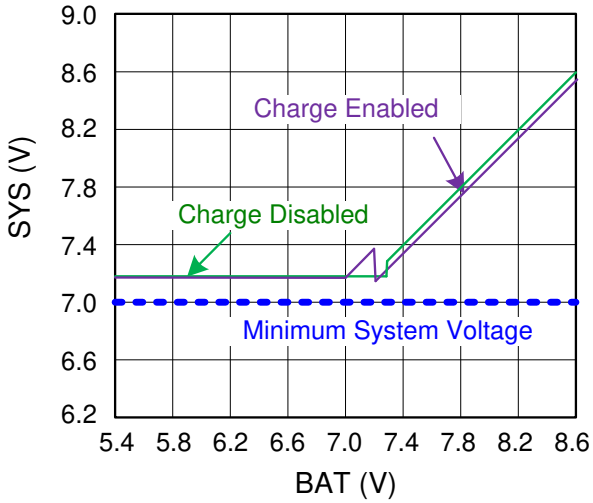

図 8-7. Typical System Voltage vs Battery Voltage for a 2S Battery Configuration

8.3.8.2 Dynamic Power Management

To meet the maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input power at the VBUS pin is too low to support the load from SYS pin and the battery charge current from BAT pin, the charger engages either IINDPM to limit its current or VINDPM to prevent further reduction in VBUS pin voltage.

When the system voltage is regulated at VSYSMIN, the charger could be in trickle charge, pre-charge or fast charge stages, the SYS voltage drops lower than VSYSMIN, the VSYSMIN loop takes over and reduces the trickle charge, pre-charge or fast charge current, so that the SYS voltage remains at the VSYSMIN level.

If the charge current falls to zero, but the input source is still overloaded, the SYS voltage will drop. Once the SYS voltage falls below the battery voltage, the device automatically enters Supplement Mode in which the BATFET turns on. The battery starts discharging so that the system is supported from both the input source and battery. In supplement mode, the battery FET is operated in ideal diode mode in which the charger regulates the battery FET gate voltage to keep the BATFET minimum V_{DS} to approximately 25 mV when the current is low. This prevents SYS voltage oscillations from entering and exiting the supplement mode. As the discharge current increases, the charger regulates the BATFET gate to a higher voltage, in order to reduce the battery FET R_{DSON} until the MOSFET is in full turn-on stage. At this point onwards, the V_{DS} of the battery FET linearly increase with the discharge current. The figure below shows the V-I curve of the BATFET gate regulation operation. The BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold.

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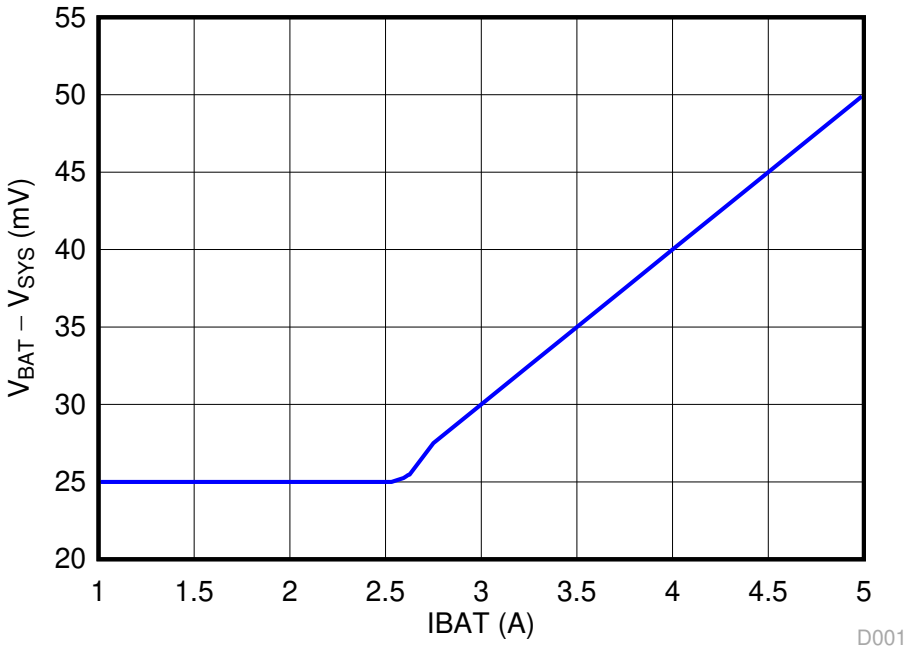

図 8-8. BATFET I-V Curve

During DPM mode, the status register bits VINDPM_STAT (VINDPM) and/or IINDPM_STAT (IINDPM) go high. The figure below shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current and 3.5V minimum system voltage setting.

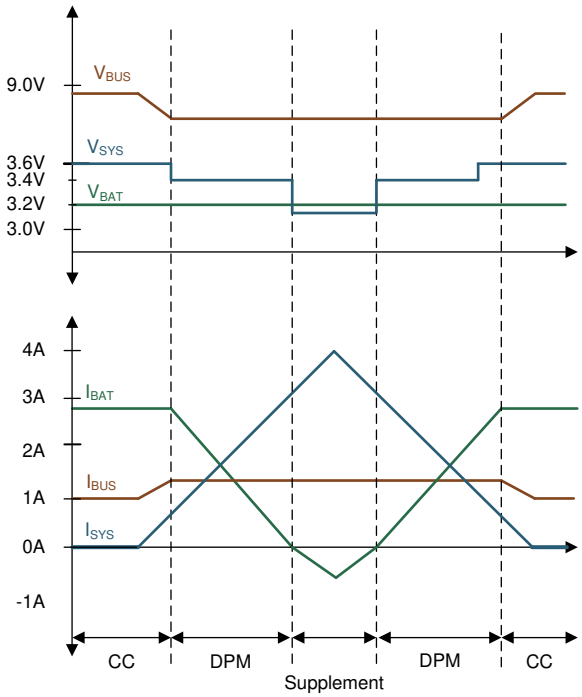

図 8-9. DPM Response

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8.3.9 Battery Charging Management

BQ25672 charges 1S~4S Li-Ion batteries with up to 3A charge current for high capacity cells. The battery charging in different stages is controlled by the integrated BATFET. The low $R_{DS(ON)}$ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

8.3.9.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit =1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in the table below. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

表 8-5. Charging Parameter Default Settings

DEFAULT MODE	
Charging voltage	4.2 V (1S), 8.4 V (2S), 12.6 V (3S), 16.8 V (4S)
Recharging voltage threshold	200 mV
Fast charge current	2 A (1S and 2S), 1 A (3S and 4S)
Pre-charge current	120 mA
Trickle charge current	100 mA
Termination current	200 mA
Temperature profile	JEITA
Fast charge safety timer	12 hours
Pre charge safety Timer	2 hours
Trickle charge safety Timer	1 hour

A new charge cycle starts when the following conditions are valid:

- Converter starts up
- Battery charging is enabled by setting register bit EN_CHG = 1 and keeping $\overline{CE}$ pin LOW
- No thermistor fault on TS pin
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits), the device automatically starts a new charging cycle. After the charging terminates, toggling either $\overline{CE}$ pin or EN_CHG bit initiates a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charging disabled (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting DIS_STAT = 1. In addition, the status register (CHG_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (VBAT < V_{BAT_SHORTZ})
- 010 – Pre-charge (V_{BAT_SHORTZ} < VBAT < V_{BAT_LOWV})
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when the charge cycle completes, an $\overline{INT}$ is asserted to notify the host.

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8.3.9.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

表 8-6. Default Charging Current Setting

VBAT	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< V_{BAT_SHORT}	I_{BAT_SHORT}	100 mA	001
V_{BAT_SHORTZ} to V_{BAT_LOWV}	I_{PRECHG}	120 mA	010
> V_{BAT_LOWV}	ICHG	1 A	011

If the charger is in DPM regulation or thermal regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Charging Safety Timer.

The V_{BAT_SHORTZ} is the battery voltage threshold for the transition from trickle charge to pre-charge, which is fixed value 2.2V. During the trickle charge to pre-charge transition, the charger regulates the battery voltage to 2.5V/cell typical for t_{BAT_SHORTZ} duration. V_{BAT_LOWV} is the battery voltage threshold for the transition from pre-charge to fast charge. It is defined as a ratio of battery voltage regulation limit (VREG).

During SYSMIN regulation with BATFET LDO operation, the charge current is limited to 2 A maximum, regardless of the charge current register setting being set higher than 2 A, in order to protect the BATFET. The BATFET LDO operation can be disabled by setting DIS_LDO = 1. In this condition, the pre-charge current and fast charge current are both regulated by the buck converter PWM current regulation loop. The SYS is no longer regulated to VSYSMIN when the LDO mode is disabled at the low battery voltage condition. When in trickle charge, setting DIS_LDO = 1 does not affect I_{BAT_SHORT} or VSYSMIN operation.

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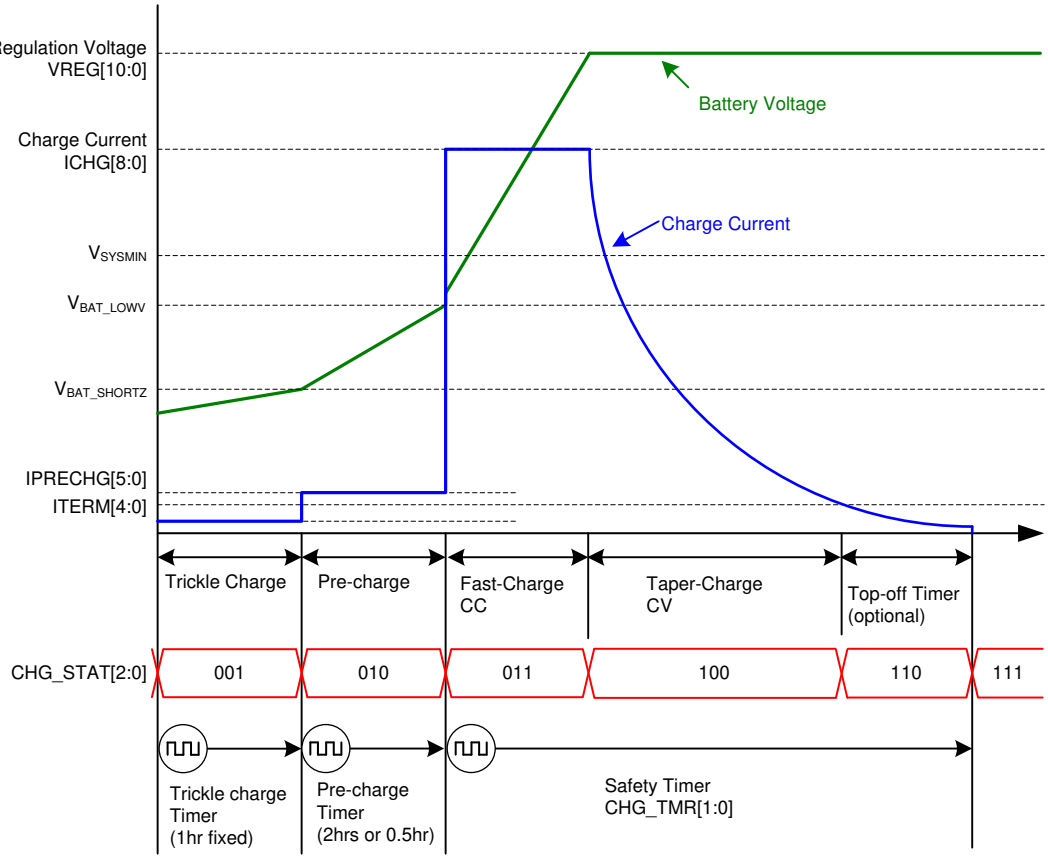

図 8-10. Battery Charging Profile

8.3.9.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter is operated in the battery constant voltage regulation loop and the current is below the termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system and the BATFET can turn on again if the supplement mode is triggered.

When termination is done, the status register CHG_STAT is set to 111 and an $\overline{INT}$ pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current (IINDPM), input voltage (VINDPM) or thermal (TREG) regulation. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charging termination. Writing 0 to EN_TERM when the termination already occurred or in the top-off charging stage does not disable termination, until the next charging cycle has been restarted. If termination is reenabled by setting EN_TERM = 1 during the current charge cycle, the change is applied immediately to the current charging cycle.

At low termination currents (like 40mA to 160mA), due to the comparator offset, the actual termination current may be up to 20%~40% higher than the termination target. In order to compensate for the comparator offset, a programmable top-off timer (default disabled) can be activated after termination is detected. Whlie the top-off timer is running, the device continues to charge the battery in constant voltage mode (BATFET stays on) until the top-off time expires. The top-off timer follows safety timer constraints, such that if the safety timer is suspended, so is the top-off timer. And if the safety timer is doubled, so is the top-off timer. CHG_STAT reports whether the top off timer is active via the 110 code. Once the top-off timer expires, the CHG_STAT register is set to 111 and an $\overline{INT}$ pulse is asserted to the host.

The top-off timer gets reset (set to 0 and counting resumes when appropriate) for any of the following conditions:

1. Charge disable to enable

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2. Termination status low to high
3. REG_RST register bit is set (disables top-off timer)

Once the charger detects termination, the charger reads the top-off timer (TOPOFF_TMR) settings. Programming the top-off timer value after termination has no effect unless a recharge cycle is initiated. The top-off timer only starts to count when the charger's termination criteria are met. If EN_TERM = 0, the charger never terminates charging, so the top-off timer does not start counting, even if it is enabled. An $\overline{INT}$ is asserted to the host when the top-off timer starts counting as well as when the top-off timer expires. All charge cycle related $\overline{INT}$ pulses (including top-off timer $\overline{INT}$ pulse) can be masked by CHG_MASK bit.

8.3.9.4 Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. The user can program the fast charge safety timer through I^2C (CHG_TMR bits). When the fast charge safety timer expires, the fault register CHG_TMR_STAT bit is set to 1, and an $\overline{INT}$ pulse is asserted to the host. The trickle charge timer is fixed 1 hour. The pre-charge safety timer is adjustable 2 hours (POR default) or 0.5 hour. The fast charging timer POR default setting is 12 hours.

The trickle charge, pre-charge and fast charge safety timers can be disabled by setting EN_TRICHG_TMR, EN_PRECHG_TMR or EN_CHG_TMR bit to 0. Each charging safety timer can be enabled anytime regardless of the current charging state. Each timer restarts counting when it is enabled. As soon as each charging stage is initiated, the associated safety timer starts to count, which is illustrated in the battery charging profile chart shown in the section Battery Charging Profile.

During input voltage, current or thermal regulation, the safety timer counts at half-clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half-clock rate feature can be disabled by setting TMR2X_EN = 0. If the host disables the half-clock rate while the charger is already running at half-clock rate, the charger keeps running at the half-clock rate and the half-clock rate is not disabled until the charger exit the voltage, current or thermal regulation.

During faults which disable charging, or supplement mode, the timer is suspended. Since the timer is not counting in this state, the TMR2X_EN bit has no effect. Once the fault goes away, the safety timer resumes. If the charging cycle is stopped and started, the timer resets. The pre-charge safety timer and the trickle charge safety timer follow the same rules as the fast charge safety timer in terms of getting suspended, reset and counting at half-rate when TMR2X_EN is set.

The fast charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold after termination)
2. BAT voltage changes from pre-charge to fast-charge or vice versa (in host-mode or default mode)
3. A change of the value of CHG_TMR[1:0] register bits

The pre-charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle$\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa, pre-charge to fast charge or vice versa (in host-mode or default mode)
3. A change of the value of PRECHG_TMR register bit.

The trickle charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle$\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa (in host-mode or default mode)

8.3.9.5 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitoring.

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8.3.9.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on the TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the VT1-VT5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature T1-T2, JEITA recommends to reduce the charge current to be lower than half of the charge current at normal temperature T2-T3. The charger register bits JEITA_ISETC[1:0] provide the charge current programmability at T1-T2, to be 20%, 40% or 100% of the charge current in the T2-T3 temperature range or charge suspend. At warm temperature T3-T5, JEITA recommends charge voltage less than 4.1V / cell. The charger register bits JEITA_VSET[2:0] provide the charge voltage programmability at T3-T5, to be with a voltage offset less than charge voltage in the T2-T3 temperature range or charge suspend.

Charging termination is still enabled (when EN_TERM = 1) at cool temperature T1-T2 and warm temperature T3-T5. The termination current remains the same in all different temperature ranges. In normal operation, battery charging terminates when the charge current is lower than the termination current, the battery voltage is higher than the battery recharge voltage and the charger is in the battery voltage CV regulation loop. When the temperature enters the T1-T2 or T3-T5 ranges, the charge current may reduce to 20% or 40% of that in the T2-T3 range, which might be lower than the termination current setting. If at this moment, the battery voltage is already higher than the battery recharge voltage and the charger is in the battery voltage CV regulation loop, the charger terminates charge.

In warm T3-T5 temperature range, the battery voltage regulation value become lower than that in the T2-T3 temperature range. If the battery voltage is already very close to the T2-T3 regulation value, the JEITA warm automatic regulation voltage reduction might cause a battery over-voltage (VBAT_OVP) fault.

In cool T1-T2 temperature range or warm T3-T5 temperature range, the charge current is different from that at the normal T2-T3 temperature range , the safety timer must be adjusted accordingly. The safety timer is suspended when the charge is suspended, and runs at half of the clock rate when the charge current is reduced to 20% or 40%, but stays the same when the charge current is unchanged.

One typical JEITA charging values are shown as the figure below, in which the blue real line is the default setting and the red dash line is the programmable options.

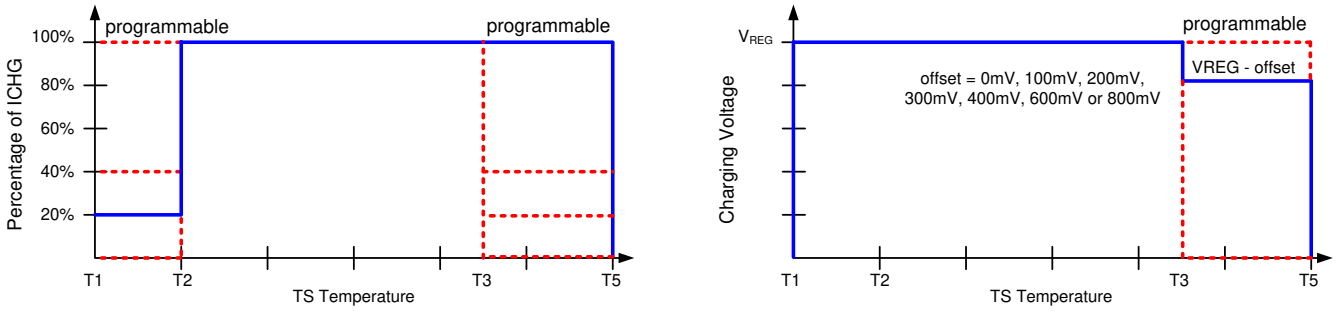

図 8-11. TS Charging Values

The NTC monitoring on the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good for charging and OTG modes. The TS_STAT including TS_COLD_STAT, TS_COOL_STAT, TS_WARM_STAT and TS_HOT_STAT, always report 000 with TS_IGNORE = 1.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information. When the battery temperature jumps from one temperature range to the other one, the associated TS status bits are updated accordingly. The TS flag bits are set for the temperature range for which the TS voltage is reporting, and an $\overline{INT}$ pulse is asserted to alert the host if TS_MASK is low. The FLAG and $\overline{INT}$ pulse can be individually

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masked by properly setting the associated mask bit, to prevent the $\overline{INT}$ pulse from alerting the host of battery temperature range changes.

The typical TS resistor network is illustrated in the figure below.

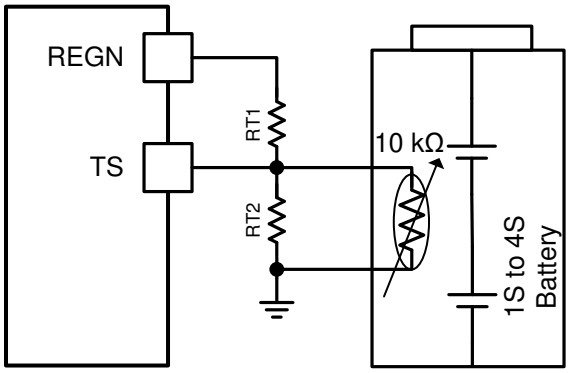

図 8-12. TS Resistor Network

Assuming a 103AT NTC thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (2)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (3)$$

where VT# are the percentages of V(REGN) per the electrical specifications table. The BQ25672 provides the comparators with fixed thresholds for VT1 x V(REGN) and VT5 x V(REGN), and comparators with programmable thresholds for VT2 x V(REGN) and VT3 x V(REGN). The thresholds for VT2 x V(REGN) and VT3 x V(REGN) are controlled by TS_COOL[1:0] and TS_WARM[1:0]. This programmability gives more flexibility for the configuration of the JEITA profile. Select T1=0°C and T5=60°C for Li-ion or Li-polymer battery, the RT1 and RT2 are calculated to be 5.24KΩ and 30.31KΩ respectively.

8.3.9.5.2 Cold/Hot Temperature Window in OTG Mode

For battery protection during OTG mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When RT1 is 5.24 KΩ and RT2 is 31.31 KΩ, TBCOLD default is -10°C and TBHOT default is 60°C. When the temperature is outside of this range, OTG mode is suspended, the converter stops switching. The charger waits in OTG mode (EN_OTG = 1). In addition, the VBUS_STAT bits are set to 000 and the corresponding TS_COLD_STAT or TS_HOT_STAT is reported. Once temperature returns to the normal temperature range, OTG mode is recovered and TS stauts bit is cleared. During TS fault, REGN still stays on.

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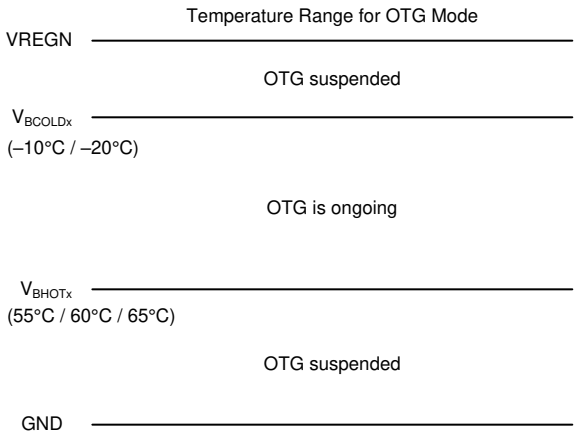

図 8-13. TS Pin Thermistor Sense Threshold in OTG Mode

8.3.10 Integrated 16-Bit ADC for Monitoring

The integrated 16-bit ADC in the device allows the user to get critical system information for optimizing the behavior of the charger. The ADC control is through the ADC Control register. The ADC_EN bit provides the ability to enable and disable the ADC in order to conserve power dissipation. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a 1-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion. The ADC_AVG bit enables or disables (default) averaging. ADC_AVG_INIT starts average using the existing (default) or using a new ADC value.

To enable the ADC, the ADC_EN bit must be set to 1. The ADC is allowed to operate if either the VAC > 3.4 V or VBUS > 3.4 V or VBAT > 2.9 V is valid. If ADC_EN is set to 1 before VAC1/VAC2, VBUS or VBAT reaches its valid threshold, then the ADC conversion is postponed until one of the power supplies reaches the threshold. If the charger is in HIZ mode, the ADC still can be enabled by setting ADC_EN = 1. At battery only condition, if the TS_ADC channel is enable, the ADC only works when battery voltage is higher than 3.2V, otherwise, the ADC works when the battery voltage is higher than 2.9V.

The ADC_SAMPLE bits control the ADC sample speed, with conversion times of t_{ADC_CONV}. If the host changes the sample speed in the middle of an ADC conversion, the ADC conversion stops the channel being converted, and that channel is reconverted at the new rate. At that point, some of the ADC register values might have been converted with one sample rate and others with a different sample rate.

By default, all ADC channels are enabled with 1-shot or continuous conversion mode unless the channel is disabled in the ADC_Function_Disable_0 or ADC_Function_Disable_1 register. If an ADC channel is disabled by setting the corresponding register bit, then the value in that register is from the last valid ADC conversion or the default POR value (all zeros if no conversions have been taken place). If an ADC channel is disabled in the middle of an ADC measurement cycle, the device finishes the conversion of that channel, but not convert the channel at the next conversion cycle. Even though no conversion takes place when all ADC channels are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC_Function_Disable_0 or ADC_Function_Disable_1 register is set to 0.

The ADC_DONE_STAT and ADC_DONE_FLAG bits are set when a conversion is complete in 1-shot mode only. This event produces an $\overline{INT}$ pulse, which can be masked with ADC_DONE_MASK. During continuous conversion mode, the ADC_DONE_STAT and ADC_DONE_FLAG bits have no meaning and remain 0.

ADC conversion operates independently of the faults present in the device. ADC conversion continues even after a fault has occurred (such as one that causes the power stage to be disabled) and the host must set ADC_EN = 0 to disable the ADC. ADC conversion is interrupted upon adapter plug-in and resumes after Input Source Type Detection default VINDPM setting are complete. ADC readings are only valid for DC states and not for transients.

Enabling ADC does not require to bring up REGN, however, when the ADC TS channel is enabled, the charger will turn on the REGN to bias the TS pin. For the ICHG channel, the ADC is able to read the battery pre-charge

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and fast charge current in forward charging mode when the adapter is present. It also can read the battery discharging current in battery only mode, OTG mode . When the charger is in trickle charge, supplement mode or charge disabled, the ICHG ADC reading is zero. In battery only mode, the battery current sensing amplifier (CSA) default turns off to minimize the quiescent current. Setting EN_IBAT = 1 is necessary to enable the CSA so that the ADC can read back the battery current information.

If the host wants to exit the ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot in order to force the ADC to stop at the end of a complete cycle of conversions
2. Disable all ADC conversion channels so that the ADC stops at the end of the current measurement.

8.3.11 Status Outputs (STAT, and $\overline{\text{INT}}$)

8.3.11.1 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled via the DIS_STAT bit.

表 8-7. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge and charging in top-off timer)	LOW
Charging complete	HIGH
HIZ mode, charge disable	HIGH
Battery only mode and OTG mode	HIGH
Charge suspend (A fault condition which disable charging)	Blinking at 1 Hz

8.3.11.2 Interrupt to Host ($\overline{\text{INT}}$)

In some applications, the host does not always monitor charger operation. The $\overline{\text{INT}}$ pin notifies the system host on the device operation. By default, the following events generate an active-low, 256μs $\overline{\text{INT}}$ pulse.

1. Good input source detected
   - V_{VBUS} < V_{VBUS_OVP} threshold
   - V_{VBUS} > $V_{POORSRC}$ (typical 3.4 V) when $I_{POORSRC}$ (typical 30 mA) current is applied (not a poor source)
2. VBUS_STAT changes state (VBUS_STAT any bit change)
3. Good input source removed
4. Entering IINDPM regulation
5. Entering VINDPM regulation
6. Entering IC junction temperature regulation (TREG)
7. I^2C Watchdog timer expired
   - At initial power up, this $\overline{\text{INT}}$ gets asserted to signal I^2C is ready for communication
8. Charger status changes state (CHRG_STAT value change), including Charge Complete
9. TS_STAT changes state (TS_STAT any bit change)
10. VBUS over-voltage detected (VBUS_OVP)
11. VAC over-voltage detected (VAC_OVP for VAC1 or VAC2)
12. Junction temperature shutdown (TSHUT)
13. Battery over-voltage detected (BATOVP)
14. System over-voltage detected (VSYS_OVP)
15. IBUS over-current detected (IBUS_OCP)
16. IBAT over-current detected (IBAT_OCP)
17. Charge safety timer expired, including trickle charge and pre-charge and fast charge safety timer expired
18. A rising edge on any of the other *_STAT bits

Each one of these $\overline{\text{INT}}$ sources can be masked off to prevent $\overline{\text{INT}}$ pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each $\overline{\text{INT}}$ source
- The FLAG bit holds information on which source produced an $\overline{\text{INT}}$, regardless of the *current status*
- The MASK bit is used to prevent the device from sending out $\overline{\text{INT}}$ for each particular event

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When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an $\overline{INT}$ pulse and keeps track of which source generated the $\overline{INT}$ via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

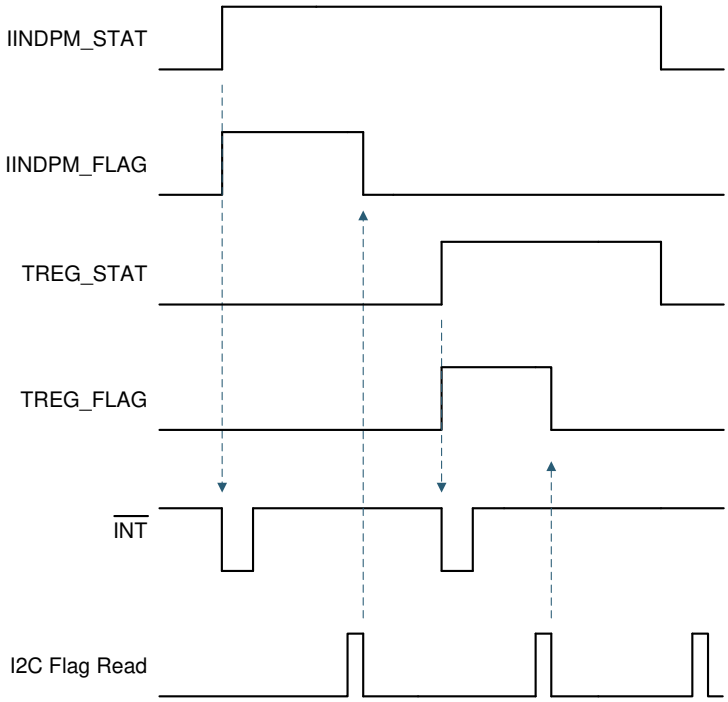

図 8-14. $\overline{INT}$ Generation Behavior Example

8.3.12 Ship FET Control

The charger provides an N-FET driving pin (SDRV) to control an external ship FET. The SDRV pin is the output of a charge pump that provides 100 nA typical drive current to drive the ship FET gate to typically 5-V above the battery voltage. When this ship FET is off, it removes leakage current from the battery to the system. The ship FET is controlled by the SDRV_CTRL[1:0] register bits, to support the shutdown mode, ship mode and the system power reset.

- **IDLE Mode** when SDRV_CTRL[1:0] = 00, POR default. The external ship FET is fully on, I^2C is enabled. The internal BATFET status is determined by the charging status. This mode is valid with adapter present, during forward charging, in OTG mode or in the battery only condition.
- **Shutdown Mode** when SDRV_CTRL[1:0] = 01. The ship FET turns off. The I^2C is disabled. The charger is totally shutdown and can only be woken up by an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.
- **Ship Mode** when SDRV_CTRL[1:0] = 10. The ship FET turns off. The I^2C is still enabled. The charger can be woken up by setting SDRV_CTRL[1:0] back to 00, or pulling the $\overline{QON}$ pin low, or an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.
- **System Power Reset** when SDRV_CTRL[1:0] = 11. The ship FET is turned off for typical 350ms to reset the system power (converter goes to HIZ mode if VBUS is high), then the ship FET is fully turned on again. The BATFET keeps the status unchanged during the system power reset. After the reset is done, SDRV_CTRL[1:0] goes back to 00.

When the host changes SDRV_CTRL[1:0] from 00 to the other values, the charger turns off the ship FET immediately or delays by t_{SM_DLY} as configured by SDRV_DLY bit.

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8.3.12.1 Shutdown Mode

To further reduce battery leakage current, the host can shut down the charger by setting the register bits SDRV_CTRL[1:0] to 01. In this mode, the I^2C is disabled and the charger is totally shut down. The device can only be woken up by plugging in an adapter.

After the SDRV_CTRL[1:0] is set to 01, the external ship FET turns off either immediately or after waiting for 10s as configured by SDRV_DLY register bit. When VBUS is high because of an adapter being present or the OTG mode being enable, SDRV_CTRL[1:0] will be reset to 00 if the host writes it to 01.

When the device exits shutdown mode, the SDRV_CTRL bits are reset to the POR default values (00).

8.3.12.2 Ship Mode

To extend battery life and minimize the system power loss when system is powered off during idle, shipping or storage, the device can turn off BATFET and external ship FET to minimize the battery leakage current. The ship mode is enabled when the host sets SDRV_CTRL[1:0] to 10. The I^2C is still enabled, but the charger system clock slows down to minimize the device quiescent current.

After the SDRV_CTRL[1:0] is set to 10, the external ship FET is turned off either immediately or after waiting 10 seconds as configured by SDRV_DLY register bit. When VBUS is high because of an adapter being present or OTG mode being enabled, SDRV_CTRL[1:0] automatically resets to 00 if the host writes it to 10.

The following events will cause an exit from ship mode:

- Plug in an adapter
- Set SDRV_CTRL[1:0] = 00
- Set REG_RST = 1, to reset all the registers including SDRV_CTRL bits back to default (00)
- A logic low of t_{SM_EXIT} (typical 1s or 15ms programmed by WKUP_DLY bit) duration on $\overline{QON}$ pin

The charger exits ship mode by turning on the ship FET and internal BATFET to reconnect the battery to the system and resetting SDRV_CTRL bits to their POR default value (00).

8.3.12.3 System Power Reset

The host can reset the system power by:

- Set the register bits SDRV_CTRL[1:0] to 11
- A logic low of t_{RST} (typical 10s) duration on $\overline{QON}$ pin

When the system power reset is enabled, the device turns off the ship FET for t_{RST_SFET} (typical 350ms) and also sets the charger in HIZ mode if VBUS is high. After the t_{RST_SFET} completes, the device then turns on the ship FET and disables the charger HIZ mode. While the SFET is off, the charger applies a 30mA (typical) sink current on SYS to discharge system voltage.

Regardless of whether the charger is at battery only condition or in the forward charging mode with adapter present, the charger resets the system power when the SDRV_CTRL[1:0] bits are set to 11 or the $\overline{QON}$ pin is pulled low for t_{RST} duration.

8.3.13 Protections

8.3.13.1 Voltage and Current Monitoring

The device closely monitors the input, system and battery voltage and current, as well as internal FET currents for safe converter operation. It provides the following protection faults :

- VAC Over-voltage Protection (VAC_OVP)
- VBUS Over-voltage Protection (VBUS_OVP)
- VBUS Under-voltage Protection (POORSRC)
- System Over-voltage Protection (VSYS_OVP)
- System Short Protection (VSYS_SHORT)
- Battery Over-voltage Protection (VBAT_OVP)
- Battery Over-current Protection (IBAT_OCP)
- Input Over-current Protection (IBUS_OCP)

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- OTG Over-voltage Protection (OTG_OVP)
- OTG Under-voltage Protection (OTG_UVP)

8.3.13.1.1 VAC Over-voltage Protection (VAC_OVP)

The charger has a programmable V_{VAC_OVP} threshold. When the VAC1 or VAC2 voltage is higher than V_{VAC_OVP} threshold per I2C register field, the corresponding ACDRV pin turns off the ACFET-RBFET. An /INT pulse is asserted to alert the host, if the related MASK is low, and the related VACx_OVP_STAT and VAC_OVP_FLAG report the fault. The charger automatically changes to the valid VAC input if available The ACDRV pin automatically turns the ACFET-RBFET on again when the over-voltage condition goes away.

8.3.13.1.2 VBUS Over-voltage Protection (VBUS_OVP)

When the VBUS voltage is higher than V_{VBUS_OVP} (typical 26 V), the converter stops switching immediately to protect the internal power MOSFETs. As the SYS voltage falls below the battery voltage, the BATFET is turned on to supplement the system load. During VBUS over-voltage, an $\overline{INT}$ pulse is asserted to alert the host, if the VBUS_OVP_MASK is low, the VBUS_OVP_STAT and VBUS_OV_FLAG registers report the fault. The device automatically starts switching again when the VBUS voltage drops below the threshold.

8.3.13.1.3 VBUS Under-voltage Protection (POORSRC)

At power up, the charger pulls $I_{POORSRC}$ from the input source. If the VBUS voltage falls below $V_{POORSRC}$, the charger considers the input voltage as being under-voltage and stops switching. The charger issues an $\overline{INT}$ pulse is asserted to alert the host if the PG_MASK is low and the POORSRC_FLAG, PG_FLAG and PG STATUS registers report the fault. The charger repeatedly tests for poor source again after 7 minutes typical until a valid source is attached.

8.3.13.1.4 System Over-voltage Protection (VSYS_OVP)

If the system voltage rises higher than VSYS_OVP threshold, the converter stops switching to protect the power MOSFETs. A /INT pulse is asserted to alert the host if VSYS_OVP_MASK is low and the VSYS_OVP_STAT and VSYS_OVP_FLAG registers report the fault. Normal switching resumes when the system voltage returns to its regulation point.

8.3.13.1.5 System Short Protection (VSYS_SHORT)

When VSYS drops below VSYS_SHORT (2.2V typical), the charger limits the converter output current to less than 1 A. An /INT pulse is asserted to alert the host if VSYS_SHORT_MASK is low and the VSYS_SHORT_STAT and VSYS_SHORT_FLAG registers report the fault.

8.3.13.1.6 Battery Over-voltage Protection (VBAT_OVP)

When the battery voltage is detected to be higher than 104% typical of the battery charging regulation voltage, the charger turns off the converter to prevent the battery voltage from further increasing. When the battery voltage drops below 102% typical of the battery charging regulation voltage, the converter automatically restarts. The system load is supplied by battery through battery FET when the converter is disabled. A /INT pulse is asserted to alert the host if the VBAT_OVP_MASK is low and the VBAT_OVP_STAT and VBAT_OVP_FLAG register bits report the fault.

8.3.13.1.7 Battery Over-current Protection (IBAT_OCP)

Battery over-current protection is available when external ship FET (SFET) is assembled, SFET_PRESENT bit is set to 1, and EN_BATOC bit is set to 1. When discharge current exceeds IBAT_OCP, the SFET turns off to stop the discharge current. Regardless of the EN_BATOC bit setting, when the battery discharging current becomes higher than IBATOC, an /INT pulse is asserted to alert the host if IBAT_OCP_MASK is low and the IBAT_OCP_STAT and IBAT_OCP_FLAG register bits report the fault.

8.3.13.1.8 Input Over-current Protection (IBUS_OCP)

When EN_IBUS_OCP=1, the charger monitors the input current in forward charging mode in order to provide IBUS over current protection. If the input current exceeds the IBUS over current threshold IBUS_OCP (typical 8A), the charger disables the converter by setting the EN_HIZ bit to 1. In addition, the charger sets DIS_ACDRV=1 in order to disable both ACDRV1 and ACDRV2. The battery FET turns on to supplement the

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system load as needed. The host must set EN_HIZ and DIS_ACDRV bits to 0 in order to restart the converter. Alternatively, removing and replacing the adapter resets the EN_HIZ bit and the DIS_ACDRV bit to 0. When EN_IBUS_OCP=0, IBUS over current protection is disabled. Regardless of the EN_ IBUS_OCP bit setting, when the IBUS input current becomes higher than IBUS_OCP, an /INT pulse is asserted to alert the host if IBUS_OCP_MASK is low, the IBUS_OCP_STAT and IBUS_OCP_FLAG register bits report the fault.

8.3.13.1.9 OTG Over-voltage Protection (OTG_OVP)

When the VBUS voltage rises above VOTG_OVP rising threshold, the converter stops switching in the next switching cycle in order to protect the power MOSFETs. The converter resumes switching when the VBUS voltage falls below the VOTG_OVP falling threshold. When OTG_OVP is detected, a /INT pulse is asserted to alert the host if OTG_OVP_MASK is low and the VOTG_OVP_STAT and VOTG_OVP_FLAG fault registers report the fault.

8.3.13.1.10 OTG Under-voltage Protection (OTG_UVP)

After the converter turns on if the VBUS voltage is lower than VOTG_UVP threshold, the charger shuts down for 500ms and retry to turn on. An /INT pulse is asserted to alert the host if OTG_UVP_MASK is low and the OTG_UVP_FLAG register reports the fault.

8.3.13.2 Thermal Regulation and Thermal Shutdown

The device monitors its internal junction temperature (T_J) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces the charge current or OTG output current to maintain the junction temperature at the thermal regulation limit. A wide thermal regulation range from 60°C to 120°C allows optimization of the system thermal performance. During thermal regulation, the actual charging current is usually below the programmed value in the ICHG registers. Therefore, termination is disabled, the fast charging safety timer runs at half the clock rate, the status register TREG_STAT bit goes high, TREG_FLAG bit is set to 1, and an $\overline{INT}$ is asserted to alert host unless TREG_MASK is set to 1.

Additionally, the device has thermal shutdown to turn off the converter when the IC junction temperature exceeds the TSHUT threshold. The fault register bits TSHUT_STAT and TSHUT_FLAG are set and an $\overline{INT}$ pulse is asserted to the host, unless TSHUT_MASK is set to 1. The BATFET and the converter resumes normal operation when the IC die temperature decreases lower than TSHUT threshold by T_{SHUT_HYS}.

8.3.14 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as controllers or targets when performing data transfers. A controller is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The device operates as a target device with 7-bit address 0x6B, receiving control inputs from the controller device like micro-controller or digital signal processor through REG00 – REG25. Register read beyond REG25 (0x25), returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits/s), and fast mode (up to 400 kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

8.3.14.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

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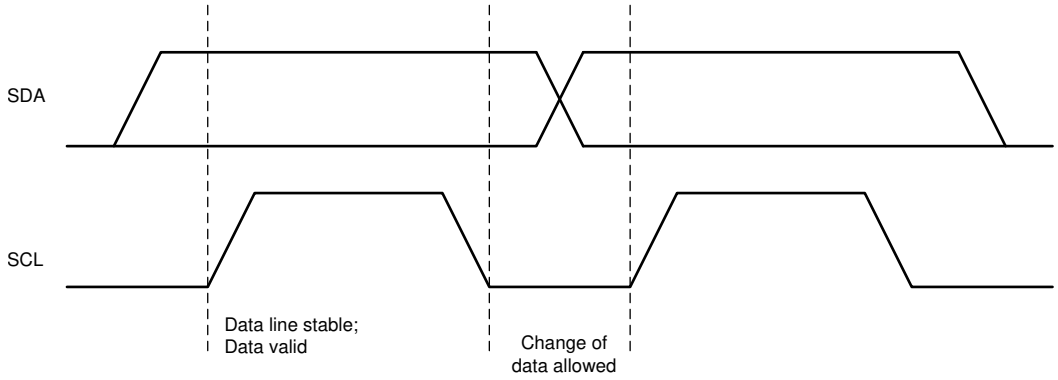

図 8-15. Bit Transfers on the I²C Bus

8.3.14.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

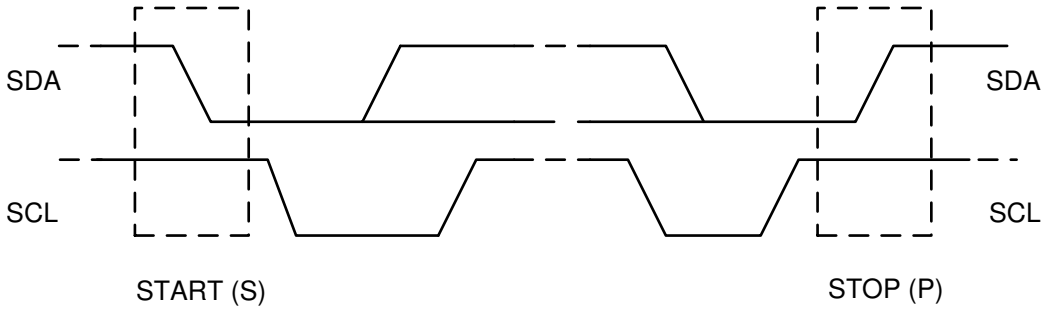

図 8-16. START and STOP Conditions on the I²C Bus

8.3.14.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

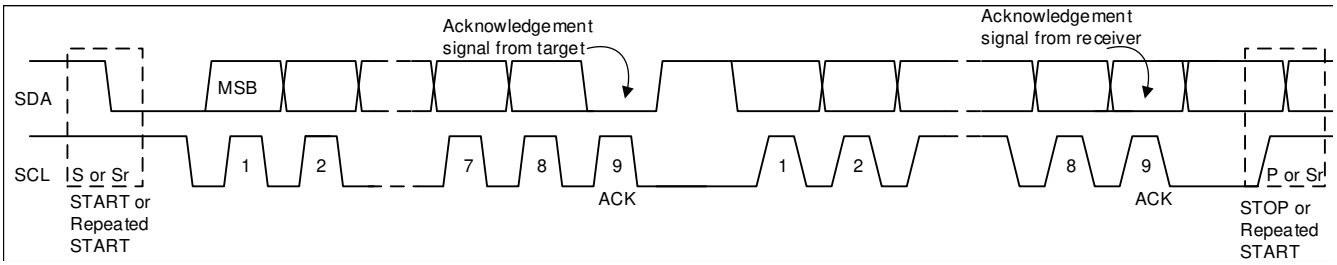

図 8-17. Data Transfer on the I²C Bus

8.3.14.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.14.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The 7-bit address is defined as 1101 011' (0x6B). The address bit arrangement is shown below.

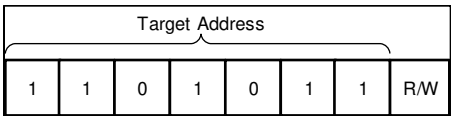

図 8-18. 7-Bit Addressing (0x6B)

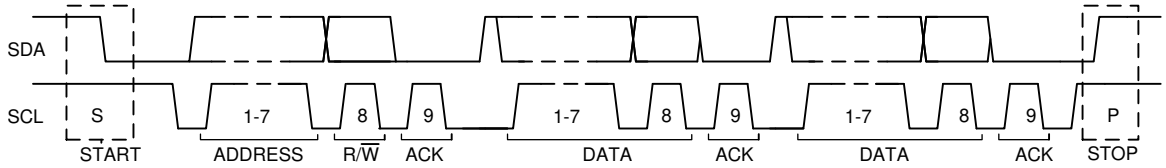

図 8-19. Complete Data Transfer on the I²C Bus

8.3.14.6 Single Write and Read

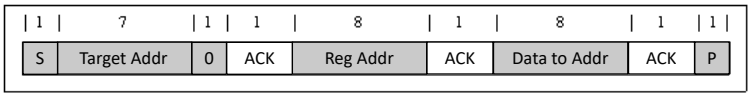

図 8-20. Single Write

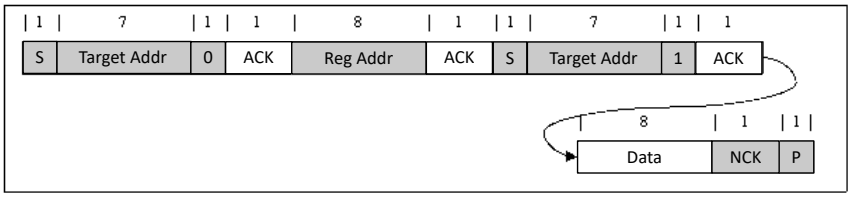

図 8-21. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

8.3.14.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire regiser map may be read in a single operation with a 49-byte read that starts at register address 0x0.

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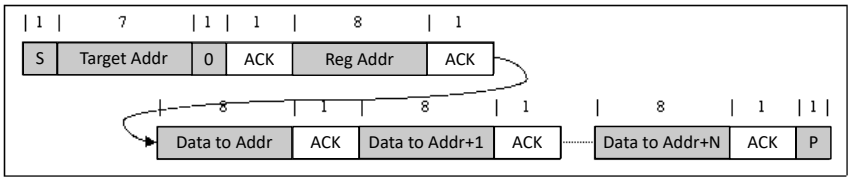

図 8-22. Multi-Write

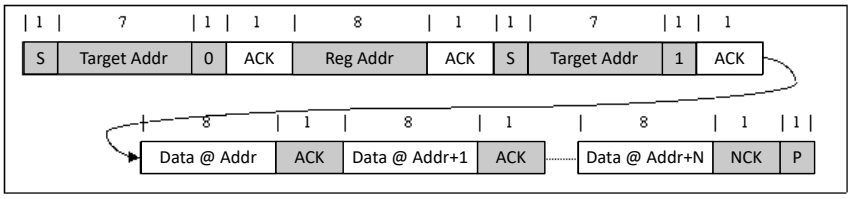

図 8-23. Multi-Read

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and all registers are reset to default values except the ones described as detailed in the Register Map section. The Watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

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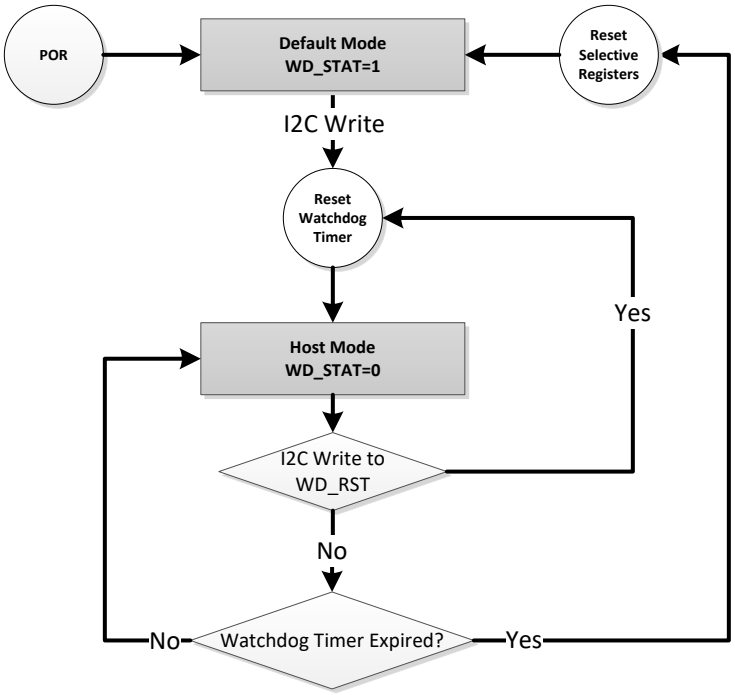

図 8-24. Watchdog Timer Flow Chart

8.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

The register reset by the REG_RST bit will not initiate the ACFET-RBFET detection, which is only done at the charger first time POR. It will not repeat the open-circuit adapter measurements for the default VINDPM setting, which in only done when an adapter is plugged in. In addition, if the charger is in the process of forced ICO or the forced open-circuit adapter measurements, set the REG_RST to 1 will terminate all of these processes, because reset the register to default values will set FORCE_ICO and FORCE_VINDPM_DET bits to 0.

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8.5 Register Map

8.5.1 I2C Registers

表 8-8 lists the I2C registers. All register offset addresses not listed in 表 8-8 should be considered as reserved locations and the register contents should not be modified.

表 8-8. I2C Registers

Offset	Acronym	Register Name	Section
0h	REG00_Minimal_System_Voltage	Minimal System Voltage	セクション 8.5.1.1
1h	REG01_Charge_Voltage_Limit	Charge Voltage Limit	セクション 8.5.1.2
3h	REG03_Charge_Current_Limit	Charge Current Limit	セクション 8.5.1.3
5h	REG05_Input_Voltage_Limit	Input Voltage Limit	セクション 8.5.1.4
6h	REG06_Input_Current_Limit	Input Current Limit	セクション 8.5.1.5
8h	REG08_Precharge_Control	Precharge Control	セクション 8.5.1.6
9h	REG09_Termination_Control	Termination Control	セクション 8.5.1.7
Ah	REG0A_Re-charge_Control	Re-charge Control	セクション 8.5.1.8
Bh	REG0B_VOTG_regulation	VOTG regulation	セクション 8.5.1.9
Dh	REG0D_IOTG_regulation	IOTG regulation	セクション 8.5.1.10
Eh	REG0E_Timer_Control	Timer Control	セクション 8.5.1.11
Fh	REG0F_Charger_Control_0	Charger Control 0	セクション 8.5.1.12
10h	REG10_Charger_Control_1	Charger Control 1	セクション 8.5.1.13
11h	REG11_Charger_Control_2	Charger Control 2	セクション 8.5.1.14
12h	REG12_Charger_Control_3	Charger Control 3	セクション 8.5.1.15
13h	REG13_Charger_Control_4	Charger Control 4	セクション 8.5.1.16
14h	REG14_Charger_Control_5	Charger Control 5	セクション 8.5.1.17
15h	REG15_MPPT_Control	MPPT Control	セクション 8.5.1.18
16h	REG16_Temperature_Control	Temperature Control	セクション 8.5.1.19
17h	REG17_NTC_Control_0	NTC Control 0	セクション 8.5.1.20
18h	REG18_NTC_Control_1	NTC Control 1	セクション 8.5.1.21
19h	REG19_ICO_Current_Limit	ICO Current Limit	セクション 8.5.1.22
1Bh	REG1B_Charger_Status_0	Charger Status 0	セクション 8.5.1.23
1Ch	REG1C_Charger_Status_1	Charger Status 1	セクション 8.5.1.24
1Dh	REG1D_Charger_Status_2	Charger Status 2	セクション 8.5.1.25
1Eh	REG1E_Charger_Status_3	Charger Status 3	セクション 8.5.1.26
1Fh	REG1F_Charger_Status_4	Charger Status 4	セクション 8.5.1.27
20h	REG20_FAULT_Status_0	FAULT Status 0	セクション 8.5.1.28
21h	REG21_FAULT_Status_1	FAULT Status 1	セクション 8.5.1.29
22h	REG22_Charger_Flag_0	Charger Flag 0	セクション 8.5.1.30
23h	REG23_Charger_Flag_1	Charger Flag 1	セクション 8.5.1.31
24h	REG24_Charger_Flag_2	Charger Flag 2	セクション 8.5.1.32
25h	REG25_Charger_Flag_3	Charger Flag 3	セクション 8.5.1.33
26h	REG26_FAULT_Flag_0	FAULT Flag 0	セクション 8.5.1.34
27h	REG27_FAULT_Flag_1	FAULT Flag 1	セクション 8.5.1.35
28h	REG28_Charger_Mask_0	Charger Mask 0	セクション 8.5.1.36
29h	REG29_Charger_Mask_1	Charger Mask 1	セクション 8.5.1.37
2Ah	REG2A_Charger_Mask_2	Charger Mask 2	セクション 8.5.1.38
2Bh	REG2B_Charger_Mask_3	Charger Mask 3	セクション 8.5.1.39
2Ch	REG2C_FAULT_Mask_0	FAULT Mask 0	セクション 8.5.1.40

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表 8-8. I2C Registers (continued)

Offset	Acronym	Register Name	Section
2Dh	REG2D_FAULT_Mask_1	FAULT Mask 1	セクション 8.5.1.41
2Eh	REG2E_ADC_Control	ADC Control	セクション 8.5.1.42
2Fh	REG2F_ADC_Function_Disable_0	ADC Function Disable 0	セクション 8.5.1.43
30h	REG30_ADC_Function_Disable_1	ADC Function Disable 1	セクション 8.5.1.44
31h	REG31_IBUS_ADC	IBUS ADC	セクション 8.5.1.45
33h	REG33_IBAT_ADC	IBAT ADC	セクション 8.5.1.46
35h	REG35_VBUS_ADC	VBUS ADC	セクション 8.5.1.47
37h	REG37_VAC1_ADC	VAC1 ADC	セクション 8.5.1.48
39h	REG39_VAC2_ADC	VAC2 ADC	セクション 8.5.1.49
3Bh	REG3B_VBAT_ADC	VBAT ADC	セクション 8.5.1.50
3Dh	REG3D_VSYS_ADC	VSYS ADC	セクション 8.5.1.51
3Fh	REG3F_TS_ADC	TS ADC	セクション 8.5.1.52
41h	REG41_TDIE_ADC	TDIE_ADC	セクション 8.5.1.53
43h	REG43_D+_ADC	D+ ADC	セクション 8.5.1.54
45h	REG45_D-_ADC	D- ADC	セクション 8.5.1.55
47h	REG47_DPDM_Driver	DPDM Driver	セクション 8.5.1.56
48h	REG48_Part_Information	Part Information	セクション 8.5.1.57

Complex bit access types are encoded to fit into small table cells. The following table shows the codes that are used for access types in this section.

表 8-9. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Others		
Range		The register bits are only valid in this defined range.
Clamped Low		Any write on the register lower than the minimal value of the valid range, will be ignored by the charger
Clamped High		Any write on the register higher than the maximum value of the valid range, will be ignored by the charger

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8.5.1.1 REG00_Minimal_System_Voltage Register (Offset = 0h) [reset = X]

REG00_Minimal_System_Voltage is shown in 図 8-25 and described in 表 8-10.

Return to the 表 8-8.

Minimal System Voltage

図 8-25. REG00_Minimal_System_Voltage Register

7	6	5	4	3	2	1	0
RESERVED		VSYSMIN_5:0					
R/W-0h		R/W-X					

表 8-10. REG00_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	RESERVED	R/W	0h		RESERVED
5-0	VSYSMIN_5:0	R/W	X	Reset by: REG_RST	Minimal System Voltage: During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power on VSYSMIN list below: 1s: 3.5V 2s: 7V 3s: 9V 4s: 12V Type : RW Range : 2500mV-16000mV Fixed Offset : 2500mV Bit Step Size : 250mV Clamped High

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8.5.1.2 REG01_Charge_Voltage_Limit Register (Offset = 1h) [reset = X]

REG01_Charge_Voltage_Limit is shown in 図 8-26 and described in 表 8-11.

Return to the 表 8-8.

Charge Voltage Limit

図 8-26. REG01_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED					VREG_10:0		
R-0h					R/W-X		
7	6	5	4	3	2	1	0
VREG_10:0							
R/W-X							

表 8-11. REG01_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-11	RESERVED	R	0h		RESERVED
10-0	VREG_10:0	R/W	X	Reset by: REG_RST	Battery Voltage Limit: During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery voltage regulation limit: 1s: 4.2V 2s: 8.4V 3s: 12.6V 4s: 16.8V Type : RW Range : 3000mV-18800mV Fixed Offset : 0mV Bit Step Size : 10mV Clamped Low

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8.5.1.3 REG03_Charge_Current_Limit Register (Offset = 3h) [reset = X]

REG03_Charge_Current_Limit is shown in 図 8-27 and described in 表 8-12.

Return to the 表 8-8.

Charge Current Limit

図 8-27. REG03_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							ICHG_8:0
R-0h							R/W-64h
7	6	5	4	3	2	1	0
ICHG_8:0							
R/W-64h							

表 8-12. REG03_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-9	RESERVED	R	0h		RESERVED
8-0	ICHG_8:0	R/W	64h	Reset by: WATCHDOG REG_RST	Charge Current Limit During POR, the device reads the resistance connected to PROG pin, to identify the default battery cell count and determine the default power-on battery charging current: POR: 1A Type : RW Range : 50mA-3000mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

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8.5.1.4 REG05_Input_Voltage_Limit Register (Offset = 5h) [reset = 24h]

REG05_Input_Voltage_Limit is shown in 図 8-28 and described in 表 8-13.

Return to the 表 8-8.

Input Voltage Limit

図 8-28. REG05_Input_Voltage_Limit Register

7	6	5	4	3	2	1	0
VINDPM_7:0							
R/W-24h							

表 8-13. REG05_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VINDPM_7:0	R/W	24h	Absolute VINDPM Threshold VINDPM register is reset to 3600mV upon adapter unplugged and it is set to the value based on the VBUS measurement when the adapter plugs in. It is not reset by the REG_RST and the WATCHDOG Type : RW POR: 3600mV (24h) Range : 3600mV-22000mV Fixed Offset : 0mV Bit Step Size : 100mV Clamped Low

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8.5.1.5 REG06_Input_Current_Limit Register (Offset = 6h) [reset = 12Ch]

REG06_Input_Current_Limit is shown in 図 8-29 and described in 表 8-14.

Return to the 表 8-8.

Input Current Limit

図 8-29. REG06_Input_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							IINDPM_8:0
R-0h							R/W-12Ch
7	6	5	4	3	2	1	0
IINDPM_8:0							
R/W-12Ch							

表 8-14. REG06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-9	RESERVED	R	0h		RESERVED
8-0	IINDPM_8:0	R/W	12Ch	Reset by: REG_RST	Based on D+/D- detection results: USB SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Adjustable High Voltage DCP = 1.5A Unknown Adapter = 3A Non-Standard Adapter = 1A/2A/2.1A/2.4A Type : RW POR: 3000mA (12Ch) Range : 100mA-3300mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

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8.5.1.6 REG08_Precharge_Control Register (Offset = 8h) [reset = C3h]

REG08_Precharge_Control is shown in 図 8-30 and described in 表 8-15.

Return to the 表 8-8.

Precharge Control

図 8-30. REG08_Precharge_Control Register

7	6	5	4	3	2	1	0
VBAT_LOWV_1:0		IPRECHG_5:0					
R/W-3h		R/W-3h					

表 8-15. REG08_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	VBAT_LOWV_1:0	R/W	3h	Reset by: REG_RST	Battery voltage thresholds for the transition from precharge to fast charge, which is defined as a ratio of battery regulation limit (VREG) Type : RW POR: 11b 0h = 15%*VREG 1h = 62.2%*VREG 2h = 66.7%*VREG 3h = 71.4%*VREG
5-0	IPRECHG_5:0	R/W	3h	Reset by: WATCHDOG REG_RST	Precharge current limit Type : RW POR: 120mA (3h) Range : 40mA-2000mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

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8.5.1.7 REG09_Termination_Control Register (Offset = 9h) [reset = 5h]

REG09_Termination_Control is shown in 図 8-31 and described in 表 8-16.

Return to the 表 8-8.

Termination Control

図 8-31. REG09_Termination_Control Register

7	6	5	4	3	2	1	0
RESERVED	REG_RST	RESERVED	ITERM_4:0				
R-0h	R/W-0h	R-0h	R/W-5h				

表 8-16. REG09_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		RESERVED
6	REG_RST	R/W	0h		Reset registers to default values and reset timer Type : RW POR: 0b 0h = Not reset 1h = Reset
5	STOP_WD_CHG	RW	0h		Defines whether a watchdog timer expiration will disable charging Type: RW 0h = WD timer expiration keeps existing EN_CHG setting (default) 1h = WD timer expiration sets EN_CHG=0
4-0	ITERM_4:0	R/W	5h	Reset by: WATCHDOG REG_RST	Termination current Type : RW POR: 200mA (5h) Range : 40mA-1000mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

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8.5.1.8 REG0A_Re-charge_Control Register (Offset = Ah) [reset = X]

REG0A_Re-charge_Control is shown in 図 8-32 and described in 表 8-17.

Return to the 表 8-8.

Re-charge Control

図 8-32. REG0A_Re-charge_Control Register

7	6	5	4	3	2	1	0
CELL_1:0		TRECHG_1:0		VRECHG_3:0			
R/W-X		R/W-2h		R/W-3h			

表 8-17. REG0A_Re-charge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	CELL_1:0	R/W	X		At POR, the charger reads the PROG pin resistance to determine the battery cell count and update this CELL bits accordingly. Type : RW 0h = 1s 1h = 2s 2h = 3s 3h = 4s
5-4	TRECHG_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Battery recharge deglich time Type : RW POR: 10b 0h = 64ms 1h = 256ms 2h = 1024ms (default) 3h = 2048ms
3-0	VRECHG_3:0	R/W	3h	Reset by: WATCHDOG REG_RST	Battery Recharge Threshold Offset (Below VREG) Type : RW POR: 200mV (3h) Range : 50mV-800mV Fixed Offset : 50mV Bit Step Size : 50mV

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8.5.1.9 REG0B_VOTG_regulation Register (Offset = Bh) [reset = DCh]

REG0B_VOTG_regulation is shown in 図 8-33 and described in 表 8-18.

Return to the 表 8-8.

VOTG regulation

図 8-33. REG0B_VOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED					VOTG_10:0		
R-0h					R/W-DCh		
7	6	5	4	3	2	1	0
VOTG_10:0							
R/W-DCh							

表 8-18. REG0B_VOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-11	RESERVED	R	0h		RESERVED
10-0	VOTG_10:0	R/W	DCh	Reset by: WATCHDOG REG_RST	OTG mode regulation voltage Type : RW POR: 5000mV (DCh) Range : 2800mV-22000mV Fixed Offset : 2800mV Bit Step Size : 10mV Clamped High

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8.5.1.10 REG0D_IOTG_regulation Register (Offset = Dh) [reset = 4Bh]

REG0D_IOTG_regulation is shown in 図 8-34 and described in 表 8-19.

Return to the 表 8-8.

IOTG regulation

図 8-34. REG0D_IOTG_regulation Register

7	6	5	4	3	2	1	0
PRECHG_TMR	IOTG_6:0						
R/W-0h	R/W-4Bh						

表 8-19. REG0D_IOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PRECHG_TMR	R/W	0h	Reset by: WATCHDOG REG_RST	Pre-charge safety timer setting Type : RW POR: 0b 0h = 2 hrs (default) 1h = 0.5 hrs
6-0	IOTG_6:0	R/W	4Bh	Reset by: WATCHDOG REG_RST	OTG current limit Type : RW POR: 3040mA (4Bh) Range : 160mA-3360mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

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8.5.1.11 REG0E_Timer_Control Register (Offset = Eh) [reset = 3Dh]

REG0E_Timer_Control is shown in 図 8-35 and described in 表 8-20.

Return to the 表 8-8.

Timer Control

図 8-35. REG0E_Timer_Control Register

7	6	5	4	3	2	1	0
TOPOFF_TMR_1:0		EN_TRICHG_TMR	EN_PRECHG_TMR	EN_CHG_TMR	CHG_TMR_1:0		TMR2X_EN
R/W-0h		R/W-1h	R/W-1h	R/W-1h	R/W-2h		R/W-1h

表 8-20. REG0E_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TOPOFF_TMR_1:0	R/W	0h	Reset by: WATCHDOG REG_RST	Top-off timer control Type : RW POR: 00b 0h = Disabled (default) 1h = 15 mins 2h = 30 mins 3h = 45 mins
5	EN_TRICHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable trickle charge timer (fixed as 1hr) Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
4	EN_PRECHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable pre-charge timer Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
3	EN_CHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable fast charge timer Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
2-1	CHG_TMR_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Fast charge timer setting Type : RW POR: 10b 0h = 5 hrs 1h = 8 hrs 2h = 12 hrs (default) 3h = 24 hrs
0	TMR2X_EN	R/W	1h	Reset by: WATCHDOG REG_RST	TMR2X_EN Type : RW POR: 1b 0h = Trickle charge, pre-charge and fast charge timer NOT slowed by 2X during input DPM or thermal regulation. 1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)

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8.5.1.12 REG0F_Charger_Control_0 Register (Offset = Fh) [reset = A2h]

REG0F_Charger_Control_0 is shown in 図 8-36 and described in 表 8-21.

Return to the 表 8-8.

Charger Control 0

図 8-36. REG0F_Charger_Control_0 Register

7	6	5	4	3	2	1	0
EN_AUTO_IBATDIS	FORCE_IBATDIS	EN_CHG	EN_ICO	FORCE_ICO	EN_HIZ	EN_TERM	RESERVED
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	

表 8-21. REG0F_Charger_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_IBATDIS	R/W	1h	Reset by: REG_RST	Enable the auto battery discharging during the battery OVP fault Type : RW POR: 1b 0h = The charger will NOT apply a discharging current on BAT during battery OVP 1h = The charger will apply a discharging current on BAT during battery OVP
6	FORCE_IBATDIS	R/W	0h	Reset by: REG_RST	Force a battery discharging current Type : RW POR: 0b 0h = IDLE (default) 1h = Force the charger to apply a discharging current on BAT regardless the battery OVP status
5	EN_CHG	R/W	1h	Reset by: WATCHDOG REG_RST	Charger Enable Configuration Type : RW POR: 1b 0h = Charge Disable 1h = Charge Enable (default)
4	EN_ICO	R/W	0h	Reset by: REG_RST	Input Current Optimizer (ICO) Enable Type : RW POR: 0b 0h = Disable ICO (default) 1h = Enable ICO
3	FORCE_ICO	R/W	0h	Reset by: WATCHDOG REG_RST	Force start input current optimizer (ICO) Note: This bit can only be set and returns 0 after ICO starts. This bit only valid when EN_ICO = 1 Type : RW POR: 0b 0h = Do NOT force ICO (Default) 1h = Force ICO start
2	EN_HIZ	R/W	0h	Reset by: REG_RST	Enable HIZ mode. This bit will be also reset to 0, when the adapter is plugged in at VBUS. Type : RW POR: 0b 0h = Disable (default) 1h = Enable
1	EN_TERM	R/W	1h	Reset by: WATCHDOG REG_RST	Enable termination Type : RW POR: 1b 0h = Disable 1h = Enable (default)

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表 8-21. REG0F_Charger_Control_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	RESERVED	R	0h		Reserved

8.5.1.13 REG10_Charger_Control_1 Register (Offset = 10h) [reset = 85h]

REG10_Charger_Control_1 is shown in 図 8-37 and described in 表 8-22.

Return to the 表 8-8.

Charger Control 1

図 8-37. REG10_Charger_Control_1 Register

7	6	5	4	3	2	1	0
		VAC_OVP_1:0		WD_RST	WATCHDOG_2:0		
R-0h		R/W-0h		R/W-0h	R/W-5h		

表 8-22. REG10_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	RESERVED	R	0h		Reserved
5-4	VAC_OVP_1:0	R/W	0h	Reset by: REG_RST	VAC_OVP thresholds Type : RW POR: 11b 0h = 26V (default) 1h = 22V 2h = 12V 3h = 7V
3	WD_RST	R/W	0h	Reset by: WATCHDOG REG_RST	I2C watch dog timer reset Type : RW POR: 0b 0h = Normal (default) 1h = Reset (this bit goes back to 0 after timer resets)
2-0	WATCHDOG_2:0	R/W	5h	Reset by: REG_RST	Watchdog timer settings Type : RW POR: 101b 0h = Disable 1h = 0.5s 2h = 1s 3h = 2s 4h = 20s 5h = 40s (default) 6h = 80s 7h = 160s

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8.5.1.14 REG11_Charger_Control_2 Register (Offset = 11h) [reset = 40h]

REG11_Charger_Control_2 is shown in 図 8-38 and described in 表 8-23.

Return to the 表 8-8.

Charger Control 2

図 8-38. REG11_Charger_Control_2 Register

7	6	5	4	3	2	1	0
FORCE_INDET	AUTO_INDET_EN	EN_12V	EN_9V	HVDCP_EN	SDRV_CTRL_1:0		SDRV_DLY
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

表 8-23. REG11_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	FORCE_INDET	R/W	0h	Reset by: WATCHDOG REG_RST	Force D+/D- detection Type : RW POR: 0b 0h = Do NOT force D+/D- detection (default) 1h = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0
6	AUTO_INDET_EN	R/W	1h	Reset by: WATCHDOG REG_RST	Automatic D+/D- Detection Enable Type : RW POR: 1b 0h = Disable D+/D- detection when VBUS is plugged-in 1h = Enable D+/D- detection when VBUS is plugged-in (default)
5	EN_12V	R/W	0h	Reset by: REG_RST	EN_12V HVDC Type : RW POR: 0b 0h = Disable 12V mode in HVDCP (default) 1h = Enable 12V mode in HVDCP
4	EN_9V	R/W	0h	Reset by: REG_RST	EN_9V HVDC Type : RW POR: 0b 0h = Disable 9V mode in HVDCP (default) 1h = Enable 9V mode in HVDCP
3	HVDCP_EN	R/W	0h	Reset by: REG_RST	High voltage DCP enable. Type : RW POR: 0b 0h = Disable HVDCP handshake (default) 1h = Enable HVDCP handshake
2-1	SDRV_CTRL_1:0	R/W	0h	Reset by: REG_RST	SFET control The external ship FET control logic to force the device enter different modes. Type : RW POR: 00b 0h = IDLE (default) 1h = Shutdown Mode 2h = Ship Mode 3h = System Power Reset

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表 8-23. REG11_Charger_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	SDRV_DLY	R/W	0h	Reset by: REG_RST	Delay time added to the taking action in bit [2:1] of the SFET control Type : RW POR: 0b 0h = Add 10s delay time (default) 1h = Do NOT add 10s delay time

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8.5.1.15 REG12_Charger_Control_3 Register (Offset = 12h) [reset = 0h]

REG12_Charger_Control_3 is shown in 図 8-39 and described in 表 8-24.

Return to the 表 8-8.

Charger Control 3

図 8-39. REG12_Charger_Control_3 Register

7	6	5	4	3	2	1	0
DIS_ACDRV	EN_OTG	PFM_OTG_DIS	PFM_FWD_DIS	WKUP_DLY	DIS_LDO	DIS_OTG_OOA	DIS_FWD_OOA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-24. REG12_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_ACDRV	R/W	0h		When this bit is set, the charger will force both EN_ACDRV1=0 and EN_ACDRV2=0 Type : RW POR: 0b
6	EN_OTG	R/W	0h	Reset by: WATCHDOG REG_RST	OTG mode control Type : RW POR: 0b 0h = OTG Disable (default) 1h = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Reset by: WATCHDOG REG_RST	Disable PFM in OTG mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	PFM_FWD_DIS	R/W	0h	Reset by: REG_RST	Disable PFM in forward mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	WKUP_DLY	R/W	0h	Reset by: REG_RST	When wake up the device from ship mode, how much time (t_{SM_EXIT}) is required to pull low the $\overline{QON}$ pin. Type : RW POR: 0b 0h = 1s (Default) 1h = 15ms
2	DIS_LDO	R/W	0h	Reset by: WATCHDOG REG_RST	Disable BATFET LDO mode in pre-charge stage. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
1	DIS_OTG_OOA	R/W	0h	Reset by: WATCHDOG REG_RST	Disable OOA in OTG mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
0	DIS_FWD_OOA	R/W	0h	Reset by: REG_RST	Disable OOA in forward mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable

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8.5.1.16 REG13_Charger_Control_4 Register (Offset = 13h) [reset = X]

REG13_Charger_Control_4 is shown in 図 8-40 and described in 表 8-25.

Return to the 表 8-8.

Charger Control 4

図 8-40. REG13_Charger_Control_4 Register

7	6	5	4	3	2	1	0
EN_ACDRV2	EN_ACDRV1	PWM_FREQ	DIS_STAT	DIS_VSYS_SHORT	DIS_VOTG_UVP	FORCE_VINDPM_DET	EN_IBUS_OCP
R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

表 8-25. REG13_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_ACDRV2	R/W	0h		External ACFET2-RBFET2 gate driver control At POR, if the charger detects that there is no ACFET2-RBFET2 populated, this bit will be locked at 0 Type : RW POR: 0b 0h = turn off (default) 1h = turn on
6	EN_ACDRV1	R/W	0h		External ACFET1-RBFET1 gate driver control At POR, if the charger detects that there is no ACFET1-RBFET1 populated, this bit will be locked at 0 Type : RW POR: 0b 0h = turn off (default) 1h = turn on
5	PWM_FREQ	R/W	X		Switching frequency selection, this bit POR default value is based on the PROG pin strapping. Type : RW 0h = 1.5 MHz 1h = 750 kHz
4	DIS_STAT	R/W	0h	Reset by: WATCHDOG REG_RST	Disable the STAT pin output Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	DIS_VSYS_SHORT	R/W	0h	Reset by: REG_RST	Disable forward mode VSYS short hiccup protection. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
2	DIS_VOTG_UVP	R/W	0h	Reset by: REG_RST	Disable OTG mode VOTG UVP hiccup protection. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable

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表 8-25. REG13_Charger_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
1	FORCE_VINDPM_DET	R/W	0h	Reset by: REG_RST	Force VINDPM detection Note: only when VBAT>VSYSMIN, this bit can be set to 1. Once the VINDPM auto detection is done, this bits returns to 0. Type : RW POR: 0b 0h = Do NOT force VINDPM detection (default) 1h = Force the converter stop switching, and ADC measures the VBUS voltage without input current, then the charger updates the VINDPM register accordingly.
0	EN_IBUS_OCP	R/W	1h	Reset by: REG_RST	Enable IBUS_OCP in forward mode Type : RW POR: 1b 0h = Disable 1h = Enable (default)

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8.5.1.17 REG14_Charger_Control_5 Register (Offset = 14h) [reset = 16h]

REG14_Charger_Control_5 is shown in 図 8-41 and described in 表 8-26.

Return to the 表 8-8.

Charger Control 5

図 8-41. REG14_Charger_Control_5 Register

7	6	5	4	3	2	1	0
SFET_PRESENT	RESERVED	EN_IBAT	IBAT_REG_1:0		EN_IINDPM	EN_EXTILIM	EN_BATOC
R/W-0h	R-0h	R/W-0h	R/W-2h		R/W-1h	R/W-1h	R/W-0h

表 8-26. REG14_Charger_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	SFET_PRESENT	R/W	0h		The user has to set this bit based on whether a ship FET is populated or not. The POR default value is 0, which means the charger does not support all the features associated with the ship FET. The register bits list below all are locked at 0. EN_BATOC=0 SDRV_CTRL=00 When this bit is set to 1, the register bits list above become programmable, and the charger can support the features associated with the ship FET Type : RW POR: 0b 0h = No ship FET populated 1h = Ship FET populated
6	RESERVED	R	0h		Reserved
5	EN_IBAT	R/W	0h	Reset by: WATCHDOG REG_RST	IBAT discharge current sensing enable Type : RW POR: 0b 0h = Disable the IBAT discharge sensing at battery only or OTG condition (default) 1h = Enable the IBAT discharge sensing at battery only or OTG condition
4-3	IBAT_REG_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Battery discharging current regulation in OTG mode Type : RW POR: 10b 0h = 3A 1h = 4A 2h = 5A 3h = Disable (default)
2	EN_IINDPM	R/W	1h	Reset by: WATCHDOG REG_RST	Enable the internal IINDPM register input current regulation Type : RW POR: 1b 0h = Disable 1h = Enable (default)
1	EN_EXTILIM	R/W	1h	Reset by: REG_RST	Enable the external ILIM_HIZ pin input current regulation Type : RW POR: 1b 0h = Disable 1h = Enable (default)

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表 8-26. REG14_Charger_Control_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	EN_BATOC	R/W	0h	Reset by: WATCHDOG REG_RST	Enable the battery discharging current OCP Type : RW POR: 0b 0h = Disable (default) 1h = Enable

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8.5.1.18 REG15_MPPT_Control Register (Offset = 15h) [reset = AAh]

REG15_MPPT_Control is shown in 図 8-42 and described in 表 8-27.

Return to the 表 8-8.

MPPT Control

図 8-42. REG15_MPPT_Control Register

7	6	5	4	3	2	1	0
VOC_PCT_2:0			VOC_DLY_1:0		VOC_RATE_1:0		EN_MPPT
R/W-5h			R/W-1h		R/W-1h		R/W-0h

表 8-27. REG15_MPPT_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	VOC_PCT_2:0	R/W	5h	Reset by: REG_RST	To set the VINDPM as a percentage of the VBUS open circuit voltage when the VOC measurement is done. Type : RW POR: 101b 0h = 0.5625 1h = 0.625 2h = 0.6875 3h = 0.75 4h = 0.8125 5h = 0.875 (default) 6h = 0.9375 7h = 1
4-3	VOC_DLY_1:0	R/W	1h	Reset by: REG_RST	After the converter stops switching, the time delay before the VOC is measured. Type : RW POR: 01b 0h = 50ms 1h = 300ms (default) 2h = 2s 3h = 5s
2-1	VOC_RATE_1:0	R/W	1h	Reset by: REG_RST	The time interval two VBUS open circuit voltage measurements. Type : RW POR: 01b 0h = 30s 1h = 2mins (default) 2h = 10mins 3h = 30mins
0	EN_MPPT	R/W	0h	Reset by: REG_RST	Enable the MPPT to measure the VBUS open circuit voltage. Type : RW POR: 0b 0h = Disable (default) 1h = Enable

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8.5.1.19 REG16_Temperature_Control Register (Offset = 16h) [reset = C0h]

REG16_Temperature_Control is shown in 図 8-43 and described in 表 8-28.

Return to the 表 8-8.

Temperature Control

図 8-43. REG16_Temperature_Control Register

7	6	5	4	3	2	1	0
TREG_1:0		TSHUT_1:0		VBUS_PD_EN	VAC1_PD_EN	VAC2_PD_EN	RESERVED
R/W-3h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R-0h

表 8-28. REG16_Temperature_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TREG_1:0	R/W	3h	Reset by: WATCHDOG REG_RST	Thermal regulation thresholds. Type : RW POR: 11b 0h = 60°C 1h = 80°C 2h = 100°C 3h = 120°C (default)
5-4	TSHUT_1:0	R/W	0h	Reset by: WATCHDOG REG_RST	Thermal shutdown thresholds. Type : RW POR: 00b 0h = 150°C (default) 1h = 130°C 2h = 120°C 3h = 85°C
3	VBUS_PD_EN	R/W	0h	Reset by: REG_RST	Enable VBUS pull down resistor (6k Ohm) Type : RW POR: 0b 0h = Disable (default) 1h = Enable
2	VAC1_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC1 pull down resistor Type : RW POR: 0b 0h = Disable (default) 1h = Enable
1	VAC2_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC2 pull down resistor Type : RW POR: 0b 0h = Disable (default) 1h = Enable
0	Reserved	R	0h	Reserved	Reserved

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8.5.1.20 REG17_NTC_Control_0 Register (Offset = 17h) [reset = 7Ah]

REG17_NTC_Control_0 is shown in 図 8-44 and described in 表 8-29.

Return to the 表 8-8.

NTC Control 0

図 8-44. REG17_NTC_Control_0 Register

7	6	5	4	3	2	1	0
JEITA_VSET_2:0			JEITA_ISETH_1:0		JEITA_ISETC_1:0		RESERVED
R/W-3h			R/W-3h		R/W-1h		R-0h

表 8-29. REG17_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	JEITA_VSET_2:0	R/W	3h	Reset by: WATCHDOG REG_RST	JEITA high temperature range (TWARN – THOT) charge voltage setting Type : RW POR: 011b 0h = Charge Suspend 1h = Set VREG to VREG-800mV 2h = Set VREG to VREG-600mV 3h = Set VREG to VREG-400mV (default) 4h = Set VREG to VREG-300mV 5h = Set VREG to VREG-200mV 6h = Set VREG to VREG-100mV 7h = VREG unchanged
4-3	JEITA_ISETH_1:0	R/W	3h	Reset by: WATCHDOG REG_RST	JEITA high temperature range (TWARN – THOT) charge current setting Type : RW POR: 11b 0h = Charge Suspend 1h = Set ICHG to 20%* ICHG 2h = Set ICHG to 40%* ICHG 3h = ICHG unchanged (default)
2-1	JEITA_ISETC_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA low temperature range (TCOLD – TCOOL) charge current setting Type : RW POR: 01b 0h = Charge Suspend 1h = Set ICHG to 20%* ICHG (default) 2h = Set ICHG to 40%* ICHG 3h = ICHG unchanged
0	RESERVED	R	0h		Reserved

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8.5.1.21 REG18_NTC_Control_1 Register (Offset = 18h) [reset = 54h]

REG18_NTC_Control_1 is shown in 図 8-45 and described in 表 8-30.

Return to the 表 8-8.

NTC Control 1

図 8-45. REG18_NTC_Control_1 Register

7	6	5	4	3	2	1	0
TS_COOL_1:0		TS_WARM_1:0		BHOT_1:0		BCOLD	TS_IGNORE
R/W-1h		R/W-1h		R/W-1h		R/W-0h	R/W-0h

表 8-30. REG18_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TS_COOL_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA VT2 comparator voltage rising thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. Type : RW POR: 01b 0h = 71.1% (5°C) 1h = 68.4% (default) (10°C) 2h = 65.5% (15°C) 3h = 62.4% (20°C)
5-4	TS_WARM_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA VT3 comparator voltage falling thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. Type : RW POR: 01b 0h = 48.4% (40°C) 1h = 44.8% (default) (45°C) 2h = 41.2% (50°C) 3h = 37.7% (55°C)
3-2	BHOT_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	OTG mode TS HOT temperature threshold Type : RW POR: 01b 0h = 55°C 1h = 60°C (default) 2h = 65°C 3h = Disable
1	BCOLD	R/W	0h	Reset by: WATCHDOG REG_RST	OTG mode TS COLD temperature threshold Type : RW POR: 0b 0h = -10°C (default) 1h = -20°C
0	TS_IGNORE	R/W	0h	Reset by: WATCHDOG REG_RST	Ignore the TS feedback, the charger considers the TS is always good to allow the charging and OTG modes, all the four TS status bits always stay at 0000 to report the normal condition. Type : RW POR: 0b 0h = NOT ignore (Default) 1h = Ignore

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8.5.1.22 REG19_ICO_Current_Limit Register (Offset = 19h) [reset = 0h]

REG19_ICO_Current_Limit is shown in 図 8-46 and described in 表 8-31.

Return to the 表 8-8.

ICO Current Limit

図 8-46. REG19_ICO_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							ICO_ILIM_8:0
R-0h							R-0h
7	6	5	4	3	2	1	0
ICO_ILIM_8:0							
R-0h							

表 8-31. REG19_ICO_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	RESERVED
8-0	ICO_ILIM_8:0	R	0h	Input Current Limit obtained from ICO or ILIM_HIZ pin setting Type : R POR: 0mA (0h) Range : 100mA-3300mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

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8.5.1.23 REG1B_Charger_Status_0 Register (Offset = 1Bh) [reset = 0h]

REG1B_Charger_Status_0 is shown in 図 8-47 and described in 表 8-32.

Return to the 表 8-8.

Charger Status 0

図 8-47. REG1B_Charger_Status_0 Register

7	6	5	4	3	2	1	0
IINDPM_STAT	VINDPM_STAT	WD_STAT	RESERVED	PG_STAT	AC2_PRESENT_STAT	AC1_PRESENT_STAT	VBUS_PRESENT_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-32. REG1B_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IINDPM_STAT	R	0h	IINDPM status (forward mode) or IOTG status (OTG mode) Type : R POR: 0b 0h = Normal 1h = In IINDPM regulation or IOTG regulation
6	VINDPM_STAT	R	0h	VINDPM status (forward mode) or VOTG status (OTG mode) Type : R POR: 0b 0h = Normal 1h = In VINDPM regulation or VOTG regualtion
5	WD_STAT	R	0h	I2C watch dog timer status Type : R POR: 0b 0h = Normal 1h = WD timer expired
4	RESERVED	R	0h	RESERVED
3	PG_STAT	R	0h	Power Good Status Type : R POR: 0b 0h = NOT in power good status 1h = Power good
2	AC2_PRESENT_STAT	R	0h	VAC2 insert status Type : R POR: 0b 0h = VAC2 NOT present 1h = VAC2 present (above present threshold)
1	AC1_PRESENT_STAT	R	0h	VAC1 insert status Type : R POR: 0b 0h = VAC1 NOT present 1h = VAC1 present (above present threshold)

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表 8-32. REG1B_Charger_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VBUS_PRESENT_STAT	R	0h	VBUS present status Type : R POR: 0b 0h = VBUS NOT present 1h = VBUS present (above present threshold)

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8.5.1.24 REG1C_Charger_Status_1 Register (Offset = 1Ch) [reset = 0h]

REG1C_Charger_Status_1 is shown in 図 8-48 and described in 表 8-33.

Return to the 表 8-8.

Charger Status 1

図 8-48. REG1C_Charger_Status_1 Register

7	6	5	4	3	2	1	0
CHG_STAT_2:0			VBUS_STAT_3:0				BC1.2_DONE_STAT
R-0h			R-0h				R-0h

表 8-33. REG1C_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CHG_STAT_2:0	R	0h	Charge Status bits Type : R POR: 000b 0h = Not Charging 1h = Trickle Charge 2h = Pre-charge 3h = Fast charge (CC mode) 4h = Taper Charge (CV mode) 5h = Reserved 6h = Top-off Timer Active Charging 7h = Charge Termination Done
4-1	VBUS_STAT_3:0	R	0h	VBUS status bits 0h: No Input or BHOT or BCOLD in OTG mode 1h: USB SDP (500mA) 2h: USB CDP (1.5A) 3h: USB DCP (3.25A) 4h: Adjustable High Voltage DCP (HVDCP) (1.5A) 5h: Unknown adaptor (3A) 6h: Non-Standard Adapter (1A/2A/2.1A/2.4A) 7h: In OTG mode 8h: Not qualified adaptor 9h: Reserved Ah: Reserved Bh: Device directly powered from VBUS Ch: Backup Mode Dh: Reserved Eh: Reserved Fh: Reserved Type : R POR: 0h

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表 8-33. REG1C_Charger_Status_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BC1.2_DONE_STAT	R	0h	BC1.2 status bit Type : R POR: 0b 0h = BC1.2 or non-standard detection NOT complete 1h = BC1.2 or non-standard detection complete

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8.5.1.25 REG1D_Charger_Status_2 Register (Offset = 1Dh) [reset = 0h]

REG1D_Charger_Status_2 is shown in 図 8-49 and described in 表 8-34.

Return to the 表 8-8.

Charger Status 2

図 8-49. REG1D_Charger_Status_2 Register

7	6	5	4	3	2	1	0
ICO_STAT_1:0		RESERVED			TREG_STAT	DPDM_STAT	VBAT_PRESENT_STAT
R-0h		R-0h			R-0h	R-0h	R-0h

表 8-34. REG1D_Charger_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ICO_STAT_1:0	R	0h	Input Current Optimizer (ICO) status Type : R POR: 00b 0h = ICO disabled 1h = ICO optimization in progress 2h = Maximum input current detected 3h = Reserved
5-3	RESERVED	R	0h	RESERVED
2	TREG_STAT	R	0h	IC thermal regulation status Type : R POR: 0b 0h = Normal 1h = Device in thermal regulation
1	DPDM_STAT	R	0h	D+/D- detection status bits Type : R POR: 0b 0h = The D+/D- detection is NOT started yet, or the detection is done 1h = The D+/D- detection is ongoing
0	VBAT_PRESENT_STAT	R	0h	Battery present status (V_{BAT} > V_{BAT_UVLOZ}) Type : R POR: 0b 0h = V_{BAT} NOT present 1h = V_{BAT} present

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8.5.1.26 REG1E_Charger_Status_3 Register (Offset = 1Eh) [reset = 0h]

REG1E_Charger_Status_3 is shown in 図 8-50 and described in 表 8-35.

Return to the 表 8-8.

Charger Status 3

図 8-50. REG1E_Charger_Status_3 Register

7	6	5	4	3	2	1	0
ACRB2_STAT	ACRB1_STAT	ADC_DONE_STAT	VSYS_STAT	CHG_TMR_STAT	TRICHG_TMR_STAT	PRECHG_TMR_STAT	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-35. REG1E_Charger_Status_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACRB2_STAT	R	0h	The ACFET2-RBFET2 status Type : R POR: 0b 0h = ACFET2-RBFET2 is NOT placed 1h = ACFET2-RBFET2 is placed
6	ACRB1_STAT	R	0h	The ACFET1-RBFET1 status Type : R POR: 0b 0h = ACFET1-RBFET1 is NOT placed 1h = ACFET1-RBFET1 is placed
5	ADC_DONE_STAT	R	0h	ADC Conversion Status (in one-shot mode only) Type : R POR: 0b 0h = Conversion NOT complete 1h = Conversion complete
4	VSYS_STAT	R	0h	VSYS Regulation Status (forward mode) Type : R POR: 0b 0h = Not in VSYSMIN regulation (V_{BAT} > V_{SYSMIN}) 1h = In VSYSMIN regulation (V_{BAT} < V_{SYSMIN})
3	CHG_TMR_STAT	R	0h	Fast charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired
2	TRICHG_TMR_STAT	R	0h	Trickle charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired

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表 8-35. REG1E_Charger_Status_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRECHG_TMR_STAT	R	0h	Pre-charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired
0	RESERVED	R	0h	RESERVED

8.5.1.27 REG1F_Charger_Status_4 Register (Offset = 1Fh) [reset = 0h]

REG1F_Charger_Status_4 is shown in 図 8-51 and described in 表 8-36.

Return to the 表 8-8.

Charger Status 4

図 8-51. REG1F_Charger_Status_4 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_STAT	TS_COLD_STAT	TS_COOL_STAT	TS_WARM_STAT	TS_HOT_STAT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

表 8-36. REG1F_Charger_Status_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	VBATOTG_LOW_STAT	R	0h	The battery voltage is too low to enable OTG mode. Type : R POR: 0b 0h = The battery voltage is high enough to enable the OTG operation 1h = The battery volage is too low to enable the OTG operation
3	TS_COLD_STAT	R	0h	The TS temperature is in the cold range, lower than T1. Type : R POR: 0b 0h = TS status is NOT in cold range 1h = TS status is in cold range
2	TS_COOL_STAT	R	0h	The TS temperature is in the cool range, between T1 and T2. Type : R POR: 0b 0h = TS status is NOT in cool range 1h = TS status is in cool range
1	TS_WARM_STAT	R	0h	The TS temperature is in the warm range, between T3 and T5. Type : R POR: 0b 0h = TS status is NOT in warm range 1h = TS status is in warm range
0	TS_HOT_STAT	R	0h	The TS temperature is in the hot range, higher than T5. Type : R POR: 0b 0h = TS status is NOT in hot range 1h = TS status is in hot range

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8.5.1.28 REG20_FAULT_Status_0 Register (Offset = 20h) [reset = 0h]

REG20_FAULT_Status_0 is shown in 図 8-52 and described in 表 8-37.

Return to the 表 8-8.

FAULT Status 0

図 8-52. REG20_FAULT_Status_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_STAT	VBUS_OVP_STAT	VBAT_OVP_STAT	IBUS_OCP_STAT	IBAT_OCP_STAT	CONV_OCP_STAT	VAC2_OVP_STAT	VAC1_OVP_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-37. REG20_FAULT_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IBAT_REG_STAT	R	0h	IBAT regulation status Type : R POR: 0b 0h = Normal 1h = Device in battery discharging current regulation
6	VBUS_OVP_STAT	R	0h	VBUS over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection
5	VBAT_OVP_STAT	R	0h	VBAT over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection
4	IBUS_OCP_STAT	R	0h	IBUS over-current status Type : R POR: 0b 0h = Normal 1h = Device in over current protection
3	IBAT_OCP_STAT	R	0h	IBAT over-current status Type : R POR: 0b 0h = Normal 1h = Device in over current protection
2	CONV_OCP_STAT	R	0h	Converter over current status Type : R POR: 0b 0h = Normal 1h = Converter in over current protection

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表 8-37. REG20_FAULT_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VAC2_OVP_STAT	R	0h	VAC2 over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection
0	VAC1_OVP_STAT	R	0h	VAC1 over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection

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8.5.1.29 REG21_FAULT_Status_1 Register (Offset = 21h) [reset = 0h]

REG21_FAULT_Status_1 is shown in 図 8-53 and described in 表 8-38.

Return to the 表 8-8.

FAULT Status 1

図 8-53. REG21_FAULT_Status_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_STAT	VSYS_OVP_STAT	OTG_OVP_STAT	OTG_UVP_STAT	RESERVED	TSHUT_STAT	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

表 8-38. REG21_FAULT_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VSYS_SHORT_STAT	R	0h	VSYS short circuit status Type : R POR: 0b 0h = Normal 1h = Device in SYS short circuit protection
6	VSYS_OVP_STAT	R	0h	VSYS over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in SYS over-voltage protection
5	OTG_OVP_STAT	R	0h	OTG over voltage status Type : R POR: 0b 0h = Normal 1h = Device in OTG over-voltage
4	OTG_UVP_STAT	R	0h	OTG under voltage status. Type : R POR: 0b 0h = Normal 1h = Device in OTG under voltage
3	RESERVED	R	0h	RESERVED
2	TSHUT_STAT	R	0h	IC temperature shutdown status Type : R POR: 0b 0h = Normal 1h = Device in thermal shutdown protection
1-0	RESERVED	R	0h	RESERVED

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8.5.1.30 REG22_Charger_Flag_0 Register (Offset = 22h) [reset = 0h]

REG22_Charger_Flag_0 is shown in 図 8-54 and described in 表 8-39.

Return to the 表 8-8.

Charger Flag 0

図 8-54. REG22_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
IINDPM_FLAG	VINDPM_FLAG	WD_FLAG	POORSRC_FLAG	PG_FLAG	AC2_PRESENT_FLAG	AC1_PRESENT_FLAG	VBUS_PRESENT_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-39. REG22_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IINDPM_FLAG	R	0h	IINDPM / IOTG flag Type : R POR: 0b 0h = Normal 1h = IINDPM / IOTG signal rising edge detected
6	VINDPM_FLAG	R	0h	VINDPM / VOTG Flag Type : R POR: 0b 0h = Normal 1h = VINDPM / VOTG regulation signal rising edge detected
5	WD_FLAG	R	0h	I2C watchdog timer flag Type : R POR: 0b 0h = Normal 1h = WD timer signal rising edge detected
4	POORSRC_FLAG	R	0h	Poor source detection flag Type : R POR: 0b 0h = Normal 1h = Poor source status rising edge detected
3	PG_FLAG	R	0h	Power good flag Type : R POR: 0b 0h = Normal 1h = Any change in PG_STAT even (adapter good qualification or adapter good going away)
2	AC2_PRESENT_FLAG	R	0h	VAC2 present flag Type : R POR: 0b 0h = Normal 1h = VAC2 present status changed

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表 8-39. REG22_Charger_Flag_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AC1_PRESENT_FLAG	R	0h	VAC1 present flag Type : R POR: 0b 0h = Normal 1h = VAC1 present status changed
0	VBUS_PRESENT_FLAG	R	0h	VBUS present flag Type : R POR: 0b 0h = Normal 1h = VBUS present status changed

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8.5.1.31 REG23_Charger_Flag_1 Register (Offset = 23h) [reset = 0h]

REG23_Charger_Flag_1 is shown in 図 8-55 and described in 表 8-40.

Return to the 表 8-8.

Charger Flag 1

図 8-55. REG23_Charger_Flag_1 Register

7	6	5	4	3	2	1	0
CHG_FLAG	ICO_FLAG	RESERVED	VBUS_FLAG	RESERVED	TREG_FLAG	VBAT_PRESENT_FLAG	BC1.2_DONE_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-40. REG23_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CHG_FLAG	R	0h	Charge status flag Type : R POR: 0b 0h = Normal 1h = Charge status changed
6	ICO_FLAG	R	0h	ICO status flag Type : R POR: 0b 0h = Normal 1h = ICO status changed
5	RESERVED	R	0h	RESERVED
4	VBUS_FLAG	R	0h	VBUS status flag Type : R POR: 0b 0h = Normal 1h = VBUS status changed
3	RESERVED	R	0h	RESERVED
2	TREG_FLAG	R	0h	IC thermal regulation flag Type : R POR: 0b 0h = Normal 1h = TREG signal rising threshold detected
1	VBAT_PRESENT_FLAG	R	0h	VBAT present flag Type : R POR: 0b 0h = Normal 1h = VBAT present status changed

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表 8-40. REG23_Charger_Flag_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BC1.2_DONE_FLAG	R	0h	BC1.2 status Flag Type : R POR: 0b 0h = Normal 1h = BC1.2 detection status changed

8.5.1.32 REG24_Charger_Flag_2 Register (Offset = 24h) [reset = 0h]

REG24_Charger_Flag_2 is shown in 図 8-56 and described in 表 8-41.

Return to the 表 8-8.

Charger Flag 2

図 8-56. REG24_Charger_Flag_2 Register

7	6	5	4	3	2	1	0
RESERVED	DPDM_DONE_FLAG	ADC_DONE_FLAG	VSYS_FLAG	CHG_TMR_FLAG	TRICHG_TMR_FLAG	PRECHG_TMR_FLAG	TOPOFF_TMR_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-41. REG24_Charger_Flag_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	DPDM_DONE_FLAG	R	0h	D+/D- detection is done flag. Type : R POR: 0b 0h = D+/D- detection is NOT started or still ongoing 1h = D+/D- detection is completed
5	ADC_DONE_FLAG	R	0h	ADC conversion flag (only in one-shot mode) Type : R POR: 0b 0h = Conversion NOT completed 1h = Conversion completed
4	VSYS_FLAG	R	0h	VSYSMIN regulation flag Type : R POR: 0b 0h = Normal 1h = Entered or existed VSYSMIN regulation
3	CHG_TMR_FLAG	R	0h	Fast charge timer flag Type : R POR: 0b 0h = Normal 1h = Fast charge timer expired rising edge detected
2	TRICHG_TMR_FLAG	R	0h	Trickle charge timer flag Type : R POR: 0b 0h = Normal 1h = Trickle charger timer expired rising edge detected
1	PRECHG_TMR_FLAG	R	0h	Pre-charge timer flag Type : R POR: 0b 0h = Normal 1h = Pre-charge timer expired rising edge detected

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表 8-41. REG24_Charger_Flag_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TOPOFF_TMR_FLAG	R	0h	Top off timer flag Type : R POR: 0b 0h = Normal 1h = Top off timer expired rising edge detected

8.5.1.33 REG25_Charger_Flag_3 Register (Offset = 25h) [reset = 0h]

REG25_Charger_Flag_3 is shown in 図 8-57 and described in 表 8-42.

Return to the 表 8-8.

Charger Flag 3

図 8-57. REG25_Charger_Flag_3 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_FLAG	TS_COLD_FLAG	TS_COOL_FLAG	TS_WARM_FLAG	TS_HOT_FLAG
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

表 8-42. REG25_Charger_Flag_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	VBATOTG_LOW_FLAG	R	0h	VBAT too low to enable OTG flag Type : R POR: 0b 0h = Normal 1h = VBAT falls below the threshold to enable the OTG mode
3	TS_COLD_FLAG	R	0h	TS cold temperature flag Type : R POR: 0b 0h = Normal 1h = TS across cold temperature (T1) is detected
2	TS_COOL_FLAG	R	0h	TS cool temperature flag Type : R POR: 0b 0h = Normal 1h = TS across cool temperature (T2) is detected
1	TS_WARM_FLAG	R	0h	TS warm temperature flag Type : R POR: 0b 0h = Normal 1h = TS across warm temperature (T3) is detected
0	TS_HOT_FLAG	R	0h	TS hot temperature flag Type : R POR: 0b 0h = Normal 1h = TS across hot temperature (T5) is detected

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8.5.1.34 REG26_FAULT_Flag_0 Register (Offset = 26h) [reset = 0h]

REG26_FAULT_Flag_0 is shown in 図 8-58 and described in 表 8-43.

Return to the 表 8-8.

FAULT Flag 0

図 8-58. REG26_FAULT_Flag_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_FLAG	VBUS_OVP_FLAG	VBAT_OVP_FLAG	IBUS_OCP_FLAG	IBAT_OCP_FLAG	CONV_OCP_FLAG	VAC2_OVP_FLAG	VAC1_OVP_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-43. REG26_FAULT_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IBAT_REG_FLAG	R	0h	IBAT regulation flag Type : R POR: 0b 0h = Normal 1h = Enter or exit IBAT regulation
6	VBUS_OVP_FLAG	R	0h	VBUS over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VBUS OVP
5	VBAT_OVP_FLAG	R	0h	VBAT over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VBAT OVP
4	IBUS_OCP_FLAG	R	0h	IBUS over-current flag Type : R POR: 0b 0h = Normal 1h = Enter IBUS OCP
3	IBAT_OCP_FLAG	R	0h	IBAT over-current flag Type : R POR: 0b 0h = Normal 1h = Enter discharged OCP
2	CONV_OCP_FLAG	R	0h	Converter over-current flag Type : R POR: 0b 0h = Normal 1h = Enter converter OCP

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表 8-43. REG26_FAULT_Flag_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VAC2_OVP_FLAG	R	0h	VAC2 over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VAC2 OVP
0	VAC1_OVP_FLAG	R	0h	VAC1 over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VAC1 OVP

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8.5.1.35 REG27_FAULT_Flag_1 Register (Offset = 27h) [reset = 0h]

REG27_FAULT_Flag_1 is shown in 図 8-59 and described in 表 8-44.

Return to the 表 8-8.

FAULT Flag 1

図 8-59. REG27_FAULT_Flag_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_FLAG	VSYS_OVP_FLAG	OTG_OVP_FLAG	OTG_UVP_FLAG	RESERVED	TSHUT_FLAG	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

表 8-44. REG27_FAULT_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VSYS_SHORT_FLAG	R	0h	VSYS short circuit flag Type : R POR: 0b 0h = Normal 1h = Stop switching due to system short
6	VSYS_OVP_FLAG	R	0h	VSYS over-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop switching due to system over-voltage
5	OTG_OVP_FLAG	R	0h	OTG over-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop OTG due to VBUS over voltage
4	OTG_UVP_FLAG	R	0h	OTG under-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop OTG due to VBUS under-voltage
3	RESERVED	R	0h	RESERVED
2	TSHUT_FLAG	R	0h	IC thermal shutdown flag Type : R POR: 0b 0h = Normal 1h = TS shutdown signal rising threshold detected
1-0	RESERVED	R	0h	RESERVED

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8.5.1.36 REG28_Charger_Mask_0 Register (Offset = 28h) [reset = 0h]

REG28_Charger_Mask_0 is shown in 図 8-60 and described in 表 8-45.

Return to the 表 8-8.

Charger Mask 0

図 8-60. REG28_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
IINDPM_MASK	VINDPM_MASK	WD_MASK	POORSRC_MASK	PG_MASK	AC2_PRESENT_MASK	AC1_PRESENT_MASK	VBUS_PRESENT_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-45. REG28_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IINDPM_MASK	R/W	0h	Reset by: REG_RST	IINDPM / IOTG mask flag Type : RW POR: 0b 0h = Enter IINDPM / IOTG does produce INT pulse 1h = Enter IINDPM / IOTG does NOT produce INT pulse
6	VINDPM_MASK	R/W	0h	Reset by: REG_RST	VINDPM / VOTG mask flag Type : RW POR: 0b 0h = Enter VINDPM / VOTG does produce INT pulse 1h = Enter VINDPM / VOTG does NOT produce INT pulse
5	WD_MASK	R/W	0h	Reset by: REG_RST	I2C watch dog timer mask flag Type : RW POR: 0b 0h = I2C watch dog timer expired does produce INT pulse 1h = I2C watch dog timer expired does NOT produce INT pulse
4	POORSRC_MASK	R/W	0h	Reset by: REG_RST	Poor source detection mask flag Type : RW POR: 0b 0h = Poor source detected does produce INT 1h = Poor source detected does NOT produce INT
3	PG_MASK	R/W	0h	Reset by: REG_RST	Power Good mask flag Type : RW POR: 0b 0h = PG toggle does produce INT 1h = PG toggle does NOT produce INT
2	AC2_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC2 present mask flag Type : RW POR: 0b 0h = VAC2 present status change does produce INT 1h = VAC2 present status change does NOT produce INT
1	AC1_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC1 present mask flag Type : RW POR: 0b 0h = VAC1 present status change does produce INT 1h = VAC1 present status change does NOT produce INT

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表 8-45. REG28_Charger_Mask_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	VBUS_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VBUS present mask flag Type : RW POR: 0b 0h = VBUS present status change does produce INT 1h = VBUS present status change does NOT produce INT

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8.5.1.37 REG29_Charger_Mask_1 Register (Offset = 29h) [reset = 0h]

REG29_Charger_Mask_1 is shown in 図 8-61 and described in 表 8-46.

Return to the 表 8-8.

Charger Mask 1

図 8-61. REG29_Charger_Mask_1 Register

7	6	5	4	3	2	1	0
CHG_MASK	ICO_MASK	RESERVED	VBUS_MASK	RESERVED	TREG_MASK	VBAT_PRESENT_MASK	BC1.2_DONE_MASK
R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

表 8-46. REG29_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	CHG_MASK	R/W	0h	Reset by: REG_RST	Charge status mask flag Type : RW POR: 0b 0h = Charging status change does produce INT 1h = Charging status change does NOT produce INT
6	ICO_MASK	R/W	0h	Reset by: REG_RST	ICO status mask flag Type : RW POR: 0b 0h = ICO status change does produce INT 1h = ICO status change does NOT produce INT
5	RESERVED	R	0h		RESERVED
4	VBUS_MASK	R/W	0h	Reset by: REG_RST	VBUS status mask flag Type : RW POR: 0b 0h = VBUS status change does produce INT 1h = VBUS status change does NOT produce INT
3	RESERVED	R	0h		RESERVED
2	TREG_MASK	R/W	0h	Reset by: REG_RST	IC thermal regulation mask flag Type : RW POR: 0b 0h = entering TREG does produce INT 1h = entering TREG does NOT produce INT
1	VBAT_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VBAT present mask flag Type : RW POR: 0b 0h = VBAT present status change does produce INT 1h = VBAT present status change does NOT produce INT
0	BC1.2_DONE_MASK	R/W	0h	Reset by: REG_RST	BC1.2 status mask flag Type : RW POR: 0b 0h = BC1.2 status change does produce INT 1h = BC1.2 status change does NOT produce INT

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8.5.1.38 REG2A_Charger_Mask_2 Register (Offset = 2Ah) [reset = 0h]

REG2A_Charger_Mask_2 is shown in 図 8-62 and described in 表 8-47.

Return to the 表 8-8.

Charger Mask 2

図 8-62. REG2A_Charger_Mask_2 Register

7	6	5	4	3	2	1	0
RESERVED	DPDM_DONE_MASK	ADC_DONE_MASK	VSYS_MASK	CHG_TMR_MASK	TRICHG_TMR_MASK	PRECHG_TMR_MASK	TOPOFF_TMR_MASK
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-47. REG2A_Charger_Mask_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		RESERVED
6	DPDM_DONE_MASK	R/W	0h	Reset by: REG_RST	D+/D- detection is done mask flag Type : RW POR: 0b 0h = D+/D- detection done does produce INT pulse 1h = D+/D- detection done does NOT produce INT pulse
5	ADC_DONE_MASK	R/W	0h	Reset by: REG_RST	ADC conversion mask flag (only in one-shot mode) Type : RW POR: 0b 0h = ADC conversion done does produce INT pulse 1h = ADC conversion done does NOT produce INT pulse
4	VSYS_MASK	R/W	0h	Reset by: REG_RST	VSYS min regulation mask flag Type : RW POR: 0b 0h = enter or exit VSYSMIN regulation does produce INT pulse 1h = enter or exit VSYSMIN regulation does NOT produce INT pulse
3	CHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Fast charge timer mask flag Type : RW POR: 0b 0h = Fast charge timer expire does produce INT 1h = Fast charge timer expire does NOT produce INT
2	TRICHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Trickle charge timer mask flag Type : RW POR: 0b 0h = Trickle charge timer expire does produce INT 1h = Trickle charge timer expire does NOT produce INT
1	PRECHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Pre-charge timer mask flag Type : RW POR: 0b 0h = Pre-charge timer expire does produce INT 1h = Pre-charge timer expire does NOT produce INT
0	TOPOFF_TMR_MASK	R/W	0h	Reset by: REG_RST	Top off timer mask flag Type : RW POR: 0b 0h = Top off timer expire does produce INT 1h = Top off timer expire does NOT produce INT

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8.5.1.39 REG2B_Charger_Mask_3 Register (Offset = 2Bh) [reset = 0h]

REG2B_Charger_Mask_3 is shown in 図 8-63 and described in 表 8-48.

Return to the 表 8-8.

Charger Mask 3

図 8-63. REG2B_Charger_Mask_3 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_MASK	TS_COLD_MASK	TS_COOL_MASK	TS_WARM_MASK	TS_HOT_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-48. REG2B_Charger_Mask_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	RESERVED	R	0h		RESERVED
4	VBATOTG_LOW_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	VBAT too low to enable OTG mask Type : RW POR: 0b 0h = VBAT falling below the threshold to enable the OTG mode, does produce INT 1h = VBAT falling below the threshold to enable the OTG mode, does NOT produce INT
3	TS_COLD_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS cold temperature interrupt mask Type : RW POR: 0b 0h = TS across cold temperature (T1) does produce INT 1h = TS across cold temperature (T1) does NOT produce INT
2	TS_COOL_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS cool temperature interrupt mask Type : RW POR: 0b 0h = TS across cool temperature (T2) does produce INT 1h = TS across cool temperature (T2) does NOT produce INT
1	TS_WARM_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS warm temperature interrupt mask Type : RW POR: 0b 0h = TS across warm temperature (T3) does produce INT 1h = TS across warm temperature (T3) does NOT produce INT
0	TS_HOT_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS hot temperature interrupt mask Type : RW POR: 0b 0h = TS across hot temperature (T5) does produce INT 1h = TS across hot temperature (T5) does NOT produce INT

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8.5.1.40 REG2C_FAULT_Mask_0 Register (Offset = 2Ch) [reset = 0h]

REG2C_FAULT_Mask_0 is shown in 図 8-64 and described in 表 8-49.

Return to the 表 8-8.

FAULT Mask 0

図 8-64. REG2C_FAULT_Mask_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_MASK	VBUS_OVP_MASK	VBAT_OVP_MASK	IBUS_OCP_MASK	IBAT_OCP_MASK	CONV_OCP_MASK	VAC2_OVP_MASK	VAC1_OVP_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 8-49. REG2C_FAULT_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IBAT_REG_MASK	R/W	0h	Reset by: REG_RST	IBAT regulation mask flag Type : RW POR: 0b 0h = enter or exit IBAT regulation does produce INT 1h = enter or exit IBAT regulation does NOT produce INT
6	VBUS_OVP_MASK	R/W	0h	Reset by: REG_RST	VBUS over-voltage mask flag Type : RW POR: 0b 0h = entering VBUS OVP does produce INT 1h = entering VBUS OVP does NOT produce INT
5	VBAT_OVP_MASK	R/W	0h	Reset by: REG_RST	VBAT over-voltage mask flag Type : RW POR: 0b 0h = entering VBAT OVP does produce INT 1h = entering VBAT OVP does NOT produce INT
4	IBUS_OCP_MASK	R/W	0h	Reset by: REG_RST	IBUS over-current mask flag Type : RW POR: 0b 0h = IBUS OCP fault does produce INT 1h = IBUS OCP fault does NOT produce INT
3	IBAT_OCP_MASK	R/W	0h	Reset by: REG_RST	IBAT over-current mask flag Type : RW POR: 0b 0h = IBAT OCP fault does produce INT 1h = IBAT OCP fault does NOT produce INT
2	CONV_OCP_MASK	R/W	0h	Reset by: REG_RST	Converter over-current mask flag Type : RW POR: 0b 0h = Converter OCP fault does produce INT 1h = Converter OCP fault does NOT produce INT
1	VAC2_OVP_MASK	R/W	0h	Reset by: REG_RST	VAC2 over-voltage mask flag Type : RW POR: 0b 0h = entering VAC2 OVP does produce INT 1h = entering VAC2 OVP does NOT produce INT
0	VAC1_OVP_MASK	R/W	0h	Reset by: REG_RST	VAC1 over-voltage mask flag Type : RW POR: 0b 0h = entering VAC1 OVP does produce INT 1h = entering VAC1 OVP does NOT produce INT

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8.5.1.41 REG2D_FAULT_Mask_1 Register (Offset = 2Dh) [reset = 0h]

REG2D_FAULT_Mask_1 is shown in 図 8-65 and described in 表 8-50.

Return to the 表 8-8.

FAULT Mask 1

図 8-65. REG2D_FAULT_Mask_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_MASK	VSYS_OVP_MASK	OTG_OVP_MASK	OTG_UVP_MASK	RESERVED	TSHUT_MASK	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	

表 8-50. REG2D_FAULT_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VSYS_SHORT_MASK	R/W	0h	Reset by: REG_RST	VSYS short circuit mask flag Type : RW POR: 0b 0h = System short fault does produce INT 1h = System short fault does NOT produce INT
6	VSYS_OVP_MASK	R/W	0h	Reset by: REG_RST	VSYS over-voltage mask flag Type : RW POR: 0b 0h = System over-voltage fault does produce INT 1h = System over-voltage fault does NOT produce INT
5	OTG_OVP_MASK	R/W	0h	Reset by: REG_RST	OTG over-voltage mask flag Type : RW POR: 0b 0h = OTG VBUS over-voltage fault does produce INT 1h = OTG VBUS over-voltage fault does NOT produce INT
4	OTG_UVP_MASK	R/W	0h	Reset by: REG_RST	OTG under-voltage mask flag Type : RW POR: 0b 0h = OTG VBUS under voltage fault does produce INT 1h = OTG VBUS under voltage fault does NOT produce INT
3	RESERVED	R/W	0h		RESERVED
2	TSHUT_MASK	R/W	0h	Reset by: REG_RST	IC thermal shutdown mask flag Type : RW POR: 0b 0h = TSHUT does produce INT 1h = TSHUT does NOT produce INT
1-0	RESERVED	R	0h		RESERVED

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8.5.1.42 REG2E_ADC_Control Register (Offset = 2Eh) [reset = 30h]

REG2E_ADC_Control is shown in 図 8-66 and described in 表 8-51.

Return to the 表 8-8.

ADC Control

図 8-66. REG2E_ADC_Control Register

7	6	5	4	3	2	1	0
ADC_EN	ADC_RATE	ADC_SAMPLE_1:0		ADC_AVG	ADC_AVG_INIT	RESERVED	
R/W-0h	R/W-0h	R/W-3h		R/W-0h	R/W-0h	R/W-0h	

表 8-51. REG2E_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_EN	R/W	0h	Reset by: WATCHDOG REG_RST	ADC Control Type : RW POR: 0b 0h = Disable 1h = Enable
6	ADC_RATE	R/W	0h	Reset by: REG_RST	ADC conversion rate control Type : RW POR: 0b 0h = Continuous conversion 1h = One shot conversion
5-4	ADC_SAMPLE_1:0	R/W	3h	Reset by: REG_RST	ADC sample speed Type : RW POR: 11b 0h = 15 bit effective resolution 1h = 14 bit effective resolution 2h = 13 bit effective resolution 3h = 12 bit effective resolution (not recommended)
3	ADC_AVG	R/W	0h	Reset by: REG_RST	ADC average control Type : RW POR: 0b 0h = Single value 1h = Running average (not available for IBAT discharge)
2	ADC_AVG_INIT	R/W	0h	Reset by: REG_RST	ADC average initial value control Type : RW POR: 0b 0h = Start average using the existing register value 1h = Start average using a new ADC conversion
1-0	RESERVED	R/W	0h		RESERVED

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8.5.1.43 REG2F_ADC_Function_Disable_0 Register (Offset = 2Fh) [reset = 0h]

REG2F_ADC_Function_Disable_0 is shown in 図 8-67 and described in 表 8-52.

Return to the 表 8-8.

ADC Function Disable 0

図 8-67. REG2F_ADC_Function_Disable_0 Register

7	6	5	4	3	2	1	0
IBUS_ADC_DIS	IBAT_ADC_DIS	VBUS_ADC_DIS	VBAT_ADC_DIS	VSYS_ADC_DIS	TS_ADC_DIS	TDIE_ADC_DIS	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

表 8-52. REG2F_ADC_Function_Disable_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	IBUS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
6	IBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	IBAT ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
5	VBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	VBUS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	VBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	VBAT ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	VSYS_ADC_DIS	R/W	0h	Reset by: REG_RST	VSYS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
2	TS_ADC_DIS	R/W	0h	Reset by: REG_RST	TS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
1	TDIE_ADC_DIS	R/W	0h	Reset by: REG_RST	TDIE ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
0	RESERVED	R	0h		RESERVED

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8.5.1.44 REG30_ADC_Function_Disable_1 Register (Offset = 30h) [reset = 0h]

REG30_ADC_Function_Disable_1 is shown in 図 8-68 and described in 表 8-53.

Return to the 表 8-8.

ADC Function Disable 1

図 8-68. REG30_ADC_Function_Disable_1 Register

7	6	5	4	3	2	1	0
DP_ADC_DIS	DM_ADC_DIS	VAC2_ADC_DIS	VAC1_ADC_DIS	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			

表 8-53. REG30_ADC_Function_Disable_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DP_ADC_DIS	R/W	0h	Reset by: REG_RST	D+ ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
6	DM_ADC_DIS	R/W	0h	Reset by: REG_RST	D- ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
5	VAC2_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC2 ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	VAC1_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC1 ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3-0	RESERVED	R	0h		RESERVED

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8.5.1.45 REG31_IBUS_ADC Register (Offset = 31h) [reset = 0h]

REG31_IBUS_ADC is shown in 図 8-69 and described in 表 8-54.

Return to the 表 8-8.

IBUS ADC

図 8-69. REG31_IBUS_ADC Register

15	14	13	12	11	10	9	8
IBUS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
IBUS_ADC_15:0							
R-0h							

表 8-54. REG31_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBUS_ADC_15:0	R	0h	IBUS ADC reading Reported in 2 's Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. Type : R POR: 0mA (0h) Range : 0mA-5000mA Fixed Offset : 0mA Bit Step Size : 1mA

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8.5.1.46 REG33_IBAT_ADC Register (Offset = 33h) [reset = 0h]

REG33_IBAT_ADC is shown in 図 8-70 and described in 表 8-55.

Return to the 表 8-8.

IBAT ADC

図 8-70. REG33_IBAT_ADC Register

15	14	13	12	11	10	9	8
IBAT_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
IBAT_ADC_15:0							
R-0h							

表 8-55. REG33_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBAT_ADC_15:0	R	0h	IBAT ADC reading Reported in 2 's Complement. . Type : R POR: 0mA (0h) Range : 0mA-8000mA Fixed Offset : 0mA Bit Step Size : 1mA The IBAT ADC reports the battery charging current in forward mode and the battery discharging current in OTG and battery only (HiZ) mode if EN_BAT bit in REG14[5]=1. The sign bit is 0b for charging current and 1b for discharging current.

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8.5.1.47 REG35_VBUS_ADC Register (Offset = 35h) [reset = 0h]

REG35_VBUS_ADC is shown in 図 8-71 and described in 表 8-56.

Return to the 表 8-8.

VBUS ADC

図 8-71. REG35_VBUS_ADC Register

15	14	13	12	11	10	9	8
VBUS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VBUS_ADC_15:0							
R-0h							

表 8-56. REG35_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS_ADC_15:0	R	0h	VBUS ADC reading. Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.48 REG37_VAC1_ADC Register (Offset = 37h) [reset = 0h]

REG37_VAC1_ADC is shown in 図 8-72 and described in 表 8-57.

Return to the 表 8-8.

VAC1 ADC

図 8-72. REG37_VAC1_ADC Register

15	14	13	12	11	10	9	8
VAC1_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VAC1_ADC_15:0							
R-0h							

表 8-57. REG37_VAC1_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC1_ADC_15:0	R	0h	VAC1 ADC reading Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.49 REG39_VAC2_ADC Register (Offset = 39h) [reset = 0h]

REG39_VAC2_ADC is shown in 図 8-73 and described in 表 8-58.

Return to the 表 8-8.

VAC2 ADC

図 8-73. REG39_VAC2_ADC Register

15	14	13	12	11	10	9	8
VAC2_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VAC2_ADC_15:0							
R-0h							

表 8-58. REG39_VAC2_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC2_ADC_15:0	R	0h	VAC2 ADC reading Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.50 REG3B_VBAT_ADC Register (Offset = 3Bh) [reset = 0h]

REG3B_VBAT_ADC is shown in 図 8-74 and described in 表 8-59.

Return to the 表 8-8.

VBAT ADC

図 8-74. REG3B_VBAT_ADC Register

15	14	13	12	11	10	9	8
VBAT_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VBAT_ADC_15:0							
R-0h							

表 8-59. REG3B_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBAT_ADC_15:0	R	0h	The battery remote sensing voltage (VBATP) ADC reading Type : R POR: 0mV (0h) Range : 0mV-20000mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.51 REG3D_VSYS_ADC Register (Offset = 3Dh) [reset = 0h]

REG3D_VSYS_ADC is shown in 図 8-75 and described in 表 8-60.

Return to the 表 8-8.

VSYS ADC

図 8-75. REG3D_VSYS_ADC Register

15	14	13	12	11	10	9	8
VSYS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VSYS_ADC_15:0							
R-0h							

表 8-60. REG3D_VSYS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VSYS_ADC_15:0	R	0h	VSYS ADC reading Type : R POR: 0mV (0h) Range : 0mV-24000mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.52 REG3F_TS_ADC Register (Offset = 3Fh) [reset = 0h]

REG3F_TS_ADC is shown in 図 8-76 and described in 表 8-61.

Return to the 表 8-8.

TS ADC

図 8-76. REG3F_TS_ADC Register

15	14	13	12	11	10	9	8
TS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
TS_ADC_15:0							
R-0h							

表 8-61. REG3F_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TS_ADC_15:0	R	0h	TS ADC reading Type : R POR: 0% (0h) Range : 0%-99.9023% Fixed Offset : 0% Bit Step Size : 0.0976563%

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8.5.1.53 REG41_TDIE_ADC Register (Offset = 41h) [reset = 0h]

REG41_TDIE_ADC is shown in 図 8-77 and described in 表 8-62.

Return to the 表 8-8.

TDIE_ADC

図 8-77. REG41_TDIE_ADC Register

15	14	13	12	11	10	9	8
TDIE_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
TDIE_ADC_15:0							
R-0h							

表 8-62. REG41_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TDIE_ADC_15:0	R	0h	TDIE ADC reading Reported in 2 's Complement. Type : R POR: 0°C (0h) Range : -40°C-150°C Fixed Offset : 0°C Bit Step Size : 0.5°C

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8.5.1.54 REG43_D+_ADC Register (Offset = 43h) [reset = 0h]

REG43_D+_ADC is shown in 図 8-78 and described in 表 8-63.

Return to the 表 8-8.

D+ ADC

図 8-78. REG43_D+_ADC Register

15	14	13	12	11	10	9	8
D+_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
D+_ADC_15:0							
R-0h							

表 8-63. REG43_D+_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D+_ADC_15:0	R	0h	D+ ADC reading Type : R POR: 0mV (0h) Range : 0mV-3600mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.55 REG45_D-_ADC Register (Offset = 45h) [reset = 0h]

REG45_D-_ADC is shown in 図 8-79 and described in 表 8-64.

Return to the 表 8-8.

D- ADC

図 8-79. REG45_D-_ADC Register

15	14	13	12	11	10	9	8
D-_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
D-_ADC_15:0							
R-0h							

表 8-64. REG45_D-_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D-_ADC_15:0	R	0h	D- ADC reading Type : R POR: 0mV (0h) Range : 0mV-3600mV Fixed Offset : 0mV Bit Step Size : 1mV

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8.5.1.56 REG47_DPDM_Driver Register (Offset = 47h) [reset = 0h]

REG47_DPDM_Driver is shown in 図 8-80 and described in 表 8-65.

Return to the 表 8-8.

DPDM Driver

図 8-80. REG47_DPDM_Driver Register

7	6	5	4	3	2	1	0
DPLUS_DAC_2:0			DMINUS_DAC_2:0			RESERVED	
R/W-0h			R/W-0h			R/W-0h	

表 8-65. REG47_DPDM_Driver Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DPLUS_DAC_2:0	R/W	0h	D+ Output Driver Type : RW POR: 000b 0h = HIZ 1h = 0 2h = 0.6V 3h = 1.2V 4h = 2.0V 5h = 2.7V 6h = 3.3V 7h = D+/D- Short
4-2	DMINUS_DAC_2:0	R/W	0h	D- Output Driver Type : RW POR: 000b 0h = HIZ 1h = 0 2h = 0.6V 3h = 1.2V 4h = 2.0V 5h = 2.7V 6h = 3.3V 7h = reserved
1-0	RESERVED	R/W	0h	RESERVED

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8.5.1.57 REG48_Part_Information Register (Offset = 48h) [reset = 33h]

REG48_Part_Information is shown in 図 8-81 and described in 表 8-66.

Return to the 表 8-8.

Part Information

図 8-81. REG48_Part_Information Register

7	6	5	4	3	2	1	0
RESERVED		PN_2:0				DEV_REV_2:0	
R-0h		R-4h				R-1h	

表 8-66. REG48_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-3	PN_2:0	R	4h	Device Part Number 100b = BQ25672 All other options are reserved.
2-0	DEV_REV_2:0	R	1h	Device Revision 001b = BQ25672 All other options are reserved.

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9 Application and Implementation

注

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9.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a multi-cell battery charger for Li-Ion and Li-polymer batteries. It integrates the four switching MOSFETs for the converter, and the battery FET (BATFET) between system and battery. The device also integrates the input current sensing and charging current sensing circuitries, the bootstrap diode for the high-side gate driving and the dual-input power mux for the power sources selection.

The charger's MPPT algorithm allows a simple but efficient interface between the charger and a small photovoltaic panel. The power mux may optionally be used to add a secondary charging port such as a barrel jack or USB input.

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9.2 Typical Application

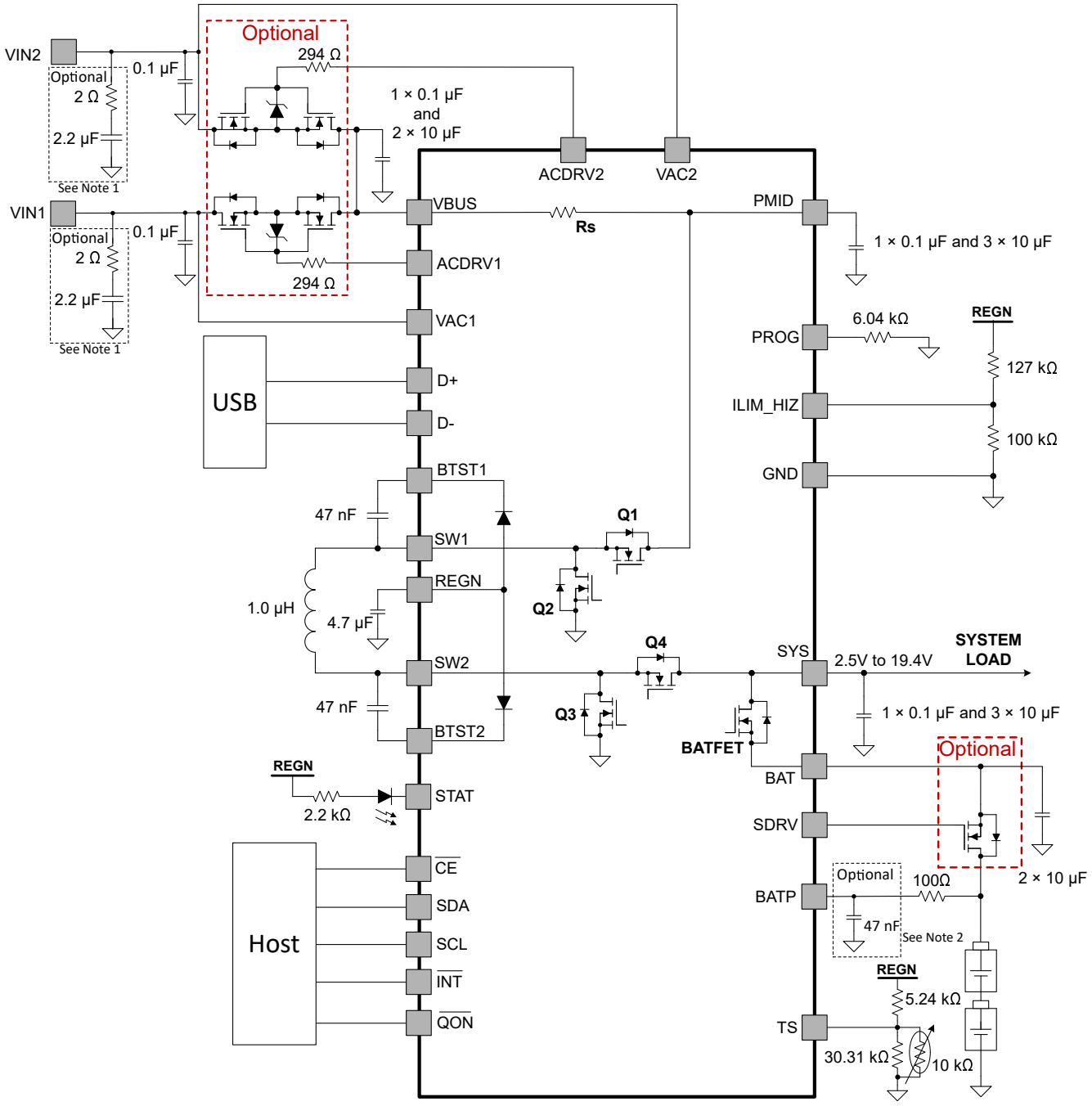

図 9-1. BQ25672 Application Diagram with Two Input Sources and Ship FET

1. Recommended if hot plugging adapters > 15 V.
2. Recommended if hot plugging 4S battery packs with long leads or PCB traces.

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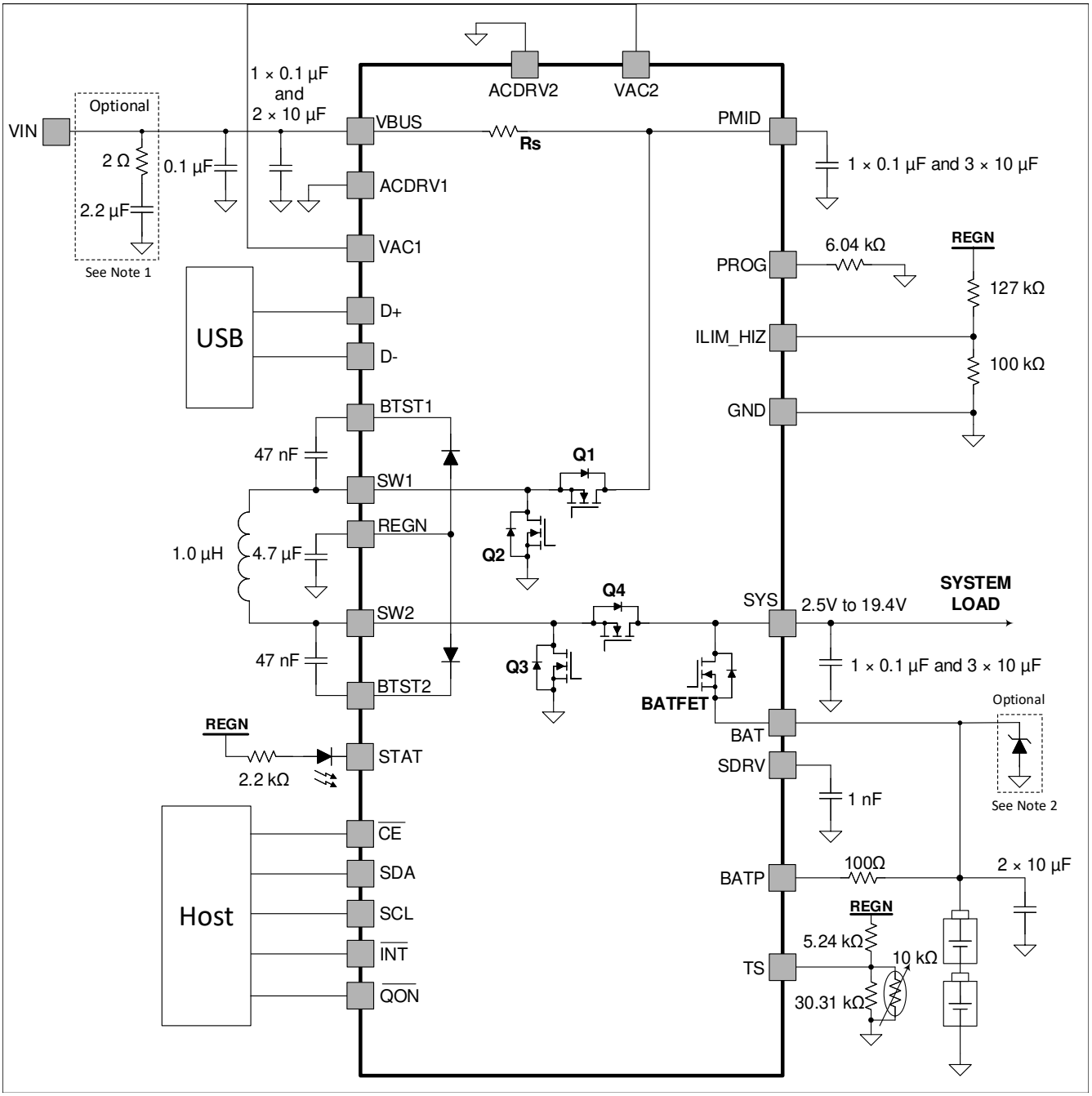

図 9-2. BQ25672 Application Diagram with Single Input Source and No Ship FET

1. Recommended if hot plugging adapters > 15 V.
2. Recommended if hot plugging 4S battery packs with long leads or PCB traces.

9.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

表 9-1. Design Parameters

PARAMETER	VALUE
VBUS voltage range	9 V to 20 V
PV panel voltage	V_{OC} = 10 V_{MPP} = 8 V
Secondary adapter voltage range	9 V to 20 V
Input current limit (IINDPM[8:0])	3.0 A
Fast charge current limit (ICHG[8:0])	3.0 A
Battery regulation voltage (VREG[10:0])	8.4 V
Enable MPPT (EN_MPPT[0])	1
VOC measure internval (VOC_RATE[1:0])	2 min
VOC measure delay (VOC_DLY[1:0])	300 ms
VOC percent for MPP (VOC_PCT[2:0])	0.8125

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor (1µH) and capacitor values. It also provide the 750kHz switching frequency to achieve higher efficiency for the applications which have enough design space to accommodate the larger inductor (2.2 µH) and capacitors. Please note that the 1.5 MHz switching frequency only works with the 1µH inductor and the 750 kHz switching frequency only works with the 2.2µH inductor.

Because the converter might be either operated in the buck mode or the boost mode, so the inductor current is equal to either the charging current or the input current. The inductor saturation current should be higher than the larger value of the input current (I_{IN}) or the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq MAX\left[\left(I_{IN} + \frac{I_{RIPPLE}}{2}\right), \left(I_{CHG} + \frac{I_{RIPPLE}}{2}\right)\right] \tag{4}$$

The inductor ripple current (I_{RIPPLE}) depends on the input voltage (V_{BUS}), the output voltage (V_{SYS}), the switching frequency (F_{SW}) and the inductance (L). The inductor current ripples for buck mode and boost mode are calculated with equations (4) and (5), respectively:

$$I_{RIPPLE_BUCK} = \frac{V_{SYS} \times (V_{BUS} - V_{SYS})}{V_{BUS} \times F_{SW} \times L} \tag{5}$$

$$I_{RIPPLE_BOOST} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times F_{SW} \times L} \tag{6}$$

The inductor current ripple in the buck mode is usually larger than that in the boost mode, since the voltage-second applied on the inductor is larger. The maximum inductor current ripple in the buck mode happens in the vicinity of D = V_{SYS} / V_{BUS} = 0.5. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case for the inductor ripples is with the 15V or 20V input voltage.

9.2.2.2 Input (VBUS / PMID) Capacitor

In the buck mode operation, the input current is discontinuous, which dominates the input RMS ripple current and input voltage ripple. The input capacitors should have enough ripple current rating to absorb the input AC current and have large enough capacitance to maintain the small input voltage ripple. For the buck mode

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operation, the input RMS ripple current is calculated by the equation (6) and the input voltage ripple is calculated by the equation (7), where D = V_{SYS} / V_{BUS}.

$$I_{CIN_BUCK} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{7}$$

$$\Delta V_{IN_BUCK} = \frac{D \times (1 - D) \times I_{CHG}}{C_{IN} \times F_{SW}} \tag{8}$$

The worst case input RMS ripple current and input voltage ripple both occur at 0.5 duty cycle condition. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is when 15V to 20V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 25V or higher voltage rating is preferred for up to 20V input voltage. 1*0.1 µF + 3*10 µF ceramic capacitors are suggested for up to 3.3-A input current limit to support the converter in forward mode.

9.2.2.3 Output (VSYS) Capacitor

In the boost mode operation, the output current is discontinuous, which dominates the output RMS ripple current and output voltage ripple. The output capacitors should have enough ripple current rating to absorb the output AC current and have large enough capacitance to maintain the small output voltage ripple. For the boost mode operation, the output RMS ripple current is calculated by the equation (8) and the output voltage ripple is calculated by the equation (9), where D = (1 - V_{BUS} / V_{SYS}).

$$I_{COUT_BOOST} = I_{CHG} \times \sqrt{\frac{D}{(1 - D)}} \tag{9}$$

$$\Delta V_{OUT_BOOST} = \frac{I_{CHG} \times D}{C_{OUT} \times F_{SW}} \tag{10}$$

The worst case output RMS ripple current and output voltage ripple both occur at the lowest VBUS input voltage. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is 5V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the output decoupling capacitor and should be placed close to the SYS and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 16V or higher voltage rating is preferred for the 2s battery configuration. 1*0.1 µF + 3*10 µF capacitors are suggested for up to 3A charging current.

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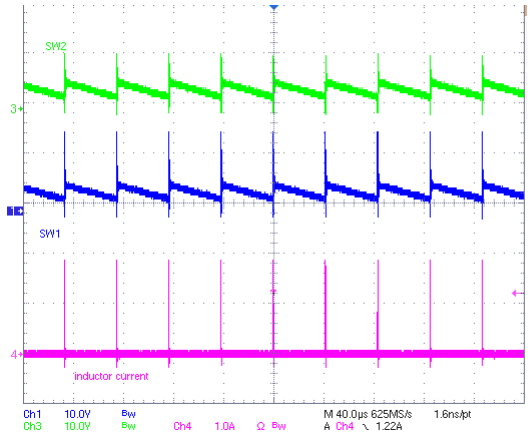
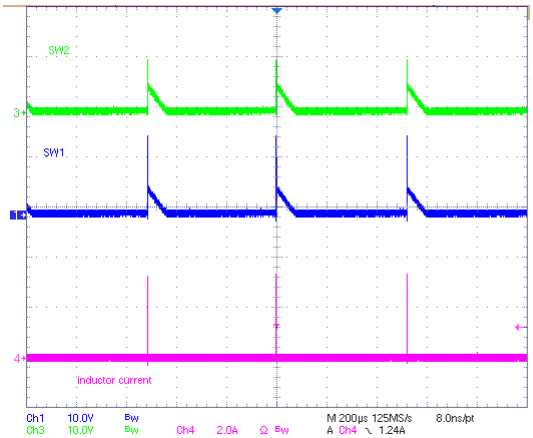
9.2.3 Application Curves

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120), Fsw = 1.5MHz.



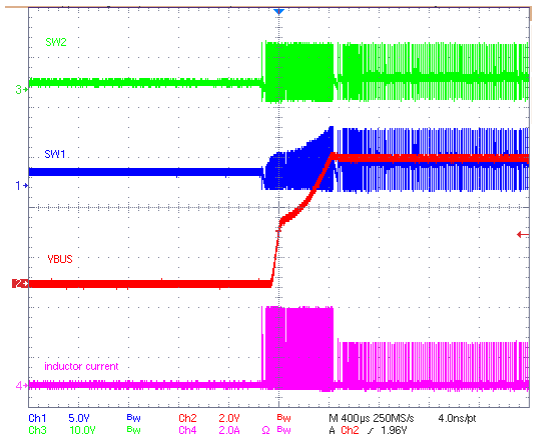
VBUS = 15V VBAT = 8V ICHG = 0A

図 9-3. Buck Mode PFM with OOA



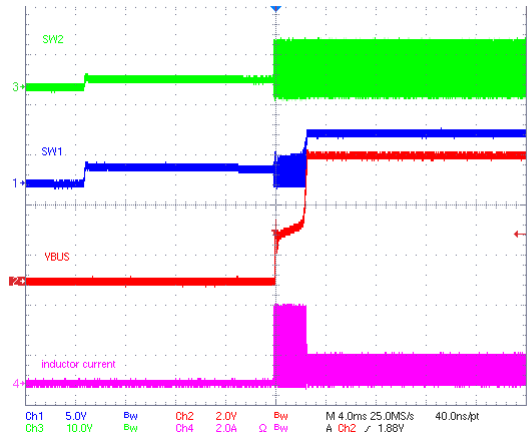
VBUS = 15V VBAT = 8V ICHG = 0A

図 9-4. Buck Mode PFM without OOA



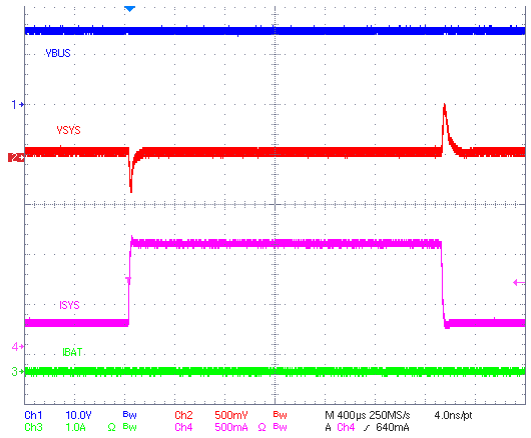
VBAT = 8V VOTG = 5V IBUS = 0A

図 9-5. OTG Startup at No Load



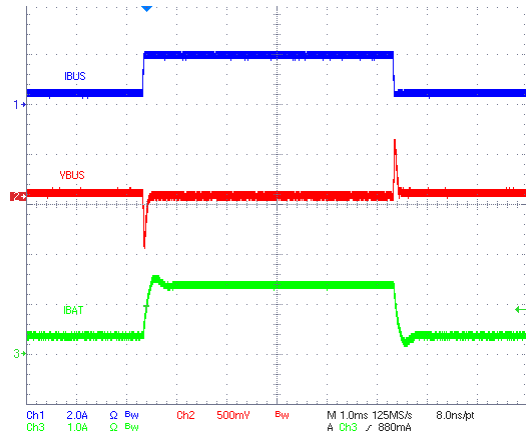
VBAT = 8V VOTG = 5V IBUS = 500mA

図 9-6. OTG Startup at 500-mA Load



VBUS = 15V VBAT = 8V Charge disabled

図 9-7. VSYS Load Transient Response



VBAT = 8V VOTG = 5V

図 9-8. VOTG Load Transient Response

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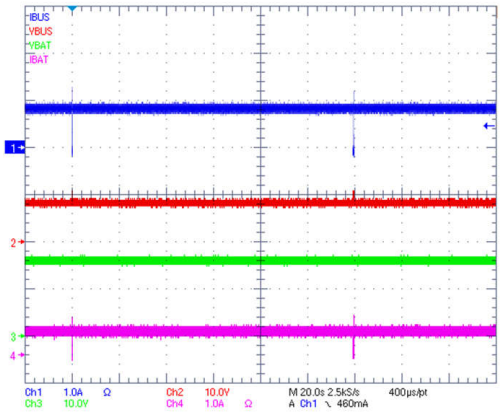
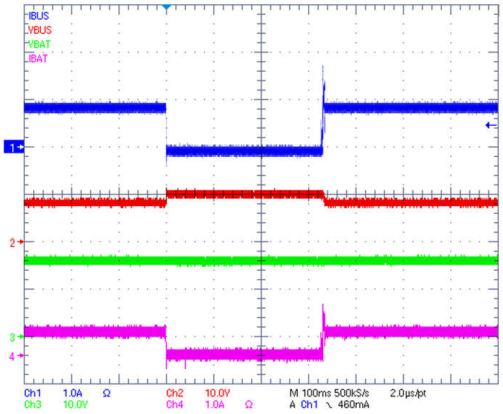


VOC = 10V VMPP = 8.1V VBAT = 8V

図 9-9. MPPT Operation



VOC = 10V VMPP = 8.1V VBAT = 8V

図 9-10. MPPT Operation Zoom

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.6 V and 24 V input with recommended >500mA current rating connected to VBUS or a 1s to 4s Li-Ion battery with voltage higher than V_{BAT_UVLO} connected to BAT. The source current rating needs to be at least 3A for the converter of the charger to provide maximum output power to SYS.

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11 Layout

11.1 Layout Guidelines

The switching nodes rising and falling times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loops (shown in the figure below) is important to prevent the electrical and magnetic field radiation and the high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the SYS output capacitors as close to SYS and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place the PMID input capacitors as close to PMID and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
3. Place the VBUS input capacitors as close to VBUS and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. The connection from SYS/PMID/VBUS to the 0.1 µF has to be routed on the top layer of the PCB, the returning back to GND also has to be in the top layer. Keep the whole routing loop as small as possible.
5. Place the inductor input terminal to SW1 and the inductor output terminal to SW2 as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the inductor current. Minimize parasitic capacitance from this area to any other trace or plane.
6. Place the BAT capacitors close to BAT and GND, place the VBUS capacitors close to VBUS and GND.
7. The REGN decoupling capacitor and the bootstrap capacitors should be placed next to the IC and make trace connection as short as possible.
8. Ensure that there are sufficient thermal vias directly under the power MOSFETs, connecting to copper on other layers.
9. Via size and number should be enough for a given current path.
10. Route BATP away from switching nodes such as SW1 and SW2.

Refer to the EVM design and more information in the *BQ25672EVM (BMS027) Evaluation Module User's Guide* for the recommended component placement with trace and via locations.

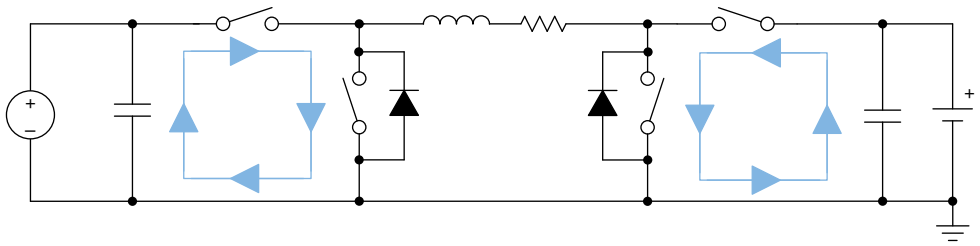

図 11-1. Buck-Boost Converter High Frequency Current Path

11.2 Layout Example

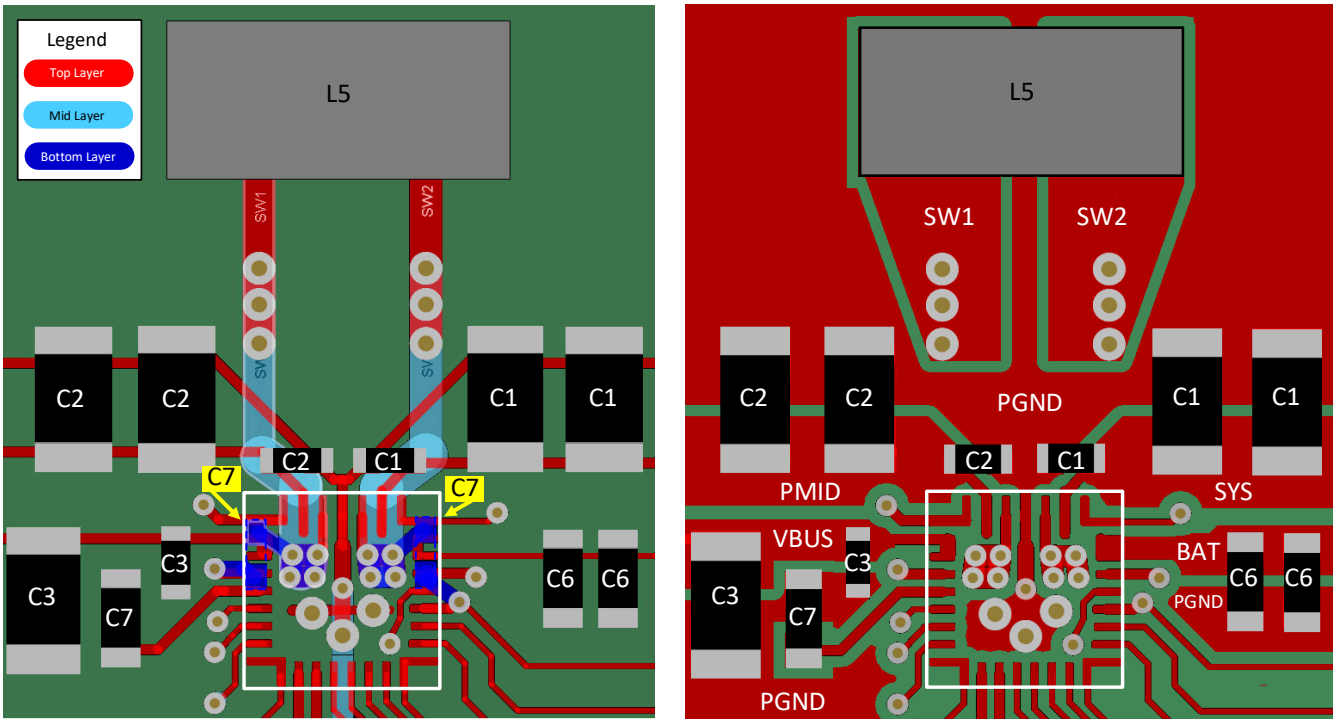

図 11-2. PCB Layout Example (Top Layer Copper Pours Removed on Left, Shown on Right)

図 11-2 shows the recommended placement and routing of external components. The components are labelled with "R," "C" or "L" to indicate resistor, capacitor or inductor and a number that corresponds to the numbered list in セクション 11.1. Since the layout guidelines are listed in priority order, this number also provides a priority for component placement.

The placement of C1 and C2 0.1 µF PMID and SYS capacitors is critical for noise filtering. They should be placed on the same layer as the BQ25672, as close to the IC as possible. This will generally require that the traces to connect SW1 and SW2 to the inductor are routed on a different layer.

The SW1 and SW2 pins are routed to vias placed under the IC and then back out on an inner PCB layer. This supports the tightest placement of C1 and C2 capctiors as described above. These vias are also used to route to the C7 BTST1 and BTST2 capactiors on the bottom layer as shown.

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12 Device and Documentation Support

12.1 Device Support

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *BQ25672EVM (BMS027) Evaluation Module User's Guide*

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12.7 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25672RQMR	Active	Production	VQFN-HR (RQM) | 29	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BQ25672
BQ25672RQMR.A	Active	Production	VQFN-HR (RQM) | 29	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BQ25672
BQ25672RQMR.B	Active	Production	VQFN-HR (RQM) | 29	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	BQ25672

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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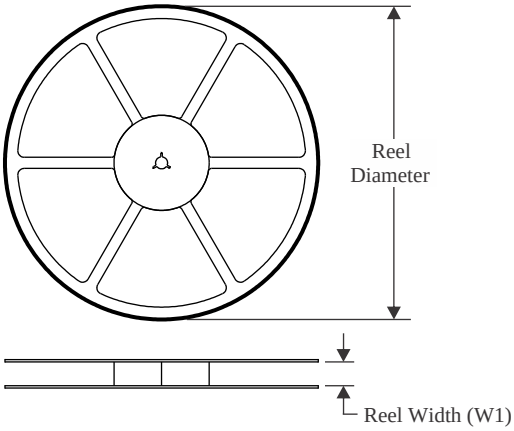
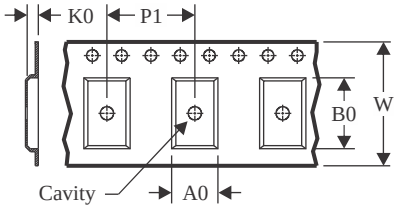
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

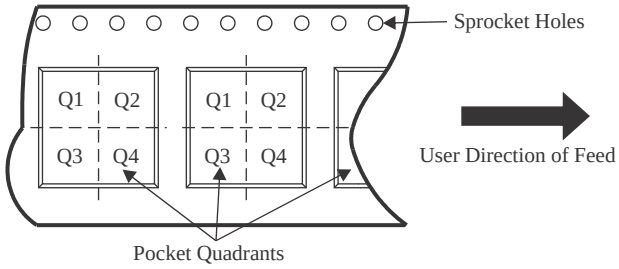


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

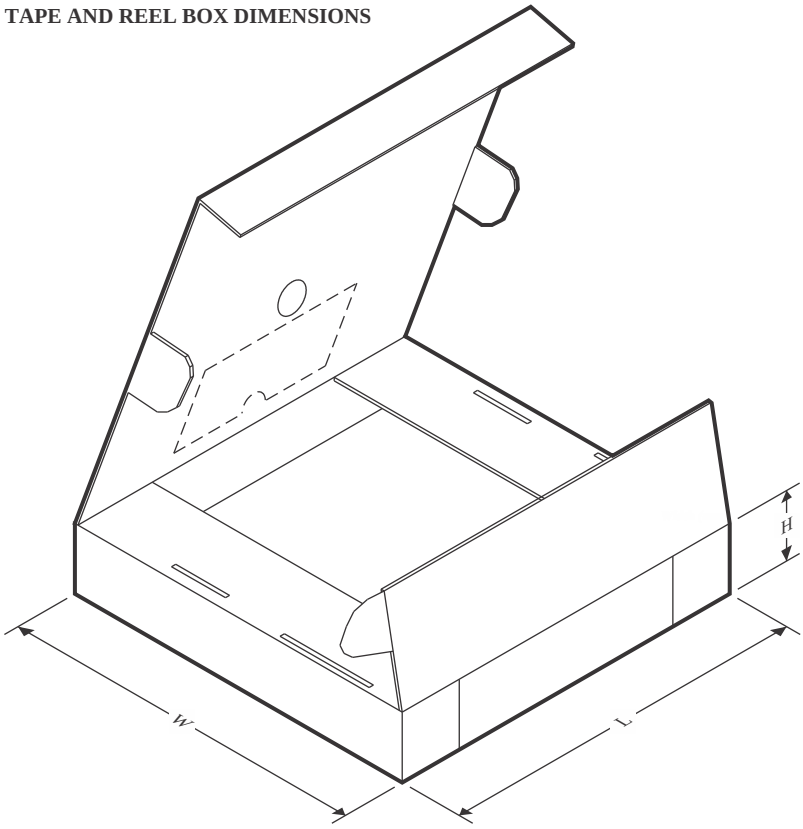
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25672RQMR	VQFN-HR	RQM	29	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

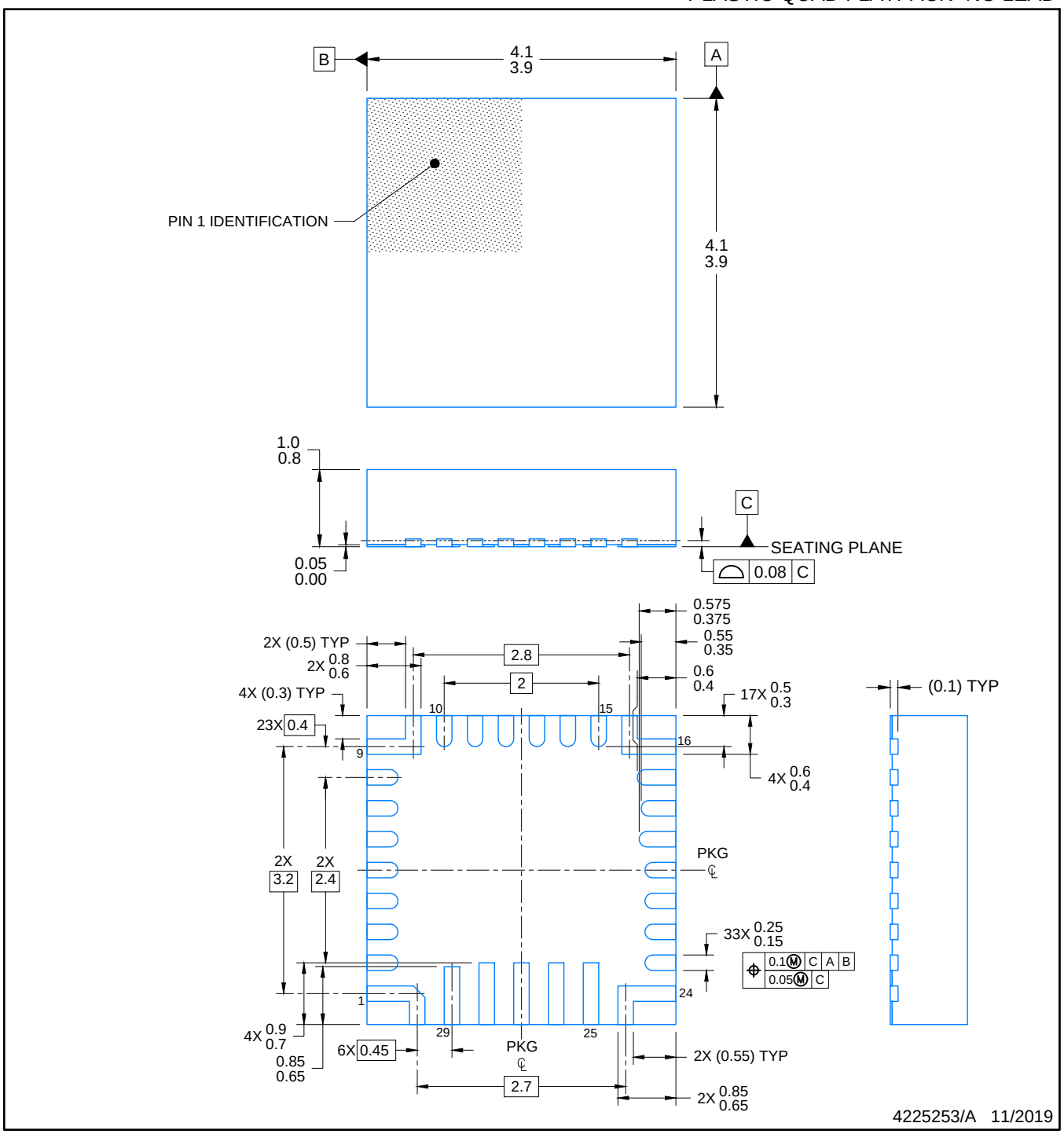
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25672RQMR	VQFN-HR	RQM	29	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RQM0029A

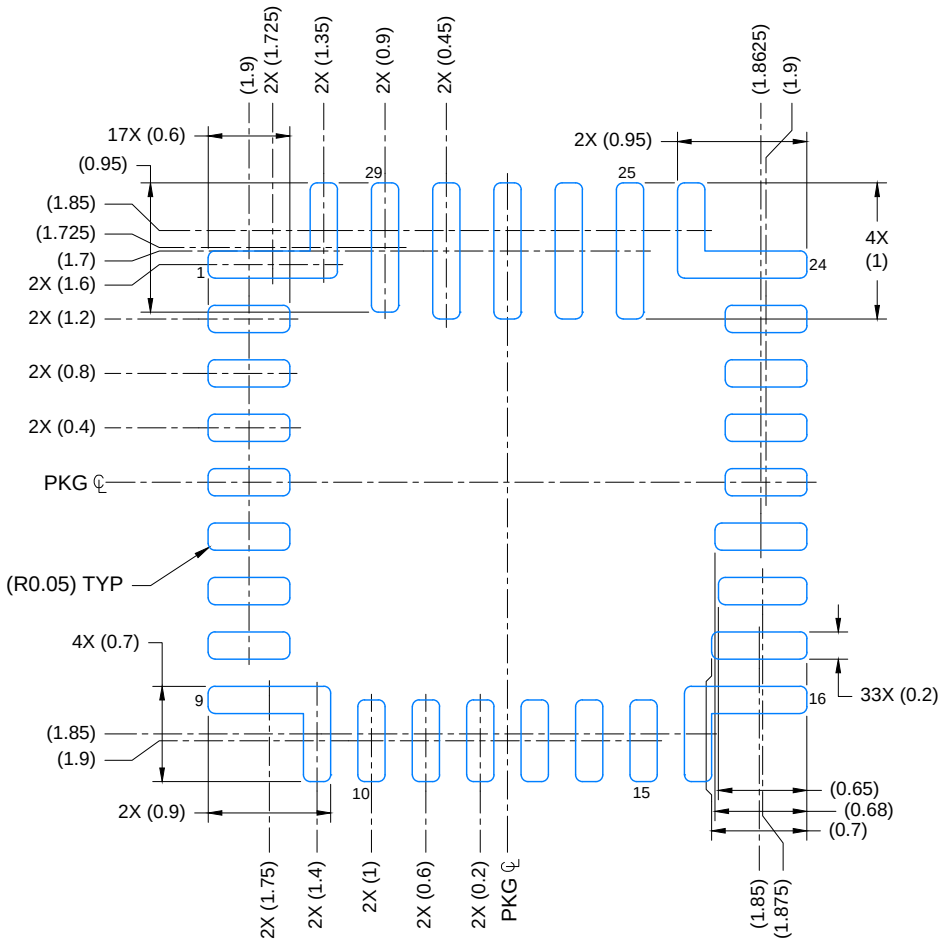
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

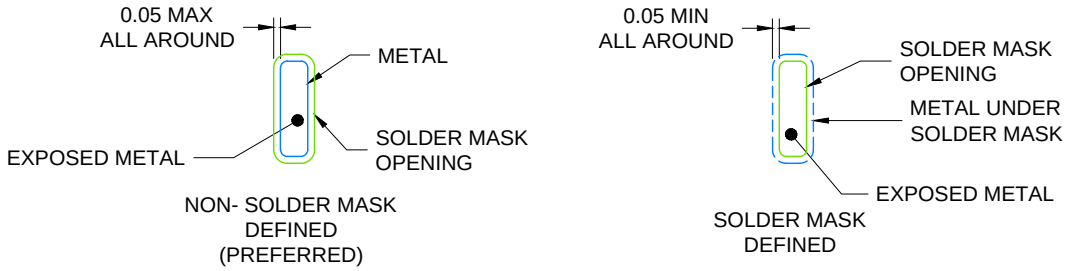
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



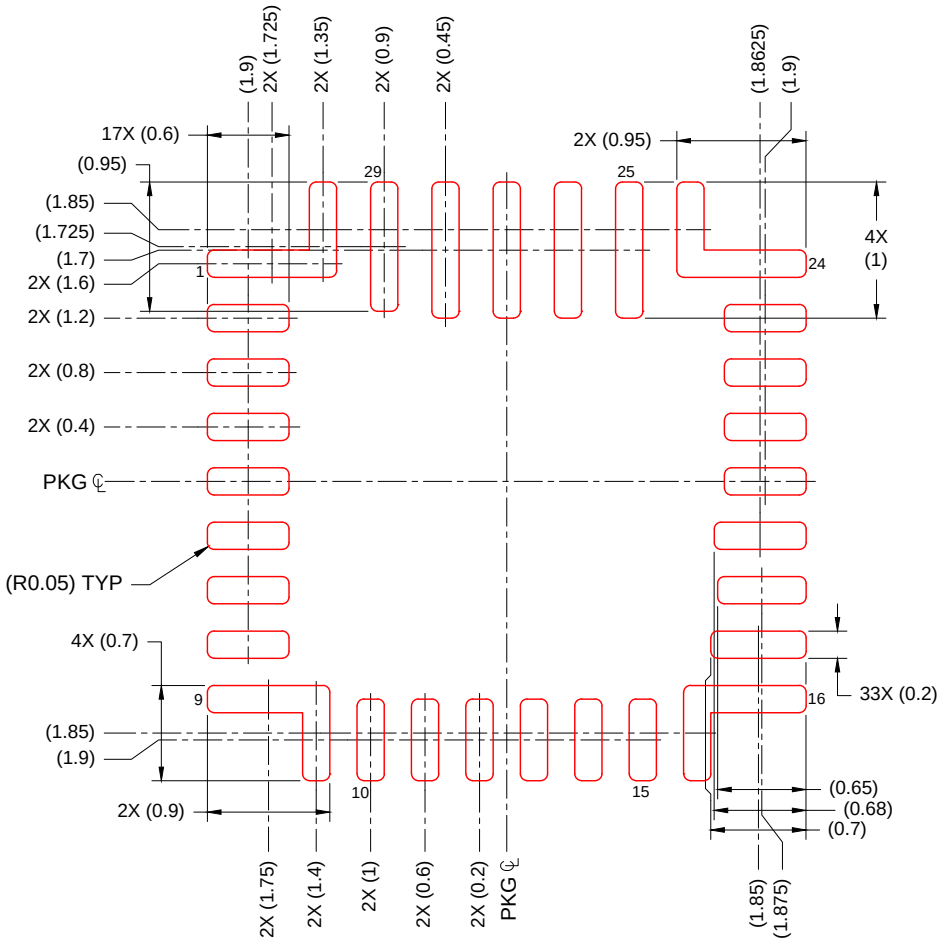
SOLDER MASK DETAILS

NOT TO SCALE

4225253/A 11/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
SCALE: 18X

4225253/A 11/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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