BQ25968 I²C 制御シングル・セル高効率 6A スイッチト・キャパシタ高速充電器、ADC 付き

1 特長

- 97% 効率の電力段により 6-A の高速充電を実現
- 50% デューティ・サイクルに最適化された特許出願中のスイッチト・キャパシタ・チャージャ・アーキテクチャ
  - 入力電圧はバッテリ電圧の 2 倍 (3.5V～4.65V)
  - 出力電流は入力電流の 2 倍 (最大 4.5A)
  - ケーブル全体の電力損失を低減
- 安全な動作の実現に役立つ、プログラマブルな各種保護機能を内蔵
  - 入力過電圧保護 (BUS_OVP)
  - 可変アラーム付き入力過電流保護 (BUS_OCP)
  - 外付け OVP FET による入力過電圧保護 (VAC_OVP、最大 17V)
  - 可変アラーム付きバッテリ過電圧保護 (BAT_OVP)
  - 出力過電圧 (VOUT_OVP)
  - 可変アラーム付き入力過電流保護 (BUS_OCP)
  - 可変アラーム付き IBAT 過電流保護 (BAT_OCP)
  - スイッチング MOSFET のサイクル単位の電流制限
  - バッテリ温度監視
  - コネクタ温度監視
- プログラム可能な設定によるシステム最適化
  - 割り込み用の STAT、FLAG、MASK オプション
  - ADC の読み取りと構成
- 16 ビット有効アナログ / デジタル・コンバータ (ADC) を内蔵
  - BUS 電圧:±0.5%
  - VOUT 電圧:±0.5%
  - 差動センシングによる BAT 電圧:–0.4%～0.2%
  - 外付け R_{SENSE} による 6A 時の BAT 電流:±1.5%
  - BAT 温度:±1%
  - BUS 温度:±1%
  - ダイ温度:±4℃

2 アプリケーション

- スマートフォン
- タブレット PC

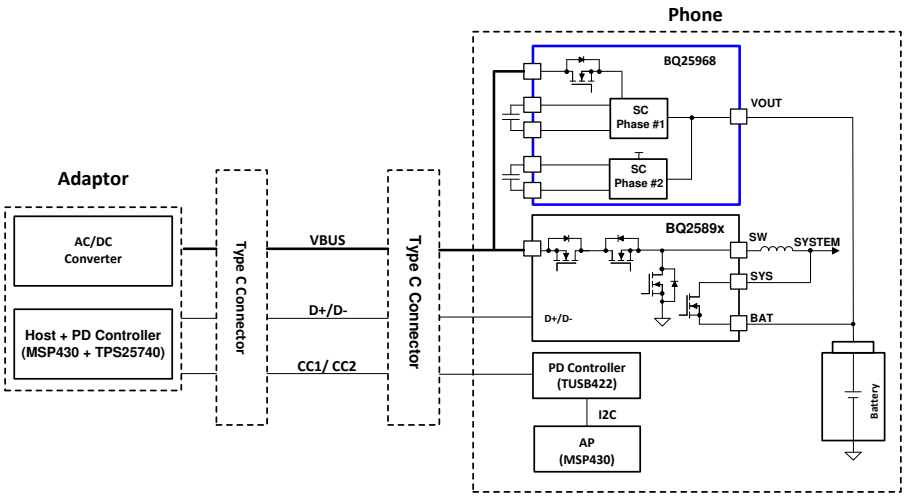
3 概要

BQ25968 は、スイッチト・キャパシタ・アーキテクチャを採用した 97% 効率の 6-A バッテリ充電ソリューションです。このアーキテクチャと内蔵 FET はデューティ・サイクル 50% を達成するように最適化されているため、ケーブル電流をバッテリに供給される電流の半分にし、充電ケーブルでの損失を低減するとともにアプリケーションの温度上昇を制限することができます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
BQ25968	DSBGA (56)	3.00mm × 3.20mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



簡略化されたアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2020) to Revision A (February 2021)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• 「特長」で「50% デューティ・サイクルに最適化されたスイッチト・キャパシタ・チャージャ・アーキテクチャ」を「50% デューティ・サイクルに最適化された特許出願中のスイッチト・キャパシタ・チャージャ・アーキテクチャ」に変更	1

5 概要 (続き)

デュアルフェーズ・アーキテクチャにより、充電効率が上がり、入力と出力のコンデンサ要件は緩和されます。BQ25790 のようなメインの充電器を組み合わせた場合、プリチャージから定電流充電、定電圧充電、充電終了まで、最低水準の電力損失で極めて高速に充電できます。

デュアルフェーズ・アーキテクチャにより、入力コンデンサ要件は緩和され、出力電圧リップルは低減します。BQ2589x のような標準の充電器を組み合わせた場合、プリチャージから定電流充電、定電圧充電、充電終了まで、最低水準の電力損失で極めて高速に充電できます。

このデバイスには、入力過電圧 / 過電流保護、出力過電圧 / 過電流保護、バッテリおよびケーブルの温度センシング、ダイ温度の監視など、安全な充電を保証するために必要なあらゆる保護機能が内蔵されています。

また、12 ビット有効アナログ / デジタル・コンバータ (ADC) を搭載しているため、バス電圧、バス電流、出力電圧、バッテリ電圧、バッテリ電流、バス温度、バッテリ温度、ダイ温度など、スマート AC アダプタやパワー・バンクからのバッテリ充電の管理に必要な測定計算値が得られます。

6 Device Comparison Table

FUNCTION	BQ25970	BQ25971	BQ25968
Device ID	0000	0001	0110
External OVPFET Control	Yes. VAC up to 40 V	No	Yes. VAC up to 40 V
IBAT, VBAT regulation	Yes, through external OVPFET	No	No
VDROP OVP protection during regulation	Yes	No	No
Recommended charging current	8A	8A	6A

7 Pin Configuration and Functions

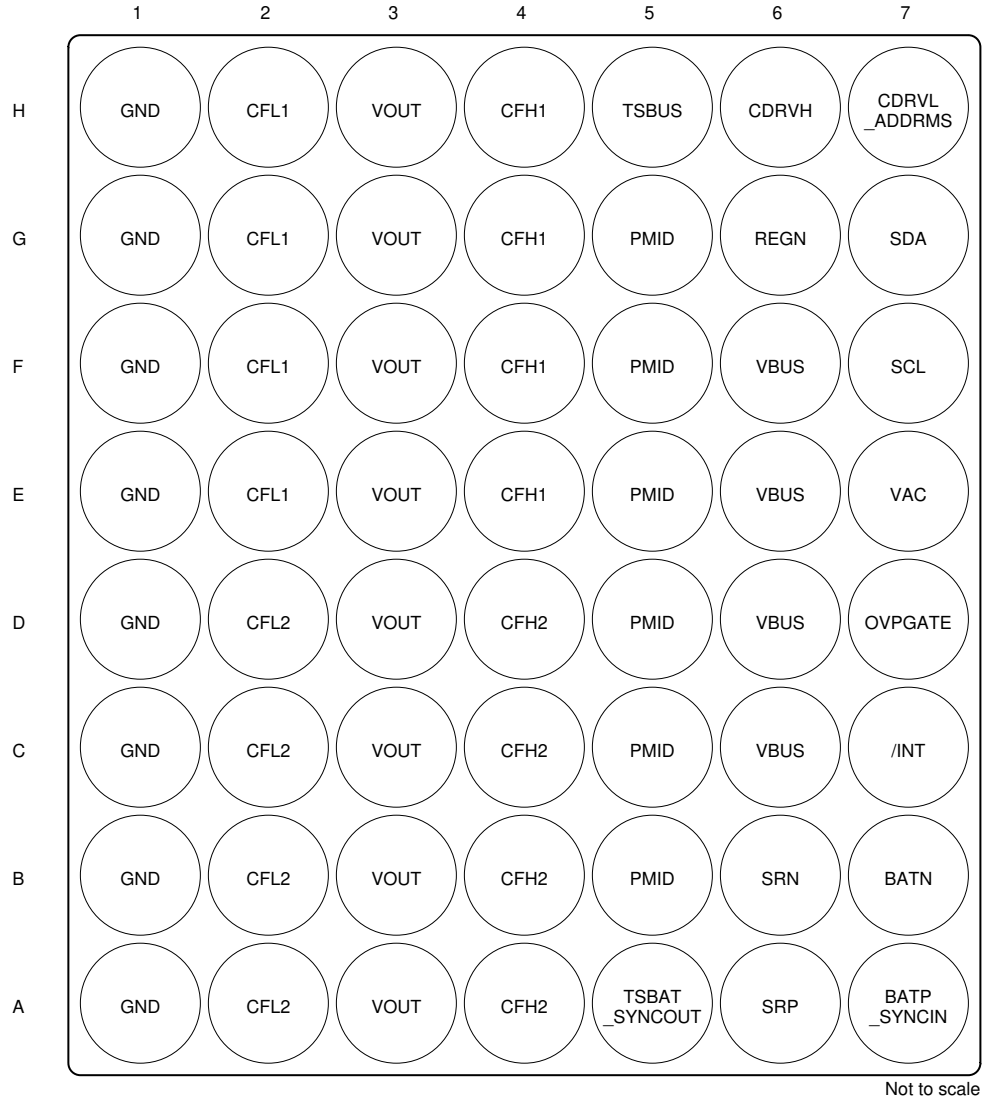


図 7-1. YFF Package 56-Pin DSBGA Bottom View

表 7-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1, B1, C1, D1, E1, F1, G1, H1	GND	P	Power ground.
A2, B2, C2, D2	CFL2	P	Switched cap flying cap connection. Connect three 22-µF capacitors in parallel between this pin and CFH2.
A3, B3, C3, D3, E3, F3, G3, H3	VOUT	P	Device power output. Connect a 22-µF capacitor between this pin and GND.
A4, B4, C4, D4	CFH2	P	Switched cap flying cap connection. Connect a three 22-µF capacitors in parallel between this pin and CFL2. Other capacitor values and number can be used, and will affect VOUT ripple and efficiency.
A5	TSBAT_SYNCOUT	AIO	Battery temperature voltage input and Master Mode SYNCOUT. Requires external resistor divider, NTC, and voltage reference. See the TSBAT section for choosing the resister divider values. If the device is in Master Mode, connect this pin to SYNCIN of the Slave device.
A6	SRP	AI	Positive input for low side battery current sensing. Place a 2-mΩ or 5-mΩ R_{SENSE} between SRN and SRP. Short to SRN and SRP together and GND if not used. Since the device senses the current by measuring the voltage drop across R_{SENSE}, if other than 2-mΩ or 5-mΩ R_{SENSE} is used, the host device will have to scale the IBAT_ADC reading appropriately.
A7	BATP_SYNCIN	AI	Positive input for battery voltage sensing. Connect to positive terminal of battery pack. Place 100-Ω to 1-kΩ series resistance between pin and positive terminal. If configured as a Slave for parallel configuration, this pin functions as SYNCIN, and connect to SYNCOUT of Master, and connect a 1-kΩ pullup resistor to REGN.
B5, C5, D5, E5, F5, G5	PMID	P	PMID is the input to the switched cap power stage. Connect 10-µF cap to PMID.
B6	SRN	AI	Negative input for low side battery current sensing. Place a 2-mΩ or 5-mΩ R_{SENSE} between SRN and SRP. Short to SRP and SRN together and to GND if not used.
B7	BATN	AI	Negative input for batter voltage sensing. Connect to negative terminal of battery pack. Place 100-Ω/1-k series resistance between pin and negative terminal.
C6, D6, E6, F6	VBUS	P	Device power input. Place a 1-µF bypass cap to GND as close as possible to these pins.
C7	$\overline{INT}$	DO	Open drain, active low interrupt output. Pull up to voltage with 10-kΩ resistor. Normally high, the device asserts low to report status and faults. $\overline{INT}$ is pulsed low for t_{INT}.
D7	OVPGATE	AO	External OVP FET N-channel gate drive pin. A minimum of 8-nC of capacitance is required from the OVP FET Gate to Source. Float if not in use.
E2, F2, G2, H2	CFL1	P	Switched cap flying cap connection. Connect three 22-µF caps in parallel between this pin an CFH1. Other capacitor values and number can be used, and will affect VOUT ripple and efficiency.
E4, F4, G4, H4	CFH1	P	Switched cap flying cap connection. Connect three 22-µF caps in parallel between this pin and CFL1. Other capacitor values and number can be used, and will affect VOUT ripple and efficiency.
E7	VAC	AI	Device power input. Tie to VBUS if BQ25971 (no external OVP FET).
F7	SCL	DIO	I^2C interface data. Pull up to voltage with 1-kΩ resistor.
G6	REGN	AO	LDO output. Connect a 4.7-µF cap between this pin and GND.
G7	SDA	DI	I^2C interface clock. Pull up to voltage with 1-kΩ resistor.
H5	TSBUS	AI	BUS temperature voltage input. Requires external resistor divider, NTC, and voltage reference.
H6	CDRVH	AIO	Charge pump for gate drive. Connect a 0.22-µF cap between CDRVH and CDRVL.

表 7-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
H7	CDRVL_ADDRMS	AIO	Charge pump for gate drive. Connect a 0.22-µF cap between CDRVH and CDRVL. During POR, this pin is used to assign the address of the device and the mode of the device as Standalone, Master, or Slave. See 表 9-2 in セクション 9.3.10 for a table of functionality.

(1) Type: P = Power , AIO = Analog Input/Output , AI = Analog Input, DO = Digital Output, AO = Analog Output, DIO = Digital Input/Output

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VAC	–2	40	V
Voltage	VBUS	–2	20	V
	PMID	–0.3	20	V
	CFL1, CFL2, VOUT	–1.4	7	V
	SRP, SRN	–0.3	1.8	V
	BATP_SYNCIN, BATN	–0.3	6	V
	OVPGATE - VBUS	–0.3	14	V
	$\overline{INT}$, SDA, SCL, CDRVL_ADDRMS, REGN	–0.3	6	V
	CDRVH	–0.3	20	V
	TSBUS, TSBAT_SYNCOUT	–0.3	6	V
Voltage	CFH1, CFH2, while maintaining CFH-VOUT = 7VMAX	0	14	V
Maximum Voltage Difference	SRP-SRN	–0.5	0.5	V
	VOUT - VBUS	–16	6	V
Output Sink Current	$\overline{INT}$		6	mA
Junction Temperature, T_J		–40	150	°C
Storage Temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VAC		12	V
	VBUS		12	V
	VOUT	3	6	V
	CFH1-VOUT, CFL1, CFH2-VOUT, CFL2		7	V
	BATP_SYNCIN, BATN	0	6	V
	SRP-SRN	–0.05	0.05	V
	SRN	–0.1		V
	TSBAT_SYNCOUT, TSBUS	0	3	V
	SDA, SCL, CDRVL_ADDRMS, $\overline{INT}$, $\overline{CHGSTAT}$	0	5	V
I_{VOUT} Current		0	8	A

8.4 Thermal Information

THERMAL METRIC		BQ25968 YFF (DSBGA) 56 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.2	°C/W
ω_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ω_{JB}	Junction-to-board characterization parameter	10.4	°C/W

8.5 Electrical Characteristics

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{Q_VBUS}	VBUS Operating Quiescent Current	ADC Disabled, Charge Disabled, OVPGATE not used		285		µA
		ADC Disabled, Charge Disabled, OVPGATE used		345		µA
		ADC Enabled (fastest mode), Charge Disabled		400		µA
		ADC Enabled (slowest mode), Charge Disabled		385		µA
I_{Q_BAT}	Battery Only Quiescent Current	ADC Disabled, Charge Disabled, VIN Not Present		8	18	µA
		ADC Enabled (slowest mode), Charge Disabled, VBUS Not Present		385		µA
		ADC Enabled (fastest mode), Charge Disabled, VBUS Not Present		385		µA
RESISTANCES						
R_{QB_ON}	VBUS to PMID On Resistance	VBUS = 9 V		6	8	mΩ
R_{QCH1_ON}	On resistance of QCH1	VPMID = 9 V		22	27	mΩ
R_{QDH1_ON}	On resistance of QDH1	CFLY = 4.5 V		10	16	mΩ
R_{QCL1_ON}	On resistance of QCL1	VOUT = 4.5 V		7	14	mΩ
R_{QDL1_ON}	On resistance of QDL1	CFLY = 4.5 V		8	14	mΩ
R_{QCH2_ON}	On resistance of QCH2	VPMID = 9 V		22	27	mΩ
R_{QDH2_ON}	On resistance of QDH2	CFLY = 4.5 V		10	16	mΩ
R_{QCL2_ON}	On resistance of QCL2	VOUT = 4.5 V		7	14	mΩ
R_{QDL2_ON}	On resistance of QDL2	CFLY = 4.5 V		8	14	mΩ
R_{VBUS_PD}	VBUS pull-down resistance			6		kΩ
R_{VAC_PD}	VAC pull-down resistance			130		Ω
INTERNAL THRESHOLDS						
$VBUS_{UVLO}$	Rising	VBUS Rising			3.3	V
VAC_{UVLO}	Rising	VAC Rising			3.3	V
	Falling Hysteresis			300		mV
$V_{OVPGATE}$	External FET Gate Drive Voltage, Measured from Gate to Source, with minimum 8 nF CGS	VAC = 8 V		10		V
$VOUT_{UVLO}$	Rising				2.3	V
	Falling Hysteresis			100		mV

8.5 Electrical Characteristics (continued)

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VAC_{PRESENT}$	Rising				3.5	V
	Falling Hysteresis			300		mV
$VBUS_{PRESENT}$	Rising				2.85	V
	Falling Hysteresis			500		mV
$VOUT_{PRESENT}$	Rising			2.3	2.85	V
	Falling Hysteresis			100		mV
T_{SHUT}	Rising Internal (TJ) Shutdown			150		°C
	Falling Hysteresis			30		°C
PROTECTION and ALARMS THRESHOLD AND ACCURACY						
V_{OUTOVP}	VOUT OVP rising threshold		4.8	4.9	5	V
V_{DROP}	VDROP rising threshold	Adjustable in Register 0x05h, bit 4 = 0		300		mV
V_{DROP}	VDROP rising threshold	Adjustable in Register 0x05h, bit 4 = 1		400		mV
V_{BATOVP}	VBAT Over-Voltage Range	Adjustable in Register 0x00h	4.2		4.65	V
	VBAT Over-Voltage Step Size			10		mV
	VBAT Over-Voltage Accuracy		–1%		1%	
V_{BAT_ALM}	VBAT Alarm Range	Adjustable in Register 0x01h	4.2		4.65	V
	VBAT Alarm Step Size			25		mV
	VBAT Alarm Hysteresis	Falling		50		mV
	VBAT Alarm Comparator Accuracy	From VBAT = 3.5 V to 4.4 V	–0.4%		0.4%	
I_{BAT_OCP}	IBAT_OCP Range	Adjustable in Register 0x02h	0		10	A
	IBAT_OCP Step Size			50		mA
	IBAT_OCP Comparator Accuracy	IBAT = 6 A	–5%		5%	
I_{BATOCP_ALM}	IBATOCP_ALM Range	Adjustable in Register 0x03h	0		10	A
	IBATOCP_ALM Step Size			50		mA
	IBATOCP_ALM Hysteresis	Falling		50		mA
	IBATOCP_ALM Comparator Accuracy	IBAT = 6 A and 9 A	–1%		1%	
I_{BATUCP_ALM}	IBATUCP_ALM Range	Adjustable in Register 0x04h	0		10	A
	IBATUCP_ALM Step Size			50		mA
	IBAT_UCP_ALM Hysteresis	Rising		50		mA
	IBATUCP_ALM Comparator Accuracy	IBAT = 3 A	–2%		2%	
V_{VAC_OVP}	VAC_OVP Range	Adjustable in Register 0x05h	6.5		17	V
	VAC_OVP Step Size	Step size valid for 11 V through 17 V only		1		V
	VAC_OVP Comparator Accuracy	Accuracy for 6.5 V	–2%		2%	
	VAC_OVP Comparator Accuracy	Accuracy for 11 V through 17 V	–2%		2%	
V_{BUS_OVP}	VBUS_OVP Range	Adjustable in Register 0x06h, 250 mV typical hysteresis	6		12.35	V
	VBUS_OVP Step Size			50		mV
	VBUS_OVP Comparator Accuracy	VBUS = 10 V	–1%		1%	
V_{BUSOVP_ALM}	VBUSOVP_ALM Range	Adjustable in Register 0x07h	6		12.35	mV
	VBUSOVP_ALM Step Size			50		mV
	VBUSOVP_ALM Hysteresis	Falling		50		mV
	VBUSOVP_ALM Comparator Accuracy		–0.5%		0.5%	

8.5 Electrical Characteristics (continued)

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BUS_OCP}	IBUS_OCP Range	Adjustable in Register 0x08h	0		4.75	A
	IBUS_OCP Step Size			50		mA
	IBUS_OCP Comparator Accuracy	3 A	–5%		5%	
I_{BUS_UCP}	IBUS_UCP Rising, IBAT must reach this value before the SS timeout or Switching Stops, Protection disabled until IBUS Current Reaches this Value	Adjustable in Register 0x2Bh, bit 2 = 0		300	375	mA
I_{BUS_UCP}	IBUS_UCP Rising, IBAT must reach this value before the SS timeout or Switching Stops, Protection disabled until IBUS Current Reaches this Value	Adjustable in Register 0x2Bh, bit 2 = 1		500	575	mA
I_{BUS_UCP}	IBUS_UCP Falling, Switching stops when IBUS current reaches this value	Adjustable in Register 0x2Bh, bit 2 = 0	10	150		mA
	IBUS_UCP Falling, Switching stops when IBUS current reaches this value	Adjustable in Register 0x2Bh, bit 2 = 1	100	250		mA
I_{BUSOCP_ALM}	IBUSOCP_ALM Range	Adjustable in Register 0x09h	0		4.95	A
	IBUSOCP_ALM Step Size			50		mA
	IBUSOCP_ALM Hysteresis	Falling		50		mA
	IBUSOCP_ALM Comparator Accuracy	IBUS = 3 A (0°C to 85°C)	–4%		4%	
TS_{BAT_FLT} TS_{BUS_FLT}	TSBUS and TSBAT voltage range		0%		75%	
	TSBUS and TSBAT Threshold Step Size		0%		0.1953%	
	TSBUS and TSBAT Comparator Accuracy		–1%		1%	
	TSBUS and TSBAT Falling Hysteresis			4%		
TIMINGS						
f_{SW}	Switching Frequency	Register set to 500 kHz in Register 0x0Bh		500		kHz
t_{VAC_OVP}	VAC OVP reaction time			0.1		µs
t_{VOUT_OVP}	VAC OVP reaction time			5.5		µs
t_{VAC_PD}	VAC Pulldown duration			400		ms
t_{VBUS_OVP}	VBUS OVP reaction time (Note: The deglitch time is increased during regulation)	Not in regulation		1		µs
t_{IBUS_OCP}	IBUS OCP reaction time (Note: The deglitch time is increased during regulation)	Not in regulation		75		µs
t_{IBUS_UCP}	IBUS UCP falling reaction time (Note: The deglitch time is increased during regulation)	Not in regulation. Adjustable in Register 0x2Eh, bit 4 = 0		10		µs
t_{IBUS_UCP}	IBUS UCP falling reaction time (Note: The deglitch time is increased during regulation)	Not in regulation. Adjustable in Register 0x2Eh, bit 4 = 1		10		ms
t_{VDROP}	VDROP rising threshold deglitch (Note: The deglitch time is increased during regulation)	Not in regulation. Adjustable in Register 0x2Eh, bit 3 = 0		10		µs
t_{VDROP}	VDROP rising threshold deglitch (Note: The deglitch time is increased during regulation)	Not in regulation. Adjustable in Register 0x2Eh, bit 3 = 1		5		ms
t_{VBAT_OVP}	VBAT OVP reaction time			0		µs
		Deglitch during regulation		5		ms
t_{VOUT_OVP}	VOUT OVP reaction time			4		µs

8.5 Electrical Characteristics (continued)

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{IBAT_OCP}	IBAT OCP reaction time			500		µs
		Deglitch during regulation		5		ms
t_{INT}	Duration that $\overline{INT}$ is pulled low when an event occurs			256		µs
$t_{REG\_TIMEOUT}$	If the part is in regulation, but below V_{DROP_OVP} for this amount of time, the part will stop switching.			650		ms
$t_{INT\_REG\_DGL}$	Deglitch when $\overline{INT}$ is pulled low after an event occurs	Rising		100		ms
		Falling		5		ms
$T_{ALM\_DEBOUNCE}$	Time between consecutive faults for ALM indication			120		ms
t_{BUS_DETACH}	IBUS threshold reaction time			1		µs
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion Time, Each Measurement	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		
		ADC_SAMPLE[1:0] = 10		6		
		ADC_SAMPLE[1:0] = 11		3		
ADC_{RES}	Effective Resolution (0°C to 85°C)	ADC_SAMPLE[1:0] = 00		14		bits
		ADC_SAMPLE[1:0] = 01		13		
		ADC_SAMPLE[1:0] = 10		12		
		ADC_SAMPLE[1:0] = 11		11		
ADC MEASUREMENT RANGES AND LSB						
IBUS_ADC	ADC Bus Current Readable in Registers 0x16h and 0x17h	Range	0		5	A
		LSB		1		mA
IBUS_ADC	ADC Accuracy	1.5 A (0°C to 85°C)	–5%		5%	
IBUS_ADC	ADC Accuracy	3 A (0°C to 85°C)	–5%		5%	
VBUS_ADC	ADC Bus Voltage Readable in Registers 0x18h and 0x19h	Range	0		14	V
		LSB		1		mV
VBUS_ADC	ADC Bus Voltage	Accuracy for 8V, ADC_RATE = 00	–0.%5		0.5%	
VAC_ADC	ADC VAC Voltage Readable in Registers 0x1Ah and 0x1Bh	Range	0		14	V
		LSB		1		mV
VAC_ADC	ADC VAC Voltage	Accuracy for 8 V, ADC_RATE = 00	–0.5%		0.5%	
VOUT_ADC	ADC Output Voltage Readable in Registers 0x1Ch and 0x1Dh	Range	0		5	V
		LSB		1		mV
VOUT_ADC	ADC Output Voltage	Accuracy for 4 V, ADC_RATE = 00	–0.5%		0.5%	
VBAT_ADC	ADC Battery Voltage Readable in Registers 0x1Eh and 0x1Fh	Range	0		5	V
		LSB		1		mV
VBAT_ADC	ADC Battery Voltage	Accuracy for 3.5 V through 4.4 V, ADC_RATE = 00	–0.4%		0.2%	
IBAT_ADC	ADC Battery Current Readable in Registers 0x20h and 0x21h	Range	0		10	A
		LSB with 2 mΩ R_{SENSE}		1		mA
IBAT_ADC	ADC Battery Current	3 A	–2%		2%	
IBAT_ADC	ADC Battery Current	6 A	–1.5%		1.5%	
IBAT_ADC	ADC Battery Current	9 A	–1.5%		1.5%	

8.5 Electrical Characteristics (continued)

over operating free-air temperature range of –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSBUS_ADC	ADC TSBUS pin voltage	Range	0.2		2.7	V
TSBUS_ADC	ADC TSBUS % of VOUT Readable in Registers 0x22h and 0x23h	Range	0%		50%	
		LSB		0.09766 %		
TSBUS_ADC	ADC TSBUS Accuracy	TSBUS pin voltage 2 V	–1%		1%	
TSBAT_ADC	ADC TSBAT pin voltage	Range	0.2		2.7	V
TSBAT_ADC	ADC TSBAT pin voltage Readable in Registers 0x24h and 0x25h	Range	0%		50%	
		LSB		0.09766 %		
TSBAT_ADC	ADC TSBAT pin voltage	TSBAT pin voltage 2 V	–1%		1%	
TDIE_ADC	ADC Die Temperature Readable in Registers 0x26h and 0x27h	Range	–40		150	°C
		LSB		0.5		°C
TDIE_ADC	ADC Die Temperature (Typ over temp)			±4		°C
REGN LDO						
V_{REGN}	REGN LDO Output Voltage	VBUS = 8 V		5		V
I_{REGN}	REGN LDO Current Limit	VBUS = 8 V, VREGN = 4.5 V	50			mA
LOGIC I/O THRESHOLDS ($\overline{INT}$, BATP_SYNCIN)						
V_{IL}	Input Low Threshold	I_{SINK} = 5 mA			0.4	V
V_{IH}	Input High Threshold	I_{SINK} = 5 mA	1.3			V
I_{LEAK}	High Level Leakage Current	$V_{PULL-UP}$ = 3.3 V			1	µA
LOGIC I/O THRESHOLDS (TSBAT_SYNCOUT)						
V_{OH}	Output High Threshold	$V_{PULL-UP}$ = 1.8V	1.3			
V_{OL}	Output Low Threshold	$V_{PULL-UP}$ = 1.8V			0.4	
I2C LEVELS and TIMINGS						
V_{IL}	Input Low Threshold	$V_{PULL-UP}$ = 1.8 V, SDA and SCL			0.4	V
V_{IH}	Input High Threshold	$V_{PULL-UP}$ = 1.8 V, SDA and SCL	1.3			V
V_{OL}	Output Low Threshold	I_{OL} = 20 mA			0.4	V
I_{BIAS}	High Level Leakage Current	$V_{PULL-UP}$ = 1.8 V, SDA and SCL			1	µA
f_{SCL}	SCL Clock Frequency				1	MHz
t_{SU_STA}	Data Set-Up Time		10			ns
t_{HD_DAT}	Data Hold Time		0		70	ns
t_{rDA}	Rise Time of SDA Signal	Cbus = 100 pF max	10		80	ns
t_{fDA}	Fall Time of SDA Signal	Cbus = 100 pF max	10		80	ns

8.6 Typical Characteristics

Typical characteristics are taken with test equipment for nonswitching tests, and with the EVM-893 for switching tests.

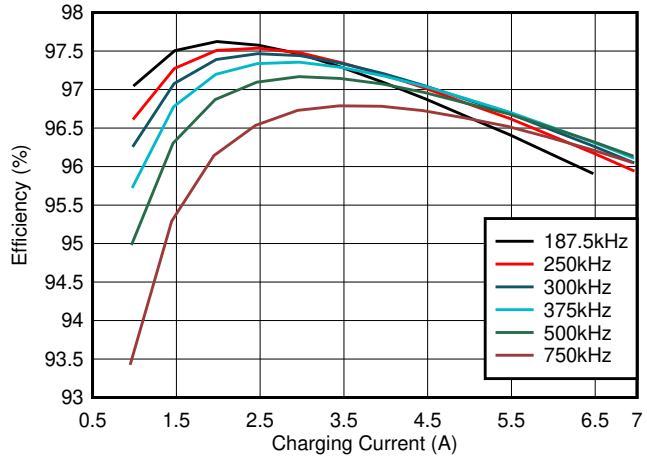


図 8-1. BQ25968 Device Efficiency, 3 x 22-µF Caps Per Phase

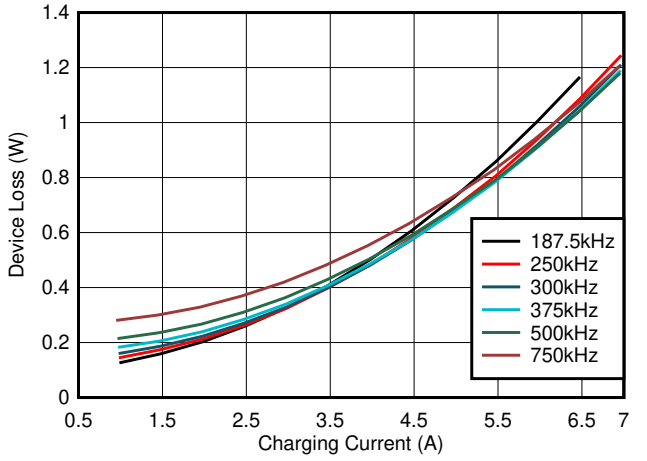


図 8-2. BQ25968 Device Power Loss, 4 x 20-µF Caps Per Phase

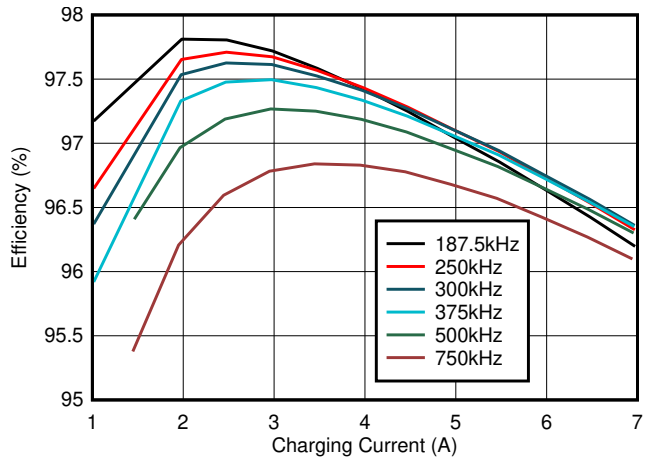


図 8-3. BQ25968 Device Efficiency, 4 x 22-µF Caps Per Phase

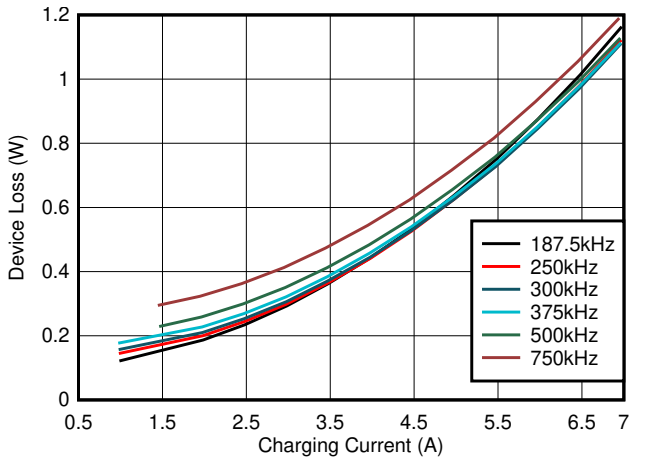
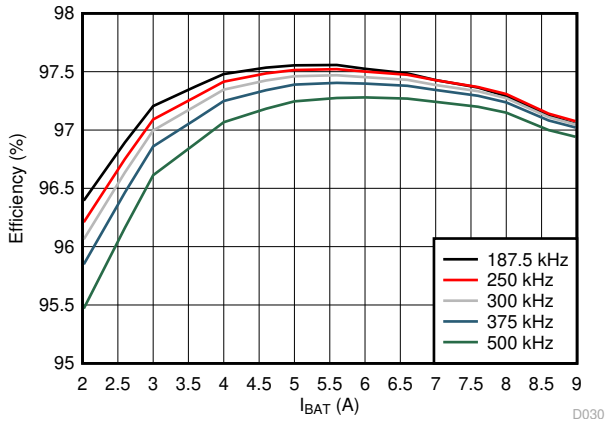
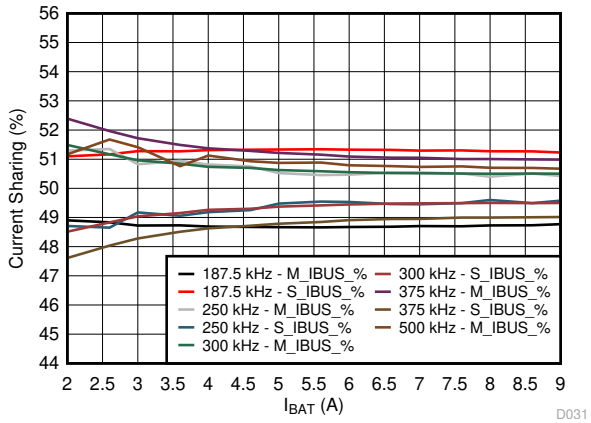


図 8-4. BQ25968 Device Power Loss, 4 x 22-µF Caps Per Phase



A1 BV L13 4*20-µF caps per phase, 2-mΩ IBAT sense resistor

図 8-5. BQ25968 Parallel Efficiency

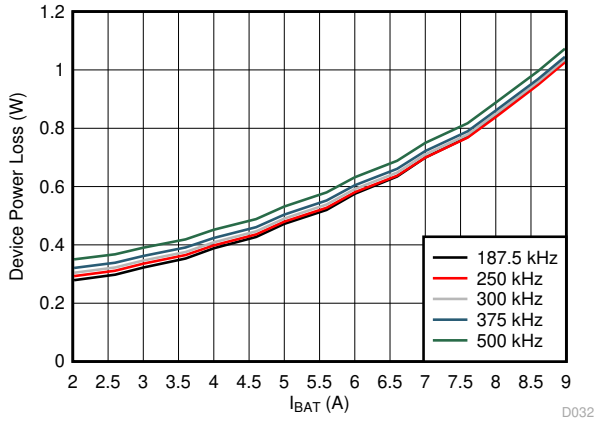


A1 BV L13 4*20-µF caps per phase, 2-mΩ IBAT sense resistor

図 8-6. BQ25968 Parallel Current Sharing

8.6 Typical Characteristics (continued)

Typical characteristics are taken with test equipment for nonswitching tests, and with the EVM-893 for switching tests.



A1 BV L13 4*20-µF caps per phase, 2-mΩ IBAT sense resistor

図 8-7. BQ25968 Parallel Power Loss

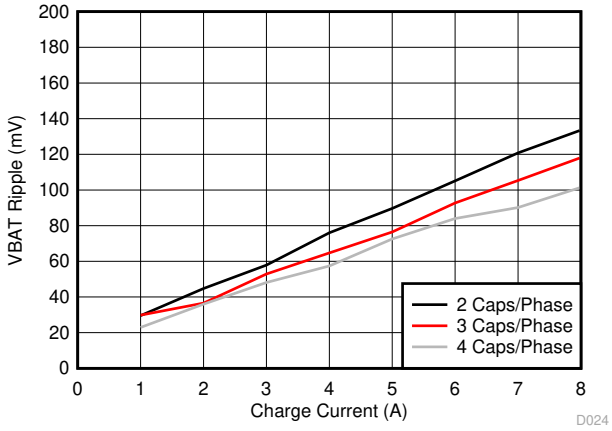


図 8-8. VBAT Ripple at 500 kHz

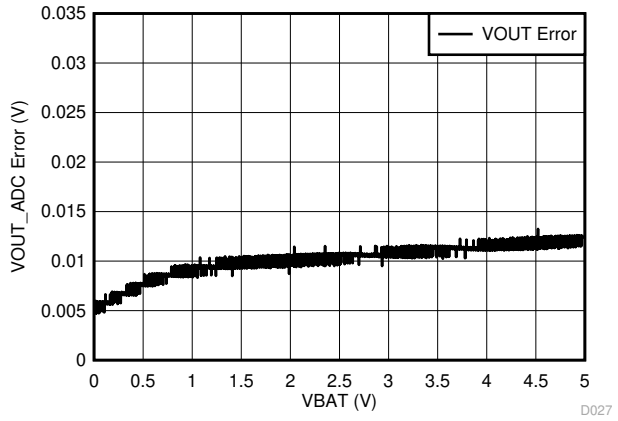


図 8-9. VOUT_ADC Error

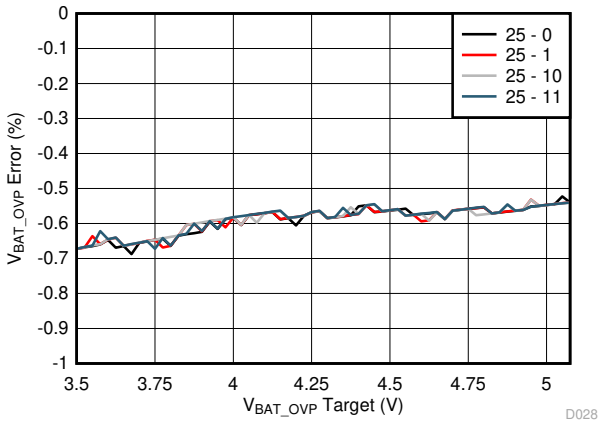


図 8-10. VBAT_OVP Error

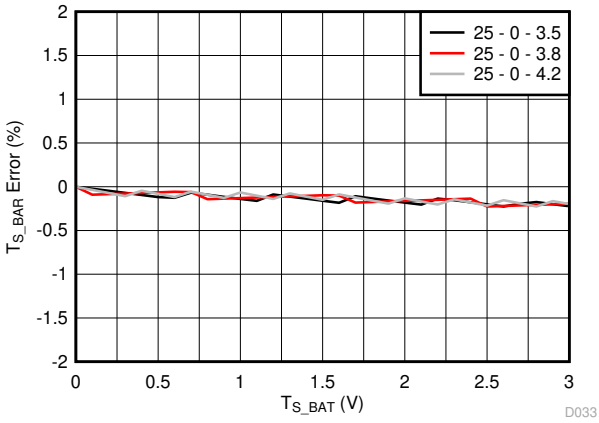


図 8-11. TS_BAT Error

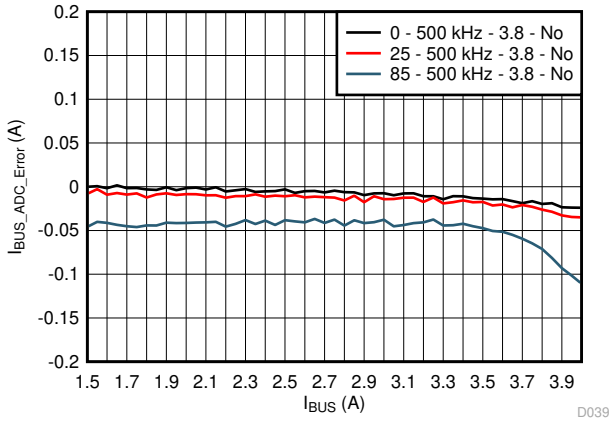


図 8-12. IBUS_ADC Error

8.6 Typical Characteristics (continued)

Typical characteristics are taken with test equipment for nonswitching tests, and with the EVM-893 for switching tests.

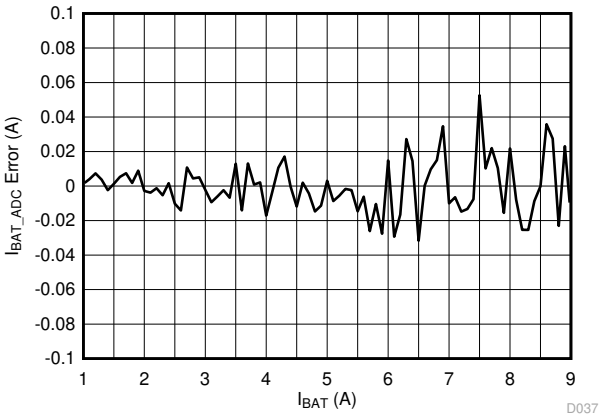


図 8-13. IBAT_ADC Error

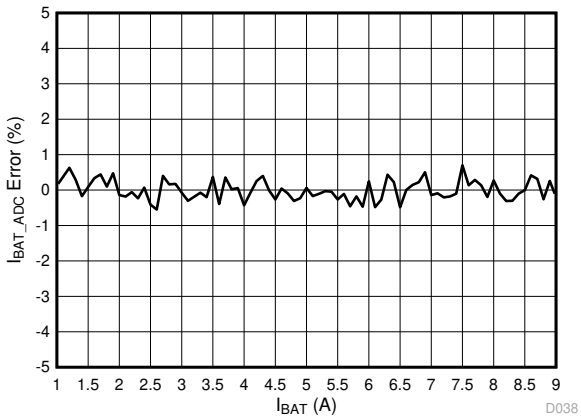


図 8-14. IBAT_ADC Error

9 Detailed Description

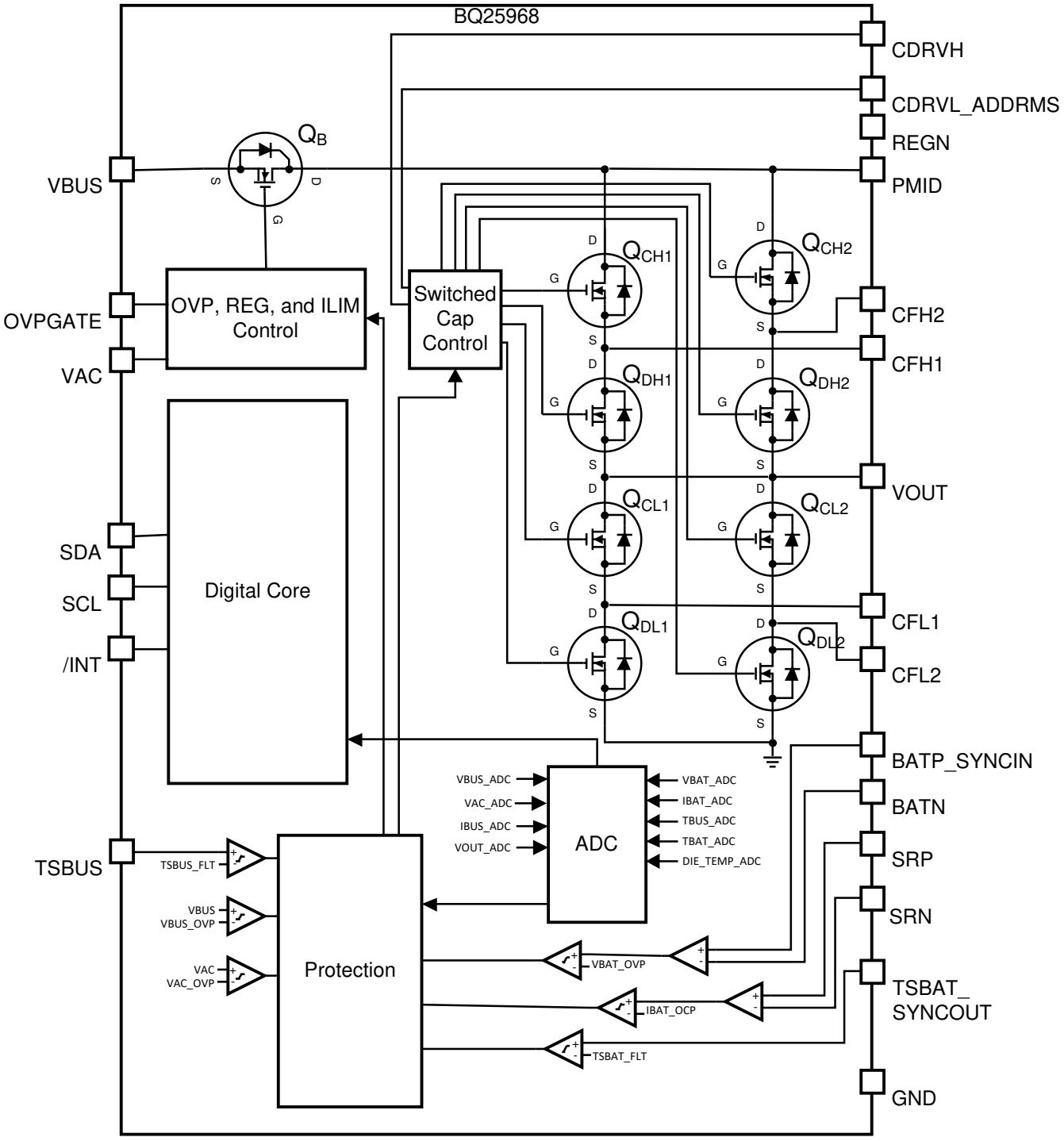
9.1 Overview

The BQ25968 is a 97% efficient, 6-A battery charging solution using a switched cap architecture. This architecture and the integrated FETs are optimized to enable a 50% duty cycle, allowing the cable current to be half the current delivered to the battery, reducing the losses over the charging cable as well as limiting the temperature rise in the application. The dual-phase architecture reduces the input cap requirements as well as reducing the output voltage ripple. When used with a standard charger such as the BQ2589x, the system enables the fastest charging at the lowest power loss from precharge through CC, CV, and termination.

The device integrates all the necessary protection features to ensure safe charging, including input overvoltage and overcurrent protection, output overvoltage and overcurrent protection, temperature sensing for the battery and cable, and monitoring the die temperature.

The device includes a 16-bit (minimum 12-bit effective) ADC to provide bus voltage, bus current, output voltage, battery voltage, battery current, bus temperature, bat temperature, die temperature, and other calculated measurements needed to manage the charging of the battery from the smart wall adapter or power bank.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Charging System

The BQ25968 is a slave charger used with a fast charging switching charger such as the BQ25890. A host must set up the protections and alarms on the BQ25968 prior to disabling the SW charger and enabling the BQ25968 charger. The host must monitor the alarms generated by the BQ25968 and communicate with the smart adapter to control the current delivered to the charger.

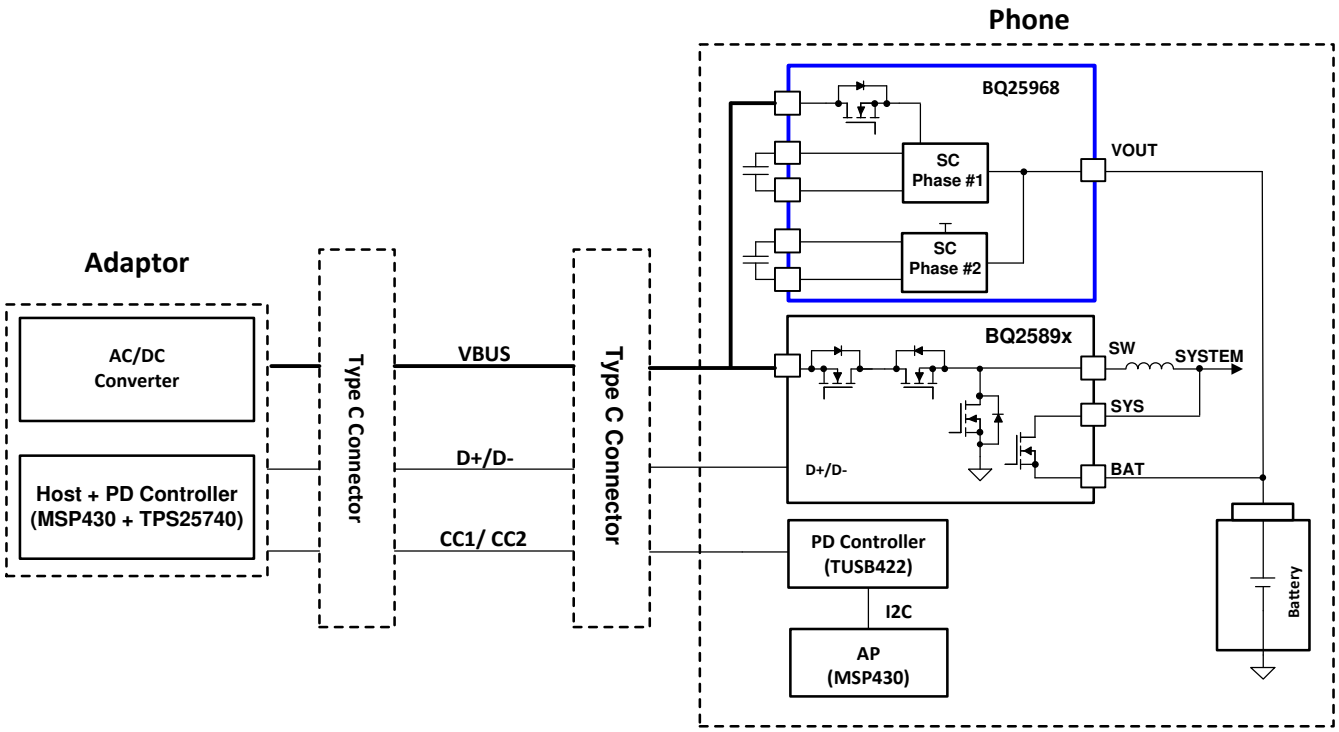


図 9-1. BQ25968 System Diagram

9.3.2 Battery Charging Profile

The system will have a specific battery charging profile that is unique due to the switched cap architecture. During the trickle charge and precharge of the battery up to 3.5 V, the charging will be controlled by the primary charger (BQ25890 in 図 9-1). Once the battery voltage reaches 3.5 V, the adapter can negotiate for a higher bus voltage, enable the BQ25968 charging, and regulate the current on VBUS to charge the battery. In the CC phase, the protection in the BQ25968 will not regulate the battery voltage, but will provide feedback to the system to increase/decrease current as needed, as well as disable the output if the voltage is exceeded. Once the CV point is reached, the BQ25968 will provide feedback to the adapter to reduce the current, effectively tapering the current until a point where the primary charger takes over again. This charging profile is shown in 図 9-2.

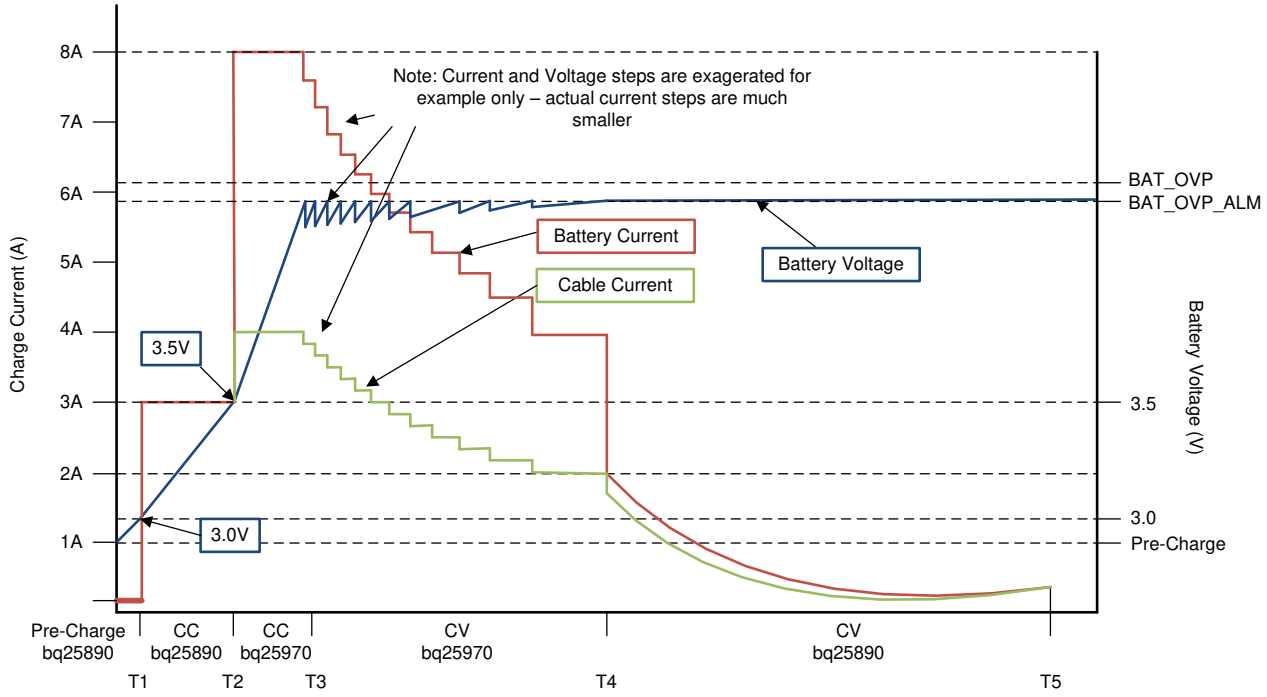


図 9-2. BQ25968 System Charging Profile

9.3.3 Control State Diagram for System Implementation

The device being charged will need to communicate with the adapter to control the current being delivered to the BQ25968. This is accomplished by using the adjustable protection and alarm settings in the BQ25968, and communicating to the wall charger (or power bank or car charge adapter) as shown in 図 9-3. The availability of the alarms are dependant on the presence of the input supply and the charge state, which is shown in 表 9-1.

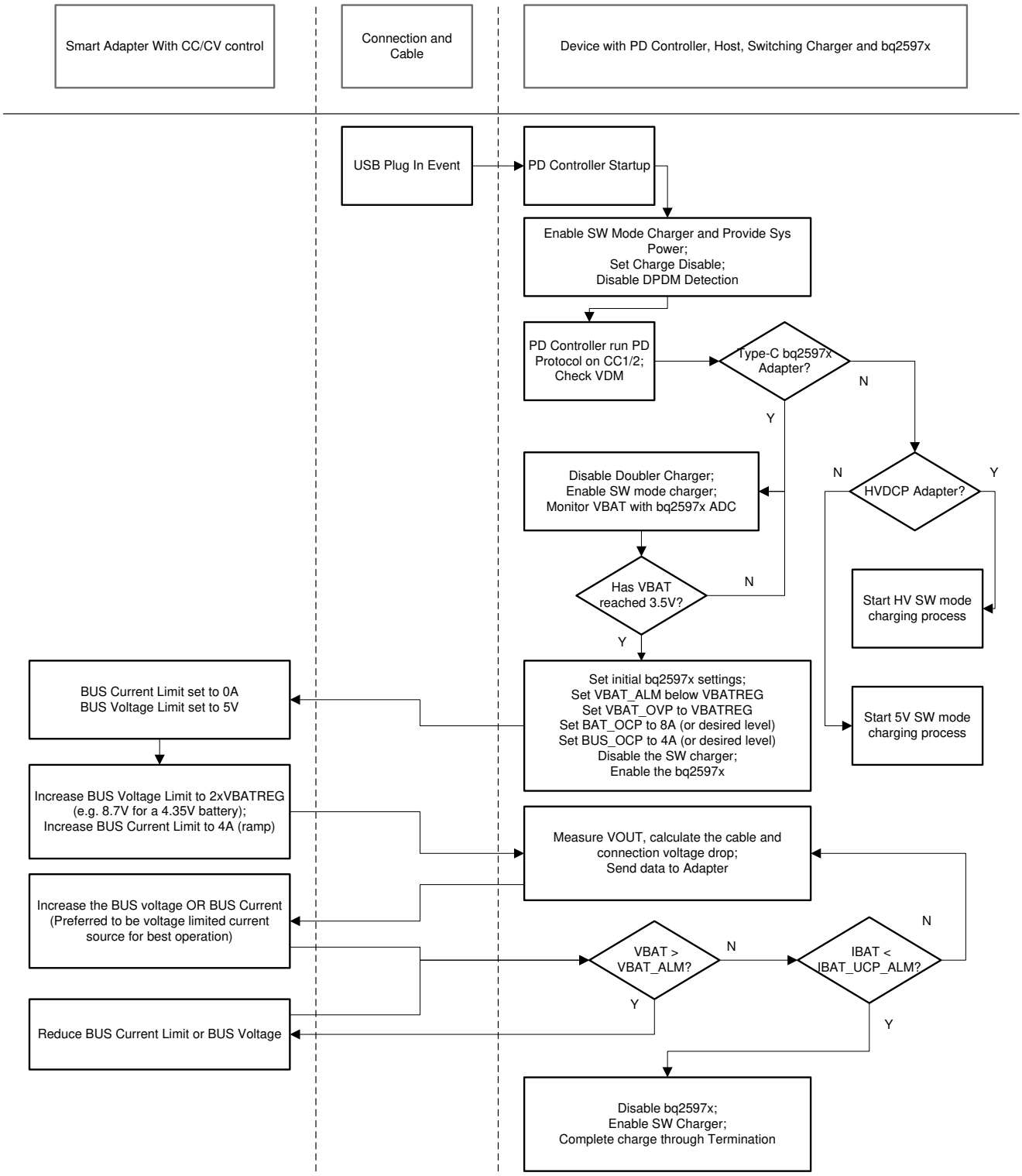


図 9-3. System Control State Diagram

表 9-1. ALM/FLT Function Activity

ALM/FLT FUNCTION	BATTERY ONLY	VAC PRESENT CHG_EN = 0	VAC PRESENT CHG_EN = 1
BAT_OVP_ALM	Not Active	Not Active	Active

表 9-1. ALM/FLT Function Activity (continued)

ALM/FLT FUNCTION	BATTERY ONLY	VAC PRESENT CHG_EN = 0	VAC PRESENT CHG_EN = 1
BAT_OCP_ALM	Not Active	Not Active	Active
BAT_UCP_ALM	Not Active	Not Active	Active
BUS_OVP_ALM	Not Active	Not Active	Active
BUS_OCP_ALM	Not Active	Not Active	Active
TSBUS_FLT	Not Active	Active	Active
TSBAT_FLT	Not Active	Active	Active
TDIE_ALM	Not Active	Active	Active
TSBUS_TSBAT_ALM	Not Active	Active	Active

9.3.4 Device Power Up

The device is powered from the greater of either VBUS or VOUT (battery). The voltage must be greater than the $VBUS_{PRESENT}$ or $VOUT_{PRESENT}$ threshold to be a valid supply. However, the device will start drawing power once the voltage rises above the $VBUS_{UVLO}$ or $VOUT_{UVLO}$ threshold.

The device has a watchdog timer, which is enabled by default. If the device is not read from or written to before the watchdog expires, the part will stop switching. The first read of the watchdog timer flag will always read '1'. During initial power up of the device, upon completion of pin detection for address, an $\overline{INT}$ pulse will be triggered to show a watchdog timeout. The host should not attempt to read or write before this initial $\overline{INT}$ signal.

The device will not charge when first powered up, as the default charge state is always not enabled. The ADC is available prior to enabling charge so the system parameters are known to the host before enabling charge. If the VOUT voltage is not greater than 3 V, the charger cannot be enabled. The lowest charge voltage allowed on VOUT is 2.8 V falling.

Although the device will depend on the smart adapter to ramp the charging current, the device implements a soft start through Q_B that limits the ramp current. If the current through Q_B is greater than the programmed V_{BUS_OCP}, the FET is disabled. The output voltage ramps as the current is increased.

9.3.5 Switched Cap Function

The power stage used in the device is a parallel-series switched cap architecture with two phases. The output voltage of the power stage is half of the input voltage. The output current of the power stage is twice the input current. By controlling the constant current source input to the power stage, the CC and CV charging phases can be achieved with the protections and alarms implemented in the device.

9.3.5.1 Theory of Operation

The power stage of the device is shown in the block diagram, and a simplified single phase circuit is shown in 図 9-4. When operating, the device switches at a 50% duty cycle with Q1 and Q3 turned on and off at the same time, while Q2 and Q4 are turned on and off simultaneously. This results in the following equivalent circuits.

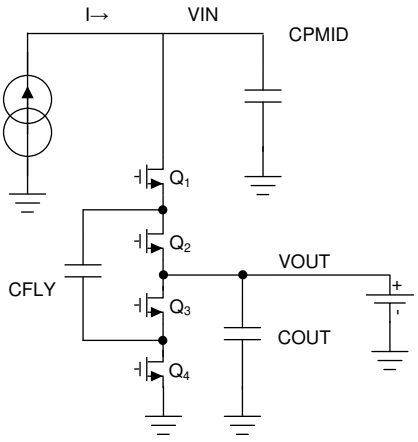


図 9-4. BQ25968 Simplified Switched Cap Architecture (single phase)

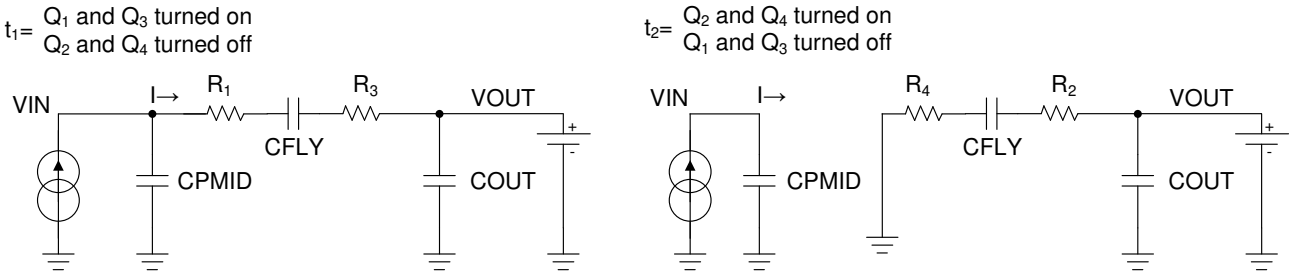


図 9-5. BQ25968 Equivalent Circuits During Operation

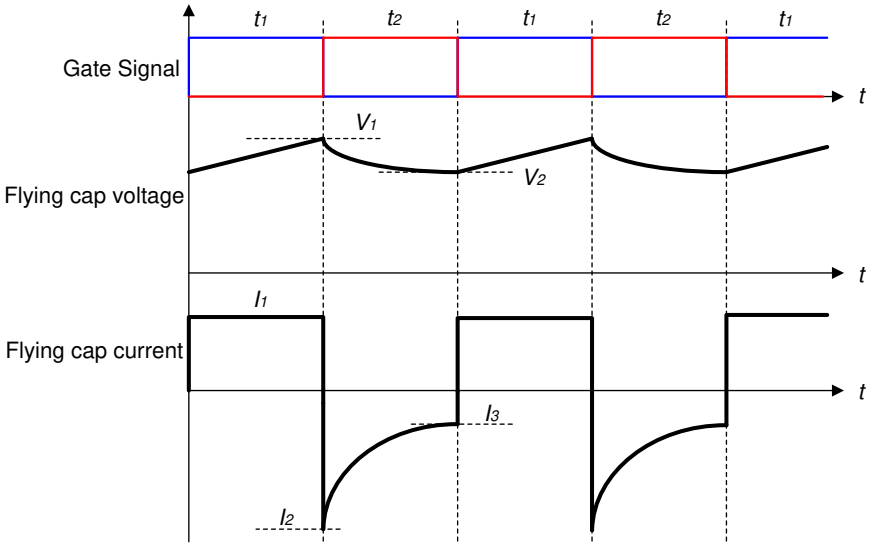


図 9-6. BQ25968 Switching Waveforms

9.3.6 Charging Start-Up

Prior to enabling charging, set all the protections to the desired thresholds. Protections available are BAT_OVP, BAT_OVP_ALM, BAT_OCP, BAT_OCP_ALM, BAT_UCP_ALM, AC_PROTECTION, BUS_OVP, BUS_OVP_ALM, BUS_OCP_UCP, and BUS_OCP_ALM. These can be found in registers 0x0h through 0x9h. The *_OVP and *_OCP registers set the thresholds where if these conditions are met, the charger stops switching. The *_ALM registers set the thresholds where an interrupt is sent to the host to take actions to avoid

reaching the *_OVP or *_OCP thresholds. The settings for the *_ALM registers will depend on the response time required from the host and the operating conditions of the system.

Once the protections have been set, the BUS voltage must be between VBUS_ERROR_LO and VBUS_ERROR_HI in order for the part to start switching. Register 0x0Ah contains the registers to check if these conditions have been met. Typically VBUS_ERROR_LO is 2.05 times VBAT. It is recommended to start with VBUS near this voltage when enabling charge. Once charge has been enabled, the CONV_SWITCHING_STAT bit should be '1', and current will start to flow to the battery. Raising the BUS voltage will increase the current to the battery. If using a current limited source, the voltage can be raised until reaching the current limit. The battery current, IBAT, must reach the IBUS_UCP_THRESHOLD rise threshold within the SS_TIMEOUT_SET time. These parameters can be set in register 0x2Bh. If the IBUS_UCP_THRESHOLD is not met within SS_TIMEOUT_SET, switching stops and the startup sequence must be done again.

9.3.7 Integrated 16-Bit ADC for Monitoring and Smart Adapter Feedback

The integrated 16-bit ADC of the device allows the user to get critical system information for optimizing the behavior of the charger control. The control of the ADC is done through the ADC_CTRL register. The ADC_EN bit provides the ability to enable and disable the ADC to conserve power. The ADC_RATE bit allows continuous conversion or one-shot behavior. The ADC_AVG_DIS bit enbles or disables averaging

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is allowed to operate if either the V_{VBUS}>$VBUS_{PRESENT}$ or V_{VOUT}>$VOUT_{PRESENT}$ is valid. If ADC_EN is set to ‘1’ before VBUS or VOUT reach their respective PRESENT threshold, then the ADC conversion will be postponed until one of the power supplies reaches the threshold.

The ADC_SAMPLE bits control the sample speed of the ADC, with conversion times of t_{ADC_CONV}. The integrated ADC has two rate conversion options: a 1-Shot Mode and a Continuous Conversion Mode set by the ADC_RATE bit. By default, all ADC parameters will be converted in 1-Shot or Continuous Conversion Mode unless disabled in the ADC_FN_DIS register. If an ADC parameter is disabled by setting the correcsponding bit in the ADC_FN_DIS register, then the value in that register will be from the last valid ADC conversion or the default POR value (all zeros if no conversions have taken place). If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC_FN_DIS register is set to ‘0’.

The ADC_DONE_* bits signal when a conversion is complete in 1-Shot Mode only. During Continuous Conversion Mode, the ADC_DONE_* bits have no meaning and will be ‘0’.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = ‘0’ to disable the ADC. ADC readings are only valid for DC states and not for transients. When the host writes ADC_EN = ‘0’, the ADC stops immediately. If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Write all the DIS bits low, and the ADC will stop at the end of the current measurement.

9.3.8 Device Internal Thermal Shutdown, TSBUS, and TSBAT Temperature Monitoring

The device has three temperature sensing mechanisms to protect the device and system during charging: TSBUS for monitoring the cable connector temperature, TSBAT for monitoring the battery temperature, and TDIE for monitoring the internal junction temperature of the device. TSBUS and TSBAT only operate when there is a valid input supply. The TSBUS and TSBAT both rely on a resistor divider that has an external pullup voltage to VOUT. Place a negative coefficient thermistor in parallel to the low-side resistor. A fault on the TSBUS and TSBAT pin is triggered on the falling edge of the voltage threshold, signifying a “hot” temperature. The threshold is adjusted using the TSBUS_FLT and TSBAT_FLT registers. A warning TSBUS_TSBAT_ALM interrupt will be sent if the percentage reached within 5% of the FLT setting. If the TSBUS_FLT or TSBAT_FLT is disabled, it will not trigger a TSBUS_TSBAT_ALM interrupt. The RLO and RHI resistors should be chosen depending on the NTC used. If a 10-kΩ NTC is used, use 10-kΩ resistors for RLO and RHI. If a 100-kΩ NTC is used, use 100-kΩ

resistors for RLO and RHI. The ratio of VTS/VOUT can be from 0% to 50%, and the voltage at the TS pin is determined by the following equation.

$$\text{VTSBUS or VTSBAT (V)} = \frac{\frac{1}{\left(\frac{1}{\text{RNTC}} + \frac{1}{\text{RLO}}\right)}}{\text{RHI} + \frac{1}{\left(\frac{1}{\text{RNTC}} + \frac{1}{\text{RLO}}\right)}} \times \text{VOUT} \quad (1)$$

The percentage of the TS pin voltage is determined by the following equation.

$$\text{TSBUS or TSBAT (\%)} = \frac{\frac{1}{\left(\frac{1}{\text{RNTC}} + \frac{1}{\text{RLO}}\right)}}{\text{RHI} + \frac{1}{\left(\frac{1}{\text{RNTC}} + \frac{1}{\text{RLO}}\right)}} \quad (2)$$

Additionally, the device has an internal die temperature measurement, with adjustable threshold TDIE_FLT.

If TSBUS, TSBAT, or TDIE protections are not used, the functions can be disabled in the CHRG_CTRL register by setting the TSBUS_DIS, TSBAT_DIS, or TDIE_DIS bit to '1'. If the TSBUS_FLT, TSBAT_FLT, thresholds are reached, the CHG_EN bit is set to '0', and the start-up sequence must be followed to resume charging.

Using the TDIE_ALM register, an alarm can be set to notify the host when the device die temperature exceeds a threshold. The device will not automatically stop switching when reaching the alarm threshold, and the host may decide on the steps to take to lower the temperature, such as reducing the charge current. The device will automatically stop switching when it reaches the TSHUT threshold.

9.3.9 $\overline{\text{INT}}$ Pin, STAT, FLAG, and MASK Registers

The $\overline{\text{INT}}$ pin is an open drain pin that needs to be pulled up to a voltage with a pullup resistor. $\overline{\text{INT}}$ is normally high and will assert low for t_{INT} when the device needs to alert the host of a fault or status change. The behavior of the $\overline{\text{INT}}$ pin is determined by six registers: INT_STAT, INT_FLAG, INT_MASK, FLT_STAT, FLT_FLAG, and FLT_MASK.

The fields in the STAT registers show the current status of the device, and are updated as the status changes. The fields in the FLAG registers indicate that the event has occurred, and the field is cleared when read. If the event persists after the FLAG register has been read and cleared, another $\overline{\text{INT}}$ signal is not sent. The fields in the MASK registers allow the user to disable the interrupt on the $\overline{\text{INT}}$ pin, but the STAT and FLAG registers are still updated even though $\overline{\text{INT}}$ is not pulled low.

9.3.10 CDRVH and CDRVL_ADDRMS Functions

The device requires a cap between the CDRVH and CDRVL_ADDRMS pins to operate correctly. The CDRVL_ADDRMS pin also allows setting the default I^2C address and power-up AC_OVP threshold for external OVP FET control. Pull to GND with a resistor for the desired setting shown in 表 9-2. Once I^2C communication begins with the device, the register sets the AC_OVP threshold.

表 9-2. BQ25968 I^2C Address and Mode Selection

RESISTOR VALUE TO GND ON CDRVL_ADDRMS	I^2C ADDR (NVM_I2CADDR_ALT = 0)	I^2C ADDR (NVM_I2CADDR_ALT = 1)	AC_OVP SETTING	MASTER, SLAVE, OR STANDALONE OPERATION
18 KΩ	0×65	0×66	6.5 V	Master
39 KΩ	0×66	0×67	(Disabled)	Slave

表 9-2. BQ25968 I²C Address and Mode Selection (continued)

RESISTOR VALUE TO GND ON CDRVL_ADDRMS	I²C ADDR (NVM_I2CADDR_ALT = 0)	I²C ADDR (NVM_I2CADDR_ALT = 1)	AC_OVP SETTING	MASTER, SLAVE, OR STANDALONE OPERATION
75 KΩ	0×65	0×67	11 V	Standalone
Open (>150 KΩ)	0×66	0×67	6.5 V	Standalone

If a standalone device is needed with the AC_OVP function disabled, use the BQ25971.

9.3.11 Parallel Operation Using Master and Slave Modes

For higher power systems, it is possible to use two BQ25968 devices in parallel. This has the effect of reducing the adapter power requirements, reducing the cable losses, and reducing the losses in the device. The parallel system is shown in the figure below. The CDRVL_ADDRMS pin is used to configure the functionality of the device as Master or Slave. Refer to セクション 9.3.10 for proper setting.

When configured as a Master, the TSBAT_SYNCOUT pin functions as SYNCOUT, and the BATP_SYNCIN pin functions as BATP. When configured as a Slave, the TSBAT_SYNCOUT pin functions as TSBAT, and the BATP_SYNCIN pin functions as SYNCIN. OVPGATE is controlled by the Master, and the OVPGATE pin on the slave should be left floating. Pull the SYNCIN/SYNCOUT pins to REGN through a 1-kΩ resistor.

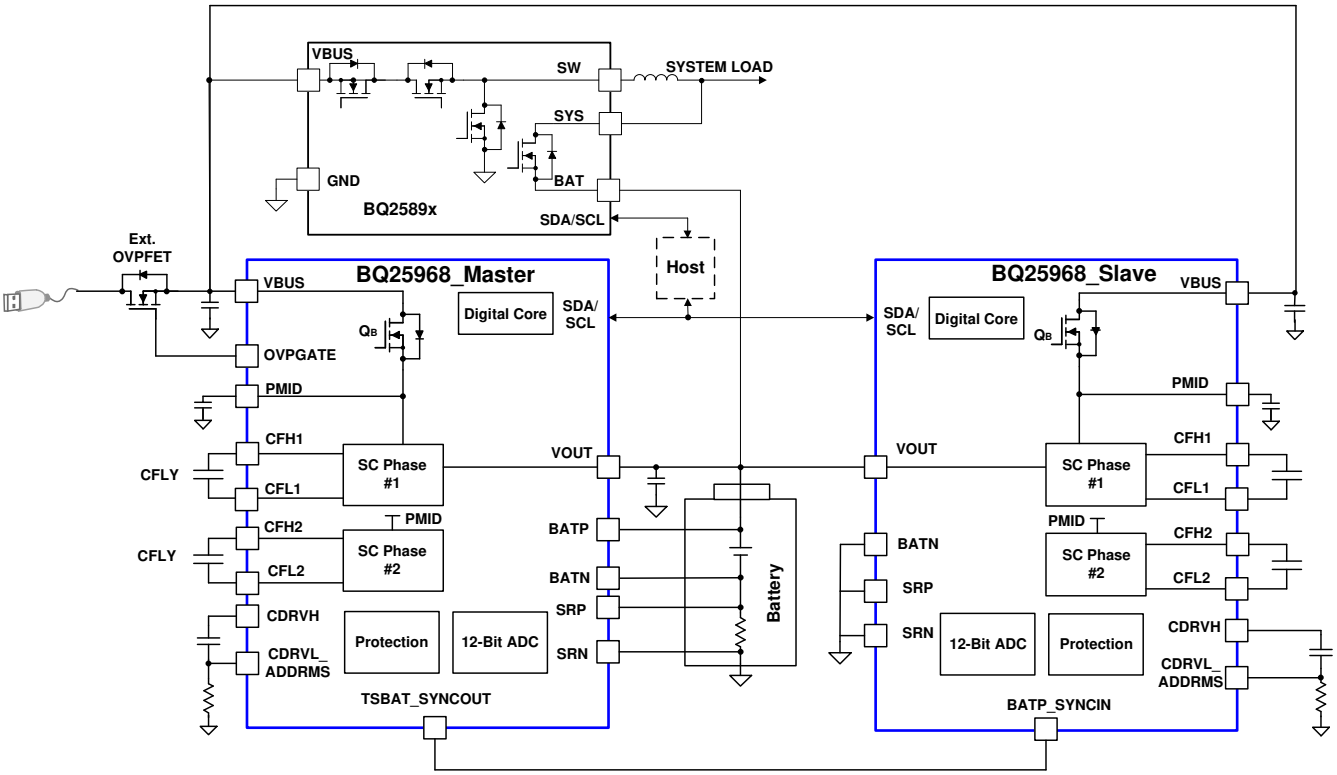


図 9-7. Parallel BQ25968 System

9.4 Device Functional Modes

9.4.1 Device Modes and Protection Status

表 9-3 shows the features and modes of the device depending on the conditions of the device.

表 9-3. Device Modes and Protection Status

FUNCTIONS AVAILABLE	STATE				
	BATT-ONLY (VAC < VACpres)	VAC > VACpresent	VAC > VACpresent	VAC > VACpresent	VAC > VACpresent
	(REGARDLESS OF VOUTpres)	CHARGE DISABLED	CHARGE DISABLED	DURING CHARGE SOFTSTART	CHARGING
	(REGARDLESS OF ADC)	(ADC NOT ENABLED)	ADC ENABLED	(REGARDLESS OF ADC)	(REGARDLESS OF ADC)
I^2C allowed	X	X	X	X	X
Allow user ADC request	X	X	X	X	X
VAC FET gate drive		X	X	X	X
VAC OVP protection		X	X	X	X
TS_BUS ALM		X	X	X	X
TS_BAT ALM		X	X	X	X
DIE TMP ALM		X	X	X	X
VBUS OVP ALM				X	X
VBAT OVP ALM				X	X
VBAT OCP ALM				X	X
VOUT_OVP			X	X	X
VBUS OCP ALM				X	X
VBUS UCP ALM					X
VBUS *In-range* (slow UVP/OVP)			X	X	X
TS_BUS FLT		X	X	X	X
TS_BAT FLT		X	X	X	X
DIE TMP FLT		X	X	X	X
VBUS OVP FLT				X	X
VBAT OVP FLT				X	X
VBAT OCP FLT				X	X
VBUS OCP FLT				X	X
VBUS UCP FLT					X
Cycle by Cycle Current Limit				X	X

Tripping any of these protection faults will cause Q_B to be off. Masking the fault or alarm does NOT disable the protection, but only keeps an INT from being triggered by the event. Disabling the fault or alarm will hold that stat and flag bits in reset, and also prevent an interrupt from occurring.

9.4.1.1 Input Overvoltage, Overcurrent, Undercurrent and Short-Circuit Protection

The device integrates the functionality of an input overvoltage protector. The device can be paired with an external N-channel FET to block input voltages higher than the setting programmed by the ADDR_MS pin. The device senses the input through the VAC pin and turns the external N-channel FET on or off through the OVPGATE pin. This eliminates the need for a separate OVP device to protect the overall system. The integrated VAC_OVP feature has a reaction time of t_{VAC_OVP}. The VAC OVP setting is adjustable in the VAC_PROTECTION register.

The integrated OVP feature has a reaction time of t_{VAC_OVP} (the actual time to turn off OVP FET will be longer and depends upon the FET gate capacitance) and the feature is always active as long as $V_{VAC} > VAC_{PRESENT}$).

The default VAC OVP threshold is set by CDRVL_ADDRMS and can be changed with the VAC_PROTECTION register bits. VAC OVP bits are only reset by a REG_RST or a POR event where the CDRVL_ADDRMS value is used.

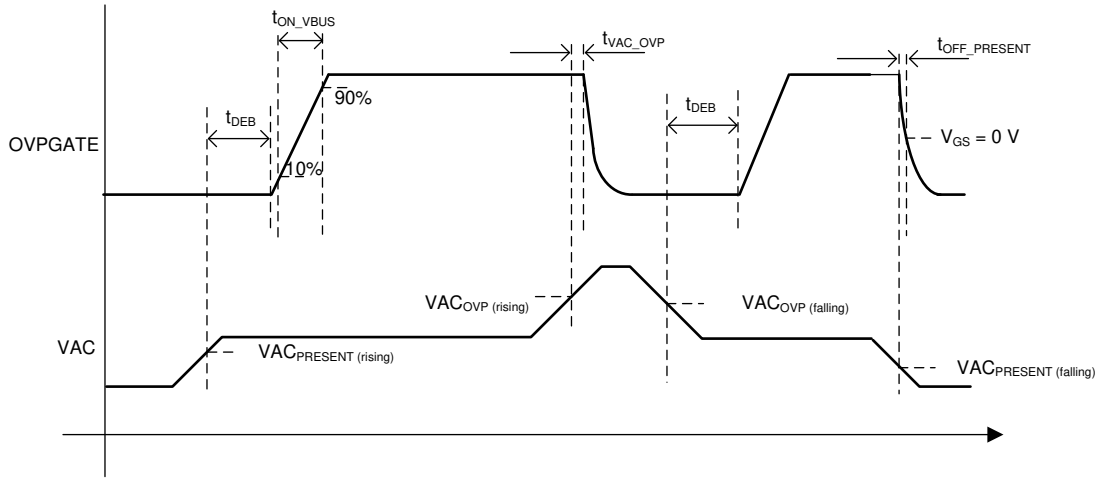


図 9-8. OVPGATE Timing

The device has an integrated blocking FET (Q_B), with a reaction time of t_{VBUS_OVP}. The BUS OVP threshold is adjustable in the BUS_OVP register.

Overcurrent protection monitors the current flow into VBUS. The overcurrent protection threshold is adjustable in the BUS_OCP register through the BUS_OCP bits, with a reaction time of t_{IBUS_OCP}.

When any input OVP, UVP, or OCP event is triggered, the CHG_EN bit is set to ‘0’ to disable charging, and the start-up protocol must be followed to begin charging again.

When the BAT_UCP_ALM is triggered, the host is notified and the CHG_EN bit is **not** set to ‘0’ to disable charging. The host must disable charging after this event and determine when to switch back to the primary switching charger. This alarm is blanked during start up for proper operation. When the device starts switching, the IBUS_UCP protection is disabled until the BUS current rises above IBUS_UCP rising threshold. After that, if the BUS current falls below IBUS_UCP falling, the device will stop switching. IBUS_UCP falling threshold cannot be masked or disabled.

9.4.1.2 Battery Overvoltage and Overcurrent Protection

The device integrates both overcurrent and overvoltage protection for the battery. The device monitors the battery voltage on BATP and BATN. In order to reduce the possibility of battery terminal shorts during manufacturing, series resistors on BATP and BATN are required. VBAT measurement accuracy must be met with a 100-Ω series resistor, but the device must still be operational with a 1-kΩ resistor. The device is intended to be operated within the window formed by the BAT_OVP and BAT_OVP_ALM. When the BAT_OVP_ALM is reached, an interrupt is sent to the host to reduce the charge current and thereby reaching the BAT_OVP threshold. If BAT_OVP is reached, charging stops, the CHG_EN bit is set to ‘0’, and the start-up sequence must be followed to resume charging.

A fixed VOUT_OVP threshold is implemented to protect the device if the battery is removed.

The device monitors current through the battery by monitoring the voltage across the external series battery sense resistor. The differential voltage of this sense resistor is measured on SRP and SRN. The device is intended to be operated within the window formed by the BAT_OCP and BAT_OCP_ALM. When the BAT_OCP_ALM is reached, an interrupt is sent to the host to reduce the charge current from reaching the BAT_OCP threshold. If BAT_OCP is reached, charging stops, the CHG_EN bit is set to ‘0’, and the start-up sequence must be followed to resume charging.

Comparator based for all battery overvoltage alarms and protections.

9.4.1.3 Cycle-by-Cycle Current Limit

The device monitors the outer switching FET current on a cycle-by-cycle basis. If an overcurrent is triggered for 16 cycles, the device responds by stopping switching and setting CHG_EN=0. When device triggered cycle-by-

cycle protection, CONV_OCP_FLAG is set to '1' and $\overline{INT}$ is asserted low to alert host. The start-up sequence must be followed to resume charging. It is recommended to limit the charging current of BQ25968 to 6 A without triggering the cycle-by-cycle protection.

9.5 Programming

The BQ25968 uses an I^2C compatible interface to program and read many parameters. I^2C is a 2-wire serial interface developed by NXP (formerly Philips Seminconductor, see I^2C BUS Specification, Version 5, October 2012). The BUS consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the BUS is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C BUS through open drain I/O terminals, SDA and SCL. A master device, usually a microcontroller or digital signal processor, controls the BUS. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the BUS under control of the master device.

The BQ25968 device works as a slave and supports the following data transfer modes, as defined in the I^2C BUS™ Specification: Standard Mode (100 kbps) and Fast Mode (400 kbps). The interface adds flexibility to the battery management solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The I^2C circuitry is powered from the battery in Active Battery Mode. The battery voltage must stay above VBATUVLO when no VIN is present to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-Mode in this document. The BQ25968 device only supports 7-bit addressing. The device 7-bit address is determined by the ADDR pin on the device.

To avoid I^2C hang-ups, a timer (TI2CRESET) runs during I^2C transactions. If the transaction takes longer than TI2CRESET, any additional commands are ignored and the I^2C engine is reset. The timeout is reset with START and repeated START conditions and stops when a valid STOP condition is sent.

9.5.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in the figure below. All I^2C-compatible devices should recognize a start condition.

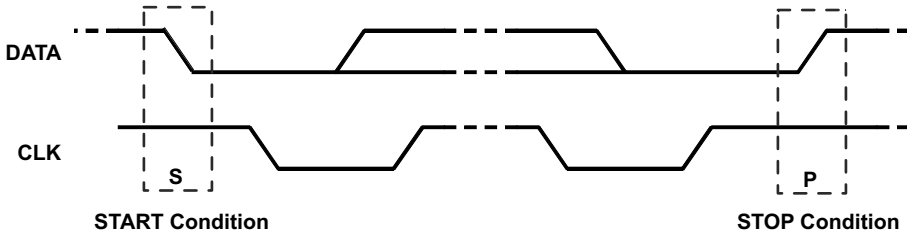


図 9-9. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 図 9-10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates and acknowledge (see 図 9-11) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

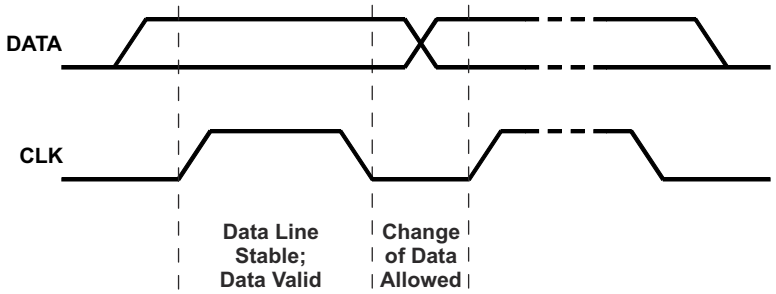


図 9-10. Bit Transfer on the Serial Interface

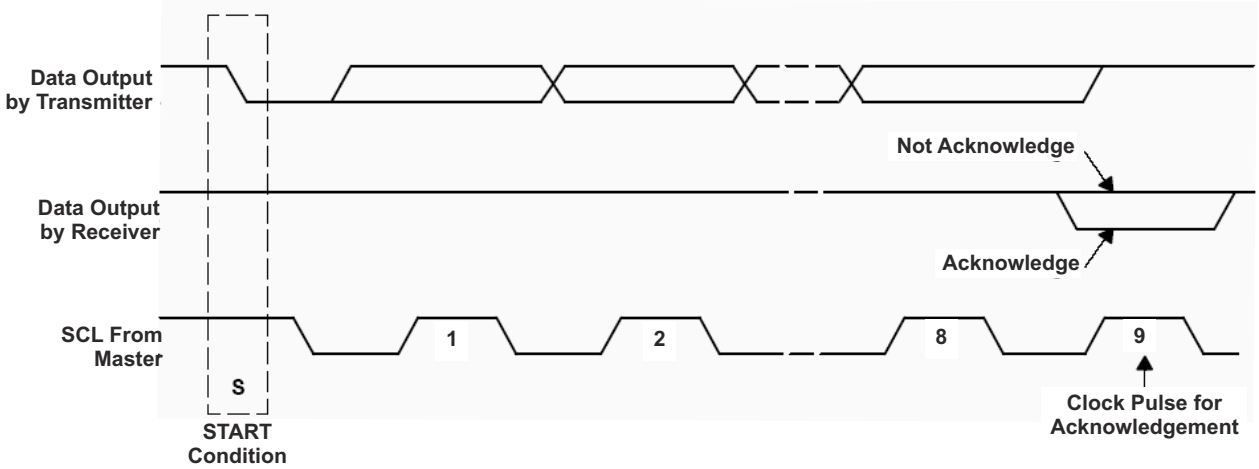


図 9-11. Acknowledge on the I²C BUS

The master generates further SCL cycles to either transmit data to the slave (R/W bit 0) or receive data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which on is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 図 9-12). This releases the BUS and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the BUS is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I²C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section will result in 0xFFh being read out.

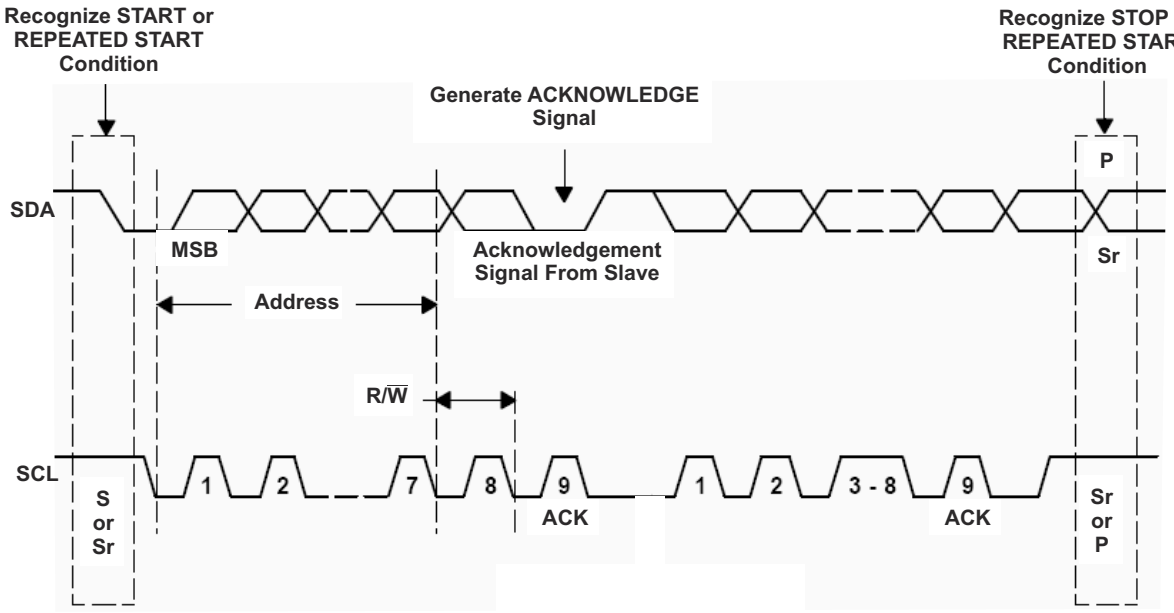


図 9-12. BUS Protocol

9.6 Register Maps

9.6.1 Customer Registers

表 9-4 can be accesses using I²C using the address programmed by the CDRVH_ADDRMS pin, and the value can be found in 表 9-2.

表 9-4. CUSTOMER Registers

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0h	BAT_OVP	Battery Voltage Limit	Go
1h	BAT_OVP_ALM	Battery Voltage Alarm	Go
2h	BAT_OCP	Charge Current Limit	Go
3h	BAT_OCP_ALM	Charge Current Alarm	Go
4h	BAT_UCP_ALM	Charge Under Current Alarm	Go
5h	AC_PROTECTION	Input Voltage Limit	Go
6h	BUS_OVP	Bus Over Voltage Protection	Go
7h	BUS_OVP_ALM	Input Voltage Alarm	Go
8h	BUS_OCP_UCP	Input Current Limit	Go
9h	BUS_OCP_ALM	Input Current Alarm	Go
Ah	CONVERTER_STATE	Converter State	Go
Bh	CONTROL	Control Register	Go
Ch	CHRG_CTRL	Charger Control 1	Go
Dh	INT_STAT	INT STAT	Go
Eh	INT_FLAG	INT Flag	Go
Fh	INT_MASK	INT Mask	Go
10h	FLT_STAT	FAULT STAT	Go
11h	FLT_FLAG	FAULT FLAG	Go
12h	FLT_MASK	FAULT MASK	Go
13h	PART_INFO	Part Information	Go
14h	ADC_CTRL	ADC Control	Go
15h	ADC_FN_DIS	ADC Function Disable	Go

表 9-4. CUSTOMER Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	SECTION
16h	IBUS_ADC1	ADC BUS Current Measurement	Go
17h	IBUS_ADC0	ADC BUS Current Measurement	Go
18h	VBUS_ADC1	ADC BUS Voltage Measurement	Go
19h	VBUS_ADC0	ADC BUS Voltage Measurement	Go
1Ah	VAC_ADC1	ADC VAC Voltage Measurement	Go
1Bh	VAC_ADC0	ADC VAC Voltage Measurement	Go
1Ch	VOUT_ADC1	ADC OUT Voltage Measurement	Go
1Dh	VOUT_ADC0	ADC OUT Voltage Measurement	Go
1Eh	VBAT_ADC1	ADC BAT Voltage Measurement	Go
1Fh	VBAT_ADC0	ADC BAT Voltage Measurement	Go
20h	IBAT_ADC1	ADC BAT Current Measurement	Go
21h	IBAT_ADC0	ADC BAT Current Measurement	Go
22h	TSBUS_ADC1	ADC TSBUS Pin Voltage Measurement	Go
23h	TSBUS_ADC0	ADC TSBUS Pin Voltage Measurement	Go
24h	TSBAT_ADC1	ADC TSBAT Pin Voltage Measurement	Go
25h	TSBAT_ADC0	ADC TSBAT Pin Voltage Measurement	Go
26h	TDIE_ADC1	ADC Die Temperature Measurement	Go
27h	TDIE_ADC0	ADC Die Temperature Measurement	Go
28h	TSBUS_FLT1	TSBUS Pin Voltage Fault Setting	Go
29h	TSBAT_FLT0	TSBAT Pin Voltage Fault Setting	Go
2Ah	TDIE_ALM	Die Temp Fault Setting	Go
2Bh	CHG_CTRL	Charger Control	Go
2Ch	VOUT_OVP_STAT	VOUT_OVP status	Go
2Dh	VOUT_OVP_FLAG_MASK	VOUT_OVP FLAG and MASK	Go
2Eh	DEGLITCH	Deglitch Settings	Go

Complex bit access types are encoded to fit into small table cells. 表 9-5 shows the codes that are used for access types in this section.

表 9-5. CUSTOMER Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value x may be 0 or 1

9.6.1.1 BAT_OVP Register (Address = 0h) [reset = 22h]

BAT_OVP is shown in 図 9-13 and described in 表 9-6.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-13. BAT_OVP Register

7	6	5	4	3	2	1	0
BAT_OVP_DIS	RESERVED	BAT_OVP[5]	BAT_OVP[4]	BAT_OVP[3]	BAT_OVP[2]	BAT_OVP[1]	BAT_OVP[0]
R/W-0h	0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

表 9-6. BAT_OVP Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OVP_DIS	R/W	0h	Y	N	N/A	Disable BAT_OVP
6	RESERVED		0h				
5	BAT_OVP[5]	R/W	1h	Y	N	800 mV	Battery Overvoltage Protection Setting. When the battery voltage goes above the programmed threshold, and $\overline{INT}$ is sent, the output is disabled and CHG_EN is set to 0. The host controller should monitor the battery voltage to ensure that the adapter keeps the voltage under this threshold for proper operation. The setting is determined by BAT_OVP = 3.475 V + BAT_OVP[5:0]*25 mV Default: 4.35 V (b 10 0010)
4	BAT_OVP[4]	R/W	0h	Y	N	400 mV	
3	BAT_OVP[3]	R/W	0h	Y	N	200 mV	
2	BAT_OVP[2]	R/W	0h	Y	N	100 mV	
1	BAT_OVP[1]	R/W	1h	Y	N	50 mV	
0	BAT_OVP[0]	R/W	0h	Y	N	25 mV	

9.6.1.2 BAT_OVP_ALM Register (Address = 1h) [reset = 1Ch]

BAT_OVP_ALM is shown in 図 9-14 and described in 表 9-7.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-14. BAT_OVP_ALM Register

7	6	5	4	3	2	1	0
BAT_OVP_ALM_DIS	RESERVED	BAT_OVP_ALM[5]	BAT_OVP_ALM[4]	BAT_OVP_ALM[3]	BAT_OVP_ALM[2]	BAT_OVP_ALM[1]	BAT_OVP_ALM[0]
R/W-0h	0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

表 9-7. BAT_OVP_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCHDOG	Bit Value	Description
7	BAT_OVP_ALM_DIS	R/W	0h	Y	N	N/A	Disable BAT_OVP_ALM
6	RESERVED		0h				
5	BAT_OVP_ALM[5]	R/W	0h	Y	N	800 mV	Battery Overvoltage Alarm Setting. When the battery voltage goes above the programmed threshold an INT is sent. The BAT_OVP_ALM should be set lower than BAT_OVP and the host controller should monitor the battery voltage to ensure that the adapter keeps the voltage under the BAT_OVP threshold for proper operation. The setting is determined by BAT_OVP_ALM = 3.5 V + BAT_OVP_ALM[5:0]*25 mV Default: 4.2 V (b01 1100)
4	BAT_OVP_ALM[4]	R/W	1h	Y	N	400 mV	
3	BAT_OVP_ALM[3]	R/W	1h	Y	N	200 mV	
2	BAT_OVP_ALM[2]	R/W	1h	Y	N	100 mV	
1	BAT_OVP_ALM[1]	R/W	0h	Y	N	50 mV	
0	BAT_OVP_ALM[0]	R/W	0h	Y	N	25 mV	

9.6.1.3 BAT_OCP Register (Address = 2h) [reset = 3Dh]

BAT_OCP is shown in 図 9-15 and described in 表 9-8.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-15. BAT_OCP Register

7	6	5	4	3	2	1	0
BAT_OCP_DIS	BAT_OCP[6]	BAT_OCP[5]	BAT_OCP[4]	BAT_OCP[3]	BAT_OCP[2]	BAT_OCP[1]	BAT_OCP[0]
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h

表 9-8. BAT_OCP Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OCP_DIS	R/W	0h	Y	N	N/A	Disable BAT_OCP
6	BAT_OCP[6]	R/W	0h	Y	N	6400 mA	Battery Overcurrent Protection Setting. Any setting over 10 A is set to 10 A. When the battery current goes above the programmed threshold, the output is disabled. The host controller should monitor the battery current to ensure that the adapter keeps the current under this threshold for proper operation. The setting is determined by BAT_OCP = 2 A + BAT_OCP[6:0]*100 mA Default: 8.1 A (b 011 1101)
5	BAT_OCP[5]	R/W	1h	Y	N	3200 mA	
4	BAT_OCP[4]	R/W	1h	Y	N	1600 mA	
3	BAT_OCP[3]	R/W	1h	Y	N	800 mA	
2	BAT_OCP[2]	R/W	1h	Y	N	400 mA	
1	BAT_OCP[1]	R/W	0h	Y	N	200 mA	
0	BAT_OCP[0]	R/W	1h	Y	N	100 mA	

9.6.1.4 BAT_OCP_ALM Register (Address = 3h) [reset = 3Ch]

BAT_OCP_ALM is shown in 図 9-16 and described in 表 9-9.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-16. BAT_OCP_ALM Register

7	6	5	4	3	2	1	0
BAT_OCP_ALM_DIS	BAT_OCP_ALM[6]	BAT_OCP_ALM[5]	BAT_OCP_ALM[4]	BAT_OCP_ALM[3]	BAT_OCP_ALM[2]	BAT_OCP_ALM[1]	BAT_OCP_ALM[0]
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h

表 9-9. BAT_OCP_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OCP_ALM_DIS	R/W	0h	Y	N	N/A	Disable BAT_OCP_ALM
6	BAT_OCP_ALM[6]	R/W	0h	Y	N	6400 mA	Battery Overcurrent Alarm Setting. When the battery current goes above the programmed threshold an $\overline{INT}$ is sent. The BAT_OCP_ALM should be set lower than the BAT_OCP and the host controller should monitor the battery current to ensure that the adapter keeps the current under the BAT_OCP threshold for proper operation. The setting is determined by BAT_OCP_ALM = 2 A + BAT_OCP_ALM[6:0]*100 mA Default: 8 A
5	BAT_OCP_ALM[5]	R/W	1h	Y	N	3200 mA	
4	BAT_OCP_ALM[4]	R/W	1h	Y	N	1600 mA	
3	BAT_OCP_ALM[3]	R/W	1h	Y	N	800 mA	
2	BAT_OCP_ALM[2]	R/W	1h	Y	N	400 mA	
1	BAT_OCP_ALM[1]	R/W	0h	Y	N	200 mA	
0	BAT_OVP_ALM[0]	R/W	0h	Y	N	100 mA	

9.6.1.5 BAT_UCP_ALM Register (Address = 4h) [reset = 28h]

BAT_UCP_ALM is shown in 図 9-17 and described in 表 9-10.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-17. BAT_UCP_ALM Register

7	6	5	4	3	2	1	0
BAT_UCP_ALM_DIS	BAT_UCP_ALM[6]	BAT_UCP_ALM[5]	BAT_UCP_ALM[4]	BAT_UCP_ALM[3]	BAT_UCP_ALM[2]	BAT_UCP_ALM[1]	BAT_UCP_ALM[0]
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

表 9-10. BAT_UCP_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_UCP_ALM_DIS	R/W	0h	Y	N	N/A	Disable BAT_UCP_ALM
6	BAT_UCP_ALM[6]	R/W	0h	Y	N	3200 mA	Battery Undercurrent Alarm Setting. When the battery current falls below the programmed threshold, an $\overline{INT}$ is sent. The host controller should monitor the battery current to determine when to disable the BQ25968 and hand overcharging to the switching charger. The setting is determined by BAT_UCP_ALM = BAT_UCP_ALM[7:0]*50 mA Default: 2 A (b0101000)
5	BAT_UCP_ALM[5]	R/W	1h	Y	N	1600 mA	
4	BAT_UCP_ALM[4]	R/W	0h	Y	N	800 mA	
3	BAT_UCP_ALM[3]	R/W	1h	Y	N	400 mA	
2	BAT_UCP_ALM[2]	R/W	0h	Y	N	200 mA	
1	BAT_UCP_ALM[1]	R/W	0h	Y	N	100 mA	
0	BAT_UCP_ALM[0]	R/W	0h	Y	N	50 mA	

9.6.1.6 AC_PROTECTION Register (Address = 5h) [reset = 3h]

AC_PROTECTION is shown in 図 9-18 and described in 表 9-11.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-18. AC_PROTECTION Register

7	6	5	4	3	2	1	0
AC_OVP_STAT	AC_OVP_FLAG	AC_OVP_MASK	RESERVED		AC_OVP[2]	AC_OVP[1]	AC_OVP[0]
R-0h	R-0h	R/W-0h	R-x		R/W-0h	R/W-1h	R/W-1h

表 9-11. AC_PROTECTION Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	AC_OVP_STAT	R	0h	Y	N/A	N/A	Status of AC_OVP. Persists until condition is no longer valid.
6	AC_OVP_FLAG	R	0h	Y	N/A	N/A	Set when an AC_OVP event occurs. Cleared upon read.
5	AC_OVP_MASK	R/W	0h	Y	N	N/A	Masks an AC_OVP event from sending an INT.
4-3	RESERVED	R	x	N	N	N/A	RESERVED
2	AC_OVP[2]	R/W	0h	Y	N	4 V	Bus Overvoltage Protection Setting. When the bus voltage reaches the programmed threshold, OVPGATE turns off the OVP FET. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under this threshold for proper operation. The setting is determined by AC_OVP = 11 V + AC_OVP[3:0]*1 V Writing all 1s to these bits sets the AC_OVP to 6.5 V
1	AC_OVP[1]	R/W	1h	Y	N	2 V	
0	AC_OVP[0]	R/W	1h	Y	N	1 V	

9.6.1.7 BUS_OVP Register (Address = 6h) [reset = 3Ah]

BUS_OVP is shown in 図 9-19 and described in 表 9-12.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-19. BUS_OVP Register

7	6	5	4	3	2	1	0
VBUS_PD_EN	BUS_OVP[6]	BUS_OVP[5]	BUS_OVP[4]	BUS_OVP[3]	BUS_OVP[2]	BUS_OVP[1]	BUS_OVP[0]
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

表 9-12. BUS_OVP Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	VBUS_PD_EN	R/W	0h	Y	N	N/A	0: Pulldown disabled, 1: Pulldown enabled Enabling this will turn off the external OVPFET, and conduct current from VBUS to GND through an internal diode. Any time the OVPFET charge pump is not running, this pulldown device will be active to help discharge VBUS after a hot-plug event.
6	BUS_OVP[6]	R/W	0h	Y	N	3200 mV	Bus Overvoltage Setting. When the bus voltage reaches the programmed threshold, QB is turned off and CH_EN is set to 0. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under the BUS_OVP threshold for proper operation. The setting is determined by BUS_OVP = 5.95 V + BUS_OVP[6:0]*50 mV Default: 8.9 V (b011 1010)
5	BUS_OVP[5]	R/W	1h	Y	N	1600 mV	
4	BUS_OVP[4]	R/W	1h	Y	N	800 mV	
3	BUS_OVP[3]	R/W	1h	Y	N	400 mV	
2	BUS_OVP[2]	R/W	0h	Y	N	200 mV	
1	BUS_OVP[1]	R/W	1h	Y	N	100 mV	
0	BUS_OVP[0]	R/W	0h	Y	N	50 mV	

9.6.1.8 BUS_OVP_ALM Register (Address = 7h) [reset = 38h]

BUS_OVP_ALM is shown in 図 9-20 and described in 表 9-13.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-20. BUS_OVP_ALM Register

7	6	5	4	3	2	1	0
BUS_OVP_ALM_DIS	BUS_OVP_ALM[6]	BUS_OVP_ALM[5]	BUS_OVP_ALM[4]	BUS_OVP_ALM[3]	BUS_OVP_ALM[2]	BUS_OVP_ALM[1]	BUS_OVP_ALM[0]
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

表 9-13. BUS_OVP_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BUS_OVP_ALM_DIS	R/W	0h	Y	N	N/A	Disable BUS_OVP_ALM
6	BUS_OVP_ALM[6]	R/W	0h	Y	N	3200 mV	Bus Overvoltage Alarm Setting. When the bus voltage reaches the programmed threshold, an INT is sent. The host controller should monitor the bus voltage to ensure that the adapter keeps the voltage under the BUS_OVP threshold for proper operation. The setting is determined by BUS_OVP_ALM = 6 V + BUS_OVP_ALM[6:0]*50 mV Default: 8.8 V (b011 1000)
5	BUS_OVP_ALM[5]	R/W	1h	Y	N	1600 mV	
4	BUS_OVP_ALM[4]	R/W	1h	Y	N	800 mV	
3	BUS_OVP_ALM[3]	R/W	1h	Y	N	400 mV	
2	BUS_OVP_ALM[2]	R/W	0h	Y	N	200 mV	
1	BUS_OVP_ALM[1]	R/W	0h	Y	N	100 mV	
0	BUS_OVP_ALM[0]	R/W	0h	Y	N	50 mV	

9.6.1.9 BUS_OCP_UCP Register (Address = 8h) [reset = Dh]

BUS_OCP_UCP is shown in 図 9-21 and described in 表 9-14.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-21. BUS_OCP_UCP Register

7	6	5	4	3	2	1	0
BUS_OCP_DIS	IBUS_UCP_RISE_FLAG	IBUS_UCP_RISE_MASK	IBUS_UCP_FALL_FLAG	BUS_OCP[3]	BUS_OCP[2]	BUS_OCP[1]	BUS_OCP[0]
R/W-0h	R-0h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-0h	R/W-1h

表 9-14. BUS_OCP_UCP Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BUS_OCP_DIS	R/W	0h	Y	N	N/A	BUS_OCP Disable
6	IBUS_UCP_RISE_FLAG	R	0h	Y	N/A	N/A	Bus Undercurrent Threshold Rising Flag. An $\overline{INT}$ is sent when this occurs, and is cleared upon read.
5	IBUS_UCP_RISE_MASK	R/W	0h	Y	N	N/A	Bus Undercurrent Threshold Rising $\overline{INT}$ Mask. 0: Not Masked, 1: Masked
4	IBUS_UCP_FALL_FLAG	R	0h	Y	N/A	N/A	Bus Undercurrent Threshold Falling Flag. An $\overline{INT}$ is sent when this occurs, and is cleared upon read.
3	BUS_OCP[3]	R/W	1h	Y	N	2 A	Bus Overcurrent Protection Setting. When the bus current reaches the programmed threshold, the output is disabled. The host controller should monitor the bus current to ensure that the adapter keeps the current under this threshold for proper operation. The setting is determined by BUS_OCP = 1 A + BUS_OCP[6:0]*250 mA Default: 4.25 A (b1101)
2	BUS_OCP[2]	R/W	1h	Y	N	1 A	
1	BUS_OCP[1]	R/W	0h	Y	N	500 mA	
0	BUS_OCP[0]	R/W	1h	Y	N	250 mA	

9.6.1.10 BUS_OCP_ALM Register (Address = 9h) [reset = 50h]

BUS_OCP_ALM is shown in 図 9-22 and described in 表 9-15.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-22. BUS_OCP_ALM Register

7	6	5	4	3	2	1	0
BUS_OCP_ALM_DIS	BUS_OCP_ALM[6]	BUS_OCP_ALM[5]	BUS_OCP_ALM[4]	BUS_OCP_ALM[3]	BUS_OCP_ALM[2]	BUS_OCP_ALM[1]	BUS_OCP_ALM[0]
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9-15. BUS_OCP_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	BUS_OCP_ALM_DIS	R/W	0h	Y	N	N/A	BUS_OCP_ALM Disable
6	BUS_OCP_ALM[6]	R/W	1h	Y	N	3200 mA	Bus Overcurrent Alarm Setting. When the bus current reaches the programmed threshold, an $\overline{INT}$ is sent. The host controller should monitor the bus current to ensure that the adapter keeps the current under BUS_OCP for proper operation. The setting is determined by BUS_OCP_ALM = BUS_OCP_ALM[6:0]*50 mA - 50 mA Writing all 0s is 0 A Default: 4 A (b1010000)
5	BUS_OCP_ALM[5]	R/W	0h	Y	N	1600 mA	
4	BUS_OCP_ALM[4]	R/W	1h	Y	N	800 mA	
3	BUS_OCP_ALM[3]	R/W	0h	Y	N	400 mA	
2	BUS_OCP_ALM[2]	R/W	0h	Y	N	200 mA	
1	BUS_OCP_ALM[1]	R/W	0h	Y	N	100 mA	
0	BUS_OCP_ALM[0]	R/W	0h	Y	N	50 mA	

9.6.1.11 CONVERTER_STATE Register (Address = Ah) [reset = 0h]

CONVERTER_STATE is shown in 図 9-23 and described in 表 9-16.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-23. CONVERTER_STATE Register

7	6	5	4	3	2	1	0
TSHUT_FLAG	TSHUT_STAT	VBUS_ERRORLO_STAT	VBUS_ERRORHI_STAT	SS_TIMEOUT_FLAG	CONV_SWITCHING_STAT	CONV_OCP_FLAG	FLYCAP_SHORT_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 9-16. CONVERTER_STATE Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCHDOG	Bit Value	Description
7	TSHUT_FLAG	R	0h	Y	N/A	N/A	Thermal Shutdown Flag. An $\overline{INT}$ is sent when this event happens, and is cleared when read.
6	TSHUT_STAT	R	0h	Y	N/A	N/A	Thermal Shutdown Status. This register is 1 until the event no longer persists.
5	VBUS_ERRORLO_STAT	R	0h	Y	N/A	N/A	VBUS is too low for the converter to start switching. This bit shows the current status, and is 0 only when the event is not happening.
4	VBUS_ERRORHI_STAT	R	0h	Y	N/A	N/A	VBUS is too high for the converter to start switching. This bit shows the current status, and is 0 only when the event is not happening.
3	SS_TIMEOUT_FLAG	R	0h	N	N/A	N/A	Soft-Start Timeout Flag. If the current is not ramped to the proper level in SS_TIMEOUT_SET[1:0] time, the converter will stop switching. An $\overline{INT}$ is sent when this event happens, and is cleared when read.
2	CONV_SWITCHING_STAT	R	0h	N	N/A	N/A	An interrupt is sent when the converter starts switching and the SS timer starts. The adapter current must be ramped to the IBUS_UCP_RISE threshold SS_TIMEOUT or switching will stop. This bit is not maskable. Only one $\overline{INT}$ is set when switching starts. The bit can be read at any time to determine if the part is switching or not.
1	CONV_OCP_FLAG	R	0h	N	N/A	N/A	Converter Overcurrent Flag. When any internal switching FET reaches current limit, an $\overline{INT}$ is sent when this event happens, and is cleared when read.

表 9-16. CONVERTER_STATE Register Field Descriptions (continued)

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCHDOG	Bit Value	Description
0	PIN_DIAG_FAIL_FLAG	R	0h	Y	N/A	N/A	Pin Diagnostic Fail Flag. When CHG_EN is set to '1', several fault conditions are checked on the CFLY and VOUT pins to ensure proper operation. If a diagnostic fails, an $\overline{INT}$ is sent when this event happens, and is cleared when read.

9.6.1.12 CONTROL Register (Address = Bh) [reset = 40h]

CONTROL is shown in 図 9-24 and described in 表 9-17.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-24. CONTROL Register

7	6	5	4	3	2	1	0
REG_RST	FSW_SET[2:0]			WD_TIMEOUT_FLAG	WATCHDOG_DIS	WATCHDOG[1:0]	
R/W-0h	R/W-4h			R-0h	R/W-0h	R/W-0h	

表 9-17. CONTROL Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCHDOG	Bit Value	Description
7	REG_RST	R/W	0h	Y	N	N/A	0 = No Register Reset 1 = Reset Registers to their Default Values Always reads 0
6	FSW_SET[2]	R/W	1h	N	N	N/A	Set the Switching Frequency 000: Slowest (187.5 kHz) 001: 250 kHz 010: 300 kHz 011: 375 kHz 100: 500 kHz (default) 101-111: Fastest (750 kHz) If master or slave, max frequency is 500 kHz
5	FSW_SET[1]	R/W	0h	N	N	N/A	
4	FSW_SET[0]	R/W	0h	N	N	N/A	
3	WD_TIMEOUT_FLAG	R	0h	Y	N/A	N/A	Watchdog Timeout Flag. An INT is sent when this event happens, and is cleared when read.
2	WATCHDOG_DIS	R/W	0h	Y	N	N/A	0 = Watchdog Enabled 1 = Watchdog Disabled
1	WATCHDOG[1]	R/W	0h	Y	N	N/A	Watchdog Timing, (Cleared by any completed read or write I^2C transaction) 00 = 0.5 s (default) 01 = 1 s 10 = 5 s 11 = 30 s
0	WATCHDOG[0]	R/W	0h	Y	N	N/A	

9.6.1.13 CHRG_CTRL Register (Address = Ch) [reset = 0h]

CHRG_CTRL is shown in 図 9-25 and described in 表 9-18.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-25. CHRG_CTRL Register

7	6	5	4	3	2	1	0
CHG_EN	MS[1:0]		FREQ_SHIFT[1:0]		TSBUS_DIS	TSBAT_DIS	TDIE_DIS
R/W-0h	R-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h

表 9-18. CHRG_CTRL Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by Reg_RST	Reset by WATCH DOG	Bit Value	Description
7	CHG_EN	R/W	0h	Y	Y	N/A	0 = Charge disabled 1 = Charge enabled
6-5	MS[1:0]	R	0h	Y	N/A	N/A	Master, Slave, or Standalone Operation. 00 = Standalone 01 = Slave 1X = Master
4-3	FREQ_SHIFT[1:0]	R/W	0h	Y	N	N/A	Adjust Fsw for EMI. 00 = Nominal Frequency 01 = +10% 10 = –10% 11 = Spread Spectrum varies frequency ±10%
2	TSBUS_DIS	R/W	0h	Y	N	N/A	Disable TSBUS protection function. 0 = Enabled 1 = Disable
1	TSBAT_DIS	R/W	0h	Y	N	N/A	Disable TSBAT protection function. 0 = Enabled 1 = Disable
0	TDIE_DIS	R/W	0h	Y	N	N/A	Disable TDIE protection function.

9.6.1.14 INT_STAT Register (Address = Dh) [reset = xh]

INT_STAT is shown in 図 9-26 and described in 表 9-19.

Return to Summary Table.

Shows current status. All bits are RESET BY REG_RST.

図 9-26. INT_STAT Register

7	6	5	4	3	2	1	0
BAT_OVP_ALM_STAT	BAT_OCP_ALM_STAT	BUS_OVP_ALM_STAT	BUS_OCP_ALM_STAT	BAT_UCP_ALM_STAT	ADAPTER_INSERT_STAT	VBAT_INSERT_STAT	ADC_DONE_STAT
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

表 9-19. INT_STAT Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset By WATCHDOG	Bit Value	Description
7	BAT_OVP_ALM_STAT	R	x	N	N/A	N/A	BAT_OVP_ALM threshold is exceeded.
6	BAT_OCP_ALM_STAT	R	x	N	N/A	N/A	BAT_OCP_ALM threshold is exceeded.
5	BUS_OVP_ALM_STAT	R	x	N	N/A	N/A	BUS_OVP_ALM threshold is exceeded.
4	BUS_OCP_ALM_STAT	R	x	N	N/A	N/A	BUS_OCP_ALM threshold is exceeded.
3	BAT_UCP_ALM_STAT	R	x	N	N/A	N/A	BAT_UCP_ALM is below the threshold.
2	ADAPTER_INSERT_STAT	R	x	N	N/A	N/A	BUS voltage is present and above the VBUS UVLO threshold.
1	VBAT_INSERT_STAT	R	x	N	N/A	N/A	BAT voltage is present.
0	ADC_DONE_STAT	R	x	N	N/A	N/A	Indicates if the ADC conversion is complete for the requested parameters in 1-Shot Mode only. This bit will change to '0' when an ADC conversion is requested in 1-Shot Mode, and it will change back to '1' when the conversion is complete. During continuous conversion mode, this bit will be 0. 0 = Conversion not complete 1 = Conversion complete

9.6.1.15 INT_FLAG Register (Address = Eh) [reset = xh]

INT_FLAG is shown in 図 9-27 and described in 表 9-20.

Return to Summary Table.

Only clears upon read. All bits are RESET BY REG_RST.

図 9-27. INT_FLAG Register

7	6	5	4	3	2	1	0
BAT_OVP_ALM_FLAG	BAT_OCP_ALM_FLAG	BUS_OVP_ALM_FLAG	BUS_OCP_ALM_FLAG	BAT_UCP_ALM_FLAG	ADAPTER_INSERT_FLAG	VBAT_INSERT_FLAG	ADC_DONE_FLAG
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

表 9-20. INT_FLAG Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OVP_ALM_FLAG	R	x	N	N/A	N/A	BAT_OVP_ALM threshold has been exceeded.
6	BAT_OCP_ALM_FLAG	R	x	N	N/A	N/A	BAT_OCP_ALM threshold has been exceeded.
5	BUS_OVP_ALM_FLAG	R	x	N	N/A	N/A	BUS_OVP_ALM threshold has been exceeded.
4	BUS_OCP_ALM_FLAG	R	x	N	N/A	N/A	BUS_OCP_ALM threshold has been exceeded.
3	BAT_UCP_ALM_FLAG	R	x	N	N/A	N/A	BAT_UCP_ALM has fallen below the threshold.
2	ADAPTER_INSERT_FLAG	R	x	N	N/A	N/A	BUS voltage has been present and above the VBUS UVLO threshold.
1	VBAT_INSERT_FLAG	R	x	N	N/A	N/A	BAT votlage has been present.
0	ADC_DONE_FLAG	R	x	N	N/A	N/A	0 = Conversion not complete 1 = Conversion complete

9.6.1.16 INT_MASK Register (Address = Fh) [reset = 0h]

INT_MASK is shown in 図 9-28 and described in 表 9-21.

Return to Summary Table.

INT will not assert low if enabled. All bits are RESET BY REG_RST.

図 9-28. INT_MASK Register

7	6	5	4	3	2	1	0
BAT_OVP_ALM_MASK	BAT_OCP_ALM_MASK	BUS_OVP_ALM_MASK	BUS_OCP_ALM_MASK	BAT_UCP_ALM_MASK	ADAPTER_INSERT_MASK	VBAT_INSERT_MASK	ADC_DONE_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9-21. INT_MASK Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OVP_ALM_MASK	R/W	0h	Y	N	N/A	Masks BAT Overvoltage Alarm Event. 0 = Not Masked 1 = Masked
6	BAT_OCP_ALM_MASK	R/W	0h	Y	N	N/A	Masks BAT Overcurrent Alarm Event. 0 = Not Masked 1 = Masked
5	BUS_OVP_ALM_MASK	R/W	0h	Y	N	N/A	Masks BUS Overvoltage Alarm Event. 0 = Not Masked 1 = Masked
4	BUS_OCP_ALM_MASK	R/W	0h	Y	N	N/A	Masks BUS Overcurrent Alarm Event. 0 = Not Masked 1 = Masked
3	BAT_UCP_ALM_MASK	R/W	0h	Y	N	N/A	Masks BAT_UCP Alarm Event. 0 = Not Masked 1 = Masked
2	ADAPTER_INSERT_MASK	R/W	0h	Y	N	N/A	Masks a ADAPTER_INSERT Event. 0 = Not Masked 1 = Masked
1	VBAT_INSERT_MASK	R/W	0h	Y	N	N/A	Masks a VBAT INSERT EVENT. 0 = Not Masked 1 = Masked
0	ADC_DONE_MASK	R/W	0h	Y	N	N/A	Masks a ADC DONE Event. 0 = Not Masked 1 = Masked

9.6.1.17 FLT_STAT Register (Address = 10h) [reset = xh]

FLT_STAT is shown in 図 9-29 and described in 表 9-22.

Return to Summary Table.

Shows current status. All bits are RESET BY REG_RST.

図 9-29. FLT_STAT Register

7	6	5	4	3	2	1	0
BAT_OVP_FLT_STAT	BAT_OCP_FLT_STAT	BUS_OVP_FLT_STAT	BUS_OCP_FLT_STAT	TSBUS_TSBAT_ALM_STAT	TSBAT_FLT_STAT	TSBUS_FLT_STAT	TDIE_ALM_STAT
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

表 9-22. FLT_STAT Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCHDOG	Bit Value	Description
7	BAT_OVP_FLT_STAT	R	x	N	N/A	N/A	Indicates a BAT Overvoltage Event is occurring.
6	BAT_OCP_FLT_STAT	R	x	N	N/A	N/A	Indicates a BAT Overcurrent Event is occurring.
5	BUS_OVP_FLT_STAT	R	x	N	N/A	N/A	Indicates a BUS Overvoltage Event is occurring.
4	BUS_OCP_FLT_STAT	R	x	N	N/A	N/A	Indicates a BUS Overcurrent Event is occurring.
3	TSBUS_TSBAT_ALM_STAT	R	x	N	N/A	N/A	Indicates that the TSBUS or TSBAT threshold is within 5% of the TSBUS_FLT or TSBAT_FLT set threshold.
2	TSBAT_FLT_STAT	R	x	N	N/A	N/A	Indicates a BAT Over Temp Fault has Occurred TSBAT voltage falls below TSBAT_FLT setting.
1	TSBUS_FLT_STAT	R	x	N	N/A	N/A	Indicates a BUS Over Temp Fault has Occurred TSBUS votlage falls below TSBUS_FLT setting.
0	TDIE_ALM_STAT	R	x	N	N/A	N/A	Indicates a DIE Over Temp Fault has Occurred TDIE_ALM temp has been exceeded.

9.6.1.18 FLT_FLAG Register (Address = 11h) [reset = xh]

FLT_FLAG is shown in 図 9-30 and described in 表 9-23.

Return to Summary Table.

Only clears upon read. All bits are RESET BY REG_RST.

図 9-30. FLT_FLAG Register

7	6	5	4	3	2	1	0
BAT_OVP_FLT_FLAG	BAT_OCP_FLT_FLAG	BUS_OVP_FLT_FLAG	BUS_OCP_FLT_FLAG	TSBUS_TSBAT_ALM_FLAG	TSBAT_FLT_FLAG	TSBUS_FLT_FLAG	TDIE_ALM_FLAG
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

表 9-23. FLT_FLAG Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset by WATCHDOG	Bit Value	Description
7	BAT_OVP_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BAT Overvoltage Event has occurred.
6	BAT_OCP_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BAT Overcurrent Event has occurred.
5	BUS_OVP_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BUS Overvoltage Event has occurred.
4	BUS_OCP_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BUS Overcurrent Event has occurred.
3	TSBUS_TSBAT_ALM_FLAG	R	x	N	N/A	N/A	Indicates that the TSBUS or TSBAT threshold has been within 5% of the TSBUS_FLT or TSBAT_FLT set threshold.
2	TSBAT_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BAT Temp Fault has Occurred.
1	TSBUS_FLT_FLAG	R	x	N	N/A	N/A	Indicates a BUS Temp Fault has Occurred.
0	TDIE_ALM_FLAG	R	x	N	N/A	N/A	Indicates a DIE Temp Fault has Occurred.

9.6.1.19 FLT_MASK Register (Address = 12h) [reset = 0h]

FLT_MASK is shown in 図 9-31 and described in 表 9-24.

Return to Summary Table.

INT will not assert if enabled. All bits are RESET BY REG_RST.

図 9-31. FLT_MASK Register

7	6	5	4	3	2	1	0
BAT_OVP_FLT_MASK	BAT_OCP_FLT_MASK	BUS_OVP_FLT_MASK	BUS_OCP_FLT_MASK	TSBUS_TSBAT_ALM_MASK	TSBAT_FLT_MASK	TSBUS_FLT_MASK	TDIE_ALM_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9-24. FLT_MASK Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	BAT_OVP_FLT_MASK	R/W	0h	Y	N	N/A	Masks BAT Overvoltage Event. 0 = Not Masked 1 = Masked
6	BAT_OCP_FLT_MASK	R/W	0h	Y	N	N/A	Masks BAT Overcurrent Event. 0 = Not Masked 1 = Masked
5	BUS_OVP_FLT_MASK	R/W	0h	Y	N	N/A	Masks BUS Overvoltage Event. 0 = Not Masked 1 = Masked
4	BUS_OCP_FLT_MASK	R/W	0h	Y	N	N/A	Masks BUS Overcurrent Event. 0 = Not Masked 1 = Masked
3	TSBUS_TSBAT_ALM_MASK	R/W	0h	Y	N	N/A	Masks TSBUS_TSBAT_ALM Event. 0 = Not Masked 1 = Masked
2	TSBAT_FLT_MASK	R/W	0h	Y	N	N/A	Masks a BAT Temp Fault. 0 = Not Masked 1 = Masked
1	TSBUS_FLT_MASK	R/W	0h	Y	N	N/A	Masks a BUS Temp Fault. 0 = Not Masked 1 = Masked
0	TDIE_ALM_MASK	R/W	0h	Y	N	N/A	Masks a DIE Temp Fault. 0 = Not Masked 1 = Masked

9.6.1.20 PART_INFO Register (Address = 13h) [reset = xh]

PART_INFO is shown in 図 9-32 and described in 表 9-25.

Return to Summary Table.

図 9-32. PART_INFO Register

7	6	5	4	3	2	1	0
RESERVED[7:4]				DEVICE_ID[3:0]			
R-x				R-x			

表 9-25. PART_INFO Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset By WATCHDOG	Bit Value	Description
7	RESERVED		0				
6	RESERVED		0				
5	RESERVED		0				
4	RESERVED		1				
3	DEVICE_ID[3]	R	x	x	N/A	x	Device ID 0000 = BQ25970 0001= BQ25971 0110= BQ25968
2	DEVICE_ID[2]	R	x	x	N/A	x	
1	DEVICE_ID[1]	R	x	x	N/A	x	
0	DEVICE_ID[0]	R	x	x	N/A	x	

9.6.1.21 ADC_CTRL Register (Address = 14h) [reset = xh]

ADC_CTRL is shown in 図 9-33 and described in 表 9-26.

Return to Summary Table.

Bits 7-3 and bit 0 are RESET BY REG_RST.

図 9-33. ADC_CTRL Register

7	6	5	4	3	2	1	0
ADC_EN	ADC_RATE	ADC_AVG	ADC_AVG_INIT	ADC_SAMPLE[1:0]		RESERVED	IBUS_ADC_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		0	R/W-0h

表 9-26. ADC_CTRL Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset By WATCH DOG	Bit Value	Description
7	ADC_EN	R/W	0h	Y	Y	N/A	Enable ADC 0 = Disabled 1 = Enabled
6	ADC_RATE	R/W	0h	Y	N	N/A	0 = Continuous Conversion 1 = One-shot
5	ADC_AVG	R/W	0h	Y	N	N/A	0 = Single Value 1 = Running Average
4	ADC_AVG_INIT	R/W	0h	Y	N	N/A	0 = Start averaging using the existing register value 1 = Start averaging using a new ADC conversion
3-2	ADC_SAMPLE[1:0]	R/W	0h	Y	N	N/A	Sample speed of the ADC. 00 = 15-bit effective resolution 01 = 14-bit effective resolution 10 = 13-bit effective resolution 11 = 12-bit effective resolution
1	RESERVED		0				
0	IBUS_ADC_DIS	R/W	0h	Y	N	N/A	0 = Enable Conversion 1 = Disable Conversion

9.6.1.22 ADC_FN_DISABLE Register (Address = 15h) [reset = 0h]

ADC_FN_DIS is shown in 図 9-34 and described in 表 9-27.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-34. ADC_FN_DISABLE Register

7	6	5	4	3	2	1	0
VBUS_ADC_DIS	VAC_ADC_DIS	VOUT_ADC_DIS	VBAT_ADC_DIS	IBAT_ADC_DIS	TSBUS_ADC_DIS	TSBAT_ADC_DIS	TDIE_ADC_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 9-27. ADC_FN_DISABLE Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset By WATCH DOG	Bit Value	Description
7	VBUS_ADC_DIS	R/W	0h	Y	N	N/A	0 = Enable Conversion 1 = Disable Conversion
6	VAC_ADC_DIS	R/W	0h	Y	N	N/A	
5	VOUT_ADC_DIS	R/W	0h	Y	N	N/A	
4	VBAT_ADC_DIS	R/W	0h	Y	N	N/A	
3	IBAT_ADC_DIS	R/W	0h	Y	N	N/A	
2	TSBUS_ADC_DIS	R/W	0h	Y	N	N/A	
1	TSBAT_ADC_DIS	R/W	0h	Y	N	N/A	
0	TDIE_ADC_DIS	R/W	0h	Y	N	N/A	

9.6.1.23 IBUS_ADC1 Register (Address = 16h) [reset = xh]

IBUS_ADC1 is shown in 図 9-35 and described in 表 9-28.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-35. IBUS_ADC1 Register

7	6	5	4	3	2	1	0
IBUS_POL	IBUS_ADC[14:8]						
R-x	R-x						

表 9-28. IBUS_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset By WATCH DOG	Bit Value	Description
7	IBUS_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	IBUS_ADC[14]	R	x	Y	N/A	16384 mA	Current of IBUS
5	IBUS_ADC[13]	R	x	Y	N/A	8192 mA	
4	IBUS_ADC[12]	R	x	Y	N/A	4096 mA	
3	IBUS_ADC[11]	R	x	Y	N/A	2048 mA	
2	IBUS_ADC[10]	R	x	Y	N/A	1024 mA	
1	IBUS_ADC[9]	R	x	Y	N/A	512 mA	
0	IBUS_ADC[8]	R	x	Y	N/A	256 mA	

9.6.1.24 IBUS_ADC0 Register (Address = 17h) [reset = xh]

IBUS_ADC0 is shown in 図 9-36 and described in 表 9-29.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-36. IBUS_ADC0 Register

7	6	5	4	3	2	1	0
IBUS_ADC[7:0]							
R-x							

表 9-29. IBUS_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset By WATCH DOG	Bit Value	Description
7	IBUS_ADC[7]	R	x	Y	N/A	128 mA	
6	IBUS_ADC[6]	R	x	Y	N/A	64 mA	
5	IBUS_ADC[5]	R	x	Y	N/A	32 mA	
4	IBUS_ADC[4]	R	x	Y	N/A	16 mA	
3	IBUS_ADC[3]	R	x	Y	N/A	8 mA	
2	IBUS_ADC[2]	R	x	Y	N/A	4 mA	
1	IBUS_ADC[1]	R	x	Y	N/A	2 mA	
0	IBUS_ADC[0]	R	x	Y	N/A	1 mA	

9.6.1.25 VBUS_ADC1 Register (Address = 18h) [reset = xh]

VBUS_ADC1 is shown in 図 9-37 and described in 表 9-30.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-37. VBUS_ADC1 Register

7	6	5	4	3	2	1	0
VBUS_POL	VBUS_ADC[14:8]						
R-x	R-x						

表 9-30. VBUS_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset By WATCH DOG	Bit Value	Description
7	VBUS_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	VBUS_ADC[14]	R	x	Y	N/A	16384 mV	Voltage of VBUS
5	VBUS_ADC[13]	R	x	Y	N/A	8192 mV	
4	VBUS_ADC[12]	R	x	Y	N/A	4096 mV	
3	VBUS_ADC[11]	R	x	Y	N/A	2048 mV	
2	VBUS_ADC[10]	R	x	Y	N/A	1024 mV	
1	VBUS_ADC[9]	R	x	Y	N/A	512 mV	
0	VBUS_ADC[8]	R	x	Y	N/A	256 mV	

9.6.1.26 VBUS_ADC0 Register (Address = 19h) [reset = xh]

VBUS_ADC0 is shown in 図 9-38 and described in 表 9-31.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-38. VBUS_ADC0 Register

7	6	5	4	3	2	1	0
VBUS_ADC[7:0]							
R-x							

表 9-31. VBUS_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset By REG_RST	Reset By WATCH DOG	Bit Value	Description
7	VBUS_ADC[7]	R	x	Y	N/A	128 mV	
6	VBUS_ADC[6]	R	x	Y	N/A	64 mV	
5	VBUS_ADC[5]	R	x	Y	N/A	32 mV	
4	VBUS_ADC[4]	R	x	Y	N/A	16 mV	
3	VBUS_ADC[3]	R	x	Y	N/A	8 mV	
2	VBUS_ADC[2]	R	x	Y	N/A	4 mV	
1	VBUS_ADC[1]	R	x	Y	N/A	2 mV	
0	VBUS_ADC[0]	R	x	Y	N/A	1 mV	

9.6.1.27 VAC_ADC1 Register (Address = 1Ah) [reset = xh]

VAC_ADC1 is shown in 図 9-39 and described in 表 9-32.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-39. VAC_ADC1 Register

7	6	5	4	3	2	1	0
VAC_POL	VAC_ADC[14:8]						
R-x	R-x						

表 9-32. VAC_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VAC_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	VAC_ADC[14]	R	x	Y	N/A	16384 mV	Voltage of VAC
5	VAC_ADC[13]	R	x	Y	N/A	8192 mV	
4	VAC_ADC[12]	R	x	Y	N/A	4096 mV	
3	VAC_ADC[11]	R	x	Y	N/A	2048 mV	
2	VAC_ADC[10]	R	x	Y	N/A	1024 mV	
1	VAC_ADC[9]	R	x	Y	N/A	512 mV	
0	VAC_ADC[8]	R	x	Y	N/A	256 mV	

9.6.1.28 VAC_ADC0 Register (Address = 1Bh) [reset = xh]

VAC_ADC0 is shown in 図 9-40 and described in 表 9-33.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-40. VAC_ADC0 Register

7	6	5	4	3	2	1	0
VAC_ADC[7:0]							
R-x							

表 9-33. VAC_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VAC_ADC[7]	R	x	Y	N/A	128 mV	
6	VAC_ADC[6]	R	x	Y	N/A	64 mV	
5	VAC_ADC[5]	R	x	Y	N/A	32 mV	
4	VAC_ADC[4]	R	x	Y	N/A	16 mV	
3	VAC_ADC[3]	R	x	Y	N/A	8 mV	
2	VAC_ADC[2]	R	x	Y	N/A	4 mV	
1	VAC_ADC[1]	R	x	Y	N/A	2 mV	
0	VAC_ADC[0]	R	x	Y	N/A	1 mV	

9.6.1.29 VOUT_ADC1 Register (Address = 1Ch) [reset = xh]

VOUT_ADC1 is shown in 図 9-41 and described in 表 9-34.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-41. VOUT_ADC1 Register

7	6	5	4	3	2	1	0
VOUT_POL	VOUT_ADC[14:8]						
R-x	R-x						

表 9-34. VOUT_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VOUT_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	VOUT_ADC[14]	R	x	Y	N/A	16384 mV	Voltage of VOUT
5	VOUT_ADC[13]	R	x	Y	N/A	8192 mV	
4	VOUT_ADC[12]	R	x	Y	N/A	4096 mV	
3	VOUT_ADC[11]	R	x	Y	N/A	2048 mV	
2	VOUT_ADC[10]	R	x	Y	N/A	1024 mV	
1	VOUT_ADC[9]	R	x	Y	N/A	512 mV	
0	VOUT_ADC[8]	R	x	Y	N/A	256 mV	

9.6.1.30 VOUT_ADC0 Register (Address = 1Dh) [reset = xh]

VOUT_ADC0 is shown in 図 9-42 and described in 表 9-35.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-42. VOUT_ADC0 Register

7	6	5	4	3	2	1	0
VOUT_ADC[7:0]							
R-x							

表 9-35. VOUT_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VOUT_ADC[7]	R	x	Y	N/A	128 mV	
6	VOUT_ADC[6]	R	x	Y	N/A	64 mV	
5	VOUT_ADC[5]	R	x	Y	N/A	32 mV	
4	VOUT_ADC[4]	R	x	Y	N/A	16 mV	
3	VOUT_ADC[3]	R	x	Y	N/A	8 mV	
2	VOUT_ADC[2]	R	x	Y	N/A	4 mV	
1	VOUT_ADC[1]	R	x	Y	N/A	2 mV	
0	VOUT_ADC[0]	R	x	Y	N/A	1 mV	

9.6.1.31 VBAT_ADC1 Register (Address = 1Eh) [reset = xh]

VBAT_ADC1 is shown in 図 9-43 and described in 表 9-36.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-43. VBAT_ADC1 Register

7	6	5	4	3	2	1	0
VBAT_POL	VBAT_ADC[14:8]						
R-x	R-x						

表 9-36. VBAT_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VBAT_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative

表 9-36. VBAT_ADC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
6	VBAT_ADC[14]	R	x	Y	N/A	16384 mV	Voltage of VBAT
5	VBAT_ADC[13]	R	x	Y	N/A	8192 mV	
4	VBAT_ADC[12]	R	x	Y	N/A	4096 mV	
3	VBAT_ADC[11]	R	x	Y	N/A	2048 mV	
2	VBAT_ADC[10]	R	x	Y	N/A	1024 mV	
1	VBAT_ADC[9]	R	x	Y	N/A	512 mV	
0	VBAT_ADC[8]	R	x	Y	N/A	256 mV	

9.6.1.32 VBAT_ADC0 Register (Address = 1Fh) [reset = xh]

VBAT_ADC0 is shown in 図 9-44 and described in 表 9-37.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-44. VBAT_ADC0 Register

7	6	5	4	3	2	1	0
VBAT_ADC[7:0]							
R-x							

表 9-37. VBAT_ADC0 Register Field Descriptions

Bit	Field	Type	Reset	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	VBAT_ADC[7]	R	x	Y	N/A	128 mV	
6	VBAT_ADC[6]	R	x	Y	N/A	64 mV	
5	VBAT_ADC[5]	R	x	Y	N/A	32 mV	
4	VBAT_ADC[4]	R	x	Y	N/A	16 mV	
3	VBAT_ADC[3]	R	x	Y	N/A	8 mV	
2	VBAT_ADC[2]	R	x	Y	N/A	4 mV	
1	VBAT_ADC[1]	R	x	Y	N/A	2 mV	
0	VBAT_ADC[0]	R	x	Y	N/A	1 mV	

9.6.1.33 IBAT_ADC1 Register (Address = 20h) [reset = xh]

IBAT_ADC1 is shown in 図 9-45 and described in 表 9-38.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-45. IBAT_ADC1 Register

7	6	5	4	3	2	1	0
IBAT_POL	IBAT_ADC[14:8]						
R-x	R-x						

表 9-38. IBAT_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	IBAT_POL	R	x	Y	N/A	N/A	Positive is charging and negative is discharging. Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	IBAT_ADC[14]	R	x	Y	N/A	16384 mA	Current of IBAT
5	IBAT_ADC[13]	R	x	Y	N/A	8192 mA	
4	IBAT_ADC[12]	R	x	Y	N/A	4096 mA	
3	IBAT_ADC[11]	R	x	Y	N/A	2048 mA	
2	IBAT_ADC[10]	R	x	Y	N/A	1024 mA	
1	IBAT_ADC[9]	R	x	Y	N/A	512 mA	
0	IBAT_ADC[8]	R	x	Y	N/A	256 mA	

9.6.1.34 IBAT_ADC0 Register (Address = 21h) [reset = xh]

IBAT_ADC0 is shown in 図 9-46 and described in 表 9-39.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-46. IBAT_ADC0 Register

7	6	5	4	3	2	1	0
IBAT_ADC[7:0]							
R-x							

表 9-39. IBAT_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	IBAT_ADC[7]	R	x	Y	N/A	128 mA	
6	IBAT_ADC[6]	R	x	Y	N/A	64 mA	
5	IBAT_ADC[5]	R	x	Y	N/A	32 mA	
4	IBAT_ADC[4]	R	x	Y	N/A	16 mA	
3	IBAT_ADC[3]	R	x	Y	N/A	8 mA	
2	IBAT_ADC[2]	R	x	Y	N/A	4 mA	
1	IBAT_ADC[1]	R	x	Y	N/A	2 mA	
0	IBAT_ADC[0]	R	x	Y	N/A	1 mA	

9.6.1.35 TSBUS_ADC1 Register (Address = 22h) [reset = xh]

TSBUS_ADC1 is shown in 図 9-47 and described in 表 9-40.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-47. TSBUS_ADC1 Register

7	6	5	4	3	2	1	0
TSBUS_POL	TSBUS_ADC[14:8]						
R-x	R-x						

表 9-40. TSBUS_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBUS_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	TSBUS_ADC[14]	R	x	Y	N/A		TSBUS Pin Voltage as a Percentage of VOUT TSBUS Percentage = TSBUS_ADC[8:0] x 0.09766%
5	TSBUS_ADC[13]	R	x	Y	N/A		
4	TSBUS_ADC[12]	R	x	Y	N/A		
3	TSBUS_ADC[11]	R	x	Y	N/A		
2	TSBUS_ADC[10]	R	x	Y	N/A		
1	TSBUS_ADC[9]	R	x	Y	N/A	50%	
0	TSBUS_ADC[8]	R	x	Y	N/A	25%	

9.6.1.36 TSBUS_ADC0 Register (Address = 23h) [reset = xh]

TSBUS_ADC0 is shown in 図 9-48 and described in 表 9-41.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-48. TSBUS_ADC0 Register

7	6	5	4	3	2	1	0
TSBUS_ADC[7:0]							
R-x							

表 9-41. TSBUS_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBUS_ADC[7]	R	x	Y	N/A	12.5%	
6	TSBUS_ADC[6]	R	x	Y	N/A	6.25%	
5	TSBUS_ADC[5]	R	x	Y	N/A	3.125%	
4	TSBUS_ADC[4]	R	x	Y	N/A	1.5625%	
3	TSBUS_ADC[3]	R	x	Y	N/A	0.78125 %	
2	TSBUS_ADC[2]	R	x	Y	N/A	0.39063 %	
1	TSBUS_ADC[1]	R	x	Y	N/A	0.19531 %	
0	TSBUS_ADC[0]	R	x	Y	N/A	0.09766 %	

9.6.1.37 TSBAT_ADC1 Register (Address = 24h) [reset = xh]

TSBAT_ADC1 is shown in 図 9-49 and described in 表 9-42.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-49. TSBAT_ADC1 Register

7	6	5	4	3	2	1	0
TSBAT_POL	TSBAT_ADC[14:8]						
R-x	R-x						

表 9-42. TSBAT_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBAT_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0b = Result is positive 1b = Result is negative

表 9-42. TSBAT_ADC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
6	TSBAT_ADC[14]	R	x	Y	N/A		
5	TSBAT_ADC[13]	R	x	Y	N/A		
4	TSBAT_ADC[12]	R	x	Y	N/A		
3	TSBAT_ADC[11]	R	x	Y	N/A		
2	TSBAT_ADC[10]	R	x	Y	N/A		
1	TSBAT_ADC[9]	R	x	Y	N/A	50%	
0	TSBAT_ADC[8]	R	x	Y	N/A	25%	

9.6.1.38 TSBAT_ADC0 Register (Address = 25h) [reset = xh]

TSBAT_ADC0 is shown in 図 9-50 and described in 表 9-43.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-50. TSBAT_ADC0 Register

7	6	5	4	3	2	1	0
TSBAT_ADC[7:0]							
R-x							

表 9-43. TSBAT_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBAT_ADC[7]	R	x	Y	N/A	12.5%	TSBAT Pin Voltage as a Percentage of VOUT TSBAT Percentage = TSBAT_ADC[8:0] x 0.09766%
6	TSBAT_ADC[6]	R	x	Y	N/A	6.25%	
5	TSBAT_ADC[5]	R	x	Y	N/A	3.125%	
4	TSBAT_ADC[4]	R	x	Y	N/A	1.5625%	
3	TSBAT_ADC[3]	R	x	Y	N/A	0.78125 %	
2	TSBAT_ADC[2]	R	x	Y	N/A	0.39063 %	
1	TSBAT_ADC[1]	R	x	Y	N/A	0.19531 %	
0	TSBAT_ADC[0]	R	x	Y	N/A	0.09766 %	

9.6.1.39 TDIE_ADC1 Register (Address = 26h) [reset = xh]

TDIE_ADC1 is shown in 図 9-51 and described in 表 9-44.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-51. TDIE_ADC1 Register

7	6	5	4	3	2	1	0
TDIE_POL	TDIE_ADC[14:8]						
R-x	R-x						

図 9-51. TDIE_ADC1 Register (continued)

表 9-44. TDIE_ADC1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TDIE_POL	R	x	Y	N/A	N/A	Reported in Two's Complement. 0 = Result is positive 1 = Result is negative
6	TDIE_ADC[14]	R	x	Y	N/A		DIE Temperature = 5°C + TDIE_ADC[8:0] * 0.5°C
5	TDIE_ADC[13]	R	x	Y	N/A		
4	TDIE_ADC[12]	R	x	Y	N/A		
3	TDIE_ADC[11]	R	x	Y	N/A		
2	TDIE_ADC[10]	R	x	Y	N/A		
1	TDIE_ADC[9]	R	x	Y	N/A		
0	TDIE_ADC[8]	R	x	Y	N/A	128°C	

9.6.1.40 TDIE_ADC0 Register (Address = 27h) [reset = xh]

TDIE_ADC0 is shown in 図 9-52 and described in 表 9-45.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-52. TDIE_ADC0 Register

7	6	5	4	3	2	1	0
TDIE_ADC[7:0]							
R-x							

表 9-45. TDIE_ADC0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TDIE_ADC[7]	R	x	Y	N/A	64°C	
6	TDIE_ADC[6]	R	x	Y	N/A	32°C	
5	TDIE_ADC[5]	R	x	Y	N/A	16°C	
4	TDIE_ADC[4]	R	x	Y	N/A	8°C	
3	TDIE_ADC[3]	R	x	Y	N/A	4°C	
2	TDIE_ADC[2]	R	x	Y	N/A	2°C	
1	TDIE_ADC[1]	R	x	Y	N/A	1°C	
0	TDIE_ADC[0]	R	x	Y	N/A	0.5°C	

9.6.1.41 TSBUS_FLT1 Register (Address = 28h) [reset = 15h]

TSBUS_FLT1 is shown in 図 9-53 and described in 表 9-46.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-53. TSBUS_FLT1 Register

7	6	5	4	3	2	1	0

図 9-53. TSBUS_FLT1 Register (continued)

TSBUS_FLT[7:0]
R/W-75h

表 9-46. TSBUS_FLT1 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBUS_FLT[7]	R/W	0h	Y	N	25.00%	TSBUS Percentage Fault Threshold A TSBUS_TSBAT_ALM interrupt will be sent when TSBUS is within 5% of the value set in this register TSBUS_FLT = TSBUS_FLT[7:0] x 0.19531% Default: 4.1% (b00010101)
6	TSBUS_FLT[6]	R/W	0h	Y	N	12.5%	
5	TSBUS_FLT[5]	R/W	0h	Y	N	6.25%	
4	TSBUS_FLT[4]	R/W	1h	Y	N	3.125%	
3	TSBUS_FLT[3]	R/W	0h	Y	N	1.5625%	
2	TSBUS_FLT[2]	R/W	1h	Y	N	0.78125 %	
1	TSBUS_FLT[1]	R/W	0h	Y	N	0.39063 %	
0	TSBUS_FLT[0]	R/W	1h	Y	N	0.19531 %	

9.6.1.42 TSBAT_FLT0 Register (Address = 29h) [reset = 15h]

TSBAT_FLT0 is shown in 図 9-54 and described in 表 9-47.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-54. TSBAT_FLT0 Register

7	6	5	4	3	2	1	0
TSBAT_FLT[7:0]							
R/W-75h							

表 9-47. TSBAT_FLT0 Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TSBAT_FLT[7]	R/W	0	Y	N	25.00%	TSBAT Percentage Fault Threshold A TSBUS_TSBAT_ALM interrupt will be sent when TSBAT is within 5% of the value set in this register. TSBAT_FLT = TSBAT_FLT[7:0] x 0.19531% Default: 4.1% (b00010101)
6	TSBAT_FLT[6]	R/W	0	Y	N	12.5%	
5	TSBAT_FLT[5]	R/W	0	Y	N	6.25%	
4	TSBAT_FLT[4]	R/W	1	Y	N	3.125%	
3	TSBAT_FLT[3]	R/W	0	Y	N	1.5625%	
2	TSBAT_FLT[2]	R/W	1	Y	N	0.78125 %	
1	TSBAT_FLT[1]	R/W	0	Y	N	0.39063 %	
0	TSBAT_FLT[0]	R/W	1	Y	N	0.19531 %	

9.6.1.43 TDIE_ALM Register (Address = 2Ah) [reset = C8h]

TDIE_ALM is shown in 図 9-55 and described in 表 9-48.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-55. TDIE_ALM Register

7	6	5	4	3	2	1	0
TDIE_ALM[7:0]							
R/W-A8h							

表 9-48. TDIE_ALM Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	TDIE_ALM[7]	R/W	1h	Y	N	64°C	TDIE Voltage Fault Threshold If the value written to the register is greater than the max or less than the min defined value, the register will be set to the maximum or minimum as necessary. TDIE_ALM = 30 + TDIE_FLT[7:0] x 0.5°C Default: 125C (b11001000)
6	TDIE_ALM[6]	R/W	1h	Y	N	32°C	
5	TDIE_ALM[5]	R/W	0h	Y	N	16°C	
4	TDIE_ALM[4]	R/W	0h	Y	N	8°C	
3	TDIE_ALM[3]	R/W	1h	Y	N	4°C	
2	TDIE_ALM[2]	R/W	0h	Y	N	2°C	
1	TDIE_ALM[1]	R/W	0h	Y	N	1°C	
0	TDIE_ALM[0]	R/W	0h	Y	N	0.5°C	

9.6.1.44 CHG_CTRL Register (Address = 2Bh) [reset = 0h]

図 9-56. CHG_CTRL Register

7	6	5	4	3	2	1	0
SS_TIMEOUT_SET2	SS_TIMEOUT_SET1	SS_TIMEOUT_SET0	RESERVED	VOUT_OVP_DIS	IBUS_UCP_RISE_THRE	SET_IBAT_SNS_RES	VAC_PD_EN
R/W - 0h			R-x	R/W - 0h			

表 9-49. CHG_CTRL Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCHDOG	Bit Value	Description
7	SS_TIMEOUT_SET2	R/W	0h	N	N	N/A	Adjustable timeout for IBUS to rise to IBUS_UCP_RISE_THRESH 000: Timeout Disabled 001: 12.5 ms 010: 25 ms 011: 50 ms 100: 100 ms 101: 400 ms 110: 1.5 s 111: 100 s
6	SS_TIMEOUT_SET1	R/W	0h	N	N	N/A	
5	SS_TIMEOUT_SET0	R/W	0h	N	N	N/A	
4	RESERVED	R	x	N	N	N/A	RESERVED
3	VOUT_OVP_DIS	R/W	0h	N	N	N/A	This register disables the VOUT_OVP function.
2	IBUS_UCP_RISE_THRESH	R/W	0h	Y	N	N/A	This is the threshold above which the BUS current must rise to within the SS_TIMEOUT. The value can only be changed prior to enabling switching.0: 300 mA rising, 150 mA falling (typ)1: 500 mA rising, 250 mA falling (typ)
1	SET_IBAT_SNS_RES	R/W	0h	N	N	N/A	This bit selects the external BAT_SNS resistor value. 0: 2 mΩ 1: 5 mΩ
0	VAC_PD_EN	R/W	0h	Y	N	N/A	When this bit is enabled, it pulls down the VAC for t_{VAC_PD} to discharge any bulk input cap on VAC.

9.6.1.45 VOUT_OVP_STAT Register (Address = 2Ch) [reset = 0h]

図 9-57. VOUT_OVP_STAT Register

7	6	5	4	3	2	1	0
RESERVED							VOUT_OVP_STAT
R-x							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 9-50. VOUT_OVP_STAT Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCHDOG	Bit Value	Description
7-1	RESERVED	R	x	N	N	N/A	RESERVED
0	VOUT_OVP_STAT	R	x	N	N	N/A	Ths bit is set when VOUT_OVP is active. It is cleared when VOUT_OVP is no longer active.

9.6.1.46 VOUT_FLAG_MASK Register (Address = 2Dh) [reset = 0h]

図 9-58. VOUT_FLAG_MASK Register

7	6	5	4	3	2	1	0
RESERVED			VOUT_OVP_FLAG	RESERVED			VOUT_OVP_MASK
R-X							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

表 9-51. VOUT_FLAG_MASK Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCHDOG	Bit Value	Description
7-5	RESERVED	R	x	N	N	N/A	RESERVED
4	VOUT_OVP_FLAG	R	x	N	N	N/A	This bit is set when VOUT_OVP has been active. It is cleared by a read and VOUT_OVP is no longer active.
3-1	RESERVED	R	x	N	N	N/A	RESERVED
0	VOUT_OVP_MASK	R/W	0h	Y	N	N/A	This register masks the interrupt when the part enters exceeds the VOUT_OVP threshold000REG.

9.6.1.47 DEGLITCH Register (Address = 2Eh) [reset = 0h]

PULSE_MODE is shown in 図 9-59 and described in 表 9-52.

Return to Summary Table.

All bits are RESET BY REG_RST.

図 9-59. Deglitch Register

7	6	5	4	3	2	1	0
RESERVED			VBUS_ERROR_LO_DG_SET	IBUS_LOW_DG_SET	RESERVED		
R/W-0h			R/W-0h	R/W-0h	R/W-0h		

表 9-52. Deglitch Register Field Descriptions

Bit	Field	Type	Reset or Default	Reset by REG_RST	Reset by WATCH DOG	Bit Value	Description
7	RESERVED		0h				
6			0h				
5			0h				
4	VBUS_ERROR_LO_DG_SET	R/W	0h	Y	N	N/A	This bit sets the deglitch time for VBUS_ERROR_LO0: 10 µs, 1: 10 ms
3	IBUS_LOW_DG_SET	R/W	0h	Y	N	N/A	Ths bit sets the deglitch time for IBUS_LOW_DG_SET0: 10 µs, 1: 5 ms
2	RESERVED		0h				
1			0h				
0			0h				

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

A typical application consists of the device configured as an I^2C controlled parallel charger along with a standard switching charger, however, it can also be used with a linear charger or PMIC with integrated charger as well. For simplicity, it is called the primary charger. As shown in 図 9-2 the device can start fast charging after the primary charger completes precharging, where the BQ25890 is used as the primary charger. The device will then hand back charging to the primary charger when final current tapering is desired. This point is usually where the efficiency of the primary charger is acceptable for the application. The device can be used to charge Li-ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. To take advantage of the high charge current capabilities of the BQ25968, it may be necessary to charge in excess of 1C. In this case, be sure to follow the battery manufacturers recommendations closely.

10.2 Typical Application

The BQ25968 system implementation on the charging device can be very small. A typical schematic is shown below with all the optional and required components shown.

10.2.1 Standalone Application Information (for use with switching charger)

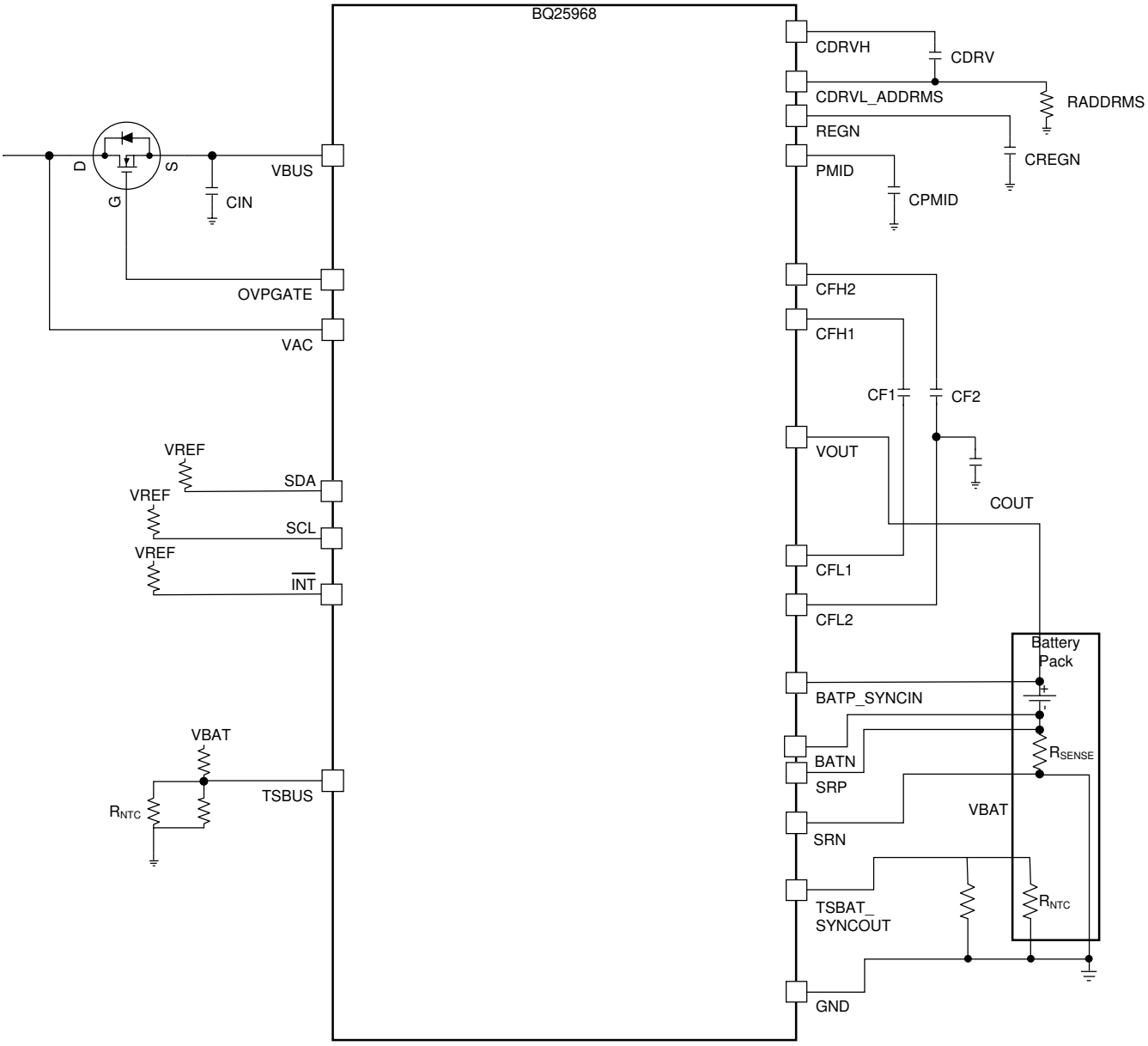


図 10-1. Typical Schematic for BQ25968

10.2.1.1 Design Requirements

The design requires a smart wall adapter to provide the proper input voltage and input current to the BQ25968, following the USB_PD Programmable Power Supply (PPS) voltage steps and current steps. The design shown is capable of charging up to 6 A, although this may not be practical for some applications due to the total power loss at this operating point. Careful consideration of the thermal constraints, space constraints, and operating conditions should be done to ensure acceptable performance.

10.2.1.2 Detailed Design Procedure

The first step is the determine if an external OVP FET is required in the application. Choosing to include the external OVP FET allows protection of the device if an over-voltage event occurs. If not using the external OVP FET capable part (BQ25970 or BQ25968), it is recommended to have some other TVS mechanism to protect the device.

The next step is to determine the number of CFLY caps to put on each phase of the design. It is important to consider the current rating of the caps, their ESR, and the capacitance rating. Be sure to consider the bias voltage derating for the caps, as the CFLY caps are biased to half of the input voltage, and this will affect their effective capacitance. An optimal system will have four 22-µF caps per phase, for a total of 8 caps per device. The recommended parts for this configuration are shown below, and result in the lowest cost, acceptable efficiency, and acceptable voltage and current ripple. It is possible to use fewer caps, with a minimum recommendation of 3. Using fewer caps will result in higher voltage and current ripple on the output, as well as lower efficiency. Using more than 4 caps per phase will not significantly improve the output voltage or current ripple, or efficiency.

The default switching frequency, f_{SW}, for the power stage is 500 kHz. The switching frequency can be adjusted in register 0x0Bh using the FSW_SET bits. Using a lower switching frequency will increase the efficiency, but also increase the voltage and current ripple. If using 3 22-µF caps per phase, it is recommended to use the default f_{SW} of 500 kHz. If using 4 22-µF caps per phase, either 500 kHz or 300 kHz is recommended.

表 10-1. BQ25968 Capacitors

CAPACITANCE (µF)	SIZE, VOLTAGE RATING, TEMP CHAR	CAPACITOR TYPE	SUPPLIER(1)	COMMENT
20	0704, 16 V, X5R	GRMJN7R61C206ME05	Murata	Lowest ESR (high efficiency) when using four caps
22	0603, 10 V, X5R	GRM188R61A226ME15	Murata	Lowest Cost and Smallest Size (Recommended) when using four caps

(1) See Third-party Products Disclaimer

10.2.1.3 Application Curves

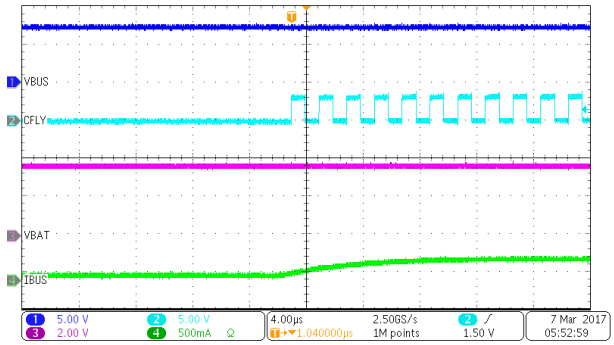


図 10-2. Power Up

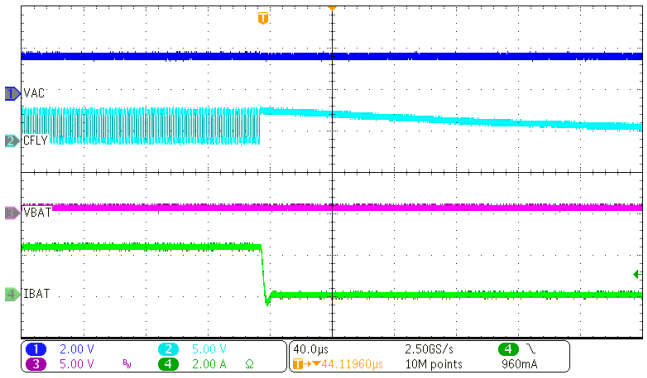


図 10-3. Disable Charge

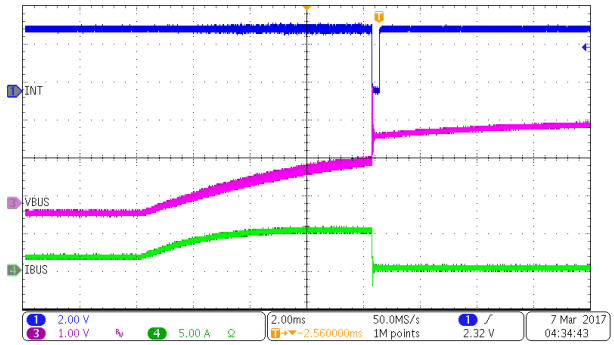


図 10-4. VBUS_OVP

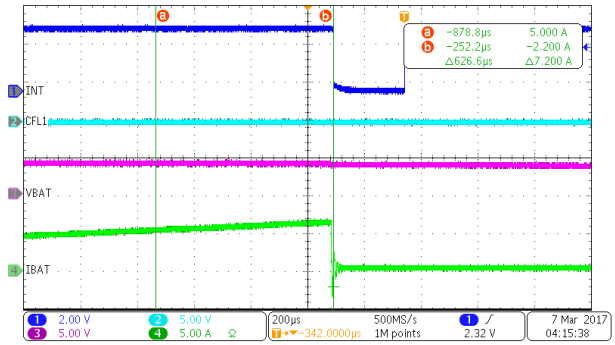


図 10-5. IBAT_OCP

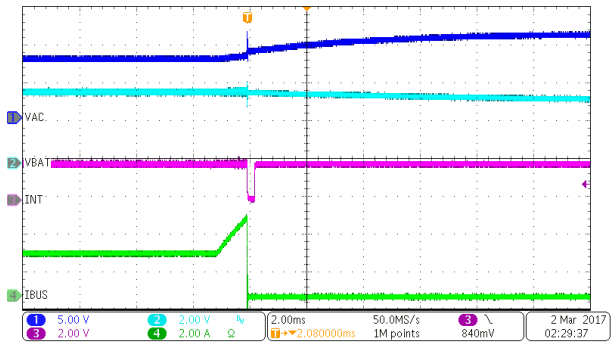


図 10-6. IBUS_OCP

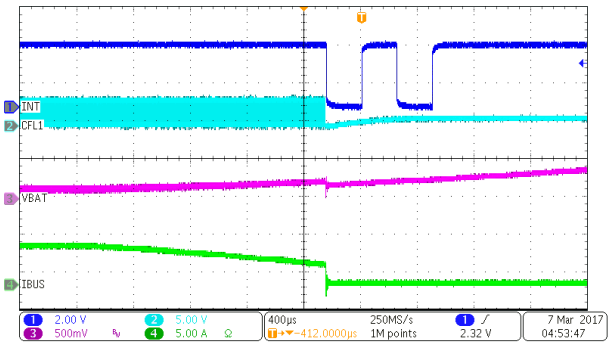


図 10-7. VBAT_OVP

10.2.2 Parallel BQ25968 for Higher Power Applications

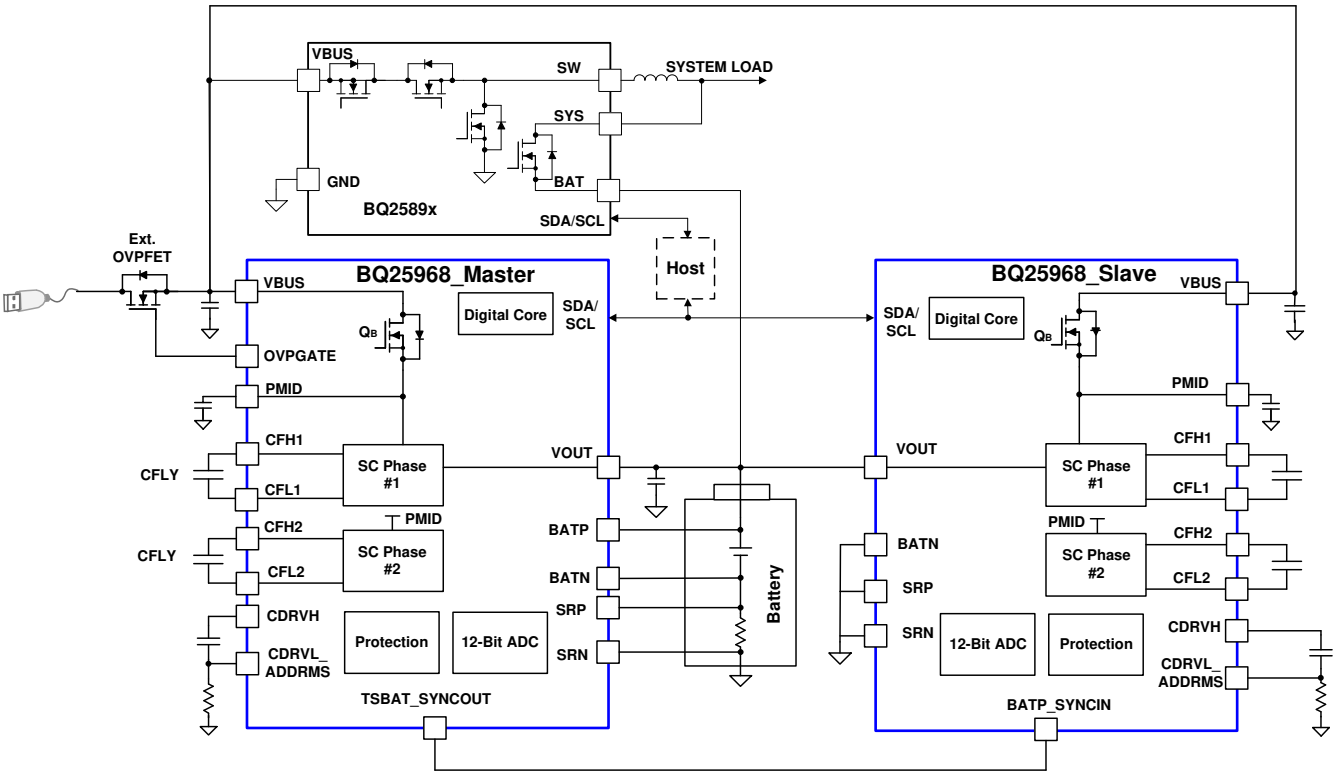


図 10-8. Parallel BQ25968 System

10.2.2.1 Design Requirements

For design requirements refer to セクション 10.2.1.1.

10.2.2.2 Detailed Design Procedure

If the total loss is greater than desired for a single BQ25968 at the fast charge current, two devices can be used in parallel to reduce losses. The same design procedure is applied for the master and slave devices, with a few additional steps for parallel operation.

The master device is used for BAT current sensing, so the slave device should short SRN and SRP to GND.

The master device supplies the SYNCOUT signal to the slave, so connect pin A5 of the master to pin A7 of the slave device.

The master device controls the OVP FET (if used), so the slave device should connect VAC to VBUS.

10.2.2.3 Application Curve

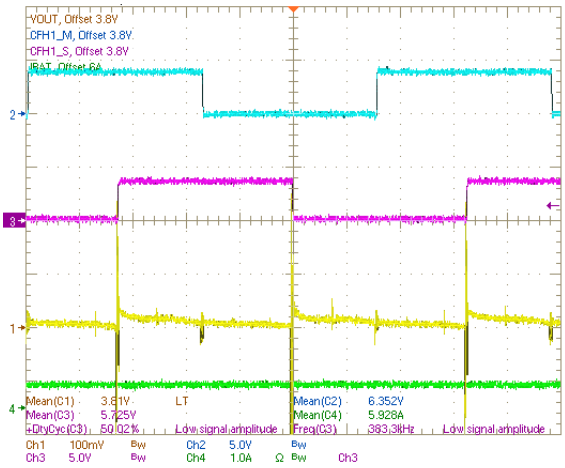


図 10-9. Parallel Switching Waveform

11 Power Supply Recommendations

The BQ25968 can be powered by a standard power supply capable of meeting the input voltage and current requirements for evaluation. In the actual application, it must be used with a wall adapter that supports USB Power Delivery (PD) Programmable Power Supply (PPS) specifications.

12 Layout

12.1 Layout Guidelines

Layout is very important to maximize the electrical and thermal performance of the total system. General guidelines are provided, but the form factor, board stack-up, and proximity of other components also need to be considered to maximize the performance. The parasitics in the board layout impacts the switching current in the MOSFETs and the output current of the device.

- VBUS traces should be as short and wide as possible to accommodate for high current.
- Minimize losses through connectors wherever possible, as the losses in these connectors will contribute a significant amount to the total power loss.
- Use vias under the exposed thermal pad for thermal relief.
- Place low ESR bypass capacitors to ground for VBUS, PMID, and VOUT. The capacitor should be placed as close to the device pins as possible.
- The CFLY pads should be as small as possible, and the CFLY caps placed as close as possible to the device, as these are switching pins and this will help reduce EMI.
- Connect all quiet signals to the AGND pins.
- Connect all power signals to the PGND pins.
- Do not route so the power planes are interrupted by signal traces.

12.2 Layout Example

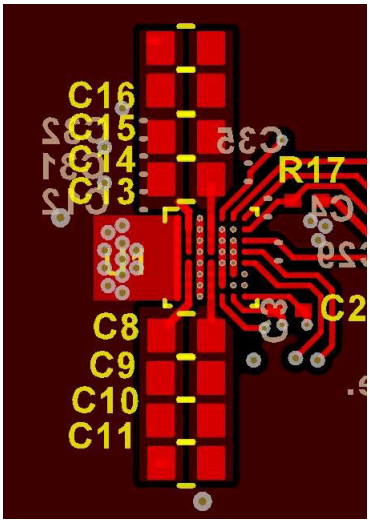


図 12-1. BQ25968 Layout Example - Top Layer

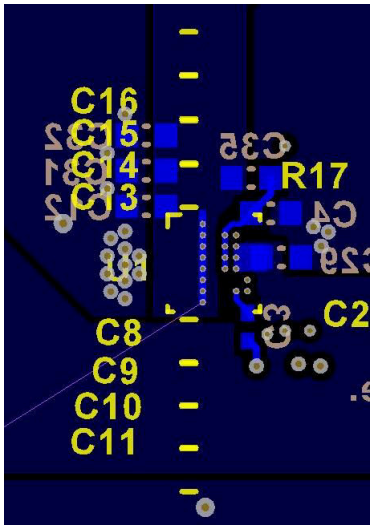


図 12-2. BQ25968 Layout Example - Bottom Layer

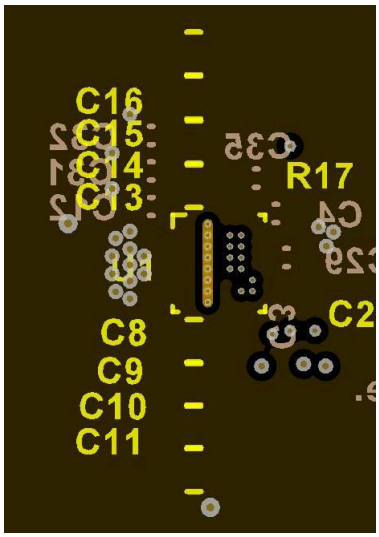


図 12-3. BQ25968 Layout Example - Signal Layer 1

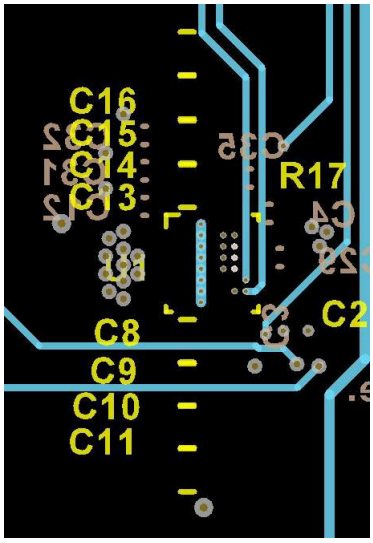


図 12-4. BQ25968 Layout Example - Signal Layer 2

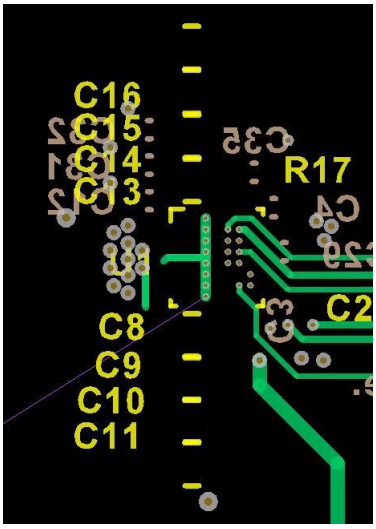


図 12-5. BQ25968Layout Example - Signal Layer 3

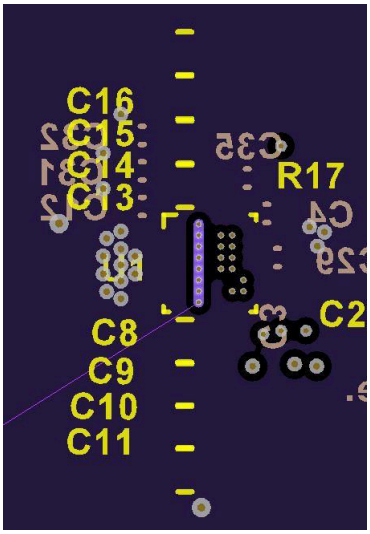


図 12-6. BQ25968 Layout Example - Signal Layer 4

13 Device and Documentation Support

13.1 Device Support

13.1.1 サード・パーティ製品に関する免責事項

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13.1.2 Device Nomenclature

IADAPT (A)	Output current of adapter
VADAPT (V)	Output voltage of adapter
VCONADROP (V)	Voltage drop across the adapter connector
VCONA (V)	Output voltage after adapter connector (same as the voltage at the beginning of the cable)
VCABLEDROP (V)	Voltage drop
VCABLED (V)	Voltage at the cable, going into the device
VCOND (V)	Output voltage after the device connector
VDEVCON (V)	Output voltage after the device control FETs (controlled by the PD controller)
IIN (A)	Input current to the BQ25968
VIN (V)	Input voltage to the BQ25968
VOUT (V)	Output voltage of the BQ25968
VCONBDROP (V)	Voltage drop across the battery connector and sense resistor
VBAT (V)	Voltage at the battery
IBAT (A)	Current at the battery

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *BQ2597xEVM-xxx User's Guide*

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 サポート・リソース

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13.5 Trademarks

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13.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

13.7 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25968YFFR	Active	Production	DSBGA (YFF) | 56	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25968
BQ25968YFFR.A	Active	Production	DSBGA (YFF) | 56	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25968

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

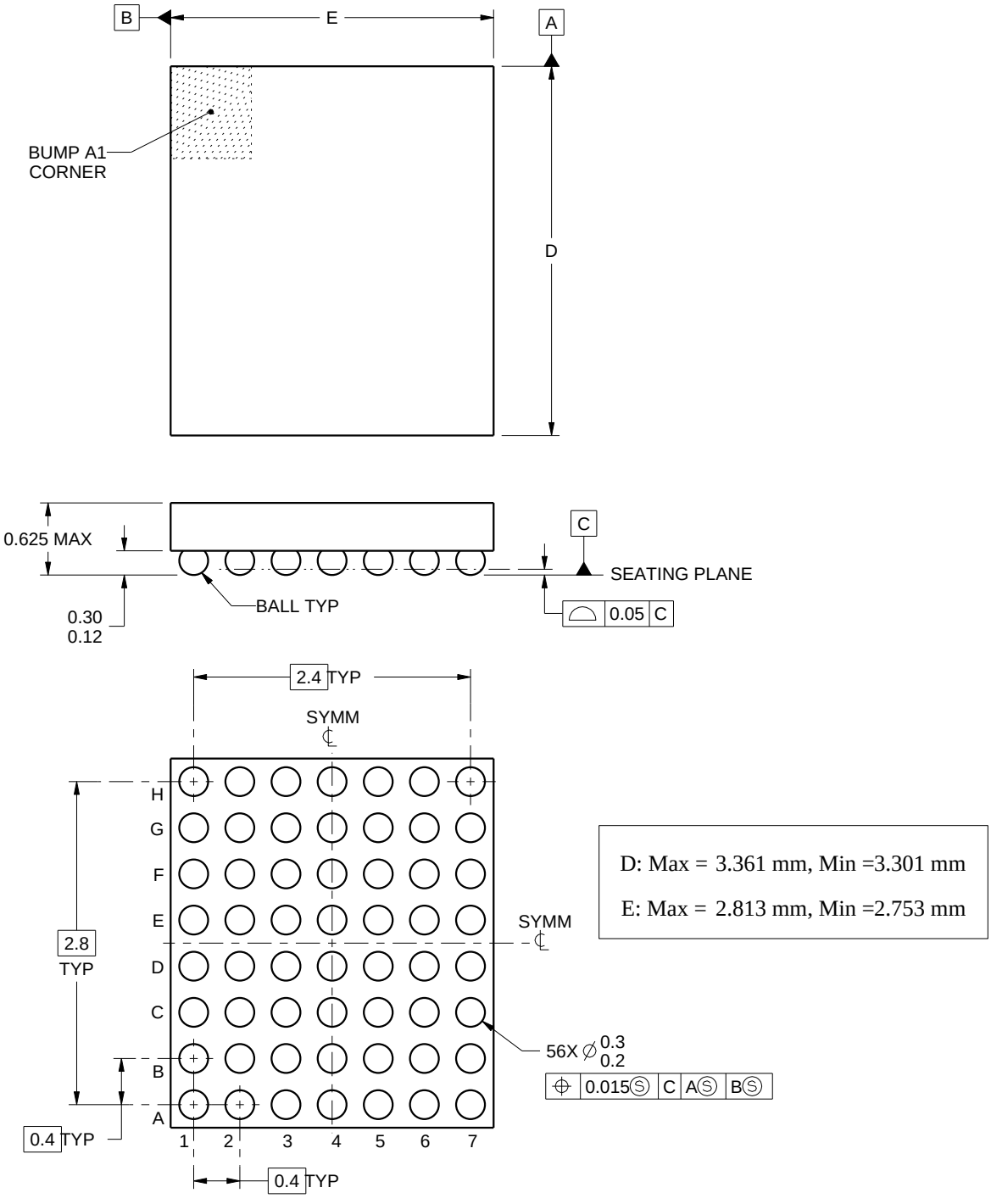
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

YFF0056

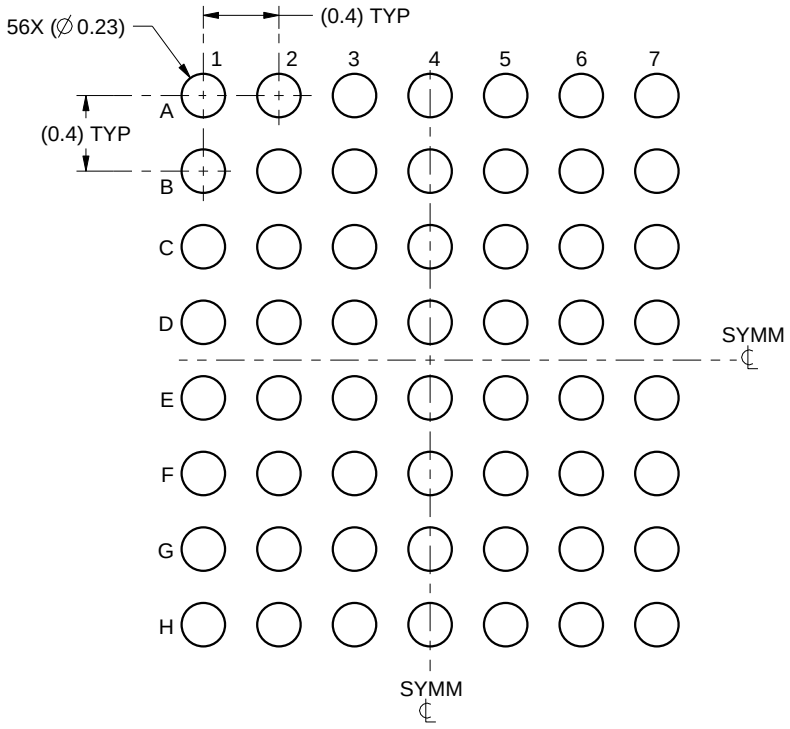
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

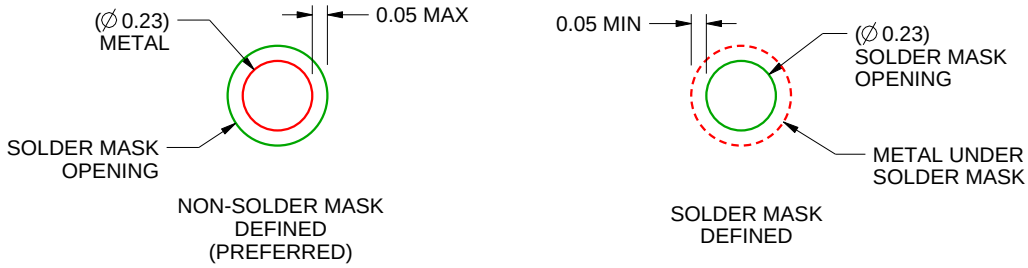


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4219481/A 10/2014

NOTES: (continued)

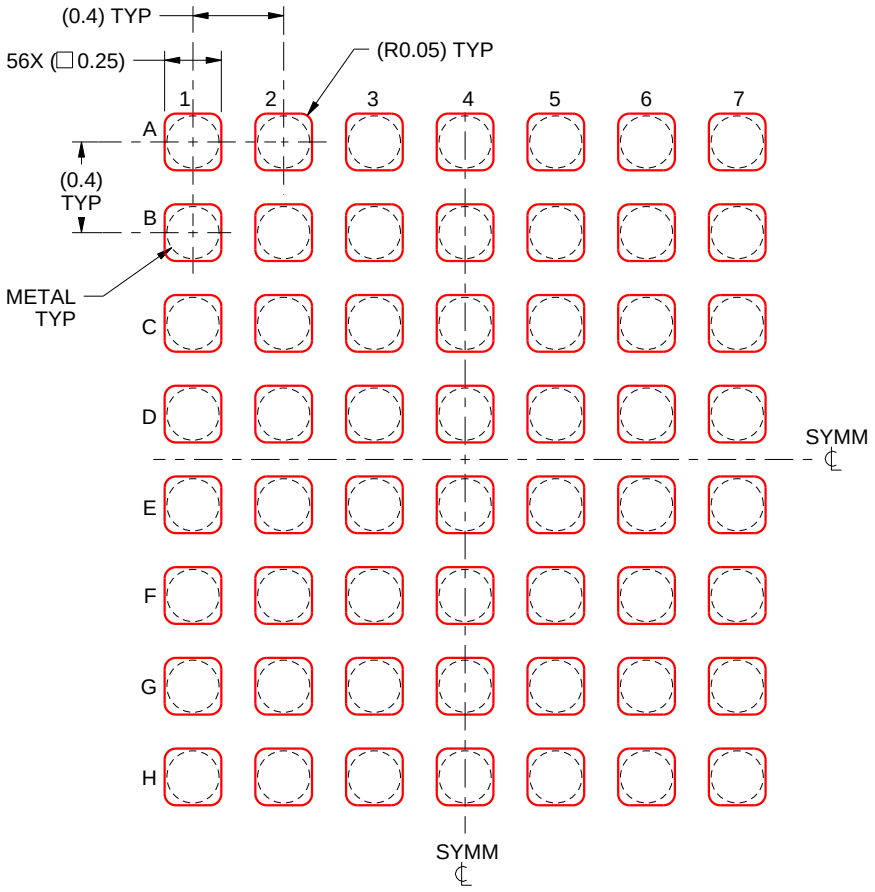
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YFF0056

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219481/A 10/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最終更新日：2025 年 10 月