



VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Li-Ion BATTERIES (2nd-LEVEL PROTECTION)

Check for Samples: [bq29410](#), [bq29411](#), [bq29412](#), [bq29413](#), [bq29414](#), [bq29415](#), [bq29419](#)

FEATURES

- 2-, 3-, or 4-Cell Secondary Protection
- Low Power Consumption $I_{CC} < 2 \mu A$
[$V_{CELL(ALL)} < V_{(PROTECT)}$]
- Fixed High Accuracy Overvoltage Protection Threshold
 - bq29410 = 4.35 V
 - bq29411 = 4.40 V
 - bq29412 = 4.45 V
 - bq29413 = 4.50 V
 - bq29414 = 4.55 V
 - bq29415 = 4.60 V
 - bq29419 = 4.30 V
- Programmable Delay Time of Detection
- High Power Supply Ripple Rejection
- Stable During Pulse Charge Operation

APPLICATIONS

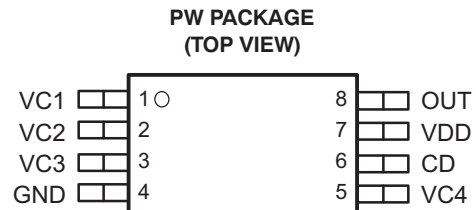
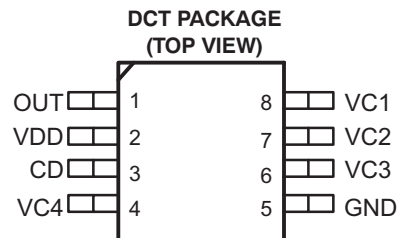
- 2nd-Level Overvoltage Protection in Li-Ion Battery Packs in:
 - Notebook Computers
 - Portable Instrumentation
 - Portable Equipment

DESCRIPTION

The bq2941x is a secondary overvoltage protection IC for 2-, 3-, or 4-cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit. It includes a programmable delay circuit for overvoltage detection time.

FUNCTION

Each cell in a multiple-cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq2941x device starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	V _(PROTECT) ⁽²⁾	PACKAGE ⁽³⁾			
		MSOP (DCT)	SYMBOL	SSOP (PW)	
–40°C to 110°C	4.30 V	bq29419DCTR	CJQ	bq29419PWG4	bq29419PWRG4
		bq29419DCTT			
	4.35 V	bq29410DCT3R	CJG	bq29410PW bq29410PWG4	bq29410PWR bq29410PWRG4
		bq29410DCTR			
		bq29410DCTT			
	4.40 V	bq29411DCT3R	CJH	bq29411PW bq29411PWG4	bq29411PWR bq29411PWRG4
		bq29411DCTR			
		bq29411DCTT			
	4.45 V	bq29412DCT3R	CJJ	bq29412PW bq29412PWG4	bq29412PWR bq29412PWRG4
		bq29412DCTR			
		bq29412DCTT			
	4.50 V	bq29413DCTR	CJk	bq29413PW	bq29413PWR
		bq29413DCTT			
	4.55 V	bq29414DCTR	CJL	bq29414PW	bq29414PWR
		bq29414DCTT			
	4.60 V	bq29415DCTR	CJM	bq29415PW	bq29415PWR
		bq29415DCTT			

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Contact your local Texas Instruments representative or sales office for alternative overvoltage threshold options.
 (3) The "R" suffix indicates tape-and-reel packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted^{(1) (2)}

		UNIT
Supply voltage range	VDD	–0.3 V to 28 V
Input voltage range	VC1, VC2, VC3, VC4	–0.3 V to 28 V
	VC1 TO VC2, VC2 TO VC3, VC3 TO VC4, VC4 TO GND	–0.3 V to 8 V
Output voltage range	OUT	–0.3 V to 28 V
	CD	–0.3 V to 28 V
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T _{stg}		–65°C to 150°C
Lead temperature (soldering, 10 s)		300°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 (2) All voltages are with respect to ground of this device except the differential voltage of VC1-VC2, VC2-VC3, VC3-VC4, and VC4-GND.

PACKAGE DISSIPATION RATINGS

PACKAGE	T _A = 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DCT	412 mW	3.3 mW/°C	264 mW	214 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT	
V_{DD}	Supply voltage	4		25	V	
V_I	Input voltage range	VC1, VC2, VC3, VC4			0	25
		VCn – VC (n=1, (n=1, 2, 3), VC4 – GND			0	5
$t_{d(CD)}$	Delay time capacitance		0.22		μ F	
R_{IN}	Voltage-monitor filter resistance	100	1k		Ω	
C_{IN}	Voltage-monitor filter capacitance	0.01	0.1		μ F	
R_{VD}	Supply-voltage filter resistance	0		1	k Ω	
C_{VD}	Supply-voltage filter capacitance		0.1		μ F	
T_A	Operating ambient temperature range	–40		110	$^{\circ}$ C	

ELECTRICAL CHARACTERISTICS

 over recommended operating free-air temperature range, $T_A = 25^{\circ}$ C (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT		
$V_{(OA)}$	Overvoltage detection accuracy	$T_A = 25^{\circ}$ C			25	35	
		$T_A = -20^{\circ}$ C to 85° C			25	50	
		$T_A = -40^{\circ}$ C to 110° C				80	
$V_{(PROTECT)}$	Overvoltage detection voltage	bq29410			4.35		
		bq29411			4.40		
		bq29412			4.45		
		bq29413			4.50		
		bq29414			4.55		
		bq29415			4.60		
		bq29419			4.30		
V_{hys}	Overvoltage detection hysteresis	bq29410/11/12/13/14/15			320		
		bq29419			250	320	450
I_{IN}	Input current	V2, V3, VC4 input, $V_{DD} = VC1$ VC1 = VC2 = VC3 = VC4 = 3.5 V (see Figure 1)				0.3	
t_{D1}	Overvoltage detection delay time	$V_{DD} = VC1$, CD = 0.22 μ F			1	1.5	2
$I_{(CD_dis)}$	CD GND clamp current	$V_{DD} = VC1$, CD = 1 V			5	12	
I_{CC}	Supply current	$V_{DD} = VC1$, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V (see Figure 1)			2	3	
		$V_{DD} = VC1$, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 2.3 V (see Figure 1)			1.5	2.5	
$V_{(OUT)}$	OUT pin drive voltage	VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = $V_{(PROTECT)Max}$, $V_{DD} = 14$ V, $I_{OH} = 0$ mA				7	
		VC1 = VC2 = VC3 = VC4 = $V_{(PROTECT)Max}$, $V_{DD} = 4.3$ V, $T_A = 0^{\circ}$ C to 70° C, $I_{OH} = 40$ μ A			1.5	2	2.5
I_{OH}	High-level output current	OUT = 3 V, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = $V_{(PROTECT)Max}$, $V_{DD} = 14$ V					–1
I_{OL}	Low-level output current	OUT = 0.1 V, $V_{DD} = VC1$, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V			5		

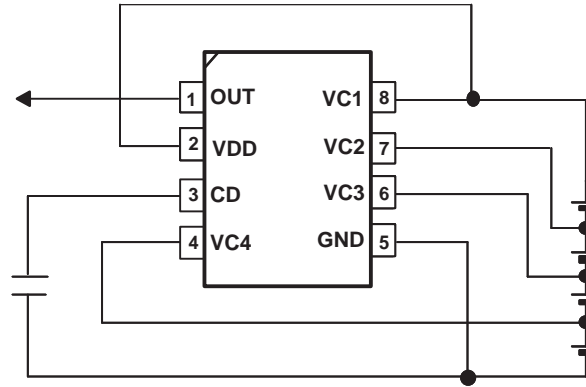
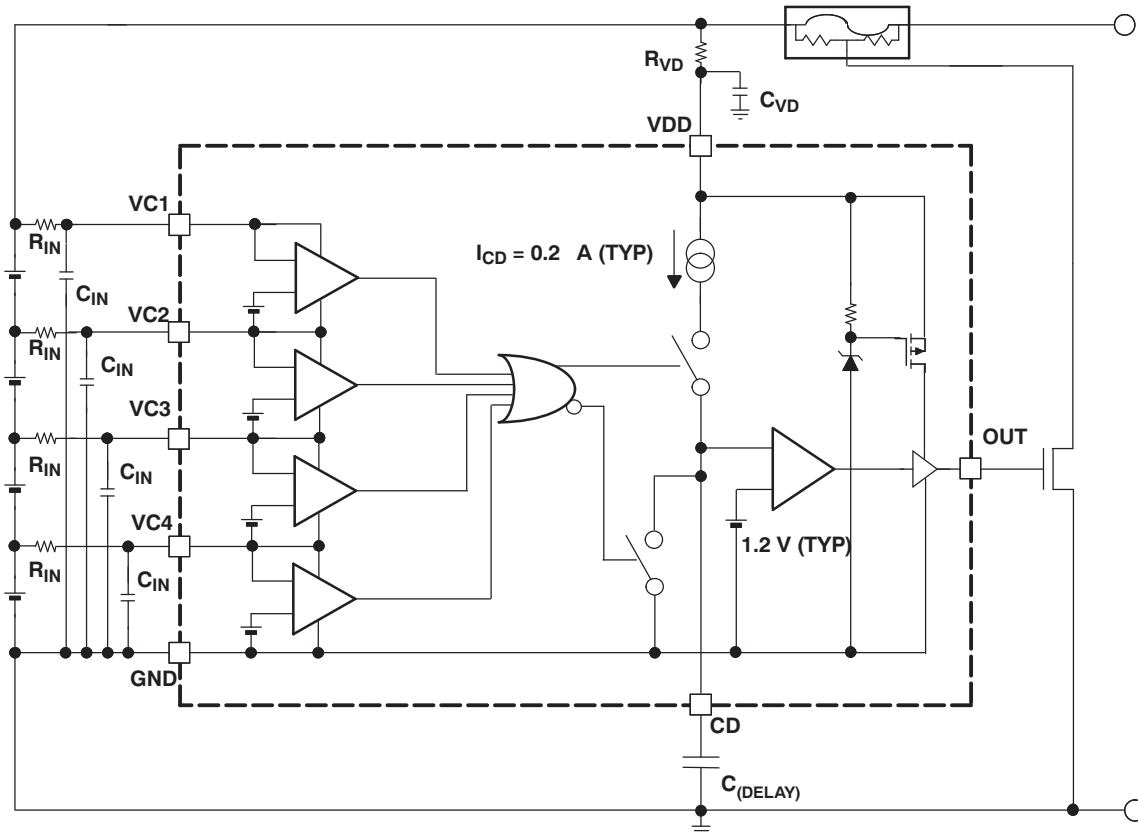


Figure 1. I_{CC} , I_{IN} Measurement (DCT Package)

Terminal Functions

TERMINAL			DESCRIPTION
MSOP (DCT)	TSSOP (PW)	NAME	
8	1	VC1	Sense voltage input for most positive cell
7	2	VC2	Sense voltage input for second most positive cell
6	3	VC3	Sense voltage input for third most positive cell
5	4	GND	Ground pin
4	5	VC4	Sense voltage input for least positive cell
3	6	CD	An external capacitor is connected to determine the programmable delay time
2	7	VDD	Power supply
1	8	OUT	Output

FUNCTIONAL BLOCK DIAGRAM



OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds $V_{(PROTECT)}$, an internal current source begins to charge the capacitor, $C_{(DELAY)}$, connected to the CD pin. If the voltage at the CD pin, V_{CD} , reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activated and blows the external fuse in the positive battery rail; see the functional block diagram.

If all cell voltages fall below $V_{(PROTECT)}$ before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor, $C_{(DELAY)}$, and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach $V_{(PROTECT)} - V_{hys}$.

DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{1.2 \text{ V} \times C_{(DELAY)}}{I_{CD}}$$

$$C_{(DELAY)} = \frac{t_d \times I_{CD}}{1.2 \text{ V}}$$

Where $I_{(CD)}$ = CD current source = 0.18 μ A

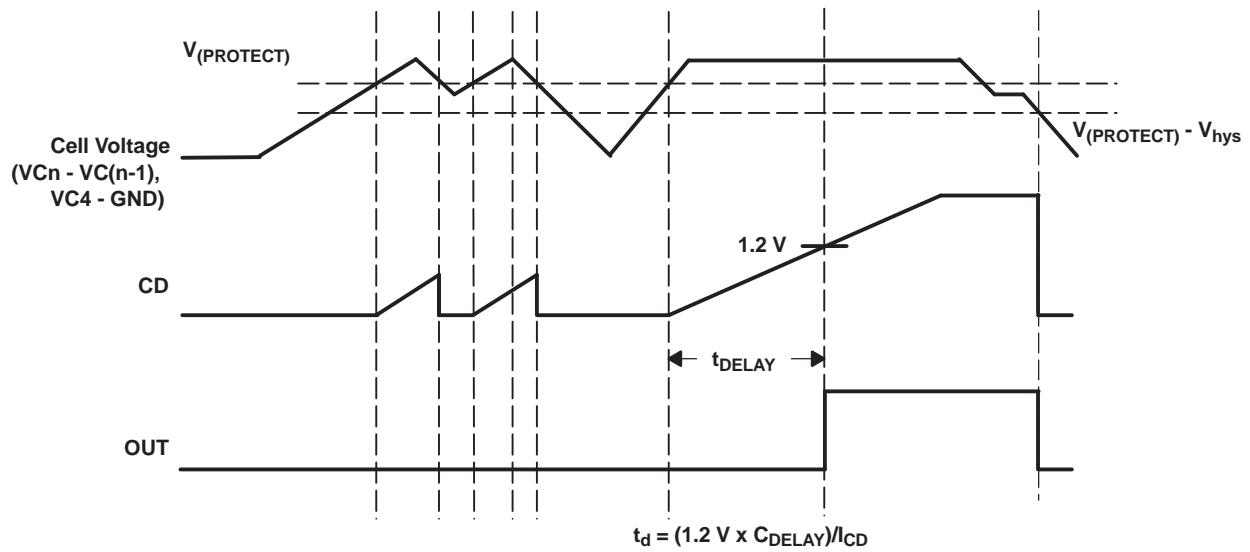


Figure 2. Timing for Overvoltage Sensing

APPLICATION INFORMATION

BATTERY CONNECTIONS

The following diagrams show the DCT package device in different cell configurations.

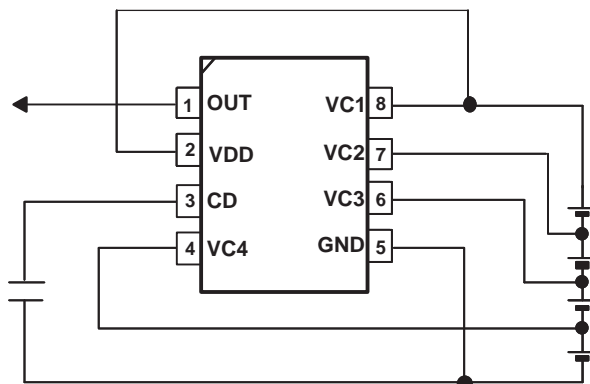


Figure 3. 4-Series Cell Configuration

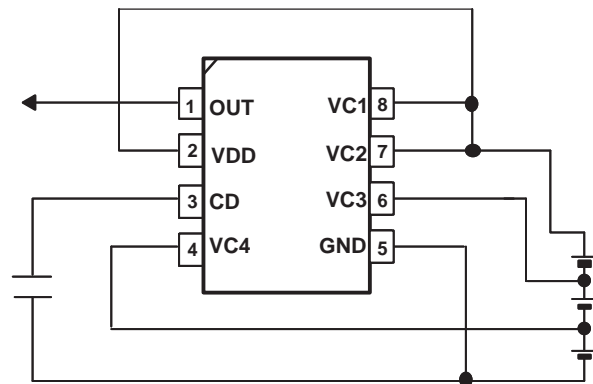


Figure 4. 3-Series Cell Configuration
 (Connect together VC1 and VC2)

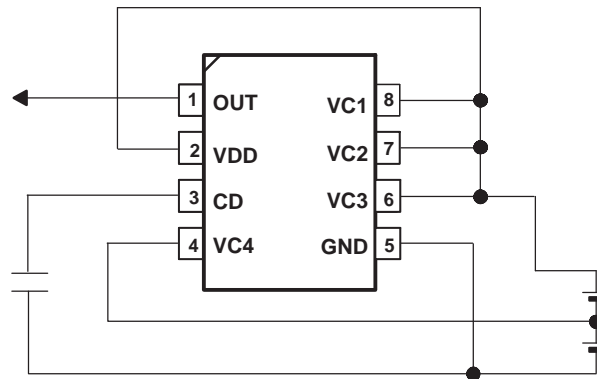


Figure 5. 2-Series Cell Configuration

CELL CONNECTIONS

To prevent incorrect output activation, the following connection sequences must be used.

4-Series Cell Configuration

- VC1(=VDD) → VC2 → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC2 → VC1(=VDD)

3-Series Cell Configuration

- VC1(=VC2=VDD) → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC1(=VC2=VDD)

2-Series Cell Configuration

- VC1(=VC2=VC3=VDD) → VC4 → GND or
- GND → VC4 → VC1(=VC2=VC3=VDD)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ29410DCT3R	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 110	CJG W
BQ29410DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W
BQ29410DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJG W
BQ29410PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	29410
BQ29410PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	29410
BQ29410PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29410
BQ29411DCT3R	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 110	CJH W
BQ29411DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJH W
BQ29411DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJH W
BQ29411PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	29411
BQ29411PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29411
BQ29412DCT3R	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 110	CJJ W
BQ29412DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W
BQ29412DCTT	Active	Production	SSOP (DCT) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJJ W
BQ29412PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	29412
BQ29412PWRG4	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	29412
BQ29413DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 110	CJK W
BQ29413PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29413
BQ29415PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	2915
BQ29419PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29419
BQ29419PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	29419

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29410DCT3R	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29410PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29410PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29411DCT3R	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29411PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29412DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29412DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29412PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29412PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29413DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
BQ29413PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
BQ29415PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29419PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

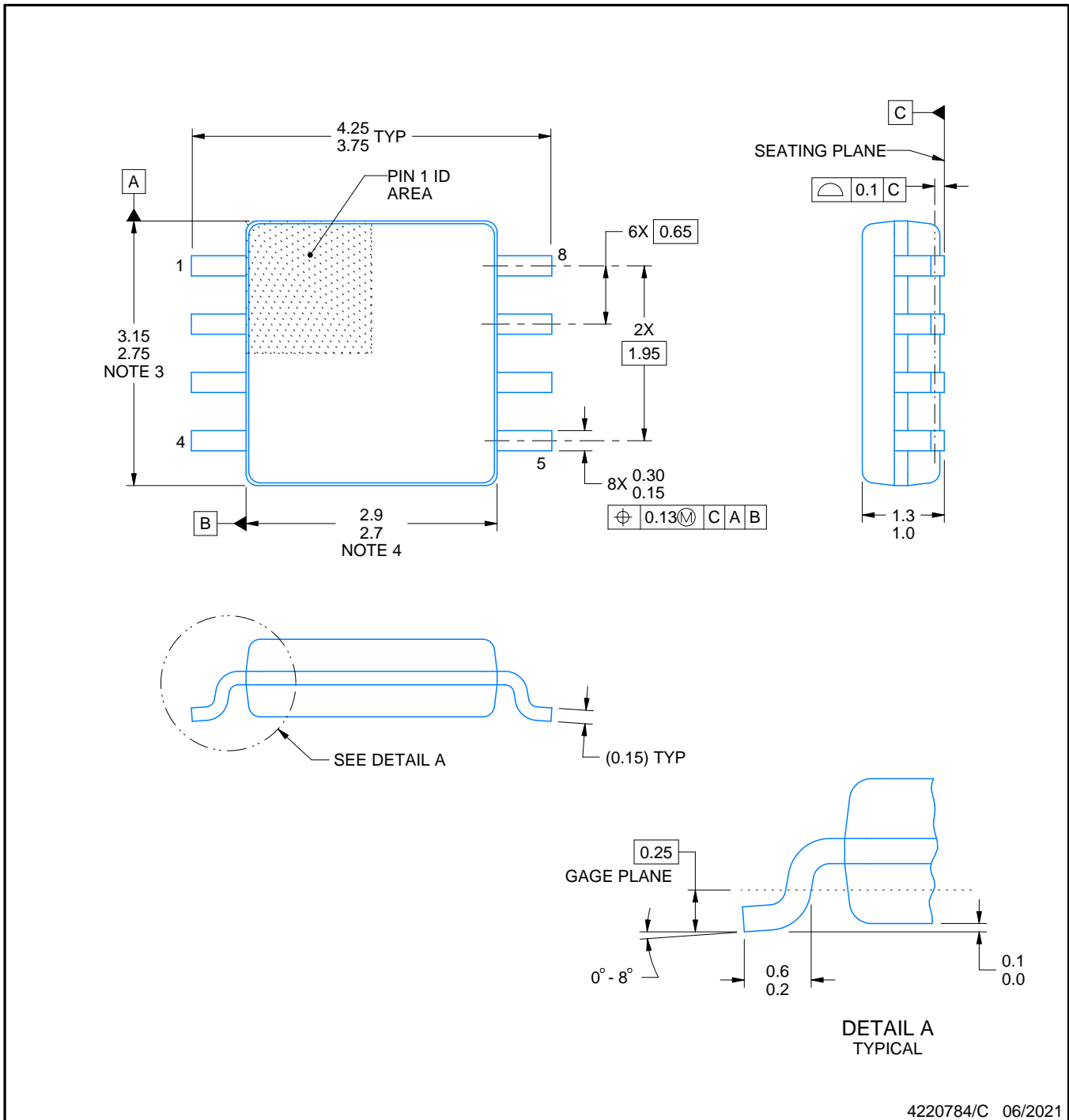
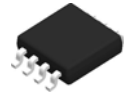

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29410DCT3R	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29410DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29410DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
BQ29410PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29410PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29411DCT3R	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29411DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29411DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
BQ29411PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29412DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29412DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
BQ29412PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29412PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29413DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
BQ29413PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29415PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
BQ29419PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ29410PW	PW	TSSOP	8	150	530	10.2	3600	3.5
BQ29411PW	PW	TSSOP	8	150	530	10.2	3600	3.5
BQ29419PW	PW	TSSOP	8	150	508	8.5	3250	2.8



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NOTES:

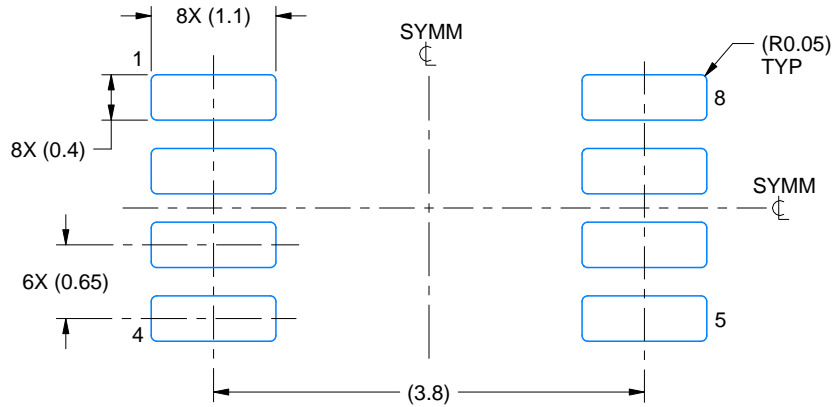
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

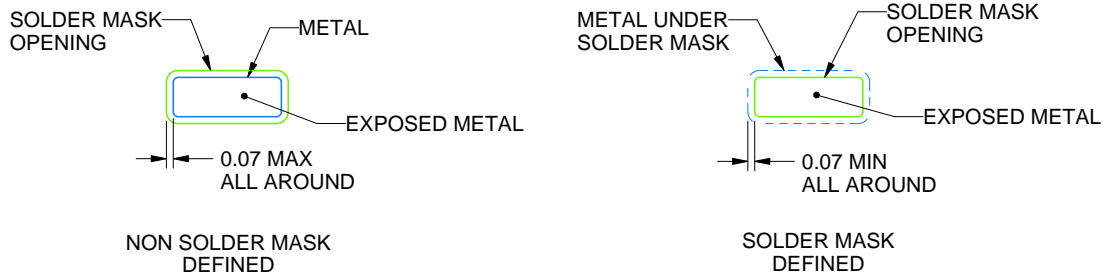
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

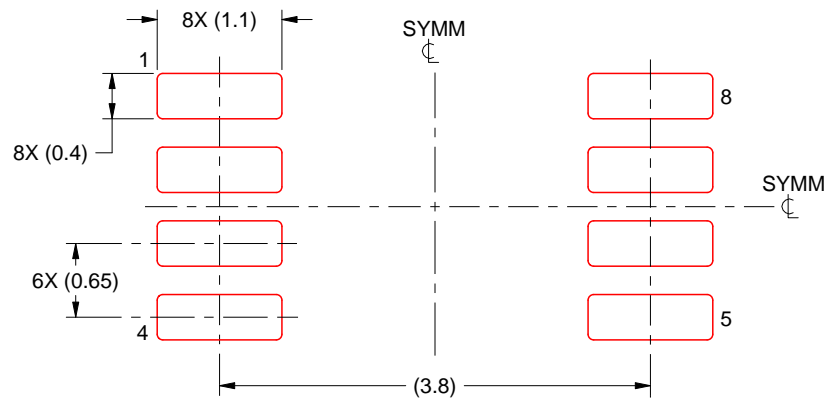
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

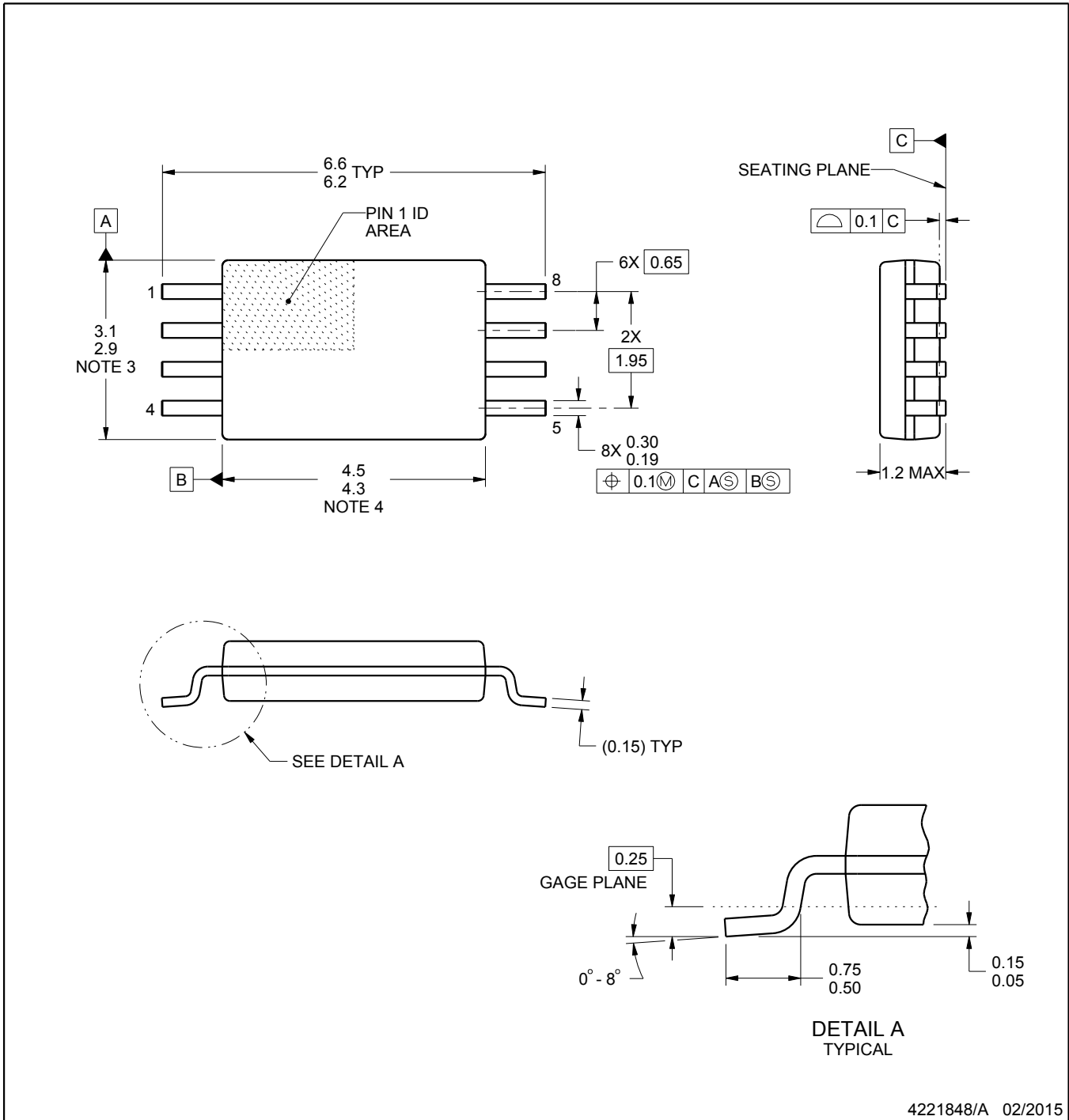
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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