BQ7716xy 2～4 直列セルのリチウムイオン・バッテリ用過電圧保護、外部遅延コンデンサ対応

1 特長

- 2、3、4 直列セルの過電圧保護
- 外付けのコンデンサで遅延タイマをプログラム
- 固定 OVP スレッショルド
- 高精度の過電圧保護:
  ±10mV
- 低消費電力 I_{CC} ≈ 1μA
  ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- セル入力あたりのリーク電流が低い:100nA 未満
- 小さいパッケージ占有面積
  - 8 ピン WSON (3.00mm × 4.00mm)

2 アプリケーション

- 電動工具
- UPS バッテリ・バックアップ
- 軽量の電気自動車
  - 電動自転車
  - 電動スクーター
  - ペダル・アシスト自転車

3 概要

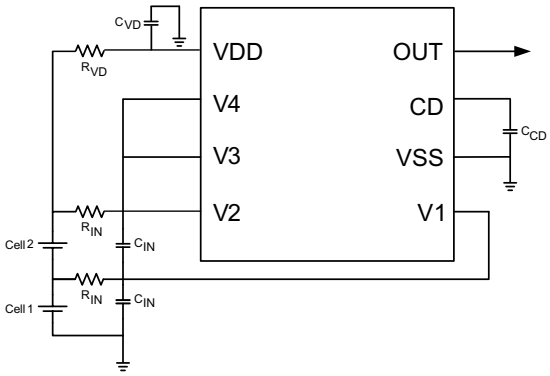
BQ7716xy デバイス・ファミリは、リチウムイオン・バッテリ・パック・システム用の過電圧モニタおよびプロテクタです。各セルの過電圧状況を個別に監視できます。生産ライン・テストを迅速に行えるよう、BQ7716xy デバイスは遅延時間を大幅に削減したカスタマ・テスト・モードを備えています。

BQ7716xy デバイスでは、いずれかのセルで過電圧状態が検出されると、外部遅延タイマが起動します。遅延タイマが満了すると、出力はアクティブ状態 (構成により HIGH または LOW) にトリガされます。外部遅延タイマ機能には、CD ピン上の遅延コンデンサの開放または短絡を検出する機能も含まれており、この場合も同様に、過電圧状況の出力ドライバがトリガされます。

表 3-1. 「製品情報」表 (1)

部品番号	パッケージ	本体サイズ (公称)
BQ771600	WSON (8)	3.00mm × 4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報およびデバイス比較表を参照してください。



簡略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (July 2015) to Revision E (April 2021) — **Page**

- Removed Product Preview devices ... 3
- Removed Product Preview devices ... 5

Changes from Revision C (August 2014) to Revision D (July 2015) — **Page**

- QFN を WSON に変更 ... 1
- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 ... 1
- Changed the BQ771605 to Production Data ... 3
- Added table note 2, which was hidden inadvertently ... 4
- Moved *Pin Details* to *Feature Description* section ... 8
- Moved from *Application Information* section to *Design Requirements* section ... 13

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5 Device Comparison Table

PART NUMBER	OVP (V)	OV HYSTERESIS (V)	OUTPUT DRIVE	TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
BQ771600	4.3	0.3	CMOS Active High	BQ771600DPJR	BQ771600DPJT
BQ771601	4.225	0.05	CMOS Active High	BQ771601DPJR	BQ771601DPJT
BQ771602	4.225	0.05	NCH Active Low, Open Drain	BQ771602DPJR	BQ771602DPJT
BQ771604	4.2	0.05	CMOS Active High	BQ771604DPJR	BQ771604DPJT
BQ771605	3.85	0.25	NCH Active Low	BQ771605DPJR	BQ771605DPJT
BQ771611	4.35	0.3	CMOS Active High	BQ771611DPJR	BQ771611DPJT
BQ771612	3.9	0.3	CMOS Active High	BQ771612DPJR	BQ771612DPJT
BQ7716xy future options(1)	3.85–4.65	0–0.3	CMOS Active High or NCH Active Low, Open Drain	BQ7716xyTBD	BQ7716xyTBD

(1) Contact TI.

6 Pin Configuration and Functions

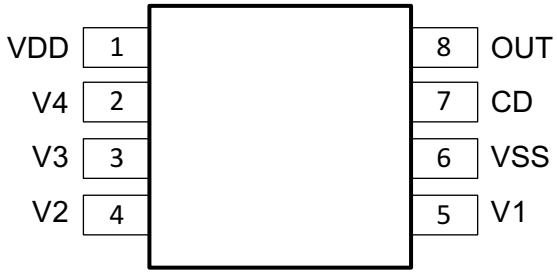

図 6-1. DPJ Package 8-Pin WSON Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.	I/O(1)	
CD	7	I/O	External capacitor connection for delay timer
OUT	8	OA	Output drive for overvoltage fault signal
VDD	1	P	Power supply
VSS	6	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
V1	5	I	Sense input for positive voltage of the lowest cell in the stack
V2	4	I	Sense input for positive voltage of the second cell from the bottom of the stack
V3	3	I	Sense input for positive voltage of the third cell from the bottom of the stack
V4	2	I	Sense input for positive voltage of the fourth cell from the bottom of the stack

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range(2)	VDD–VSS	–0.3	30	V
Input voltage range(2)	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3	30	V
Output voltage range(2)	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.		
Functional temperature		–40	110	°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300		°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings for input voltage range, output voltage range, and supply voltage are assured by design and not tested in production.

7.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Rating	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} (1)	Supply voltage	3		20	V
V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	Input voltage range	0		5	V
T_A	Operating ambient temperature range	–40		110	°C

(1) See *セクション 9.2*.

7.4 Thermal Information

THERMAL METRIC(1)		BQ7716xy DPJ (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	11.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 14.4V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	BQ771600		4.300		V
		BQ771601		4.225		V
		BQ771602		4.225		V
		BQ771604		4.200		V
		BQ771605		3.850		V
		BQ771611		4.350		V
		BQ771612		3.900		V
V_{HYS}	OV Detection Hysteresis	BQ771600	250	300	400	mV
		BQ771601	25	50	75	mV
		BQ771602	25	50	75	mV
		BQ771604	25	50	75	mV
		BQ771605	200	250	300	mV
		BQ771611	250	300	400	mV
		BQ771612	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		44	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	Supply Current	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See 図 8-3.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See 図 8-3.)	–0.1		0.1	µA

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Typical values stated where T_A = 25°C and VDD = 14.4V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVE OUT, CMOS ACTIVE HIGH VERSIONS ONLY						
V_{OUT1}	Output Drive Voltage, Active High	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, I_{OH} = 100 µA	6			V
		If three of four cells are short circuited, only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA		VDD – 0.3		V
		(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH1}	OUT Source Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1}	OUT Sink Current (No OV)	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD. Measured into OUT pin	0.5		14	mA
OUTPUT DRIVE OUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY						
V_{OUT2}	Output Drive Voltage, Active Low	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH2}	OUT Sink Current (During OV)	(V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 14.4 V. OUT = VDD. Measured into OUT pin	0.5		14	mA
I_{OUTLK}	OUT Pin Leakage	(V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD. Measured out of OUT pin			100	nA
DELAY TIMER						
t_{CD}	OV Delay Time	C_{CD} = 0.1 µF	1	1.5	2	s
V_{CD}	CD Fault Detection External Comparator Threshold, Initial Charge Value	The CD pin will first be quickly charged to this value before being discharged back to VSS.		1.5		V
$t_{CHGDELAY}$	CD Charging Delay	OVP to OUT delay with CD shorted to ground	20		170	ms
I_{CHG}	OV Detection Charging Current	CD pin fast charging current from VSS to V_{CD} to begin delay countdown		300		µA
I_{DSG}	OV Detection Discharging Current	CD pin discharging current from V_{DELAY} to VSS		100		nA

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7.6 Typical Characteristics

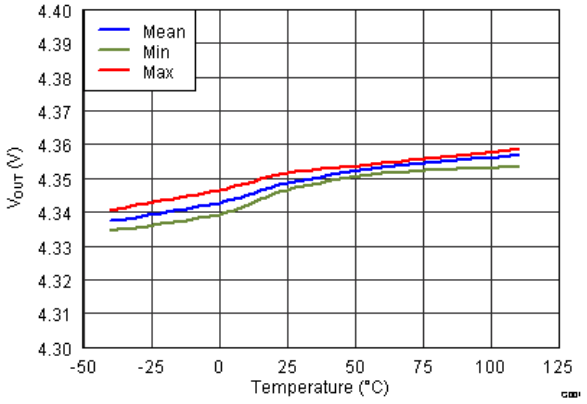

図 7-1. Overvoltage Threshold (OVT) vs. Temperature

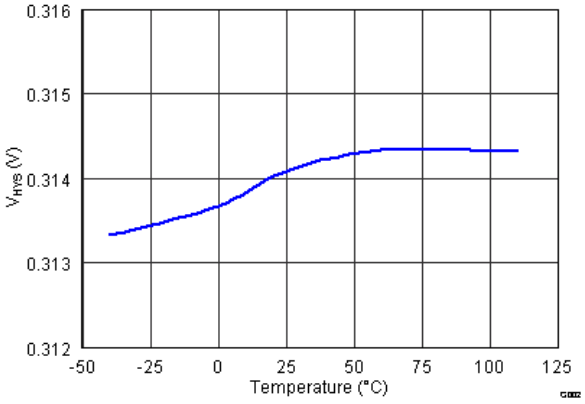

図 7-2. Hysteresis V_{HYS} vs. Temperature

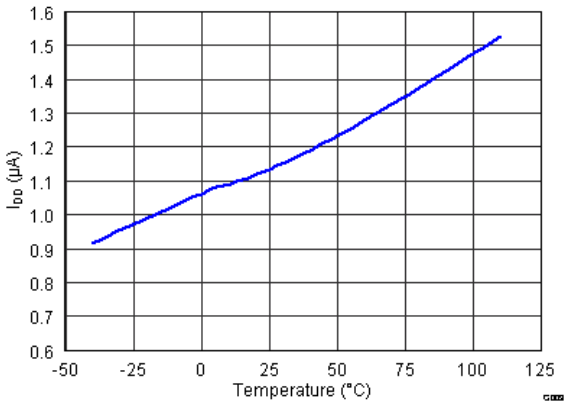

図 7-3. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

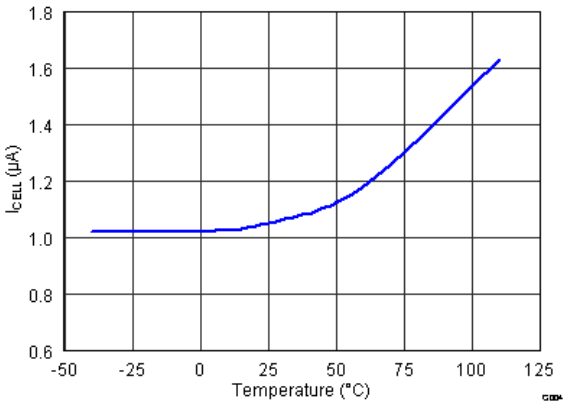

図 7-4. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

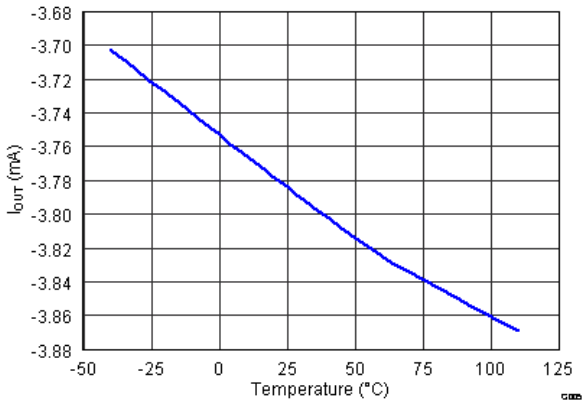

図 7-5. Output Current I_{OUT} vs. Temperature

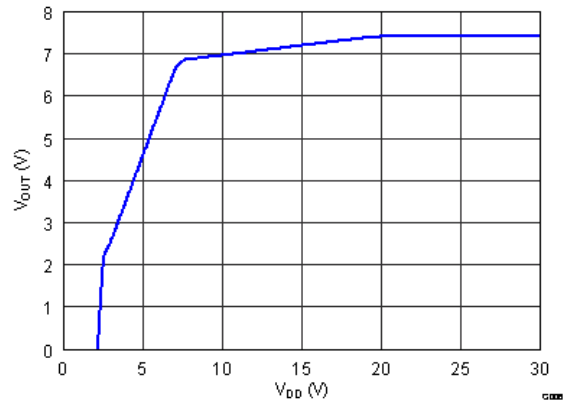

図 7-6. V_{OUT} vs. V_{DD}

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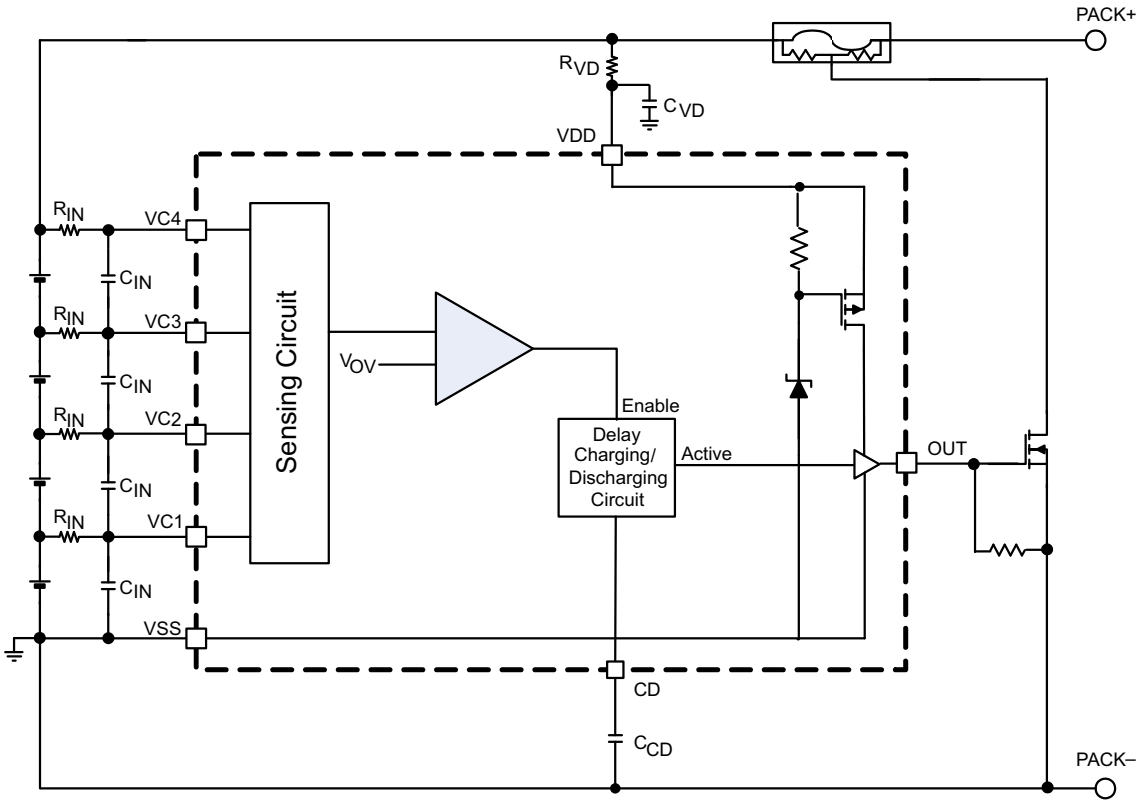
8 Detailed Description

8.1 Overview

In the BQ7716xy family of devices for overvoltage protection, each cell is monitored independently and an external delay timer is initiated if an overvoltage condition is detected when any cell voltage is higher than the protection voltage threshold, VOV. After the delay time expires, the OUT pin is inserted.

For quicker production-line testing, the device provides a Customer Test Mode with greatly reduced delay time.

8.2 Functional Block Diagram



8.3 Feature Description

In the BQ7716xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See 図 8-1 for reference.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present), and is high impedance when inactive (no OV).

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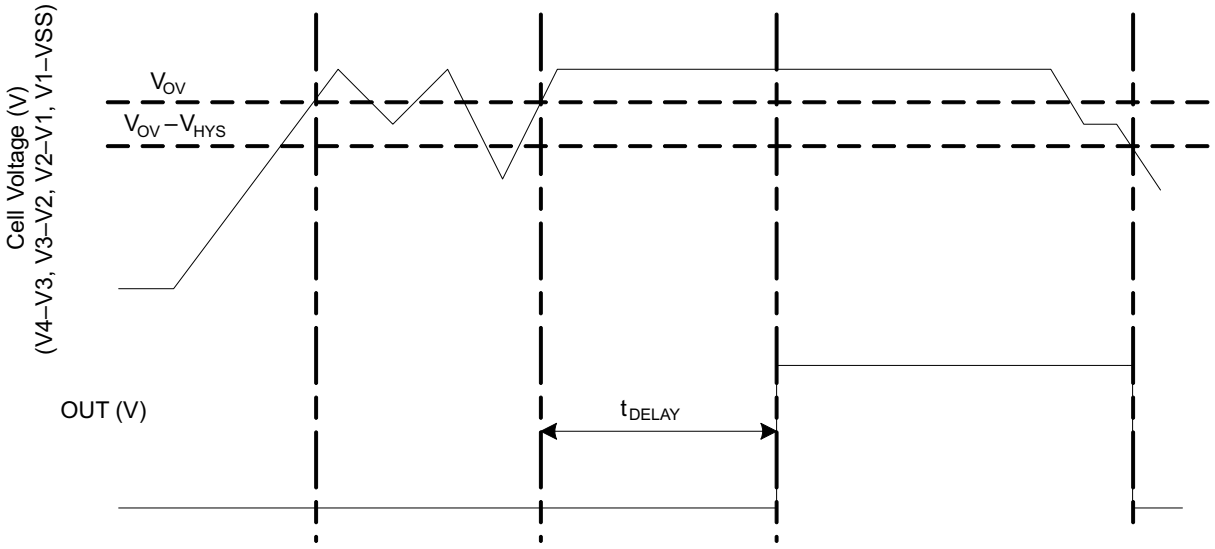

図 8-1. Timing for Overvoltage Sensing

図 8-2 shows an overview of the behavior of the CD pin during an OV sequence.

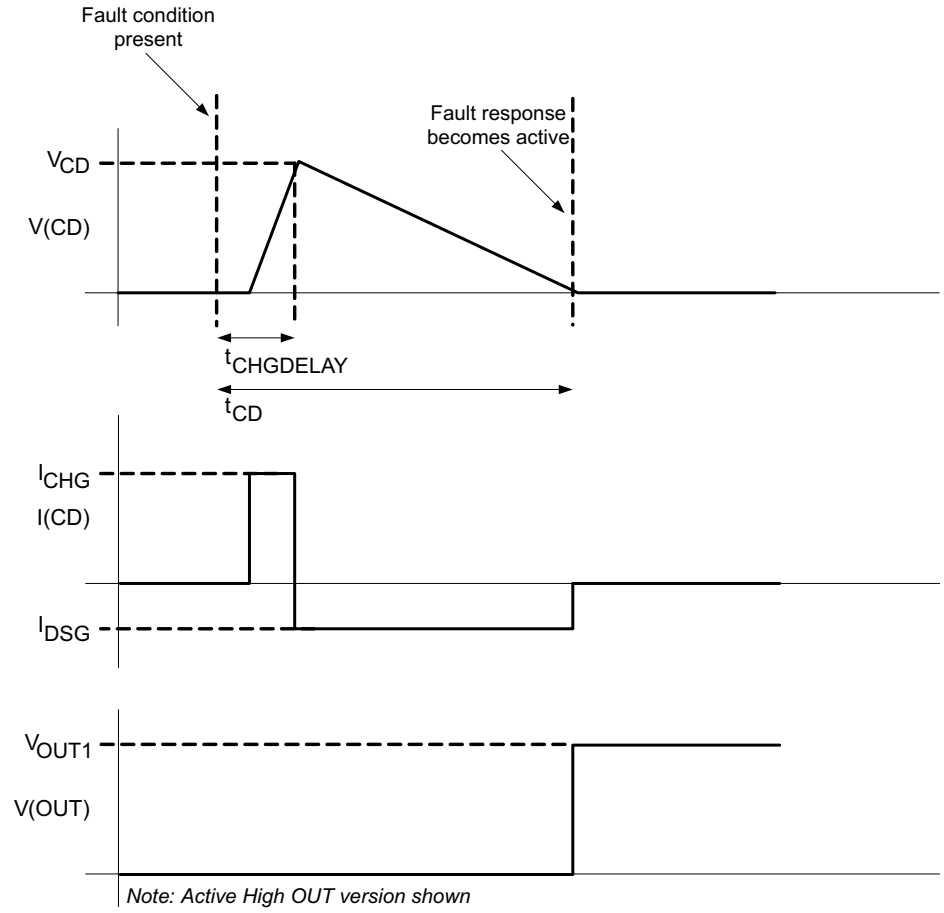

図 8-2. CD Pin Mechanism

8.3.1 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 External Delay Capacitor, CD

This terminal is connected to an external capacitor that is used for setting the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

To calculate the delay, use the following equation:

$$t_{CD}\ (s) = K \times C_{CD}\ (\mu F), \text{ where } K = 10 \text{ to } 20 \text{ range.} \quad (1)$$

Example: If C_{CD}= 0.1 µF (typical), then the delay timer range is

t_{CD} (s) = 10 × 0.1 = 1 s (Minimum)

t_{CD} (s) = 20 × 0.1 = 2 s (Maximum)

注

The tolerance on the capacitor used for C_{CD} increases the range of the t_{CD} timer.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive and if configured:

- Active high is low
- Active low is being externally pulled up and is an open drain

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, VOV for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When all of the cell voltages fall below the (VOV–VHYS), the device returns to NORMAL mode

8.4.3 Customer Test Mode

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CHGDELAY)}$ value, which has a maximum of 170 ms.

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注意

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

図 8-3 shows the timing for the Customer Test Mode.

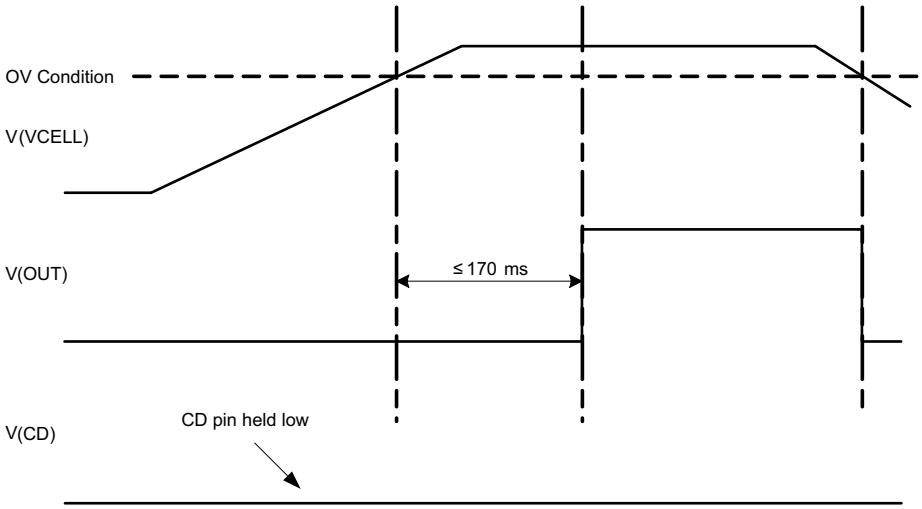

図 8-3. Timing for Customer Test Mode

図 8-4 shows the measurement for current consumption for the product for both VDD and Vx.

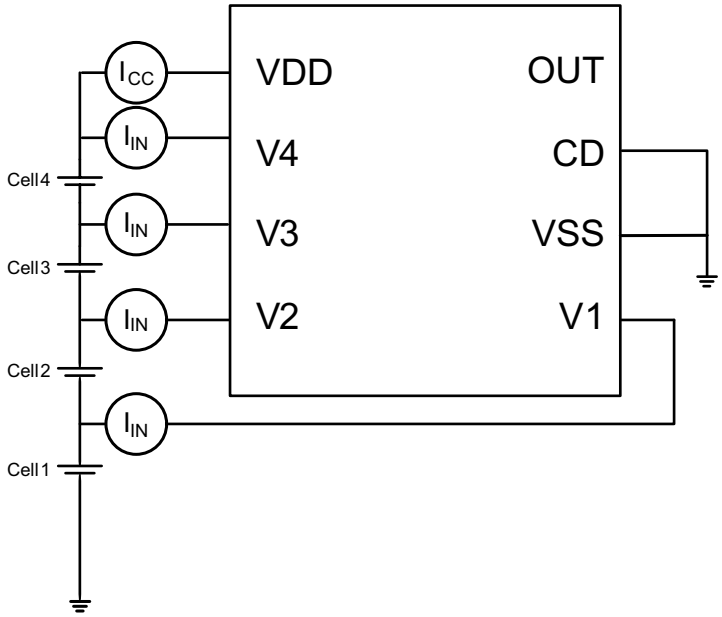

図 8-4. Configuration for IC Current Consumption Test

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9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

図 9-1 shows each external component.

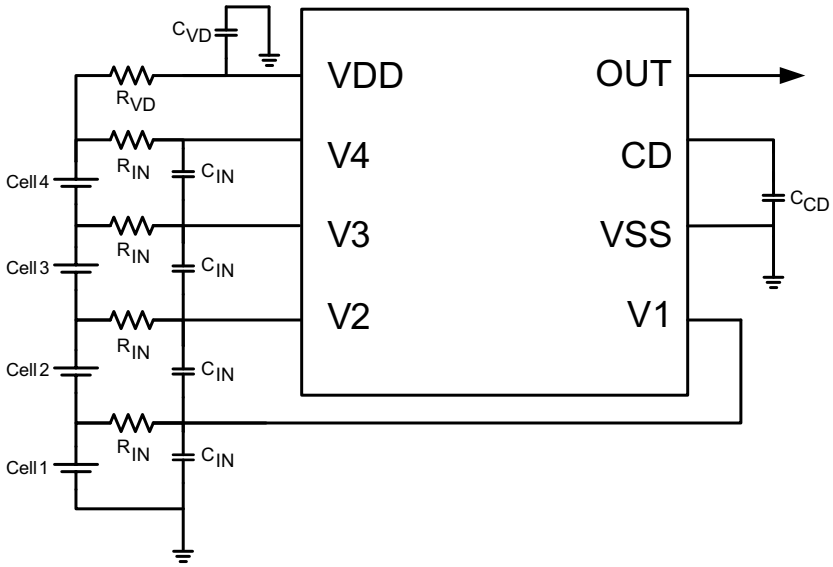

図 9-1. Application Configuration

注

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements.

注

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

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9.2 Typical Application

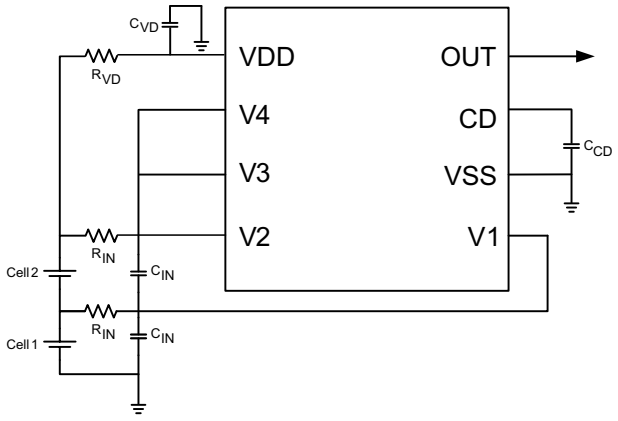

図 9-2. 2-Series Cell Configuration with Capacitor-Programmed Delay

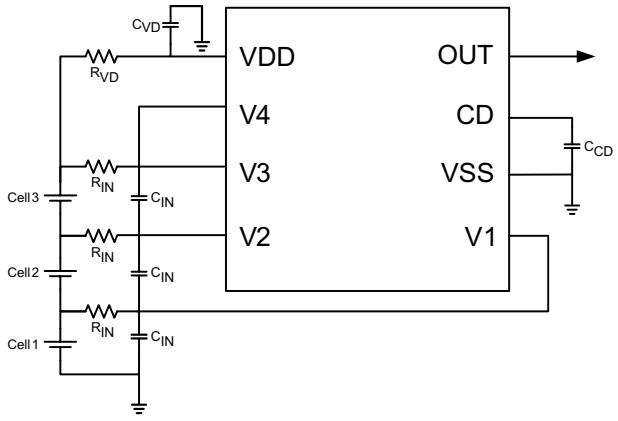

図 9-3. 3-Series Cell Configuration with Capacitor-Programmed Delay

注

In these application examples of 2 s and 3 s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

9.2.1 Design Requirements

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements.

表 9-1. Design Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	µF
Supply voltage filter resistance	R_{VD}	100		1K	Ω
Supply voltage filter capacitance	C_{VD}		0.1		µF
CD external delay capacitance	C_{CD}		0.1	1	µF
OUT Open drain version pull-up resistance to PACK+	R_{OUT}		100k		Ω

9.2.2 Detailed Design Procedure

1. Determine the number of cells in series. The device supports a 2-S to 4-S cell configuration. For 2S and 3S, the top unused pin(s) should be shorted as shown in 図 9-2 and 図 9-3.
2. Determine the overvoltage protection delay. Follow the calculation example described in *セクション 8.3.4*. Select the correct capacitor to connect to the CD pin.
3. Follow the application schematic to connect the device. If the OUT pin is configured to open drain, an external pull-up resistor should be used. Refer to the Out Sink Current specification, IOUTH2 to ensure a proper pull-up resistor value is used, so that the OUT pin sink current is able to pull down the pin during OV condition.

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9.2.3 Application Curves

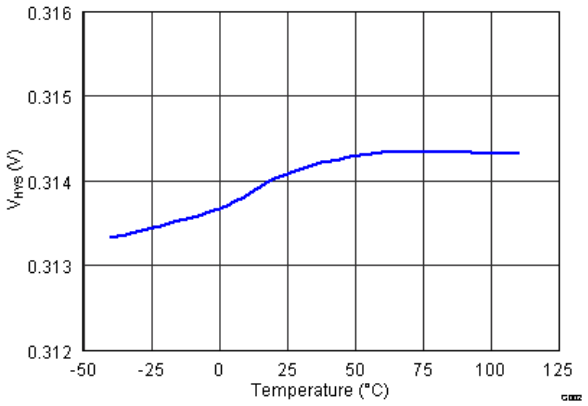

図 9-4. Hysteresis V_{HYS} vs. Temperature

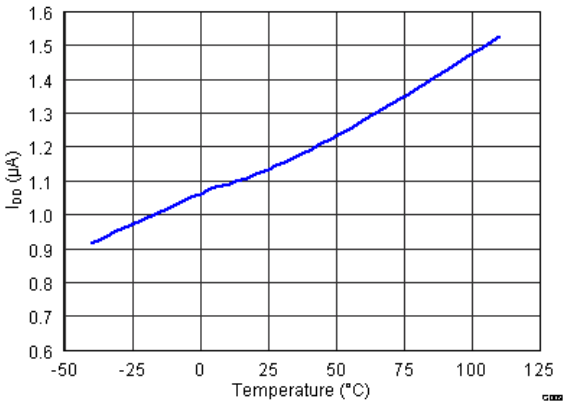

図 9-5. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

10 Power Supply Recommendations

The maximum power of this device is 20 V on VDD.

11 Layout

11.1 Layout Guidelines

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for CD pin should be placed close to the IC terminals.

11.2 Layout Example

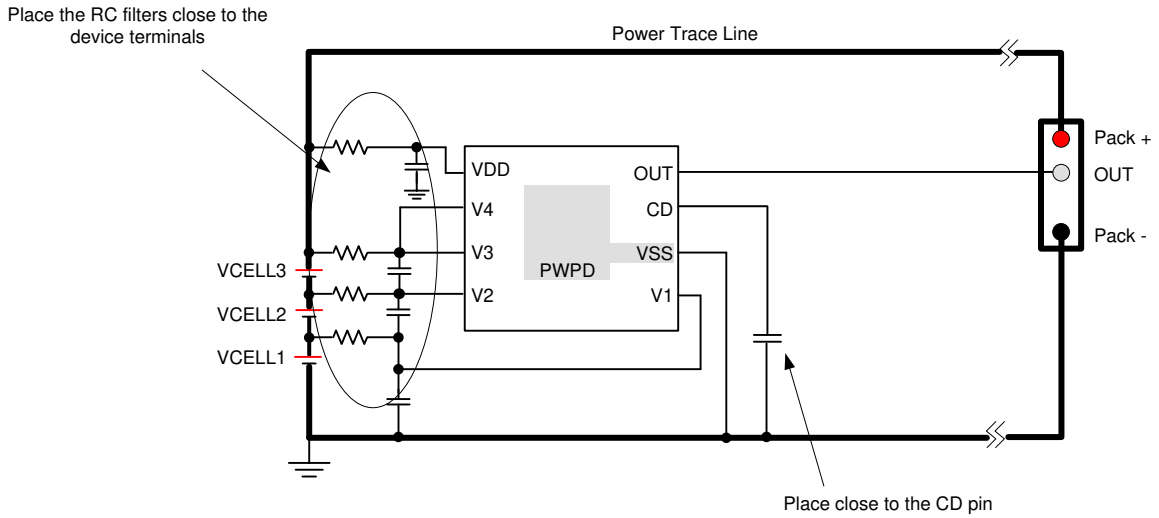

図 11-1. Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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13 Mechanical, Packaging, and Orderable Information

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ771600DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	771600
BQ771600DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771600
BQ771600DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	771600
BQ771600DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771600
BQ771601DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	771601
BQ771601DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771601
BQ771601DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	771601
BQ771601DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771601
BQ771602DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	771602
BQ771602DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771602
BQ771602DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	771602
BQ771602DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771602
BQ771604DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771604
BQ771604DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771604
BQ771604DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771604
BQ771604DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771604
BQ771605DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605
BQ771605DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605
BQ771605DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605
BQ771605DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605
BQ771611DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611
BQ771611DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611
BQ771611DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611
BQ771611DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611
BQ771612DPJR	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612
BQ771612DPJR.A	Active	Production	WSON (DPJ) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612
BQ771612DPJT	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612
BQ771612DPJT.A	Active	Production	WSON (DPJ) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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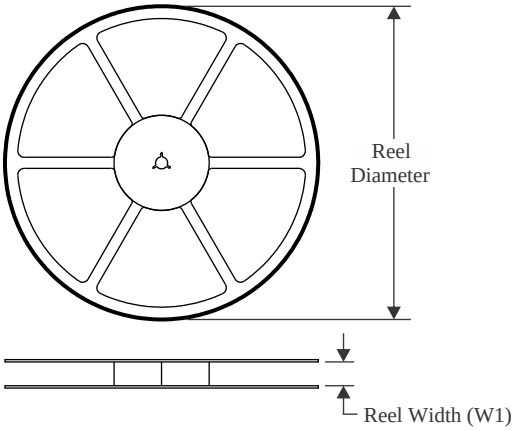
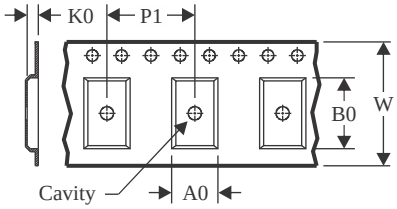
TAPE AND REEL INFORMATION

REEL DIMENSIONS

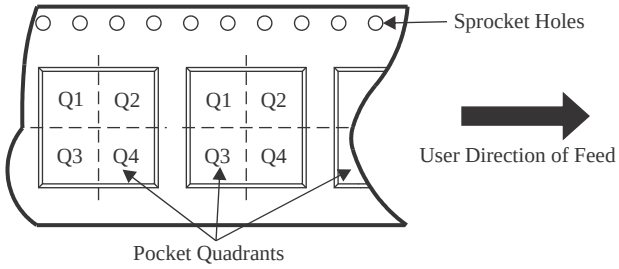


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

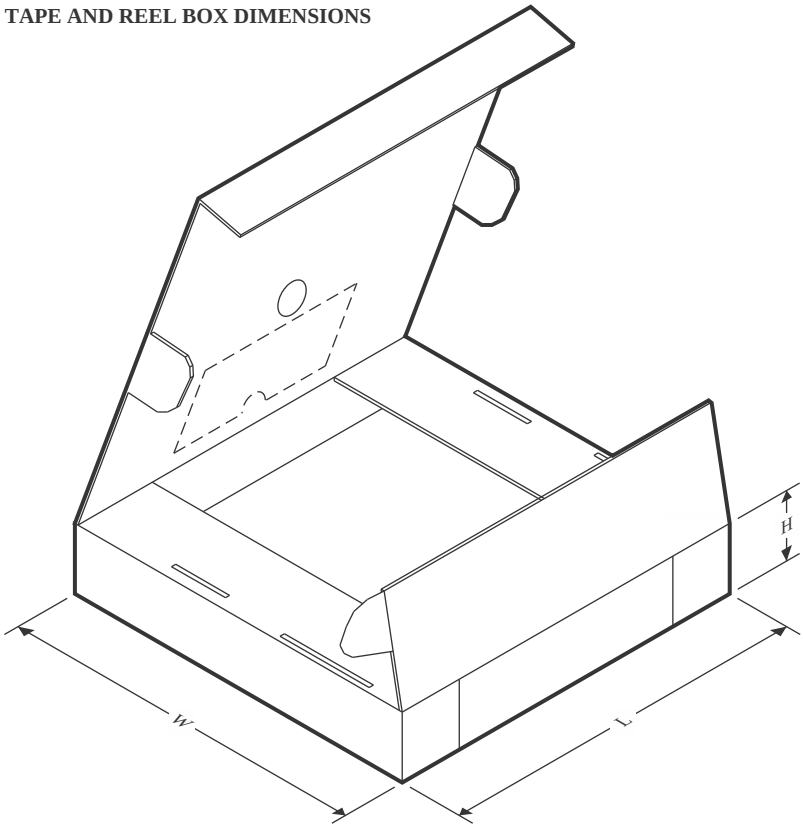
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771600DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771612DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771612DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

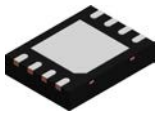


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771600DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771600DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771601DPJR	WSON	DPJ	8	3000	346.0	346.0	33.0
BQ771601DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771602DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771602DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771604DPJR	WSON	DPJ	8	3000	346.0	346.0	33.0
BQ771604DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771605DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771605DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771611DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771611DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771612DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771612DPJT	WSON	DPJ	8	250	182.0	182.0	20.0

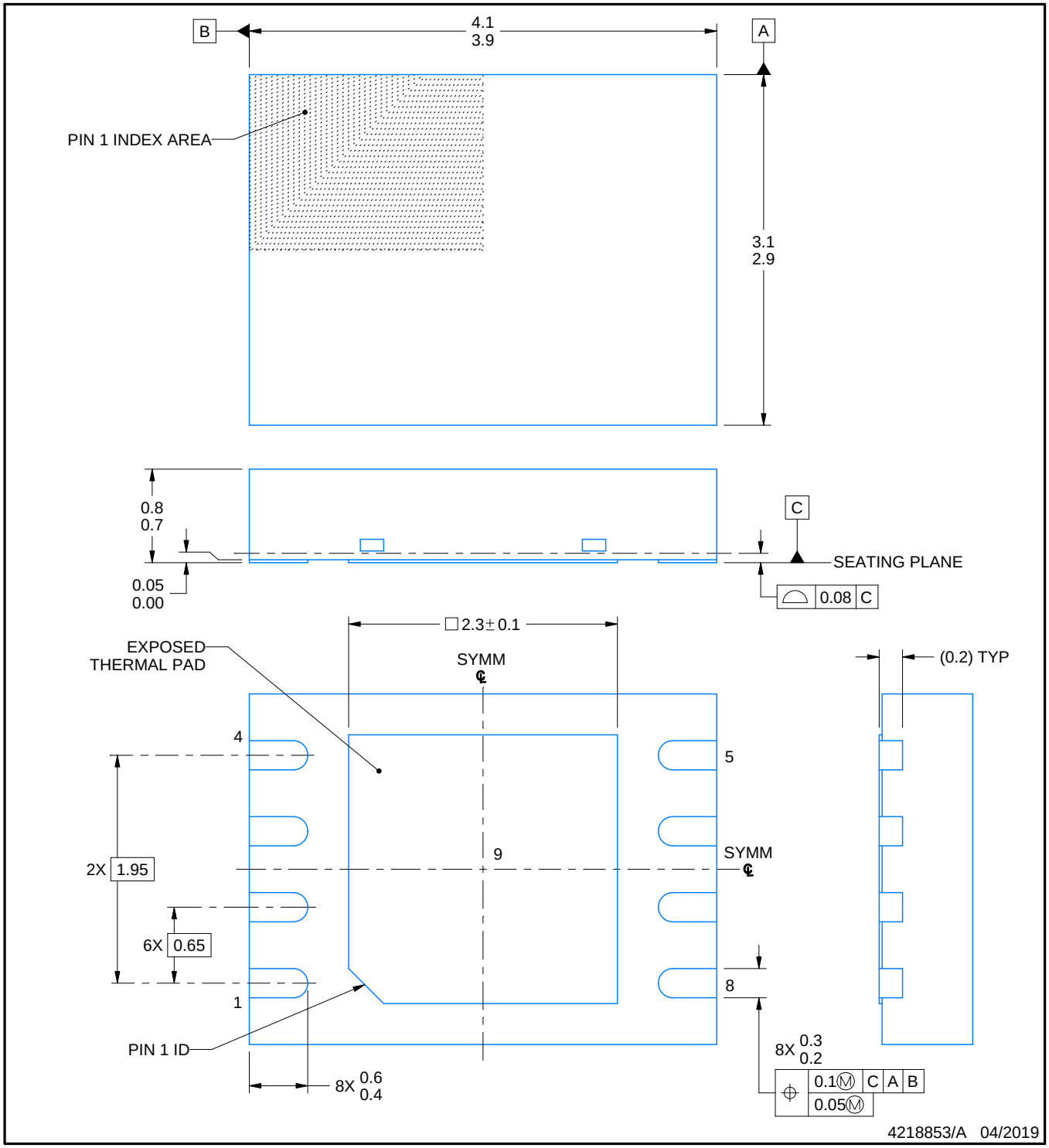
PACKAGE OUTLINE

DPJ0008A



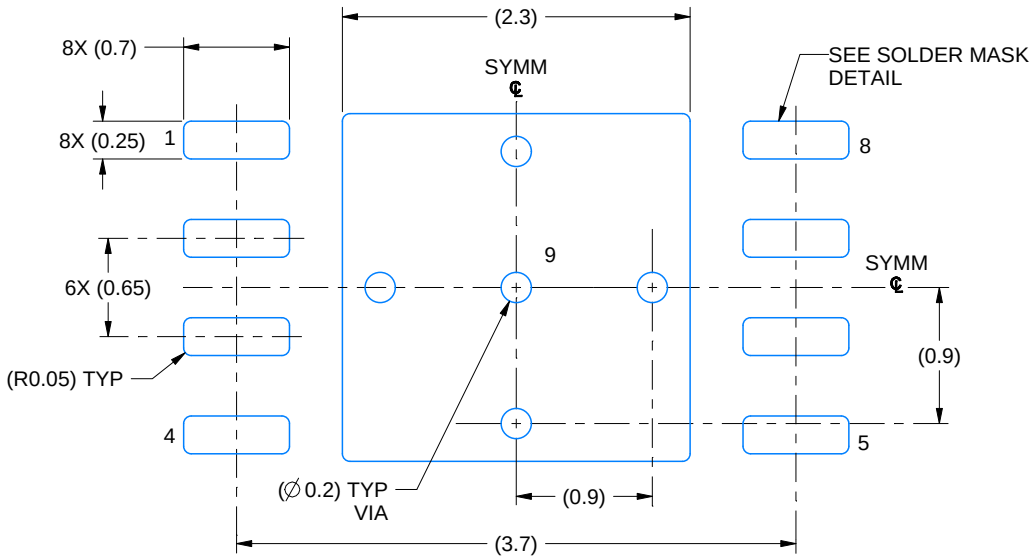
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

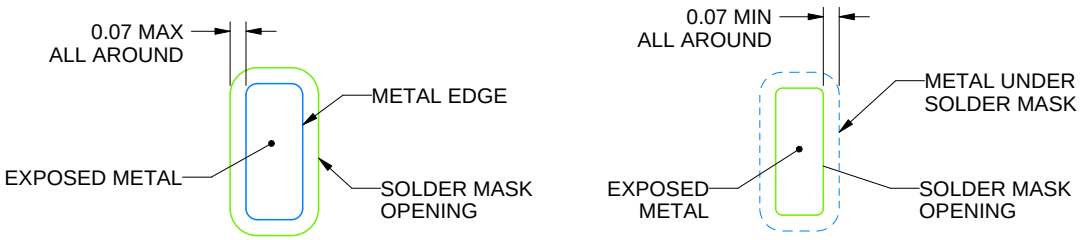


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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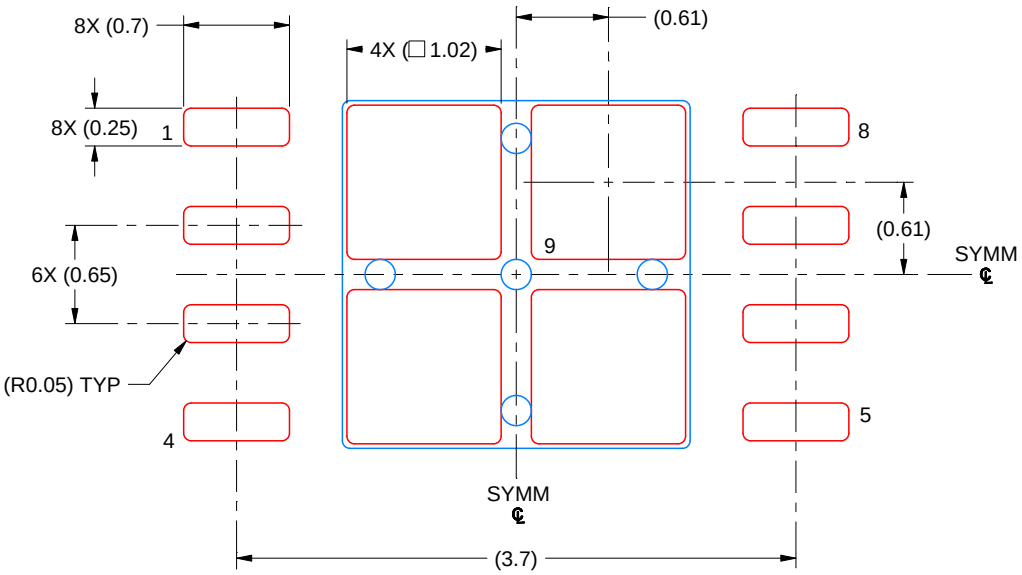
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 9
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218853/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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