TEXAS INSTRUMENTS
CD54HC393, CD74HC393, CD54HCT393, CD74HCT393
JAJSO95F – SEPTEMBER 1997 – REVISED MARCH 2022

CDx4HC393、CDx4HCT393 ハイスピード CMOS ロジック、デュアル、4 段バイナリ・カウンタ

1 特長

- 完全静的動作
- バッファ付き入力
- コモン・リセット
- ネガティブ・エッジ・クロッキング
- ファンアウト (全温度範囲にわたって):
  - 標準出力は 10 個の LSTTL 負荷を駆動可能
  - バス・ドライバ出力は 15 個の LSTTL 負荷を駆動可能
- 広い動作温度範囲:–55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:N_{IL} = V_{CC} の 30%、N_{IH} = V_{CC} の 30% (VCC = 5V の場合)
- HCT タイプ
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、V_{IL} = 0.8V (最大値)、V_{IH} = 2V (最小値)
  - CMOS 入力互換、V_{OL}、V_{OH} で $I_I \leq 1\mu A$

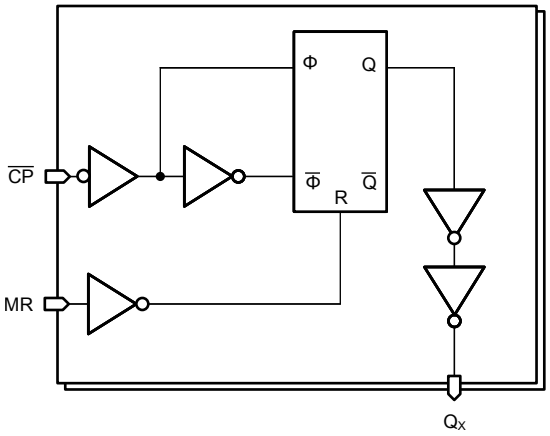
2 概要

HC393 と HCT393 は、4 段リップルキャリー・バイナリ・カウンタです。すべてのカウンタ段は、1 次動作可能なフリップ・フロップです。段の状態は、各クロック・パルスの負の遷移時に 1 カウント進み、MR ラインが High レベルになると、すべてのカウンタがゼロ状態にリセットされます。すべての入出力はバッファ付きです。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
CD74HC393M	SOIC (14)	8.65mm × 3.90mm
CD74HC393E	PDIP (14)	19.31mm × 6.35mm
CD74HCT393M	SOIC (14)	8.65mm × 3.90mm
CD74HCT393E	PDIP (14)	19.31mm × 6.35mm
CD54HC393F3A	CDIP (14)	19.55mm × 6.71mm
CD54HCT393F	CDIP (14)	19.55mm × 6.71mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (August 2003) to Revision F (March 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1

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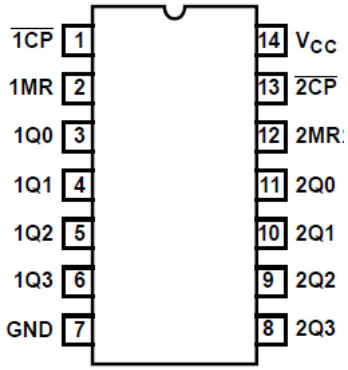
4 Pin Configuration and Functions



J, N, or D package
14-PIN CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For V_I < –0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output diode current	For V_O < –0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Output source or sink current per output pin	For V_O> –0.5 V or V_O < V_{CC} + 0.5 V		±25	mA
	Continous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	DC input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	N (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	86	80	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			-40℃ to 85℃		-55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I_{OH} – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low level output voltage TTL loads	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	6			8		80		160	μA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage TTL loads	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} and GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	5.5			8		80		160	μA
ΔI_{CC} (1)	Additional supply current per input pin	$n\overline{CP}$ input held at V_{CC} -2.1	4.5 to 5.5		100	144		180		196	μA
		nMR input held at V_{CC} – 2.1	4.5 to 5.5		100	360		450		490	μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

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5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25℃			-40℃ to 85℃		-55℃ to 125℃		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
f_{MAX}	Maximum clock frequency	2	6			5		4		MHz
		4.5	30			24		20		
		6	35			28		24		
t_W	Clock pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t_{REC}	Reset recovery time	2	5			5		5		ns
		4.5	5			5		5		
		6	5			5		5		
t_W	Reset pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
HCT TYPES										
f_{MAX}	Maximum clock frequency	4.5	27			22		18		MHz
t_W	Clock pulse width	4.5	19			24		29		ns
t_{REC}	Reset recovery time	4.5	5			5		5		ns
t_W	Reset pulse width	4.5	16			20		24		ns

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. See (Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			-40℃ to 85℃		-55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay time $n\overline{CP}$ to nQ_0	C_L = 50 pF	2			150		190		225	ns
			4.5			30		38		59	
		C_L = 15 pF	5		12						ns
		C_L = 50 pF	6			26		33		50	ns
t_{PLH}, t_{PHL}	$n\overline{CP}$ to nQ_1	C_L = 50 pF	2			190		245		295	ns
			4.5			38		49		59	
			6			33		42		50	
t_{PLH}, t_{PHL}	$n\overline{CP}$ to nQ_2	C_L = 50 pF	2			240		300		360	ns
			4.5			48		60		72	
			6			41		51		61	
t_{PLH}, t_{PHL}	$n\overline{CP}$ to nQ_3	C_L = 50 pF	2			285		355		430	ns
			4.5			57		71		86	
			6			48		60		73	
t_{PLH}, t_{PHL}	MR to Q_n	C_L = 50 pF	2			135		170		205	ns
			4.5			27		34		41	
		C_L = 15 pF	5		11						ns
		C_L = 50 pF	6			23		29		35	

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5.6 Switching Characteristics (continued)

Input t_r, t_f = 6 ns. See (Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			-40℃ to 85℃		-55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	2			75		95		110	ns
			4.5			15		19		22	
			6			13		16		19	
C_{IN}	Input capacitance	C_L = 50 pF				10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)	C_L = 15 pF	5		20						pF
HCT TYPES											
t_{PLH}, t_{PHL}	Propagation delay time $n\overline{CP}$ to nQ_0	C_L = 50 pF	4.5			32		40		48	ns
		C_L = 15 pF	5		13						ns
t_{PLH}, t_{PHL}	$n\overline{CP}$ to nQ_1	C_L = 50 pF	4.5			44		55		66	ns
t_{PLH}, t_{PHL}	$n\overline{CP}$ to nQ_2	C_L = 50 pF	4.5			50		63		75	ns
t_{PLH}, t_{PHL}	n_{CP} to nQ_3	C_L = 50 pF	4.5			62		78		93	ns
t_{PLH}, t_{PHL}	MR to Q_n	C_L = 50 pF	4.5			32		40		48	ns
		C_L = 15 pF	5		13						ns
t_{TLH}, t_{THL}	Output transition	C_L = 50 pF	4.5			15		19		22	ns
C_{IN}	Input capacitance	C_L = 15 pF				10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)	C_L = 15 pF	5		21						pF

(1) C_{PD} is used to determine the dynamic power consumption, per stage.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

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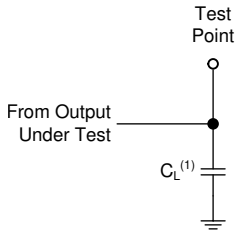
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

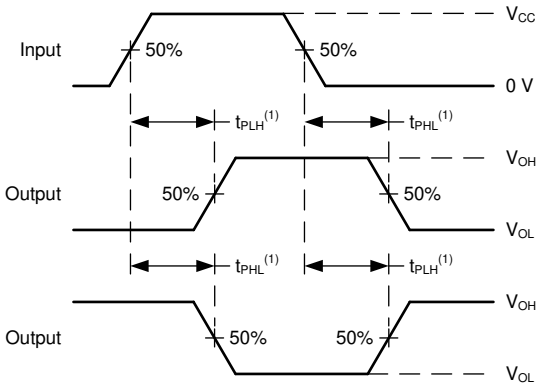
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



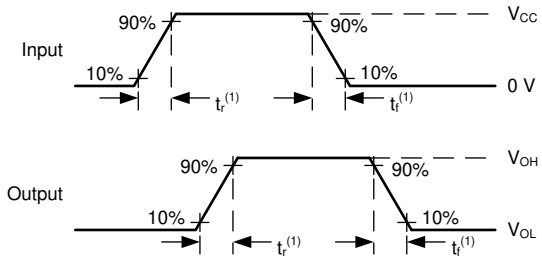
(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for Push-Pull Outputs



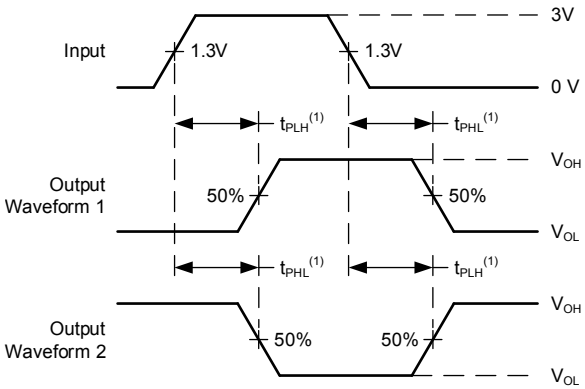
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

図 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

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7 Detailed Description

7.1 Overview

The ’HC393 and ’HCT393 are 4-stage ripple-carry binary counters. All counter stages are controller flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

7.2 Functional Block Diagram

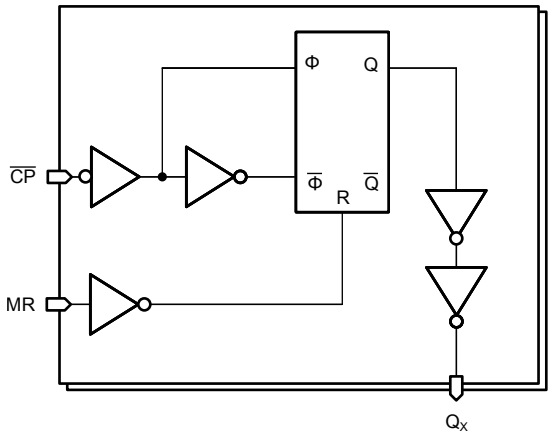

図 7-1. Functional Diagram

7.3 Device Functional Modes

表 7-1. Truth Table(1)

CP COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

(1) H = high voltage level, L = low voltage level, X = don’t care, ↑ = transition from low to high level, ↓ = transition from high to low.

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表 7-2. Truth Table(1)

CP COUNT	MR	OUTPUT
↑	L	No change
↓	L	Count
X	H	L L L L

(1) H = high voltage level, L = low voltage level, X = don't care, ↑ = transition from low to high level, ↓ = transition from high to low.

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8989001CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8989001CA CD54HCT393F3A
CD54HC393F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8410001CA CD54HC393F3A
CD54HC393F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8410001CA CD54HC393F3A
CD54HCT393F	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT393F
CD54HCT393F.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT393F
CD54HCT393F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8989001CA CD54HCT393F3A
CD54HCT393F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8989001CA CD54HCT393F3A
CD74HC393E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC393E
CD74HC393E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC393E
CD74HC393M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC393M
CD74HC393M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC393M
CD74HC393M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC393M
CD74HCT393E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT393E
CD74HCT393E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT393E
CD74HCT393M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT393M
CD74HCT393M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT393M
CD74HCT393MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT393M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC393, CD54HCT393, CD74HC393, CD74HCT393 :

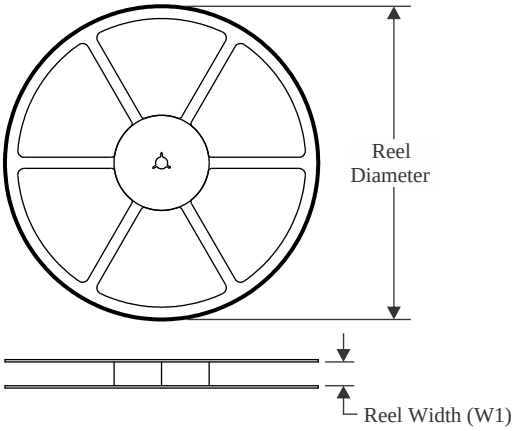
- Catalog : CD74HC393, CD74HCT393
- Military : CD54HC393, CD54HCT393

NOTE: Qualified Version Definitions:

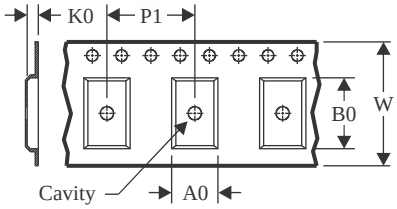
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

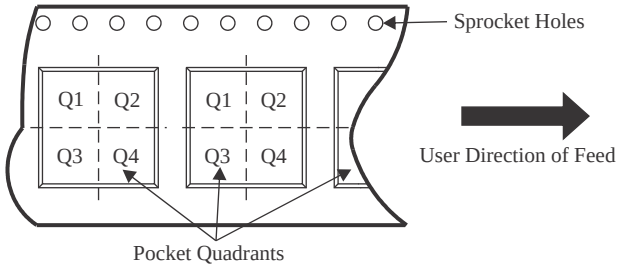


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

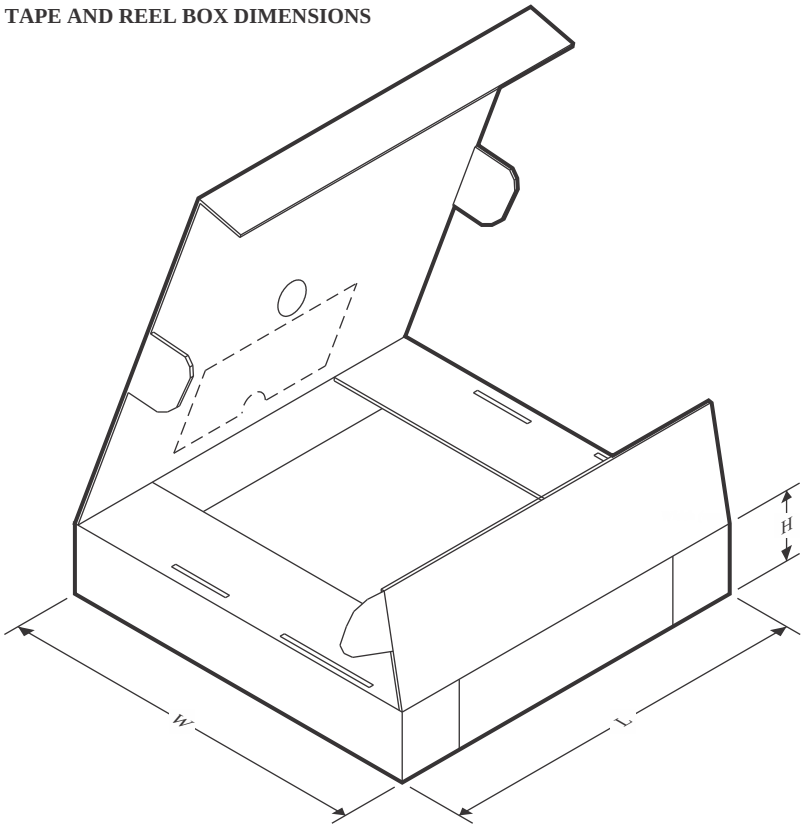
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC393M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT393M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

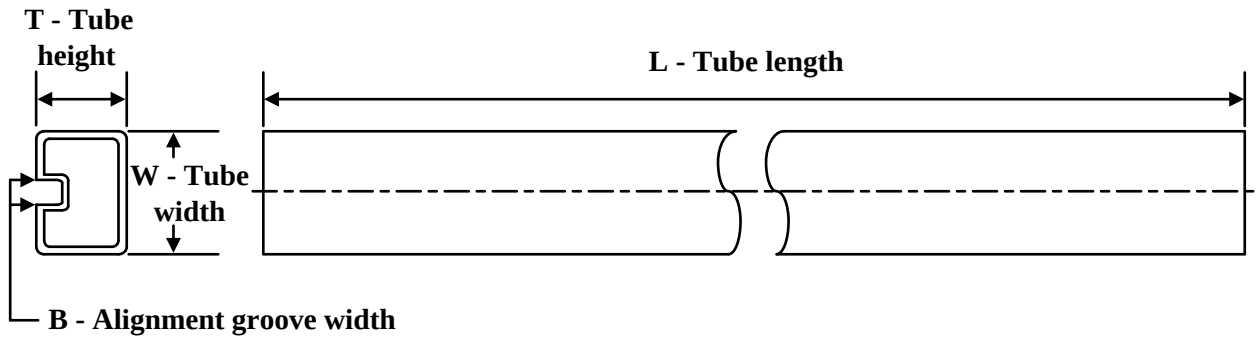
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC393M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HCT393M96	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



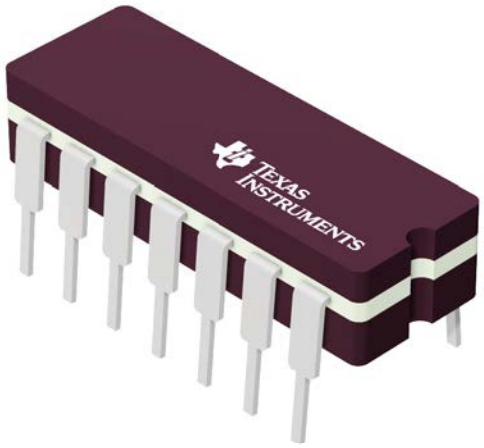
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC393E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC393E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC393E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC393E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT393E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT393E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT393E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT393E.A	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

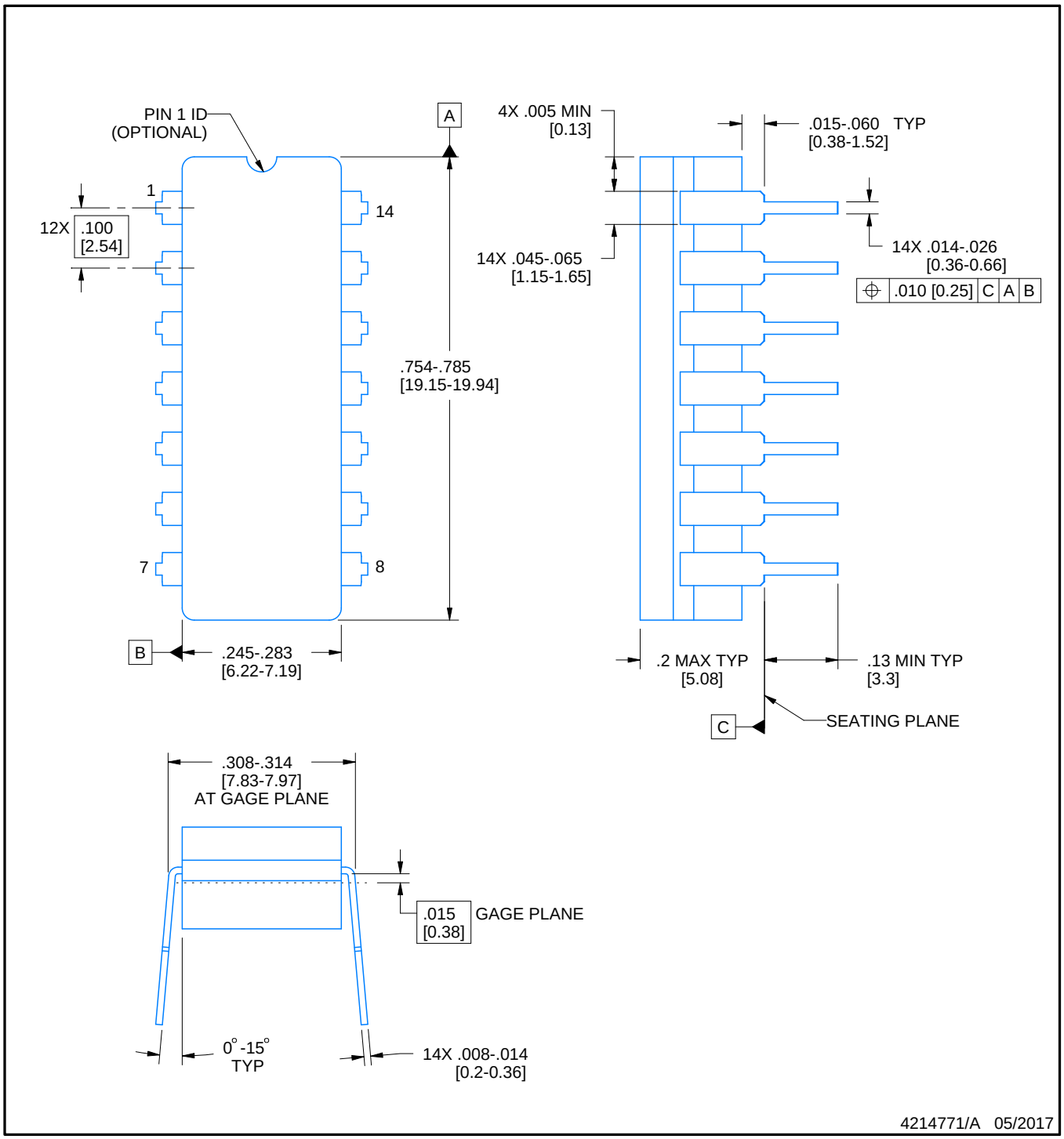
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

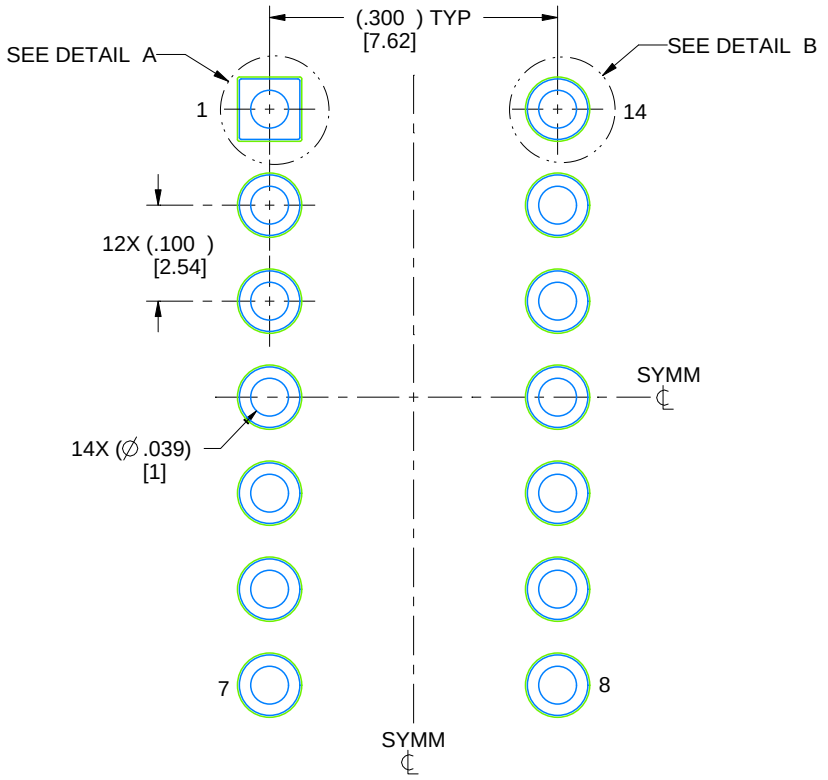
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

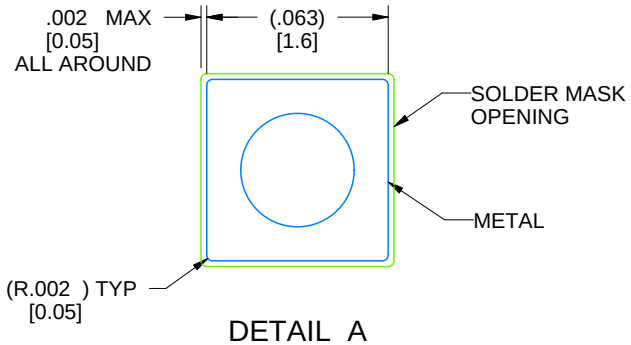
J0014A

CDIP - 5.08 mm max height

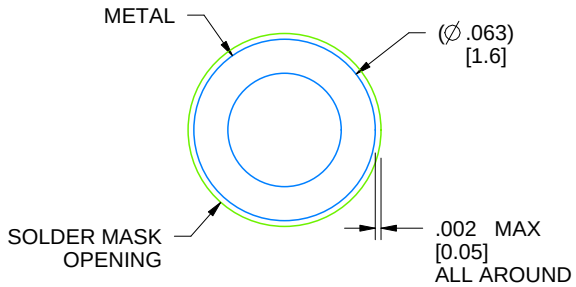
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



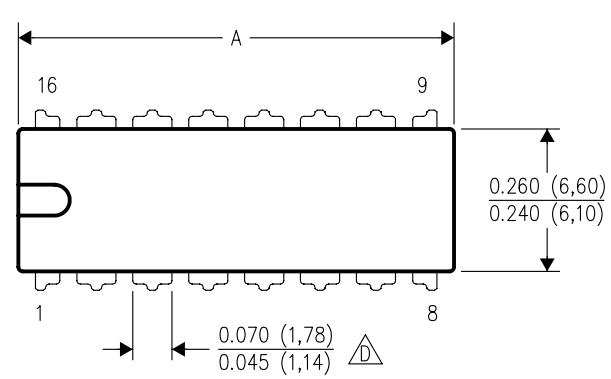
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

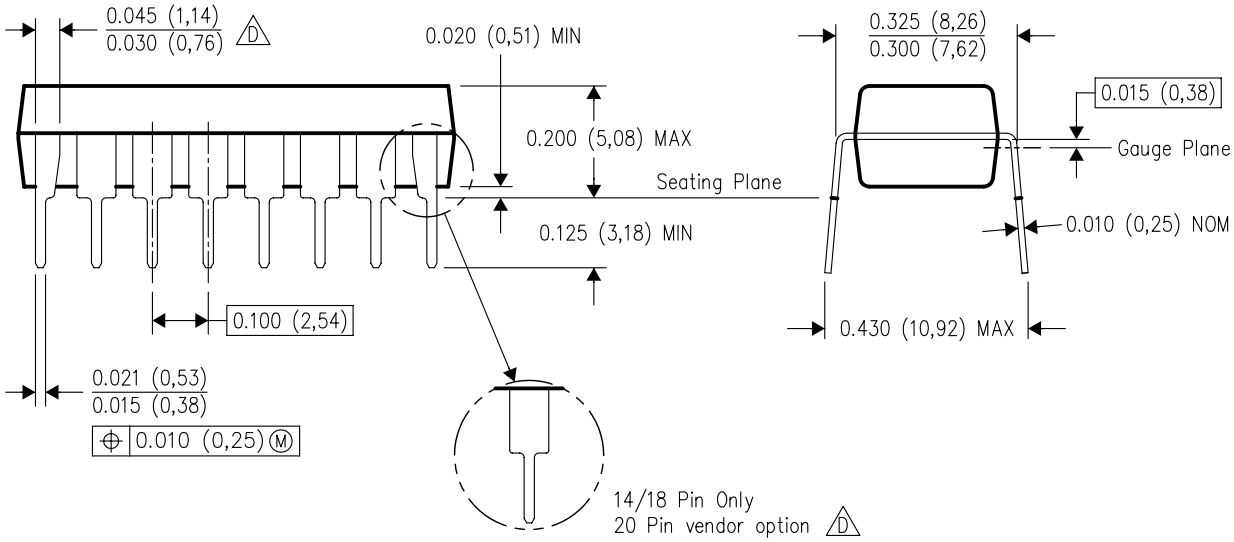
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

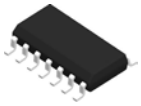


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

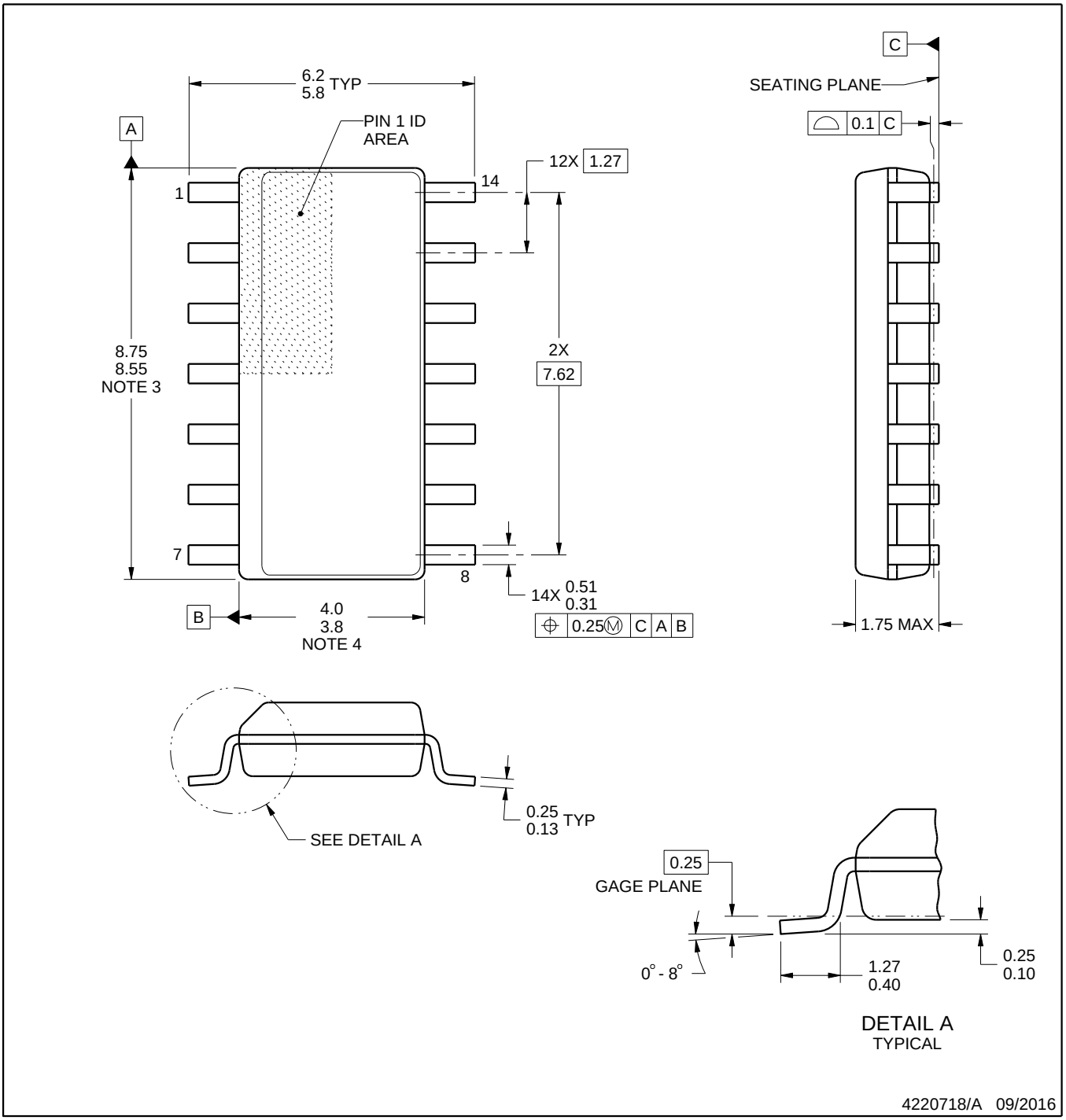


PACKAGE OUTLINE

D0014A

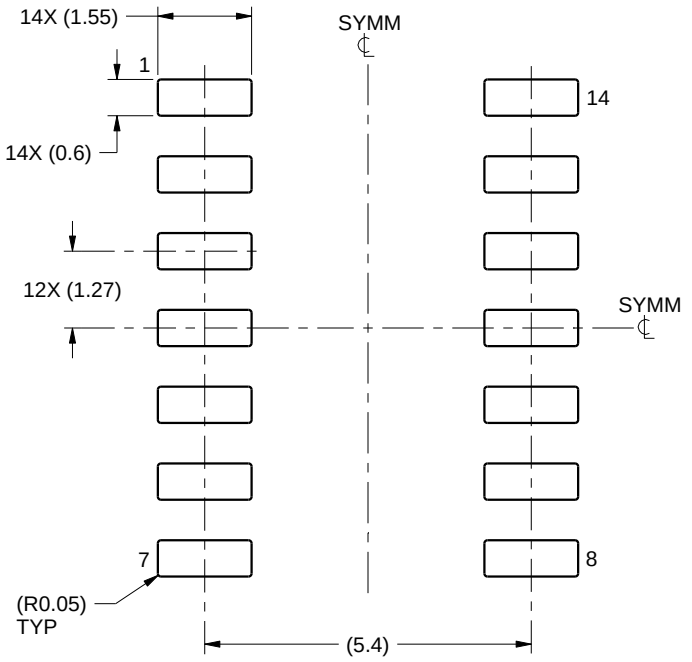
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

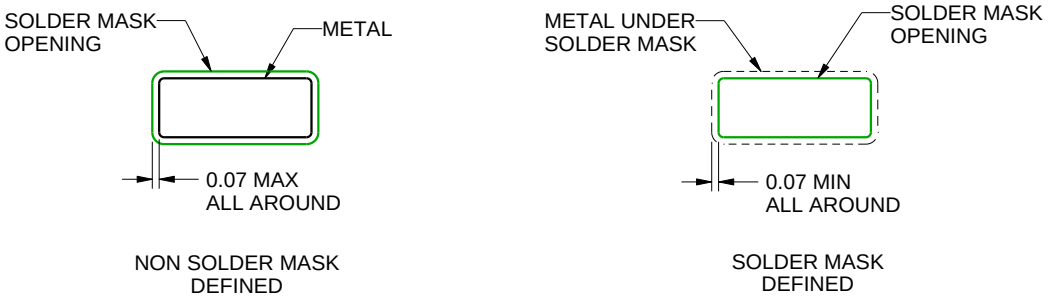


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

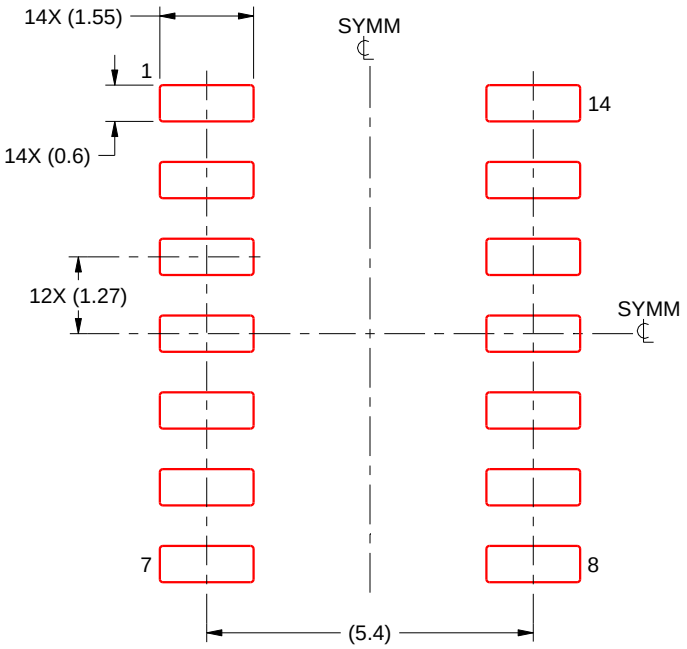
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月