

CDx4HC4040、CDx4HCT4040 高速 CMOS ロジック、12 段バイナリ・カウンタ

1 特長

- 完全静的動作
- バッファ付き入力
- コモン・リセット
- 負のエッジのパルス
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 個の LSTTL 負荷
 - バス・ドライバ出力: 15 個の LSTTL 負荷
- 広い動作温度範囲: $-55^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- 平衡のとれた伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V~6V で動作
 - 優れたノイズ耐性: V_{CC} に対して $N_{\text{IL}} = 30\%$ ($V_{\text{CC}} = 5\text{V}$ 時)
- HCT タイプ
 - 4.5V~5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{\text{IL}} = 0.8\text{V}$ (最大値)、 $V_{\text{IH}} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_{\text{L}} \leq 1\mu\text{A}$

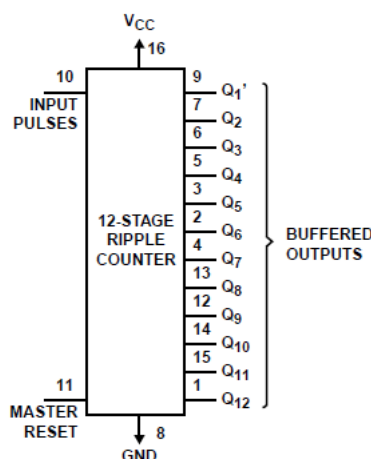
2 概要

'HC4040 および 'HCT4040 は、14 段リップルキャリー・バイナリ・カウンタです。すべてのカウンタ段は、コントローラ・フリップフロップです。段の状態は、各入力パルスの負のクロック遷移時に 1 カウント進み、MR ラインが High 電圧レベルになると、すべてのカウンタがゼロ状態にリセットされます。すべての入出力はバッファ付きです。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC4040	J (CDIP, 16)	24.38mm × 6.92mm
CD54HCT4040	J (CDIP, 16)	24.38mm × 6.92mm
CD74HC4040	D (SOIC, 16)	9.90mm × 3.90mm
	N (PDIP, 16)	19.31mm × 6.35mm
CD74HCT4040	D (SOIC, 16)	9.90mm × 3.90mm
	N (PDIP, 16)	19.31mm × 6.35mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



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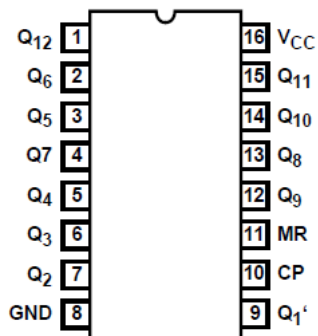
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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2003) to Revision E (July 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....	1

4 Pin Configuration and Functions



J, D, or N package
16-Pin CDIP, SOIC, or PDIP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		– 0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	(V _I < – 0.5 V or V _I > V _{CC} + 0.5 V)		± 20	mA
I _{OK}	Output clamp current ⁽²⁾	(V _O < – 0.5 V or V _O > V _{CC} + 0.5 V)		± 20	mA
I _O	Output source or sink current per output pin	(V _O > – 0.5 V or V _{CC} + 0.5 V)		± 25	mA
	Continuous current through V _{CC} or GND			± 50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		– 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V _I , V _O	DC input or output voltage		0	V _{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Temperature range		–55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	NS (SOP)	UNIT
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	64	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	
HC TYPES										
V _{IH}	High level input voltage		2	1.5		1.5		1.5		V
			4.5	3.15		3.15				
			6	4.2		4.2				
V _{IL}	Low level input voltage		2	0.5		0.5		0.5		V
			4.5	1.35		1.35				
			6	1.8		1.8				
V _{OH}	High level output voltage CMOS loads	I _{OH} = − 20 µA	2	1.9		1.9		1.9		V
		I _{OH} = − 20 µA	4.5	4.4		4.4				
		I _{OH} = − 20 µA	6	5.9		5.9				
	High level output voltage TTL loads	I _{OH} − 4 mA	4.5	3.98		3.84		3.7		V
		I _{OH} − 5.2 mA	6	5.48		5.34		5.2		
V _{OL}	Low level output voltage CMOS loads	I _{OL} = 20 µA	2	0.1		0.1		0.1		V
		I _{OL} = 20 µA	4.5	0.1		0.1				
		I _{OL} = 20 µA	6	0.1		0.1				
	Low level output voltage TTL loads	I _{OL} = 4 mA	4.5	0.26		0.33		0.4		V
		I _{OL} = 5.2 mA	6	0.26		0.33		0.4		
I _I	Input leakage current	V _{CC} or GND	6	±0.1		±1		±1		µA
I _{CC}	Supply current	V _{CC} or GND	6	8		80		160		µA
HCT TYPES										
V _{IH}	High level input voltage		4.5 to 5.5	2		2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8		0.8		0.8		V
V _{OH}	High level output voltage CMOS loads	I _{OH} = − 20 µA	4.5	4.4		4.4		4.4		V
	High level output voltage TTL loads	I _{OH} = − 4 mA	4.5	3.98		3.84		3.7		V
V _{OL}	Low level output voltage CMOS loads	I _{OL} = 20 µA	4.5	0.1		0.1		0.1		V
	Low level output voltage TTL loads	I _{OL} = 4 mA	4.5	0.26		0.33		0.4		V
I _I	Input leakage current	V _{CC} and GND	5.5	±0.1		±1		±1		µA
I _{CC}	Supply current	V _{CC} or GND	5.5	8		80		160		µA
ΔI _{CC} ⁽²⁾	Additional supply current per input pin	MR input held at V _{CC} -2.1	4.5 to 5.5	100	234	292.5		318.5		µA
		CP input held at V _{CC} − 2.1	4.5 to 5.5	100	180	225		245		µA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
f _{MAX}	Maximum input pulse frequency	2	6			5		4		MHz
		4.5	30			25		20		
		6	35			29		24		
t _W	Input pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
t _{REM}	Reset removal time	2	50			65		75		ns
		4.5	10			13		15		
		6	9			11		13		
t _W	Reset pulse width	2	80			100		120		ns
		4.5	16			20		24		
		6	14			17		20		
HCT TYPES										
f _{MAX}	Maximum input pulse frequency	4.5	25			20		16		MHz
t _W	Input pulse width	4.5	20			25		30		ns
t _{REC}	Reset recovery time	4.5	10			13		15		ns
t _W	Reset pulse width	4.5	20			25		30		ns

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. See [Parameter Measurement Information](#)

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t _{PLH} , t _{PHL}	Propagation delay time CP to Q1' Output	C _L = 50 pF	2	140			175		210		ns
			4.5	28			35		42		
		C _L = 15 pF	5	11							
		C _L = 50 pF	6	24			30		36		
t _{PLH} , t _{PHL}	Q _n to Q _n + 1	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		
		C _L = 15 pF	5	4							
		C _L = 50 pF	6	13			16		19		
t _{PLH} , t _{PHL}	MR to Q _n	C _L = 50 pF	2	170			215		255		ns
			4.5	34			43		51		
			5	14							
			6	29			37		43		
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		
			6	13			16		19		
C _{IN}	Input capacitance	C _L = 50 pF		10			10		10		pF
C _{PD}	Power dissipation capacitance ^{(1) (2)}	C _L = 15 pF	5	40							pF
HCT TYPES											

5.6 Switching Characteristics (continued)

Input t_r , t_f = 6 ns. See [Parameter Measurement Information](#)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} , t_{PHL}	Propagation delay time CP to Q1' Output	$C_L = 50$ pF	4.5			40		50		60	ns
		$C_L = 15$ pF	5		17						
t_{PLH} , t_{PHL}	Q_n to Q_{n+1}	$C_L = 50$ pF	4.5			15		19		22	ns
		$C_L = 15$ pF	5		4						
t_{PLH} , t_{PHL}	MR to Q_n	$C_L = 50$ pF	4.5			40		50		60	ns
		$C_L = 15$ pF	5		17						
t_{TLH} , t_{THL}	Output transition	$C_L = 50$ pF	4.5			15		19		22	ns
C_{IN}	Input capacitance	$C_L = 50$ pF				10		10		10	pF
C_{PD}	Power dissipation capacitance ^{(1) (2)}	$C_L = 15$ pF	5		45						pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.

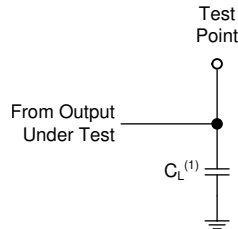
(2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input frequency, C_L = Output load capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

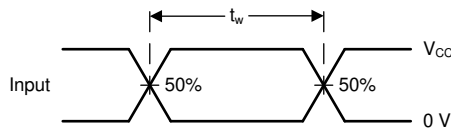
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

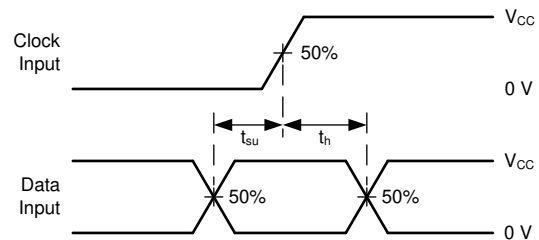


(1) C_L includes probe and test-fixture capacitance.

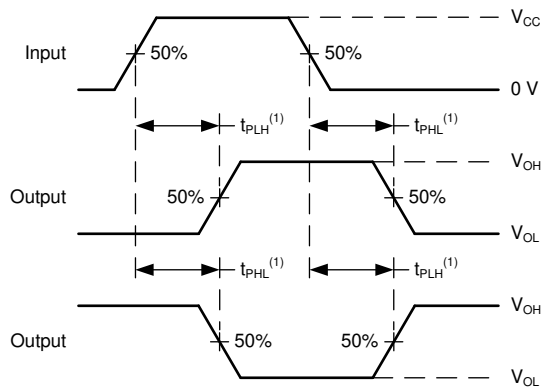
FIG 6-1. Load Circuit for Push-Pull Outputs



**FIG 6-2. Voltage Waveforms, Standard CMOS Inputs
 Pulse Duration**

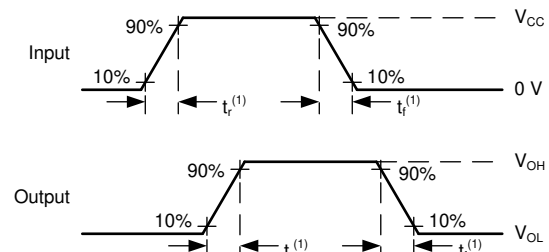


**FIG 6-3. Voltage Waveforms, Standard CMOS Inputs
 Setup and Hold Times**



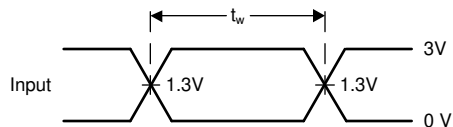
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

**FIG 6-4. Voltage Waveforms, Propagation Delays for
 Standard CMOS Inputs**

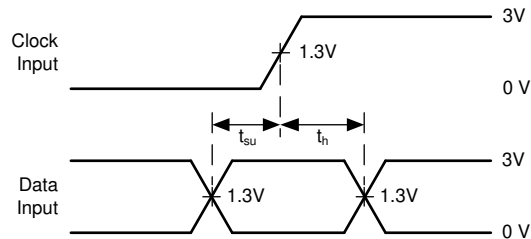


(1) The greater between t_r and t_f is the same as t_t .

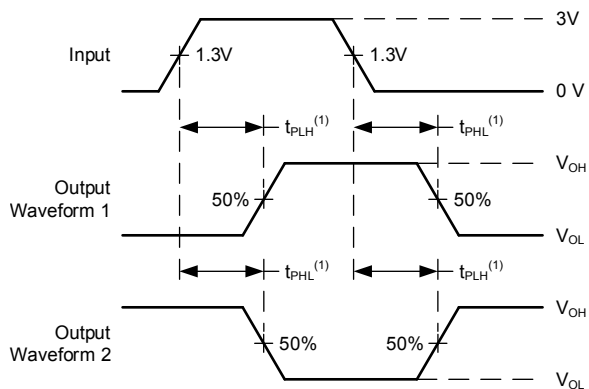
**FIG 6-5. Voltage Waveforms, Input and Output
 Transition Times for Standard CMOS Inputs**



6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration



6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

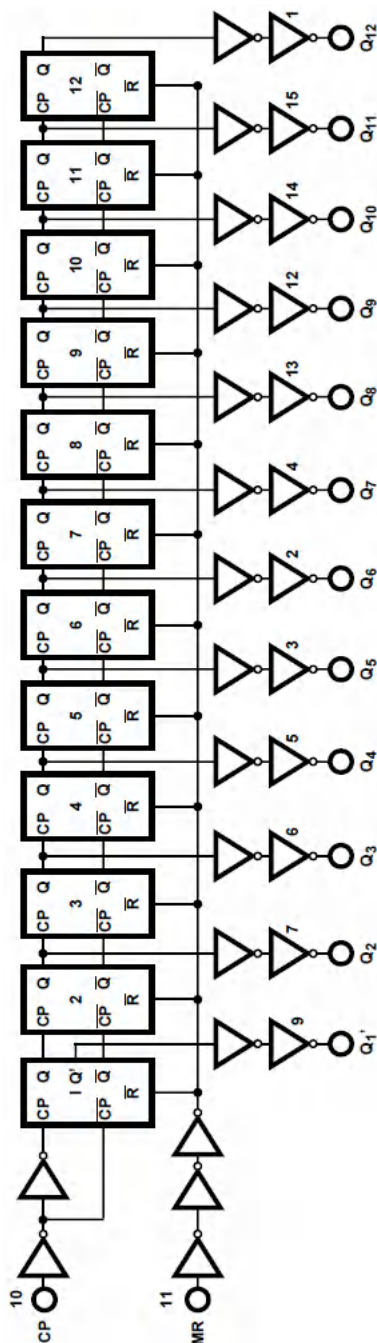
6-8. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The 'HC4040 and 'HCT4040 are 14-stage ripple-carry binary counters. All counter stages are controller flipflops. The state of the stage advances one count on the negative clock transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

7.2 Functional Block Diagram



7-1. Functional Block Diagram

7.3 Device Functional Modes

Function Table
(Each Flip-Flop)⁽¹⁾

CP COUNT	MR	OUTPUT STATE
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

(1) H = High voltage level, L = Low voltage level, X = Don't care, ↑ = Transition time from low to high level, ↓ = Transition from high to low.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8994701MEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994701ME A CD54HCT4040F3A
CD54HC4040F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4040F
CD54HC4040F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4040F
CD54HC4040F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500401EA CD54HC4040F3A
CD54HC4040F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8500401EA CD54HC4040F3A
CD54HCT4040F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994701ME A CD54HCT4040F3A
CD54HCT4040F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8994701ME A CD54HCT4040F3A
CD74HC4040E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4040E
CD74HC4040E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4040E
CD74HC4040M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC4040M
CD74HC4040M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4040M
CD74HC4040M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4040M
CD74HC4040M961G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4040M
CD74HC4040M961G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4040M
CD74HCT4040E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4040E
CD74HCT4040E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4040E
CD74HCT4040M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT4040M
CD74HCT4040M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4040M
CD74HCT4040M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4040M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC4040, CD54HCT4040, CD74HC4040, CD74HCT4040 :

- Catalog : [CD74HC4040](#), [CD74HCT4040](#)
- Military : [CD54HC4040](#), [CD54HCT4040](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4040M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4040M961G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4040M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4040M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4040M961G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4040M96	SOIC	D	16	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4040E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4040E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4040E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4040E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4040E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4040E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4040E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4040E.A	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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