TEXAS INSTRUMENTS
CD74HC595
JAJSO10A – JANUARY 2004 – REVISED FEBRUARY 2022

CD74HC595 3 ステート出力レジスタ搭載 8 ビット・シフト・レジスタ

1 特長

- 8 ビットのシリアル入力、パラレル出力シフト
- 幅広い動作電圧範囲:2V～6V
- 大電流 3 ステート出力により最大 15 個の LSTTL 負荷を駆動可能
- 低消費電力、最大 I_{CC} 80μA
- t_{PD} = 14ns (標準値)
- 5V で ±6mA の出力駆動能力
- 低い入力電流:最大 1μA
- シフト・レジスタはダイレクト・クリアを装備

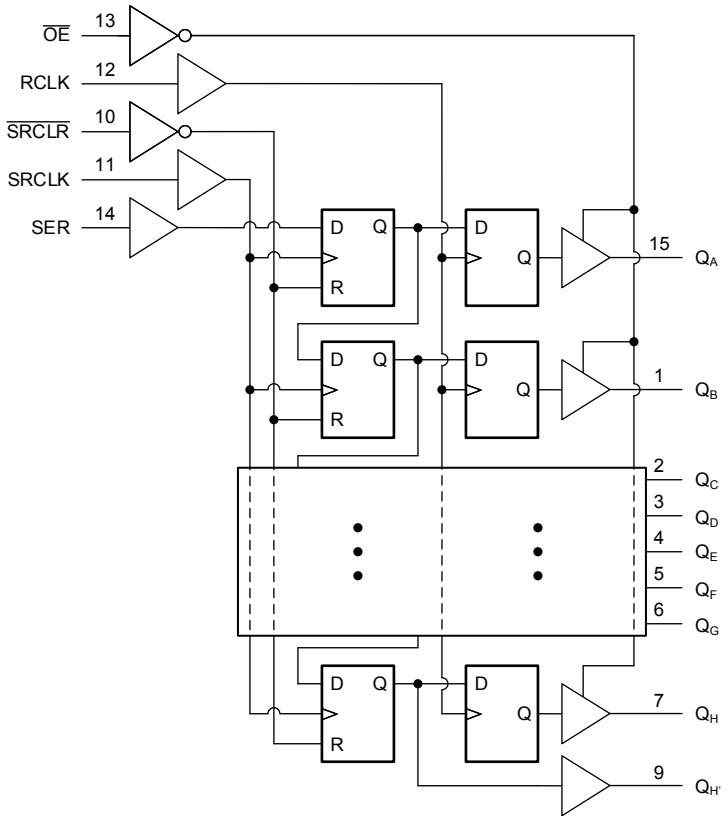
2 概要

CD74HC595 は、出力レジスタおよび 3 ステート出力を備えた 8 ビット・シリアル入力パラレル出力シフト・レジスタです。

デバイス情報

部品番号	パッケージ (1)	本体サイズ (公称)
CD74HC595E	PDIP (16)	19.31mm × 6.35mm
CD74HC595DW	SOIC-DW (16)	10.30mm × 7.50mm
CD74HC595M	SOIC-D (16)	9.90mm × 3.90mm
CD74HC595NS	SO (16)	10.20mm × 5.30mm
CD74HC595SM	SSOP (16)	6.20mm × 5.30mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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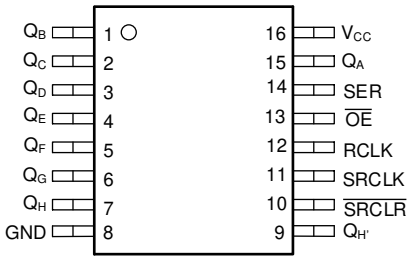
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (January 2004) to Revision A (February 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1

4 Pin Configuration and Functions



D, DW, N, NS, or DB Package
16-Pin SOIC, PDIP, SO, or SSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input clamp current(2)	For $V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	For $V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continous output current	For -0.5V < V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5			V
		V_{CC} = 4.5V	3.15			
		V_{CC} = 6V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2V			0.5	V
		V_{CC} = 4.5V			1.35	
		V_{CC} = 6V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t (2)	Input transition rise and fall time	V_{CC} = 2V			1000	ns
		V_{CC} = 4.5V			500	
		V_{CC} = 6V			400	
T_A	Operating free-air temperature		-55		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

5.3 Thermal Information

THERMAL METRIC		N (PDIP) 16 PINS	DW (SOIC) 16 PINS	D (SOIC) 16 PINS	NS (SO) 16 PINS	DB (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	67	57	73	64	82	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

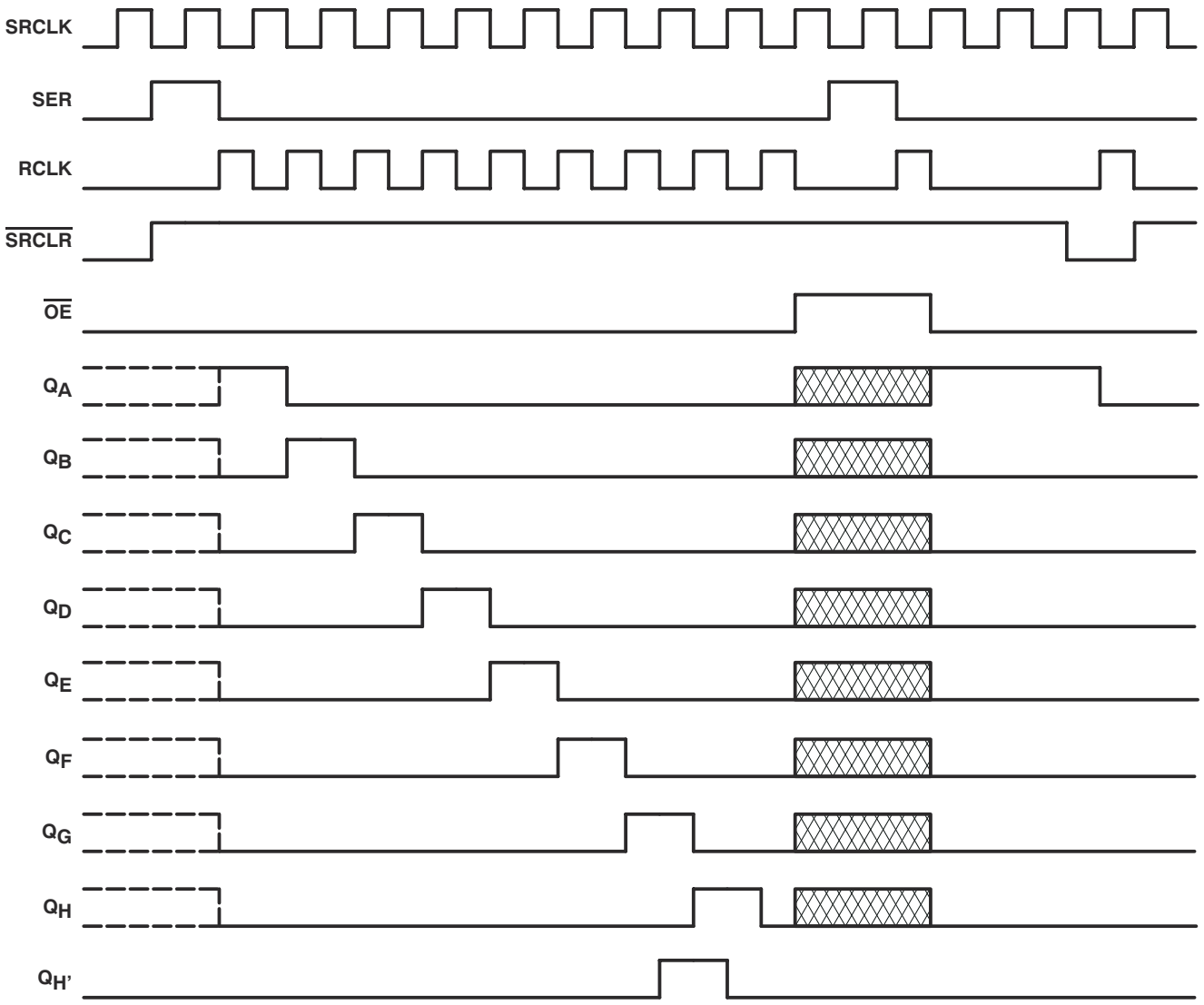
PARAMETER	TEST CONDITIONS[1]	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
V_{OH}	I_{OH} = – 20 µA	2	1.9	1.998		1.9		1.9		V
		4.5	4.4	4.499		4.4		4.4		
		6	5.9	5.999		5.9		5.9		
	$Q_{H'}$, I_{OH} = – 4 mA	4.5	3.98	4.3		3.84		3.7		
	Q_A-Q_H, I_{OH} = – 6 mA		3.98	4.3		3.84		3.7		
	$Q_{H'}$, I_{OH}= – 5.2 mA	6	5.48	5.8		5.34		5.2		
	Q_A-Q_H, I_{OH} = – 57.8 mA		5.48	5.8		5.34		5.2		
V_{OL}	I_{OL} = 20 µA	2		0.002	0.1		0.1		0.1	V
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	$Q_{H'}$, I_{OL} = 4 mA	4.5		0.17	0.26		0.33		0.4	V
	Q_A-Q_H, I_{OL} = 6 mA			0.17	0.26		0.33		0.4	V
	$Q_{H'}$, I_{OL}= 5.2 mA	6		0.15	0.26		0.33		0.4	V
	Q_A-Q_H, I_{OL} = 7.8 mA			0.15	0.26		0.33		0.4	V
I_I	V_I = V_{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0, QA-Q_H	6		±0.01	±0.5		±5		±10	µA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6			8		80		160	µA
C_i		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}

5.5 Timing Requirements

PARAMETER			V_{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
f_{clock}	Clock frequency		2		6		5		4.2	MHz
			4.5		31		25		21	
			6		36		29		25	
t_W	Pulse duration	SRCLK or RCLK high or low	2	80		100		120		ns
			4.5	16		20		24		
			6	14		17		20		
		$\overline{SRCLR}$ low	2	80		100		120		
			4.5	16		20		24		
			6	14		17		20		
t_{SU}	Setup time	SER before SRCLK ↑	2	100		125		150		ns
			4.5	20		25		30		
			6	17		21		25		
		SRCLK ↑ before RCLK ↑ (1)	2	75		94		113		
			4.5	15		19		23		
			6	13		16		19		
		$\overline{SRCLR}$ low before RCLK ↑	2	50		65		75		
			4.5	10		13		15		
			6	9		11		13		
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑	2	50		60		75		
			4.5	10		12		15		
			6	9		11		13		
t_h	Hold time, SER after SRCLK ↑		2	0		0		0		ns
			4.5	0		0		0		
			6	0		0		0		

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



NOTE: ▨ implies that the output is in 3-State mode.

Timing Diagram

5.6 Switching Characteristics

over operating free-air temperature range, C_L = 50pF (unless otherwise noted) (Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A=-40°C to 85°C		T_A = -55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2	6	26		5		4.2		MHz
			4.5	31	38		25		21		
			6	36	42		29		25		
t_{pd}	SRCLK	$Q_{H'}$	2		50	160		200		240	ns
			4.5		17	32		40		48	
			6		14	27		34		41	
	RCLK	Q_A-Q_H	2		50	150		187		225	
			4.5		17	30		37		45	
			6		14	26		32		38	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2		51	175		219		261	ns
			4.5		18	35		44		52	
			6		15	30		37		44	
t_{en}	$\overline{OE}$	Q_A-Q_H	2		40	150		187		225	ns
			4.5		15	30		37		45	
			6		13	26		32		38	
t_{dis}	$\overline{OE}$	Q_A-Q_H	2		42	200		250		300	ns
			4.5		23	40		50		60	
			6		20	34		43		51	
t_t		Q_A-Q_H	2		28	60		75		90	ns
			4.5		8	12		15		18	
			6		6	10		13		15	
		$Q_{H'}$	2		28	75		95		110	
			4.5		8	15		19		22	
			6		6	13		16		19	

5.6 Switching Characteristics

over operating free-air temperature range, C_L = 150pF (unless otherwise noted) (Figure 6)

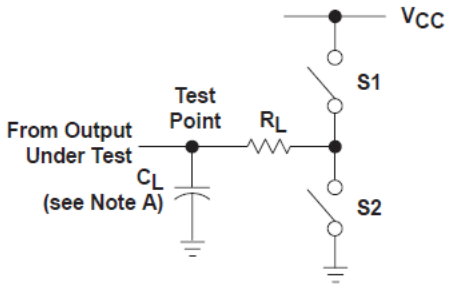
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A=-40°C to 85°C		T_A = -55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{pd}	RCLK	Q_A-Q_H	2		60	200		250		300	MHz
			4.5		22	40		50		60	
			6		19	34		43		51	
t_{en}	$\overline{OE}$	Q_A-$Q_{H'}$	2		70	200		250		298	ns
			4.5		2340	40		50		60	
			6		19	34		43		51	
t_t		Q_A-Q_H	2		45	210		265		315	ns
			4.5		17	42		53		63	
			6		13	36		45		53	

5.7 Operating Characteristics

T_A = 25°C

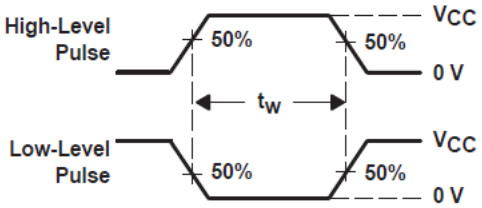
		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

6 Parameter Measurement Information

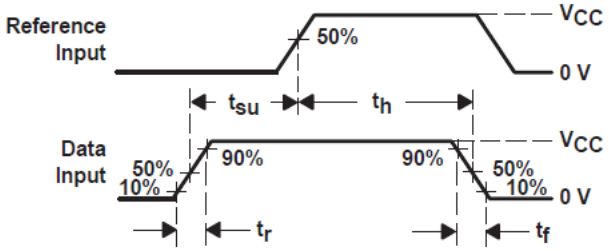


LOAD CIRCUIT

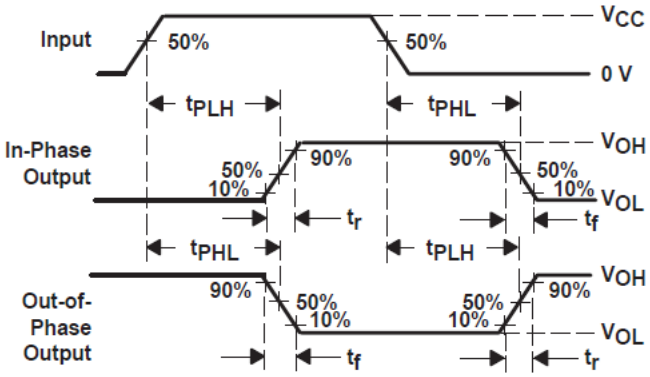
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



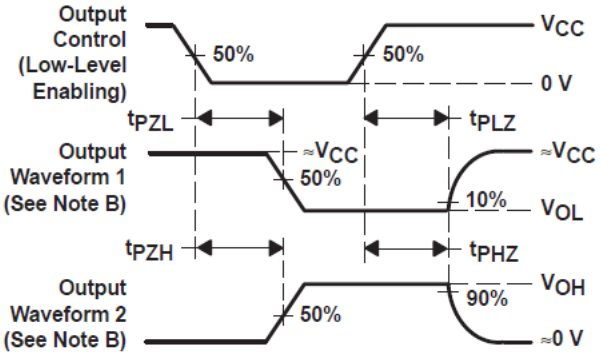
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

図 6-1. Load Curcuit and Voltage Waveforms

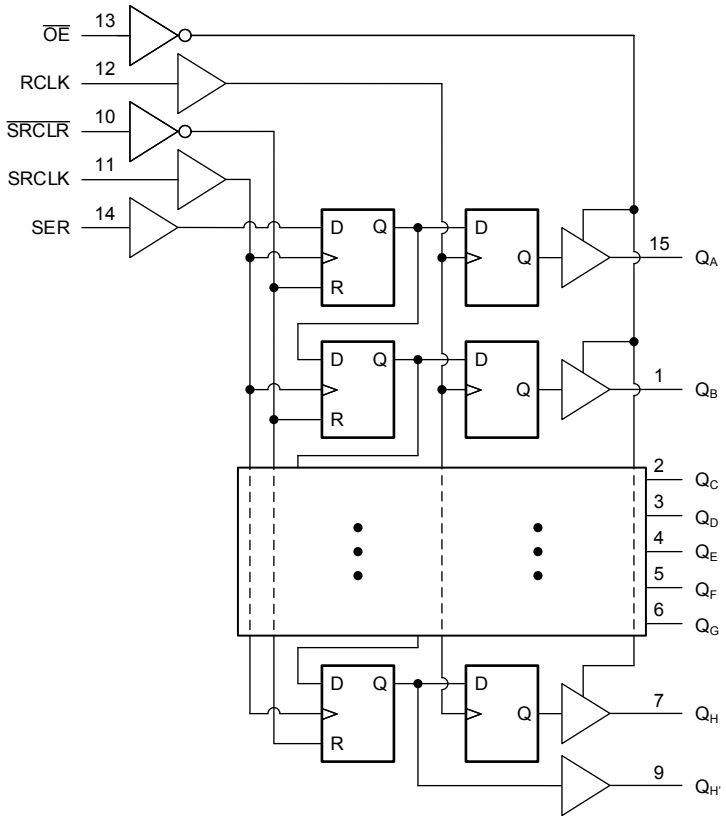
7 Detailed Description

7.1 Overview

The CD74HC595 device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial output for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1 lists the functional modes of the CD74HC595.

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC595DW	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	-55 to 125	HC595M
CD74HC595DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC595E
CD74HC595E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC595E
CD74HC595M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC595M
CD74HC595M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595M96G4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC595M
CD74HC595NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC595M
CD74HC595SM96	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ595
CD74HC595SM96.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ595

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

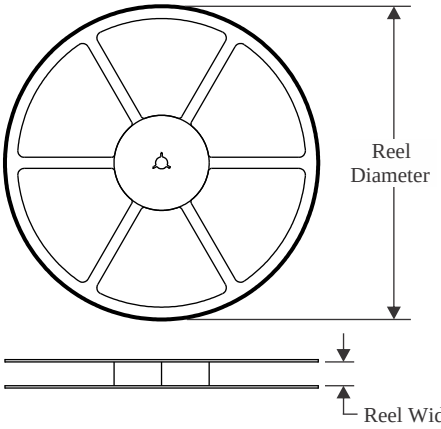
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

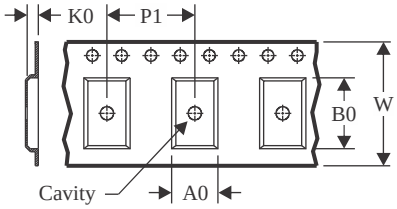
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

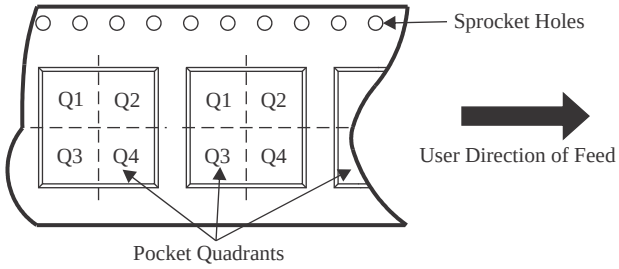


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

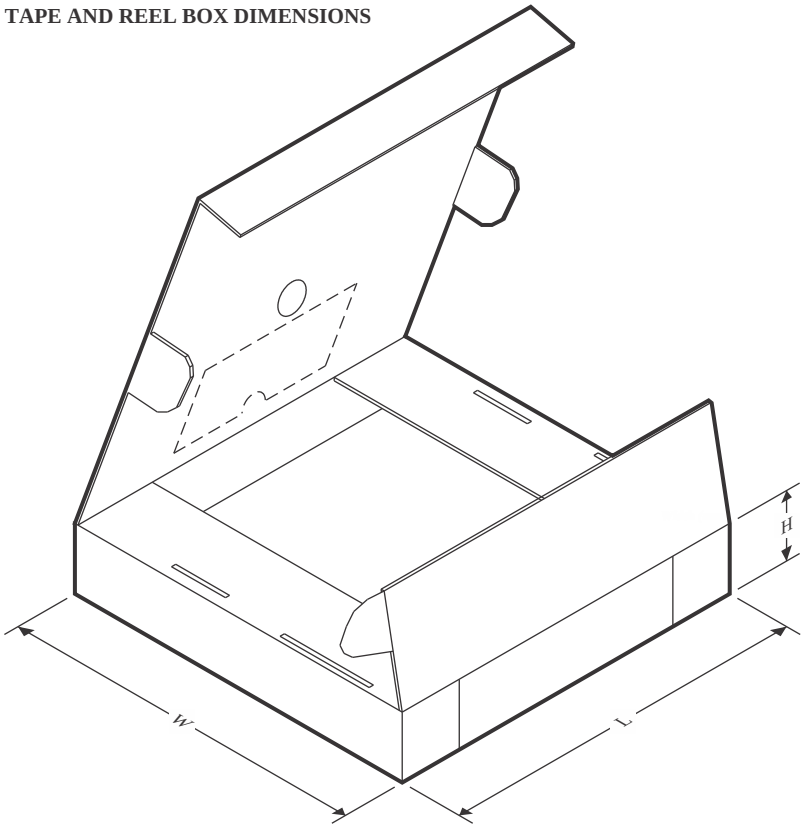
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC595DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD74HC595M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC595M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC595NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC595SM96	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

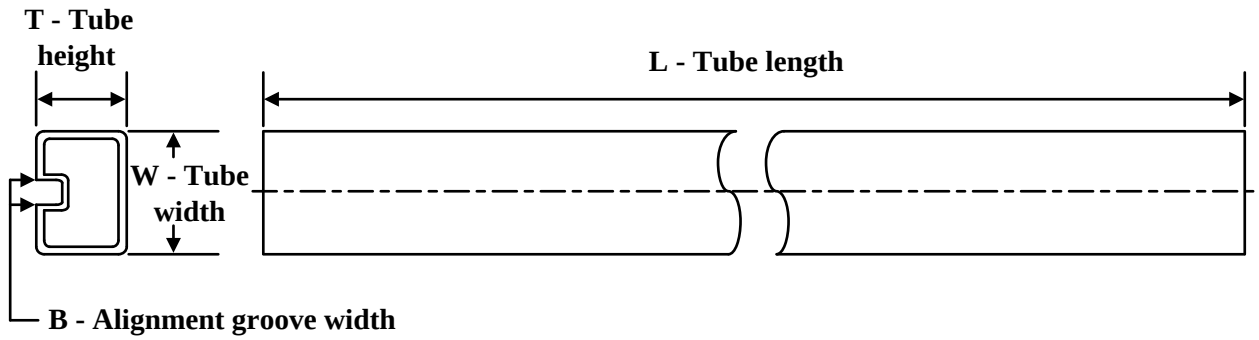
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

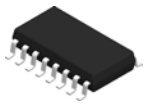
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC595DWR	SOIC	DW	16	2000	350.0	350.0	43.0
CD74HC595M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC595M96G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC595NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC595SM96	SSOP	DB	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC595E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC595E.A	N	PDIP	16	25	506	13.97	11230	4.32

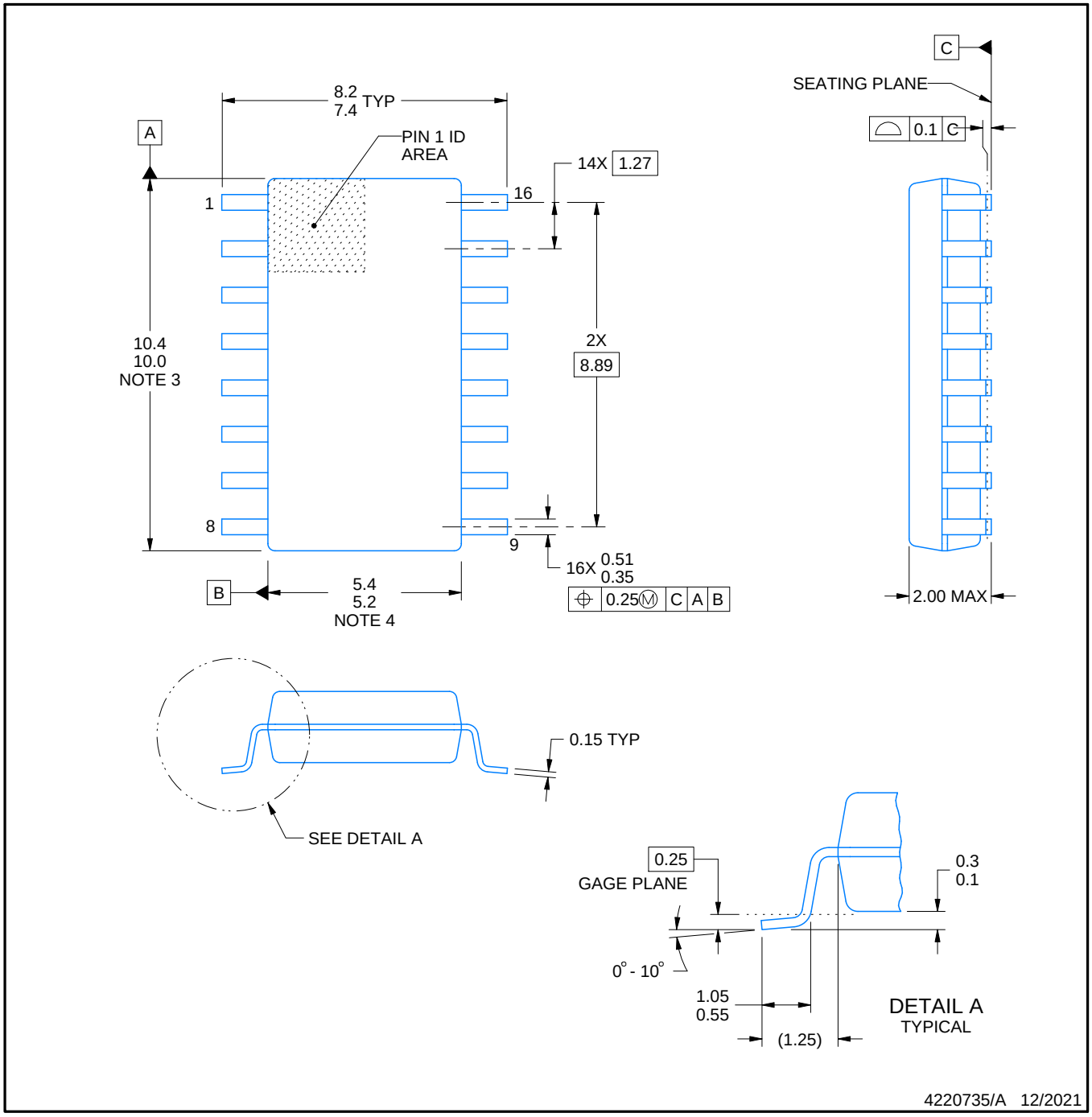


PACKAGE OUTLINE

NS0016A

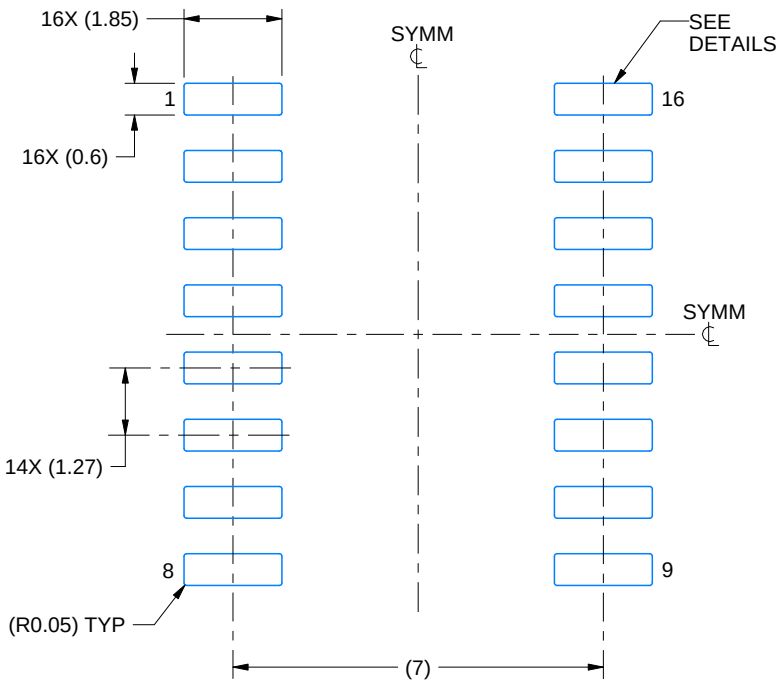
SOP - 2.00 mm max height

SOP

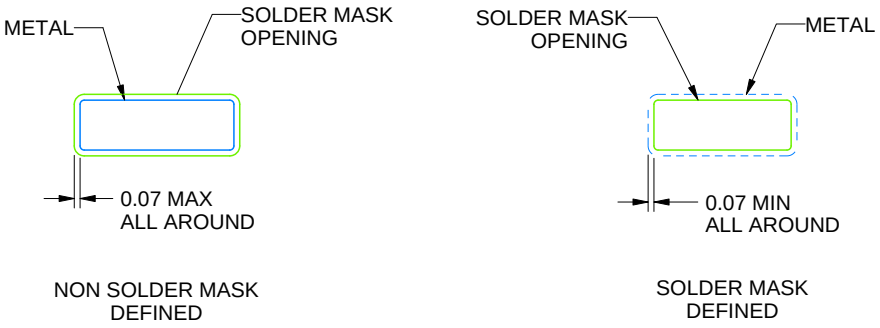


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

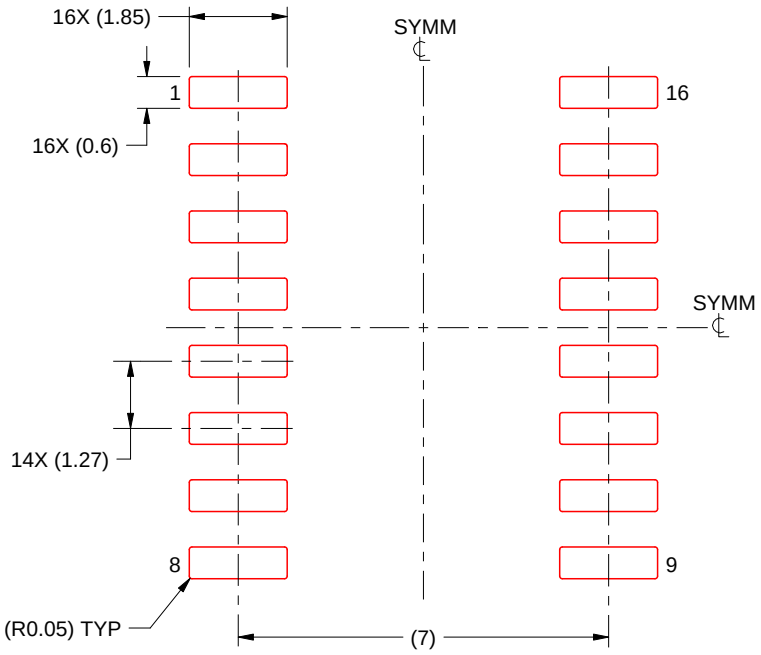
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



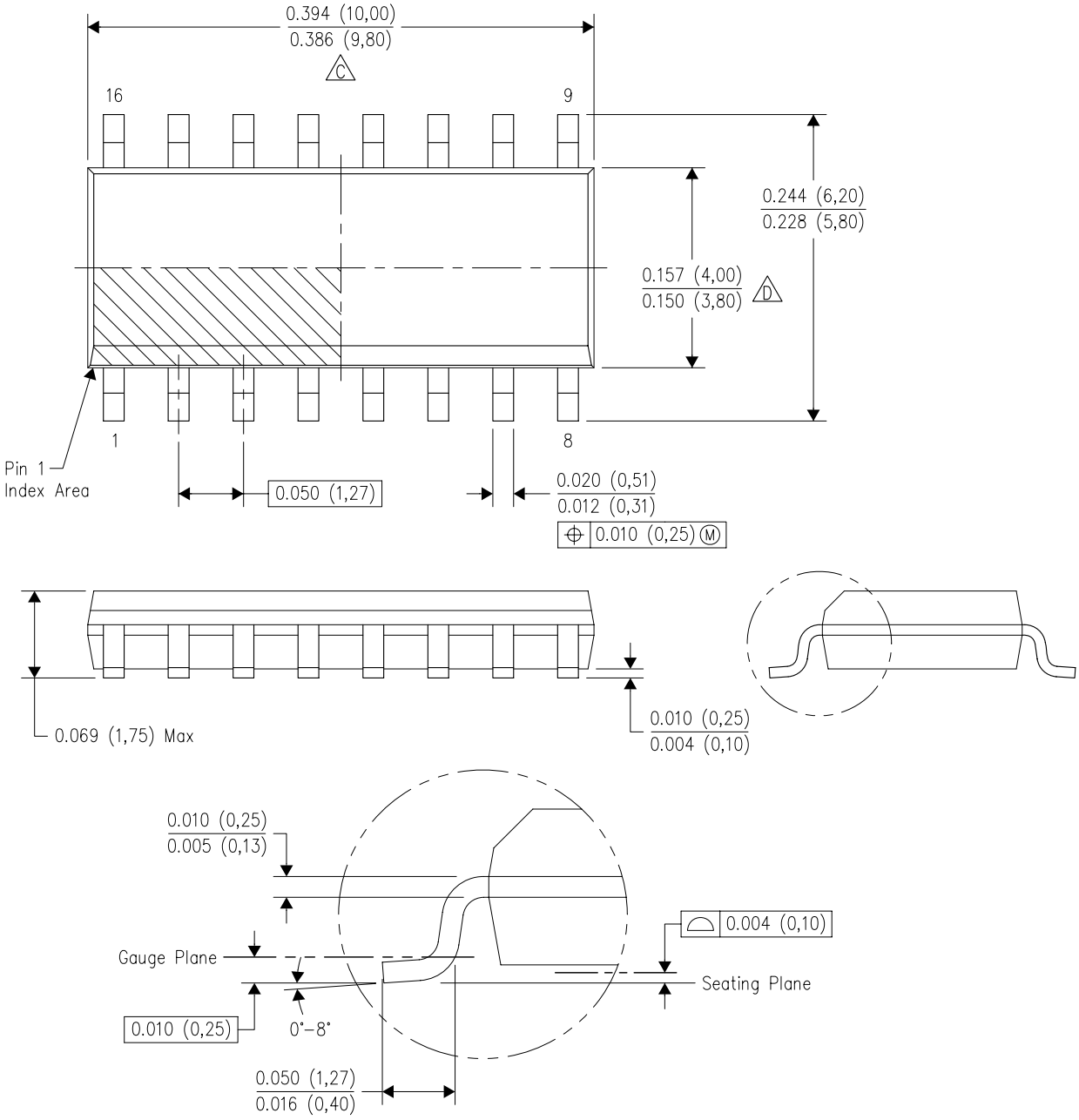
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



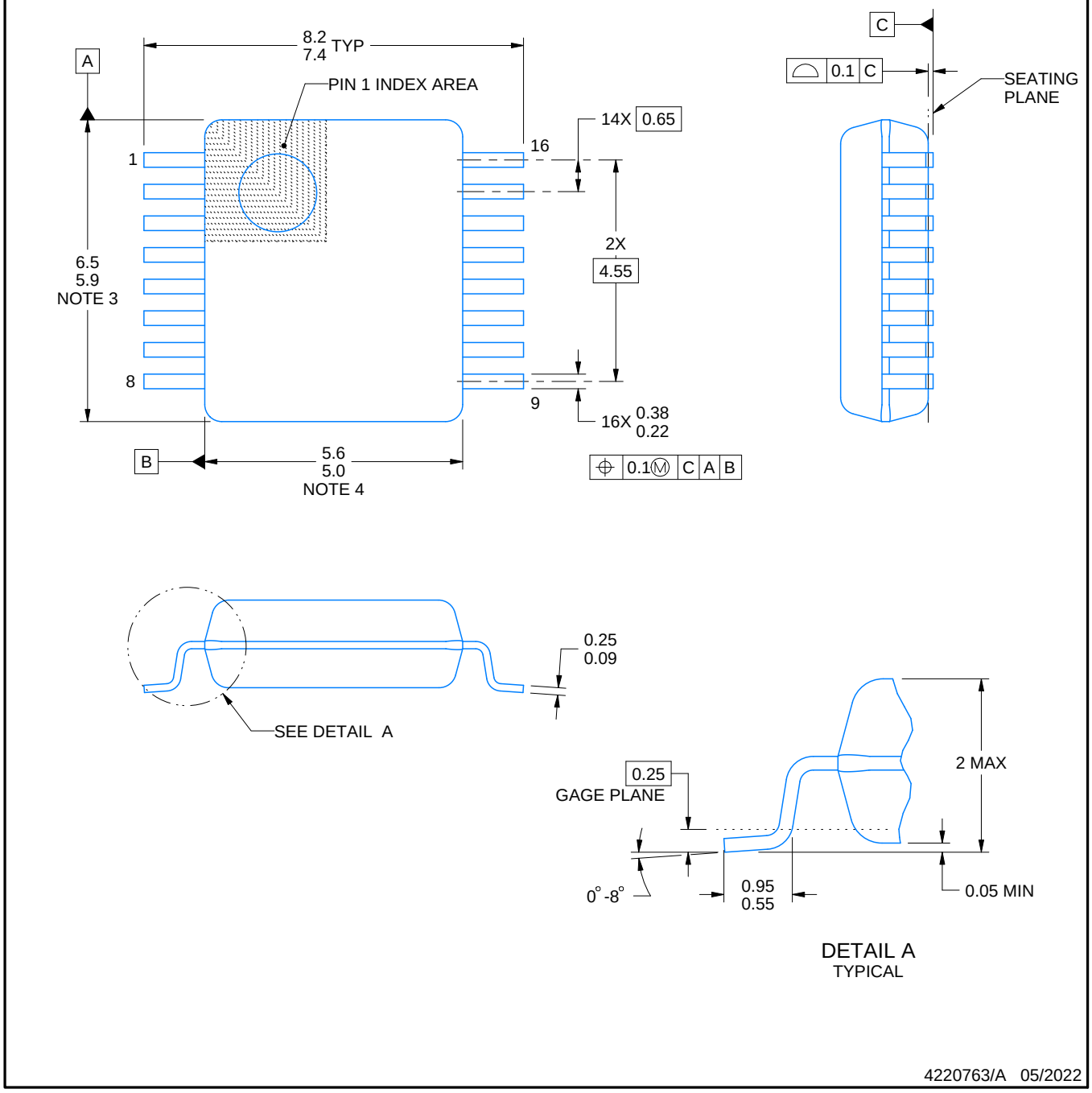
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

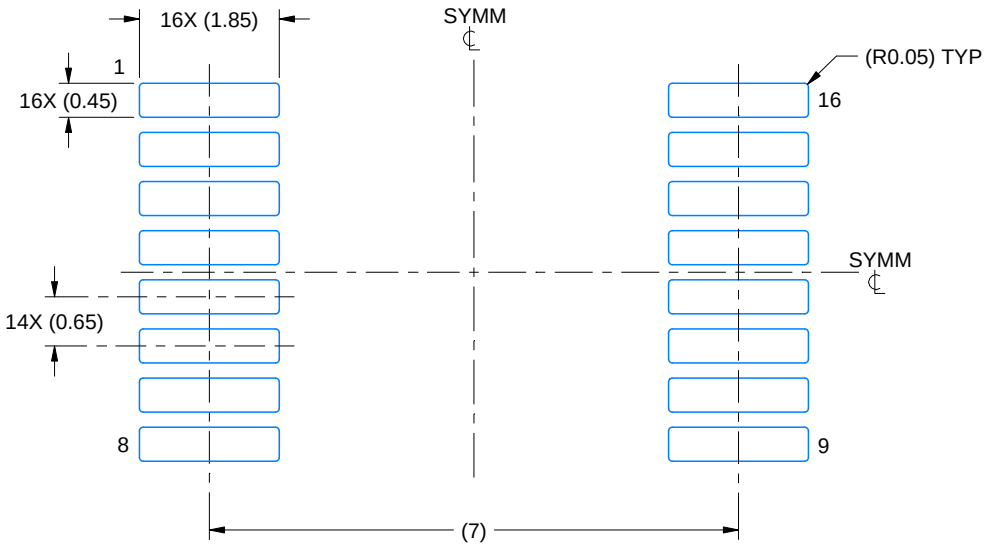
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

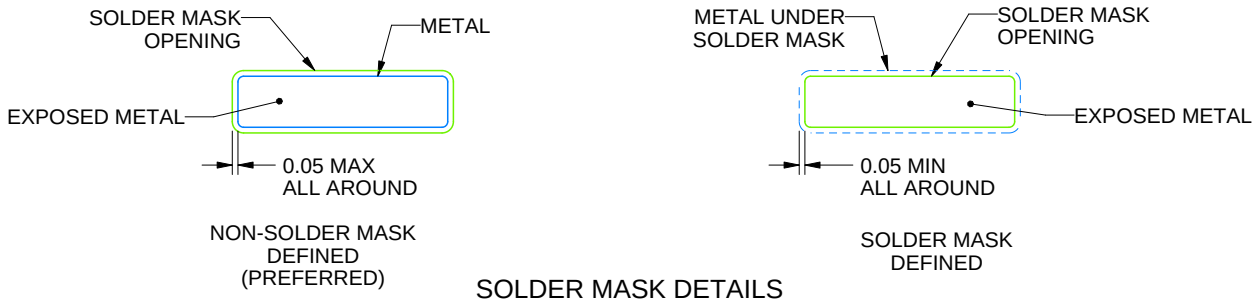


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

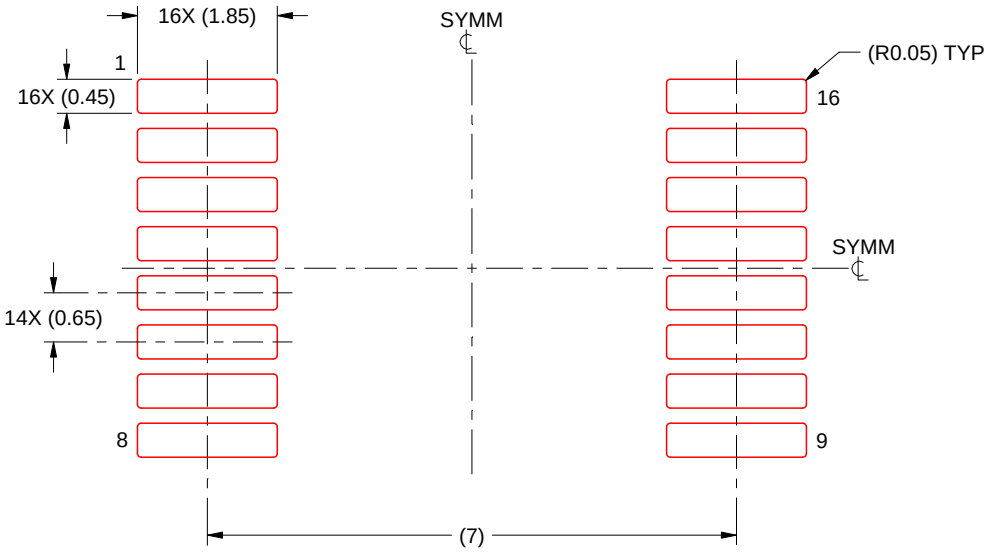


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

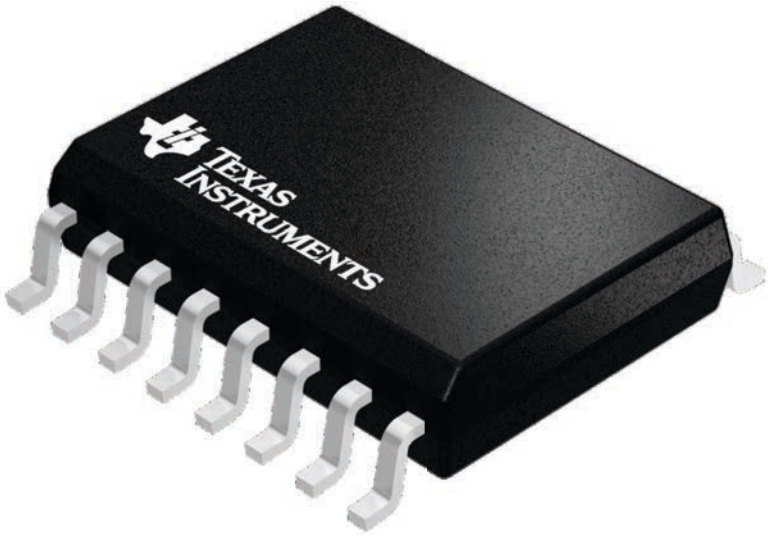
DW 16

SOIC - 2.65 mm max height

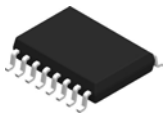
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

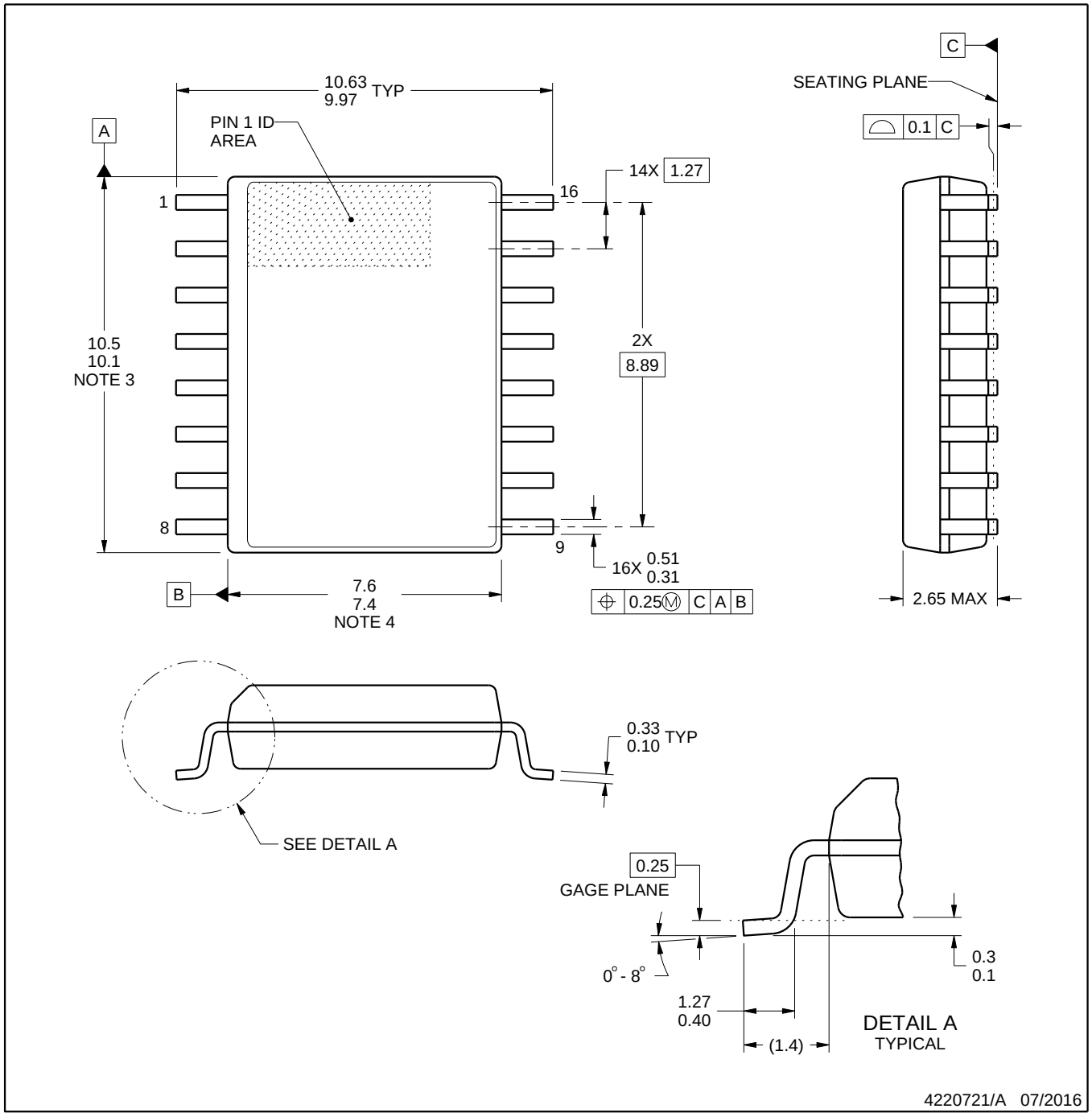


PACKAGE OUTLINE

DW0016A

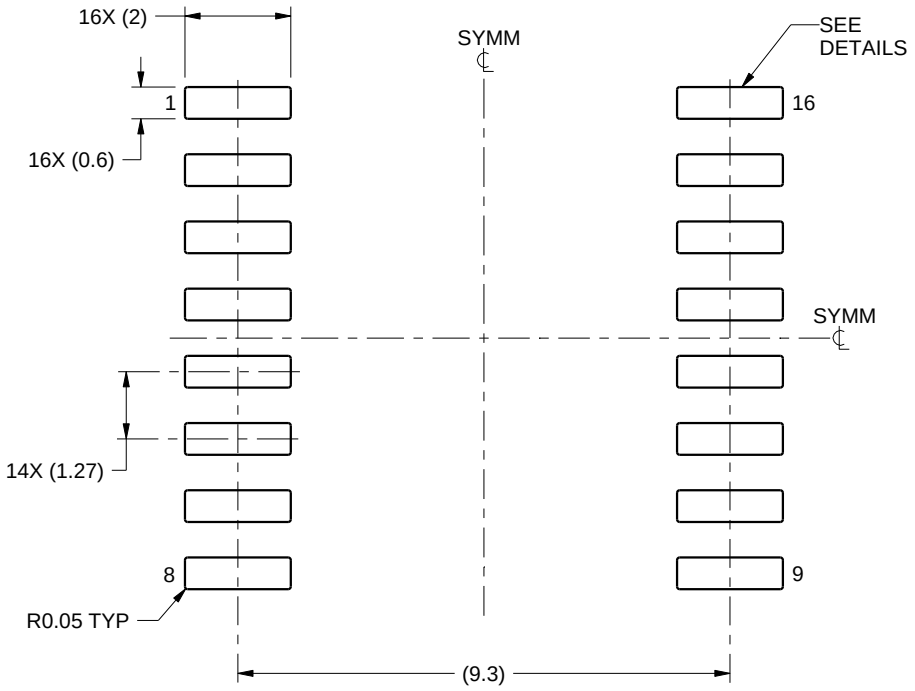
SOIC - 2.65 mm max height

SOIC

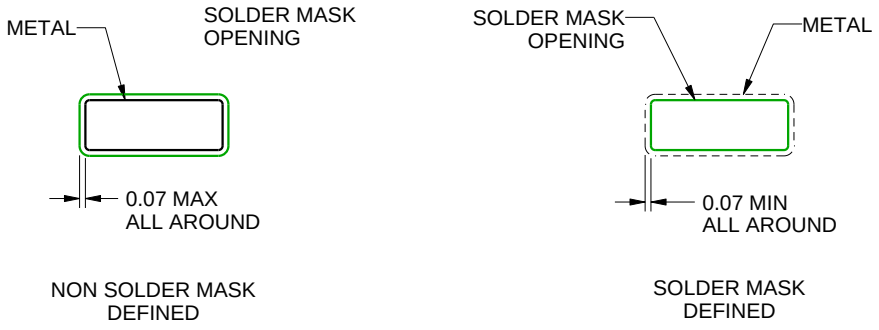


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

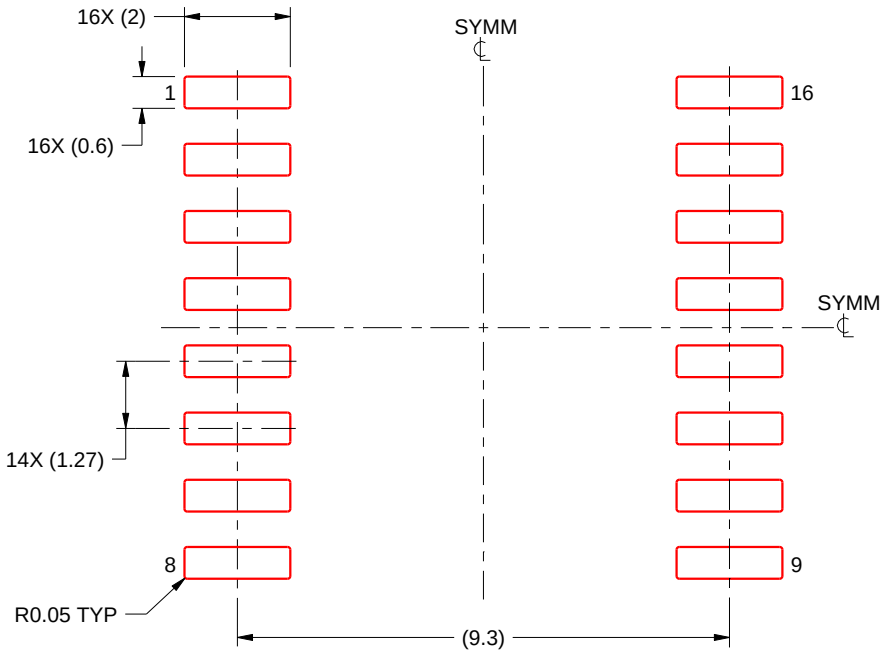


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

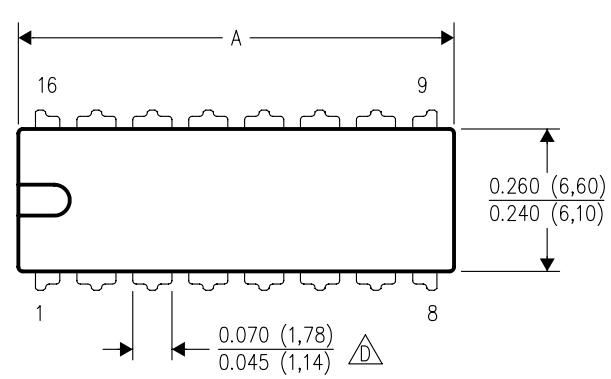
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

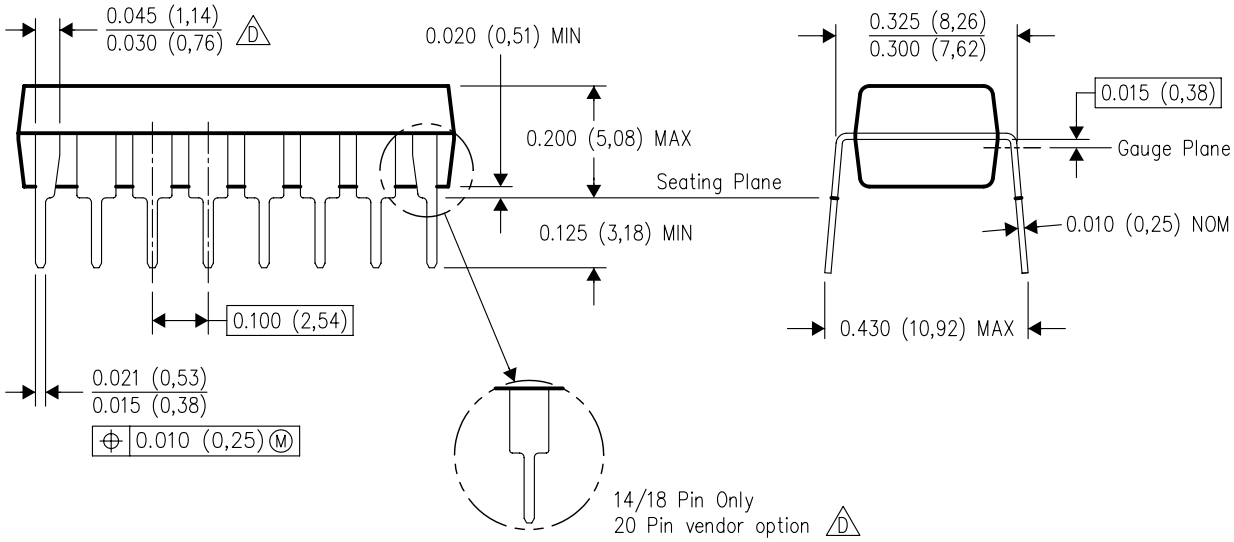
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日：2025 年 10 月