TEXAS INSTRUMENTS
CD54HC251, CD74HC251, CD54HCT251, CD74HCT251
JAJSOA6D – NOVEMBER 1998 – REVISED MARCH 2022

# CDx4HC251、CDx4HCT251 ハイスピード CMOS ロジック、8 入力マルチプレクサ、スリー・ステート

## 1 特長

- 8 つのバイナリ・データ入力のいずれかを選択
- スリー・ステート出力能力
- 真および補数出力
- 14ns の伝搬遅延 (出力データ標準値、$V_{CC}$ = 5V、$C_L$ = 15pF、$T_A$ = 25℃)
- ファンアウト (全温度範囲にわたって)
  - 標準出力:10 の LSTTL 負荷
  - バス・ドライバ出力:15 の LSTTL 負荷
- 広い動作温度範囲:– 55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- Philips 社製品を代替
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:$V_{cc}$ の $N_{IL}$ = 30%、$N_{IH}$ = 30% ($V_{CC}$ = 5V 時)
- HCT タイプ
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、$V_{IL}$ = 0.8V (最大値)、$V_{IH}$ = 2V (最小値)
  - CMOS 入力互換、$V_{OL}$、$V_{OH}$ で $I_I \leq 1\mu A$

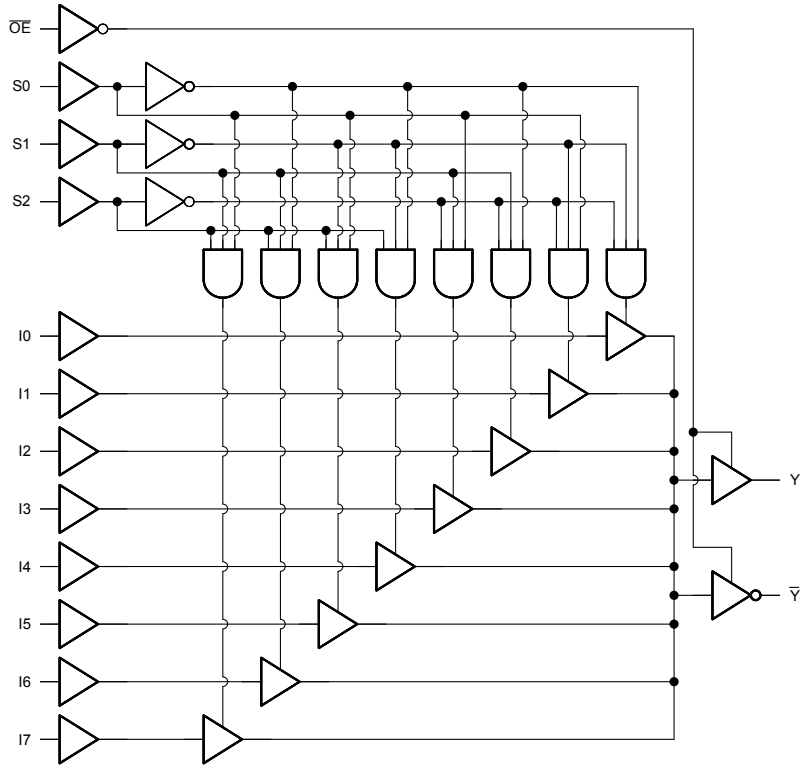
## 2 説明

HC251 および HCT251 は、スリー・ステート出力を備えた 8 チャネルのデジタル・マルチプレクサで、高速シリコンゲート CMOS テクノロジーを使用して製造されています。標準 CMOS IC の低消費電力と、10 個の LSTTL 負荷に耐える駆動能力とを合わせ持っています。スリー・ステート機能を備えているため、バス指向システムでのバス・ラインとのインターフェイスに最適です。

**デバイス情報**

| 部品番号 | パッケージ(1) | 本体サイズ (公称) |
|---|---|---|
| CD54HC251F | CDIP (16) | 24.38mm × 6.92mm |
| CD54HCT251F | CDIP (16) | 24.38mm × 6.92mm |
| CD74HC251M | SOIC (16) | 9.90mm × 3.90mm |
| CD74HCT251M | SOIC (16) | 9.90mm × 3.90mm |
| CD74HC251E | PDIP (16) | 19.31mm × 6.35mm |
| CD74HCT251E | PDIP (16) | 19.31mm × 6.35mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**機能ブロック図**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# Table of Contents

**1 特長** ... 1
**2 説明** ... 1
**3 Revision History** ... 2
**4 Pin Configuration and Functions** ... 3
**5 Specifications** ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 Recommended Operating Conditions(1) ... 4
5.3 Thermal Information ... 4
5.4 Electrical Characteristics ... 5
5.5 Switching Characteristics ... 6
**6 Parameter Measurement Information** ... 7
**7 Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Device Functional Modes ... 10
**8 Power Supply Recommendations** ... 11
**9 Layout** ... 11
9.1 Layout Guidelines ... 11
**10 Device and Documentation Support** ... 12
10.1 Documentation Support ... 12
10.2 Receiving Notification of Documentation Updates ... 12
10.3 サポート・リソース ... 12
10.4 Trademarks ... 12
10.5 Electrostatic Discharge Caution ... 12
10.6 Glossary ... 12
**11 Mechanical, Packaging, and Orderable Information** ... 12

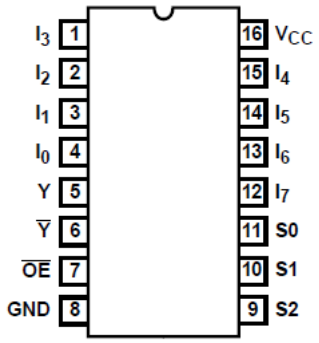
## 3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (October 2003) to Revision D (March 2022) | Page |
|---|---|
| • 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新 | 1 |


Copyright © 2022 Texas Instruments Incorporated

## 4 Pin Configuration and Functions




**J, N, or D Package**
**16-Pin CDIP, PDIP, or SOIC**
**Top View**

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $I_{IK}$ | Input diode current(2) | $V_I < 0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_{OK}$ | Output diode current(2) | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_O$ | Drain current, per output | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | | ±25 | mA |
| $I_O$ | Output source or sing current per output pin | $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |
| | Lead temperature (Soldering 10s) (SOIC - lead tips only) | | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 Recommended Operating Conditions(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | HC Types | 2 | 6 | V |
| | | HCT Types | 4.5 | 5.5 | V |
| $V_I$, $V_O$ | DC input or output voltage | | 0 | $V_{CC}$ | V |
| $t_t$ | Input rise and fall time | 2 V | | 1000 | ns |
| | | 4.5 V | | 500 | |
| | | 6 V | | 400 | |
| $T_A$ | Temperature range | | – 55 | 125 | ℃ |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

## 5.3 Thermal Information

| THERMAL METRIC | | D (SOIC) 16 PINS | N (PDIP) 16 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1) | 67 | 73 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.


Copyright © 2022 Texas Instruments Incorporated

## 5.4 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS[1] | $V_{CC}$ (V) | 25°C | | | –40°C to 85°C | | –55°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2 | 1.5 | | | 1.5 | | 1.5 | | V |
| | | | 4.5 | 3.15 | | | 3.15 | | 3.15 | | V |
| | | | 6 | 4.2 | | | 4.2 | | 4.2 | | V |
| $V_{IL}$ | Low-level input voltage | | 2 | | | 0.5 | | 0.5 | | 0.5 | V |
| | | | 4.5 | | | 1.35 | | 1.35 | | 1.35 | V |
| | | | 6 | | | 1.8 | | 1.8 | | 1.8 | V |
| $V_{OH}$ | High-level output voltage CMOS loads | $I_{OH}$ = – 20μA | 2 | 1.9 | | | 1.9 | | 1.9 | | V |
| | | $I_{OH}$ = – 20μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = – 20μA | 6 | 5.9 | | | 5.9 | | 5.9 | | V |
| | High-level output voltage TTL loads | $I_{OH}$ = – 6mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | V |
| | | $I_{OH}$ = – 7.8mA | 6 | 5.48 | | | 5.34 | | 5.2 | | V |
| $V_{OL}$ | Low-level output voltage CMOS loads | $I_{OL}$ = 20μA | 2 | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 20μA | 4.5 | | | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 20μA | 6 | | | 0.1 | | 0.1 | | 0.1 | V |
| | Low-level output voltage TTL loads | $I_{OL}$ = 6mA | 4.5 | | | 0.26 | | 0.33 | | 0.4 | V |
| | | $I_{OL}$ = 7.8mA | 6 | | | 0.26 | | 0.33 | | 0.4 | V |
| $I_I$ | Input leakage current | $V_{CC}$ or GND | 6 | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | Supply current | $V_{CC}$ or GND | 6 | | | 8 | | 80 | | 160 | μA |
| $I_{OZ}$ | Three-state leakage current | | 6 | | | ±0.5 | | ±0.5 | | ±10 | μA |
| **HCT TYPES** | | | | | | | | | | | |
| $V_{IH}$ | High-level input voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage CMOS loads | $I_{OH}$ = – 20μA | 4.5 | 4.4 | | | 4.4 | | 4.4 | | V |
| | High-level output voltage TTL loads | $I_{OH}$ = – 6mA | 4.5 | 3.98 | | | 3.84 | | 3.7 | | V |
| $V_{OL}$ | Low-level output voltage CMOS loads | $I_{OL}$ = 20μA | 4.5 | | | 0.1 | | 0.1 | | 0.1 | V |
| | Low-level output voltage TTL loads | $I_{OL}$ = 6mA | 4.5 | | | 0.26 | | 0.33 | | 0.4 | V |
| $I_I$ | Input leakage current | $V_{CC}$ and GND | 5.5 | | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | Supply Current | $V_{CC}$ and GND | 5.5 | | | 8 | | 80 | | 160 | μA |
| $I_{OZ}$ | Three-state leakage current | | 6 | | | ±0.5 | | ±5.0 | | ±10 | μA |
| $\Delta I_{CC}$ [2] [3] | Additional supply current per input pin | S0, S1, S2 | 4.5 to 5.5 | | 55 | 198 | | 247.5 | | 269.5 | μA |
| | | I0 - I7 | 4.5 to 5.5 | | 50 | 180 | | 225 | | 245 | μA |
| | | $\overline{OE}$ | 4.5 to 5.5 | | 265 | 954 | | 1192.5 | | 1298.5 | μA |

(1) $V_I = V_{IH}$ or $V_{IL}$, unless otherwise noted.
(2) For dual-supply systems theoretical worst case ($V_I$ = 2.4 V, $V_{CC}$ = 5.5 V) specification is 1.8 mA..
(3) Inputs held at $V_{CC}$ – 2.1.

Copyright © 2022 Texas Instruments Incorporated

## 5.5 Switching Characteristics

Input $t_t$ = 6ns. Unless otherwise specified, $C_L$ = 50pF

| PARAMETER | | $V_{CC}$ (V) | 25°C | | -40°C to 85°C | -55°C to 125°C | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | MAX | MAX | |
| **HC TYPES** | | | | | | | |
| $t_{pd}$ | Select to outputs | 2 | | 245 | 305 | 370 | ns |
| | | 4.5 | 21(1) | 49 | 61 | 74 | |
| | | 6 | | 42 | 52 | 63 | |
| $t_{pd}$ | Data to outputs | 2 | | 175 | 220 | 265 | ns |
| | | 4.5 | 12(1) | 35 | 44 | 53 | |
| | | 6 | | 30 | 37 | 45 | |
| $t_{pd}$ | Enable to high Z and enable from high Z | 2 | | 140 | 175 | 210 | ns |
| | | 4.5 | 11(1) | 28 | 35 | 42 | |
| | | 6 | | 24 | 30 | 36 | |
| $t_t$ | Output transition times | 2 | | 75 | 95 | 110 | ns |
| | | 4.5 | | 15 | 19 | 22 | |
| | | 6 | | 13 | 16 | 19 | |
| $C_i$ | Input capacitance | | | 10 | 10 | 10 | pF |
| $C_O$ | Three-state output capacitance | | | 15 | 15 | 15 | pF |
| $C_{pd}$ (3) (4) | Power dissipation capacitance | 5 | 60(2) | | | | pF |
| **HCT TYPES** | | | | | | | |
| $t_{pd}$ | Select to outputs | 4.5 | 18(1) | 42 | 53 | 63 | ns |
| $t_{pd}$ | Data to outputs | 4.5 | 12(1) | 35 | 44 | 53 | ns |
| $t_{pd}$ | Enable to high Z and enable from high Z | 4.5 | 12(1) | 30 | 38 | 45 | ns |
| $t_t$ | Output transition times | 4.5 | | 15 | 19 | 22 | ns |
| $C_i$ | Input capacitance | | | 10 | 10 | 10 | pF |
| $C_{pd}$ (3) (4) | Power dissipation capacitance | 5 | 60(2) | | | | pF |

(1) Typical value tested at 5V, $C_L$ = 15pF.
(2) Typical value tested at 5V.
(3) $C_{PD}$ is used to determine the dynamic power consumption, per channel.
(4) $P_D = V_{CC}{}^2 f_i(C_{PD} + C_L)$ where $f_i$ = input frequency, $C_L$ = output load capacitance, $V_{CC}$ = supply voltage.

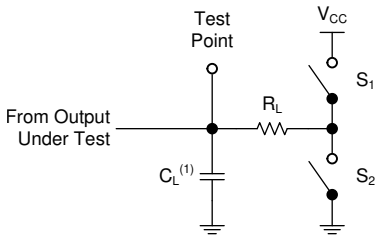

Copyright © 2022 Texas Instruments Incorporated

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.

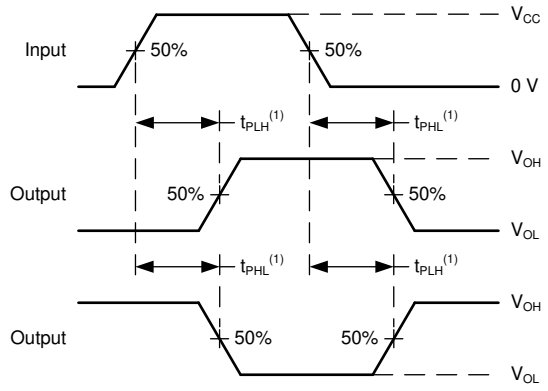
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



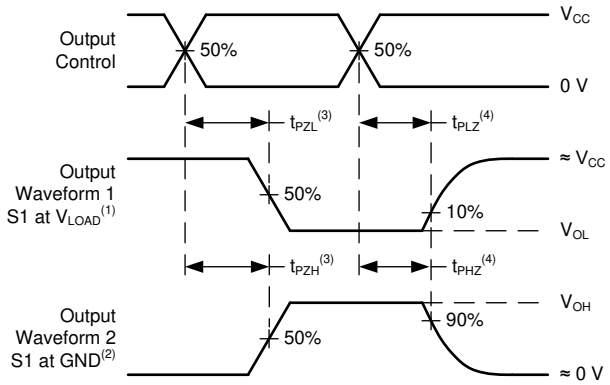

(1) $C_L$ includes probe and test-fixture capacitance.

**図 6-1. Load Circuit for 3-State Outputs**



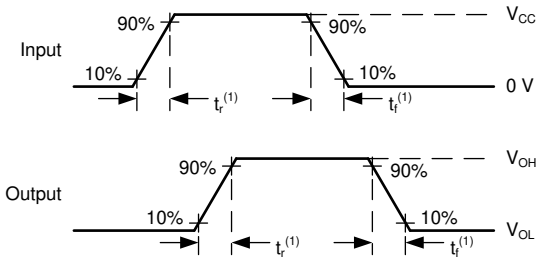

(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**




(1) $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
(2) $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

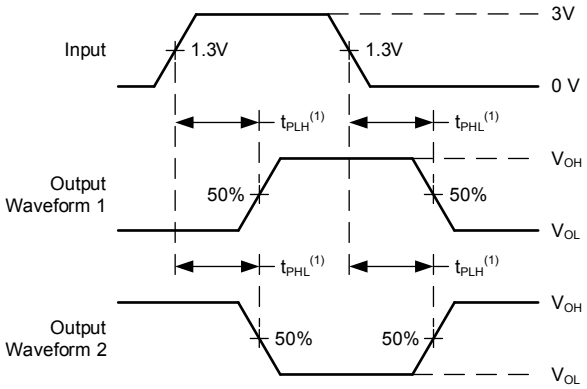
**図 6-3. Voltage Waveforms, Standard CMOS Inputs Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

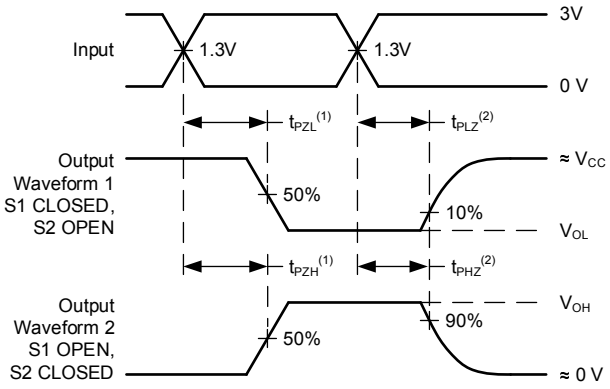
**図 6-4. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**

Copyright © 2022 Texas Instruments Incorporated




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**図 6-5. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**




(1) $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
(2) $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**図 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**


Copyright © 2022 Texas Instruments Incorporated

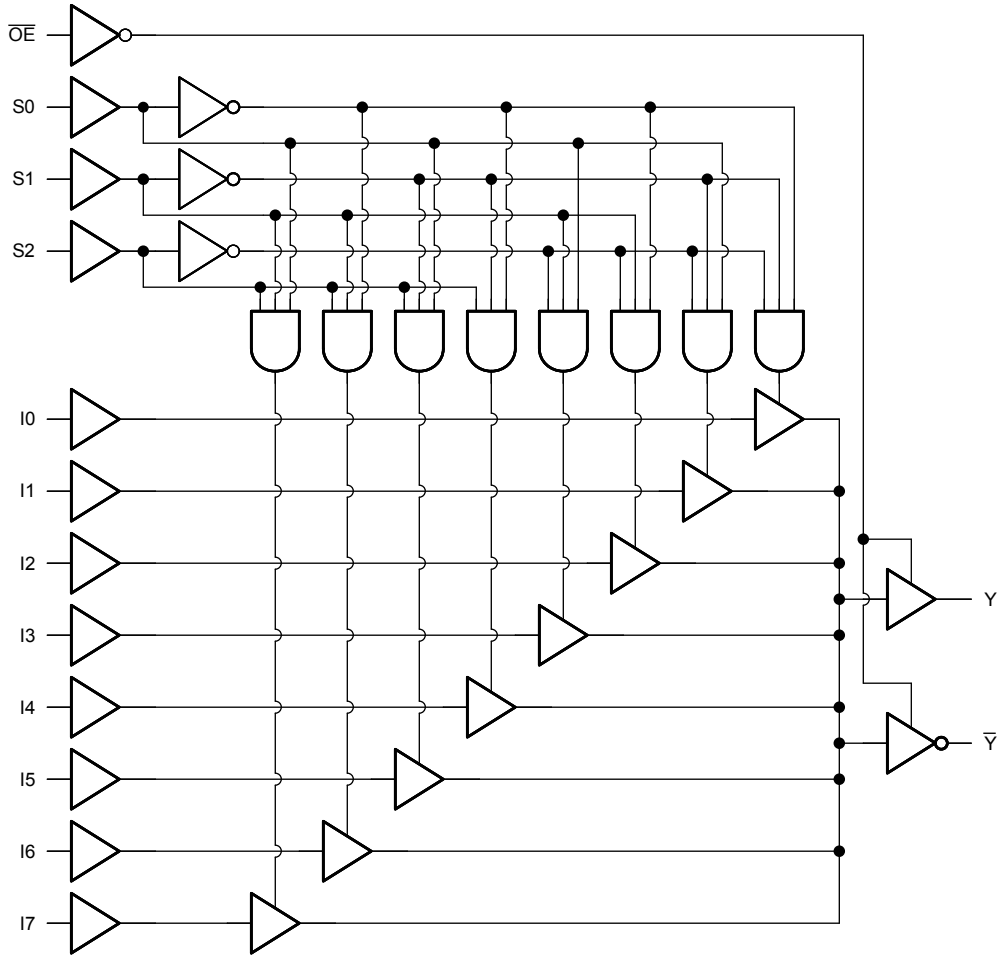
# 7 Detailed Description

## 7.1 Overview

The ’HC251 and ’HCT251 are 8-channel digital multiplexers with three-state outputs, fabricated with high-speed silicongate CMOS technology. Together with the low power consumption of standard CMOS integrated circuits, they possess the ability to drive 10 LSTTL loads. The three-state feature makes them ideally suited for interfacing with bus lines in a bus-oriented system.

This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an output enable ($\overline{OE}$) input. The $\overline{OE}$ must be at a low logic level to enable this device. When the $\overline{OE}$ input is high, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs. The ’HCT251 logic family is speed, function, and pin-compatible with the standard ’LS251.

## 7.2 Functional Block Diagram



## 7.3 Device Functional Modes

**表 7-1. Truth Table**(1)

| INPUTS | | | | OUTPUT | |
|---|---|---|---|---|---|
| SELECT | | | | | |
| S2 | S1 | S0 | OUTPUT CONTROL $\overline{OE}$ | Y | $\overline{Y}$ |
| X | X | X | H | Z | Z |
| L | L | L | L | $I_0$ | $\overline{I}_0$ |
| L | L | H | L | $I_1$ | $\overline{I}_1$ |
| L | H | L | L | $I_2$ | $\overline{I}_2$ |
| L | H | H | L | $I_3$ | $\overline{I}_3$ |
| H | L | L | L | $I_4$ | $\overline{I}_4$ |
| H | L | H | L | $I_5$ | $\overline{I}_5$ |
| H | H | L | L | $I_6$ | $\overline{I}_6$ |
| H | H | H | L | $I_7$ | $\overline{I}_7$ |

(1) H = High voltage level.
L = Low voltage level.
X = Dont care.
Z = High impedance (Off).
$I_0$, $I_1$… $I_7$ = The level of the respective input.


Copyright © 2022 Texas Instruments Incorporated

# 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

# 9 Layout

## 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

Copyright © 2022 Texas Instruments Incorporated

# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### 10.1.1 Related Documentation

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2022 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9052401MEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9052401MEA CD54HCT251F3A |
| CD54HC251F | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC251F |
| CD54HC251F.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | CD54HC251F |
| CD54HC251F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8512501EA CD54HC251F3A |
| CD54HC251F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8512501EA CD54HC251F3A |
| CD54HCT251F3A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9052401MEA CD54HCT251F3A |
| CD54HCT251F3A.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9052401MEA CD54HCT251F3A |
| CD74HC251E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC251E |
| CD74HC251E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HC251E |
| CD74HC251M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC251M |
| CD74HC251M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC251M |
| CD74HC251M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC251M |
| CD74HC251MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HC251M |
| CD74HCT251E | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT251E |
| CD74HCT251E.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -55 to 125 | CD74HCT251E |
| CD74HCT251M | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT251M |
| CD74HCT251M96 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HCT251M |
| CD74HCT251M96.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT251M |
| CD74HCT251M96G4 | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT251M |
| CD74HCT251M96G4.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT251M |
| CD74HCT251MT | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | -55 to 125 | HCT251M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC251, CD54HCT251, CD74HC251, CD74HCT251 :**

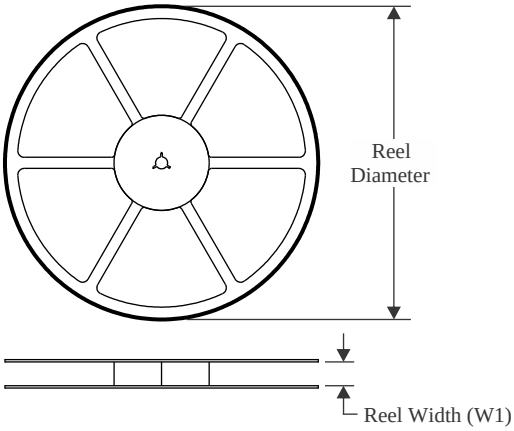
- Catalog : CD74HC251, CD74HCT251
- Military : CD54HC251, CD54HCT251

NOTE: Qualified Version Definitions:

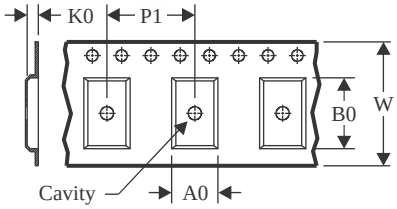
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

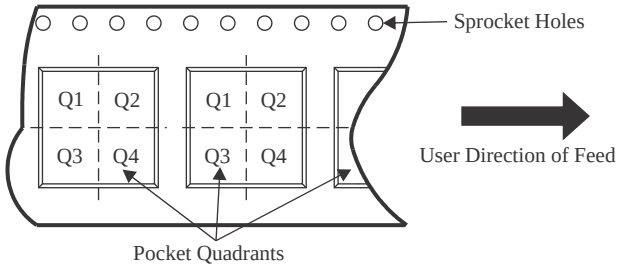



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

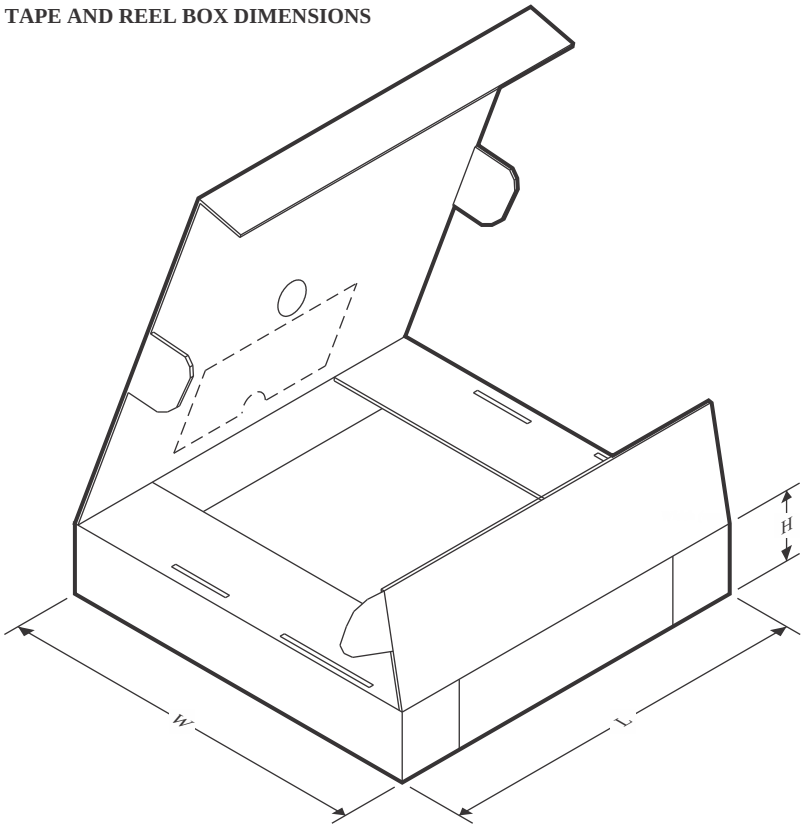
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC251M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT251M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT251M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

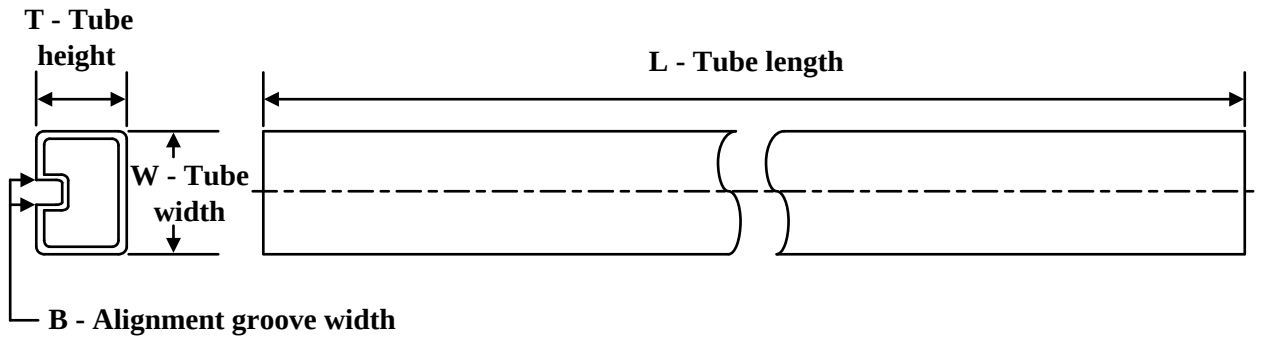
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC251M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HCT251M96 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| CD74HCT251M96G4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |

## TUBE



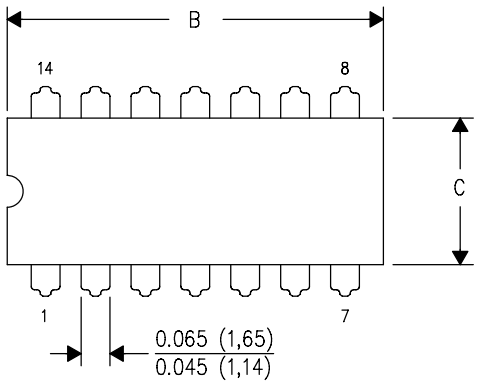

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC251E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC251E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC251E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC251E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT251E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT251E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT251E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT251E.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

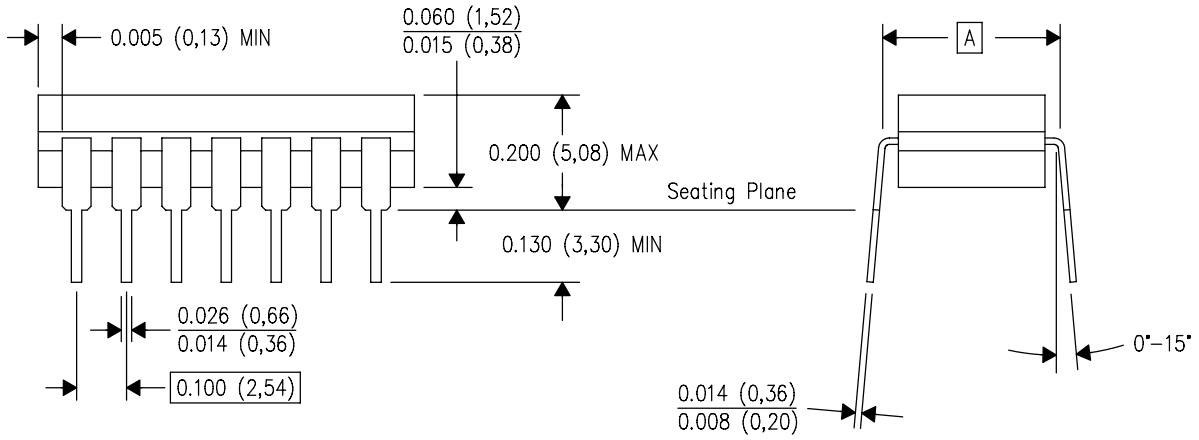
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



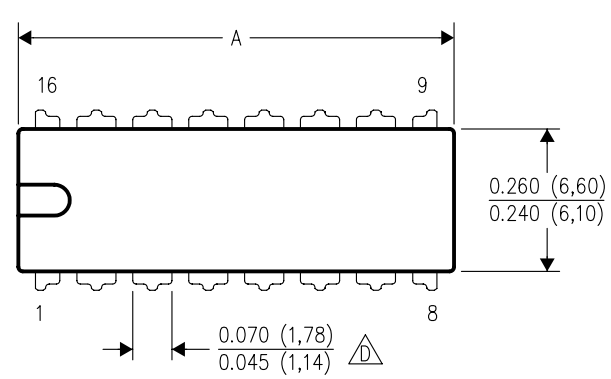

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

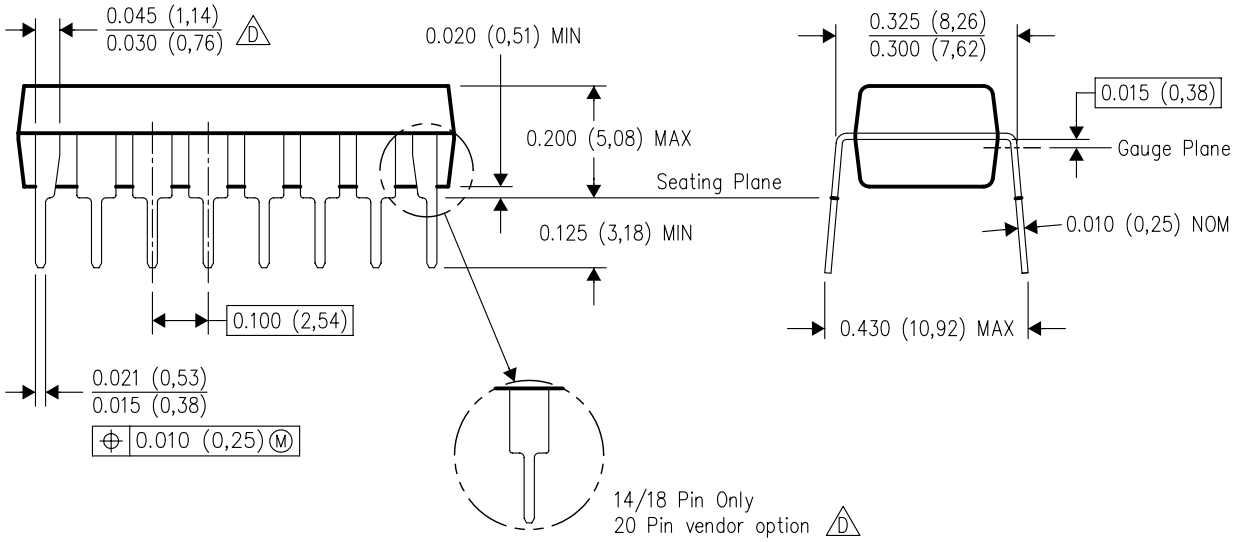
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



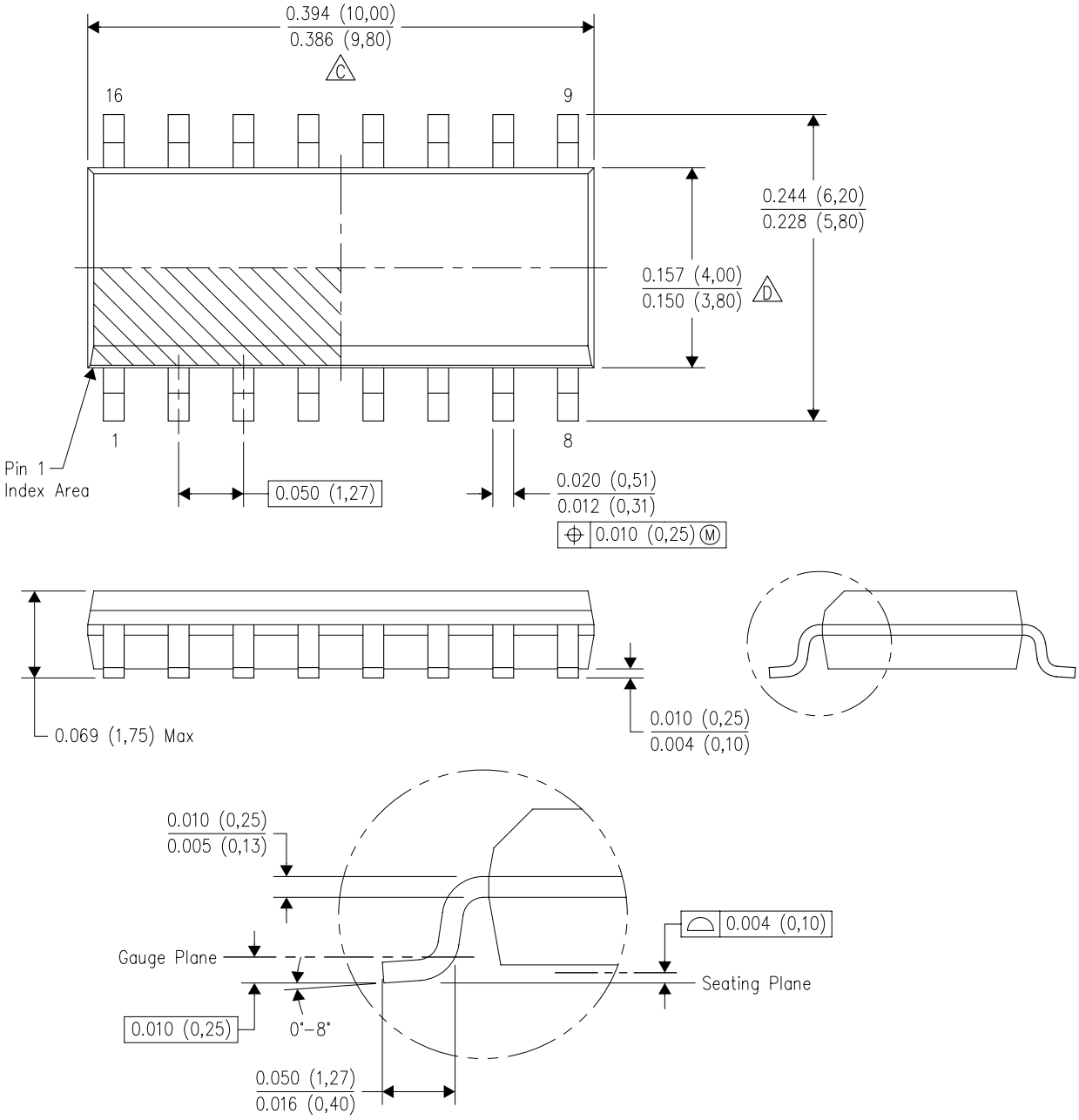

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月