

# DAC4390x-Q1 車載用スマート DAC、対数フェードイン・フェードアウトおよびシーケンシャル・ターン・アニメーション用、I<sup>2</sup>C、SPI、GPIO、PWM インターフェイス搭載

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み :
  - 温度グレード 1 : -40°C ~ +125°C、T<sub>A</sub>
- デジタル・ピンでのパルス幅変調 (PWM) 出力 (218Hz ~ 48.8kHz)
- 対数調光
- GPIO 制御による LED フェードイン・フェードアウト
- シーケンシャル方向指示器のアニメーション
- GPIO として構成されたプログラマブルなコンパレータと DAC
- I<sup>2</sup>C または SPI を自動検出
  - V<sub>IH</sub> : 1.62V (V<sub>DD</sub> = 5.5V の場合)
- VREF/MODE ピンにより、プログラミング・モードとスタンダアロン・モードを選択
- ユーザーがプログラム可能な不揮発性メモリ (NVM)
- 基準電圧として、内部、外部または電源を使用可能
- 幅広い動作範囲
  - 電源 : 1.8V ~ 5.5V
  - 温度範囲 : -40°C ~ +125°C
- 超小型パッケージ : 16 ピン WQFN (3mm × 3mm)

## 2 アプリケーション

- リア・ライト
- スモール・ライト
- 室内灯

## 3 概要

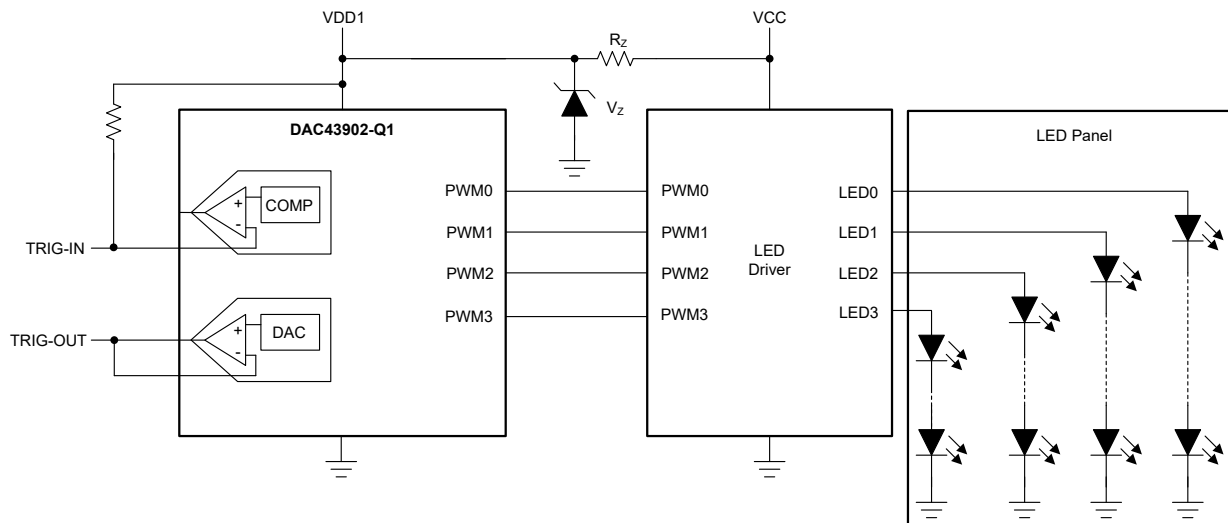
DAC43901-Q1 および DAC43902-Q1 (DAC4390x-Q1) は、デュアルおよびクワッド PWM 出力を備えた車載用 8 ビット・スマート D/A コンバータのファミリです。DAC43901-Q1 には 2 つの PWM 出力があり、DAC43902-Q1 には 4 つの PWM 出力があります。DAC チャンネルは、トリガ入力または出力としても機能します。DAC4390x-Q1 には、タイミングを構成可能な対数調光をロジックで生成する、構成済みの状態のマシンが搭載されています。PWM ベースの対数調光は、車内 / 車外照明の対数フェードイン / フェードアウト・アプリケーションに適用できます。DAC4390x-Q1 は、車載用方向指示器に適用できるシーケンシャル・アニメーションもサポートしています。これらのデバイスは、構成を保存するための NVM を提供します。このスマート DAC は、GPIO と NVM を使用するプロセッサを必要とせずに動作します (プロセッサレス動作)。

これらのデバイスは、I<sup>2</sup>C または SPI を自動的に検出し、内部基準電圧を備えています。小型パッケージと低消費電力を機能セットと組み合わせたスマート DAC は、車載照明アプリケーションの優れた選択肢です。

### 製品情報

部品番号	PWM 出力	パッケージ (1)
DAC43901-Q1	2	RTE (WQFN, 16)
DAC43902-Q1	4	

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



DAC43902-Q1 を使用したシーケンシャル方向指示器のアニメーション



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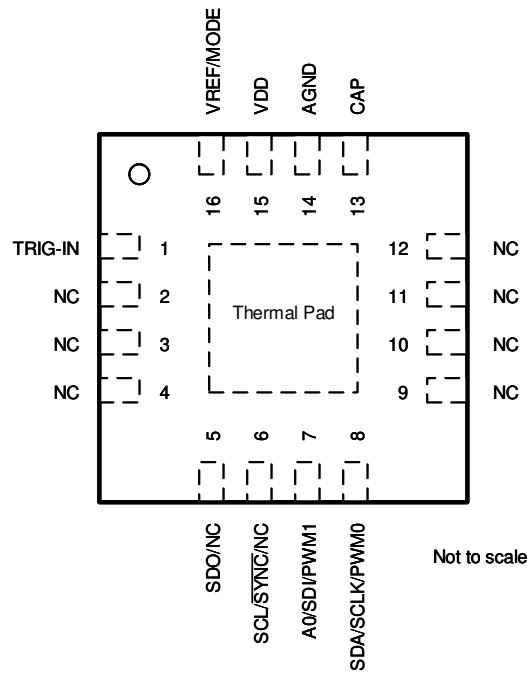
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## 4 Revision History

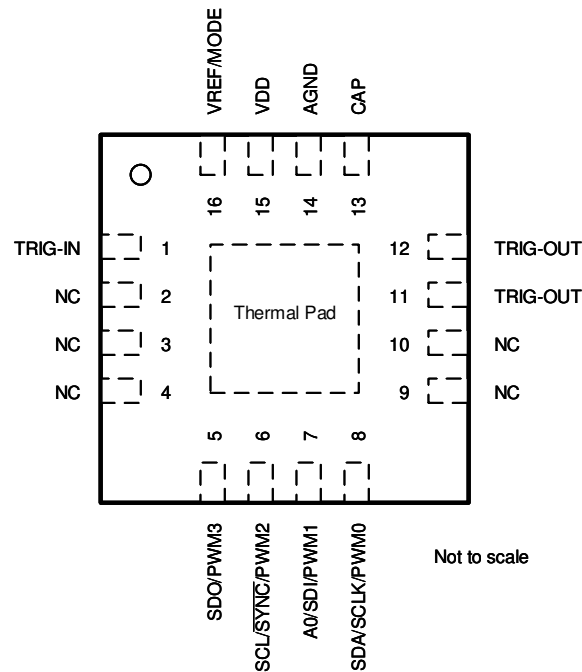
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2023	*	Initial release

## 5 Pin Configuration and Functions



**図 5-1. DAC43901-Q1: RTE Package, 16-pin WQFN (Top View)**



**図 5-2. DAC43902-Q1: RTE Package, 16-pin WQFN (Top View)**

表 5-1. Pin Functions

NO.	PIN		TYPE	DESCRIPTION
	NAME			
	DAC43901-Q1	DAC43902-Q1		
1	TRIG-IN	TRIG-IN	Input	Trigger input. This pin acts as the trigger input for fade-in fade-out or animation application.
2-4	NC	NC	—	No connection. Solder this pin to the pad.
5	SDO/NC	SDO/PWM3	Output	SDO: Serial data output for SPI in programming mode (VREF/MODE pin is low). When configured as SDO, connect this pin to the I/O voltage with an external pullup resistor. NC: No connection in standalone mode. Solder this pin to the pad. PWM3: PWM output channel 3 in standalone mode (VREF/MODE pin is high). This pin must be connected to the I/O voltage using an external pullup resistor.
6	SCL/ $\overline{\text{SYNC}}$ /NC	SCL/ $\overline{\text{SYNC}}$ /PWM2	Output	SCL: I <sup>2</sup> C serial interface clock or SPI chip select input in programming mode (VREF/MODE pin is low). This pin must be connected to the I/O voltage using an external pullup resistor. SYNC: Synchronize pin in programming mode. NC: No connection in standalone mode. Solder this pin to the pad. PWM2: PWM output channel 2 in standalone mode (VREF/MODE pin is high). This pin must be connected to the I/O voltage using an external pullup resistor.
7	A0/SDI/PWM1	A0/SDI/PWM1	Input	A0: Address configuration input for I <sup>2</sup> C or serial data input for SPI in programming mode (VREF/MODE pin is low). When set to A0, connect this pin to VDD, AGND, SDA, or SCL for address configuration. SDI: Serial data input for SPI in programming mode. When used as SDI, do not pull up or pull down this pin. PWM1: PWM output channel 1 in standalone mode (VREF/MODE pin is high). Connect this pin to the I/O voltage using an external pullup resistor.
8	SDA/SCLK/ PWM0	SDA/SCLK/ PWM0	Input/ Output	SDA: Bidirectional I <sup>2</sup> C serial data bus in programming mode (VREF/MODE pin is low). SCLK: SPI clock input in programming mode. PWM0: PWM output channel 0 in standalone mode (VREF/MODE pin is high). Connect this pin to the I/O voltage using an external pullup resistor.
9-10	NC	NC	—	No connection. Solder this pin to the pad.
11	NC	TRIG-OUT	Output	NC: No connection. Solder this pin to the pad. TRIG-OUT: Trigger output. Connect this pin to pin 12.
12	NC	TRIG-OUT	Input/ Output	NC: No connection. Solder this pin to the pad. TRIG-OUT: Trigger output. Connect this pin to pin 11.
13	CAP	CAP	Power	External bypass capacitor for the internal LDO. Connect a capacitor (approximately 1.5 $\mu$ F) between CAP and AGND.
14	AGND	AGND	Ground	Ground reference point for all circuitry on the device.
15	VDD	VDD	Power	Supply voltage: 1.8 V to 5.5 V.
16	VREF/MODE	VREF/MODE	Input	External reference or interface mode select input. Connect a capacitor (approximately 0.1 $\mu$ F) between VREF/MODE and AGND. Use a pullup resistor to VDD when the external reference is not used. In case an external reference is used or when in interface select mode, make sure the reference ramps up after VDD. In interface select mode: Pull this pin low to enable I <sup>2</sup> C or SPI communication. Pull this pin high to enable standalone mode.
Thermal Pad	Thermal Pad	Thermal Pad	Ground	Connect the thermal pad to AGND.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage, V <sub>DD</sub> to AGND	-0.3	6	V
	Digital inputs to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	V <sub>TRIG-OUT</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	V <sub>TRIG-IN</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>REF</sub>	External reference, V <sub>REF</sub> to AGND	-0.3	V <sub>DD</sub> + 0.3	V
	Current into any pin except the TRIG-OUT, VDD, and AGND pins	-10	10	mA
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000	V	
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, 8, 9, 12, 13, and 16)		±750
			All pins		±500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Positive supply voltage to ground (AGND)	1.7		5.5	V
V <sub>REF</sub>	External reference to ground (AGND)	1.7		V <sub>DD</sub>	V
V <sub>IH</sub>	Digital input high voltage, 1.7 V < V <sub>DD</sub> ≤ 5.5 V	1.62			V
V <sub>IL</sub>	Digital input low voltage			0.4	V
C <sub>CAP</sub>	External capacitor on CAP pin	0.5		15	μF
T <sub>A</sub>	Ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DAC4390x-Q1		UNIT
		RTE (WQFN)		
		16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	49		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	24.1		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	24.1		°C/W

THERMAL METRIC <sup>(1)</sup>		DAC4390x-Q1	UNIT
		RTE (WQFN)	
		16 PINS	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics: Comparator Mode

all minimum/maximum specifications at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  and typical specifications at  $T_A = 25^\circ\text{C}$ ,  $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , DAC reference tied to VDD, gain = 1 ×, DAC output pin (TRIG-OUT) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC PERFORMANCE</b>						
	Offset error <sup>(1) (2)</sup>	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ; DAC at midscale, comparator input at Hi-Z, and DAC operating with external reference.	-7.5	0	7.5	mV
	Offset-error time drift <sup>(1)</sup>	$V_{DD} = 5.5\text{ V}$ , external reference, $T_A = 125^\circ\text{C}$ , TRIG-IN in Hi-Z mode, DAC at full scale and $V_{\text{TRIG-IN}}$ at 0 V or DAC at zero scale and $V_{\text{TRIG-IN}}$ at 1.84 V, drift specified for 10 years of continuous operation		4		mV
<b>OUTPUT</b>						
	Input voltage	$V_{\text{REF}}$ connected to $V_{DD}$ , TRIG-IN resistor network connected to ground	0		$V_{DD}$	V
		$V_{\text{REF}}$ connected to $V_{DD}$ , TRIG-IN resistor network disconnected from ground	0		$V_{DD} (1/3 - 1/100)$	
$V_{OL}$	Logic-low output voltage	$I_{LOAD} = 100\text{ }\mu\text{A}$ , output in open-drain mode		0.1		V
<b>DYNAMIC PERFORMANCE</b>						
$t_{\text{resp}}$	Output response time	DAC at midscale with 10-bit resolution, TRIG-IN input at Hi-Z, and transition step at TRIG-IN node is ( $V_{DAC} - 2\text{ LSB}$ ) to ( $V_{DAC} + 2\text{ LSB}$ ), transition time measured between 10% and 90% of output, output current of $100\text{ }\mu\text{A}$ , comparator output configured in push-pull mode, load capacitor at DAC output is $25\text{ pF}$		10		$\mu\text{s}$

- (1) Specified by design and characterization, not production tested.  
 (2) This specification does not include the total unadjusted error (TUE) of the DAC.

## 6.6 Electrical Characteristics: General

all minimum/maximum specifications at  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  and typical specifications at  $T_A = 25^{\circ}\text{C}$ ,  $1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , reference tied to VDD, gain = 1 ×, DAC output pin (TRIG-OUT) loaded with resistive load ( $R_L = 5\text{ k}\Omega$  to AGND) and capacitive load ( $C_L = 200\text{ pF}$  to AGND), and digital inputs at VDD or AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERNAL REFERENCE</b>						
	Initial accuracy	$T_A = 25^{\circ}\text{C}$ for all measurements	1.1979	1.212	1.224	V
	Reference output temperature coefficient <sup>(1) (2)</sup>				60	ppm/ $^{\circ}\text{C}$
<b>EXTERNAL REFERENCE (<math>V_{REF}</math>)</b>						
	External reference input voltage		1.7		$V_{DD}$	V
	$V_{REF}$ input impedance <sup>(1) (3)</sup>			192		k $\Omega$ -ch
<b>EEPROM</b>						
	Endurance <sup>(1)</sup>	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		20000		Cycles
		$T_A = 125^{\circ}\text{C}$		1000		
	Data retention <sup>(1)</sup>			50		Years
	EEPROM programming write cycle time <sup>(1)</sup>				200	ms
	Device boot-up time <sup>(1)</sup>	Time taken from power valid ( $V_{DD} \geq 1.7\text{ V}$ ) to output valid state (output state as programmed in EEPROM), 0.5- $\mu\text{F}$ capacitor on the CAP pin		5		ms
<b>DIGITAL INPUTS</b>						
	Pin capacitance	Per pin		10		pF
<b>POWER</b>						
$I_{DD}$	Current flowing into VDD	Sleep mode, internal reference disabled, external reference at 5.5 V			28	$\mu\text{A}$
		Sleep mode, internal reference enabled, additional current through internal reference <sup>(1)</sup>		10		
		DAC channels enabled, internal reference enabled, additional current through internal reference per DAC channel <sup>(1)</sup>		12.5		$\mu\text{A}$ -ch
		Normal operation, state machine enabled <sup>(1)</sup>	DAC43901-Q1	1.02		mA
	DAC43902-Q1	1.2				

- (1) Specified by design and characterization, not production tested.  
 (2) Measured at  $-40^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  and calculated the slope.  
 (3) Impedances for the DAC channels are connected in parallel.



## 6.7 Timing Requirements: I<sup>2</sup>C Standard Mode

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 1.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, -40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCLK</sub>	SCL frequency			100	kHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	4.7			μs
t <sub>HDSTA</sub>	Hold time after repeated start	4			μs
t <sub>SUSTA</sub>	Repeated start setup time	4.7			μs
t <sub>SUSTO</sub>	Stop condition setup time	4			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	250			ns
t <sub>LOW</sub>	SCL clock low period	4700			ns
t <sub>HIGH</sub>	SCL clock high period	4000			ns
t <sub>F</sub>	Clock and data fall time			300	ns
t <sub>R</sub>	Clock and data rise time			1000	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			3.45	μs
t <sub>VDACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			3.45	μs

## 6.8 Timing Requirements: I<sup>2</sup>C Fast Mode

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 1.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, -40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCLK</sub>	SCL frequency			400	kHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	1.3			μs
t <sub>HDSTA</sub>	Hold time after repeated start	0.6			μs
t <sub>SUSTA</sub>	Repeated start setup time	0.6			μs
t <sub>SUSTO</sub>	Stop condition setup time	0.6			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	100			ns
t <sub>LOW</sub>	SCL clock low period	1300			ns
t <sub>HIGH</sub>	SCL clock high period	600			ns
t <sub>F</sub>	Clock and data fall time			300	ns
t <sub>R</sub>	Clock and data rise time			300	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.9	μs
t <sub>VDACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.9	μs

## 6.9 Timing Requirements: I<sup>2</sup>C Fast-Mode Plus

all input signals are timed from VIL to 70% of V<sub>pull-up</sub>, 1.7 V ≤ V<sub>DD</sub> ≤ 5.5 V, -40°C ≤ T<sub>A</sub> ≤ +125°C, and 1.7 V ≤ V<sub>pull-up</sub> ≤ V<sub>DD</sub>

		MIN	NOM	MAX	UNIT
f <sub>SCLK</sub>	SCL frequency			1	MHz
t <sub>BUF</sub>	Bus free time between stop and start conditions	0.5			μs
t <sub>HDSTA</sub>	Hold time after repeated start	0.26			μs
t <sub>SUSTA</sub>	Repeated start setup time	0.26			μs
t <sub>SUSTO</sub>	Stop condition setup time	0.26			μs
t <sub>HDDAT</sub>	Data hold time	0			ns
t <sub>SUDAT</sub>	Data setup time	50			ns
t <sub>LOW</sub>	SCL clock low period	0.5			μs
t <sub>HIGH</sub>	SCL clock high period	0.26			μs
t <sub>F</sub>	Clock and data fall time			120	ns
t <sub>R</sub>	Clock and data rise time			120	ns
t <sub>VDDAT</sub>	Data valid time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.45	μs
t <sub>VDACK</sub>	Data valid acknowledge time, R = 360 Ω, C <sub>trace</sub> = 23 pF, C <sub>probe</sub> = 10 pF			0.45	μs

### 6.10 Timing Requirements: SPI Write Operation

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			50	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	9			ns
$t_{\text{SCLKLOW}}$	SCLK low time	9			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	18			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	10			ns
$t_{\text{CSHIGH}}$	$\overline{\text{SYNC}}$ high time	50			ns
$t_{\text{DACWAIT}}$	Sequential update wait time(time between subsequent $\overline{\text{SYNC}}$ rising edges) for same channel	2			$\mu\text{s}$

### 6.11 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 0)

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , and  $\text{FSDO} = 0$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			1.25	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	350			ns
$t_{\text{SCLKLOW}}$	SCLK low time	350			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	400			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	400			ns
$t_{\text{CSHIGH}}$	$\overline{\text{SYNC}}$ high time	1			$\mu\text{s}$
$t_{\text{SDODLY}}$	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$ , $C_L = 20 \text{ pF}$			300	ns

### 6.12 Timing Requirements: SPI Read and Daisy Chain Operation (FSDO = 1)

all input signals are specified with  $t_r = t_f = 1 \text{ V/ns}$  (10% to 90% of  $V_{IO}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH}) / 2$ ,  $1.7 \text{ V} \leq V_{IO} \leq 5.5 \text{ V}$ ,  $1.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , and  $\text{FSDO} = 1$

		MIN	NOM	MAX	UNIT
$f_{\text{SCLK}}$	Serial clock frequency			2.5	MHz
$t_{\text{SCLKHIGH}}$	SCLK high time	175			ns
$t_{\text{SCLKLOW}}$	SCLK low time	175			ns
$t_{\text{SDIS}}$	SDI setup time	8			ns
$t_{\text{SDIH}}$	SDI hold time	8			ns
$t_{\text{CSS}}$	$\overline{\text{SYNC}}$ to SCLK falling edge setup time	300			ns
$t_{\text{CSH}}$	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	300			ns
$t_{\text{CSHIGH}}$	$\overline{\text{SYNC}}$ high time	1			$\mu\text{s}$
$t_{\text{SDODLY}}$	SCLK rising edge to SDO falling edge, $I_{OL} \leq 5 \text{ mA}$ , $C_L = 20 \text{ pF}$			300	ns

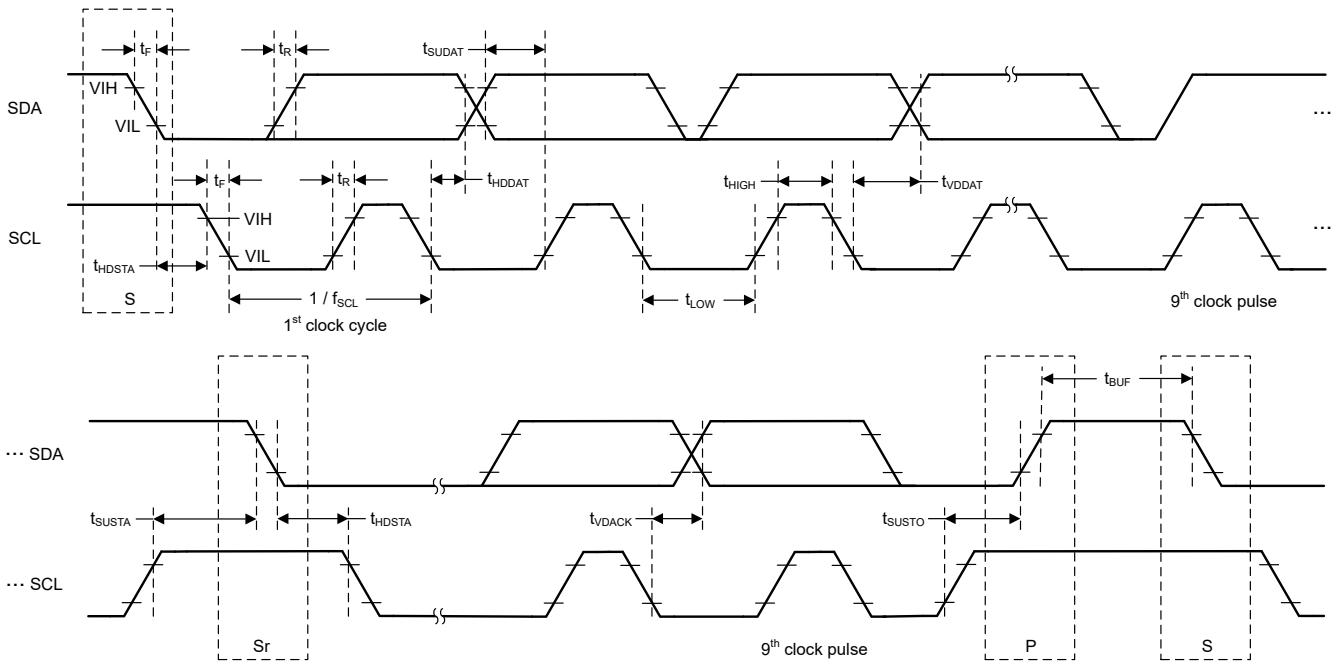
### 6.13 Timing Requirements: PWM Output

all input signals are timed from VIL to 70% of  $V_{pull-up}$ ,  $1.7 V \leq V_{DD} \leq 5.5$ ,  $-40^{\circ}C \leq T_A \leq +125^{\circ}C$ , and  $1.7 V \leq V_{pull-up} \leq V_{DD}$

		MIN	NOM	MAX	UNIT
$f_{PWMOUT}$	PWM frequency <sup>(1)</sup>	0.218		48.828	kHz
$t_{PWMOHI}$	PWM high time	1			$\mu s$
$t_{PWMOLO}$	PWM low time	1			$\mu s$
$t_{PWMODTY}$	PWM duty cycle	0		100	%

(1) The frequency range does not account for the internal oscillator frequency error.

### 6.14 Timing Diagrams



S: Start bit, Sr: Repeated start bit, P: Stop bit

图 6-1. I<sup>2</sup>C Timing Diagram

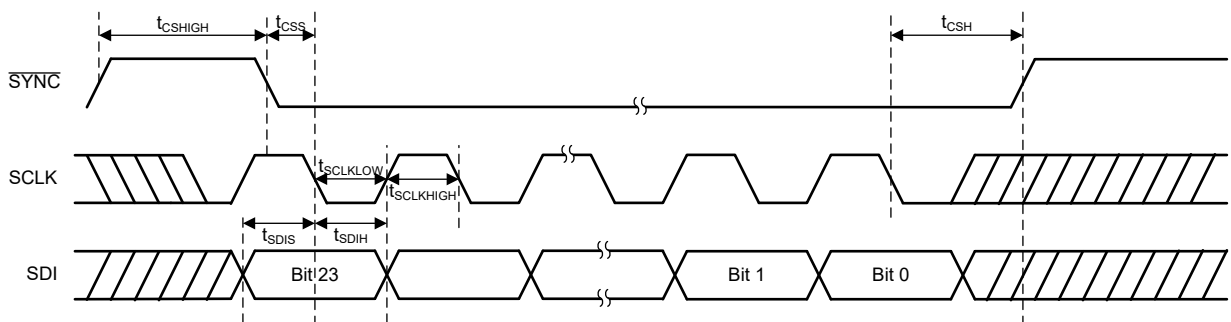


图 6-2. SPI Write Timing Diagram

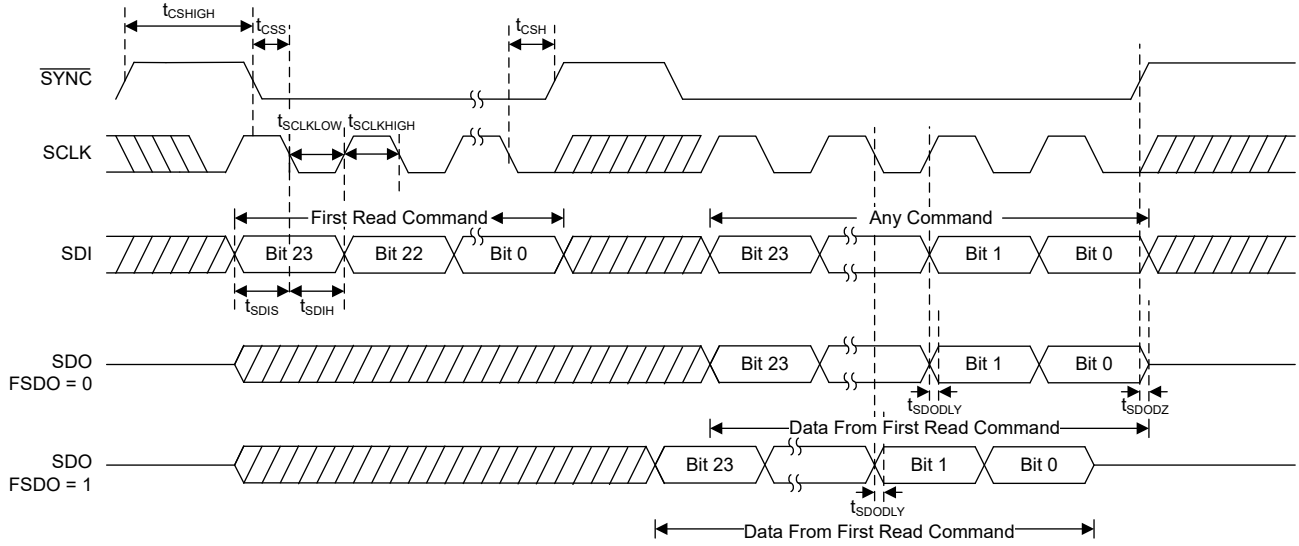


図 6-3. SPI Read Timing Diagram

## 6.15 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , external reference = 5.5 V, gain = 1  $\times$ , and DAC outputs unloaded (unless otherwise noted)

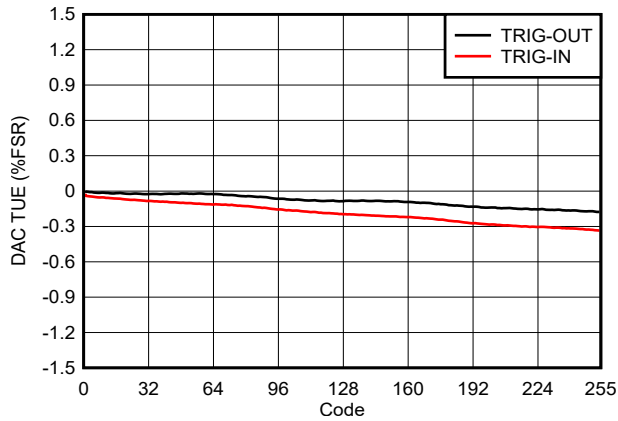


図 6-4. DAC TUE vs Digital Input Code

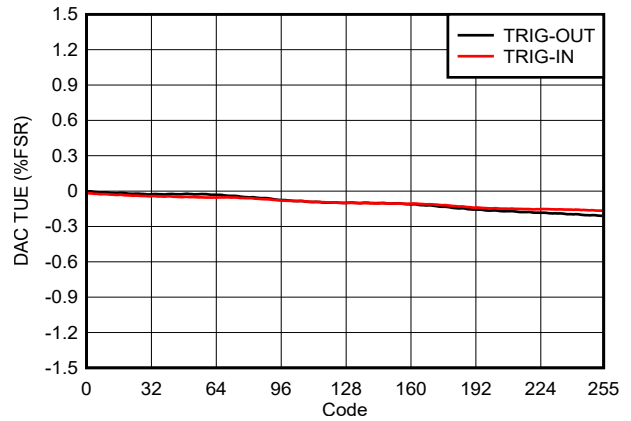


図 6-5. DAC TUE vs Digital Input Code

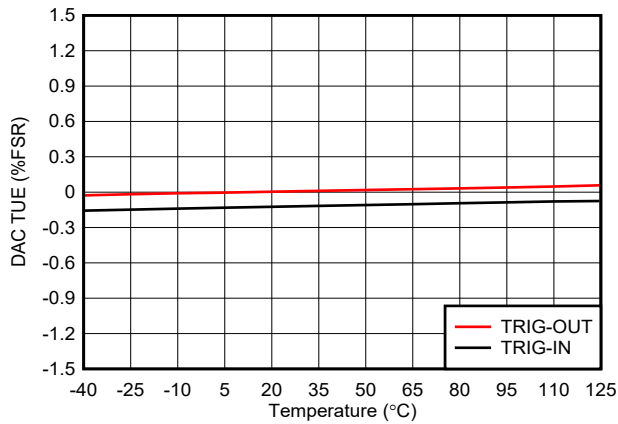


図 6-6. DAC TUE vs Temperature

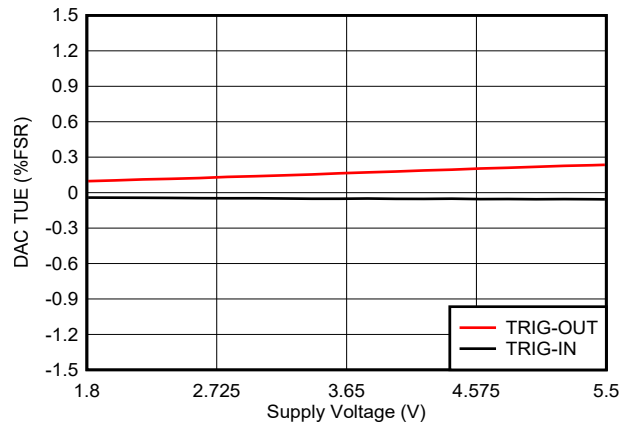


図 6-7. DAC TUE vs Supply Voltage

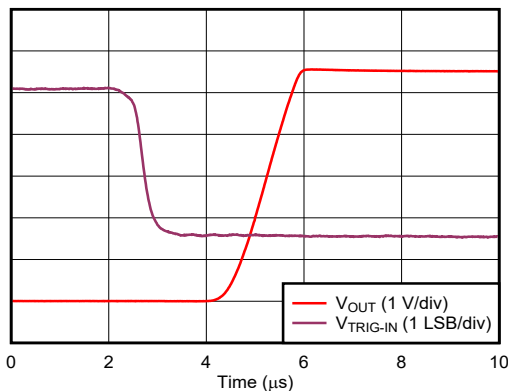


図 6-8. Comparator Response Time: Low-to-High Transition

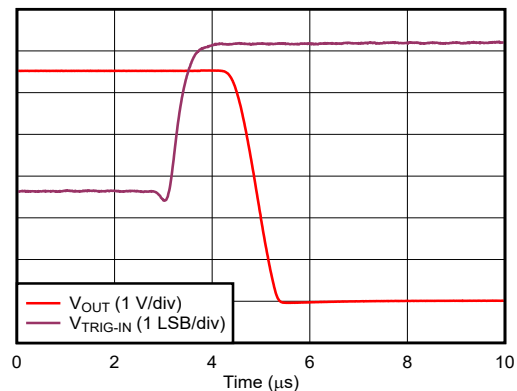


図 6-9. Comparator Response Time: High-to-Low Transition

### 6.15 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.5\text{ V}$ , external reference =  $5.5\text{ V}$ , gain =  $1 \times$ , and DAC outputs unloaded (unless otherwise noted)

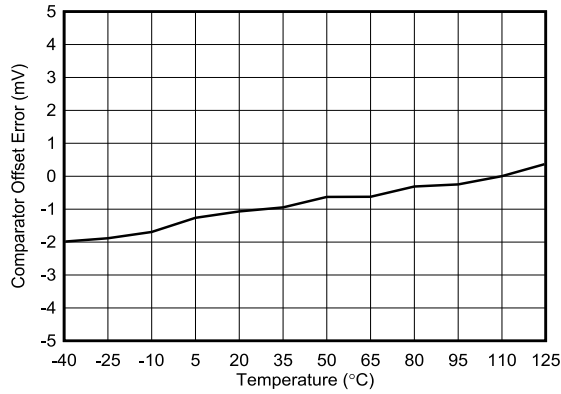


Figure 6-10. Comparator Offset Error vs Temperature

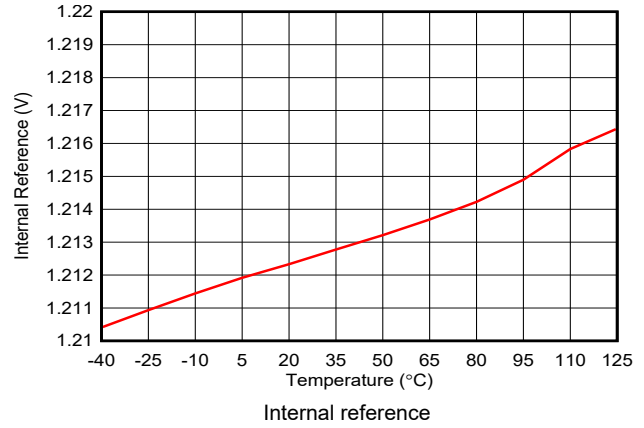


Figure 6-11. Internal Reference vs Temperature

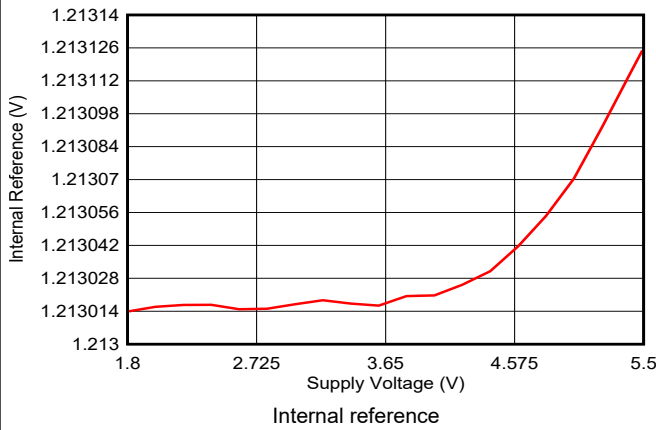


Figure 6-12. Internal Reference vs Supply Voltage

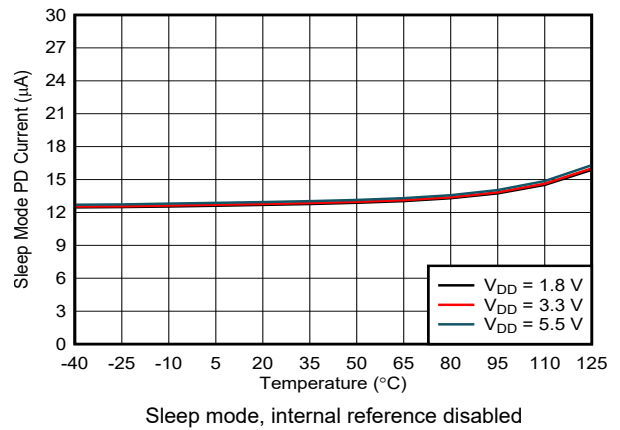


Figure 6-13. Power-Down Current vs Temperature

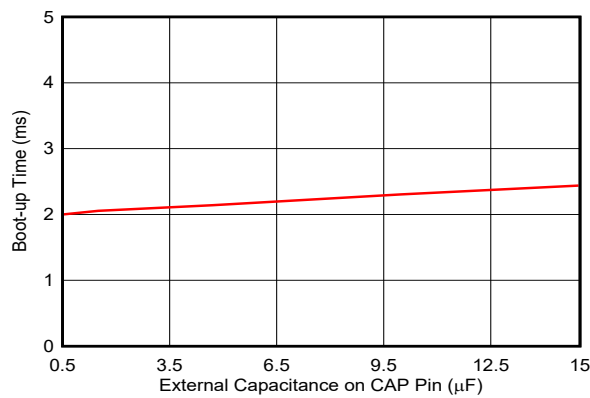


Figure 6-14. Boot-up Time vs Capacitance on CAP pin

## 7 Detailed Description

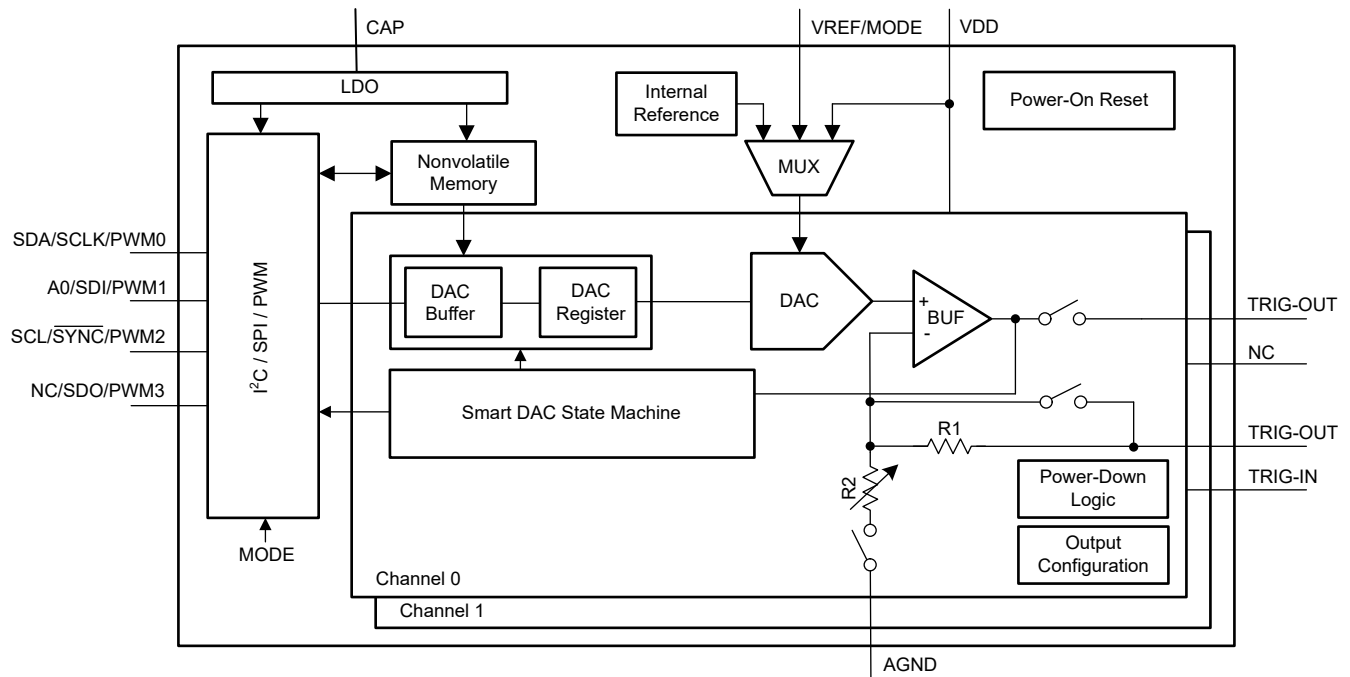
### 7.1 Overview

The DAC43901-Q1 and the DAC43902-Q1 (DAC4390x-Q1) are 8-bit smart DACs with an internal reference, programmable comparator. The DAC43901-Q1 supports logarithmic fade-in fade-out with PWM output. The DAC43902-Q1 supports sequential animation for automotive, turn indicator lights. DAC43901-Q1 and DAC43902-Q1 devices can be cascaded to create animation for more than four channels.

These smart DACs use the VREF/MODE pin to select between the programming mode (I<sup>2</sup>C or SPI) and standalone mode (PWM and TRIG-IN/OUT). The DAC4390x-Q1 provide nonvolatile memory (NVM) to store the register settings at factory using the I<sup>2</sup>C or SPI. After being programmed, these devices function autonomously without the need for a processor.

The PWM outputs are generated using the four digital pins. When PWM output mode is selected, one DAC channel is configured as a comparator to support the TRIG-IN input while the other DAC acts as an on/off voltage output to support TRIG-OUT.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

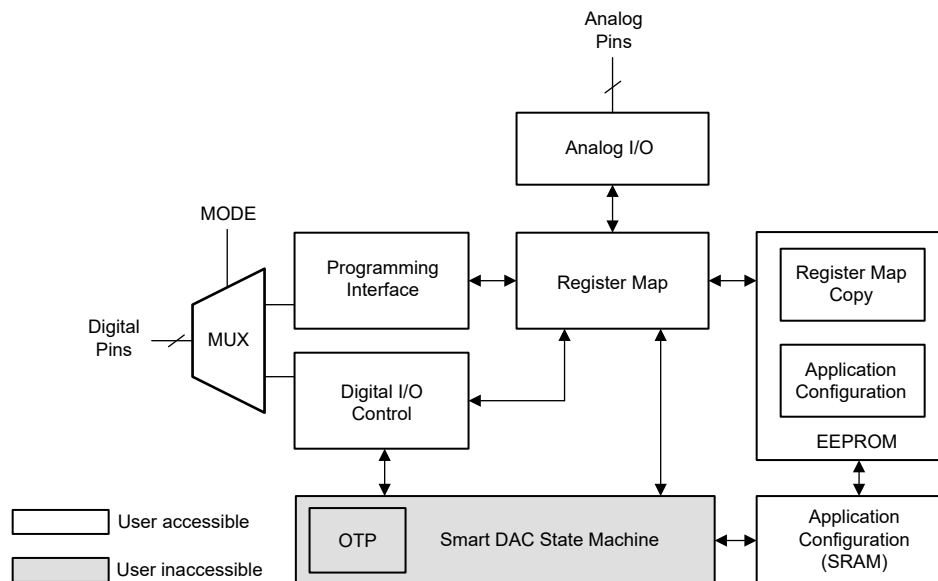
### 7.3.1 Smart Digital-to-Analog Converter (DAC) Architecture

The DAC4390x-Q1 feature a programmable state machine supporting arithmetic, logic, and timing operations, as shown in [Figure 7-1](#). This state machine is preprogrammed as a logarithmic fade-in and fade-out animation controller for the DAC43901-Q1, and as a sequential turn indicator for the DAC43902-Q1, allowing the user to program the fade-in fade-out and channel delay timings. The state machine can be disabled by writing to the STATE-MACHINE-CONFIG0 register. The user configurations are stored in the NVM. The state machine can be operated in standalone mode without interfacing to a processor (*processor-less* operation).

The DAC4390x-Q1 provide digital PWM outputs with 7-bit duty-cycle resolution and 32 discrete frequency settings. The PWM pins are multiplexed with the programming pins. The VREF/MODE pin selects between the programming and standalone modes of operation.

The DAC4390x-Q1 provide DAC channels that use a string architecture with a voltage-output amplifier that can also be used as comparators. [Section 7.2](#) shows the DAC architecture within the block diagram, which operates from a 1.8-V to 5.5-V power supply. The DAC channels use one of the following three reference options: the DAC internal voltage reference of 1.21 V, an external reference on the VREF/MODE pin, or the power supply.

The DAC4390x-Q1 devices include a *smart* feature set to enable *processor-less* operation and high-integration. The NVM enables a predictable start-up. These devices support internal function generation, such as sawtooth, triangular, sine, and PWM. These devices also support a state machine that is preconfigured for specific applications on different devices. These state machines are configured using the register map, and the parameters can be stored in the NVM.



**図 7-1. Smart DAC Architecture**

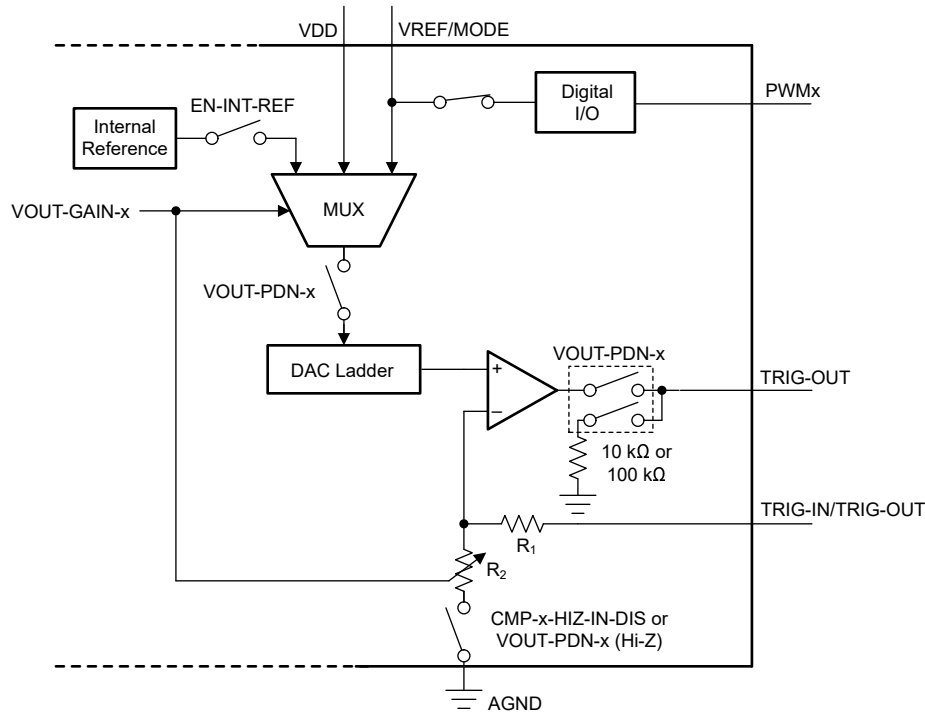


### 7.3.2 Threshold DAC

The threshold DAC for TRIG-IN is enabled by selecting the power-up option in the VOUT-X-PDN fields in the COMMON-CONFIG register. For output trigger on DAC43902-Q1, short the TRIG-OUT pins of respective channel externally. The TRIG-OUT can toggle between VDD and AGND. The DAC4390x-Q1 provide multiple reference options and amplifier gains for the required TRIG-IN range.

#### 7.3.2.1 Voltage Reference and DAC Transfer Function

There are three voltage reference options possible with the DAC4390x-Q1: internal reference, external reference, and the power supply as reference, as shown in 7-2. The threshold-DAC transfer function changes based on the voltage reference selection.



7-2. Voltage Reference Selection and Power-Down Logic

#### 7.3.2.2 Power-Supply as Reference

By default, the DAC4390x-Q1 operate with the power-supply pin (VDD) as a reference. 1 shows DAC transfer function when the power-supply pin is used as reference. The gain at the output stage is always 1 ×.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{DD} \quad (1)$$

where:

- N is the resolution in bits, 8 bits for DAC4390x-Q1.
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC\_DATA ranges from 0 to  $2^N - 1$ .
- $V_{DD}$  is used as the DAC reference voltage.

### 7.3.2.3 Internal Reference

The DAC4390x-Q1 contain an internal reference that is disabled by default. To enable the internal reference, write 1 to bit EN-INT-REF in the COMMON-CONFIG register. The internal reference generates a fixed 1.21-V voltage (typical). Use the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register to achieve gains of 1.5 ×, 2 ×, 3 ×, or 4 × for the DAC output voltage (V<sub>OUT</sub>). 式 2 shows the threshold-DAC transfer function using the internal reference.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \times GAIN \quad (2)$$

where:

- N is the resolution in bits, 8 bits for DAC4390x-Q1
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC\_DATA ranges from 0 to 2<sup>N</sup> – 1.
- V<sub>REF</sub> is the internal reference voltage = 1.21 V.
- GAIN = 1.5 ×, 2 ×, 3 ×, or 4 ×, based on VOUT-GAIN-x bits.

### 7.3.2.4 External Reference

The DAC4390x-Q1 provide an external reference input. Select the external reference option by configuring the VOUT-GAIN-x field in the DAC-x-VOUT-CMP-CONFIG register appropriately. The external reference can be between 1.8 V and VDD. 式 3 shows the threshold-DAC transfer function when the external reference is used.

#### 注

The external reference must be less than VDD in both transient and steady-state conditions. Therefore, the external reference must ramp up after VDD and ramp down before VDD.

$$V_{OUT} = \frac{DAC\_DATA}{2^N} \times V_{REF} \quad (3)$$

where:

- N is the resolution in bits, 8 bits for DAC4390x-Q1.
- DAC\_DATA is the decimal equivalent of the binary code that is loaded to the DAC register.
- DAC\_DATA ranges from 0 to 2<sup>N</sup> – 1.
- V<sub>REF</sub> is the external reference voltage.

### 7.3.3 Programming Interface

The DAC4390x-Q1 have four digital I/O pins that include I<sup>2</sup>C and SPI. These devices automatically detect I<sup>2</sup>C and SPI protocols at the first successful communication after power-on, and then connect to the detected interface. After an interface protocol is connected, any change in the protocol is ignored. The I<sup>2</sup>C interface uses the A0 pin to select from among four address options. The SPI is a 3-wire interface by default. No readback capability is available in this mode. The NC/SDO pin can be configured in the register map and then programmed in to the NVM as the SDO pin. The SPI readback mode is slower than the write mode. The programming interface pins are:

- I<sup>2</sup>C: SCL, SDA, A0
- SPI: SCLK, SDI,  $\overline{\text{SYNC}}$ , NC/SDO

All the digital pins are open-drain when used as outputs. Therefore, all the output pins must be pulled up to the desired I/O voltage using external resistors.

### 7.3.4 Nonvolatile Memory (NVM)

The DAC4390x-Q1 contain nonvolatile memory (NVM) bits. These memory bits are user programmable and erasable, and retain the set values in the absence of a power supply. All the register bits, as shown in the highlighted gray cells in the *Register Map* section, can be stored in the NVM by setting NVM-PROG = 1 in the COMMON-TRIGGER register. The NVM-PROG is an autoresetting bit. The default values for all the registers in the DAC4390x-Q1 are loaded from NVM as soon as a POR event is issued.

The DAC4390x-Q1 also implement NVM-RELOAD bit in the COMMON-TRIGGER register. Set this bit to 1 for the device to start an NVM-reload operation. After completion, the device autoresets the NVM-RELOAD bit to 0. During the NVM write or reload operation, all read/write operations to the device are blocked. The *Electrical Characteristics: General* section provides the timing specification for the NVM write cycle. The processor must wait for the specified duration before resuming any read or write operation on the SPI or I<sup>2</sup>C interface.

#### 7.3.4.1 NVM Cyclic Redundancy Check (CRC)

The DAC4390x-Q1 implements a cyclic redundancy check (CRC) feature for the NVM to make sure that the data stored in the NVM is uncorrupted. There are two types of CRC alarm bits implemented in the DAC4390x-Q1:

- NVM-CRC-FAIL-USER
- NVM-CRC-FAIL-INT

The NVM-CRC-FAIL-USER bit indicates the status of user-programmable NVM bits, and the NVM-CRC-FAIL-INT bit indicates the status of internal NVM bits. The CRC feature is implemented by storing a 16-bit CRC (CRC-16-CCITT) along with the NVM data each time the NVM program operation (write or reload) is performed and during the device boot up. The device reads the NVM data and validates the data with the stored CRC. The CRC alarm bits (NVM-CRC-FAIL-USER and NVM-CRC-FAIL-INT in the GENERAL-STATUS register) report any errors after the data are read from the device NVM. The alarm bits are set only at boot up.

##### 7.3.4.1.1 NVM-CRC-FAIL-USER Bit

A logic 1 on NVM-CRC-FAIL-USER bit indicates that the user-programmable NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. To reset the alarm bits to 0, issue a software reset (see [セクション 7.3.6](#)) command, or cycle power to the device. A software reset or power-cycle also reloads the user-programmable NVM bits. In case the failure persists, reprogram the NVM.

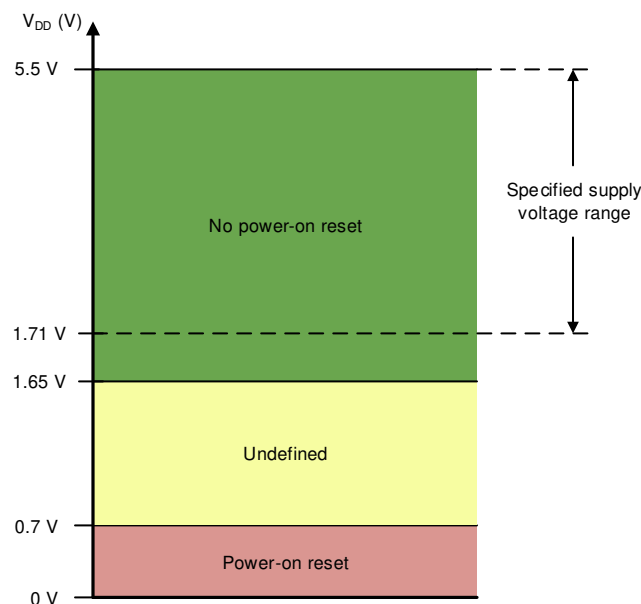
##### 7.3.4.1.2 NVM-CRC-FAIL-INT Bit

A logic 1 on NVM-CRC-FAIL-INT bit indicates that the internal NVM data are corrupt. During this condition, all registers in the device are initialized with factory reset values, and any registers can be written to or read from. In case of a temporary failure, to reset the alarm bits to 0, issue a software reset (see [セクション 7.3.6](#)) command or cycle power to the device. A permanent failure in the NVM makes the device unusable.

### 7.3.5 Power-On Reset (POR)

The DAC4390x-Q1 family of devices includes a power-on reset (POR) function that controls the output voltage at power up. After the  $V_{DD}$  supply has been established, a POR event is issued. The POR causes all registers to initialize to default values, and communication with the device is valid only after a POR (boot-up) delay. The default value for all the registers in the DAC4390x-Q1 is loaded from NVM as soon as the POR event is issued.

When the device powers up, a POR circuit sets the device to the default mode. The POR circuit requires specific  $V_{DD}$  levels, as indicated in [Figure 7-3](#), to make sure that the internal capacitors discharge and reset the device at power up. To make sure that a POR occurs,  $V_{DD}$  must be less than 0.7 V for at least 1 ms. When  $V_{DD}$  drops to less than 1.65 V, but remains greater than 0.7 V (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions. In this case, initiate a POR. When  $V_{DD}$  remains greater than 1.65 V, a POR does not occur.



**Figure 7-3. Threshold Levels for  $V_{DD}$  POR Circuit**

### 7.3.6 External Reset

An external reset to the device can be triggered through the register map. To initiate a device software reset event, write the reserved code 1010b to the RESET field in the COMMON-TRIGGER register. A software reset initiates a POR event.

### 7.3.7 Register-Map Lock

The DAC4390x-Q1 implement a register-map lock feature that prevents an accidental or unintended write to the DAC registers. The device locks all the registers when the DEV-LOCK bit in the COMMON-CONFIG register is set to 1. However, the software reset function through the COMMON-TRIGGER register is not blocked when using I<sup>2</sup>C interface. To bypass the DEV-LOCK setting, write 0101b to the DEV-UNLOCK bits in the COMMON-TRIGGER register.

## 7.4 Device Functional Modes

### 7.4.1 Comparator Mode

A threshold DAC and a comparator is used for the TRIG-IN input. The threshold DAC is fixed at midscale. To enter the comparator mode for a channel, write 1 to the CMP-x-EN bit in the respective DAC-x-VOUT-CMP-CONFIG register. The comparator output can be configured as push-pull or open-drain using the CMP-x-OD-EN bit. To enable the comparator output on the output pin, write 1 to the CMP-x-OUT-EN bit. To invert the comparator output, write 1 to the CMP-x-INV-EN bit. The TRIG-IN pin has a finite impedance. By default, the TRIG-IN pin is in the high-impedance mode. To disable high-impedance on the TRIG-IN pin, write 1 to the CMP-x-HIZ-IN-DIS bit. 表 7-1 shows the comparator output at the pin for different bit settings. 表 7-2 shows the full scale analog input settings for the comparator. Any higher input voltage is clipped.

**表 7-1. Comparator Output Configuration**

CMP-x-EN	CMP-x-OUT-EN	CMP-x-OD-EN	CMP-x-INV-EN	CMP-x-OUT PIN
0	X	X	X	Comparator not enabled
1	0	X	X	No output
1	1	0	0	Push-pull output
1	1	0	1	Push-pull and inverted output
1	1	1	0	Open-drain output
1	1	1	1	Open-drain and inverted output

**表 7-2. Full Scale Analog Input ( $V_{FS}$ )**

REFERENCE ( $V_{REF}$ )	GAIN	$V_{FS}$ (HI-Z INPUT MODE)	$V_{FS}$ (FINITE IMPEDANCE INPUT MODE)
Power supply	1 ×	VDD / 3	VDD
External	1 ×	VREF / 3	VREF
Internal	1.5 ×	(VREF × GAIN) / 3	VREF × GAIN
	2 ×	(VREF × GAIN) / 3	VREF × GAIN
	3 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2
	4 ×	(VREF × GAIN) / 6	(VREF × GAIN) / 2

### 7.4.2 PWM Fade-In Fade-Out Mode

The DAC43901-Q1 support a state-machine preconfigured for PWM (pulse-width-modulation) fade-in fade-out, used for smooth dimming of lights and starting of motors. The fade-in fade-out is done logarithmically. DAC channel 0 is used as a comparator and the TRIG-IN pin is used as the trigger input for the fade-in fade-out. The PWM outputs are available on the digital pins in standalone mode. The device goes into the standalone mode when the VREF/MODE pin is pulled high. In this mode, the programming interface is disabled. The digital programming interface (I<sup>2</sup>C and SPI) pins are open-drain outputs and must be pulled up to function as PWMx outputs. In standalone mode, the device runs using the configurations in NVM. Pulling the VREF/MODE pin low brings the device into programming mode. When the PWM output mode is enabled, all four programming interface pins act as PWMx outputs, even if not used. Partial selection is not possible. The fade-in fade-out PWM output is available on PWM0 (SDA/SCLK) and PWM1 (A0/SDI). 表 7-3 shows the PWM output mapping on the digital pins. The PWM duty-cycle resolution is 7 bits. The PWM0 transitions from the predefined minimum duty cycle to the maximum duty cycle on the rising edge of the trigger input and transitions from the maximum duty cycle to minimum duty cycle on the falling edge of the trigger input. The fade-in fade-out configurations for PWM0 are programmed using the SRAM or the register addresses shown in 表 7-4.

表 7-3. Fade-In Fade-Out Pin Mapping

FADE-IN FADE-OUT INTERFACE	MULTIPLEXED PROGRAMMING PIN	PIN NO.
PWM0	SDA/SCLK	8
PWM1	A0/SDI	7
TRIG-IN	TRIG-IN	1

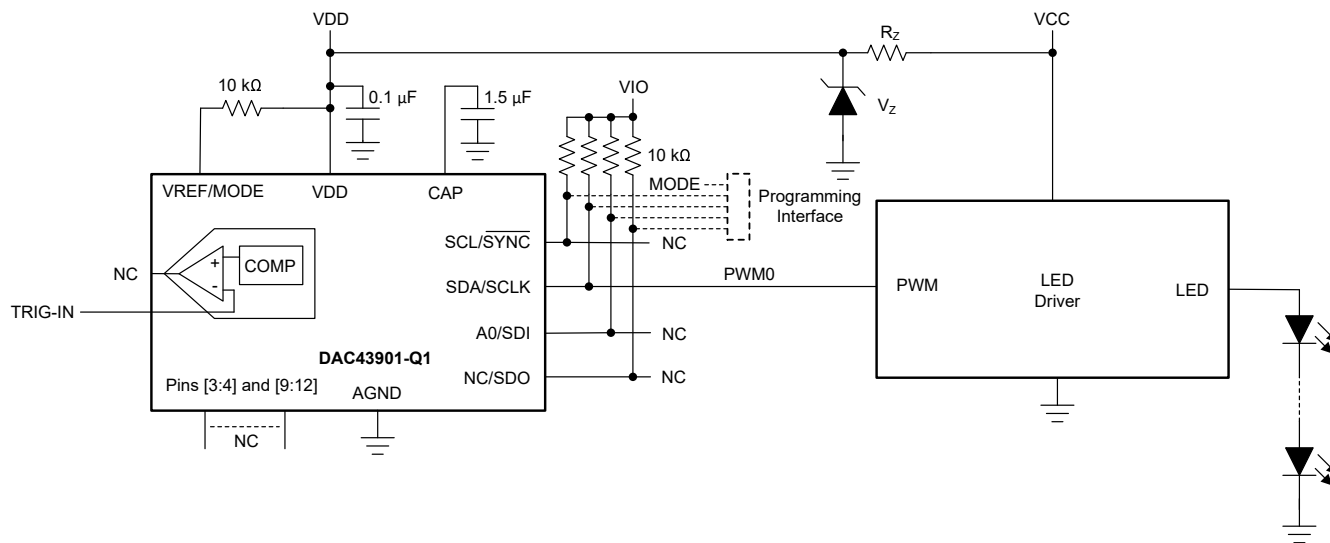


図 7-4. PWM Fade-In Fade-Out

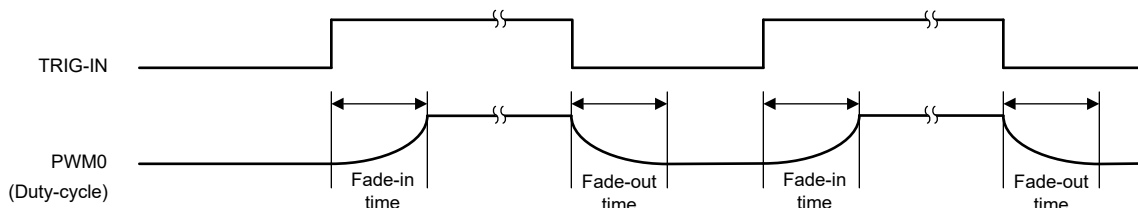


図 7-5. Fade-In Fade-out High-Level Timing Diagram

By default the DAC43901-Q1 is configured in the PWM fade-in fade-out with the default settings as shown in 表 7-4. To change settings in the SRAM, write the SRAM address to the SRAM-ADDR register followed by a write to the SRAM-DATA register with the data. The register locations can be directly written with a single I<sup>2</sup>C or SPI sequence. In fade-in fade-out mode or animation mode, the basic setting is the fade-in or fade-out SLEW\_RATE as depicted in 図 7-6. The SLEW\_RATE defines the timing resolution of the application. When the SLEW\_RATE is multiplied with the number of steps in the fading, the fading time is obtained. The SLEW\_RATE can be calculated using 式 4. In logarithmic fading, the number of steps are nonlinear and also depend on the start and end duty-cycle settings. The total fading time is calculated using 式 5 and 表 7-5. The fade-in can be started after a delay, calculated per 式 7. CH0-DELAY defines the fade-in delay for PWM0, and COM-DELAY defines the fade-in delay for PWM1. The delay applies even when the fade-in is disabled by writing 0 for FADE-IN SLEW\_RATE. In this case, a predefined delay setting of 256 is considered. There is no delay for fade-out.

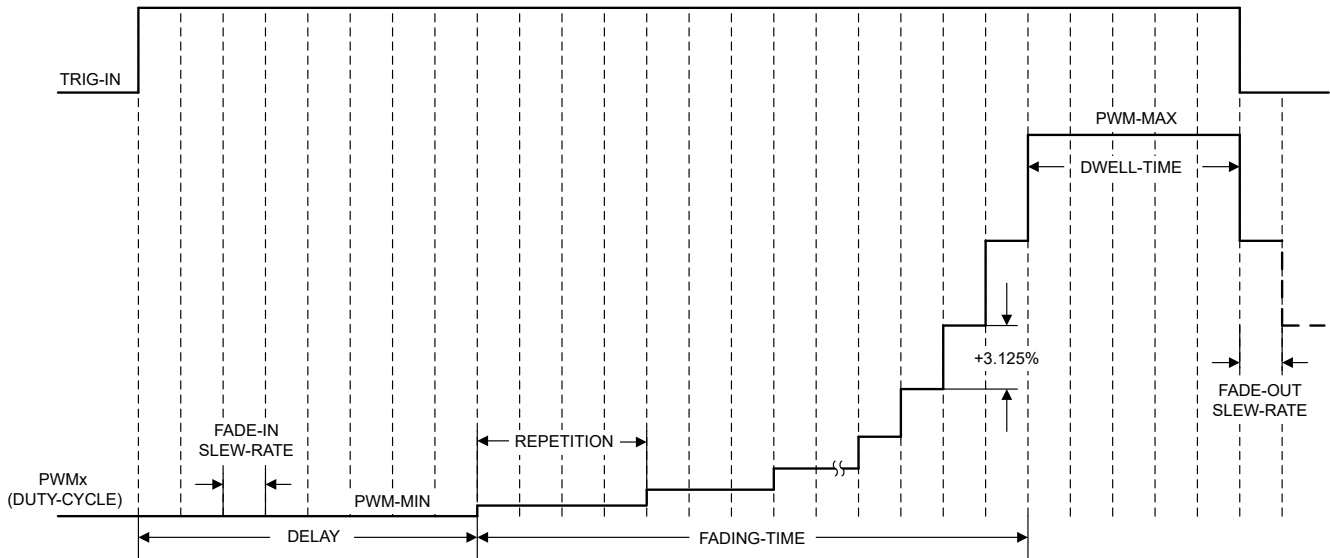


図 7-6. Fade-in Fade-Out Detailed Timing Diagram

$$t_{\text{SLEW}}(\mu\text{s}) = 2.4 \times \text{SLEW\_RATE} + 5.6 \quad (4)$$

where:

- $t_{\text{SLEW\_RATE}}$  is the fade-in or fade-out unit time in microseconds/step.
- SLEW\_RATE is the FADE-IN SLEW-RATE or FADE-OUT SLEW-RATE as specified in 表 7-4.

The pseudocode to compute the fade-in and fade-out steps is as follows:

```

min_duty = <user input>
max_duty = <use input>
if(min_duty == 0)
    min_duty = 1
#IF FADE-IN
current_duty = min_duty << 5
next_duty = integer(current_duty + (current_duty >> 5))
#ELIF FADE-OUT
current_duty = max_duty << 5
next_duty = integer(current_duty - (current_duty >> 5))
#ENDIF
current_duty = next_duty
output_duty = integer(next_duty >> 5)
#IF FADE-IN
if(output_duty > max_duty)
    output = max_duty
else
    output = output_duty
#ELIF FADE-OUT
if(output_duty < min_duty)
    output = min_duty
else
    output = output_duty
#ENDIF
    
```

$$t_{\text{FADE}} = t_{\text{SLEW\_RATE}} \times \sum_{n = \text{PWM}_{\text{START}}}^{\text{PWM}_{\text{END}}} \text{REPETATION}(n) \quad (5)$$

where:

- $t_{\text{FADE}}$  is the total fading (fade-in or fade-out) time as depicted in [Figure 7-6](#).
- $t_{\text{SLEW\_RATE}}$  is the fade-in or fade-out time slice in seconds/step.
- SLEW\_RATE is the FADE-IN SLEW-RATE or FADE-OUT SLEW-RATE, as specified in [Table 7-4](#).
- $n$  is the CODE corresponding to the PWM duty cycle, as specified in [Table 7-5](#).
- $\text{PWM}_{\text{START}}$  is the PWM-MIN value for fade-in and PWM-MAX value for fade-out, as specified in [Table 7-4](#).
- $\text{PWM}_{\text{END}}$  is the PWM-MAX value for fade-in and PWM-MIN value for fade-out, as specified in [Table 7-4](#).
- REPETATION( $n$ ) is the REPETITION(CODE) value specified for every PWM code, as specified in [Table 7-5](#).

[Table 7-6](#) shows the list of register settings done for the device configuration.



**表 7-4. Fade-In Fade-Out Configuration**

REGISTER FIELD NAME	LOCATION	ADDRESS [BITS]	DEFAULT VALUE	DESCRIPTION
PWM-MAX	SRAM, NVM	0x21 [6:0]	0xF7	Maximum PWM duty cycle
PWM-MIN	SRAM, NVM	0x20 [6:0]	0x00	Minimum PWM duty cycle
FADE-IN SLEW-RATE	SRAM, NVM	0x23 [15:0]	0x0000	See 式 4 and 式 5
FADE-OUT SLEW-RATE	SRAM, NVM	0x26 [15:0]	0x0000	See 式 4 and 式 5
CH0-DELAY	SRAM, NVM	0x24 [15:0]	0x0000	Delay for PWM0. See 式 7
COM-DELAY	SRAM, NVM	0x25 [15:0]	0x0000	Delay for PWM1. See 式 7
PWM-FREQ	SRAM, NVM	0x22 [11:7]	0x00	Frequency selection as per 表 7-7

**表 7-5. Fade-In Steps**

CODE	REPETATION (CODE)	CODE	REPETATION (CODE)	CODE	REPETATION (CODE)	CODE	REPETATION (CODE)	CODE	REPETATION (CODE)
1	32	17	2	33	1	54	1	88	1
2	16	18	2	34	1	55	1	90	1
3	11	19	2	35	1	57	1	93	1
4	8	20	1	36	1	59	1	96	1
5	7	21	2	37	1	61	1	99	1
6	5	22	1	38	1	62	1	102	1
7	5	23	2	39	1	64	1	105	1
8	4	24	1	41	1	66	1	109	1
9	3	25	1	42	1	68	1	112	1
10	4	26	2	43	1	71	1	116	1
11	3	27	1	45	1	73	1	119	1
12	2	28	1	46	1	75	1	123	1
13	3	29	1	47	1	77	1	127	1
14	2	30	1	49	1	80	1	—	—
15	2	31	1	50	1	82	1	—	—
16	2	32	1	52	1	85	1	—	—

**表 7-6. DAC43901-Q1 Register Settings**

REGISTER NAME	ADDRESS	DEFAULT VALUE
COMMON-CONFIG	0x1F	0x13FF
DAC-0-VOOUT-CMP-CONFIG	0x15	0x0407
STATE-MACHINE-CONFIG0	0x27	0x0003

**表 7-7. PWM Frequency Configuration**

SRAM LOCATION	PWM-FREQ	PWM FREQUENCY (kHz)	DUTY CYCLE (%) FOR CODE 1	DUTY CYCLE (%) FOR CODE 126
PWM-FREQ (0x22 [11:7])	0	Invalid	N/A	N/A
	1	48.828	4.88	95.12
	2	24.414	2.44	97.56
	3	16.276	1.63	98.37
	4	12.207	1.22	98.44
	5	8.138	0.81	98.44
	6	6.104	0.78	98.44
	7	3.052	0.78	98.44
	8	2.035	0.78	98.44
	9	1.526	0.78	98.44
	10	1.221	0.78	98.44
	11	1.017	0.78	98.44
	12	0.872	0.78	98.44
	13	0.763	0.78	98.44
	14	0.678	0.78	98.44
	15	0.610	0.78	98.44
	16	0.555	0.78	98.44
	17	0.509	0.78	98.44
	18	0.470	0.78	98.44
	19	0.436	0.78	98.44
	20	0.407	0.78	98.44
	21	0.381	0.78	98.44
	22	0.359	0.78	98.44
	23	0.339	0.78	98.44
	24	0.321	0.78	98.44
	25	0.305	0.78	98.44
	26	0.291	0.78	98.44
	27	0.277	0.78	98.44
	28	0.265	0.78	98.44
	29	0.254	0.78	98.44
	30	0.244	0.78	98.44
	31	0.218	0.78	98.44

The duty cycle of the PWM is proportional to the 7-bit code, 0d to 126d. As 表 7-8 shows, the code 127d corresponds to 100% duty cycle. The duty cycle 99.22% (127d/128d) is skipped to achieve 100% duty cycle using a 7-bit code. The PWM duty-cycle setting is done by the state machine and is not exposed to the user.

**表 7-8. PWM Duty Cycle Setting**

CODE	DUTY CYCLE	DESCRIPTION
0	0%	Always 0
1	0.78%	Minimum linear duty cycle
x	(x/128)%	x is the code between 2d and 125d, both included
126	98.44%	Maximum linear duty cycle
127	100%	Always 1. The duty cycle 99.22% (127d/128d) is skipped.

### 7.4.3 Sequential Turn-Indicator Animation Mode

The DAC43901-Q1 and DAC43902-Q1 support state-machines preconfigured for sequential turn-indicator animation, as shown in 図 7-7, 図 7-8, and 図 7-9. The fade-in is done logarithmically. 表 7-9 shows the pin multiplexing of the PWM channels and the programming interface. The PWM outputs are available on the digital pins in the standalone mode. The device goes into standalone mode when the VREF/MODE pin is pulled high. In this mode, the programming interface is disabled. The device functions per the configurations in the NVM. The digital programming interface (I<sup>2</sup>C and SPI) pins are open-drain outputs and must be pulled up to function as PWM outputs. Pulling the VREF/MODE pin low brings the device into programming mode. When the PWM output mode is enabled, all four programming interface pins act as PWM outputs, even if not used. Partial selection is not possible. The PWM duty-cycle resolution is 7 bits. The animation pattern is triggered by an external signal applied to the TRIG-IN pin or by controlling the power supply to the smart DAC. When more than four channels are required, multiple devices can be cascaded by daisy-chaining the TRIG-OUT (DAC43902-Q1 only) and the TRIG-IN pins, as shown in 図 7-8. In some cases, the LED modules are in separate subsystems and there is no way to daisy-chain the device; the only common connection is the power. 図 7-9 shows a configuration wherein the delay for the first channel in the following devices is configured to match the cumulative delay of all the channels in the predecessor devices. The timing diagram of the sequential turn-indicator animation is shown in 図 7-10. The fade-in timing configurations are done as described in セクション 7.4.2. The PWM frequency is configured as per 表 7-7.

表 7-9. Animation Pin Mapping

ANIMATION INTERFACE	MULTIPLEXED PROGRAMMING PIN	PIN NUMBER
PWM0	SDA/SCLK	8
PWM1	A0/SDI	7
PWM2 (DAC43902-Q1 only)	SCL/SYNC	6
PWM3 (DAC43902-Q1 only)	NC/SDO	5
TRIG-IN	TRIG-IN	1
TRIG-OUT (DAC43902-Q1 only)	TRIG-OUT	11

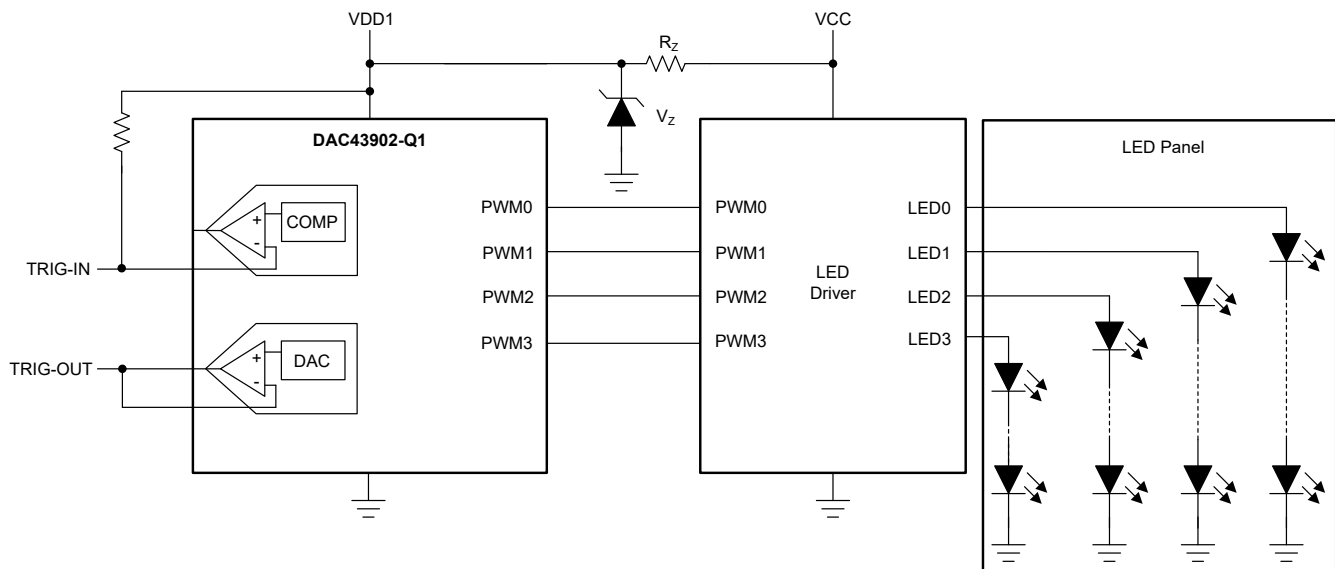


図 7-7. Sequential Turn-Indicator Animation

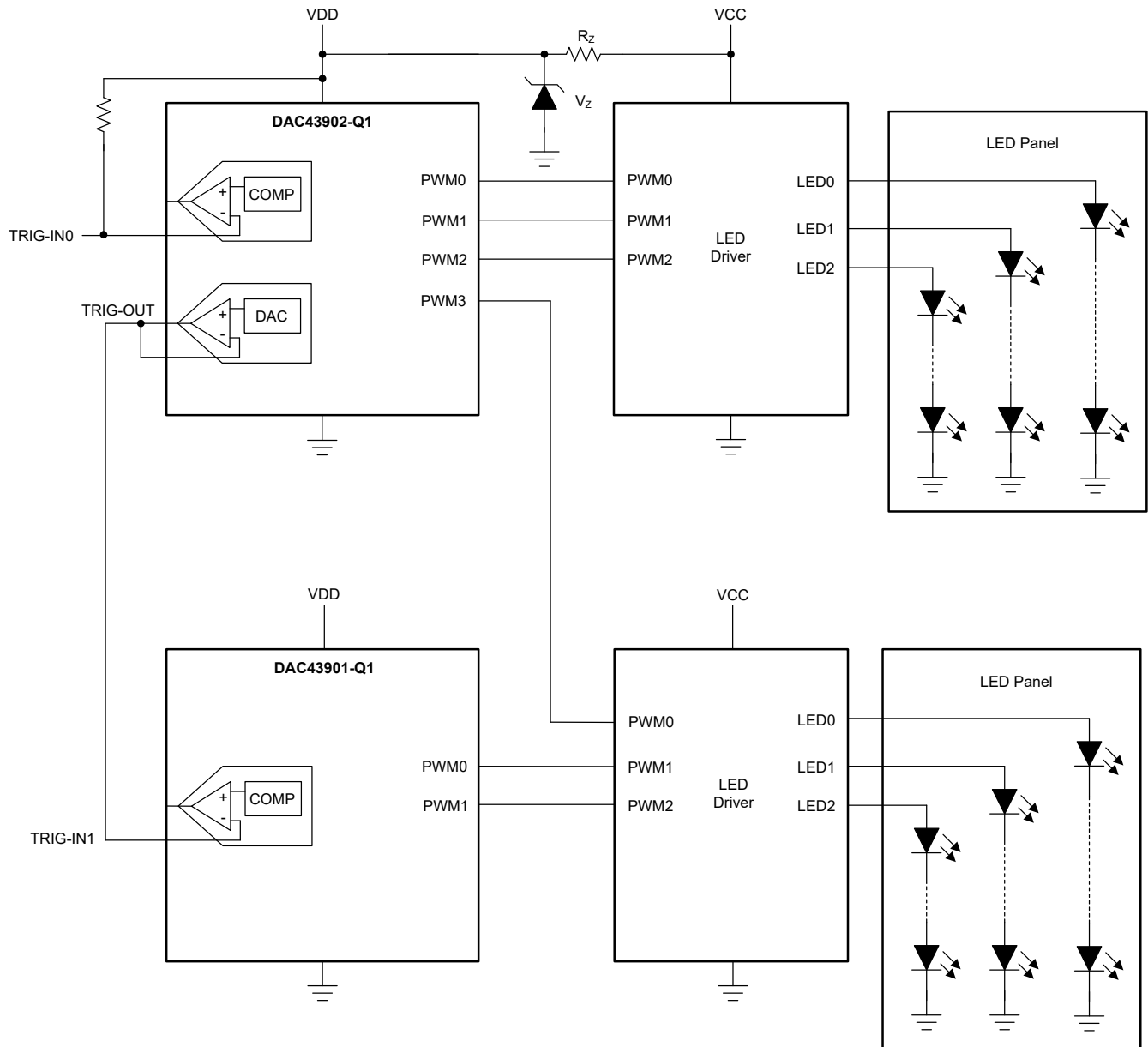
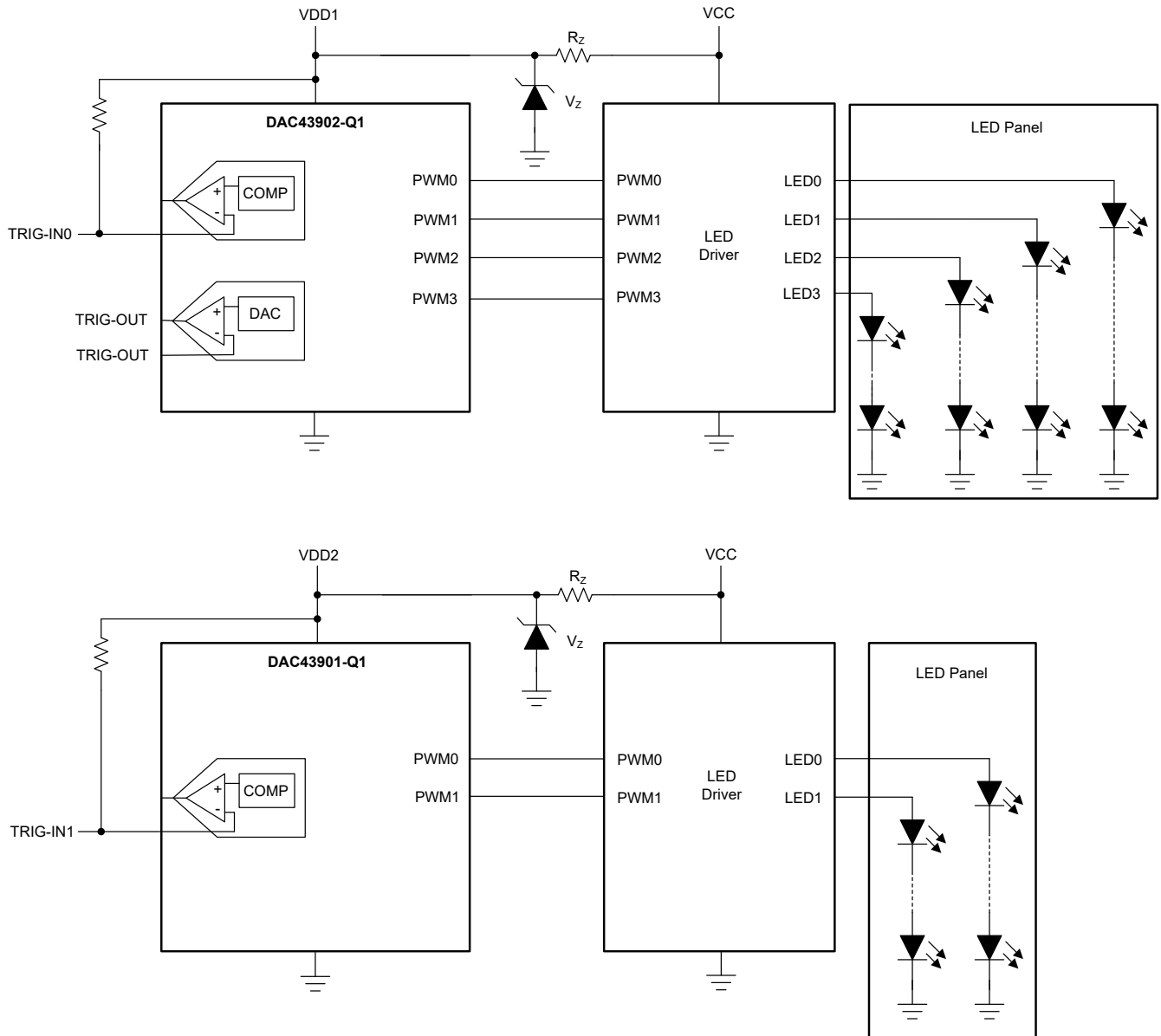
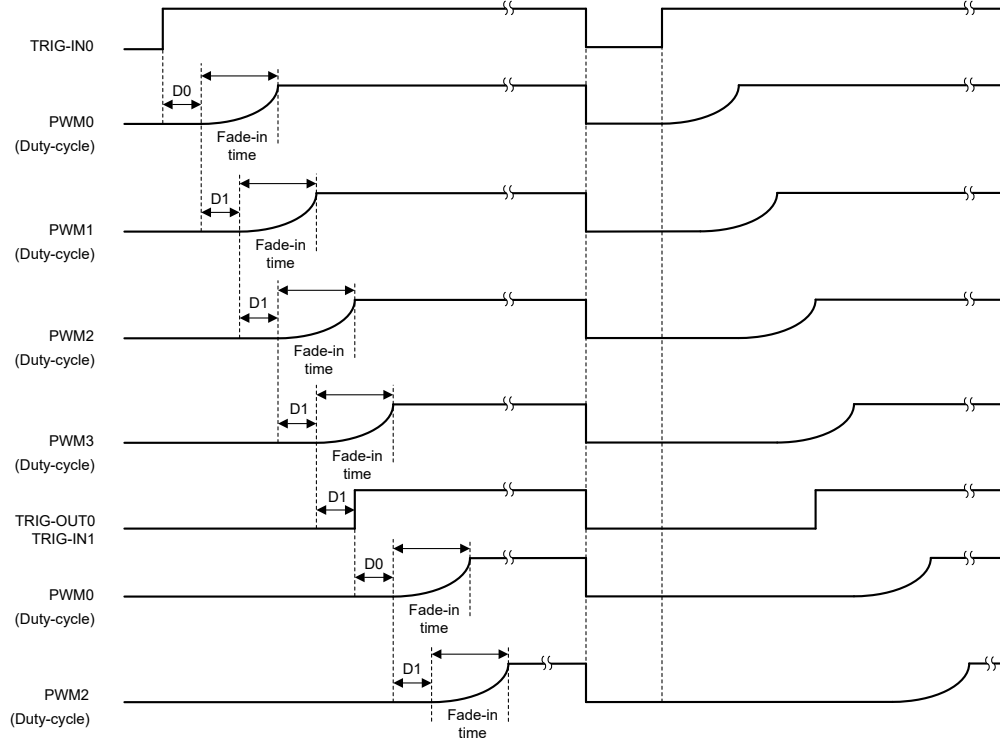


図 7-8. Sequential Turn-Indicator Animation With Cascaded Devices



**図 7-9. Sequential Turn-Indicator Animation Using Unconnected LED Modules**



D0: Delay for channel 0  
 D1: Delay for rest of the channels

**図 7-10. Sequential Turn-Indicator Animation Timing Diagram**

Each PWM channel can be started after a delay with respect to the previous respective channel. [図 7-10](#) shows that there is a separate delay for the first channel, PWM0, and then a common delay for other channels, including the TRIG-OUT pin. [式 6](#) gives the SLEW-RATE calculation for DAC43902-Q1. [式 5](#) gives the calculation for total fade-in time. The channel delays are a function of the SLEW-RATE, as given in [式 4](#) and the delay settings, CH0-DELAY or COM-DELAY. [式 7](#) is used to calculate the delay. CH0-DELAY defines the delay before starting the fade-in operation for PWM0, and COM-DELAY defines the delay before starting the fade-in for all other PWM channels, including the delay before toggling TRIG-OUT. The delay applies even when the fade-in is disabled by writing 0 for FADE-IN-RATE. In this case, a predefined delay setting of 256 is considered. The DAC43902-Q1 does not have the fade-out function.

$$t_{\text{SLEW}}(\mu\text{s}) = 2.4 \times \text{SLEW\_RATE} + 5.6 \quad (6)$$

where:

- $t_{\text{SLEW\_RATE}}$  is the fade-in unit time in microseconds/step.
- SLEW\_RATE is the FADE-IN-RATE as specified in [表 7-10](#) for DAC43902-Q1.

$$t_{\text{DELAY}} = \text{DELAY} \times t_{\text{SLEW}} \quad (7)$$

where:

- $t_{\text{DELAY}}$  is the delay before the fade-in operation for each channel in seconds.
- DELAY is the CH0-DELAY or COM-DELAY as specified in [表 7-10](#) for DAC43902-Q1 or as specified in [表 7-4](#) for DAC43901-Q1.
- $t_{\text{SLEW}}$  is the unit slew rate calculated as per [式 4](#).

**表 7-10. Fade-In Configuration**

PARAMETER	LOCATION	ADDRESS [BITS]	DEFAULT VALUE	DESCRIPTION
PWM-MAX	SRAM, NVM	0x21 [15:9]	0xF7	Maximum PWM duty cycle.
PWM-MIN	SRAM, NVM	0x20 [15:9]	0x00	Minimum PWM duty cycle.
FADE-IN-RATE	SRAM, NVM	0x23 [15:0]	0x0000	See <a href="#">式 4</a> , <a href="#">式 6</a> , and <a href="#">式 5</a> .
CH0-DELAY	SRAM, NVM	0x24 [15:0]	0x0000	Delay for PWM0.
COM-DELAY	SRAM, NVM	0x25 [15:0]	0x0000	Delay for all channels and TRIGGER-OUT except PWM0.
PWM-FREQ	SRAM, NVM	0x22 [11:7]	0x00	Frequency selection as per <a href="#">表 7-7</a> .

[表 7-11](#) shows the list of register settings done for the device configuration.

**表 7-11. DAC43902-Q1 Register Settings**

REGISTER NAME	ADDRESS	DEFAULT VALUE
COMMON-CONFIG	0x1F	0x13F9
DAC-0-VOOUT-CMP-CONFIG	0x15	0x0407
DAC-1-VOOUT-CMP-CONFIG	0x03	0x0400
STATE-MACHINE-CONFIG0	0x27	0x0003

## 7.5 Programming

### 7.5.1 SPI Programming Mode

An SPI access cycle for DAC4390x-Q1 is initiated by asserting the  $\overline{\text{SYNC}}$  pin low. The serial clock, SCLK, can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. The SPI frame for DAC4390x-Q1 is 24 bits long. Therefore, the  $\overline{\text{SYNC}}$  pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the  $\overline{\text{SYNC}}$  pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. By default, the SDO pin is not enabled (three-wire SPI). In the three-wire SPI mode, if the access cycle contains more than the minimum clock edges, only the first 24 bits are used by the device. When  $\overline{\text{SYNC}}$  is high, the SCLK and SDI signals are blocked, and SDO becomes Hi-Z to allow data readback from other devices connected on the bus.

表 7-12 and 図 7-11 describe the format for the 24-bit SPI access cycle. The first byte input to SDI is the instruction cycle. The instruction cycle identifies the request as a read or write command and the 7-bit address that is to be accessed. The last 16 bits in the cycle form the data cycle.

表 7-12. SPI Read/Write Access Cycle

BIT	FIELD	DESCRIPTION
23	R/ $\overline{\text{W}}$	Identifies the communication as a read or write command to the address register: R/ $\overline{\text{W}}$ = 0 sets a write operation. R/ $\overline{\text{W}}$ = 1 sets a read operation
22-16	A[6:0]	Register address: specifies the register to be accessed during the read or write operation
15-0	DI[15:0]	Data cycle bits: If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are <i>don't care</i> values.

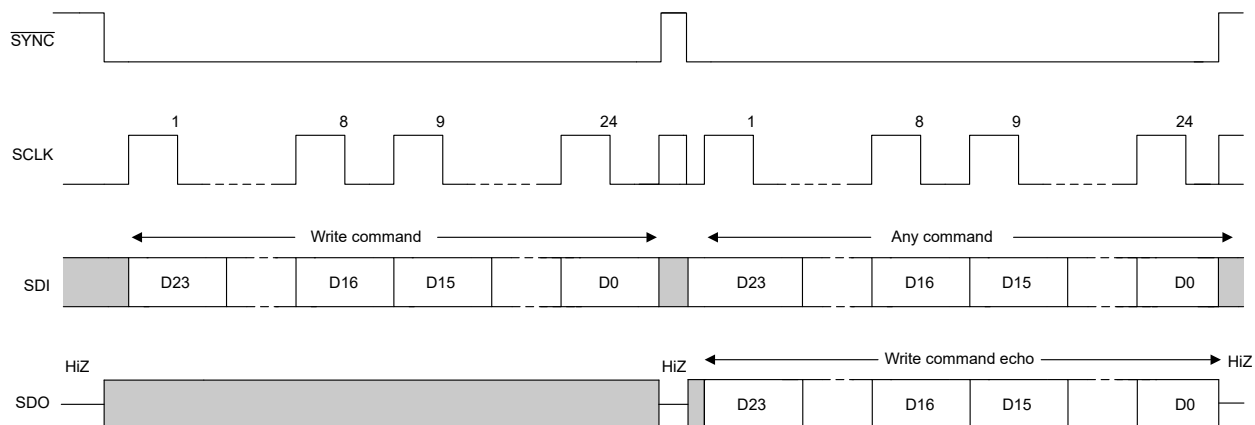


図 7-11. SPI Write Cycle

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit in the INTERFACE-CONFIG register. This configuration is called four-wire SPI. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. The output data format is shown in 表 7-13 and 図 7-12. Data are clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit (see 図 6-3).

表 7-13. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	R/ $\overline{\text{W}}$	Echo R/ $\overline{\text{W}}$ from previous access cycle
22-16	A[6:0]	Echo register address from previous access cycle
15-0	DI[15:0]	Readback data requested on previous access cycle



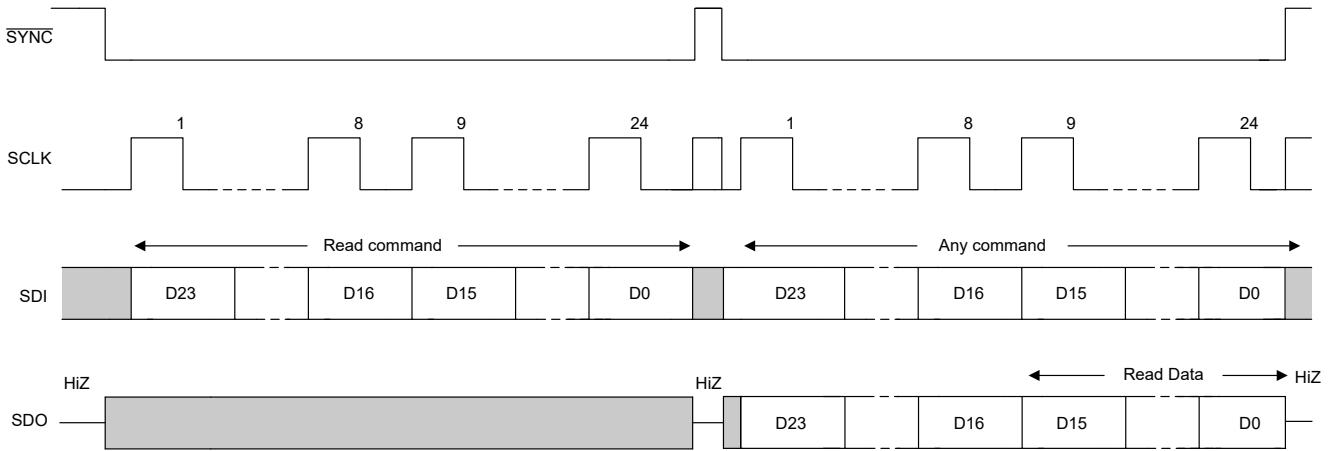


図 7-12. SPI Read Cycle

The daisy-chain operation is also enabled with the SDO pin. In daisy-chain mode, multiple devices are connected in a *chain* with the SDO pin of one device is connected to SDI pin of the following device, as shown in 図 7-13. The SPI host drives the SDI pin of the first device in the chain. The SDO pin of the last device in the chain is connected to the POCI pin of the SPI host. In four-wire SPI mode, if the access cycle contains multiples of 24 clock edges, only the last 24 bits are used by the device first device in the chain. If the access cycle contains clock edges that are not in multiples of 24, the SPI packet is ignored by the device. 図 7-14 describes the packet format for the daisy-chain write cycle.

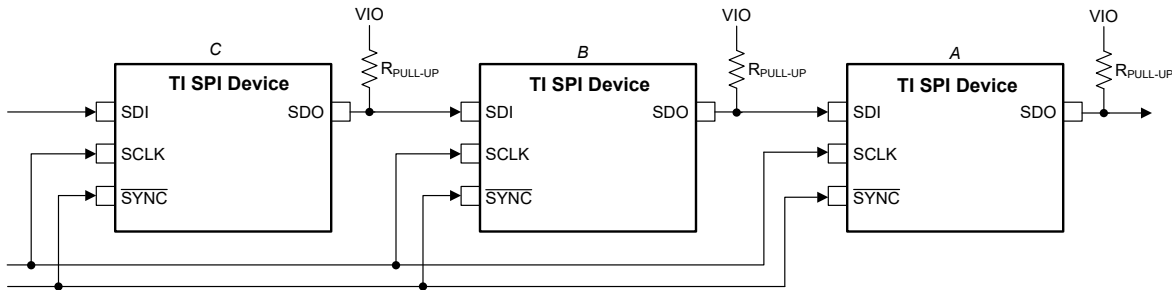


図 7-13. SPI Daisy-Chain Connection

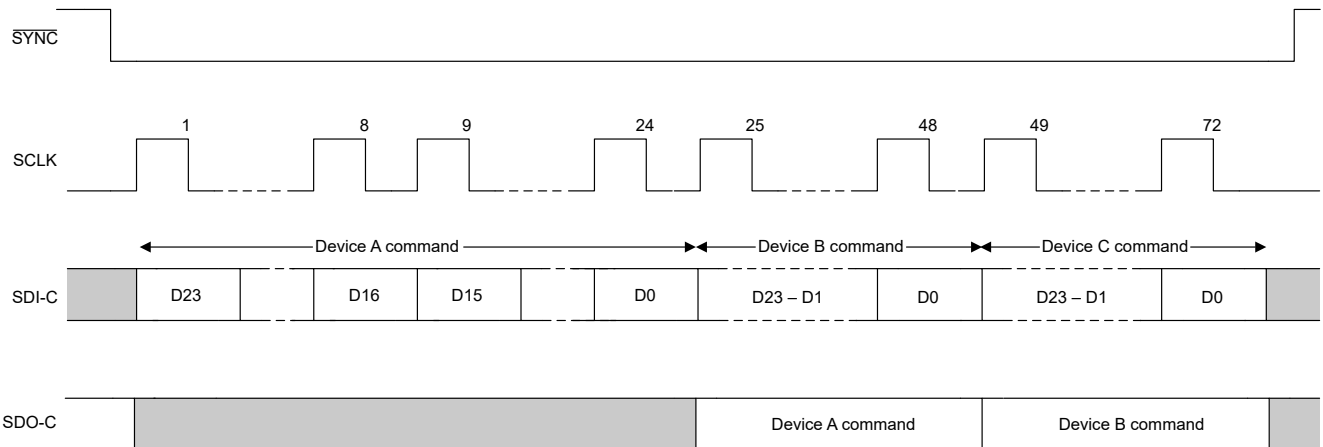


図 7-14. SPI Daisy-Chain Write Cycle

### 7.5.2 I<sup>2</sup>C Programming Mode

The DAC4390x-Q1 devices have a 2-wire serial interface (SCL and SDA), and one address pin (A0), as shown in the pin diagram in the *Pin Configuration and Functions* section. The I<sup>2</sup>C bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through the open drain I/O pins, SDA and SCL.

The I<sup>2</sup>C specification states that the device that controls communication is called a *controller*, and the devices that are controlled by the controller are called *targets*. The controller generates the SCL signal. The controller also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the controller. The controller on an I<sup>2</sup>C bus is typically a microcontroller or digital signal processor (DSP). The DAC4390x-Q1 family operates as a target on the I<sup>2</sup>C bus. A target acknowledges controller commands, and upon controller control, receives or transmits data.

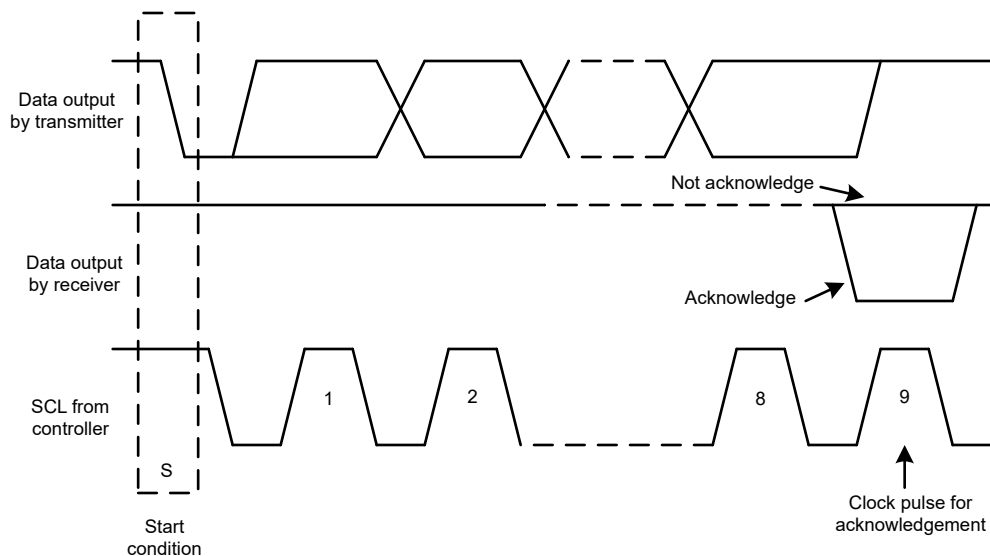
Typically, the DAC4390x-Q1 family operates as a target receiver. A controller writes to the DAC4390x-Q1, a target receiver. However, if a controller requires the DAC4390x-Q1 internal register data, the DAC4390x-Q1 operate as a target transmitter. In this case, the controller reads from the DAC4390x-Q1. According to I<sup>2</sup>C terminology, read and write refer to the controller.

The DAC4390x-Q1 family supports the following data transfer modes:

- Standard mode (100Kbps)
- Fast mode (400Kbps)
- Fast mode plus (1.0Mbps)

The data transfer protocol for standard and fast modes is exactly the same; therefore, both modes are referred to as *F/S-mode* in this document. The fast mode plus protocol is supported in terms of data transfer speed, but not output current. The low-level output current is 3 mA; similar to the case of standard and fast modes. The DAC4390x-Q1 family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device: start or repeated start, 0x00, 0x06, stop. The reset is asserted within the device on the rising edge of the ACK bit, following the second byte.

Other than specific timing signals, the I<sup>2</sup>C interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. An acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle, as shown in [Figure 7-15](#).

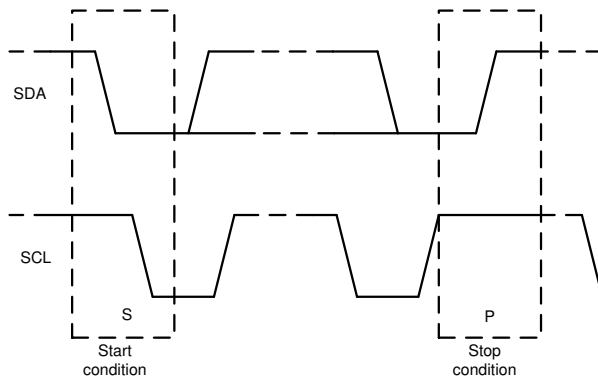


**Figure 7-15. Acknowledge and Not Acknowledge on the I<sup>2</sup>C Bus**

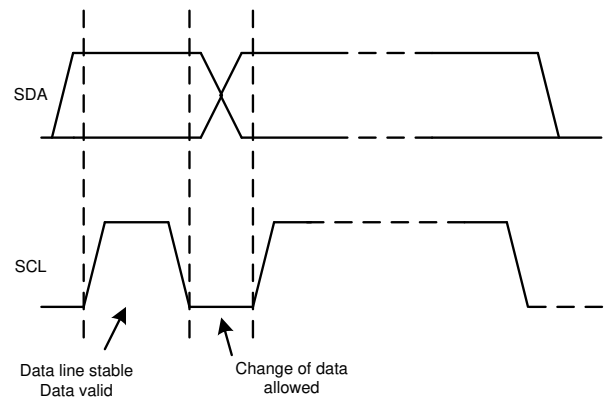
### 7.5.2.1 F/S Mode Protocol

The following steps explain a complete transaction in F/S mode.

1. The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in [Figure 7-16](#). All I<sup>2</sup>C-compatible devices recognize a start condition.
2. The controller then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit ( $R/\bar{W}$ ) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in [Figure 7-17](#). All devices recognize the address sent by the controller and compare the address to the respective internal fixed address. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in [Figure 7-15](#). When the controller detects this acknowledge, the communication link with a target has been established.
3. The controller generates further SCL cycles to transmit ( $R/\bar{W}$  bit 0) or receive ( $R/\bar{W}$  bit 1) data to the target. In either case, the receiver must acknowledge the data sent by the transmitter. The acknowledge signal can be generated by the controller or by the target, depending on which is the receiver. The 9-bit valid data sequences consists of eight data bits and one acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high, as shown in [Figure 7-16](#). This action releases the bus and stops the communication link with the addressed target. All I<sup>2</sup>C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all target devices then wait for a start condition followed by a matching address.



**Figure 7-16. Start and Stop Conditions**



**Figure 7-17. Bit Transfer on the I<sup>2</sup>C Bus**

### 7.5.2.2 I<sup>2</sup>C Update Sequence

For a single update, the DAC4390x-Q1 require a start condition, a valid I<sup>2</sup>C address byte, a command byte, and two data bytes, as listed in 表 7-14.

表 7-14. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte セクション 7.5.2.2.1				Command byte セクション 7.5.2.2.2				Data byte - MSDB				Data byte - LSDB			
DB [31:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DAC4390x-Q1 family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in 図 7-18. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I<sup>2</sup>C address byte selects the DAC4390x-Q1.

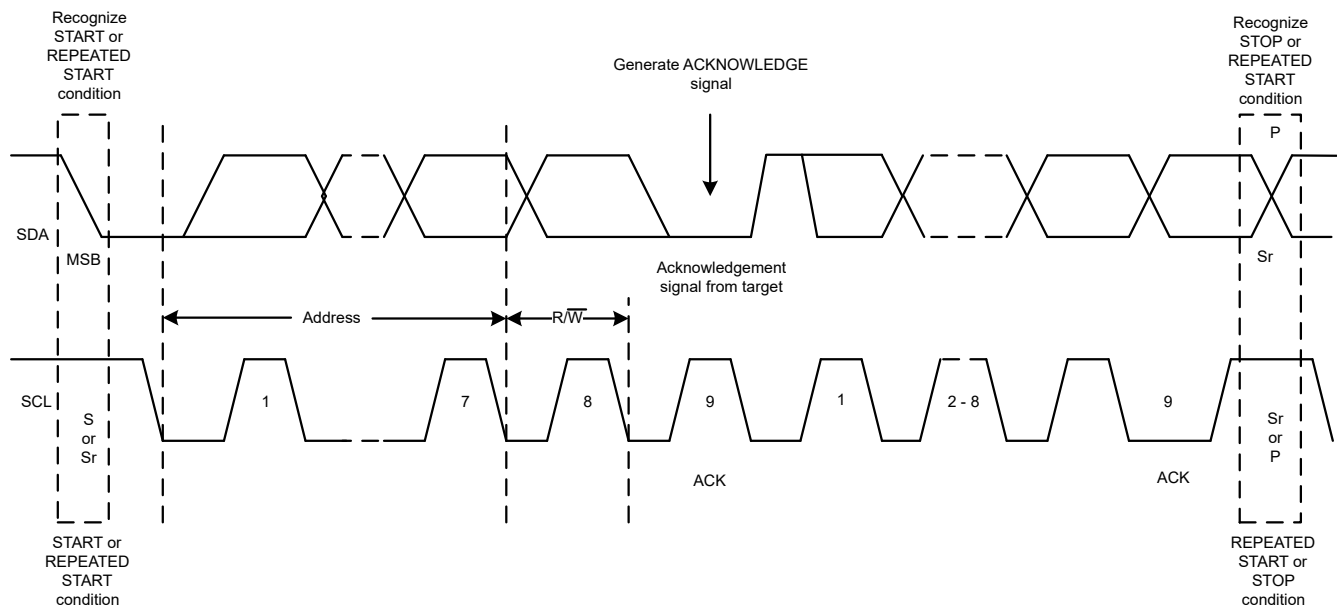


図 7-18. I<sup>2</sup>C Bus Protocol

The command byte sets the operating mode of the selected DAC4390x-Q1 device. For a data update to occur when the operating mode is selected by this byte, the DAC4390x-Q1 device must receive two data bytes: the most significant data byte (MSDB) and least significant data byte (LSDB). The DAC4390x-Q1 device performs an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 10 kSPS. Using fast mode plus (clock = 1 MHz), the maximum DAC update rate is limited to 25 kSPS. When a stop condition is received, the DAC4390x-Q1 device releases the I<sup>2</sup>C bus and awaits a new start condition.

### 7.5.2.2.1 Address Byte

The address byte, as shown in 表 7-15, is the first byte received from the controller device following the start condition. The first four bits (MSBs) of the address are factory preset to 1001. The next three bits of the address are controlled by the A0 pin. The A0 pin input can be connected to VDD, AGND, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin, and consequently responds to that particular address according to 表 7-16.

表 7-15. Address Byte

COMMENT	MSB							LSB
	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
—								R/W
General address	1	0	0	1	See 表 7-16 (target address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

表 7-16. Address Format

TARGET ADDRESS	A0 PIN
000	AGND
001	VDD
010	SDA
011	SCL

The DAC4390x-Q1 supports broadcast addressing, which is used for synchronously updating or powering down multiple DAC4390x-Q1 devices. When the broadcast address is used, the DAC4390x-Q1 responds regardless of the address pin state. Broadcast is supported only in write mode.

### 7.5.2.2.2 Command Byte

The *Register Names* table in the *Register Map* section lists the command byte in the ADDRESS column.

### 7.5.2.3 I<sup>2</sup>C Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a target address and the R/W bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the target address and the R/W bit set to 1 for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The controller must acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

The broadcast address cannot be used for reading.

表 7-17. Read Sequence

S	MSB	...	R/W (0)	ACK	MSB	...	LSB	ACK	Sr	MSB	...	R/W (1)	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
	ADDRESS BYTE セクション 7.5.2.2.1				COMMAND BYTE セクション 7.5.2.2.2				Sr	ADDRESS BYTE セクション 7.5.2.2.1				MSDB				LSDB			
	From Controller			Target	From Controller			Target		From Controller			Target	From Target			Controller	From Target			Controller

## 7.6 Register Maps

表 7-18. Register Map

REGISTER	MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOP	NOP															
DAC-X-VOUT-CMP-CONFIG	X		VOUT-GAIN-x				X				CMP-x-OD-EN	CMP-x-OUT-EN	CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN	
COMMON-CONFIG	RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-0		RESERVED						VOUT-PDN-1		RESERVED	
COMMON-TRIGGER	DEV-UNLOCK				RESET				RESERVED						NVM-PROG	NVM-RELOAD
COMMON-PWM-TRIG	RESERVED			START-FUNCTION-A	RESERVED			START-FUNCTION-B	RESERVED			START-FUNCTION-C	RESERVED		START-FUNCTION-D	
GENERAL-STATUS	NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	RESERVED				NVM-BUSY	DEVICE-ID						VERSION-ID		
INTERFACE-CONFIG	X			TIMEOUT-EN	X			RESERVED	X				FSDO-EN	X	SDO-EN	
STATE-MACHINE-CONFIG0	RESERVED												SM-ABORT	SM-START	SM-EN	
SRAM-CONFIG	X								SRAM-ADDR							
SRAM-DATA	SRAM-DATA															

Note: Shaded cells indicate the register bits or fields that are stored in NVM.

Note: X = Don't care.

**表 7-19. Register Names**

I <sup>2</sup> C OR SPI ADDRESS (COMMAND BYTE)	REGISTER NAME	SECTION
00h	NOP	<a href="#">セクション 7.6.1</a>
03h	DAC-1-VOUT-CMP-CONFIG	<a href="#">セクション 7.6.2</a>
15h	DAC-0-VOUT-CMP-CONFIG	<a href="#">セクション 7.6.2</a>
1Fh	COMMON-CONFIG	<a href="#">セクション 7.6.3</a>
20h	COMMON-TRIGGER	<a href="#">セクション 7.6.4</a>
21h	COMMON-PWM-TRIG	<a href="#">セクション 7.6.5</a>
22h	GENERAL-STATUS	<a href="#">セクション 7.6.6</a>
26h	INTERFACE-CONFIG	<a href="#">セクション 7.6.7</a>
27h	STATE-MACHINE-CONFIG0	<a href="#">セクション 7.6.8</a>
2Bh	SRAM-CONFIG	<a href="#">セクション 7.6.9</a>
2Ch	SRAM-DATA	<a href="#">セクション 7.6.10</a>

### 7.6.1 NOP Register (address = 00h) [reset = 0000h]

図 7-19. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
R/W-0h															

表 7-20. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NOP	R/W	0000h	No operation

### 7.6.2 DAC-x-VOUT-CMP-CONFIG Register (address = 15h, 03h)

図 7-20. DAC-x-VOUT-CMP-CONFIG Register (x = 0, 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		VOUT-GAIN-x				X			CMP-x-OD-EN	CMP-x-OUT-EN	CMP-x-HIZ-IN-DIS	CMP-x-INV-EN	CMP-x-EN		
X-0h		R/W-0h				X-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

表 7-21. DAC-x-VOUT-CMP-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12-10	VOUT-GAIN-x	R/W	0h	000: Gain = 1 ×, external reference on VREF/MODE pin 001: Gain = 1 ×, VDD as reference 010: Gain = 1.5 ×, internal reference 011: Gain = 2 ×, internal reference 100: Gain = 3 ×, internal reference 101: Gain = 4 ×, internal reference Others: Invalid
9-5	X	X	0h	Don't care
4	CMP-x-OD-EN	R/W	0	0: Set comparator out pin as push-pull 1: Set comparator out pin as open-drain in comparator mode (CMP-x-EN = 1 and CMP-x-OUT-EN = 1)
3	CMP-x-OUT-EN	R/W	0	0: Generate comparator output but consume internally 1: Bring comparator output to the respective pin
2	CMP-x-HIZ-IN-DIS	R/W	0	0: TRIG-IN input has high-impedance. Input voltage range is limited. 1: TRIG-IN input is connected to resistor divider and has finite impedance. Input voltage range is same as full-scale.
1	CMP-x-INV-EN	R/W	0	0: Don't invert the comparator output 1: Invert the comparator output
0	CMP-x-EN	R/W	0	0: Disable comparator mode 1: Enable comparator mode. Current-output must be in power-down. Voltage-output mode must be enabled.



### 7.6.3 COMMON-CONFIG Register (address = 1Fh)

**図 7-21. COMMON-CONFIG Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	DEV-LOCK	RESERVED	EN-INT-REF	VOUT-PDN-0	RESERVED							VOUT-PDN-1	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-00b	R/W-7Fh							R/W-00b	R/W-1b		

**表 7-22. COMMON-CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0	Always write 0.
14	DEV-LOCK	R/W	0	0: Device not locked. 1: Device locked, the device locks all the registers. To set this bit back to 0 (unlock device), write to the unlock code to the DEV-UNLOCK field in the COMMON-TRIGGER register first, followed by a write to the DEV-LOCK bit as 0.
13	RESERVED	R/W	0	Always write 0.
12	EN-INT-REF	R/W	0	0: Disable internal reference. 1: Enable internal reference. This bit must be set before using internal reference gain settings.
11-10, 2-1	VOUT-PDN-x	R/W	11	00: Power-up channel-x 01: Power-down channel-x with 10 KΩ to AGND 10: Power-down channel-x with 100 KΩ to AGND 11: Power-down channel-x with Hi-Z to AGND
9-3, 0	RESERVED	R/W	1	Always write 1.

### 7.6.4 COMMON-TRIGGER Register (address = 20h) [reset = 0000h]

図 7-22. COMMON-TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV-UNLOCK				RESET				RESERVED				NVM-PROG	NVM-RELOAD		
R/W-0h				R/W-0h				R/W-00h				R/W-0h	R/W-0h		

表 7-23. COMMON-TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	DEV-UNLOCK	R/W	0000	0101: Device unlocking password. To unlock device, write this unlock password first, followed by a write 0 to the DEV-LOCK bit in the COMMON-CONFIG register. Others: Don't care
11-8	RESET	W	0000	1010: POR reset triggered. This bit self-resets. Others: Don't care
7-2	RESERVED	R/W	0	Always write 00h.
1	NVM-PROG	R/W	0	0: NVM write not triggered 1: NVM write triggered. This bit self-resets.
0	NVM-RELOAD	R/W	0	0: NVM reload not triggered 1: Reload data from NVM to register map. This bit self-resets.

### 7.6.5 COMMON-PWM-TRIG Register (address = 21h) [reset = 0000h]

図 7-23. COMMON-PWM-TRIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			START-FUNC-A	RESERVED			START-FUNC-B	RESERVED			START-FUNC-C	RESERVED			START-FUNC-D
W-0h			R/W-0h	W-0h			R/W-0h	W-0h			R/W-0h	W-0h			R/W-0h

表 7-24. COMMON-PWM-TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13, 11-9, 7-5, 3-1	RESERVED	W	0	Always write 0.
12, 8, 4, 0	START-FUNCTION-x	R/W	0	0: Stop PWM generation 1: Invalid. This bit is automatically set by the state machine.

### 7.6.6 GENERAL-STATUS Register (address = 22h) [reset = 00h, DEVICE-ID, VERSION-ID]

図 7-24. GENERAL-STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NVM-CRC-FAIL-INT	NVM-CRC-FAIL-USER	RESERVED					NVM-BUSY	DEVICE-ID					VERSION-ID		
R-0h	R-0h	R-0h					R-0h	R					R-0h		

表 7-25. GENERAL-STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NVM-CRC-FAIL-INT	R	0	0: No CRC error in OTP. 1: Indicates a failure in OTP loading. A software reset or power-cycle can bring the device out of this condition in case of temporary failure.
14	NVM-CRC-FAIL-USER	R	0	0: No CRC error in NVM loading. 1: Indicates a failure in NVM loading. The register settings are corrupted. The device allows all operations during this error condition. Reprogram the NVM to get original state. A software reset brings the device out of this error condition.
13	X	R	0	Don't care
8	NVM-BUSY	R	0	0: NVM is available for read and write. 1: NVM is not available for read or write.
7-2	DEVICE-ID	R	DAC43901-Q1: 16h DAC43902-Q1: 15h	Device identifier
1-0	VERSION-ID	R	00	Version identifier

### 7.6.7 INTERFACE-CONFIG Register (address = 26h) [reset = 0000h]

図 7-25. INTERFACE-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X		TIMEOUT-EN	RESERVED									FSDO-EN	X	SDO-EN	
X-0h		R/W-0h	R/W-0h									R/W-0h	X-0h	R/W-0h	

表 7-26. INTERFACE-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	X	X	0h	Don't care
12	TIMEOUT-EN	R/W	0	0: I <sup>2</sup> C timeout disabled 1: I <sup>2</sup> C timeout enabled
11-9	RESERVED	R/W	0h	Always write 0h
2	FSDO-EN	R/W	0	0: Fast SDO (FSDO) disabled 1: Fast SDO enabled
1	X	X	0	Don't care
0	SDO-EN	R/W	0	0: SDO disabled 1: SDO enabled.

### 7.6.8 STATE-MACHINE-CONFIG0 Register (address = 27h) [reset = 0003h]

図 7-26. STATE-MACHINE-CONFIG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												SM-ABORT	SM-START	SM-EN	
R/W-0h												R/W-0h	R/W-1	R/W-1	

表 7-27. STATE-MACHINE-CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0000h	Always write 0.
2	SM-ABORT	R/W	0	0: State machine not aborted. 1: State machine aborted.
1	SM-START	R/W	1	0: State machine stopped. 1: State machine started. The state machine must be enabled using the SM-EN bit.
0	SM-EN	R/W	1	0: State machine disabled. 1: State machine enabled.

### 7.6.9 SRAM-CONFIG Register (address = 2Bh) [reset = 0000h]

図 7-27. SRAM-CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								SRAM-ADDR							
X-00h								R/W-00h							

表 7-28. SRAM-CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	X	X	00h	Don't care
7-0	SRAM-ADDR	R/W	00h	8-bit SRAM address. Writing to this register field configures the SRAM address to be accessed next. This address automatically increments after a write to the SRAM.

### 7.6.10 SRAM-DATA Register (address = 2Ch) [reset = 0000h]

図 7-28. SRAM-DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM-DATA															
R/W-0000h															

表 7-29. SRAM-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SRAM-DATA	R/W	0000h	16-bit SRAM data. Data are written to or read from the address configured in the SRAM-CONFIG register.

## 8 Application and Implementation

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### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Application Information

The DAC4390x-Q1 are a family of smart DACs that provide PWM-based logarithmic dimming. The DAC43902-Q1 provides four PWM outputs with configurable logarithmic fade-in time, and delays between each channel that can be used to create a sequential pattern for automotive turn-indicator lights. The DAC43901-Q1 provides two PWM outputs with a configurable fade-in and fade-out time applicable for automotive interior and exterior lighting. Both devices support an active-high GPI trigger to start the fade in of the PWM outputs. The DAC43902-Q1 also has a trigger output that can be used to cascade multiple DAC43902-Q1 devices. The PWM outputs are on the digital interface pins of the device. All the digital outputs are open drain; use external pullup resistors on these pins. The interface protocol is detected at power on, and the device locks to the protocol as long as VDD is on. In I<sup>2</sup>C mode, when allocating the I<sup>2</sup>C addresses in the system, consider the broadcast address as well. The I<sup>2</sup>C timeout can be enabled for robustness. SPI mode is three-wire by default. After the configuration is initially programmed, the MODE pin of the device is pulled high to enable the PWM outputs on the digital pins. The NVM available in these devices can be used to store the necessary configuration settings so that the devices can work in standalone mode without the need for a processor.

### 8.2 Typical Applications

This section describes the design details of an interior light with fade-in and fade-out using the DAC43901-Q1 and a sequential turn-indicator using the DAC43902-Q1.

## 8.2.1 Sequential Turn Indicator

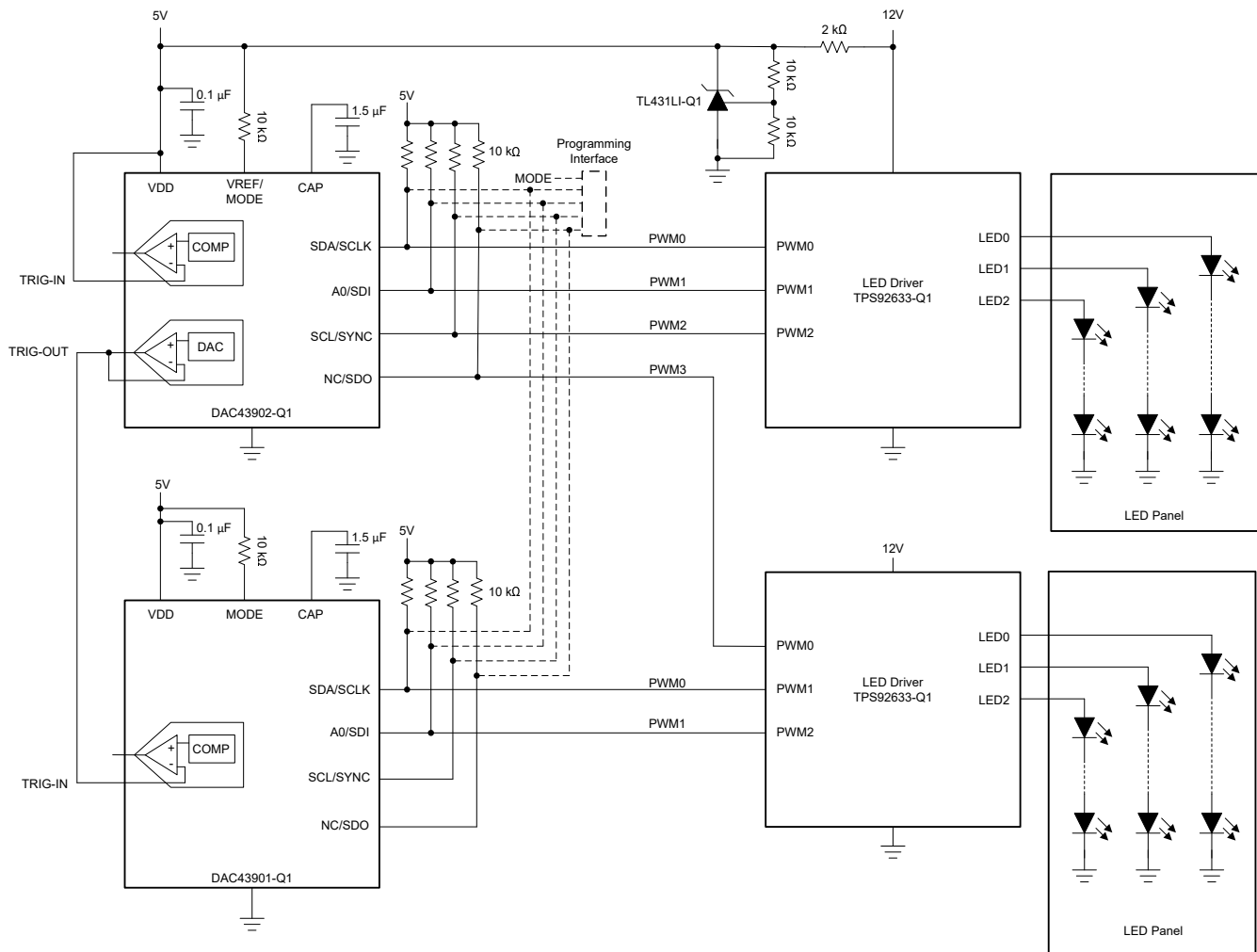


図 8-1. Sequential Turn Indicator

This application example describes a sequential turn indicator for linear perception of LED fade-in fade-out. The DAC43902-Q1 has four PWM output channels with configurable delays between each channel to create a sequential pattern. 図 8-1 shows how to create a sequential pattern with more than four channels by cascading DAC43902-Q1 and DAC43901-Q1 devices.

### 8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Fade-in time	100.2 ms
Channel delay	100.2 ms
PWM frequency	218 Hz
Duty cycle range	0% to 100%

### 8.2.1.2 Detailed Design Procedure

The [TL431LI-Q1](#) adjustable precision shunt regulator can be used to supply the DAC43902-Q1 from the 12-V system voltage. The TL431LI-Q1 has a 2.5-V precision reference. Two 10-k $\Omega$  resistors are used as shown in the simplified figure to regulate the output voltage to 5 V to supply DAC43902-Q1.

In some tail-light designs, the LED driver is supplied by a PWM signal to control the flashing of the LEDs. If this is the case, the trigger input of the DAC43902-Q1 can be tied to VDD. The sequential turn animation begins automatically when VDD is applied.

The state machine in the DAC43902-Q1 is enabled by default; therefore, the PWM outputs are used with the default settings when the VREF/MODE pin is pulled high. To change these default parameters, pull the VREF/MODE pin low to enter programming mode, and write a 0 to the SM-START and SM-EN bits of the STATE-MACHINE-CONFIG0 register to disable the state machine. After the state machine is disabled, program the SRAM parameters and register settings to configure the DAC43902-Q1:

On the rising edge of TRIG-IN, the DAC43902-Q1 PWM outputs fade-in to the 7-bit PWM duty cycle defined in the PWM-MAX parameter located in bits [6:0] of SRAM location 0x21. On the falling edge of TRIG-IN, the PWM outputs jump to the 7-bit PWM duty cycle defined in the PWM-MIN parameter located in bits [6:0] of SRAM location 0x20.

The 5-bit PWM frequency is set in the PWM-FREQ parameter located in bits [11:7] of SRAM location 0x22. The available PWM frequencies are given in [表 7-7](#). The [TPS92633-Q1](#) LED driver used in the example schematic recommends a 200-Hz PWM frequency with a 1% to 100% duty cycle for brightness control. In that case, the maximum frequency setting of 31 can be set in PWM-FREQ to get a PWM output frequency of 218 Hz. Make sure to left shift this value by 7 bits when loading the parameter into the SRAM location.

The four PWM output channels use the same fade-in rate as defined in the FADE-IN SLEW-RATE parameter located in bits [15:0] of SRAM location 0x23. The total fade-in time can be calculated using [式 4](#) and [式 5](#). The SLEW-RATE parameter is used in [式 4](#) to get the  $t_{\text{SLEW\_RATE}}$  in ms/step. For example, if a value of 235 is used for the FADE-IN SLEW-RATE parameter, the resulting  $t_{\text{SLEW\_RATE}}$  is: 0.569 ms/step.

The information given in [表 7-5](#) is used to calculate the total number of duty cycle steps in the fade-in. If PWM-MIN is set to 0 and PWM-MAX is set to 0x7F, a total of 176 steps are needed. [式 5](#) calculates the total fade time,  $t_{\text{FADE}}$  as 100.2 ms.

The delays between each channel are configured in the CH0-DELAY and COM-DELAY parameters in bits [15:0] of SRAM location 0x24 and 0x25, respectively. CH0-DELAY represents the delay between the rising edge of trigger and the start of channel 0. COM-DELAY represents the delay between the start of channel 0 and the start of channel 1, the start of channel 1 and the start of channel 2, and the start of channel 2 and the start of channel 3. The delay time is calculated using [式 7](#). If a delay value of 176 is set in the COM-DELAY parameter, the delay is 100.2 ms.

After all register settings and SRAM parameters are configured, restart the state machine by writing a 1 to the SM-START and SM-EN bits of the STATE-MACHINE-CONFIG0 register. Save these settings to the NVM by writing a 1 to the NVM-PROG bit of the COMMON-TRIGGER register. Pull the VREF/MODE pin high to put the device in standalone mode and enable the PWM outputs on the digital interface pins.

The SRAM parameters and register settings need to be applied to the second DAC43902-Q1 or DAC43901-Q1 in the cascade as well. Apply the TRIG-OUT on channel 1 of the first DAC43902-Q1, to the trigger input on TRIG-IN of the second device.

The pseudocode for getting started with a sequential turn indicator application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (REGISTER ADDRESS)>, <MSB DATA>, <LSB DATA>
//Pull VREF/MODE pin low to enter programming mode
//Disable the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x00
//Power-up DAC channels 0 and 1, disable the internal reference
WRITE COMMON-CONFIG(0x1F), 0x03, 0xF9
//Enable comparator settings for channel 0, and set reference to VDD
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x04, 0x07
//Set the reference for channel 1 to VDD
WRITE DAC-1-VOUT-CMP-CONFIG(0x3), 0x04, 0x00
//Set the comparator threshold to mid-scale
WRITE SRAM-ADDR(0x2B), 0x00, 0x27
WRITE SRAM-DATA(0x2C), 0x80, 0x00
//Set max PWM duty cycle to 100%
WRITE SRAM-ADDR(0x2B), 0x00, 0x21
WRITE SRAM-DATA(0x2C), 0x00, 0x7F
//Set min PWM duty cycle to 0%
WRITE SRAM-ADDR(0x2B), 0x00, 0x20
WRITE SRAM-DATA(0x2C), 0x00, 0x00
//Set PWM frequency to 218Hz
WRITE SRAM-ADDR(0x2B), 0x00, 0x22
WRITE SRAM-DATA(0x2C), 0x0F, 0x80
//Set fade-in time to 100.2 ms
WRITE SRAM-ADDR(0x2B), 0x00, 0x23
WRITE SRAM-DATA(0x2C), 0x00, 0xEB
//Set the CH0 delay to 0
WRITE SRAM-ADDR(0x2B), 0x00, 0x24
WRITE SRAM-DATA(0x2C), 0x00, 0x00
//Set the COM delay to 100.2 ms
WRITE SRAM-ADDR(0x2B), 0x00, 0x25
WRITE SRAM-DATA(0x2C), 0x00, 0xB0
//Enable and start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Save all settings in NVM
WRITE COMMON-TRIGGER(0x20) 0x00, 0x02
//Pull the VREF/MODE pin high to enter standalone mode
```

### 8.2.1.3 Application Curve

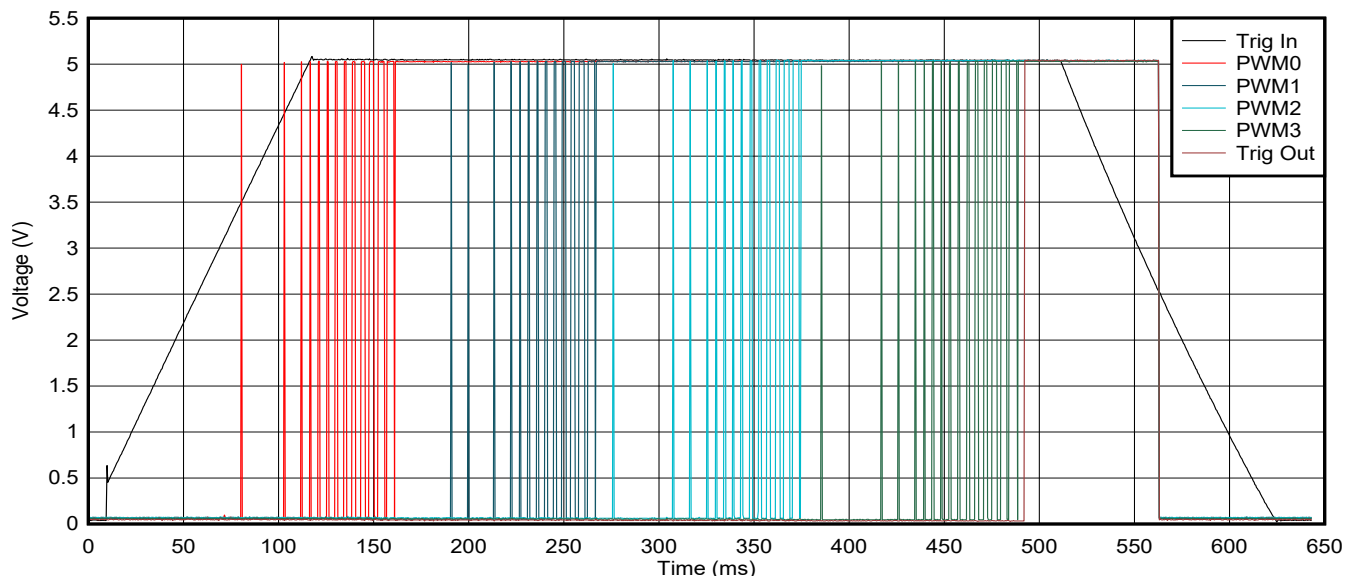


図 8-2. Sequential Turn Indicator Plot



## 8.2.2 Logarithmic Fade-In Fade-Out

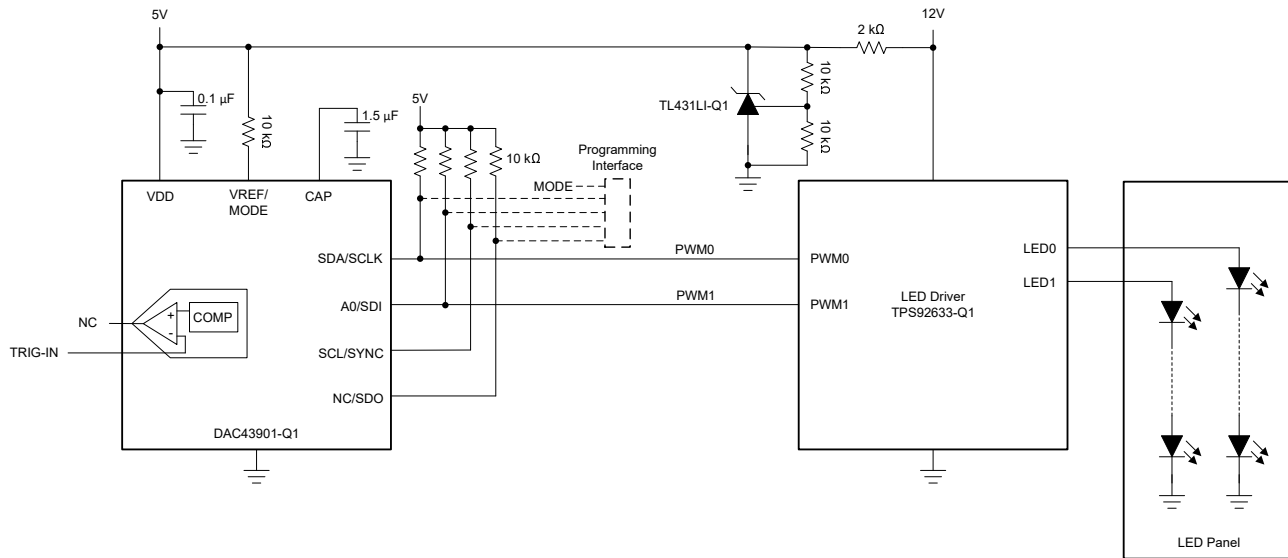


図 8-3. Logarithmic Fade-In Fade-Out

The human eye perceives dimming light logarithmically. For the human eye perceive a linear fade-in or fade-out, the LEDs must fade logarithmically. The DAC43901-Q1 provides two PWM channels that provide simple control of the slew and logarithmic fade-in fade-out for smooth dimming of automotive interior lights, without the need for a microcontroller. The DAC43901-Q1 has one GPI trigger that controls the fade-in fade-out for both channels and a configurable delay between each channel. 図 8-3 shows an example schematic.

### 8.2.2.1 Design Requirements

表 8-2. Design Parameters

PARAMETER	VALUE
Fade-in fade-out time	1 s
Channel delay	500 ms
PWM frequency	218 Hz
Duty cycle range	0% to 100%

### 8.2.2.2 Detailed Design Procedure

The TL431LI-Q1 adjustable, precision shunt regulator can be used to supply the DAC43901-Q1 from the 12-V system voltage. The TL431LI-Q1 has a 2.5-V precision reference. Two 10-kΩ resistors are used, as shown in the simplified figure, to regulate the output voltage to 5 V to supply DAC43901-Q1.

The state machine in DAC43901-Q1 is enabled by default; therefore, the PWM outputs are used with the preset parameters when the VREF/MODE pin is pulled high. To change these default parameters, pull the VREF/MODE pin low to enter programming mode, and write a 0 to the SM-START and SM-EN bits of the STATE-MACHINE-CONFIG0 register to disable the state machine. After the state machine is disabled, program the following SRAM parameters and register settings:

On the rising edge of TRIG-IN, the DAC43901-Q1 PWM outputs fade-in to the 7-bit PWM duty cycle defined in the PWM-MAX parameter located in bits [6:0] of SRAM location 0x21. On the falling edge of TRIG-IN, the PWM outputs fade-out to the 7-bit PWM duty cycle defined in the PWM-MIN parameter located in bits [6:0] of SRAM location 0x20.

The 5-bit PWM frequency is set in the PWM-FREQ parameter located in bits [11:7] of SRAM location 0x22. The available PWM frequencies are given in 表 7-7. The TPS92633-Q1 LED driver used in the example schematic

recommends a 200-Hz PWM frequency with a 1% to 100% duty cycle for brightness control. In that case, the maximum frequency setting of 31 can be set in PWM-FREQ to get a PWM output frequency of 218 Hz. Make sure to left-shift this value by 7 bits when loading the parameter into the SRAM location.

Both PWM output channels use the same fade-in rate and fade-out rate as defined in the FADE-IN SLEW-RATE and FADE-OUT SLEW-RATE parameters located in bits [15:0] of SRAM locations 0x23 and 0x26, respectively. The total fade-in or fade-out time can be calculated using 式 4 and 式 5. The SLEW-RATE parameter is used in 式 4 to get the  $t_{\text{SLEW\_RATE}}$  in ms/step. For example, if a value of 2366 is used for the FADE-IN SLEW-RATE parameter, the resulting  $t_{\text{SLEW\_RATE}}$  is 5.68 ms/step.

The information given in 表 7-5 is used to calculate the total number of duty-cycle steps in the fade-in or fade-out transition. If PWM-MIN is set to 0 and PWM-MAX is set to 0x7F, a total of 176 steps are needed. 式 5 is used to calculate the total fade time,  $t_{\text{FADE}}$  as one second.

The delays between each channel are configured in the CH0-DELAY and COM-DELAY parameters in bits [15:0] of SRAM location 0x24 and 0x25, respectively. CH0-DELAY represents the delay between the rising edge of trigger and the start of channel 0. COM-DELAY represents the delay between the start of channel 0 and the start of channel 1. The delay time is calculated using 式 7. If a delay value of 88 is set in the COM-DELAY parameter, the delay between the start of channel 0 and start of channel 1 is 500 ms.

After all register settings and SRAM parameters are configured, restart the state machine by writing ones to the SM-START and SM-EN bits of the STATE-MACHINE-CONFIG0 register. Save these settings to the NVM by writing a 1 to the NVM-PROG bit of the COMMON-TRIGGER register. Pull the VREF/MODE pin high to put DAC43901-Q1 in standalone mode and enable the PWM outputs on the digital interface pins.

The pseudocode for getting started with a logarithmic fade-in fade-out application is as follows:

```
//SYNTAX: WRITE <REGISTER NAME (REGISTER ADDRESS)>, <MSB DATA>, <LSB DATA>
//Pull VREF/MODE pin low to enter programming mode
//Disable the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x00
//Power-up DAC channel 0, disable the internal reference
WRITE COMMON-CONFIG(0x1F), 0x03, 0xFF
//Enable comparator settings for channel 0, and set reference to VDD
WRITE DAC-0-VOUT-CMP-CONFIG(0x15), 0x04, 0x07
//Set the comparator threshold to mid-scale
WRITE SRAM-ADDR(0x2B), 0x00, 0x27
WRITE SRAM-DATA(0x2C), 0x80, 0x00
//Set max PWM duty cycle to 100%
WRITE SRAM-ADDR(0x2B), 0x00, 0x21
WRITE SRAM-DATA(0x2C), 0x00, 0x7F
//Set min PWM duty cycle to 0%
WRITE SRAM-ADDR(0x2B), 0x00, 0x20
WRITE SRAM-DATA(0x2C), 0x00, 0x00
//Set PWM frequency to 218Hz
WRITE SRAM-ADDR(0x2B), 0x00, 0x22
WRITE SRAM-DATA(0x2C), 0x0F, 0x80
//Set fade-in time to 1 s
WRITE SRAM-ADDR(0x2B), 0x00, 0x23
WRITE SRAM-DATA(0x2C), 0x09, 0x39
//Set fade-out time to 1 s
WRITE SRAM-ADDR(0x2B), 0x00, 0x26
WRITE SRAM-DATA(0x2C), 0x09, 0x3E
//Set the CH0 delay to 0
WRITE SRAM-ADDR(0x2B), 0x00, 0x24
WRITE SRAM-DATA(0x2C), 0x00, 0x00
//Set the COM delay to 500 ms
WRITE SRAM-ADDR(0x2B), 0x00, 0x25
WRITE SRAM-DATA(0x2C), 0x00, 0x58
//Enable and start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Save all settings in NVM
WRITE COMMON-TRIGGER(0x20) 0x00, 0x02
//Pull the VREF/MODE pin high to enter standalone mode
```

### 8.3 Power Supply Recommendations

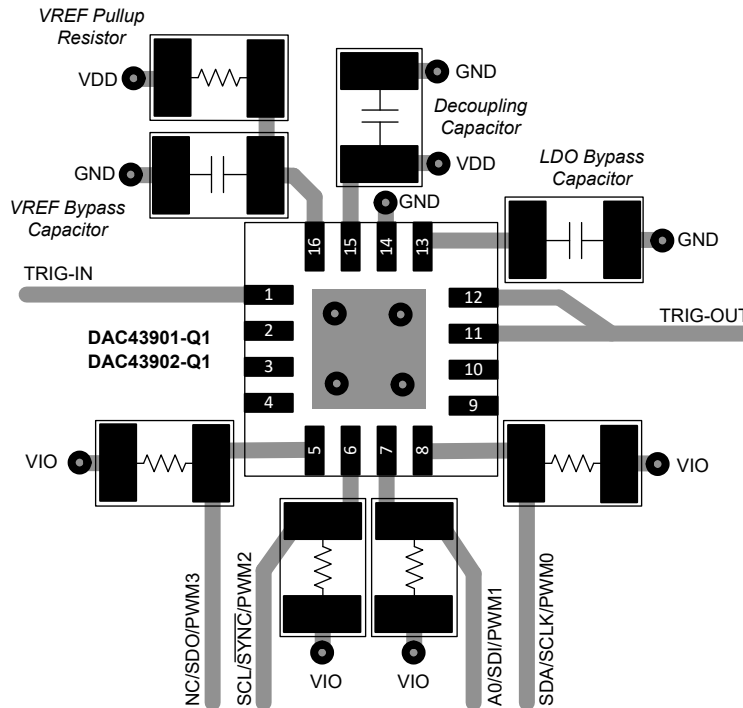
The DAC4390x-Q1 does not require specific power-supply sequencing. These devices require a single power supply,  $V_{DD}$ . However, make sure the external voltage reference is applied after  $V_{DD}$ . Use a 0.1- $\mu\text{F}$  decoupling capacitor for the  $V_{DD}$  pin. Use a bypass capacitor with a value approximately 1.5  $\mu\text{F}$  for the CAP pin.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

The DAC4390x-Q1 pin configuration separates the analog, digital, and power pins for an optimized layout. For signal integrity, separate the digital and analog traces, and place decoupling capacitors close to the device pins.

#### 8.4.2 Layout Example



**8-4. Layout Example**

Note: The ground and power planes have been omitted for clarity. Connect the thermal pad to ground.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.2 サポート・リソース

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### 9.3 Trademarks

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### 9.4 静電気放電に関する注意事項



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### 9.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC43901RTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	43901Q	<a href="#">Samples</a>
DAC43902RTERQ1	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	43902Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## GENERIC PACKAGE VIEW

**RTE 16**

**WQFN - 0.8 mm max height**

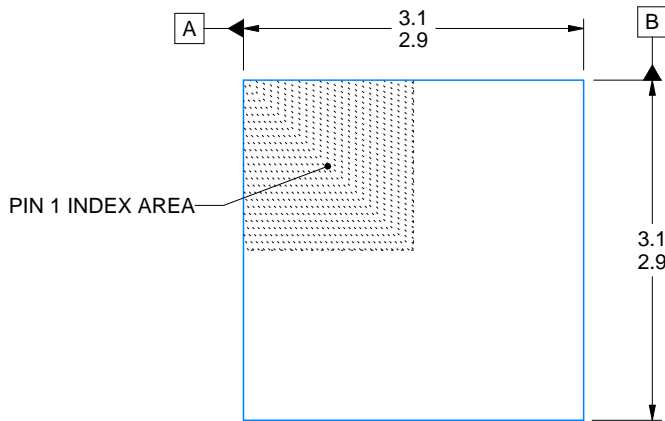
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

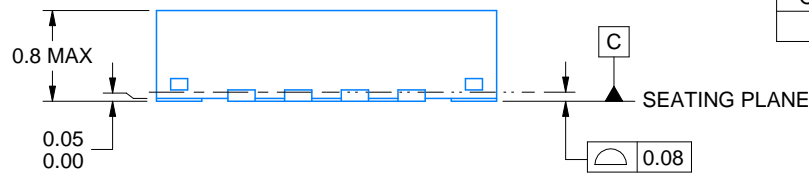
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

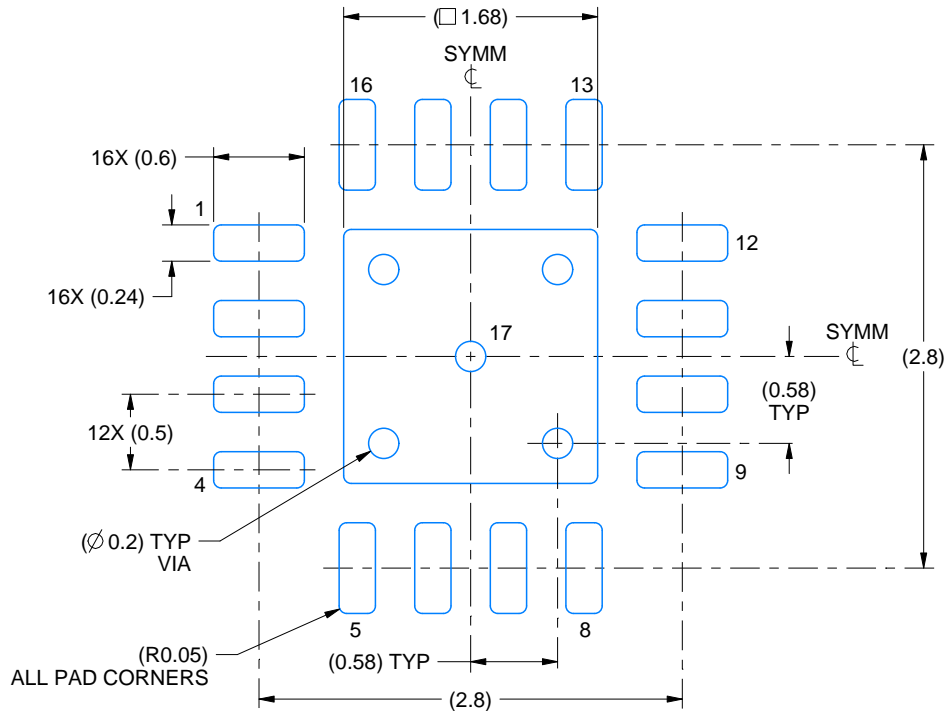


# EXAMPLE BOARD LAYOUT

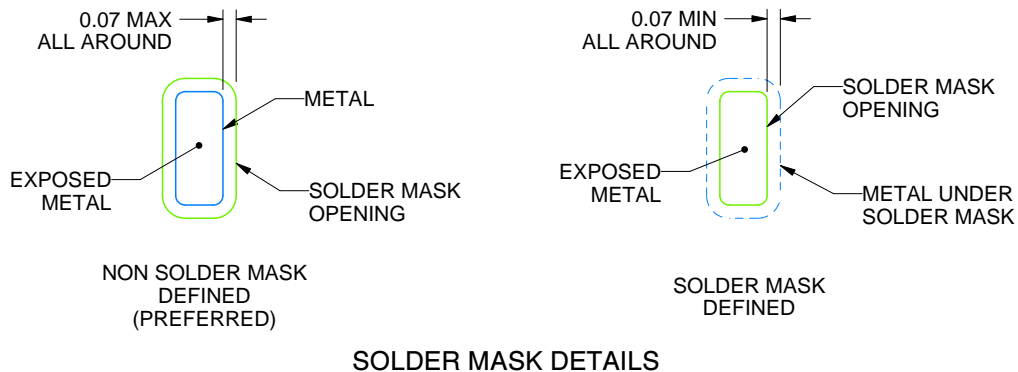
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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