



## 16-BIT, QUAD VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- **Low Power: 10 mW**
- **Unipolar or Bipolar Operation**
- **Settling Time: 10  $\mu$ s to 0.003%**
- **15-Bit Linearity and Monotonicity:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$**
- **Programmable Reset to Mid-Scale or Zero-Scale**
- **Double-Buffered Data Inputs**

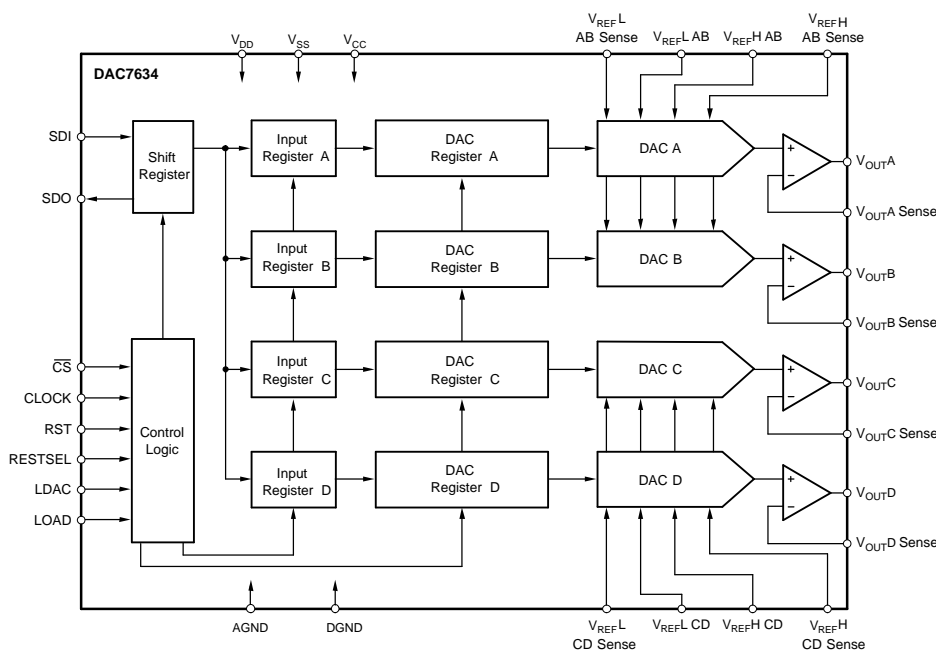
### APPLICATIONS

- **Process Control**
- **Closed-Loop Servo-Control**
- **Motor Control**
- **Data Acquisition Systems**
- **DAC-Per-Pin Programmers**

### DESCRIPTION

The DAC7634 is a 16-bit, quad voltage output, digital-to-analog converter with specified 15-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000<sub>H</sub> or to a zero-scale of 0000<sub>H</sub>. The DAC7634 can operate from a single 5-V supply or from 5-V and  $-5$  V supplies.

Low power and small size per DAC make the DAC7634 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7634 is available in a 48-lead SSOP package and offers specifications over the  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		UNIT
	$V_{CC}$ and $V_{DD}$ to $V_{SS}$	-0.3 V to 11 V
	$V_{CC}$ and $V_{DD}$ to GND	-0.3 V to 5.5 V
	$V_{REFL}$ to $V_{SS}$	-0.3 V to ( $V_{CC} - V_{SS}$ )
	$V_{CC}$ to $V_{REFH}$	-0.3 V to ( $V_{CC} - V_{SS}$ )
	$V_{REFH}$ to $V_{REFL}$	-0.3 V to ( $V_{CC} - V_{SS}$ )
	Digital input voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
	Digital output voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
$T_J$	Maximum junction temperature	150°C
$T_A$	Operating temperature range	-40°C to 85°C
$T_{stg}$	Storage temperature range	-65°C to 125°C
	Lead temperature (solder, 10s)	300°C

(1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

### SPECIFICATIONS

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = V_{CC} = 5$  V,  $V_{SS} = -5$  V,  $V_{REFH} = 2.5$  V, and  $V_{REFL} = -2.5$  V, unless otherwise noted

PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ACCURACY</b>								
Linearity error			±3	±4		±2	±3	LSB
Linearity match			±4			±2		LSB
Differential linearity error			±2	±3		±1	±2	LSB
Monotonicity, $T_{MIN}$ to $T_{MAX}$		14			15			Bits
Bipolar zero error			±1	±2		±1	±2	mV
Bipolar zero error drift			5	10		5	10	ppm/°C
Full-scale error			±1	±2		±1	±2	mV
Full-scale error drift			5	10		5	10	ppm/°C
Bipolar zero matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Full-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Power supply rejection ratio (PSRR)	At full scale		10	100		10	100	ppm/V

**SPECIFICATIONS (continued)**

 At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{SS} = -5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ , and  $V_{REFL} = -2.5\text{ V}$ , unless otherwise noted

PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ANALOG INPUT</b>								
Voltage output	$V_{REF} = -2.5\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $V_{SS} = -5\text{ V}$	$V_{REFL}$		$V_{REFH}$	$V_{REFL}$		$V_{REFH}$	V
Output current		-1.25		1.25	1.25		1.25	mA
Maximum load capacitance	No oscillation		500		500			pF
Short-circuit current			-10, 30		-10, +30			mA
Short-circuit duration	GND or $V_{CC}$ or $V_{SS}$		Indefinite		Indefinite			
<b>REFERENCE INPUT</b>								
Ref high input voltage range		$V_{REFL}$ +1.25		2.5	$V_{REFL}$ +1.25		2.5	V
Ref low input voltage range		-2.5		$V_{REFH}$ -1.25	-2.5		$V_{REFH}$ -1.25	V
Ref high input current			500		500			$\mu\text{A}$
Ref low input current			-500		-500			$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>								
Settling time	To $\pm 0.003\%$ , 5-V output step		8	10		8	10	$\mu\text{s}$
Channel-to-channel crosstalk	See Figure 5		0.5		0.5			LSB
Digital feedthrough			2		2			nV-s
Output noise voltage	$f = 10\text{ kHz}$		60		60			$\text{nV}/\sqrt{\text{Hz}}$
DAC glitch	$7FFF_H$ to $8000_H$ or $8000_H$ to $7FFF_H$		40		40			nV-s
<b>DIGITAL INPUT</b>								
$V_{IH}$		$0.7 \times V_{DD}$			$0.7 \times V_{DD}$			V
$V_{IL}$		$0.3 \times V_{DD}$			$0.3 \times V_{DD}$			V
$I_{IH}$			$\pm 10$		$\pm 10$			$\mu\text{A}$
$I_{IL}$			$\pm 10$		$\pm 10$			$\mu\text{A}$
<b>DIGITAL OUTPUT</b>								
$V_{OH}$	$I_{OH} = -0.8\text{ mA}$	3.6	4.5		3.6	4.5		V
$V_{OL}$	$I_{OL} = 1.6\text{ mA}$		0.3	0.4		0.3	0.4	V
<b>POWER SUPPLY</b>								
$V_{DD}$		4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{CC}$		4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{SS}$		-5.25	-5.0	-4.75	-5.25	-5.0	-4.75	V
$I_{CC}$			1.5	2		1.5	2	mA
$I_{DD}$			50		50			$\mu\text{A}$
$I_{SS}$		-2.3	-1.5		-2.3	-1.5		mA
Power			15	20		15	20	mW

**SPECIFICATIONS**

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ , and  $V_{REFL} = 0\text{ V}$ , unless otherwise noted

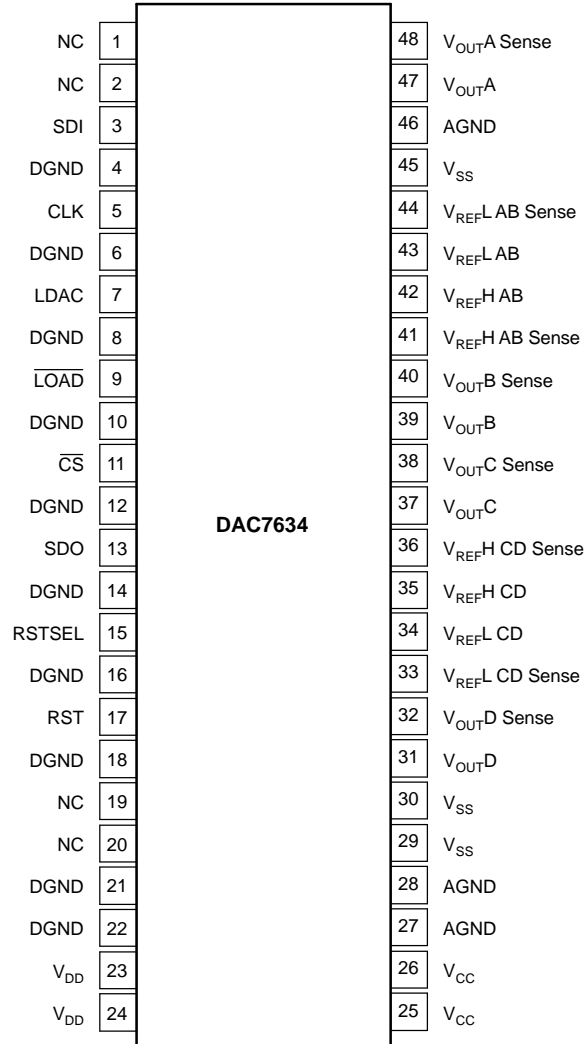
PARAMETER	TEST CONDITIONS	DAC7634E			DAC7634EB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>ACCURACY</b>								
Linearity error <sup>(1)</sup>			±3	±4		±2	±3	LSB
Linearity match			±4			±2		LSB
Differential linearity error			±2	±3		±1	±2	LSB
Monotonicity, $T_{MIN}$ to $T_{MAX}$		14			15			Bits
Zero-scale error			±1	±2		±1	±2	mV
Zero-scale error drift			5	10		5	10	ppm/°C
Full-scale error			±1	±2		±1	±2	mV
Full-scale error drift			5	10		5	10	ppm/°C
Zero-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Full-scale matching	Channel-to-channel matching		±1	±2		±1	±2	mV
Power supply rejection ratio (PSRR)	At full scale		10	100		10	100	ppm/V
<b>ANALOG INPUT</b>								
Voltage output	$V_{REFL} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $R_L = 10\text{ k}\Omega$	0		$V_{REFH}$	0		$V_{REFH}$	V
Output current		-1.25		1.25	-1.25		1.25	mA
Maximum load capacitance	No oscillation		500			500		pF
Short-circuit current			±30			±30		mA
Short-circuit duration	GND or $V_{CC}$		Indefinite			Indefinite		
<b>REFERENCE INPUT</b>								
Ref high input voltage range		$V_{REFL} + 1.25$		2.5	$V_{REFL} + 1.25$		2.5	V
Ref low input voltage range		0		$V_{REFH} - 1.25$	0		$V_{REFH} - 1.25$	V
Ref high input current			250			250		μA
Ref low input current			-250			-250		μA
<b>DYNAMIC PERFORMANCE</b>								
Settling time	To ±0.003%, 2.5-V output step		8	10		8	10	μs
Channel-to-channel crosstalk	See Figure 6		0.5			0.5		LSB
Digital feedthrough			2			2		nV-s
Output noise voltage	$f = 10\text{ kHz}$		60			60		nV/√Hz
DAC glitch	7FFF <sub>H</sub> to 8000 <sub>H</sub> or 8000 <sub>H</sub> to 7FFF <sub>H</sub>		40			40		nV-s
<b>DIGITAL INPUT</b>								
$V_{IH}$		$0.7 \times V_{DD}$			$0.7 \times V_{DD}$			V
$V_{IL}$		$0.3 \times V_{DD}$			$0.3 \times V_{DD}$			V
$I_{IH}$			±10			±10		μA
$I_{IL}$			±10			±10		μA
<b>DIGITAL OUTPUT</b>								
$V_{OH}$	$I_{OH} = -0.8\text{ mA}$	3.6	4.5		3.6	4.5		V
$V_{OL}$	$I_{OL} = 1.6\text{ mA}$		0.3	0.4		0.3	0.4	V
<b>POWER SUPPLY</b>								
$V_{DD}$		4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{CC}$		4.75	5.0	5.25	4.75	5.0	5.25	V
$V_{SS}$		0	0	0	0	0	0	V
$I_{CC}$			1.5	2		1.5	2	mA
$I_{DD}$			50			50		μA
Power			7.5	10		7.5	10	mW

(1) If  $V_{SS} = 0\text{ V}$  specification applies at Code 0040<sub>H</sub> and above due to possible negative zero-scale error.

**PIN DESCRIPTIONS**

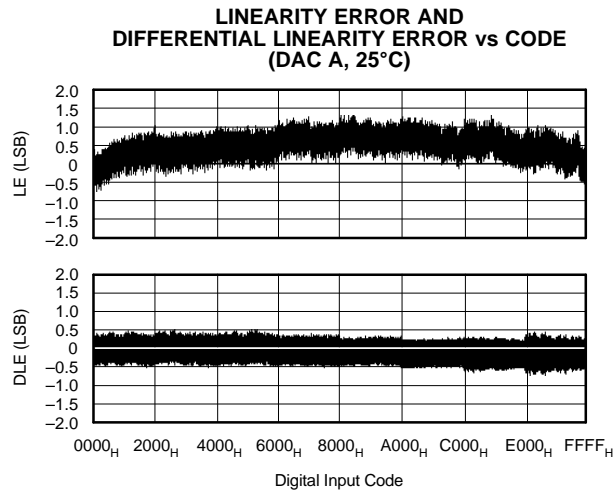
PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	NC	No connection	25	V <sub>CC</sub>	Analog +5-V power supply
2	NC	No connection	26	V <sub>CC</sub>	Analog +5-V power supply
3	SDI	Serial data input	27	AGND	Analog ground
4	DGND	Digital ground	28	AGND	Analog ground
5	CLK	Data clock input	29	V <sub>SS</sub>	Analog +5-V power supply or 0-V single supply
6	DGND	Digital ground	30	V <sub>SS</sub>	Analog +5-V power supply or 0-V single supply
7	LDAC	DAC register load control, rising edge triggered	31	V <sub>OUTD</sub>	DAC D output voltage
8	DGND	Digital ground	32	V <sub>OUTD</sub> Sense	DAC D's output amplifier inverting input. Used to close feedback loop at load.
9	$\overline{\text{LOAD}}$	DAC input register load control, active low	33	V <sub>REFL</sub> CD Sense	DAC C and D reference low sense input
10	DGND	Digital ground	34	V <sub>REFL</sub> CD	DAC C and D reference low input
11	$\overline{\text{CS}}$	Chip select, active low	35	V <sub>REFH</sub> CD	DAC C and D reference high input
12	DGND	Digital ground	36	V <sub>REFH</sub> CD Sense	DAC C and D reference high sense input
13	SDO	Serial data output	37	V <sub>OUTC</sub>	DAC C output voltage
14	DGND	Digital ground	38	V <sub>OUTC</sub> Sense	DAC C's output amplifier inverting input. Used to close the feedback loop at the load.
15	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST common sets the DAC registers to mid-scale (8000 <sub>H</sub> ). If LOW, a RST command sets the DAC registers to zero (0000 <sub>H</sub> ).	39	V <sub>OUTB</sub>	DAC B output voltage
16	DGND	Digital ground	40	V <sub>OUTB</sub> Sense	DAC B's output amplifier inverting input. Used to close the feedback loop at the load.
17	RST	Reset, rising edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.	41	V <sub>REFH</sub> AB Sense	DAC A and B reference high sense input
18	DGND	Digital ground	42	V <sub>REFH</sub> AB	DAC A and B reference high input
19	NC	No connection	43	V <sub>REFL</sub> AB	DAC A and B reference low input
20	NC	No connection	44	V <sub>REFL</sub> AB Sense	DAC A and B reference low sense input
21	DGND	Digital ground	45	V <sub>SS</sub>	Analog –5-V power supply or 0-V single supply
22	DGND	Digital ground	46	AGND	Analog ground
23	V <sub>DD</sub>	Digital 5-V power supply	47	V <sub>OUTA</sub>	DAC A output voltage
24	V <sub>DD</sub>	Digital 5-V power supply	48	V <sub>OUTA</sub> Sense	DAC A's output amplifier inverting input. Used to close the feedback loop at the load.

**PIN CONFIGURATION**

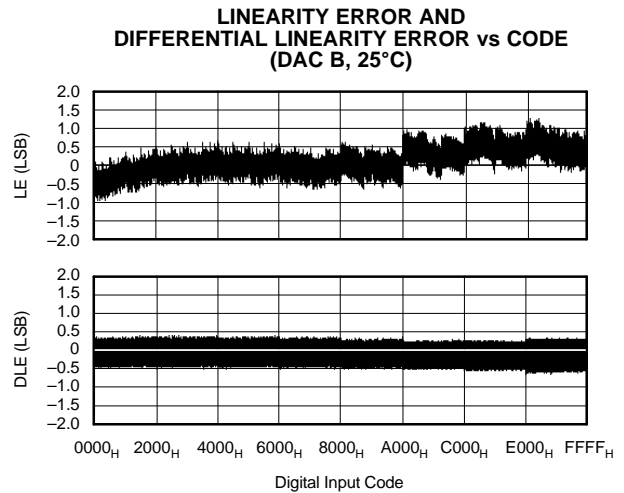


**TYPICAL PERFORMANCE CURVES:  $V_{SS} = 0$  V**

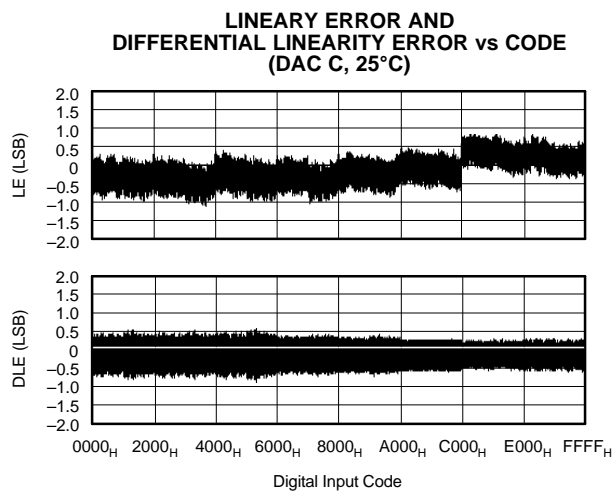
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5$  V,  $V_{REFH} = 2.5$  V,  $V_{REFL} = 0$  V, representative unit, unless otherwise specified.



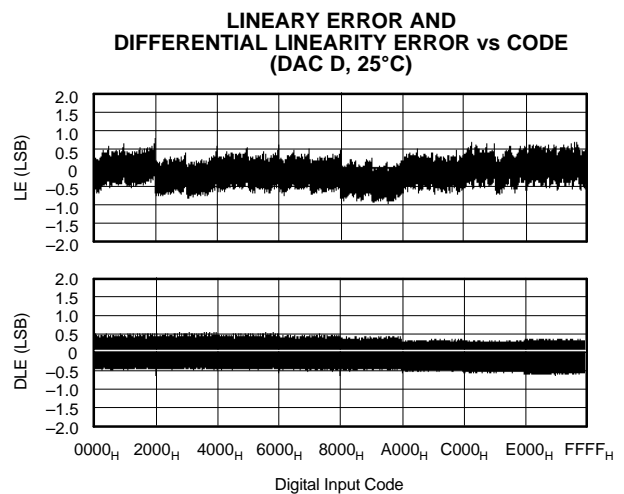
**Figure 1.**



**Figure 2.**



**Figure 3.**



**Figure 4.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = 0\text{ V}$  (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.

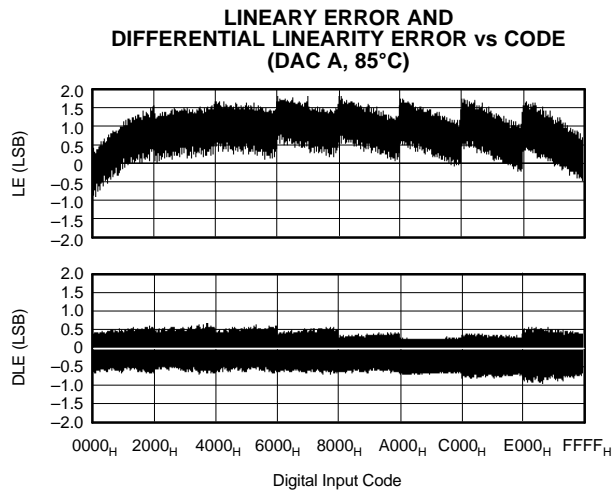


Figure 5.

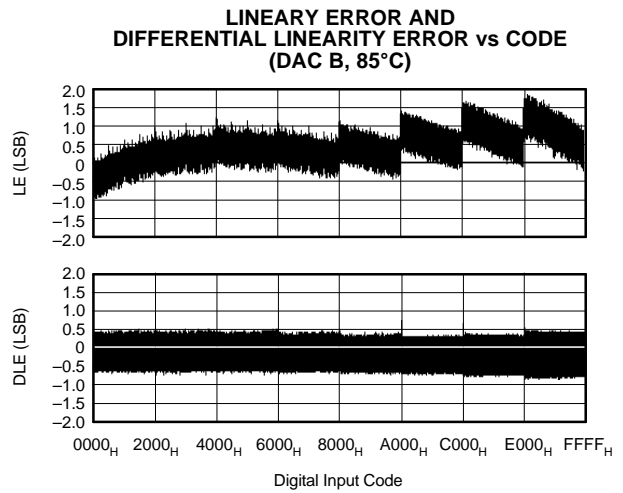


Figure 6.

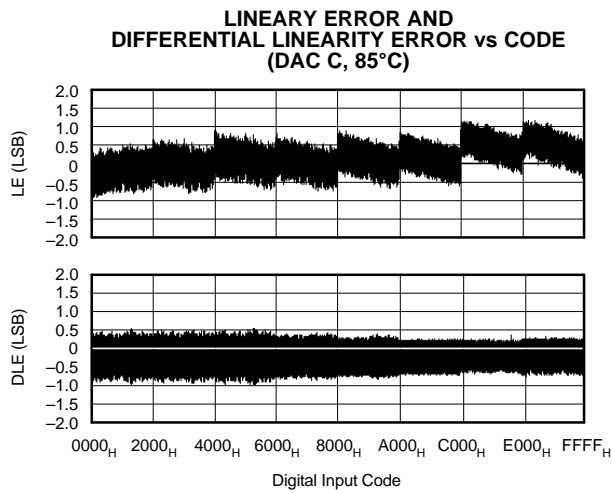


Figure 7.

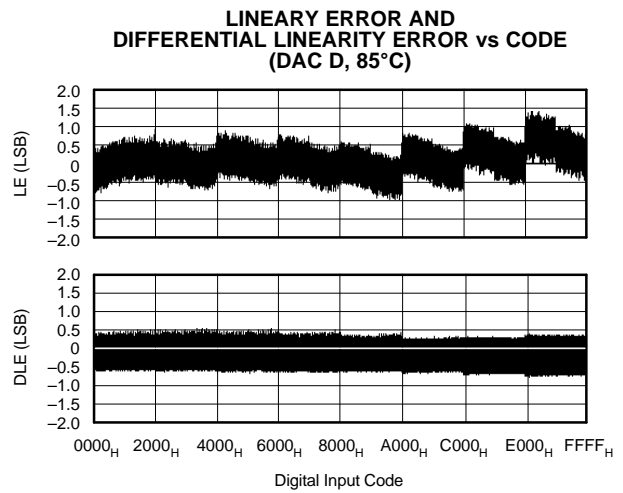
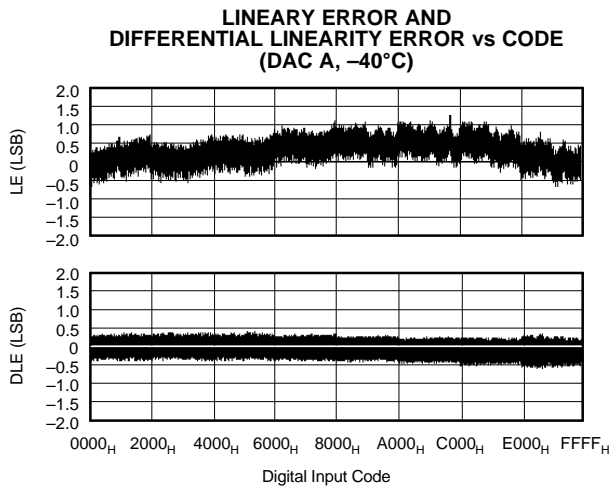


Figure 8.

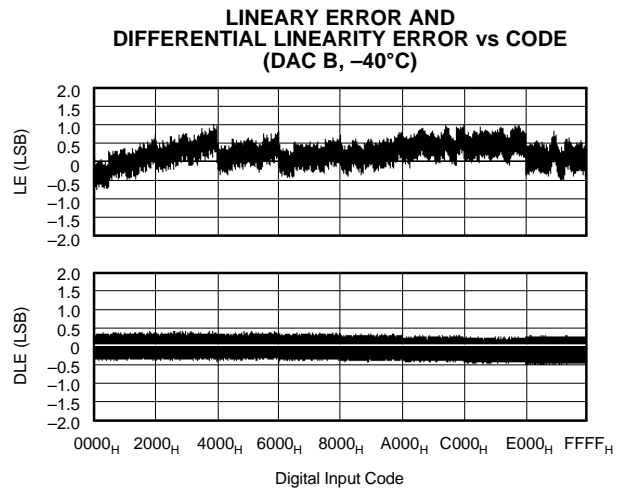


**TYPICAL PERFORMANCE CURVES:  $V_{SS} = 0$  V (continued)**

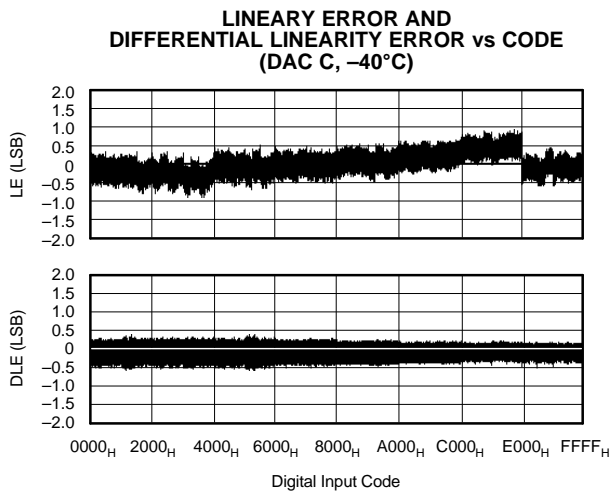
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5$  V,  $V_{REFH} = 2.5$  V,  $V_{REFL} = 0$  V, representative unit, unless otherwise specified.



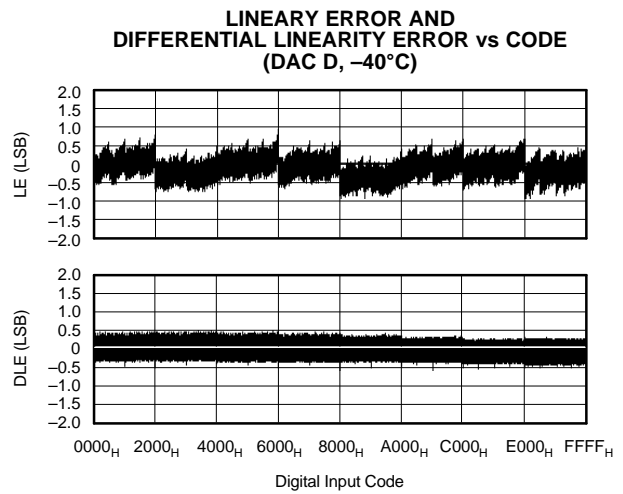
**Figure 9.**



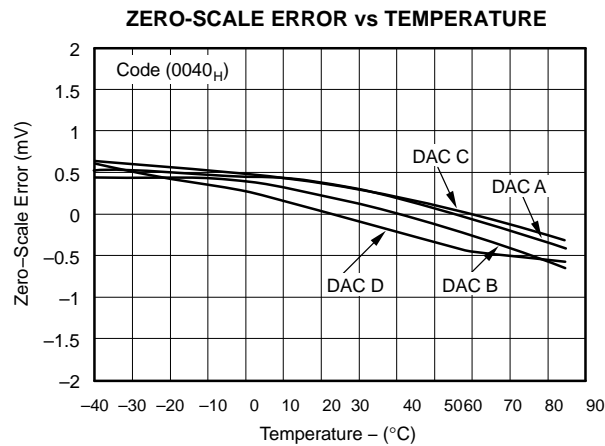
**Figure 10.**



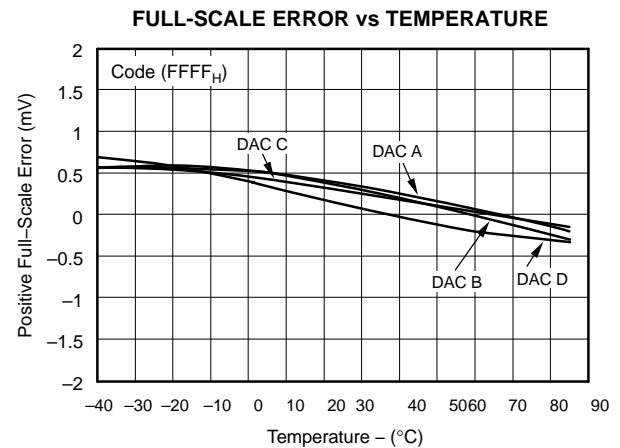
**Figure 11.**



**Figure 12.**



**Figure 13.**



**Figure 14.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = 0$  V (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5$  V,  $V_{REFH} = 2.5$  V,  $V_{REFL} = 0$  V, representative unit, unless otherwise specified.

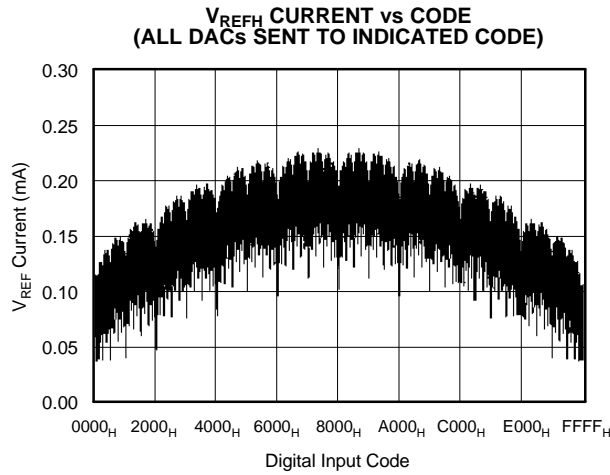


Figure 15.

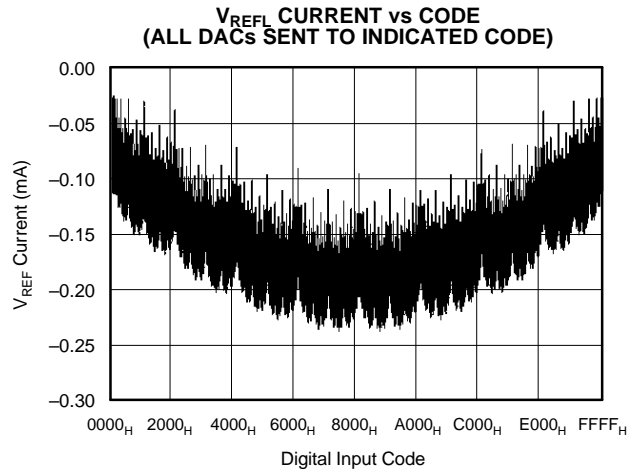


Figure 16.

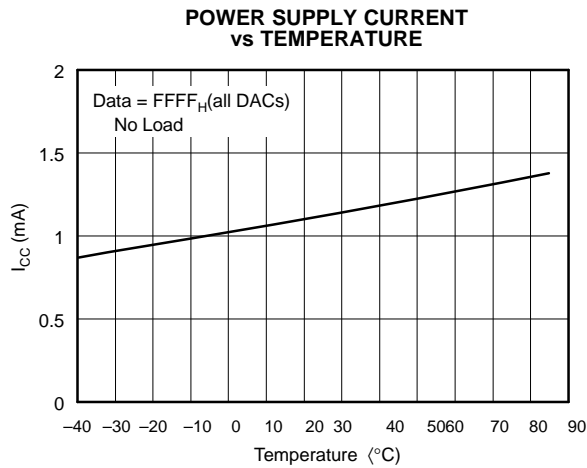


Figure 17.

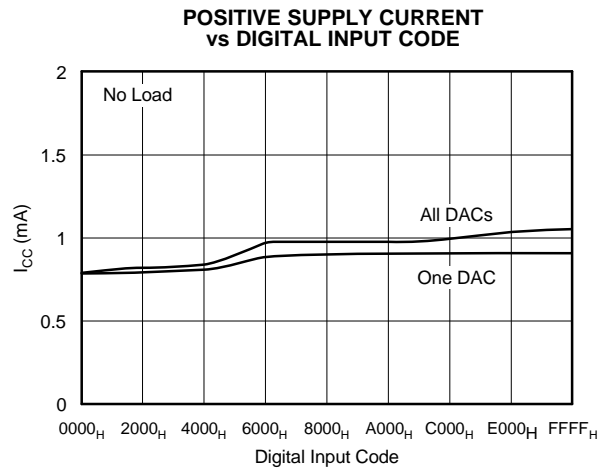


Figure 18.

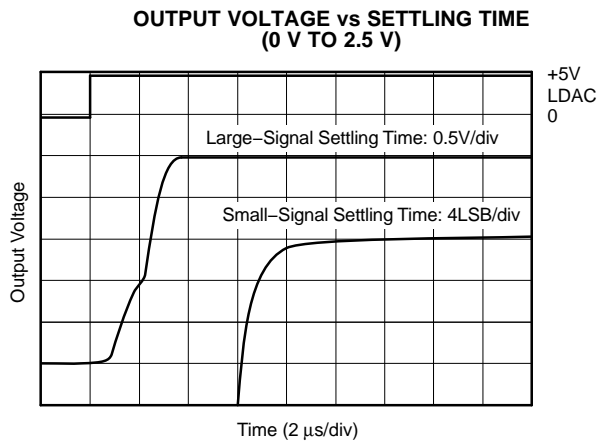


Figure 19.

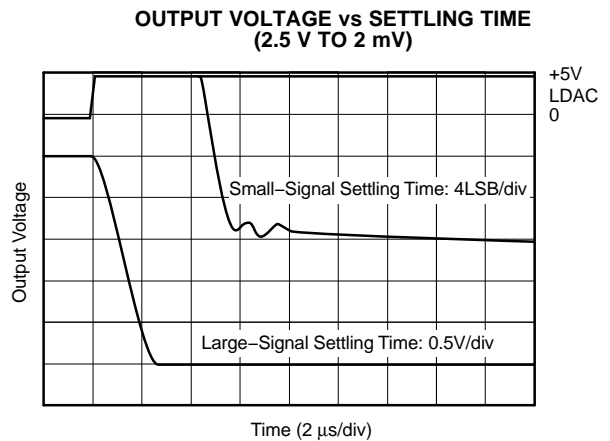
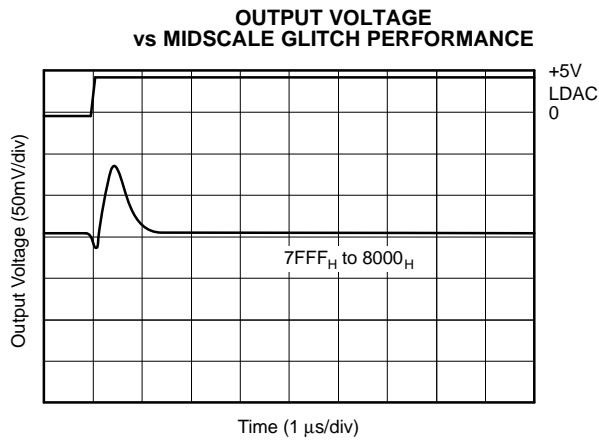


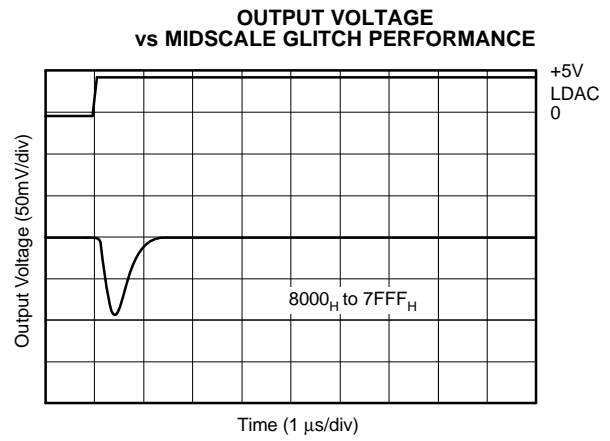
Figure 20.

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = 0\text{ V}$  (continued)**

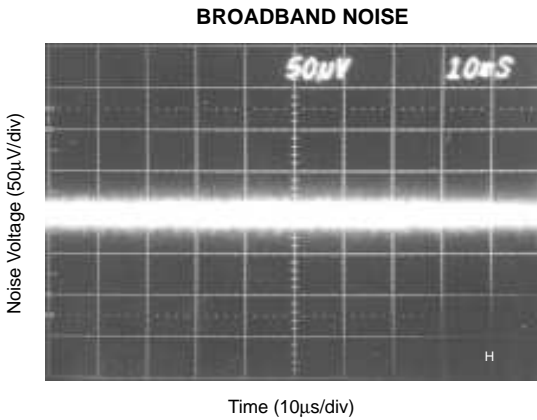
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.



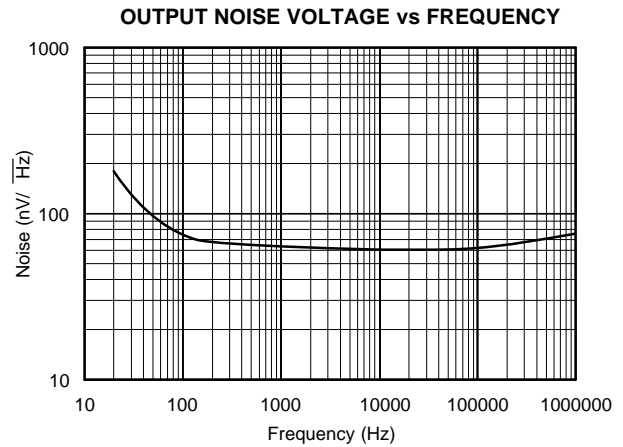
**Figure 21.**



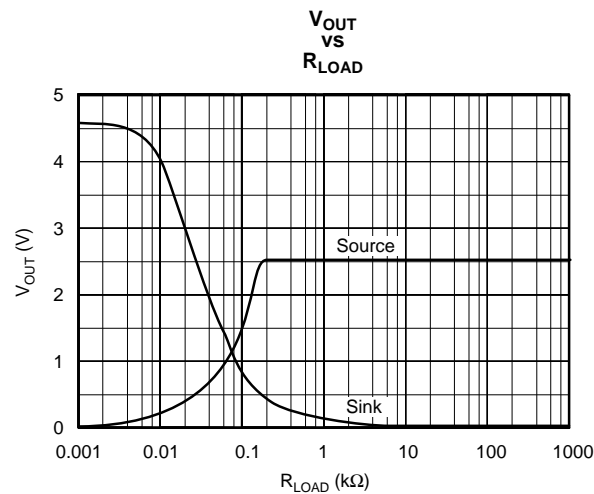
**Figure 22.**



**Figure 23.**



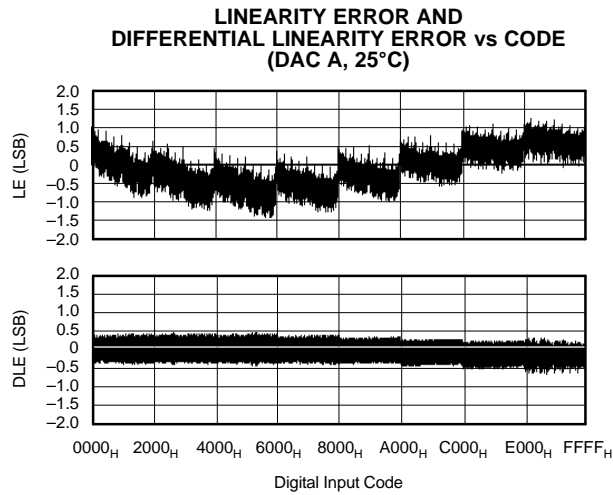
**Figure 24.**



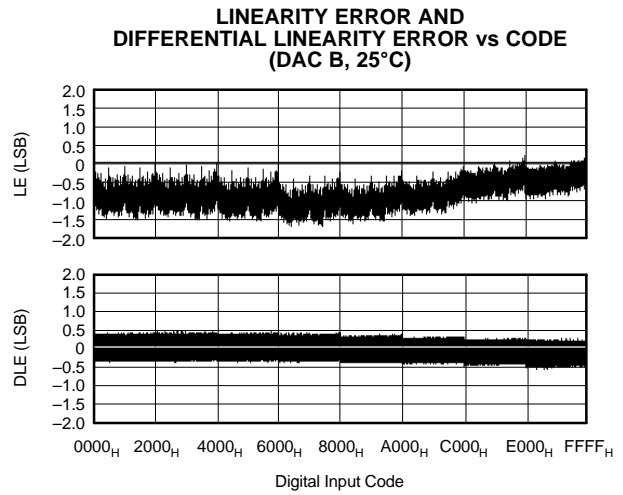
**Figure 25.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = -5\text{ V}$**

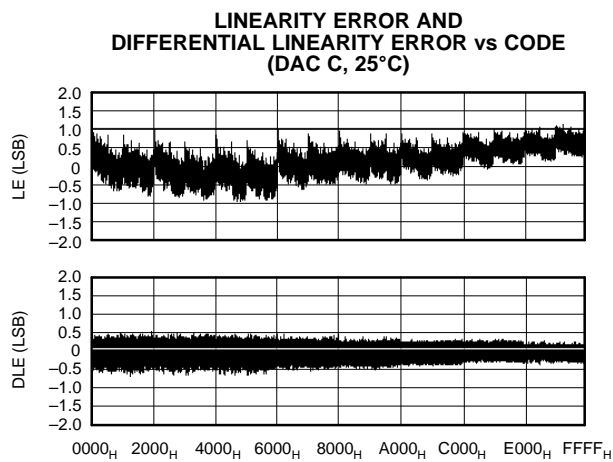
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.



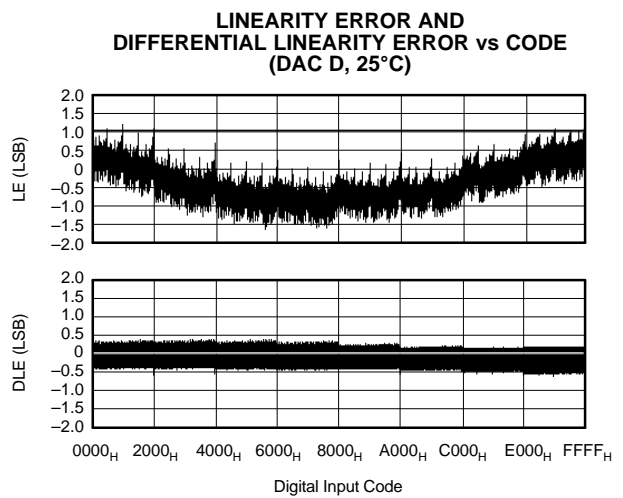
**Figure 26.**



**Figure 27.**



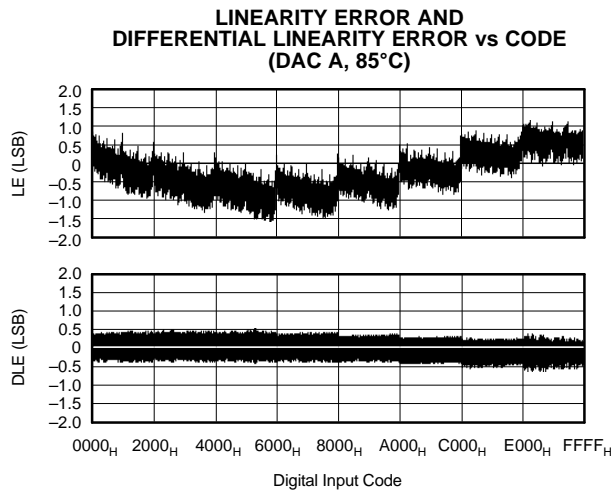
**Figure 28.**



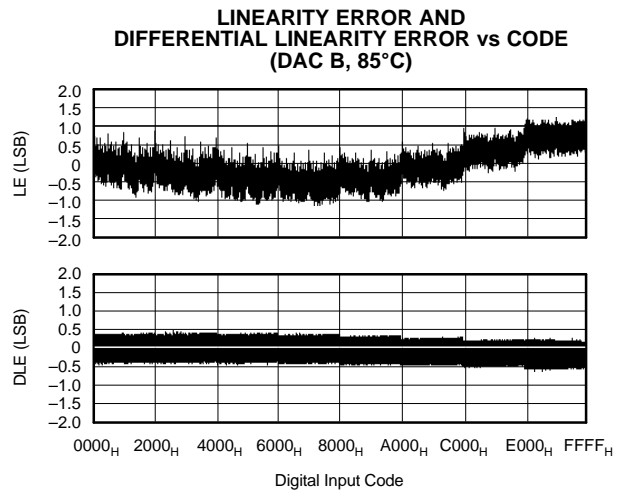
**Figure 29.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = -5\text{ V}$  (continued)**

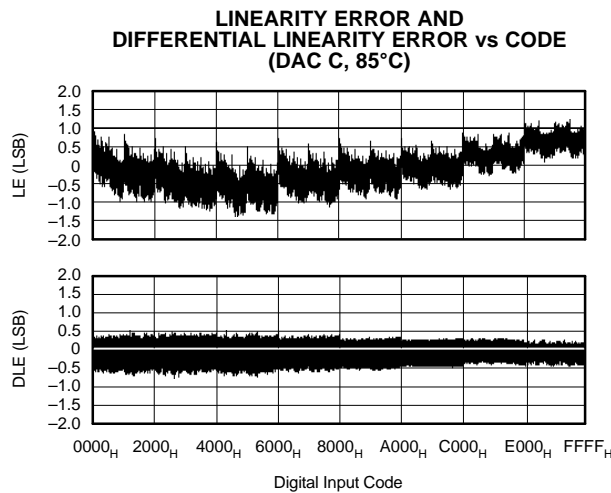
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.



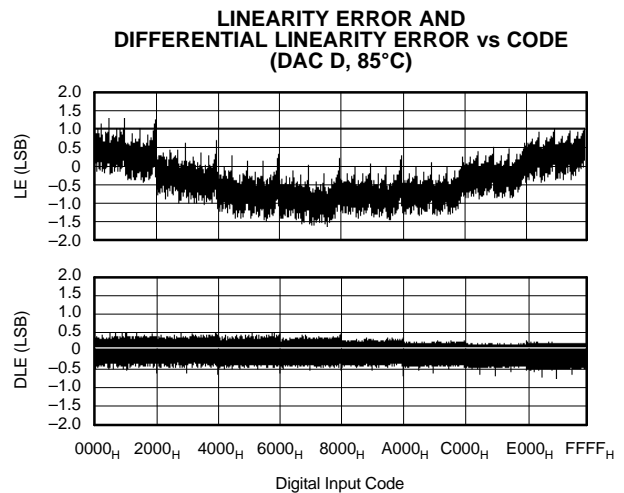
**Figure 30.**



**Figure 31.**



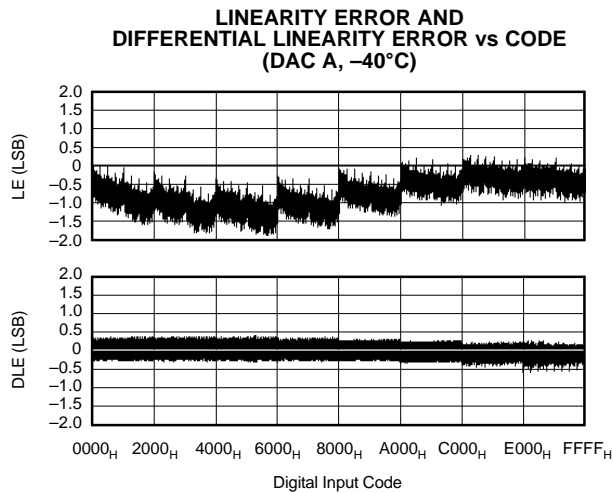
**Figure 32.**



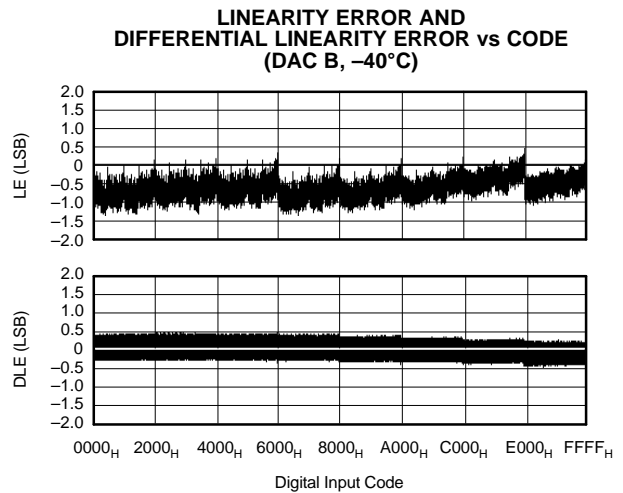
**Figure 33.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = -5\text{ V}$  (continued)**

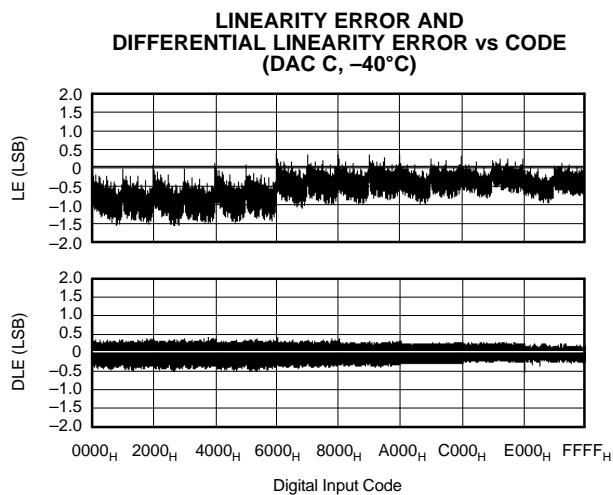
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.



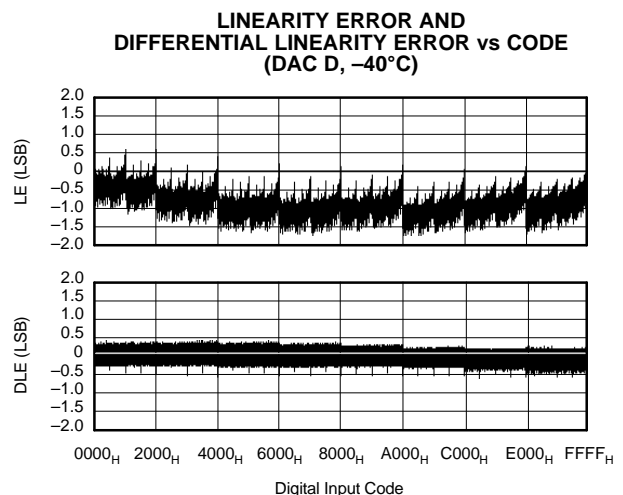
**Figure 34.**



**Figure 35.**



**Figure 36.**



**Figure 37.**

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = -5\text{ V}$  (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.

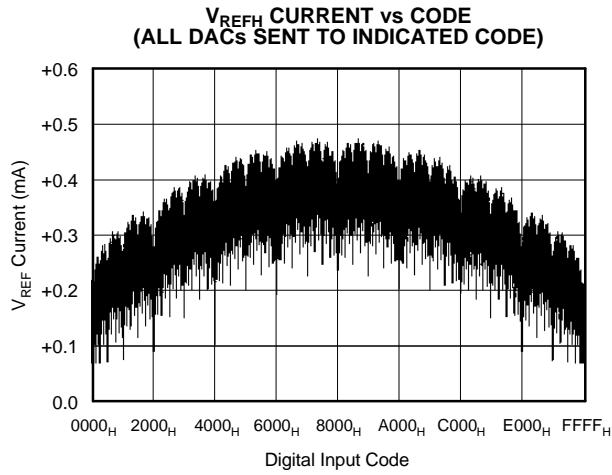


Figure 38.

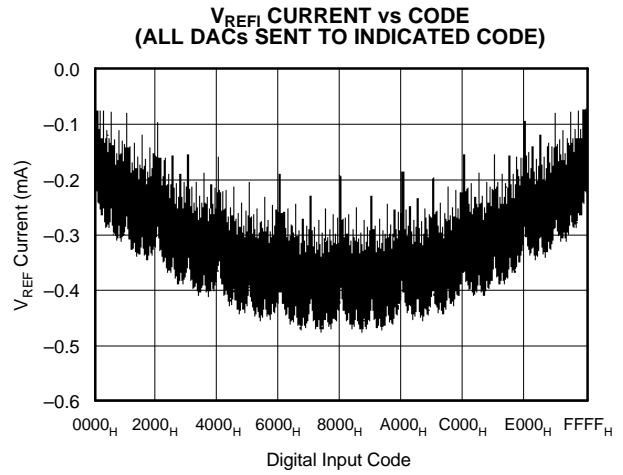


Figure 39.

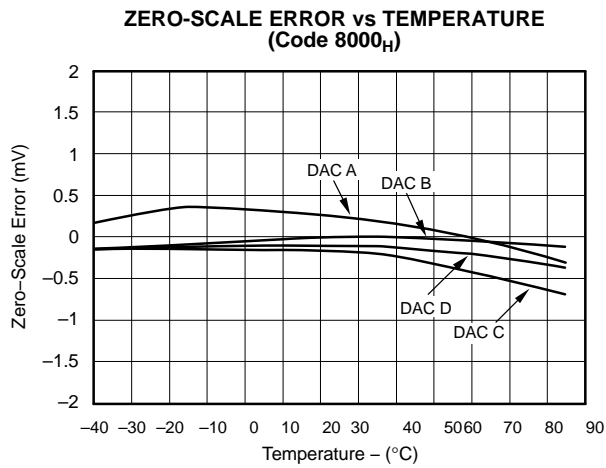


Figure 40.

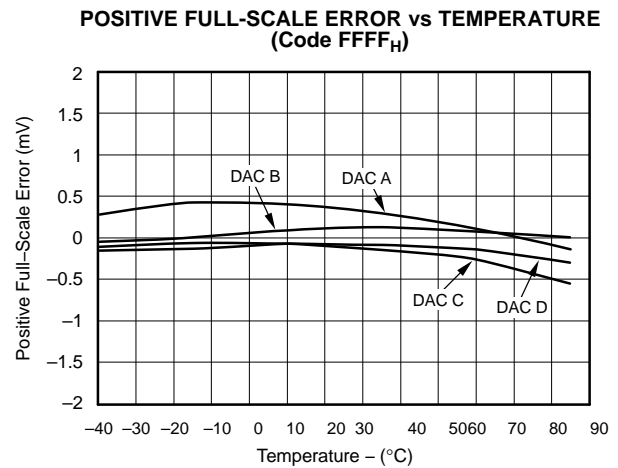


Figure 41.

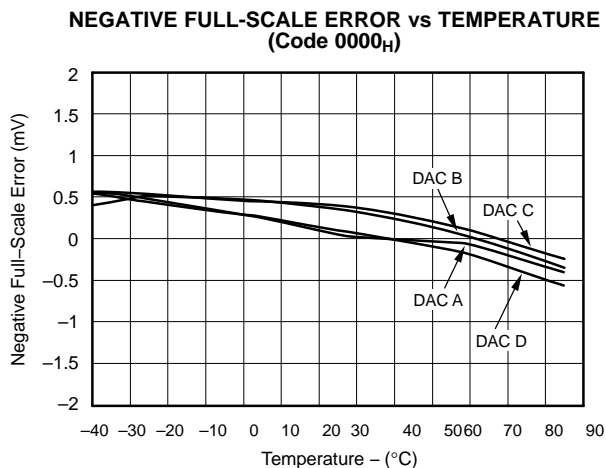


Figure 42.

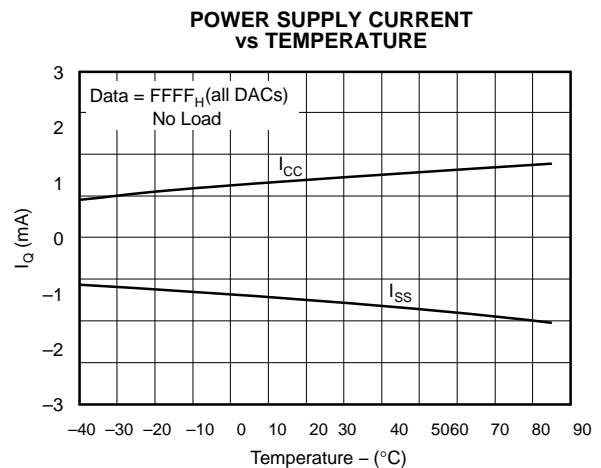


Figure 43.

**TYPICAL PERFORMANCE CURVES:  $V_{SS} = -5\text{ V}$  (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = 5\text{ V}$ ,  $V_{REFH} = 2.5\text{ V}$ ,  $V_{REFL} = 0\text{ V}$ , representative unit, unless otherwise specified.

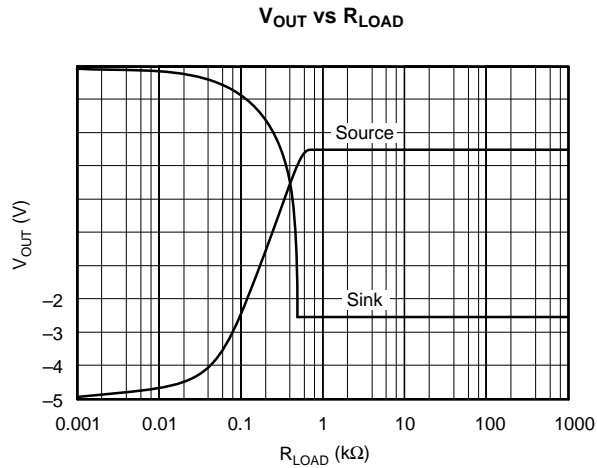


Figure 44.

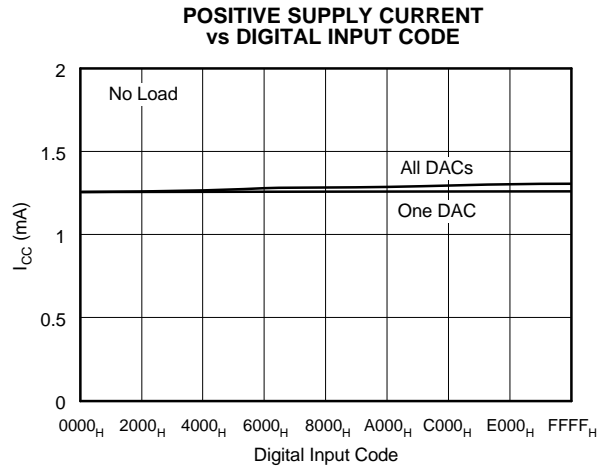


Figure 45.

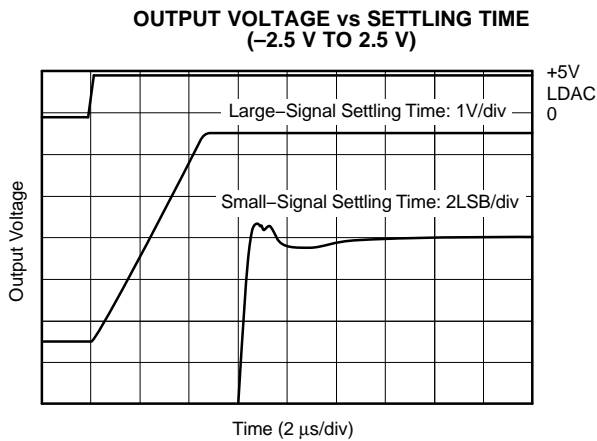


Figure 46.

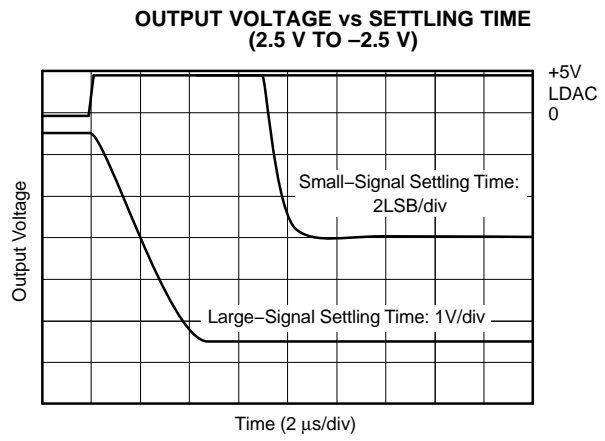


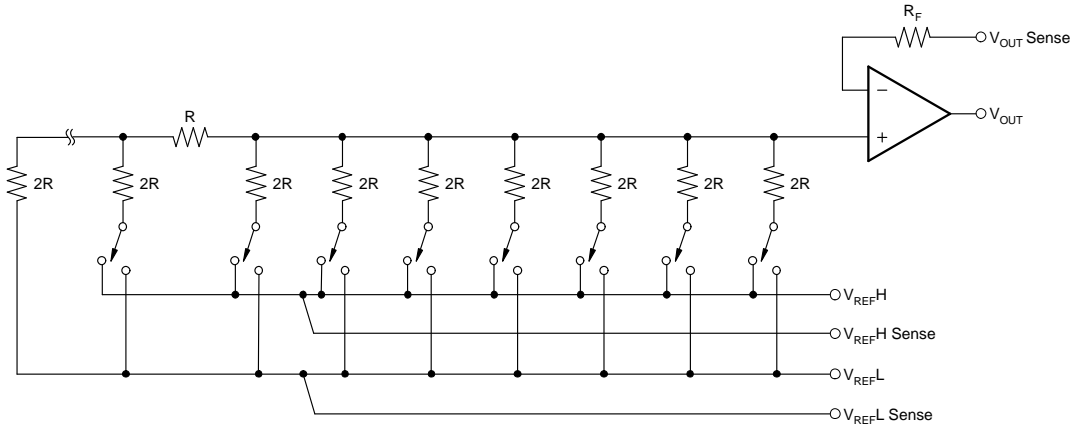
Figure 47.

**THEORY OF OPERATION**

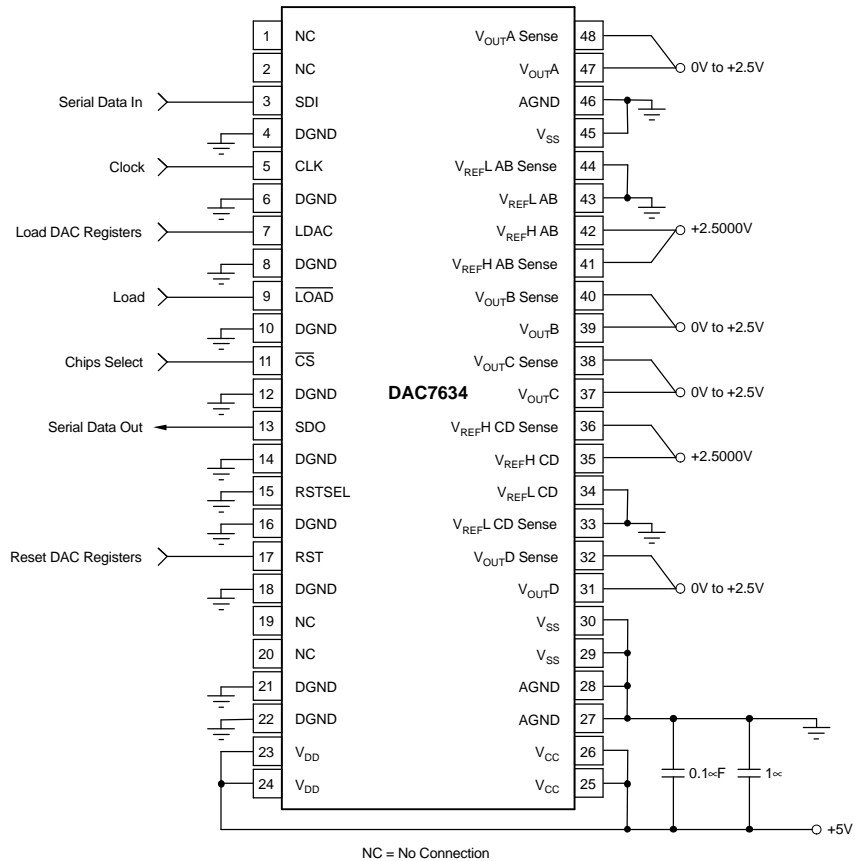
The DAC7634 is a quad voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output operational amplifier, as shown in Figure 48. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references ( $V_{REFL}$  and  $V_{REFH}$ , respectively).

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits, and the 16-bit DAC code (MSB first). The converters can be powered from either a single 5-V supply or a dual  $\pm 5\text{-V}$  supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code  $8000_H$  or to zero-scale, code  $0000_H$ . See Figure 49 and Figure 50 for the basic operation of the DAC7634.

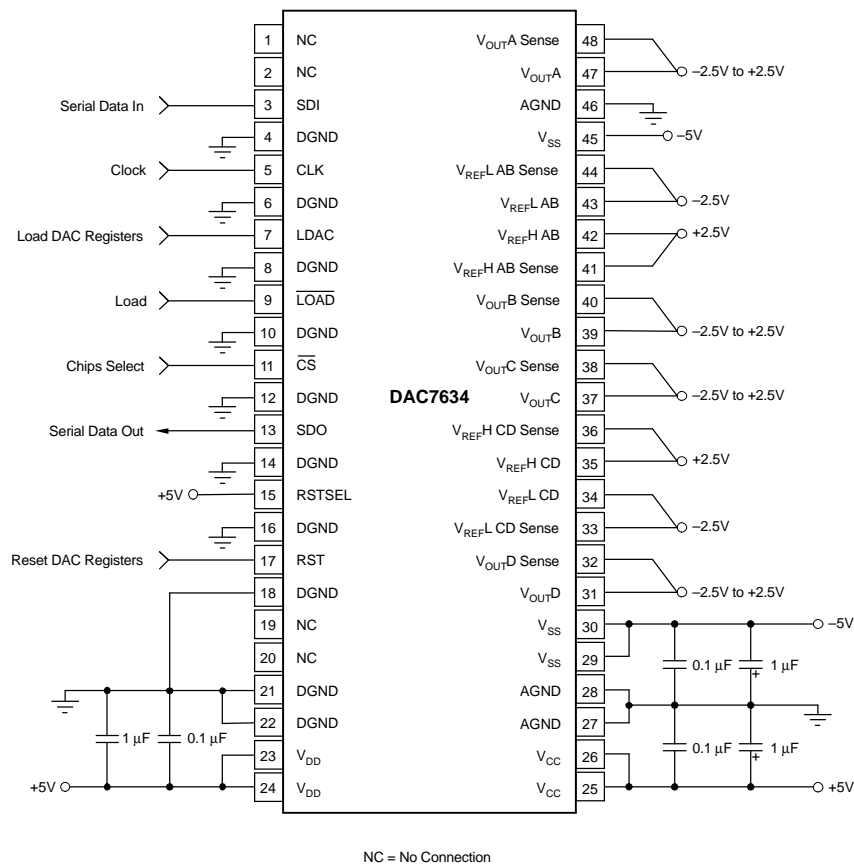




**Figure 48. DAC7634 Architecture**



**Figure 49. Basic Single-Supply Operation of the DAC7634**



**Figure 50. Basic Dual-Supply Operation of the DAC7634**

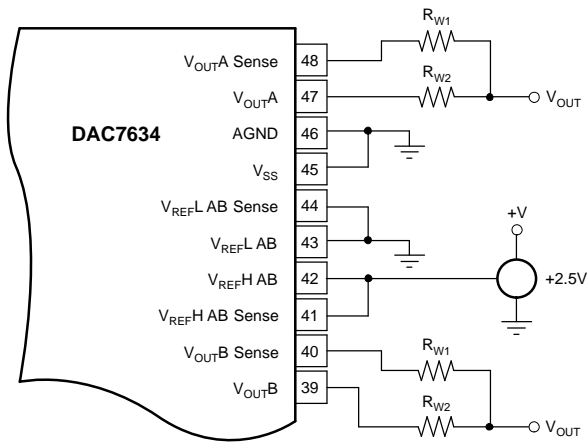
**ANALOG OUTPUTS**

When  $V_{SS} = -5V$  (dual supply operation), the output amplifier can swing to within 2.25 V of the supply rails, specified over the  $-40^{\circ}C$  to  $85^{\circ}C$  temperature range. When  $V_{SS} = 0 V$  (single-supply operation), and with  $R_{LOAD}$  also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when  $V_{SS} = 0 V$ . Because the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000<sub>H</sub>, 0001<sub>H</sub>, 0002<sub>H</sub>, etc.) if the output amplifier has a negative offset. At the negative limit of  $-2 mV$ , the first specified output starts at code 0040<sub>H</sub>.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become important. A 16-bit

converter with a 2.5 V full-scale range has a 1-LSB value of 38  $\mu V$ . With a load current of 1 mA, series wiring and connector resistance of only 40 m $\Omega$  ( $R_{W2}$ ) causes a voltage drop of 40  $\mu V$ , as shown in Figure 51. To understand what this means in terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed-circuit board is 1.2 m $\Omega$  per square. For a 1-mA load, a 10-mil wide printed-circuit conductor 600 mil long results in a voltage drop of 30  $\mu V$ .

The DAC7634 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 51), thus ensuring an accurate output voltage.



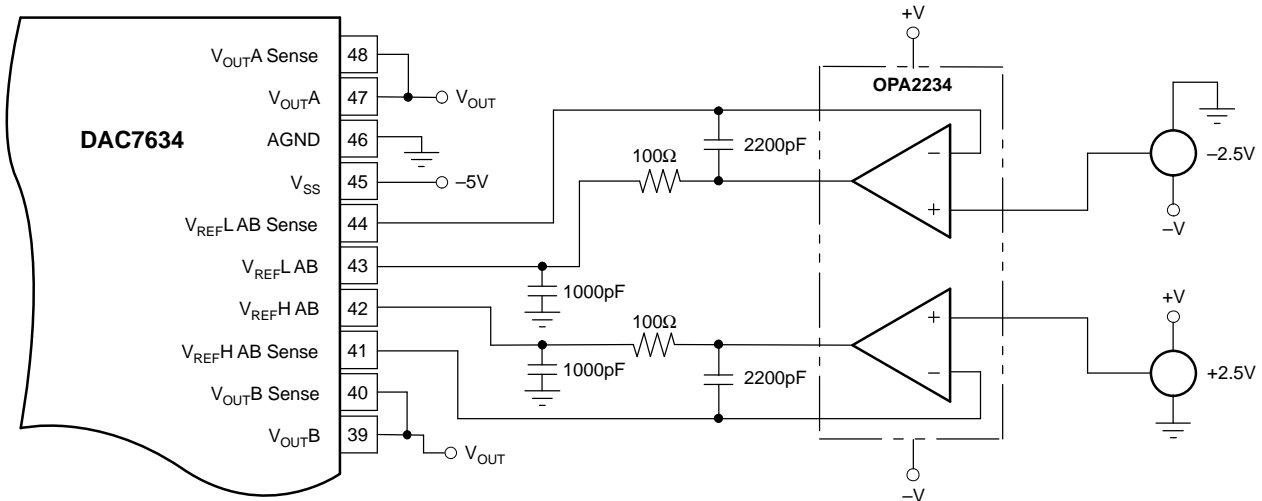
**Figure 51. Analog Output Closed-Loop Configuration (1/2 DAC7634)**  
( $R_W$  Represents Wiring Resistances)

**REFERENCE INPUTS**

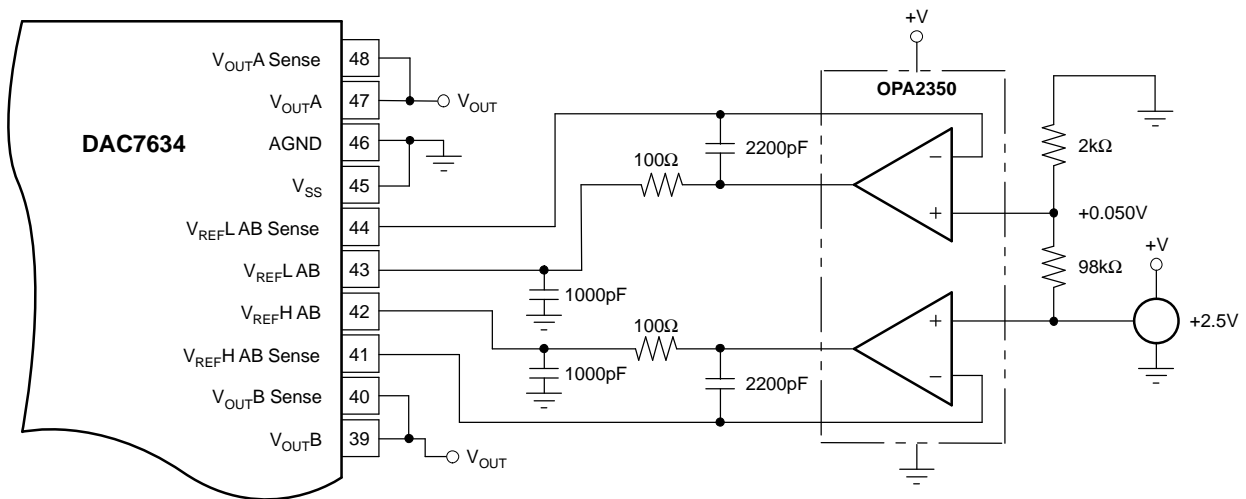
The reference inputs,  $V_{REFL}$  and  $V_{REFH}$ , can be any voltage between  $V_{SS} + 2.5\text{ V}$  and  $V_{CC} - 2.5\text{ V}$ , provided that  $V_{REFH}$  is at least 1.25 V greater than

$V_{REFL}$ . The minimum output of each DAC is equal to  $V_{REFL}$  plus a small offset voltage (essentially, the offset of the output operational amp). The maximum output is equal to  $V_{REFH}$  plus a similar offset voltage. Note that  $V_{SS}$  (the negative power supply) must either be connected to ground or must be in the range of  $-4.75\text{ V}$  to  $-5.25\text{ V}$ . The voltage on  $V_{SS}$  sets several bias points within the converter. If  $V_{SS}$  is not in one of these two configurations, the bias values may be in error and proper operation of the device is not specified.

The current into the  $V_{REFH}$  input and out of  $V_{REFL}$  depends on the DAC output voltages, and can vary from a few microamps to approximately 0.5 mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7634 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figure 52 through Figure 60 show different reference configurations, and the effect on the linearity and differential linearity.



**Figure 52. Dual Supply Configuration-Buffered References, Used for Dual Supply Performance**



NOTE:  $V_{REFL}$  has been chosen to be 50 mV to allow for current sinking voltage drops across the 100- $\Omega$  resistor and the output stage of the buffer operational amplifier.

Figure 53. Single-Supply Buffered Reference With a Reference Low of 50 mV (1/2 DAC7634)

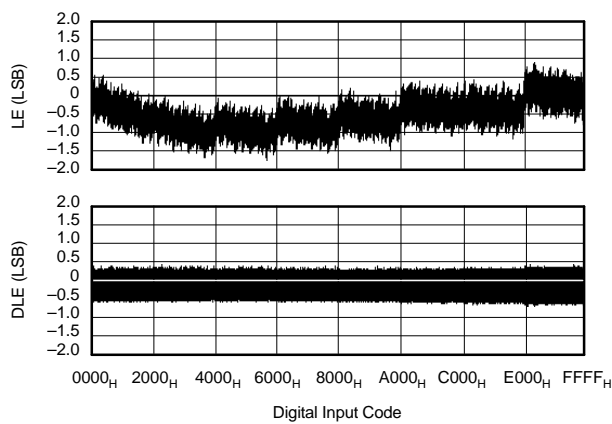


Figure 54. Integral Linearity and Differential Linearity Error Curves for Figure 53

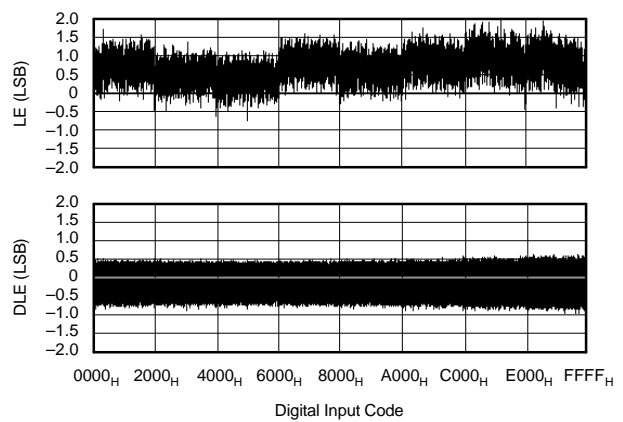


Figure 55. Integral Linearity and Differential Linearity Error Curves for Figure 56

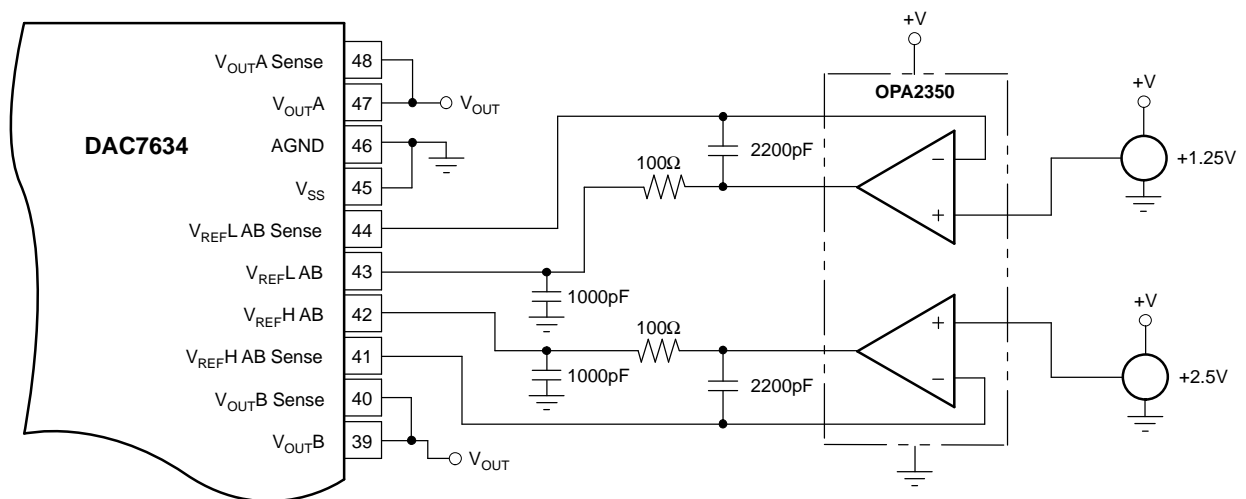


Figure 56. Single-Supply Buffered Reference With  $V_{REFL} = 1.25$  V and  $V_{REFH} = 2.5$  V (1/2 DAC7634)

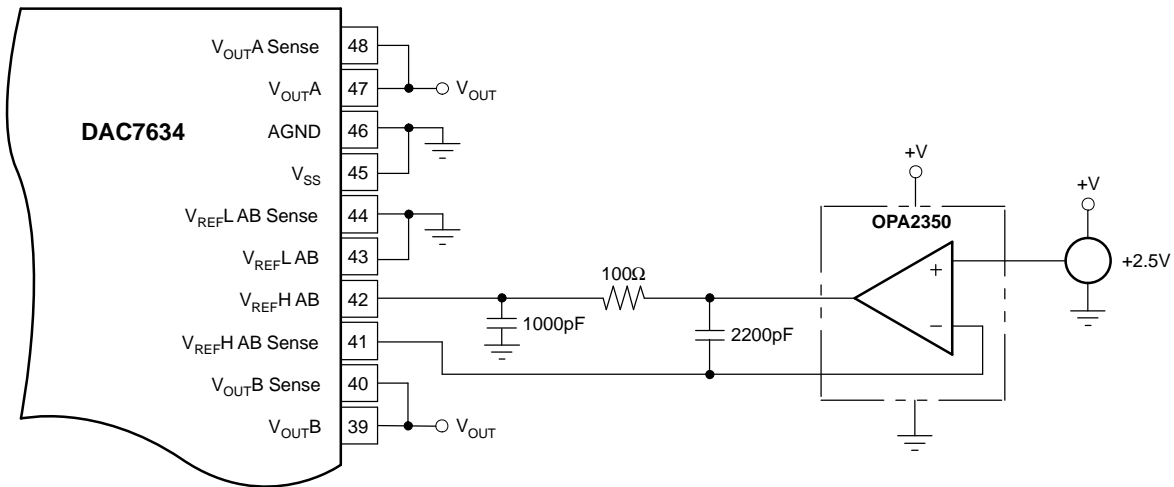


Figure 57. Single-Supply Buffered  $V_{REFH}$  (1/2 DAC7634)

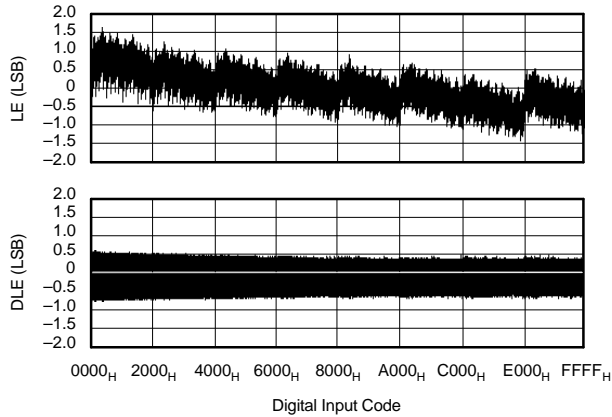


Figure 58. Linearity and Differential Linearity Error Curves for Figure 57

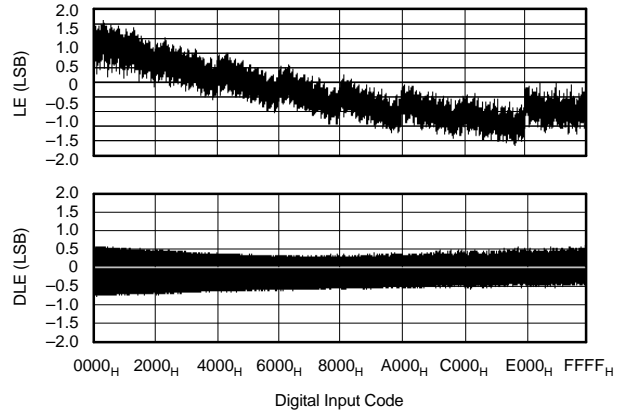


Figure 59. Linearity and Differential Linearity Error Curves for Figure 60

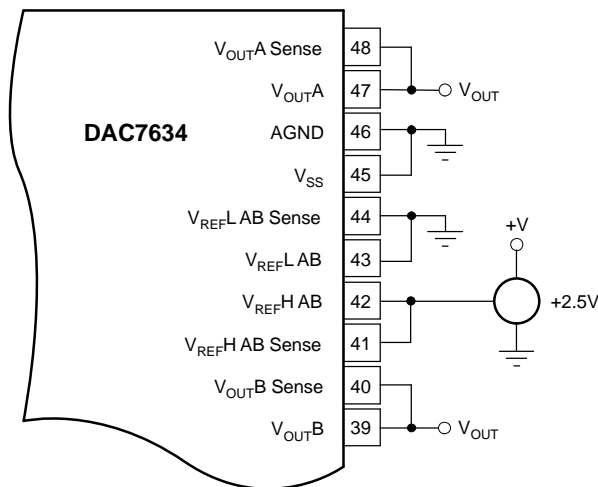


Figure 60. Low Cost Single-Supply Configuration

## DIGITAL INTERFACE

Table 1 shows the basic control logic for the DAC7634. The interface consists of a signal data clock (CLK) input, serial data (SDI), DAC input register load control signal ( $\overline{\text{LOAD}}$ ), and DAC register load control signal (LDAC). In addition, a chip select ( $\overline{\text{CS}}$ ) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Figure 15). The first two bits select the input register that is updated when  $\overline{\text{LOAD}}$  goes LOW. The third bit is a *Quick Load* bit such that if HIGH, the code in the shift register is loaded into ALL DAC's input register when  $\overline{\text{LOAD}}$  signal goes LOW. If the *Quick Load* bit is LOW, the content of shift register is loaded only to the DAC input register that is addressed. The *Quick Load* bit is followed by five unused bits. The last sixteen bits (MSB first) are the DAC code.

## SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 1. DAC7634 Logic Truth Table<sup>(1)</sup>

A1	A0	$\overline{\text{CS}}$	RST	RSTSEL	LDAC	$\overline{\text{LOAD}}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write Input	A
L	H	L	H	X	X	L	Write	Hold	Write Input	B
H	L	L	H	X	X	L	Write	Hold	Write Input	C
H	H	L	H	X	X	L	Write	Hold	Write Input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero	All
X	X	X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale	All

(1) If the DAC7634 is the only device on the serial bus, the  $\overline{\text{CS}}$  pin can be connected to DGND permanently, which enables the shift register all the time. In this case, only the CLK operates the serial shift register and all other functions listed in Table 1 should be followed as shown. The DAC updates on the rising edge of LDAC.

The internal DAC register is edge-triggered and not level-triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level-triggered via the  $\overline{\text{LOAD}}$  signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that  $\overline{\text{CS}}$  and CLK are combined with an OR

gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when  $\overline{\text{CS}}$  rises at the end of a serial transfer. If CLK is LOW when  $\overline{\text{CS}}$  rises, the OR gate provides a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both  $\overline{\text{CS}}$  and CLK are used,  $\overline{\text{CS}}$  should rise only when CLK is HIGH. If not, then either  $\overline{\text{CS}}$  or CLK can be used to operate the shift register. See Table 2 for more information.

## SERIAL-DATA OUTPUT

Table 2. Serial Shift Register Truth Table

$\overline{CS}$ (1)	CLK(1)	$\overline{LOAD}$	RST	SERIAL SHIFT REGISTER
H(2)	X(3)	H	H	No Change
L(4)	L	H	H	No Change
L	↑(5)	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H(6)	X	L(7)	H	No Change
H(6)	X	H	↑(8)	No Change

- (1)  $\overline{CS}$  and CLK are interchangeable.
- (2) H = Logic HIGH
- (3) X = Don't Care
- (4) L = Logic LOW
- (5) Positive logic transition
- (6) A HIGH value is suggested in order to avoid a *false clock* from advancing the shift register and changing the shift register.
- (7) If data is clocked into the serial register while  $\overline{LOAD}$  is LOW, the selected DAC register changes as the shift register bits *flow* through A1 and A0. This corrupts the data in each DAC register that has been erroneously selected.
- (8) Rising edge of RST causes no change in the contents of the serial shift register.

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7634, the SDO is a driven output and does not require an external pull-up. Any number of DAC7634s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in [Figure 61](#).

### DIGITAL TIMING

[Figure 62](#) and [Table 3](#) provide detailed timing for the digital interface of the DAC7634.

### DIGITAL INPUT CODING

The DAC7634 input data is in straight binary format. The output voltage is given by [Equation 1](#).

Where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

$$V_{OUT} = V_{REF}^L + \frac{(V_{REF}^H - V_{REF}^L) \times N}{65,536} \quad (1)$$

### DIGITALLY-PROGRAMMABLE CURRENT

### SOURCE

The DAC7634 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7634 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally- programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left[ \left( \frac{V_{REF}^H - V_{REF}^L}{R_{SENSE}} \right) \times \left( \frac{N}{65,536} \right) \right] + \left( V_{REF}^L / R_{SENSE} \right) \quad (2)$$

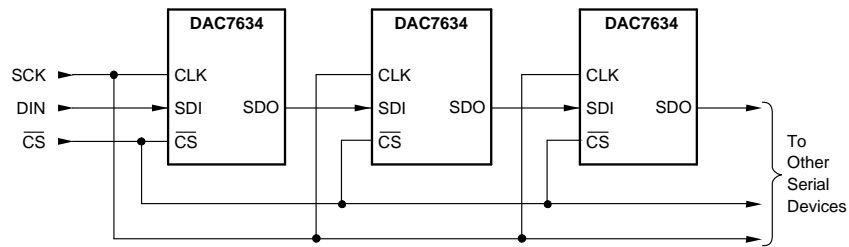


Figure 61. Daisy-Chaining DAC7634

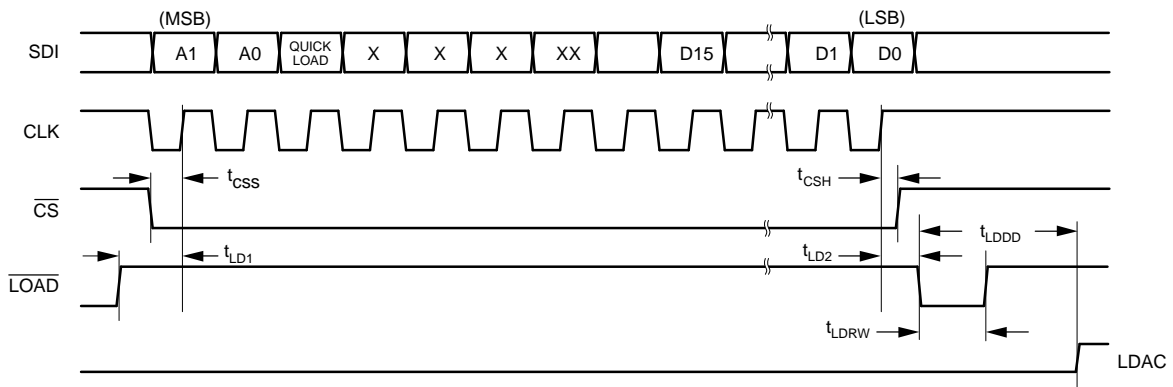


Figure 62. Serial Interface Timing

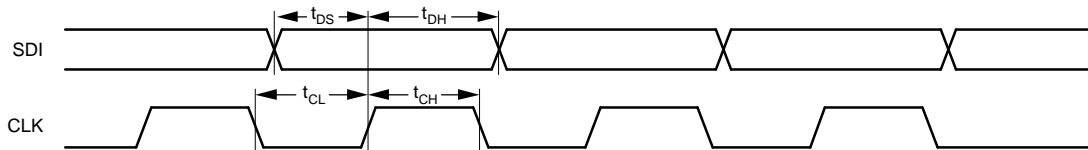


Figure 63. Data and Clock Timing

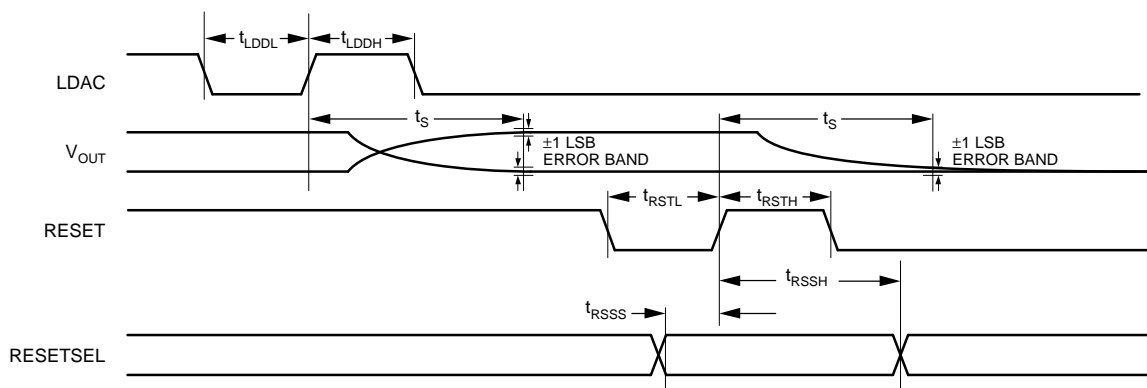


Figure 64. Reset and Output Timing



**Table 3. Timing Specifications ( $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )**

SYMBOL	DESCRIPTION	MIN	UNITS
$t_{DS}$	Data Valid to CLK Rising	10	ns
$t_{DH}$	Data Held Valid after CLK Rises	20	ns
$t_{CH}$	CLK HIGH	25	ns
$t_{CL}$	CLK LOW	25	ns
$t_{CSS}$	$\overline{CS}$ LOW to CLK Rising	15	ns
$t_{CSH}$	CLK HIGH to $\overline{CS}$ Rising	0	ns
$t_{LD1}$	$\overline{LOAD}$ HIGH to CLK Rising	10	ns
$t_{LD2}$	CLK Rising to $\overline{LOAD}$ LOW	30	ns
$t_{LDRW}$	$\overline{LOAD}$ LOW Time	30	ns
$t_{LDDL}$	LDAC LOW Time	100	ns
$t_{LDDH}$	LDAC HIGH Time	150	ns
$t_{LDDD}$	LDAC Rising from $\overline{LOAD}$ LOW	40	ns
$t_{RSSS}$	RESETSEL Valid to RESET HIGH	0	ns
$t_{RSSH}$	RESET HIGH to RESETSEL Not Valid	100	ns
$t_{RSTL}$	RESET LOW Time	10	ns
$t_{RSTH}$	RESET HIGH Time	10	ns
$t_s$	Settling Time	10	$\mu\text{s}$

Figure 65 shows a DAC7634 in a 4-mA to 20-mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left[ \left( \frac{2.5\text{ V} - 0.5\text{ V}}{125\ \Omega} \right) \times \left( \frac{N}{65,536} \right) \right] + \left( \frac{0.5\text{ V}}{125\ \Omega} \right) \quad (3)$$

At full-scale, the output current is 16 mA, plus the 4 mA, for the zero current. At zero scale, the output current is the offset current of 4 mA ( $0.5\text{ V}/125\ \Omega$ ).

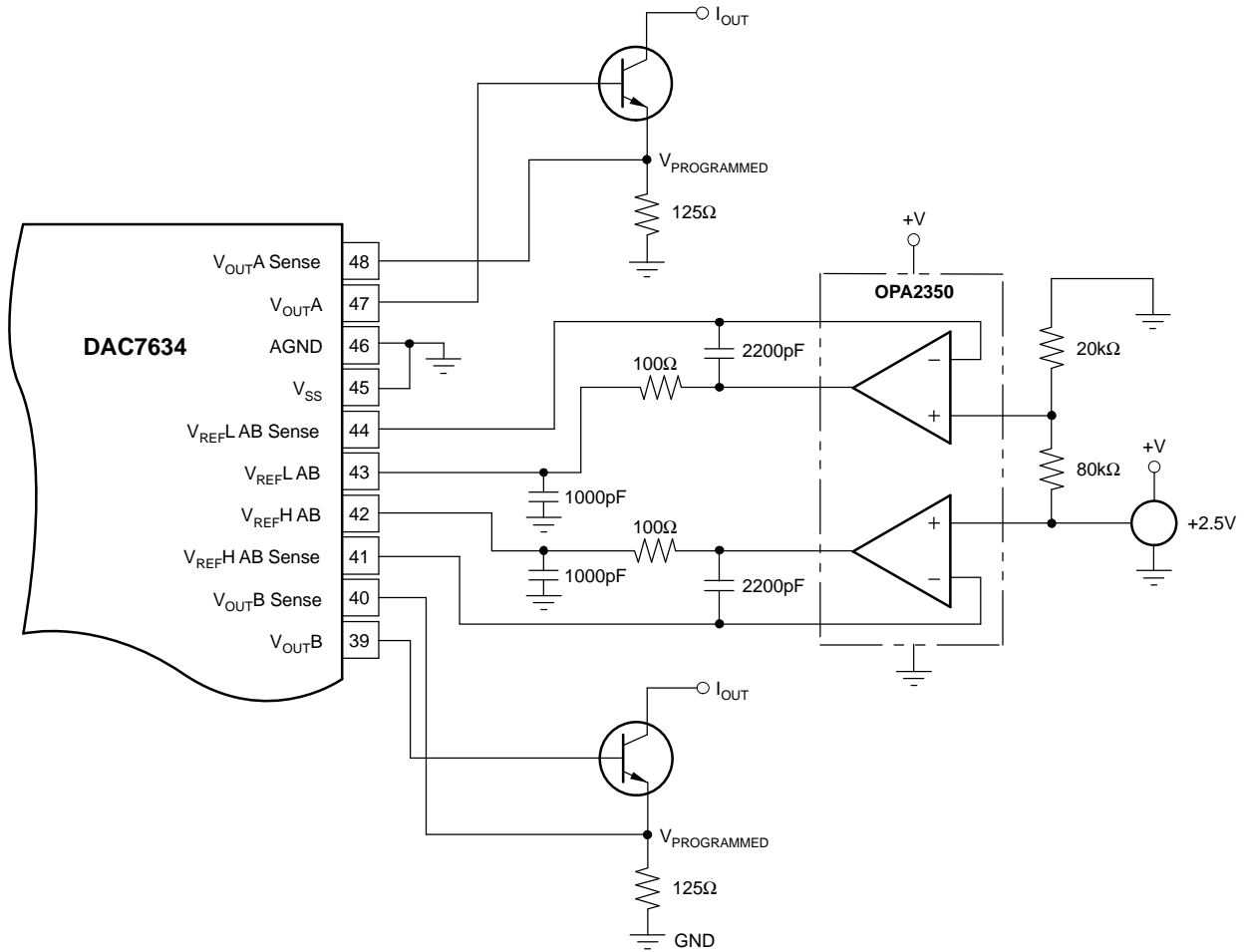


Figure 65. 4 mA to 20 mA Digitally Controlled Current Source (1/2 DAC7634)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7634E	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B	<a href="#">Samples</a>
DAC7634E/1K	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B	<a href="#">Samples</a>
DAC7634EB	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B	<a href="#">Samples</a>
DAC7634EBG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7634E B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7634E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7634E/1K	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC7634E	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634EB	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7634EBG4	DL	SSOP	48	25	473.7	14.24	5110	7.87





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