DLP470NE 0.47 インチ 1080P デジタル マイクロミラー デバイス

1 特長

- 対角 0.47 インチのマイクロミラー アレイ
  - フル HD/1080P (1920 × 1080)
  - マイクロミラー ピッチ:5.4 ミクロン
  - マイクロミラー傾斜角:±17° (平面に対して)
  - 下部光源
- 2 個の LVDS 入力データ バス
- DLP470NE チップセットの構成部品:
  - DLP470NE DMD
  - DLPC4420 コントローラ
  - DLPA100 コントローラ パワー マネージメントおよびモーター ドライバ IC

2 アプリケーション

- フル HD (1080P) ディスプレイ
- レーザー TV
- モバイル・スマート TV
- デジタル・サイネージ
- ゲーム
- ホームシアター

3 概要

テキサス・インスツルメンツ DLP® DLP470NE デジタル マイクロミラー デバイス (DMD) は、デジタル制御型の MEMS (micro-electromechanical system) 空間光変調器 (SLM) で、色鮮やかなフル HD ディスプレイ システムを実現します。DLP470NE DMD と DLPC4420 ディスプレイ コントローラ、DLPA100 コントローラ電源、モーター ドライバを組み合わせることで、高性能なシステムを実現でき、小型パッケージで高解像度と 16:9 のアスペクト比、高輝度、システムの簡素化を必要とするディスプレイ アプリケーションに最適です。DLP470NE DMD は、DLPC4430 をディスプレイ コントローラとして使用することもできます。

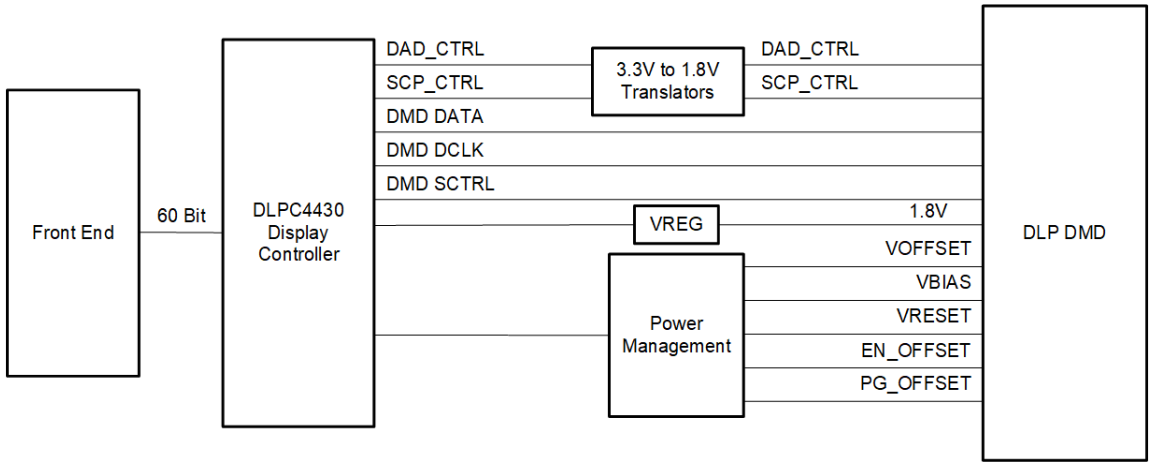
DMD のエコシステムに、設計期間の短縮に役立つ定評あるリソースが用意されています。承認済みの光学モジュール メーカーやサード パーティー プロバイダを探すには、DLP® Products サード パーティー プロバイダ検索ツールをご利用ください。

DMD を使用して設計を始める方法の詳細については、『テキサス・インスツルメンツの DLP ディスプレイ テクノロジーを使用した設計の開始』をご覧ください。

製品情報

部品番号	パッケージ(1)	パッケージ サイズ
DLP470NE	FXH (257)	33.2mm × 22.3mm

(1) 詳細については、このデータシートの末尾にある注文情報を参照してください。



DLP470NE のアプリケーション概略図

Table of Contents

4 Pin Configuration and Functions

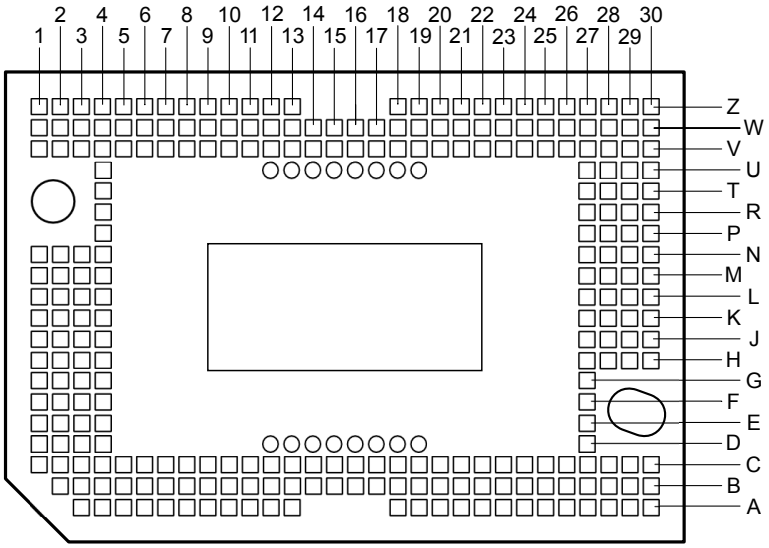


図 4-1. Series 410 257-pin FXH Bottom View

注意

To ensure reliable, long-term operation of the .47-inch 1080P s410 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the *PCB Design Requirements for TI DLP Standard TRP Digital Micromirror Devices* application report before designing the board.

表 4-1. Pin Functions

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_AN(0)	C6	NC	LVDS	DDR	Differential	No connect	805.0
D_AN(1)	C3						
D_AN(2)	E1						
D_AN(3)	C4						
D_AN(4)	D1						
D_AN(5)	B8						
D_AN(6)	F4						
D_AN(7)	E3						
D_AN(8)	C11						
D_AN(9)	F3						
D_AN(10)	K4						
D_AN(11)	H3						
D_AN(12)	J3						
D_AN(13)	C13						
D_AN(14)	A5						
D_AN(15)	A3						

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_AP(0)	C7	NC	LVDS	DDR	Differential	No connect	805.0
D_AP(1)	C2						
D_AP(2)	E2						
D_AP(3)	B4						
D_AP(4)	C1						
D_AP(5)	B7						
D_AP(6)	E4						
D_AP(7)	D3						
D_AP(8)	C12						
D_AP(9)	F2						
D_AP(10)	J4						
D_AP(11)	G3						
D_AP(12)	J2						
D_AP(13)	C14						
D_AP(14)	A6						
D_AP(15)	A4						
D_BN(0)	N4	NC	LVDS	DDR	Differential	No connect	805.0
D_BN(1)	Z11						
D_BN(2)	W4						
D_BN(3)	W10						
D_BN(4)	L1						
D_BN(5)	V8						
D_BN(6)	W6						
D_BN(7)	M1						
D_BN(8)	R4						
D_BN(9)	W1						
D_BN(10)	U4						
D_BN(11)	V2						
D_BN(12)	Z5						
D_BN(13)	N3						
D_BN(14)	Z2						
D_BN(15)	L4						

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_BP(0)	M4	NC	LVDS	DDR	Differential	No connect	805.0
D_BP(1)	Z12						
D_BP(2)	Z4						
D_BP(3)	Z10						
D_BP(4)	L2						
D_BP(5)	V9						
D_BP(6)	W7						
D_BP(7)	N1						
D_BP(8)	P4						
D_BP(9)	V1						
D_BP(10)	T4						
D_BP(11)	V3						
D_BP(12)	Z6						
D_BP(13)	N2						
D_BP(14)	Z3						
D_BP(15)	L3						
D_CN(0)	H27	I	LVDS	DDR	Differential	Data negative	805.0
D_CN(1)	A20						
D_CN(2)	H28						
D_CN(3)	K28						
D_CN(4)	K30						
D_CN(5)	C23						
D_CN(6)	G27						
D_CN(7)	J30						
D_CN(8)	B24						
D_CN(9)	A21						
D_CN(10)	A27						
D_CN(11)	C29						
D_CN(12)	A26						
D_CN(13)	C25						
D_CN(14)	A29						
D_CN(15)	C30						

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_CP(0)	J27	I	LVDS	DDR	Differential	Data positive	805.0
D_CP(1)	A19						
D_CP(2)	H29						
D_CP(3)	K27						
D_CP(4)	K29						
D_CP(5)	C22						
D_CP(6)	F27						
D_CP(7)	H30						
D_CP(8)	B25						
D_CP(9)	B21						
D_CP(10)	B27						
D_CP(11)	C28						
D_CP(12)	A25						
D_CP(13)	C24						
D_CP(14)	A28						
D_CP(15)	B30						
D_DN(0)	V25	I	LVDS	DDR	Differential	Data negative	805.0
D_DN(1)	V28						
D_DN(2)	T30						
D_DN(3)	V27						
D_DN(4)	U30						
D_DN(5)	W23						
D_DN(6)	R27						
D_DN(7)	T28						
D_DN(8)	V20						
D_DN(9)	R28						
D_DN(10)	L27						
D_DN(11)	N28						
D_DN(12)	M28						
D_DN(13)	V18						
D_DN(14)	Z26						
D_DN(15)	Z28						

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_DP(0)	V24	I	LVDS	DDR	Differential	Data positive	805.0
D_DP(1)	V29						
D_DP(2)	T29						
D_DP(3)	W27						
D_DP(4)	V30						
D_DP(5)	W24						
D_DP(6)	T27						
D_DP(7)	U28						
D_DP(8)	V19						
D_DP(9)	R29						
D_DP(10)	M27						
D_DP(11)	P28						
D_DP(12)	M29						
D_DP(13)	V17						
D_DP(14)	Z25						
D_DP(15)	Z27						
SCTRL_AN	G1	NC	LVDS	DDR	Differential	No connect	805.0
SCTRL_AP	F1						
SCTRL_BN	V5						
SCTRL_BP	V4						
SCTRL_CN	C26	I	LVDS	DDR	Differential	Serial control negative	805.0
SCTRL_CP	C27	I	LVDS	DDR	Differential	Serial control positive	805.0
SCTRL_DN	P30	I	LVDS	DDR	Differential	Serial control negative	805.0
SCTRL_DP	R30	I	LVDS	DDR	Differential	Serial control positive	805.0
DCLK_AN	H2	NC	LVDS		Differential	No connect	805.0
DCLK_AP	H1						
DCLK_BN	V6						
DCLK_BP	V7						
DCLK_CN	D27	I	LVDS		Differential	Clock negative	805.0
DCLK_CP	E27	I	LVDS		Differential	Clock positive	805.0
DCLK_DN	N29	I	LVDS		Differential	Clock negative	805.0
DCLK_DP	N30	I	LVDS		Differential	Clock positive	805.0
SCPCLK	A10	I	LVCMOS		Pull down	Serial communications port clock. Active only when SCPENZ is logic low	
SCPDI	A12	I	LVCMOS	SDR	Pull down	Serial communications port data input. Synchronous to SCPCLK rising edge	
SCPENZ	C10	I	LVCMOS		Pull down	Serial communications port enable active low	
SCPDO	A11	O	LVCMOS	SDR		Serial communications port output	
RESET_ADDR(0)	Z13	I	LVCMOS		Pull down	Reset driver address select	
RESET_ADDR(1)	W13						
RESET_ADDR(2)	V10						
RESET_ADDR(3)	W14						

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
RESET_MODE(0)	W9	I	LVCMOS		Pull down	Reset driver mode select	
RESET_SEL(0)	V14					Reset driver level select	
RESET_SEL(1)	Z8					Reset driver level select	
RESET_STROBE	Z9	I	LVCMOS		Pull down	Rising edge latches in RESET_ADDR, RESET_MODE, and RESET_SEL	
PWRDNZ	A8	I	LVCMOS		Pull down	Active low device reset	
RESET_OEZ	W15	I	LVCMOS		Pull up	Active low output enable for internal reset driver circuits	
RESET_IRQZ	V16	O	LVCMOS			Active low output interrupt to DLP display controller	
EN_OFFSET	C9	O	LVCMOS			Active high enable for external VOFFSET regulator	
PG_OFFSET	A9	I	LVCMOS		Pull up	Active low fault from external VOFFSET regulator	
TEMP_N	B18		Analog			Temperature sensor diode cathode	
TEMP_P	B17		Analog			Temperature sensor diode anode	
RESERVED	D12, D13, D14, D15, D16, D17, D18, D19, U12, U13, U14, U15	NC	Analog		Pull Down	Do not connect on DLP system board. No connect. No electrical connections from CMOS bond pad to package pin	
No Connect	U16, U17, U18, U19	NC				No connect. No electrical connection from CMOS bond pad to package pin	
RESERVED_BA	W11	O	LVCMOS			Do not connect on DLP system board.	
RESERVED_BB	B11						
RESERVED_BC	Z20						
RESERVED_BD	C18						
RESERVED_PFE	A18	I	LVCMOS		Pull down	Connect to ground on DLP system board.	
RESERVED_TM	C8						
RESERVED_TP0	Z19	I	Analog			Do not connect on DLP system board.	
RESERVED_TP1	W20						
RESERVED_TP2	W19						
VBIAS[1]	C15, C16, V11, V12	P	Analog			Supply voltage for positive bias level of micromirror reset signal	
VRESET[1]	G4, H4, J1, K1	P	Analog			Supply voltage for negative reset level of micromirror reset signal	
VOFFSET[1]	A30, B2, M30, Z1, Z30	P	Analog			Supply voltage for HVCMOS logic. Supply voltage for positive offset level of micromirror reset signal. Supply voltage for stepped high voltage at micromirror address electrodes	

表 4-1. Pin Functions (続き)

PIN		I/O[3]	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
VCC[1]	A24, A7, B10, B13, B16, B19, B22, B28, B5, C17, C20, D4, J29, K2, L29, M2, N27, U27, V13, V15, V22, W17, W21, W26, W29, W3, Z18, Z23, Z29, Z7	P	Analog			Supply voltage for LVCMOS core. Supply voltage for positive offset level of micromirror reset signal during Power down. Supply voltage for normal high level at micromirror address electrodes	
VSS[2]	A13, A22, A23, B12, B14, B15, B20, B23, B26, B29, B3, B6, B9, C19, C21, C5, D2, G2, J28, K3, L28, L30, M3, P27, P29, U29, V21, V23, V26, W12, W16, W18, W2, W22, W25, W28, W30, W5, W8, Z21, Z22, Z24	G				Device ground. Common return for all power	

(1) V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies must be connected for proper DMD operation.
(2) V_{SS} must be connected for proper DMD operation.
(3) I = Input, O = Output, P = Power, G = Ground, NC = No connect

5 Specifications

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
V_{CC}	Supply voltage for LVCMOS core logic(1)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(1) (2)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(1)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(1)	–15	–0.3	V
$\lvert V_{BIAS} – V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(3)		11	V
$\lvert V_{BIAS} – V_{RESET} \rvert$	Supply voltage difference (absolute value)(4)		34	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins(1)	–0.5	V_{CC} + 0.5	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(5)		500	mV
I_{ID}	Input differential current(6)		6.3	mA
Clocks				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_C		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_D		400	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Temperature, operating(7)	0	90	°C
	Temperature, non–operating(7)	–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 (8)		30	°C
T_{DP}	Dew point temperature, operating and non–operating (noncondensing)		81	°C

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified voltages.
(3) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(4) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(5) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(6) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(7) The highest temperature of the active array (as calculated using Micromirror Array Temperature Calculation) or of any point along the window edge as defined in 図 6-2. The locations of thermal test points TP2, TP3, TP4 and TP5 in 図 6-2 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, use that point.
(8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 6-2. The window test points TP2, TP3, TP4, and TP5 shown in 図 6-2 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, use that point.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range , (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Limit the exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	–14.5	–14	–13.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(3)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value)(4)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage(5)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(5)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(5)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(5)	–0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse duration(6)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(7)			500	kHz
t_{SCP_PD}	Propagation delay, Clock to Q, from rising–edge of SCPCLK to valid SCPDO(8)	0		900	ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the first rising- edge of SCPCLK	1			µs
$t_{SCP\_POS\_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t_{SCP_DS}	SCPDI Clock setup time (before SCPCLK falling edge)(8)	800			ns
t_{SCP_DH}	SCPDI Hold time (after SCPCLK falling edge)(8)	900			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse duration (high level)	2			µs

5.4 Recommended Operating Conditions (続き)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(9)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)(10)	150	300	440	mV
V_{CM}	Common mode voltage(10)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(10)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long–term operational(11) (12) (13)	10		40 to 70(14)	°C
	Array temperature, short–term operational, 500-hour max(12) (15)	0		10	°C
T_{WINDOW}	Window temperature – operational(16) (22)			85	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(17)			14	°C
$T_{DP\ -AVG}$	Average dew point temperature (non-condensing)(18)			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing)(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{θ}	Illumination marginal ray angle(22)			55	degrees
SOLID STATE ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 410nm(11) (21)			10	mW/cm2
ILL_{VIS}	Illumination power at wavelengths ≥ 410nm and ≤ 800nm(20) (21)			44.9	W/cm2
ILL_{IR}	Illumination power at wavelengths > 800nm(21)			10	mW/cm2
ILL_{BLU}	Illumination power at wavelengths ≥ 410nm and ≤ 475nm(20) (21)			14.3	W/cm2
ILL_{BLU1}	Illumination power at wavelengths ≥ 410nm and ≤ 440nm (20) (21)			2.3	W/cm2
LAMP ILLUMINATION					
ILL_{UV}	Illumination power at wavelengths < 395nm(11) (21)			2.0	mW/cm2
ILL_{VIS}	Illumination power at wavelengths ≥ 395nm and ≤ 800nm(20) (21)			36.8	W/cm2
ILL_{IR}	Illumination power at wavelengths > 800nm(21)			10	mW/cm2

(1) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(2) V_{OFFSET} supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified limit. See セクション 8, 図 8-1, 表 8-1.
(4) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than specified limit. See セクション 8, 図 8-1, 表 8-1.
(5) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, “Low-Power Double Data Rate (LPDDR)” JESD209B.Tester Conditions for VIH and VIL.
- Frequency = 60MHz. Maximum Rise Time = 2.5ns @ (20% – 80%)
- Frequency = 60MHz. Maximum Fall Time = 2.5ns @ (80% – 20%)

(6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(7) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(8) See 図 5-2
(9) See LVDS Timing Requirements in セクション 5.8 and 図 5-6.
(10) Refer to 図 5-5.
(11) Simultaneous exposure of the DMD to the maximum セクション 5.4 for temperature and UV illumination reduces device lifetime.
(12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 6-2 and the package セクション 5.5 using the calculation in セクション 6.6.
(13) Long-term is defined as the usable life of the device.

(14) Per 図 5-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See セクション 6.8 for a definition of micromirror landed duty cycle.
(15) Short-term is defined as cumulative time over the usable life of the device.
(16) The locations of thermal test points TP2, TP3, TP4, and TP5 in 図 6-2 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 6-2. The window test points TP2, TP3, TP4, and TP5 shown in 図 6-2 are intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
(20) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature (T_{ARRAY}).
(21) To calculate see セクション 6.7.
(22) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

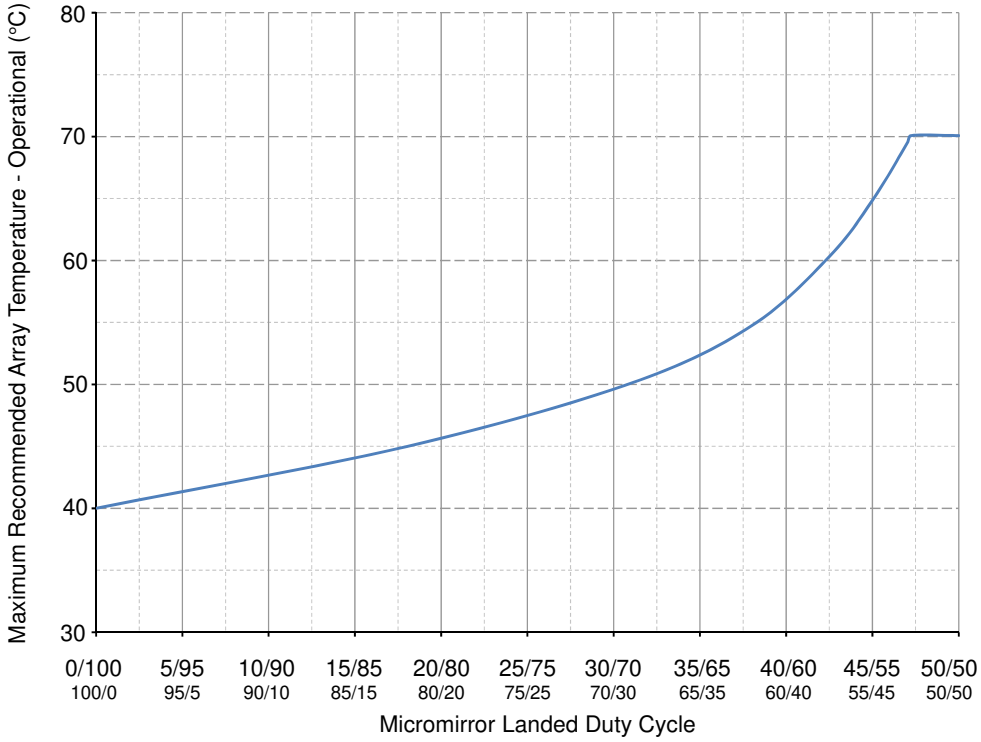


図 5-1. Maximum Recommended Array Temperature—Derating Curve

5.5 Thermal Information

THERMAL METRIC	DLP470NE FXH Package 257 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.90	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*.
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.
Optical systems must be designed to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
V_{OH}	High level output voltage	V_{CC} = 1.8V, I_{OH} = –2mA	0.8 × V_{CC}			V
V_{OL}	Low level output voltage	V_{CC} = 1.95V, I_{OL} = 2mA			0.2 × V_{CC}	V
I_{OZ}	High impedance output current	V_{CC} = 1.95V	–40		25	µA
I_{IL}	Low level input current	V_{CC} = 1.95V, V_I = 0	–1			µA
I_{IH}	High level input current(2) (3)	V_{CC} = 1.95V, V_I = V_{CC}			110	µA
I_{CC}	Supply current VCC	V_{CC} = 1.95V			715	mA
I_{OFFSET}	Supply current VOFFSET(3)	V_{OFFSET} = 10.5V			7	mA
I_{BIAS}	Supply current VBIAS(3) (4)	V_{BIAS} = 18.5V			2.75	mA
I_{RESET}	Supply current VRESET(4)	V_{RESET} = –14.5V			-5	mA
P_{CC}	Supply power dissipation V_{CC}	V_{CC} = 1.95V			1394.25	mW
P_{OFFSET}	Supply power dissipation V_{OFFSET} (3)	V_{OFFSET} = 10.5V			73.50	mW
P_{BIAS}	Supply power dissipation V_{BIAS} (3) (4)	V_{BIAS} = 18.5V			50.87	mW
P_{RESET}	Supply power dissipation V_{RESET} (4)	V_{RESET} = 14.5V			72.5	mW
P_{TOTAL}	Supply power dissipation V_{TOTAL}				1591.12	mW

(1) All voltage values are with respect to the ground pins (VSS).
(2) Applies to LVCMOS pins only. Excludes LVDS pins and MBRST (15:0) pins.
(3) To prevent excess current, the supply voltage difference |VBIAS – VOFFSET| must be less than the specified limits listed in the *Recommended Operating Conditions* table.
(4) To prevent excess current, the supply voltage difference |VBIAS – VRESET| must be less than the specified limit in *Recommended Operating Conditions*.

5.7 Capacitance at Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{I_lvds}	LVDS input capacitance 2xLVDS	f = 1MHz			20	pF
$C_{I\_nonlvds}$	Non-LVDS input capacitance 2xLVDS	f = 1MHz			20	pF
C_{I_tdiode}	Temperature diode input capacitance 2xLVDS	f = 1MHz			30	pF
C_O	Output capacitance	f = 1MHz			20	pF

5.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP(1)						
t_r	Rise time	20% to 80% reference points			30	ns
t_f	Fall time	80% to 20% reference points			30	ns
LVDS(2)						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock cycle	DCLK_C,LVDS pair	2.5			ns
		DCLK_D, LVDS pair	2.5			ns
t_W	Pulse duration	DCLK_C LVDS pair	1.19	1.25		ns
		DCLK_D LVDS pair	1.19	1.25		ns
t_{Su}	Setup time	D_C(15:0) before DCLK_C, LVDS pair	0.275			ns
		D_D(15:0) before DCLK_D, LVDS pair	0.275			ns
		SCTRL_C before DCLK_C, LVDS pair	0.275			ns
		SCTRL_D before DCLK_D, LVDS pair	0.275			ns
t_h	Hold time	D_C(15:0) after DCLK_C, LVDS pair	0.195			ns
		D_D(15:0) after DCLK_D, LVDS pair	0.195			ns
		SCTRL_C after DCLK_C, LVDS pair	0.195			ns
		SCTRL_D after DCLK_D, LVDS pair	0.195			ns
t_{SKEW}	Skew time	Channel D relative to Channel C(3) (4), LVDS pair	–1.25		1.25	ns

(1) See 図 5-3 for Rise Time and Fall Time for SCP.
(2) See 図 5-5 for Timing Requirements for LVDS.
(3) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0) and D_CP(15:0).
(4) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0) and D_DP(15:0).

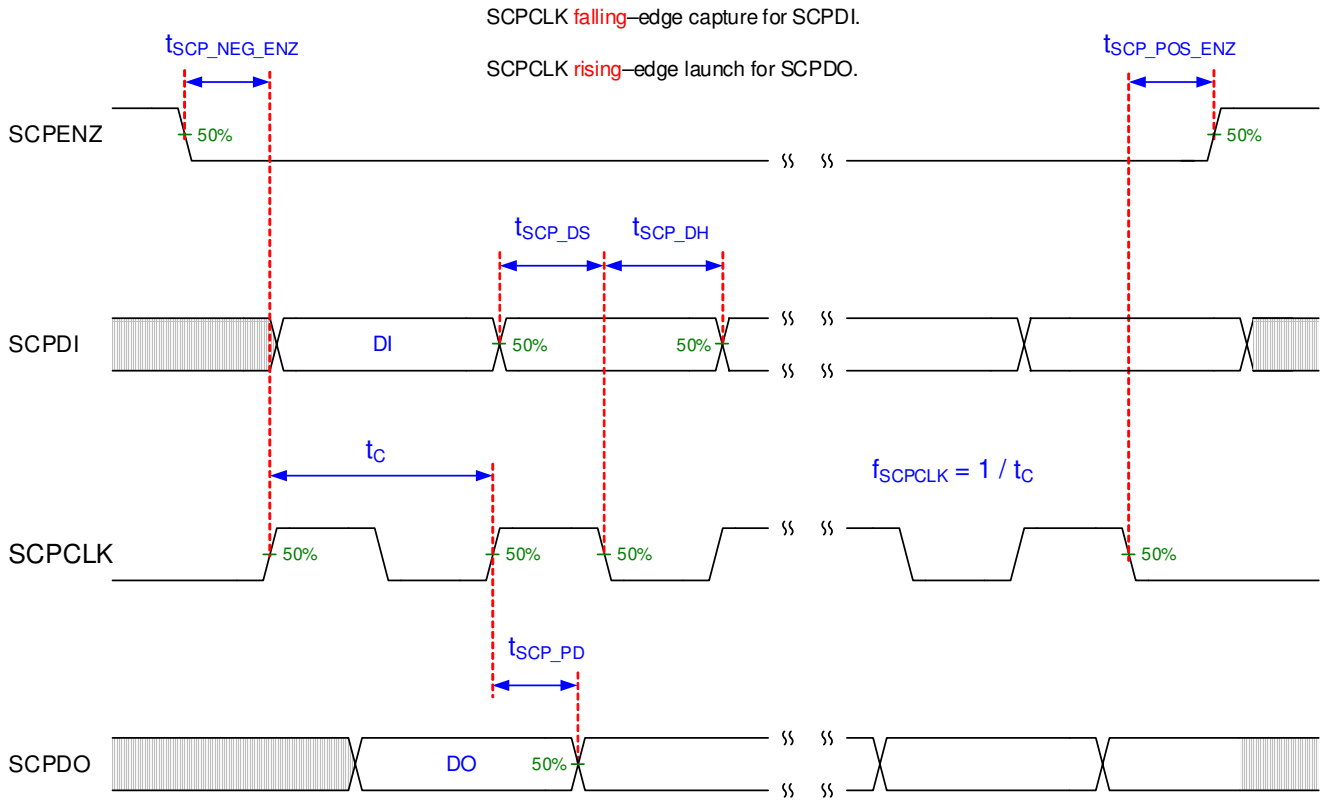


図 5-2. SCP Timing Requirements

See Recommended Operating Conditions for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH}, and t_{SCP_PD} specifications.

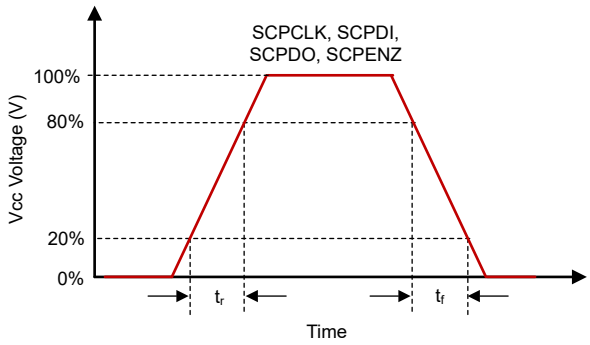


図 5-3. SCP Requirements for Rise and Fall

See Timing Requirements for t_r and t_f specifications and conditions.

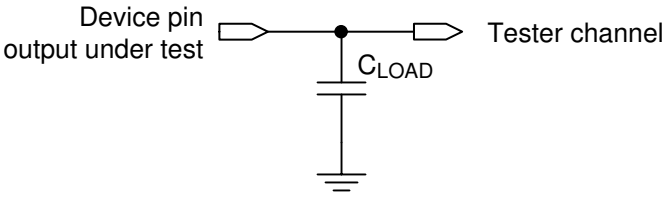


図 5-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. See 図 5-4.

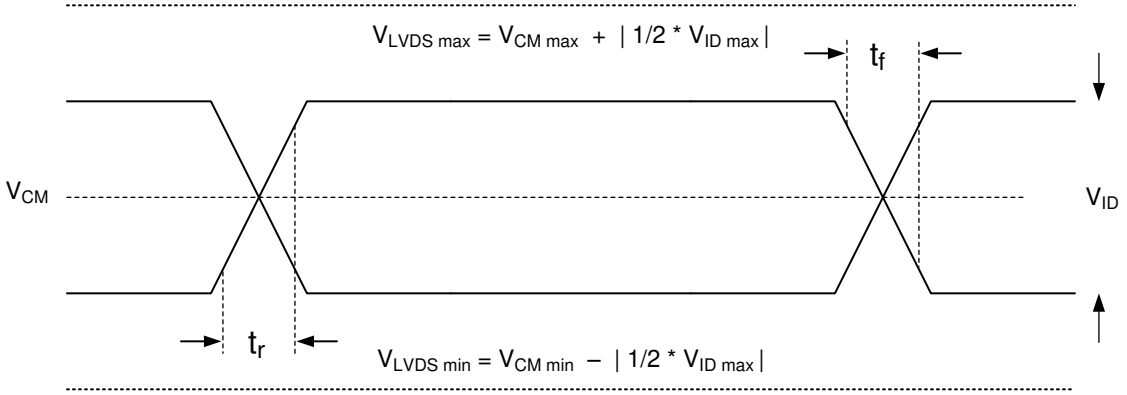


図 5-5. LVDS Waveform Requirements

See Recommended Operating Conditions for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

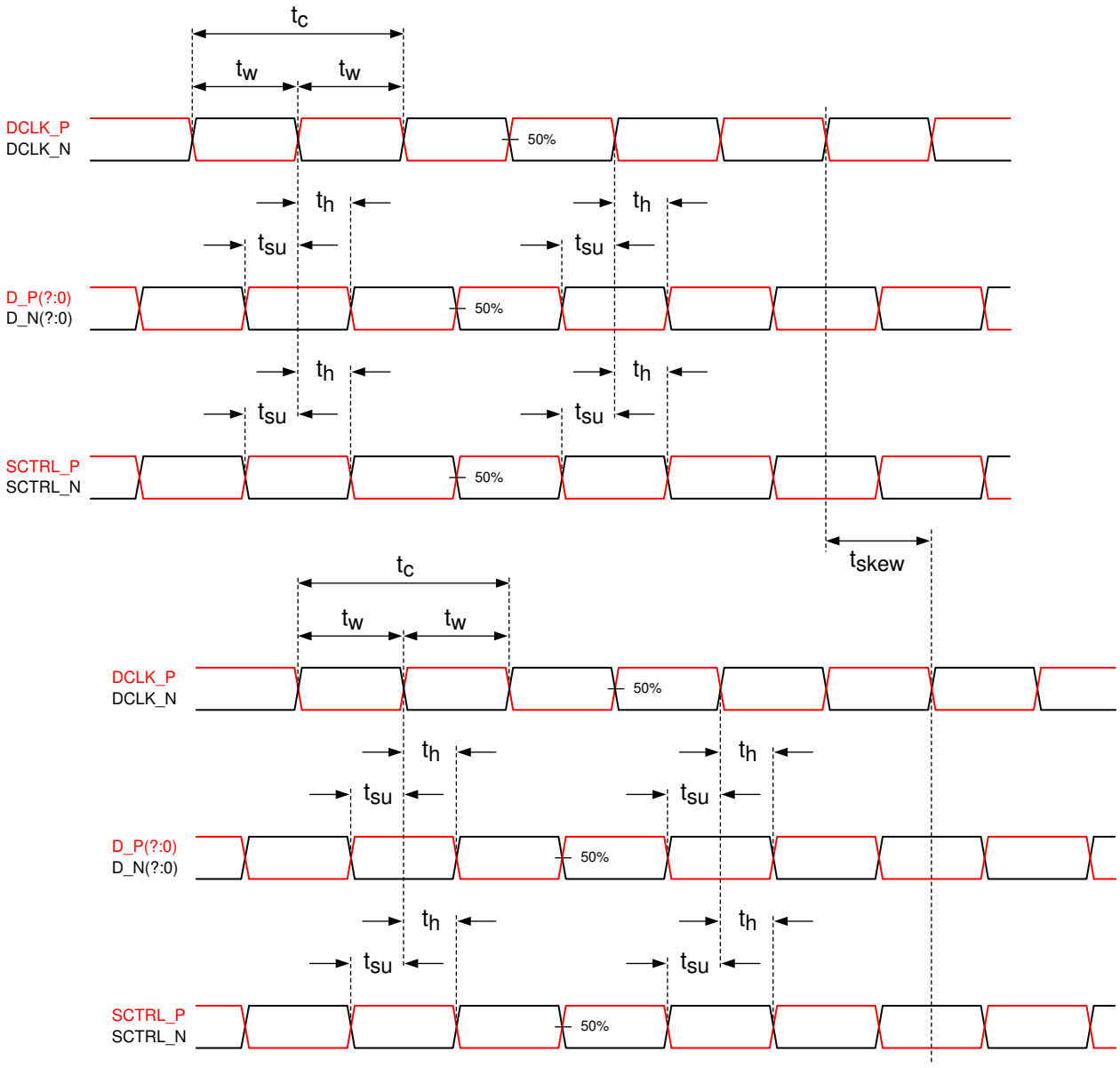


図 5-6. Timing Requirements

See Timing Requirements for timing requirements and LVDS pairs per channel (bus) defining D_P(?:0) and D_N(?:0).

5.9 System Mounting Interface Loads

表 5-1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Thermal interface area(1)			12	kg
Electrical interface area(1)			25	kg

(1) Uniformly distributed within area shown in 図 5-7

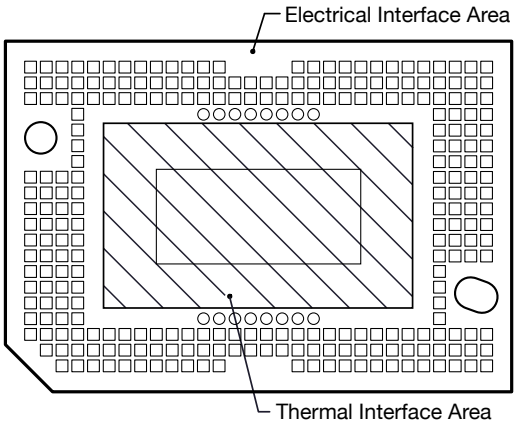


図 5-7. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

表 5-2. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1)	M	1920	micromirrors
Number of active rows (1)	N	1080	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width (1)	Micromirror Pitch × number of active columns	10.368	mm
Micromirror active array height (1)	Micromirror Pitch × number of active rows	5.832	mm
Micromirror active border (Top / Bottom) (2)	Pond of micromirrors (POM)	80	micromirrors/side
Micromirror active border (Right / Left) (2)	Pond of micromirrors (POM)	84	micromirrors/side

(1) See 図 5-8.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the *Pond Of Mirrors* (POM). These micromirrors are structurally and electrically prevented from tilting toward the bright or ON state but still require an electrical bias to tilt toward the OFF state.

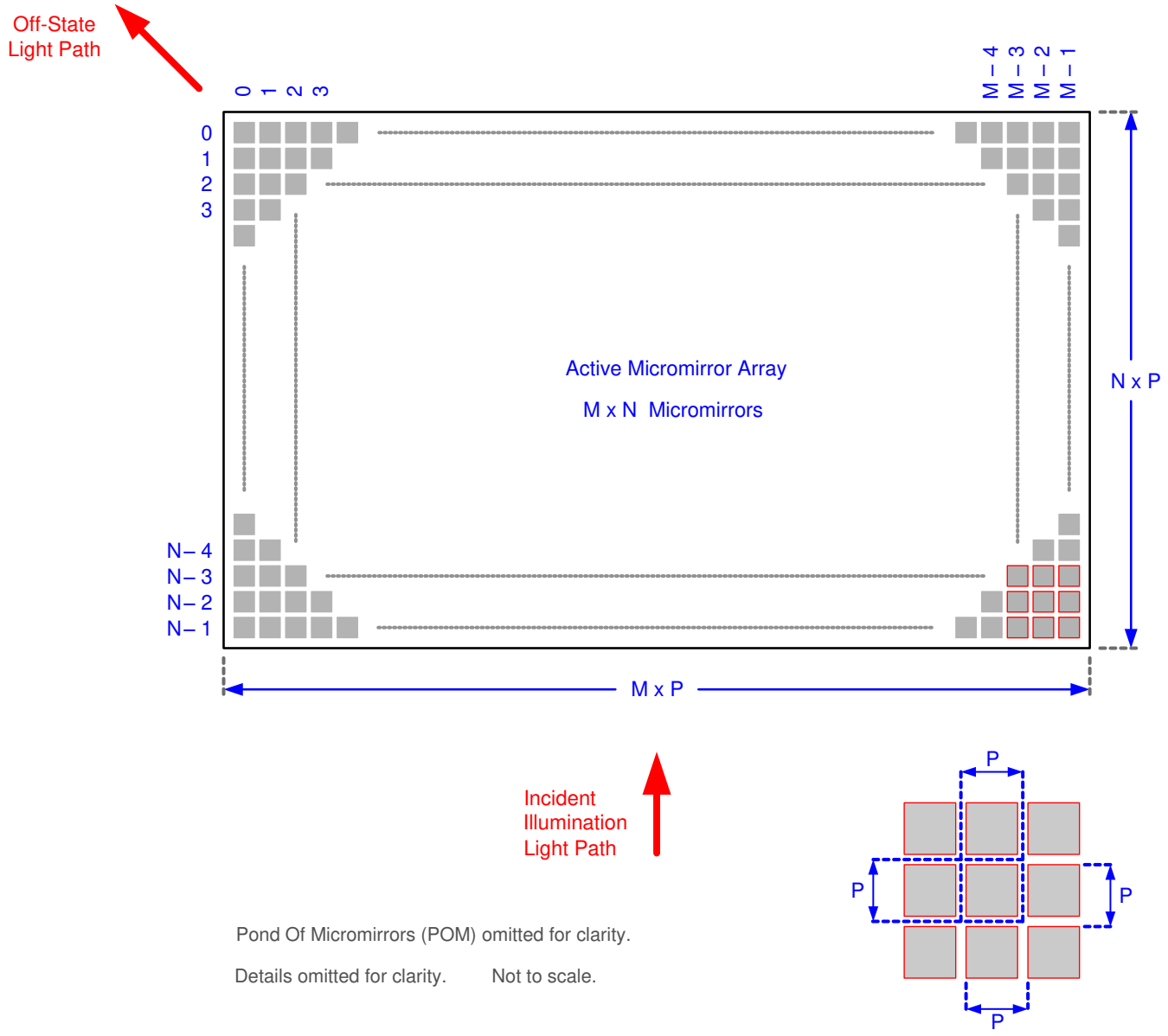


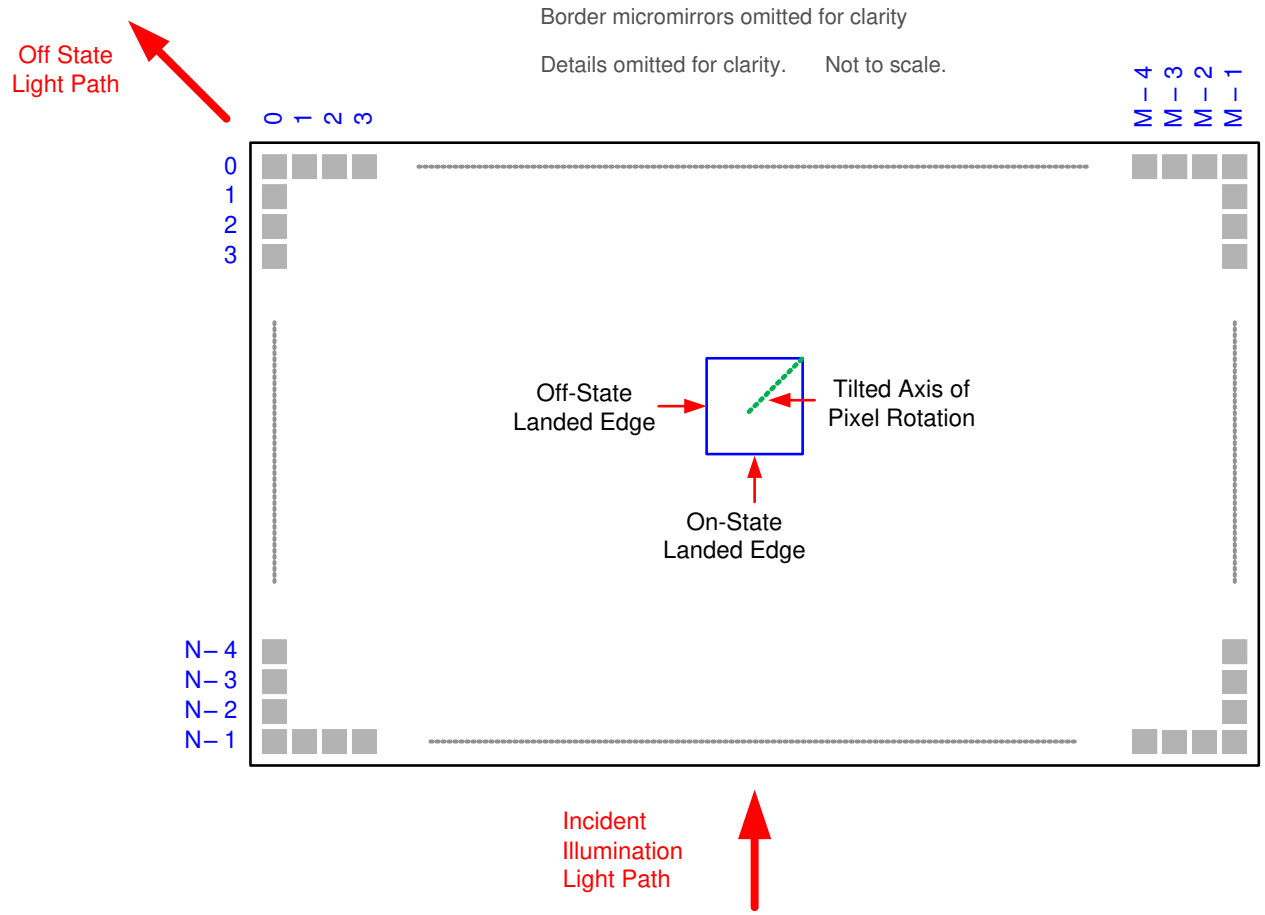
図 5-8. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
Micromirror tilt angle, variation device to device (2) (3) (4) (5)		Landed State(1)	15.6	17	18.4	degrees
Image performance(6)	Bright pixel(s) in active area(7)	Gray 10 screen(10)			0	micromirrors
	Bright pixel(s) in the POM(7) (9)	Gray 10 screen(10)			1	
	Dark pixel(s) in the active area(8)	White screen(11)			4	
	Adjacent pixel(s)(12)	Any screen			0	
	Unstable pixel(s) in active area(13)	Any screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) This represents the variation that can occur between any two individual micromirrors, locaed on the same device or located on different devices.
(4) For some applications it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(5) See figure 図 5-9.
(6) Conditions of acceptance. All DMD image performance returns are evaluated using the following projected image test conditions:
- Test set degamma shall be linear.
- Test set brightness and contrast shall be set to nominal.
- The diagonal size of the projected image shall be a minimum of 60 inches.
- The projections screen shall be a 1× gain.
- The projected image shall be inspected from an 8-foot minimum viewing distance.
- The image shall be in focus during all image performance tests.

(7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
(8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
(9) POM definition: The rectangular border of off-state mirrors surrounding the active area.
(10) Gray 10 screen definition: A full screen with RGB values set to R=10/255, G=10/255, B=10/255.
(11) White screen definition: A full screen with RGB values set to R=255/255, G=255/255, B=255/255.
(12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point. Also referred to as a cluster.
(13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.



A. Pond of Mirrors (POM) omitted for clarity
B. Refer to Micromirror Array Physical Characteristics table for M, N, and P specifications.

図 5-9. Micromirror Landed Orientation and Tilt

5.12 Window Characteristics

表 5-3. DMD Window Characteristics

DESCRIPTION	MIN	NOM
Window Material		Corning Eagle XG
Window Refractive Index at 546.1nm		1.5119
Window Transmittance, minimum within the wavelength range between 420nm and 680nm. Applies to all angles between 0°–30° AOI. (1) (2)	97%	
Window Transmittance, average over the wavelength range 420nm and 680nm. Applies to all angles 30°–45° AOI. (1) (2)	97%	

(1) Single-pass through both surfaces and glass.
(2) The angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

5.13 Chipset Component Usage Specification

The DLP470NE DMD's reliable function and operation require that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

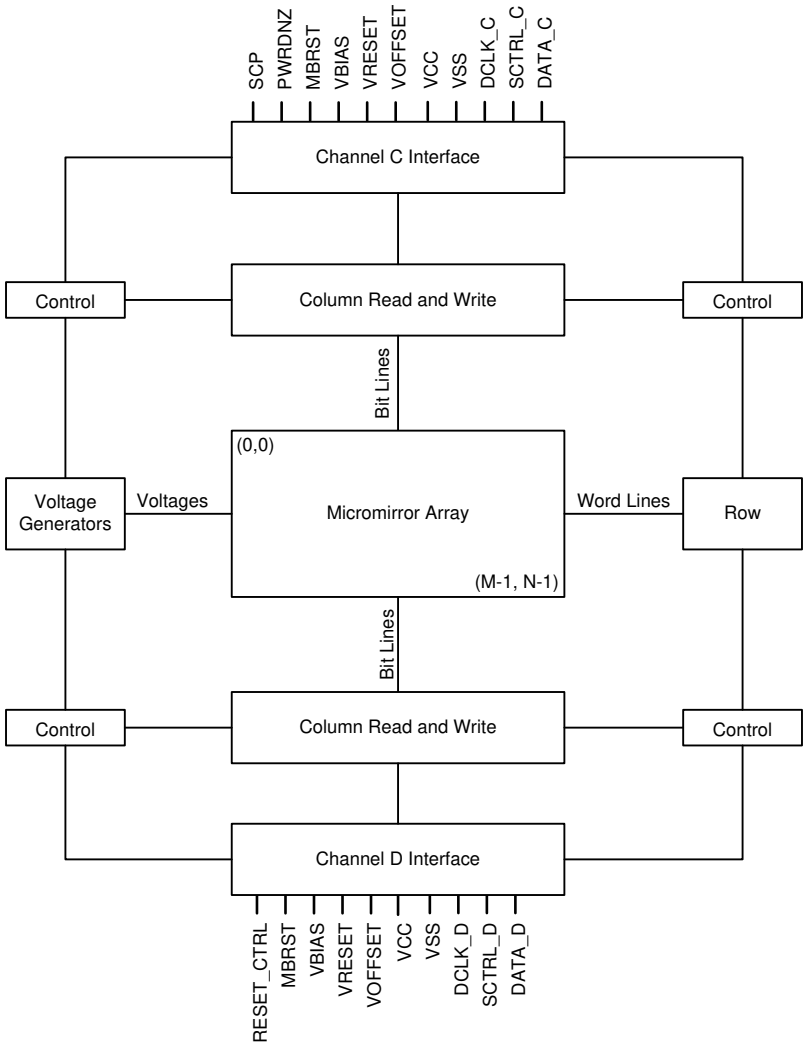
6 Detailed Description

6.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the セクション 6.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP470NE DMD is part of the chipset comprising of the DLP470NE DMD, the DLPC4420 display controller, and the DLPA100 power and motor driver. To ensure reliable operation, the DLP470NE DMD must always be used with the DLPC4420 display controller and the DLPA100 power and motor driver.

6.2 Functional Block Diagram



For pin details on Channels C, and D, refer to Pin Configuration and Functions and LVDS Interface section of セクション 5.8. RESET_CTRL is used in applications when an external reset signal is required.

図 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power Interface

The DMD requires five DC voltages: DMD_P3P3V, DMD_P1P8V, VOFFSET, VRESET, and VBIAS. DMD_P3P3V is created by the DLPA100 power and motor driver and is used on the DMD board to create the other four DMD voltages, as well as powering various peripherals (TMP411, I2C, and TI level translators). DMD_P1P8V is created by the TI PMIC LP38513S and provides the VCC voltage required by the DMD. VOFFSET (10V), VRESET (-14V), and VBIAS (18V) are made by the TI PMIC TPS65145 and are supplied to the DMD to control the micromirrors.

6.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 5-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers: Use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. See the *DLPC4420 Display Controller Data Sheet* or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade-offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area needs to be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast degradation and objectionable artifacts may occur in the display border or active area.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical

system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level to be acceptable.

6.6 Micromirror Array Temperature Calculation

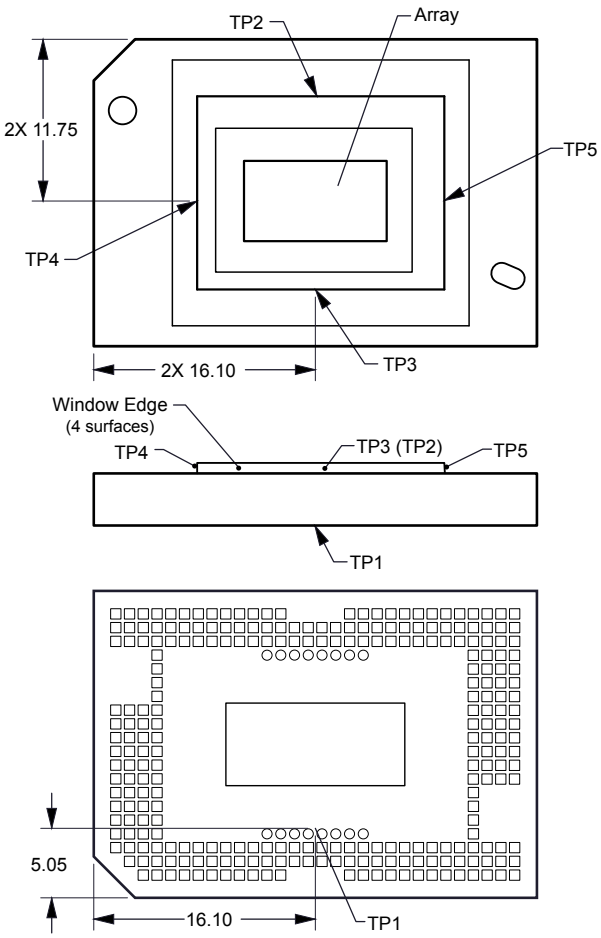


図 6-2. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The following equations show the relationship between array temperature and the reference ceramic temperature, thermal test TP1 図 6-2 shown above:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + (Q_{ILLUMINATION})$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 図 6-2
- $R_{ARRAY–TO–CERAMIC}$ = Thermal resistance of package specified in セクション 5.5 from array to ceramic TP1 図 6-2 (°C/W).
- Q_{ARRAY} = Total DMD Power (electrical + absorbed) on the array (W)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)

- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$ (W)
- DMD average thermal absorptivity = 0.41

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.9W. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$Q_{INCIDENT}$ = 31W (measured)

$T_{CERAMIC}$= 55.0° (measured)

$Q_{ELECTRICAL}$ = 0.9W

Q_{ARRAY} = 0.9W + (0.41 × 31W) = 13.61W

T_{ARRAY} = 55.0°C + (13.61W × 0.90°C/W) = 67.2°C

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000mW/W \div A_{ILL}$ (mW/cm^2)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm^2)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm^2)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm ^{2}) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410nm to the total optical power in the illumination spectrum (spectral measurement)

- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths >800nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤475nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths ≥410nm and ≤440nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 31W (measured)

A_{ARRAY} = (10.3680mm × 5.8320mm) ÷ 100mm^2/cm^2 = 0.6047cm^2 (data sheet)

OV_{ILL} = 16.3% (optical model)

$OP_{UV-RATIO}$ = 0.00017 (spectral measurement)

$OP_{VIS-RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR-RATIO}$ = 0.00006 (spectral measurement)

$OP_{BLU-RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1-RATIO}$ = 0.03200 (spectral measurement)

A_{ILL} = 0.6047cm^2 ÷ (1 - 0.163) = 0.7224cm^2

ILL_{UV} = [0.00017 × 31W] × 1000mW/W ÷ 0.7224cm^2 = 7.295mW/cm^2

ILL_{VIS} = [0.99977 × 31W] ÷ 0.7224cm^2 = 42.90W/cm^2

ILL_{IR} = [0.00006 × 31W] × 1000mW/W ÷ 0.7224cm^2 = 2.575mW/cm^2

ILL_{BLU} = [0.28100 × 31W] ÷ 0.7224cm^2 = 12.06W/cm^2

ILL_{BLU1} = [0.03200 × 31W] ÷ 0.7224cm^2 = 1.37W/cm^2

6.8 Micromirror Landed-On/Landed-Off Duty Cycle

6.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the Off state 0% of the time); whereas, 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD usable life. This is quantified in the derating curve shown in 図 5-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD Temperature at a given long-term average Landed Duty Cycle.

6.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 6-1.

表 6-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use this equation to calculate the landed duty cycle of a given pixel during a given time period:

Landed Duty Cycle =

(Red_Cycle_% × Red_Scale_Value) +

(Green_Cycle_% × Green_Scale_Value) +

(Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities are as shown in 表 6-2 and 表 6-3.

表 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

CYCLE PERCENTAGE		
RED	GREEN	BLUE
50%	20%	30%

表 6-3. Example Landed Duty Cycle for Full-Color

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source in one of two directions, towards the projection optics or collection optics. Typical applications using the DLP470NE include home theater, digital signage, interactive displays, low-latency gaming displays, and portable smart displays.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology, called TRP. With a smaller pixel pitch of 5.4 µm and an increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP chipsets are a great fit for any system that requires high-resolution and high-brightness displays.

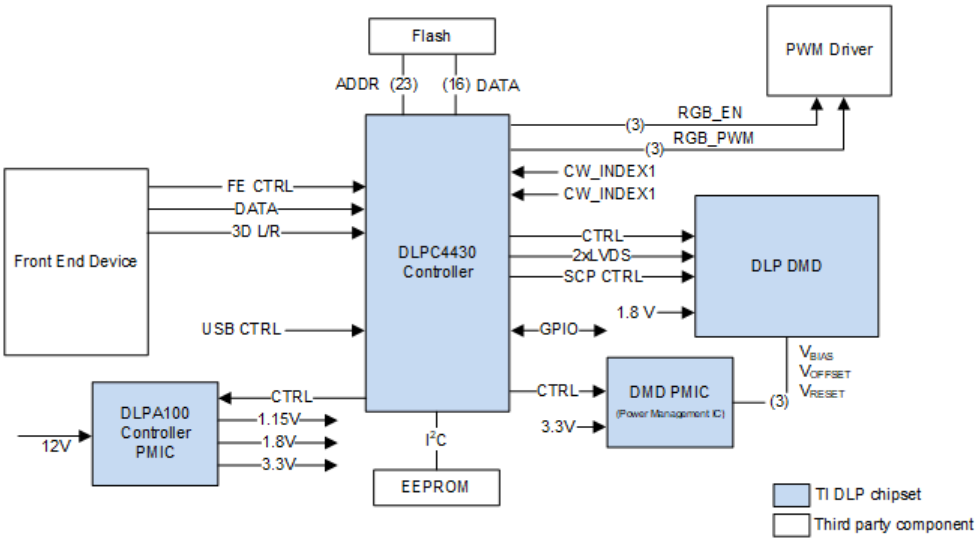
The following orderables were replaced by the DLP470NE.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	Mechanical ICD
DLP470NETA	FXH (257)	33.2mm × 22.3mm	2516206
1910-5432B	FXH (257)	33.2mm × 22.3mm	2516206
1910-5437B	FXH (257)	33.2mm × 22.3mm	2516206
1910-543AB	FXH (257)	33.2mm × 22.3mm	2516206

7.2 Typical Application

The DLP470NE digital micromirror device (DMD), combined with a DLPC4420 (or DLPC4430) digital controller and DLPA100 power management device, provides full HD resolution for bright, colorful display applications. 図 7-1 shows a typical display system using the DLP470NE and additional system components.



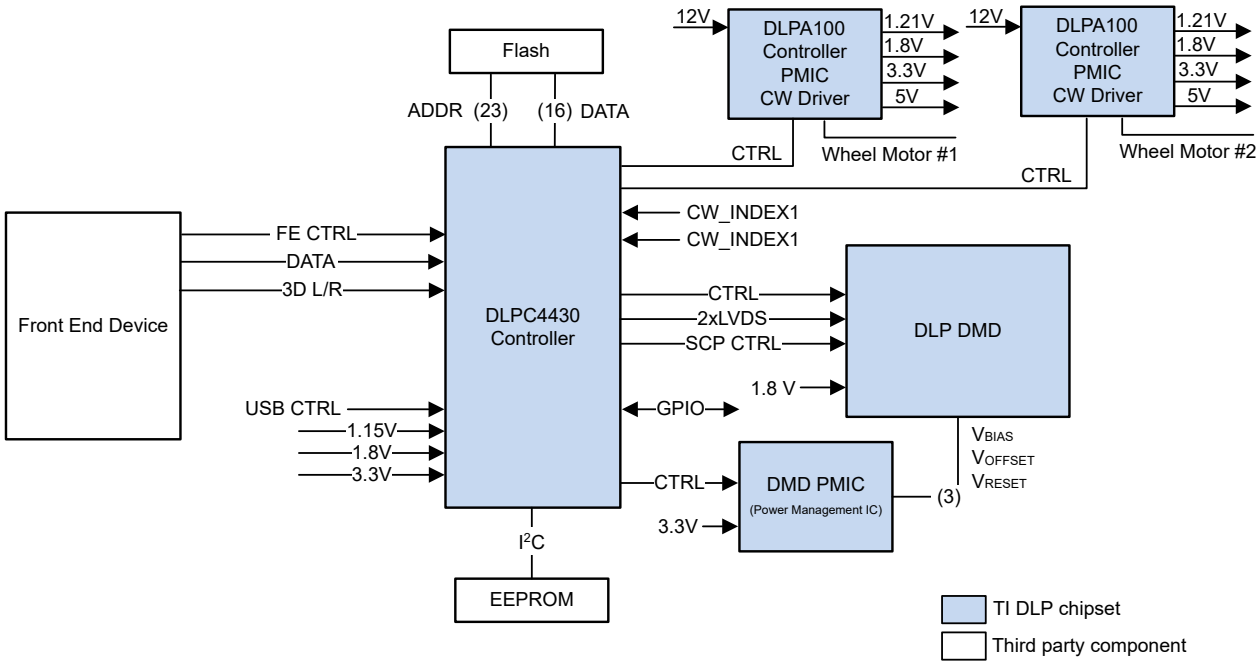


図 7-1. Typical DLPC4430 Application (LED, Top; LPCW, Bottom)

7.2.1 Design Requirements

A DLP470NE projection system is created by using the DMD chipset, including the DLP470NE, DLPC4420, and DLPA100. The DLP470NE is used as the core imaging device in the display system and contains a 0.47-inch array of micromirrors. The DLPC4420 controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The DLPA100 power management device provides voltage regulators for the DMD, controller, and illumination functionality.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness have a major effect on the overall system design and size.

7.2.2 Detailed Design Procedure

For connecting the DLPC4420 display controller and the DLP470NE DMD, see the reference design schematic. For a complete DLP system, an optical module or light engine is required that contains the DLP470NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DLP470NE DMD must always be used with the DLPC4420 display controller and a DLPA100 PMIC driver. Refer to PCB Design Requirements for DLP Standard TRP Digital Micromirror Devices for the DMD board design and manufacturing handling of the DMD subassemblies.

7.2.3 Application Curves

When LED illumination is used, a typical LED-current-to-Luminance relationship is shown in 図 7-2.

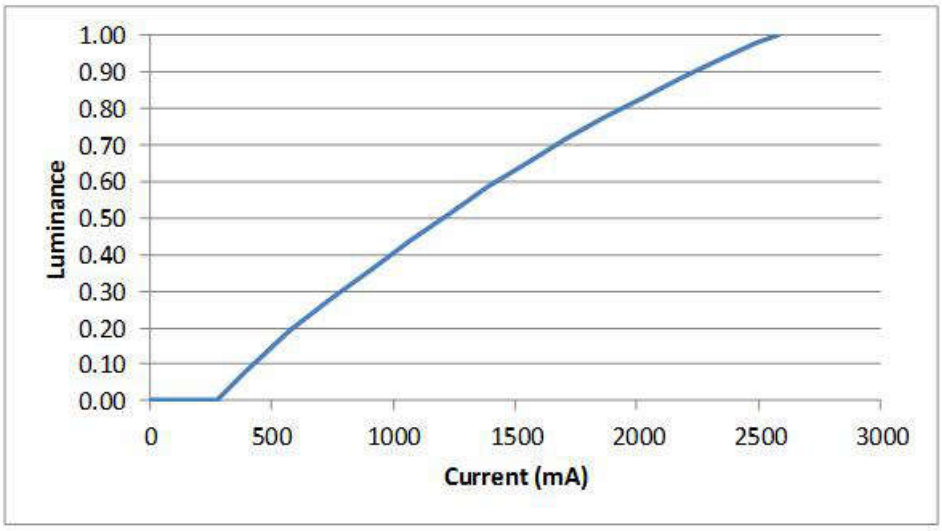
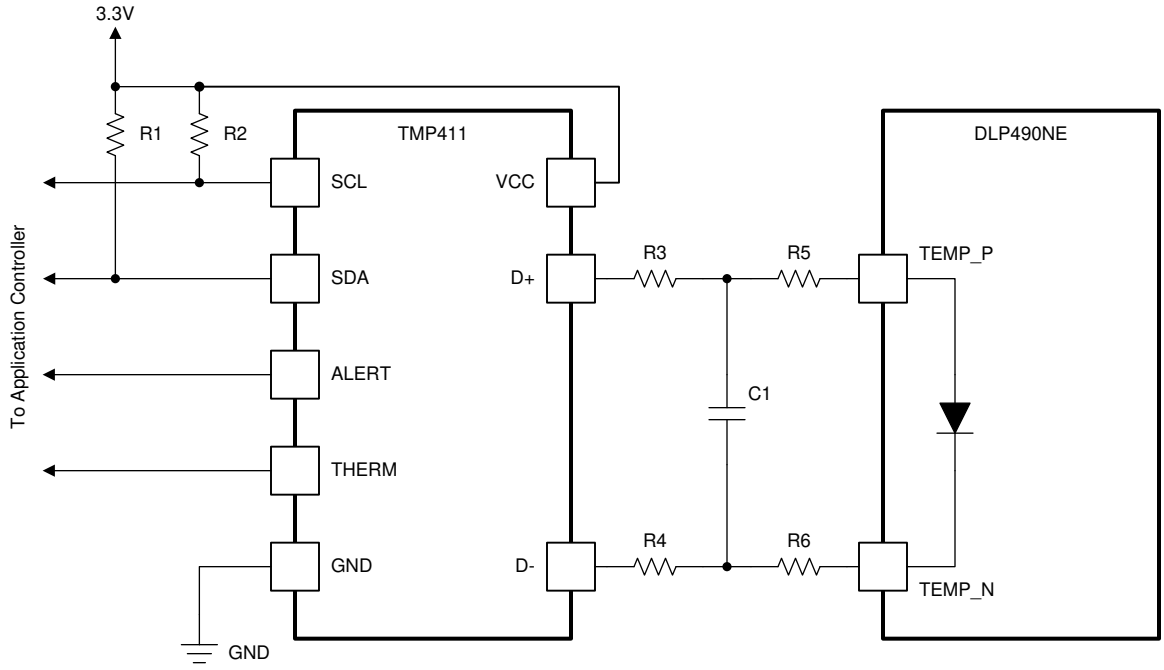


図 7-2. Luminance vs. Current

7.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor, as shown in 図 7-3. The serial bus from the TMP411 can be connected to the DLPC4420 display controller to enable its temperature-sensing features. See the *DLPC4420 Programmers' Guide* for instructions on installing the DLPC4420 controller support firmware bundle and obtaining the temperature readings.

The software application contains functions to configure the TMP411 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth. All communication between the TMP411 and the DLPC4420 controller is completed using the I^2C interface. The TMP411 connects to the DMD via pins B17 and B18, as outlined in セクション 4.



A. Details omitted for clarity, see the TI Reference Design for connections to the DLPC4420 controller.
B. See the TMP411 data sheet for system board layout recommendation.
C. See the TMP411 data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0Ω. R6 = 0Ω. Zero-ohm resistors need to be located close to the DMD package pins.

図 7-3. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- VSS
- VBIAS
- VCC
- VOFFSET
- VRESET

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

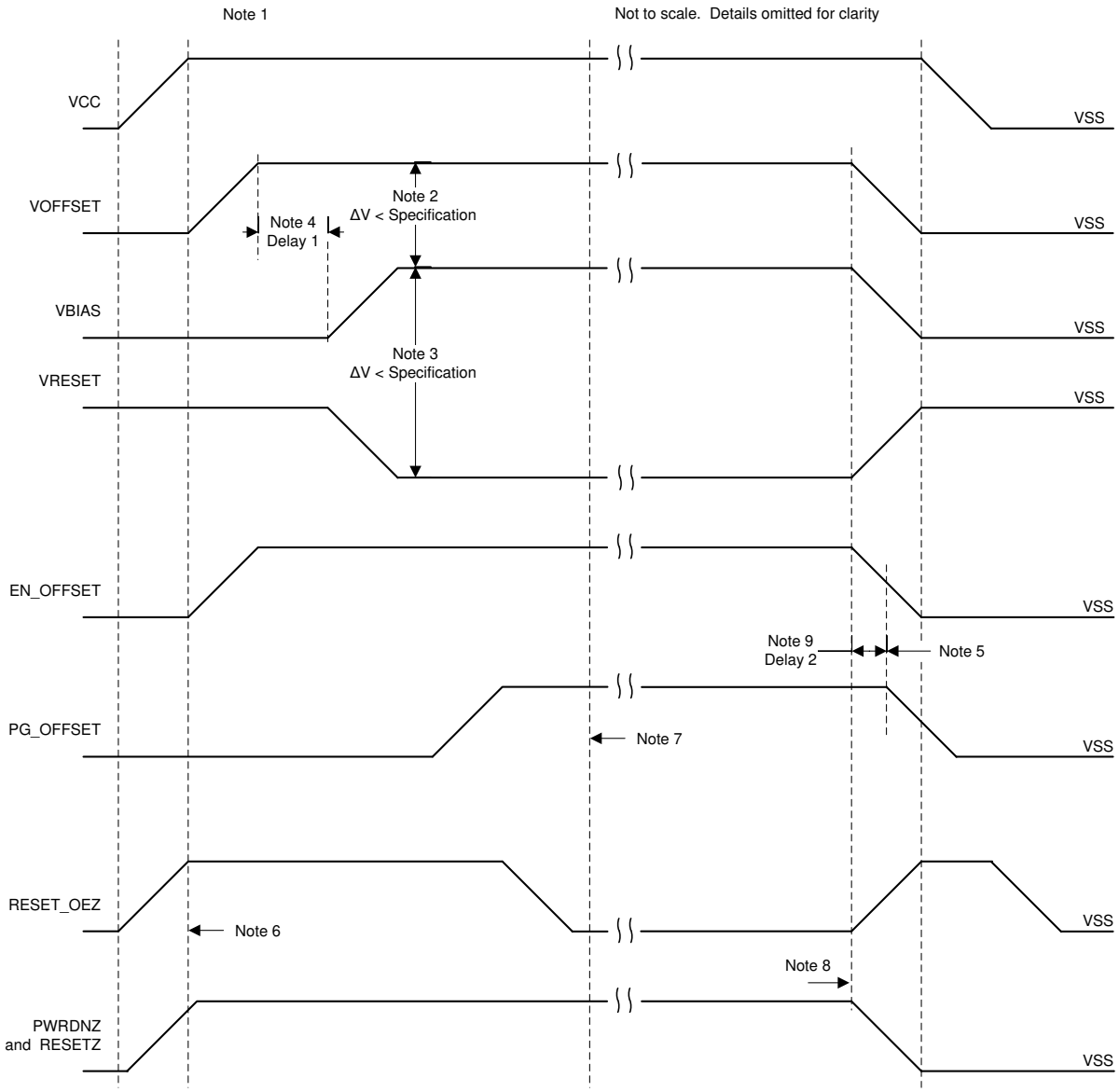
> **注意**
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 図 8-1 DMD Power Supply Sequencing Requirements.
>
> VBIAS, VCC, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground VSS must also be connected.

8.1 DMD Power Supply Power-Up Procedure

- During power-up, VCC must always start and settle before VOFFSET plus Delay1 specified in 表 8-1, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in セクション 5.4.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in セクション 5.1, in セクション 5.4, and in 図 8-1.
- During power-up, LVCMOS input pins must not be driven high until after VCC have settled at operating voltages listed in セクション 5.4.

8.2 DMD Power Supply Power-Down Procedure

- During power-down, VCC must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. See 表 8-1.
- During power-down, it is a strict requirement that the voltage difference between VBIAS and VOFFSET must be within the specified limit shown in セクション 5.4.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in セクション 5.1, in セクション 5.4, and in 図 8-1.
- During power-down, LVCMOS input pins must be less than specified in セクション 5.4.



A. See セクション 5.4 and Pin Configuration and Functions.
B. To prevent excess current, the supply voltage difference |VOFFSET – VBIAS| must be less than specified limit in セクション 5.4.
C. To prevent excess current, the supply difference |VBIAS – VRESET| must be less than specified limit in セクション 5.4.
D. VBIAS must power up after VOFFSET has powered up, per the Delay1 specification in 表 8-1.
E. PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in 表 8-1.
F. DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
G. DLP controller software initiates the global VBIAS command.
H. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET.
I. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal goes high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

図 8-1. DMD Power Supply Requirements

表 8-1. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from VOFFSET settled at recommended operating voltage to VBIAS and VRESET power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

9 Layout

9.1 Layout Guidelines

The DLP470NE DMD is part of a chipset controlled by the DLPC4420 display controller in conjunction with the DLPA100 power and motor driver. These guidelines help to design a PCB board with the DLP470NE DMD. The DLP470NE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic using dual-edge clock rates up to 400MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTL signals. TI recommends that mini power planes are used for VOFFSET, VRESET, and VBIAS. Solid planes are required for DMD_P3P3V(3.3V), DMD_P1P8V and Ground. The target impedance for the PCB is 50Ω ±10% with the LVDS traces being 100Ω ±10% differential. Use an 8-layer stack-up, as described in 表 9-1.

9.2 Layout Example

9.2.1 Layers

The layer stack-up and copper weight for each layer are shown in 表 9-1 . Small subplanes are allowed on signal routing layers to connect components to major subplanes on top or bottom layers if necessary.

表 9-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low-frequency signals, power subplanes
2	Ground	1	Solid ground plane (net GND)
3	Signal	0.5	50Ω and 100Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3V power plane (net DMD_P3P3V)
6	Signal	0.5	50Ω and 100Ω differential signals
7	Ground	1	Solid ground plane (net GND)
8	Side B - All other Components	1.5	Discrete components, low-frequency signals, power subplanes

9.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50Ω ±10% for all signals. The exceptions are listed in 表 9-2.

表 9-2. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
C channel LVDS differential pairs	DDCP(0:15), DDCN(0:15)	100 ±10% differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	DDDP(0:15), DDDN(0:15)	100 ±10% differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

9.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005-inch / 0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

9.2.3.1 Voltage Signals

表 9-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin

表 9-3. Special Trace Widths, Spacing Requirements (続き)

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from U2 to U3
VRESET	15	Create mini plane from U2 to U3
VBIAS	15	Create mini plane from U2 to U3
All U3 control connections	10	Use 10mil etch to connect all signals/voltages to DMD pads

10 Device and Documentation Support

10.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.2 Device Support

10.2.1 Device Nomenclature

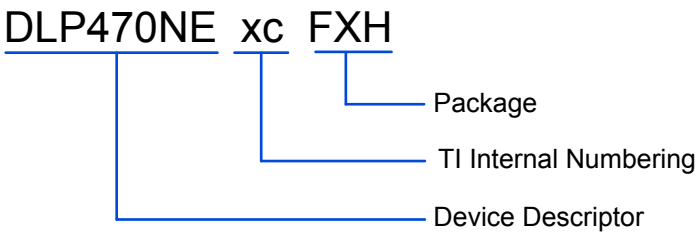


図 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 図 10-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of serial number, and part 2 of serial number.

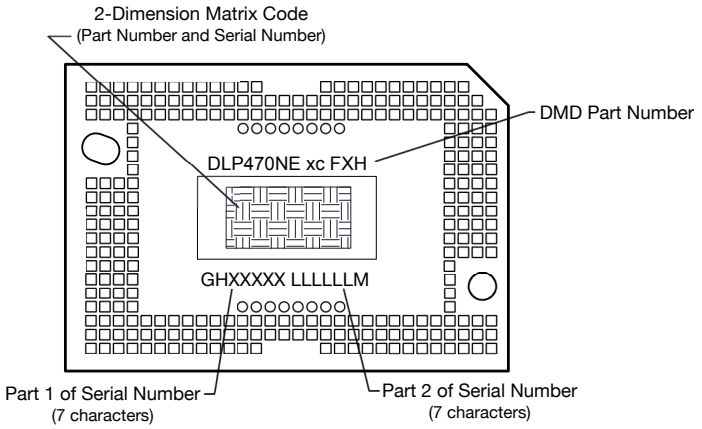


図 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP470NE.

- *DLPC4430 Display Controller Data Sheet*
- *DLPC4420 Display Controller Data Sheet*
- *DLPA100 Power and Motor Driver Data Sheet*

10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.5 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

10.6 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

10.7 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.8 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (February 2023) to Revision D (December 2024)	Page
• ドキュメント全体を通してメイン コントローラを DLPC4420 に更新	1
• サポートされるディスプレイ コントローラとして DLPC4420 を追加。	1
• DLP 製品のサード パーティ検索ツールおよび『テキサス・インスツルメンツの DLP ディスプレイ テクノロジーを使用した設計の開始』へのリンクを追加。	1
• Updated section Recommended Operating Conditions	11
• Updated Micromirror Array Optical Characteristics Table	21
• Updated controller name to DLPC4420 and added link to DLPC4420 data sheet	25
• Updated Micromirror Array Temperature Calculation	26
• Added section Micromirror Power Density Calculation	27
• Changed controller name to DLPC4420	34

Changes from Revision B (June 2022) to Revision C (February 2023)	Page
• コントローラを DLPC4430 に更新し、チップセット コンポーネントを製品ページにリンク。	1
• コントローラ名を DLPC4430 に変更。	1
• Added the lamp illumination section to the table	11
• Changed controller name to DLPC4430	23
• Changed controller name to DLPC4430	25

- Added a table with legacy device information, added the mechanical ICD....32
- Changed controller name to DLPC4430....32
- Changed controller name to DLPC4430....33
- Changed controller name to DLPC4430....33
- Changed controller name to DLPC4430....34
- Changed controller name to DLPC4430....39
- Changed controller name to DLPC4430, updated the links....41

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP470NEAAFXH	Active	Production	CLGA (FXH) | 257	33 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	0 to 70	
DLP470NEAAFXH.B	Active	Production	CLGA (FXH) | 257	33 | JEDEC TRAY (5+1)	-	Call TI	N/A for Pkg Type	0 to 70	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

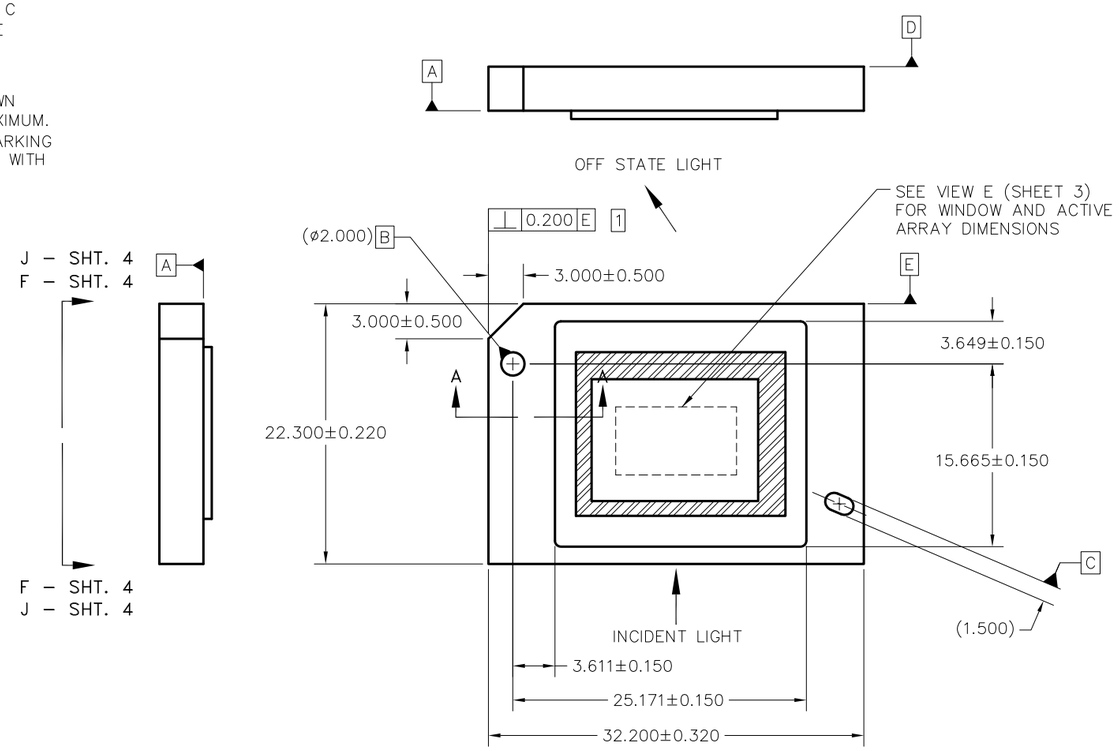
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

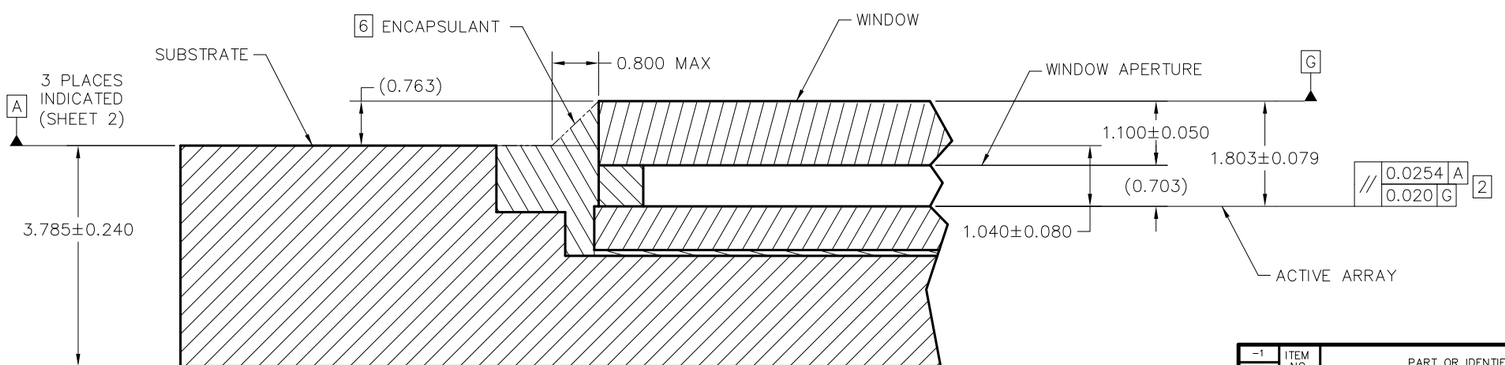
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2174191, INITIAL RELEASE	05/11/2018	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA TO THE LEFT OF THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA TO THE RIGHT OF THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

PARTS LIST

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
-1				

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG	05/11/2018
ENGR	F. ARMSTRONG	05/11/2018
QA	F. KONRAD	05/11/2018
CQE	M. DORAK	05/11/2018

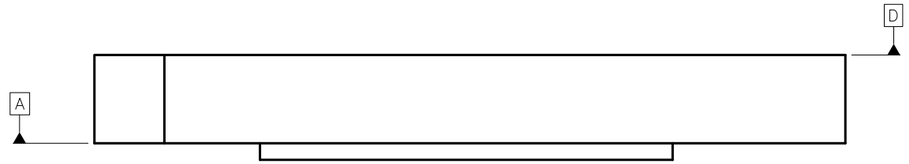
TEXAS INSTRUMENTS
Dallas, Texas

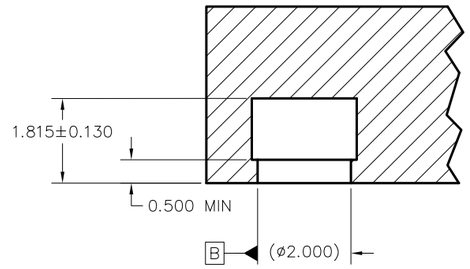
ICD, MECHANICAL, DMD
.47" 1080p MTRP 2xLVDS HB C
SERIES 410 (FXH PACKAGE)

THIRD ANGLE PROJECTION		
NEXT ASSY	NONE	0314DA
APPLICATION	USED ON	

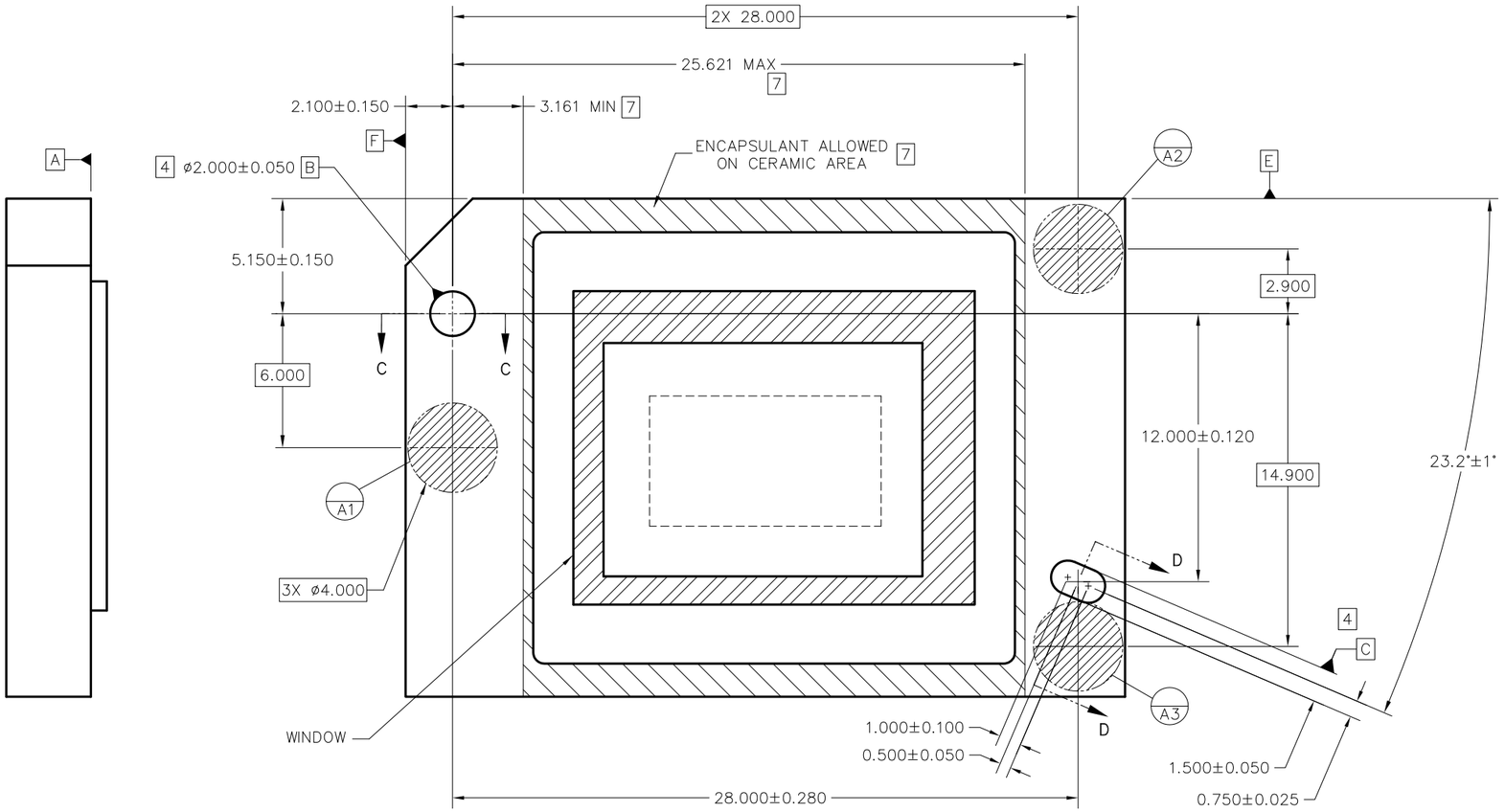
SIZE B | DRAWING NO 2516206 | REV A
SCALE 4/1 | SHEET 1 OF 4

ACED1g

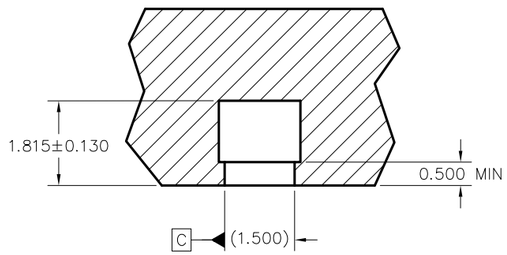




SECTION C–C
DATUM B
SCALE 16/1



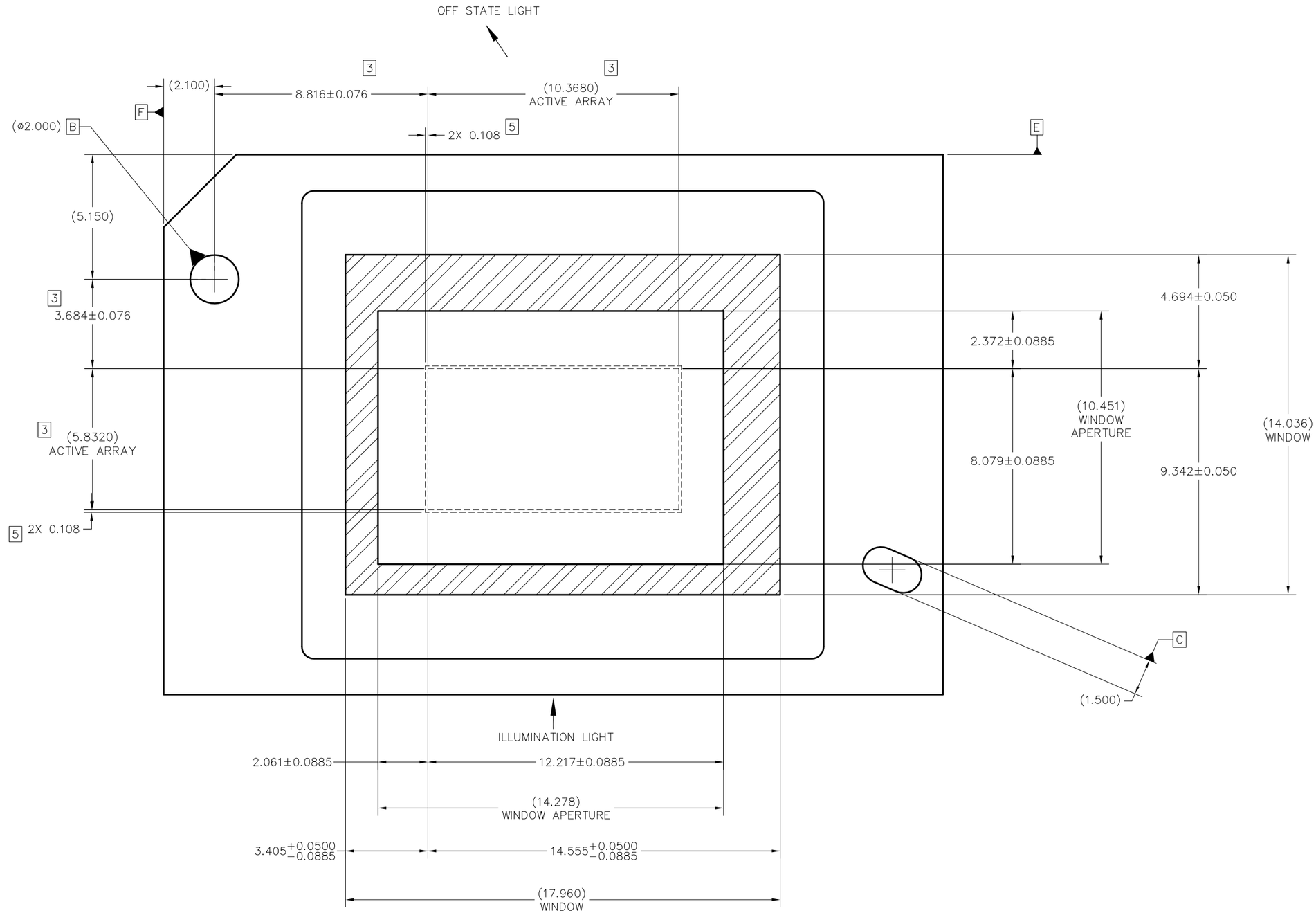
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

Texas Instruments, Dallas, Texas	DWN DATE / ISSUE DATE	SIZE B	DRAWING NO 2516206	REV A
		SCALE 4/1	SHEET 2	

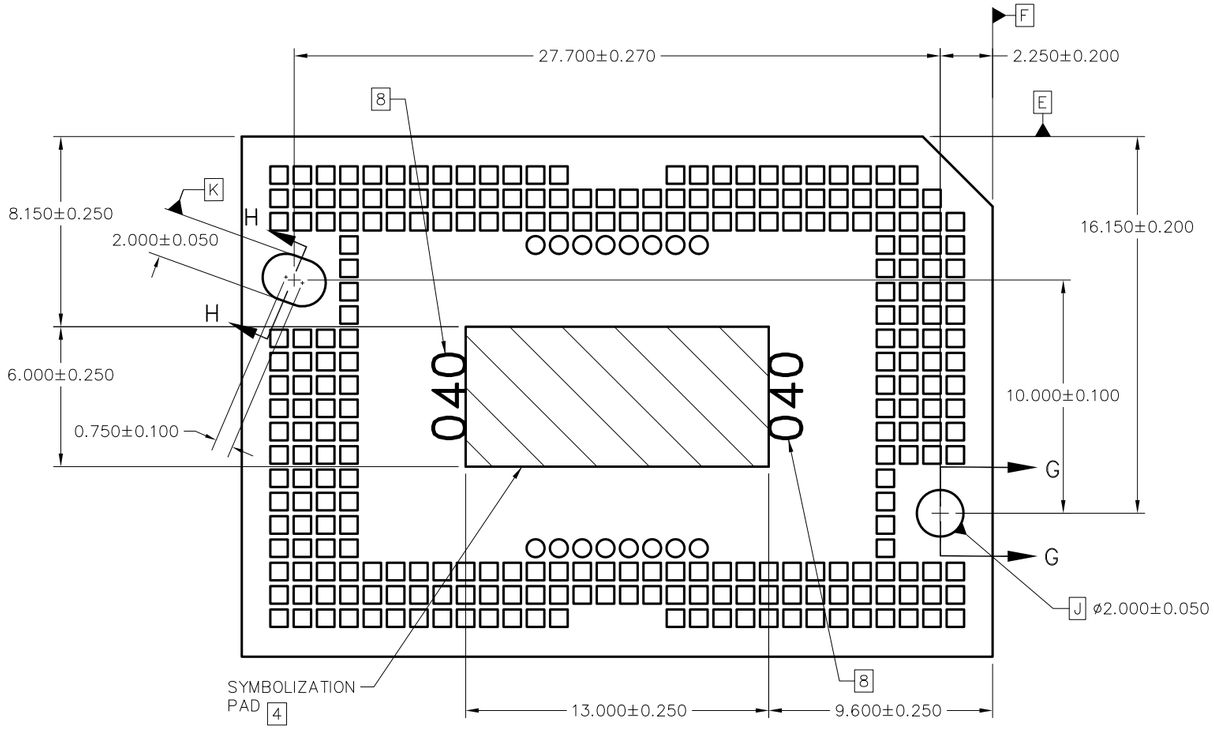
ACED2c



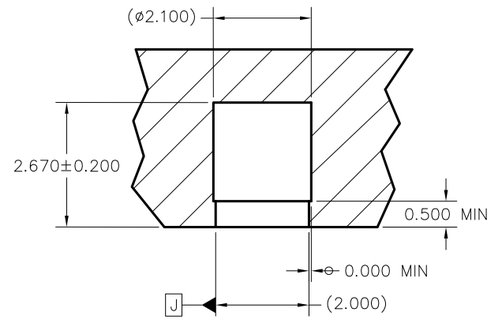
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

Texas Instruments, Dallas, Texas	DWN / DATE	SIZE B	DRAWING NO 2516206	REV A
	ISSUE DATE	SCALE 4/1	SHEET 3	

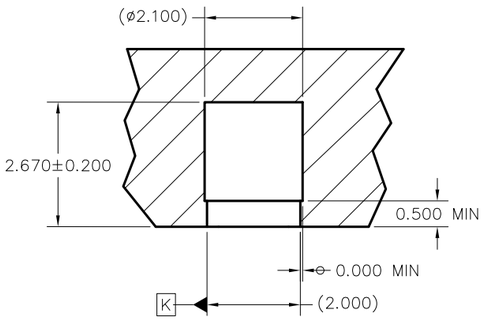
ACED2c



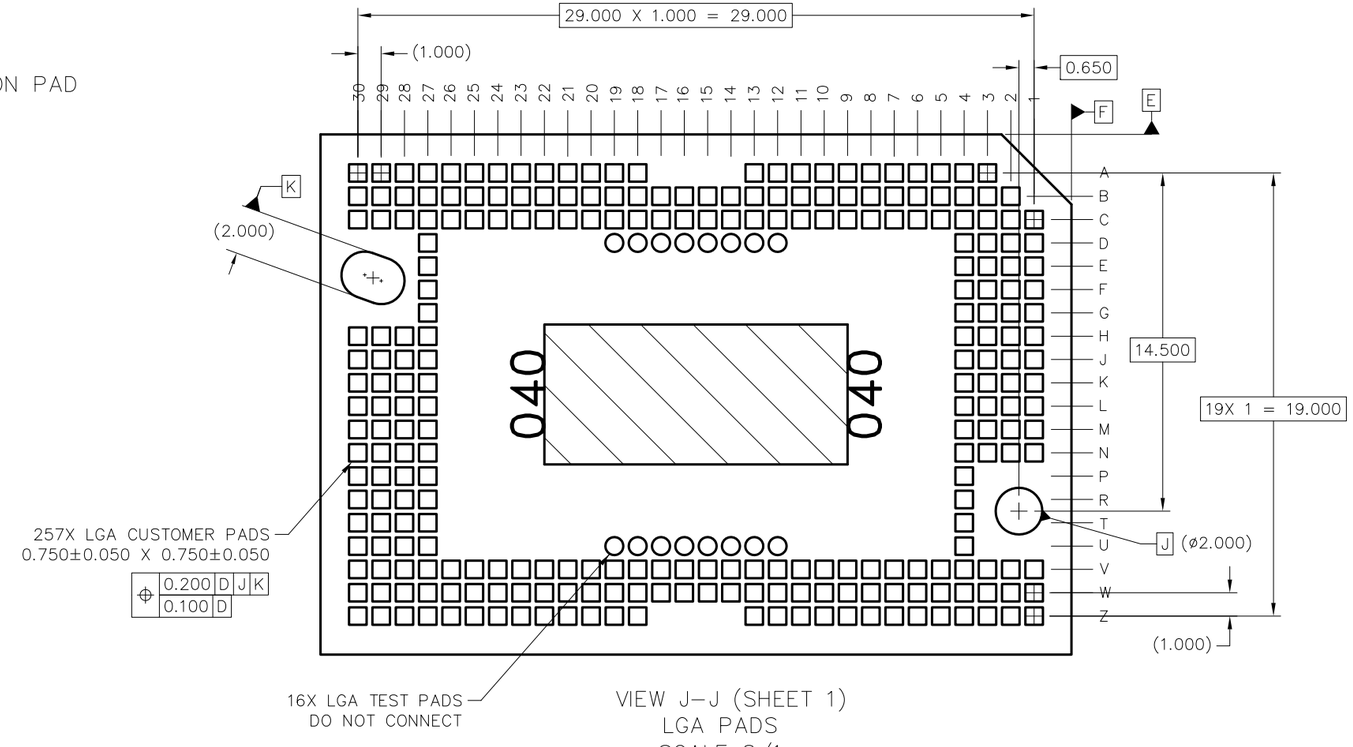
VIEW F–F (SHEET 1)
DATUMS J AND K, SYMBOLIZATION PAD
SCALE 8/1



SECTION G–G
DATUM J
SCALE 16/1



SECTION H–H
DATUM K
SCALE 16/1



VIEW J–J (SHEET 1)
LGA PADS
SCALE 8/1

TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE B	DRAWING NO 2516206	REV A
	ISSUE DATE		SCALE 4/1	SHEET 4	

ACED2c

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、 テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス・インスツルメンツがこれらのリソースを提供することは、適用される テキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265