DLP5534-Q1 車載ディスプレイ用の 0.55 インチ、1.3 メガピクセル 405nm DMD

1 特長

- 車載アプリケーションに対応
  - DMD アレイの動作温度範囲:–40℃～105℃
- 405nm の照明光源をサポート
- 以下の製品で構成される DLP5534-Q1 車載用チップセット
  - DLP5534-Q1 DMD
  - DLPC230-Q1 DMD コントローラ
  - TPS99000-Q1 システム管理および照明コントローラ
- 対角 0.55 インチのマイクロミラー・アレイ
  - 7.6µm のマイクロミラー・ピッチ
  - マイクロミラー傾斜角:±12° (フラット状態に対して)
  - 底面照明による最良の効率と光学エンジン・サイズ
  - 1152 × 576 の入力解像度をサポート
  - LED またはレーザー照明と互換
- 600MHz の Sub-LVDS DMD インターフェイスによる低い消費電力と放射妨害波
- 上限や下限の温度でも 10kHz の DMD リフレッシュ・レートを維持
- DMD メモリ・セルの内蔵セルフ・テスト

2 アプリケーション

- 車のフロント、サイド、およびリア・ウィンドウ用透明ウィンドウ・ディスプレイ

3 概要

DLP5534-Q1 車載用 DMD を DLPC230-Q1 DMD コントローラ、TPS99000-Q1 システム管理および照明コントローラと組み合わせることで、高性能の透明ウィンドウ・ディスプレイ・プロジェクタを実現できます。このチップセットを 405nm の照明光源 (例:LED、レーザー) と組み合わせて光学投影システムとすることで、発光性蛍光体薄膜を埋め込んだウィンドウに投影できます。これらの透明な発光性薄膜を DLP5534-Q1 プロジェクタの 405nm 光で励起すると、そのウィンドウは可視スペクトルで発光するディスプレイになります。DLP5534-Q1 の光学スループットは前世代の DLP3034-Q1 車載用 DMD の 3 倍を超えるため、より明るくて大きなディスプレイが可能になります。また、このチップセットを使用すると、ダイナミック・レンジが広く、温度にかかわらずスイッチング速度が速い大出力光学システムを実現できます。

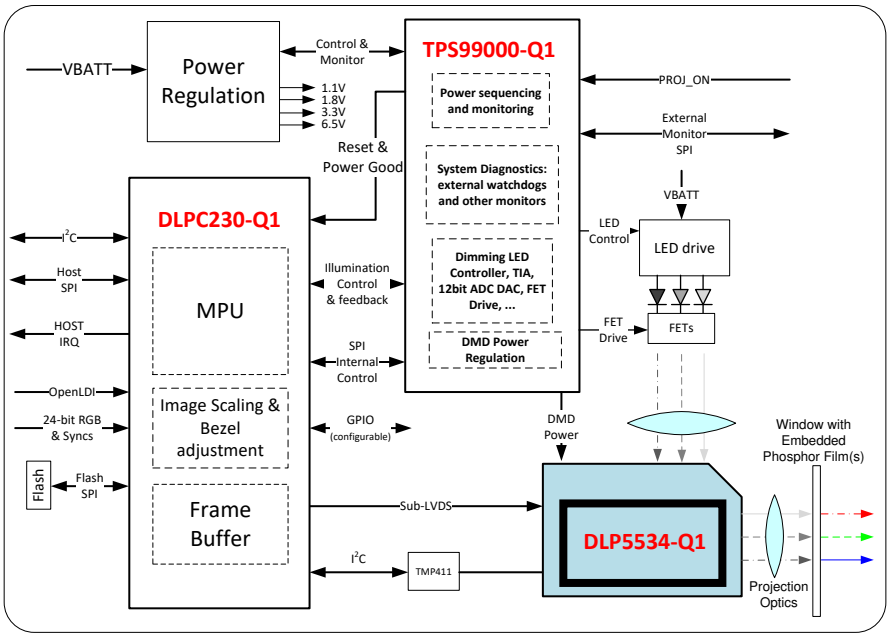
製品情報(1)(2)

型番	パッケージ	本体サイズ(公称)
DLP5534-Q1	FYK (149)	22.30mm×32.20mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) このデータシートは、405nm 光を使用する透明ウィンドウ・ディスプレイ・アプリケーションでの本 DMD の仕様とアプリケーションに準じています。別の最終機器の仕様と関連アプリケーション情報については、他の DLP553X-Q1 データシートを参照してください。

DLP5534-Q1 DLP®チップセットのシステム・ブロック図



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4 改訂履歴

日付	リビジョン	注
2019 年 9 月	*	初版

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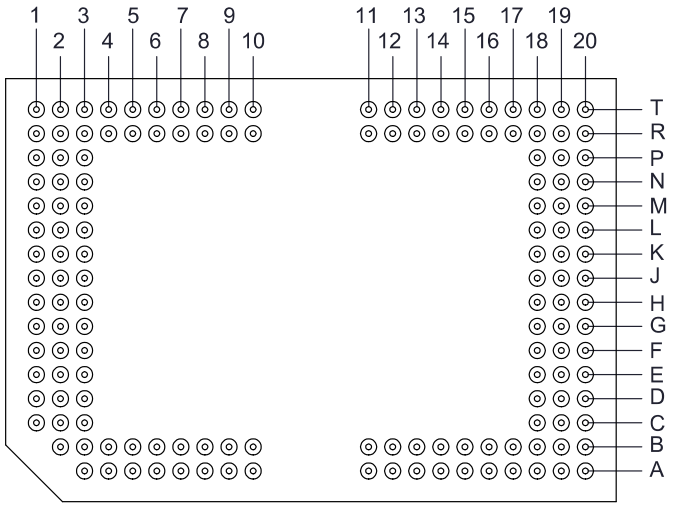
5 Pin Configuration and Functions

FYK Package
149-Pin CPGA
Bottom View



Pin Functions – Connector Pins

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	L2	I	SubLVDS	Double	Data, Negative
D_AN(1)	K2	I	SubLVDS	Double	Data, Negative
D_AN(2)	J2	I	SubLVDS	Double	Data, Negative
D_AN(3)	H2	I	SubLVDS	Double	Data, Negative
D_AN(4)	F2	I	SubLVDS	Double	Data, Negative
D_AN(5)	E2	I	SubLVDS	Double	Data, Negative
D_AN(6)	D2	I	SubLVDS	Double	Data, Negative
D_AN(7)	C2	I	SubLVDS	Double	Data, Negative
D_AP(0)	L1	I	SubLVDS	Double	Data, Positive
D_AP(1)	K1	I	SubLVDS	Double	Data, Positive
D_AP(2)	J1	I	SubLVDS	Double	Data, Positive
D_AP(3)	H1	I	SubLVDS	Double	Data, Positive
D_AP(4)	F1	I	SubLVDS	Double	Data, Positive
D_AP(5)	E1	I	SubLVDS	Double	Data, Positive
D_AP(6)	D1	I	SubLVDS	Double	Data, Positive
D_AP(7)	C1	I	SubLVDS	Double	Data, Positive
D_BN(0)	K19	I	SubLVDS	Double	Data, Negative
D_BN(1)	J19	I	SubLVDS	Double	Data, Negative
D_BN(2)	H19	I	SubLVDS	Double	Data, Negative
D_BN(3)	G19	I	SubLVDS	Double	Data, Negative
D_BN(4)	E19	I	SubLVDS	Double	Data, Negative
D_BN(5)	D19	I	SubLVDS	Double	Data, Negative
D_BN(6)	C19	I	SubLVDS	Double	Data, Negative
D_BN(7)	B19	I	SubLVDS	Double	Data, Negative
D_BP(0)	K20	I	SubLVDS	Double	Data, Positive
D_BP(1)	J20	I	SubLVDS	Double	Data, Positive

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Pin Functions – Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BP(2)	H20	I	SubLVDS	Double	Data, Positive
D_BP(3)	G20	I	SubLVDS	Double	Data, Positive
D_BP(4)	E20	I	SubLVDS	Double	Data, Positive
D_BP(5)	D20	I	SubLVDS	Double	Data, Positive
D_BP(6)	C20	I	SubLVDS	Double	Data, Positive
D_BP(7)	B20	I	SubLVDS	Double	Data, Positive
DCLK_AN	G2	I	SubLVDS	Double	Clock, Negative
DCLK_AP	G1	I	SubLVDS	Double	Clock, Positive
DCLK_BN	F19	I	SubLVDS	Double	Clock, Negative
DCLK_BP	F20	I	SubLVDS	Double	Clock, Positive
LS_CLKN	R3	I	SubLVDS	Single	Clock for Low Speed Interface, Negative
LS_CLKP	T3	I	SubLVDS	Single	Clock for Low Speed Interface, Positive
LS_WDATAN	R2	I	SubLVDS	Single	Write Data for Low Speed Interface, Negative
LS_WDATAP	T2	I	SubLVDS	Single	Write Data for Low Speed Interface, Positive
CONTROL INPUTS					
DMD_DEN_ARSTZ	T10	I	LPSDR		Asynchronous Reset Active Low. Logic High Enables DMD.
LS_RDATA_A	T5	O	LPSDR	Single	Read Data for Low Speed Interface
LS_RDATA_B	T6	O	LPSDR	Single	Read Data for Low Speed Interface
TEMPERATURE SENSE DIODE					
TEMP_N	P1	O			Calibrated temperature diode used to assist accurate temperature measurements of DMD die.
TEMP_P	N1	I			
RESERVED PINS					
VCCH	A8	Ground			Reserved Pin. Connect to Ground.
VCCH	A9	Ground			
VCCH	A10	Ground			
VCCH	B8	Ground			
VCCH	B9	Ground			
VCCH	B10	Ground			
VSSH	A11	Ground			Reserved Pin. Connect to Ground.
VSSH	A12	Ground			
VSSH	A13	Ground			
VSSH	B11	Ground			
VSSH	B12	Ground			
VSSH	B13	Ground			

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Pin Functions – Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
POWER					
VBIAS	T7	Power			Supply voltage for positive bias level at micromirrors.
VBIAS	T15	Power			
VOFFSET	T9	Power			Supply voltage for High Voltage CMOS core logic. Supply voltage for offset level at micromirrors.
VOFFSET	T13	Power			
VOFFSET	A5	Power			
VOFFSET	B5	Power			
VOFFSET	A16	Power			
VOFFSET	B16	Power			
VRESET	T8	Power			Supply voltage for negative reset level at micromirrors.
VRESET	T14	Power			
VDD	R4	Power			Supply voltage for Low Voltage CMOS core logic; for LPSDR inputs; for normal high level at micromirror address electrodes.
VDD	R10	Power			
VDD	R11	Power			
VDD	R20	Power			
VDD	N2	Power			
VDD	M20	Power			
VDD	L3	Power			
VDD	K18	Power			
VDD	H3	Power			
VDD	G18	Power			
VDD	E3	Power			
VDD	D18	Power			
VDD	C3	Power			
VDD	A6	Power			
VDD	A18	Power			
VDDI	T4	Power			Supply voltage for SubLVDS receivers.
VDDI	R1	Power			
VDDI	M3	Power			
VDDI	L18	Power			
VDDI	J3	Power			
VDDI	H18	Power			
VDDI	F3	Power			
VDDI	E18	Power			
VDDI	B3	Power			
VDDI	B18	Power			

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Pin Functions – Connector Pins (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
VSS	T1	Ground			Common return. Ground for all power.
VSS	T16	Ground			
VSS	T19	Ground			
VSS	T20	Ground			
VSS	R5	Ground			
VSS	R6	Ground			
VSS	R7	Ground			
VSS	R8	Ground			
VSS	R9	Ground			
VSS	R13	Ground			
VSS	R14	Ground			
VSS	R15	Ground			
VSS	P2	Ground			
VSS	P3	Ground			
VSS	P20	Ground			
VSS	N19	Ground			
VSS	N20	Ground			
VSS	M1	Ground			
VSS	M2	Ground			
VSS	L19	Ground			
VSS	L20	Ground			
VSS	K3	Ground			
VSS	J18	Ground			
VSS	G3	Ground			
VSS	F18	Ground			
VSS	D3	Ground			
VSS	C18	Ground			
VSS	B2	Ground			
VSS	B4	Ground			
VSS	B15	Ground			
VSS	B17	Ground			
VSS	A3	Ground			
VSS	A4	Ground			
VSS	A7	Ground			
VSS	A15	Ground			
VSS	A17	Ground			
VSS	A19	Ground			
VSS	A20	Ground			

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Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
T11	Do not connect
T12	Do not connect
T17	Do not connect
T18	Do not connect
R12	Do not connect
R16	Do not connect
R17	Do not connect
R18	Do not connect
R19	Do not connect
P18	Do not connect
P19	Do not connect
N3	Do not connect
N18	Do not connect
M18	Do not connect
M19	Do not connect
B6	Do not connect
B7	Do not connect
B14	Do not connect
A14	Do not connect

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
VDD	Supply voltage for LVCMOS core logic (2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
VDDI	Supply voltage for SubLVDS receivers (2)	–0.5	2.3	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2)(3)	–0.5	8.75	V
VBIAS	Supply voltage for micromirror electrode (2)	–0.5	17	V
VRESET	Supply voltage for micromirror electrode (2)	–11	0.5	V
| VDDI–VDD |	Supply voltage delta (absolute value) (4)		0.3	V
| VBIAS–VOFFSET |	Supply voltage delta (absolute value) (5)		8.75	V
| VBIAS–VRESET |	Supply voltage delta (absolute value) (6)		28	V
INPUT VOLTAGE				
Input voltage for other inputs LPSDR (2)		–0.5	VDD + 0.5	V
Input voltage for other inputs SubLVDS (2)(7)		–0.5	VDDI + 0.5	V
INPUT PINS				
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value) (7)		810	mV
I_{ID}	SubLVDS input differential current		10	mA
CLOCK FREQUENCY				
f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
ENVIRONMENTAL				
T_{ARRAY}	Operating DMD array temperature (8)	–40	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(3) VOFFSET supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage to the internal termination resistors may result.
(8) See *Micromirror Array Temperature Calculation* section.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	125	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), Corner Pins, per JESD22-C101 (2)	±750	
		Charged-device model (CDM), All Other Pins, per JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(3)						
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface		1.7	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers		1.7	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode(4)		8.25	8.5	8.75	V
VBIAS	Supply voltage for mirror electrode		15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrode		–9.5	–10	–10.5	V
| VDDI–VDD |	Supply voltage delta (absolute value)(5)				0.3	V
| VBIAS–VOFFSET |	Supply voltage delta (absolute value)(6)				8.75	V
CLOCK FREQUENCY						
f_{clock}	Clock frequency for low speed interface LS_CLK				120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(7)				600	MHz
	Duty cycle distortion DCLK		44%		56%	
SUBLVDS INTERFACE(7)						
$\lvert V_{ID} \rvert$	SubLVDS input differential voltage (absolute value, see Figure 6, Figure 7)		150	250	350	mV
V_{CM}	Common mode voltage (see Figure 6, Figure 7)		700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage (see Figure 6, Figure 7)		575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)		90	100	110	Ω
Z_{IN}	Internal differential termination resistance (see Figure 8)		80	100	120	Ω
TEMPERATURE DIODE						
I_{TEMP_DIODE}	Max current source into Temperature Diode(8)				120	µA
ENVIRONMENTAL						
T_{ARRAY}	Operating DMD array temperature(9)		–40		105	°C
$ILL_{sub\text{-}385nm}$	Illumination, wavelength < 385 nm				2	mW/cm^2
$ILL_{385\text{-}to\text{-}395nm}$	Illumination, 385 nm < wavelength < 395 nm				250	mW/cm^2
$ILL_{395\text{-}to\text{-}400nm}$	Illumination, 395 nm < wavelength < 400 nm				800	mW/cm^2
$ILL_{400\text{-}to\text{-}420nm}$	Illumination, 400 nm < wavelength < 420 nm				8	W/cm^2
ILL_{VIS}	Illumination, 420 nm < wavelength < 800 nm				Thermally limited(10)	W/cm^2
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in areas shown in Figure 1(11)	$T_{ARRAY} \le 75°C$			40	mW/mm^2
	Illumination overfill maximum heat load in areas shown in Figure 1(11)	$T_{ARRAY} > 75°C$			29	

(1) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required.
(2) *Recommended Operating Conditions* are applicable after the DMD is installed in the final product.
(3) All voltage values are with respect to the ground pins (VSS).
(4) VOFFSET supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit.
(7) Refer to the SubLVDS timing requirements in *Timing Requirements*.
(8) Temperature Diode is to allow accurate measurement of the DMD array temperature during operation.
(9) DMD active array temperature can be calculated as shown in *Micromirror Array Temperature Calculation* section. Additionally, the DMD array temperature is monitored in the system using the TMP411-Q1 and DLPC230-Q1 as shown in the system block diagram.
(10) Limited by the resulting micromirror array temperature. Refer to the calculation example in *Micromirror Array Temperature Calculation* section.
(11) The active area of the DLP5534-Q1 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

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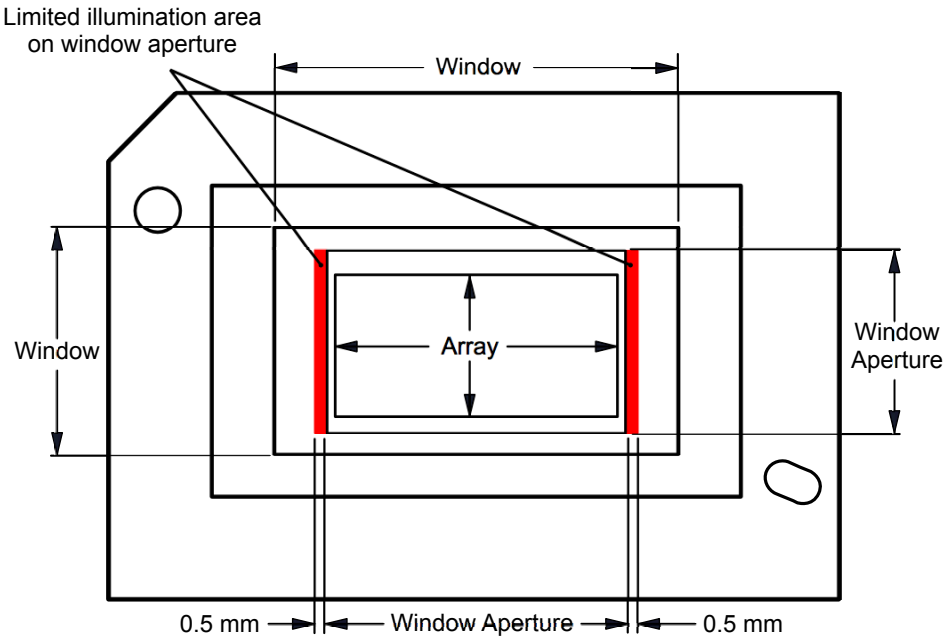

Figure 1. Illumination Overfill Diagram

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6.5 Thermal Information

THERMAL METRIC(1)		DLP5534-Q1 FYK (CPGA) 149 PINS	UNIT
Thermal resistance	Active area-to-test point 1 (TP1)(1)	1.1	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(3)	MAX	UNIT
CURRENT						
I_{DD}	Supply current: VDD(4)(5)	VDD = 1.95 V			369	mA
		VDD = 1.8 V				
I_{DDI}	Supply current: VDDI(4)(5)	VDDI = 1.95 V			62	mA
		VDD = 1.8 V				
I_{OFFSET}	Supply current: VOFFSET(6)	VOFFSET = 8.75 V			16.1	mA
		VOFFSET = 8.5 V				
I_{BIAS}	Supply current: VBIAS(6)	VBIAS = 16.5 V			1.3	mA
		VBIAS = 16 V				
I_{RESET}	Supply current: VRESET	VRESET = –10.5 V			–10.2	mA
		VRESET = –10 V				
POWER(7)						
P_{DD}	Supply power dissipation: VDD(4)(5)	VDD = 1.95 V			720	mW
		VDD = 1.8 V				
P_{DDI}	Supply power dissipation: VDDI(4)(5)	VDDI = 1.95 V			121	mW
		VDD = 1.8 V				
P_{OFFSET}	Supply power dissipation: VOFFSET(6)	VOFFSET = 8.75 V			141	mW
		VOFFSET = 8.5 V				
P_{BIAS}	Supply power dissipation: VBIAS(6)	VBIAS = 16.5 V			22	mW
		VBIAS = 16 V				
P_{RESET}	Supply power dissipation: VRESET	VRESET = –10.5 V			108	mW
		VRESET = –10 V				
P_{TOTAL}	Supply power dissipation: Total				1110	mW

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) Typical current consumption is application and video content dependent. Please see a TI applications engineer for additional information.
(4) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than the specified limit.
(5) Supply power dissipation based on non–compressed commands and data.
(6) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit.
(7) The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, VRESET. All VSS connections are also required.

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP(3)	MAX	UNIT
LPSDR INPUT(8)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × VDD		VDD + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × VDD	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × VDD		VDD + 0.3	V
$V_{IL(AC)}$	AC input low voltage		–0.3		0.2 × VDD	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	See Figure 9	0.1 × VDD		0.4 × VDD	V
I_{IL}	Low–level input current	VDD = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	VDD = 1.95 V; V_I = 1.95 V			300	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × VDD			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × VDD	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (1152 × 144) micromirrors	350	400	450	pF
C_{TEMP}	Temperature sense diode capacitance	f = 1 MHz			20	pF

(8) LPSDR input specifications are for pin DMD_DEN_ARSTZ.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) LPSDR output specification is for pins LS_RDATA_A and LS_RDATA_B.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(20% to 80%) × VDD, see Figure 2	0.25			V/ns
t_f	Fall slew rate(1)	(80% to 20%) × VDD, see Figure 2	0.25			V/ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, see Figure 4	0.75			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, see Figure 4	0.75			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑ or LS_CLK ↓, see Figure 4	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑ or LS_CLK ↓, see Figure 4	1.5			ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, see Figure 3	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, see Figure 3	0.7	1		V/ns
t_c	Cycle time DCLK	See Figure 4	1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, see Figure 4	0.75			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, see Figure 4	0.75			ns
t_{WINDOW}	Window time	Setup time + Hold time, see Figure 4, Figure 5	0.3			ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(2)				2000	ns

(1) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 2.
(2) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

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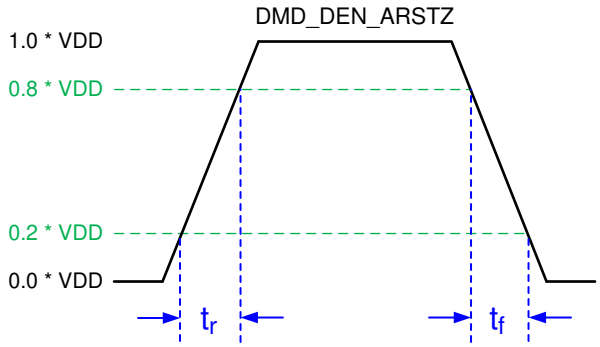

Figure 2. LPSDR Input Rise and Fall Slew Rate

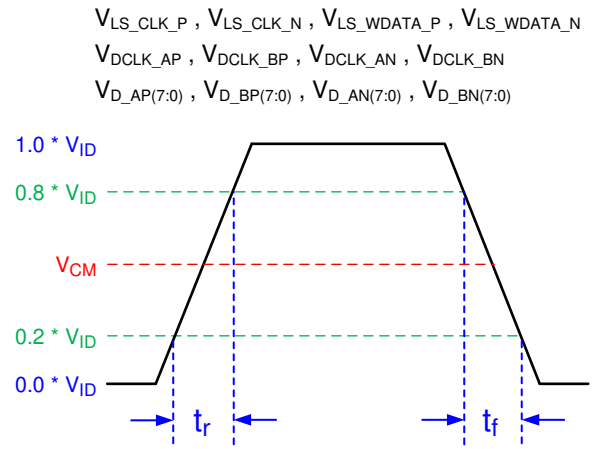

Figure 3. SubLVDS Input Rise and Fall Slew Rate

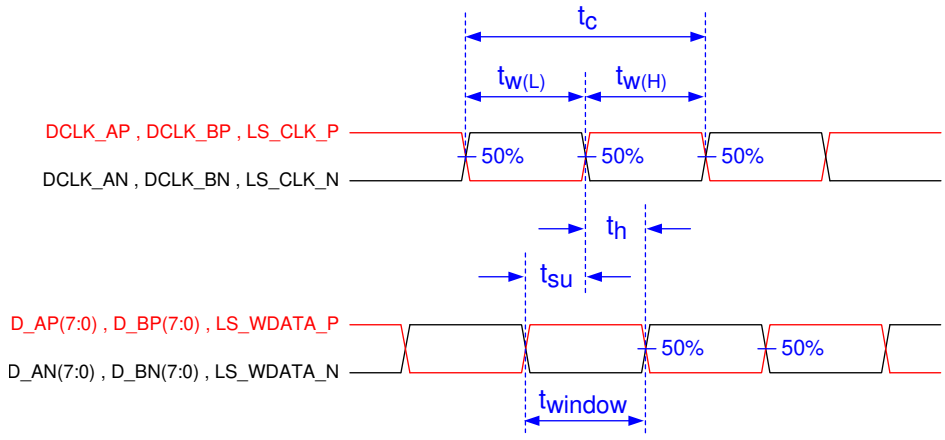

Figure 4. SubLVDS Switching Parameters

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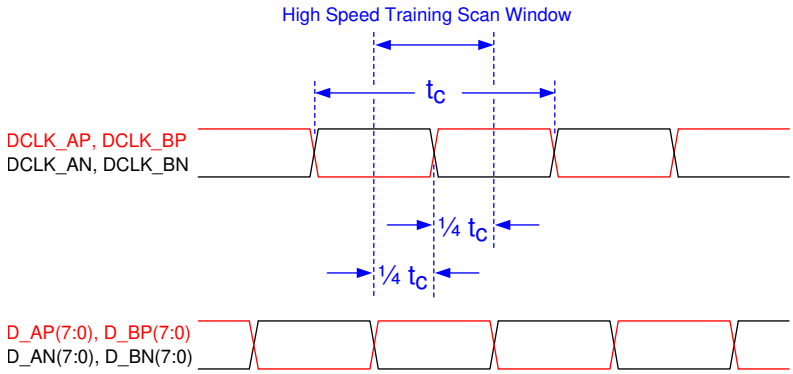

Figure 5. High-Speed Training Scan Window

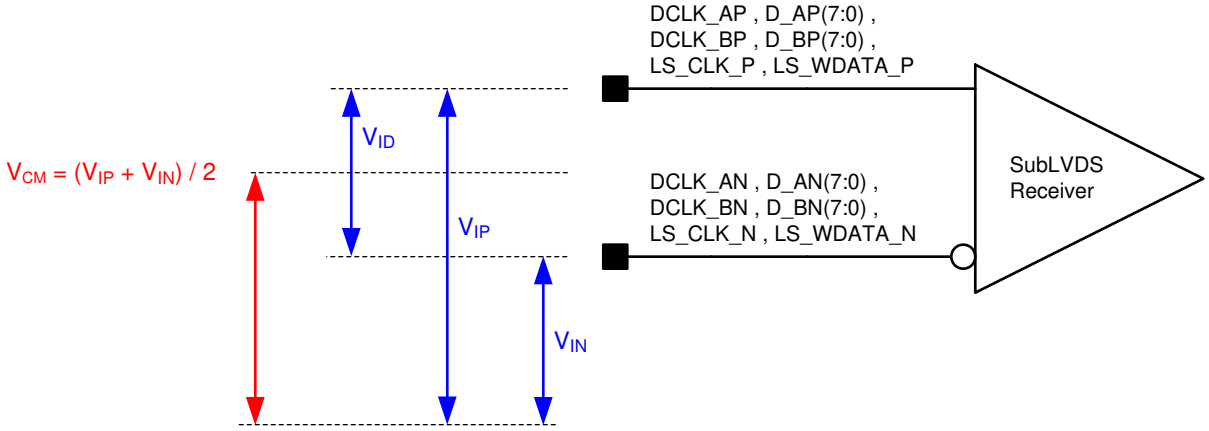

Figure 6. SubLVDS Voltage Parameters

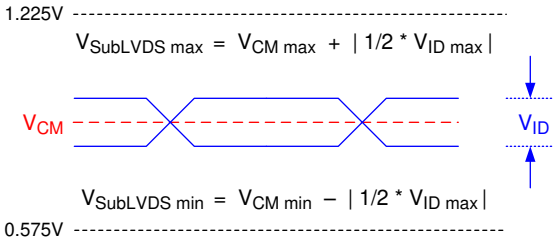

Figure 7. SubLVDS Waveform Parameters

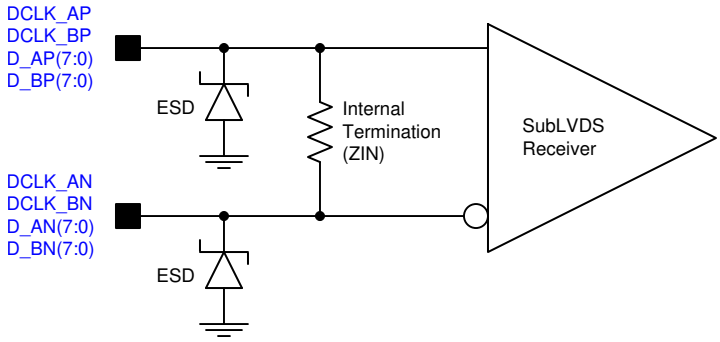

Figure 8. SubLVDS Equivalent Input Circuit

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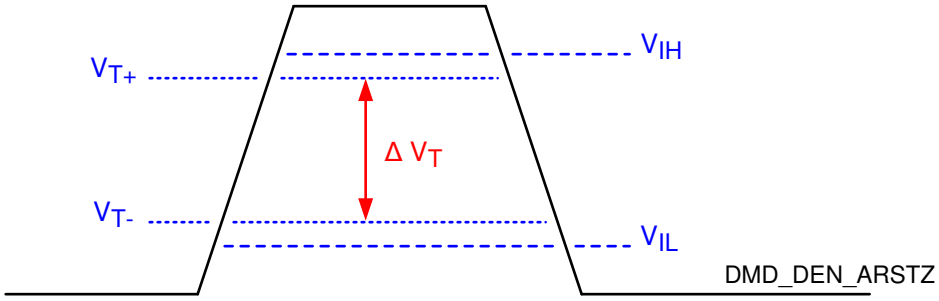

Figure 9. LPSDR Input Hysteresis

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6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output. See Figure 10, Figure 11	C_L = 45 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

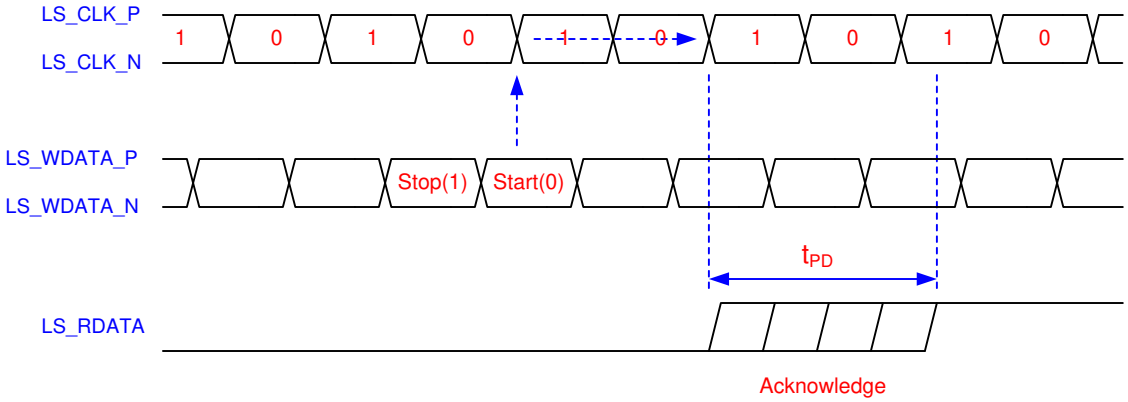
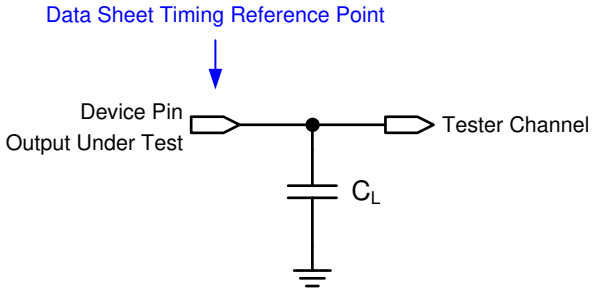


Figure 10. LPSDR Read Out



See *Sub-LVDS Data Interface* for more information.

Figure 11. Test Load Circuit for Output Propagation Measurement

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6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1: Maximum load evenly distributed within each area(1)				
Thermal Interface Area			110.8	N
Electrical Interface Area			111.3	
Condition 2: Maximum load evenly distributed within each area(1)				
Thermal Interface Area			0	N
Electrical Interface Area			222.1	

(1) See Figure 12.

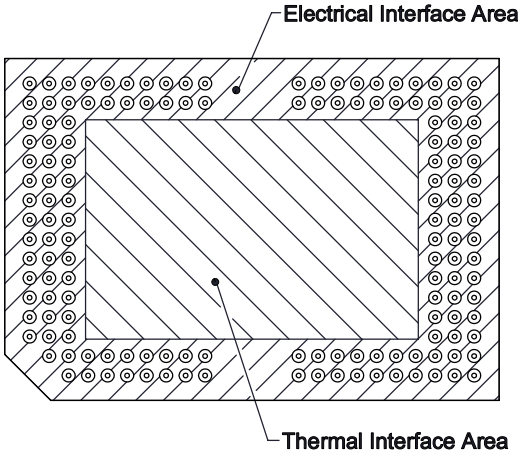

Figure 12. System Interface Loads

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6.10 Physical Characteristics of the Micromirror Array

PARAMETER			VALUE	UNIT
M	Number of active columns	See Figure 13	1152	micromirrors
N	Number of active rows	See Figure 13	1152	micromirrors
ε	Micromirror (pixel) pitch - diagonal	See Figure 14	7.6	µm
P	Micromirror (pixel) pitch - horizontal and vertical	See Figure 14	10.8	µm
	Micromirror active array width	P × M + P / 2; see Figure 13	12.447	mm
	Micromirror active array height	(P × N) / 2 + P / 2; see Figure 13	6.226	mm
	Micromirror active border	Pond of micromirrors (POM)(1)	10	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

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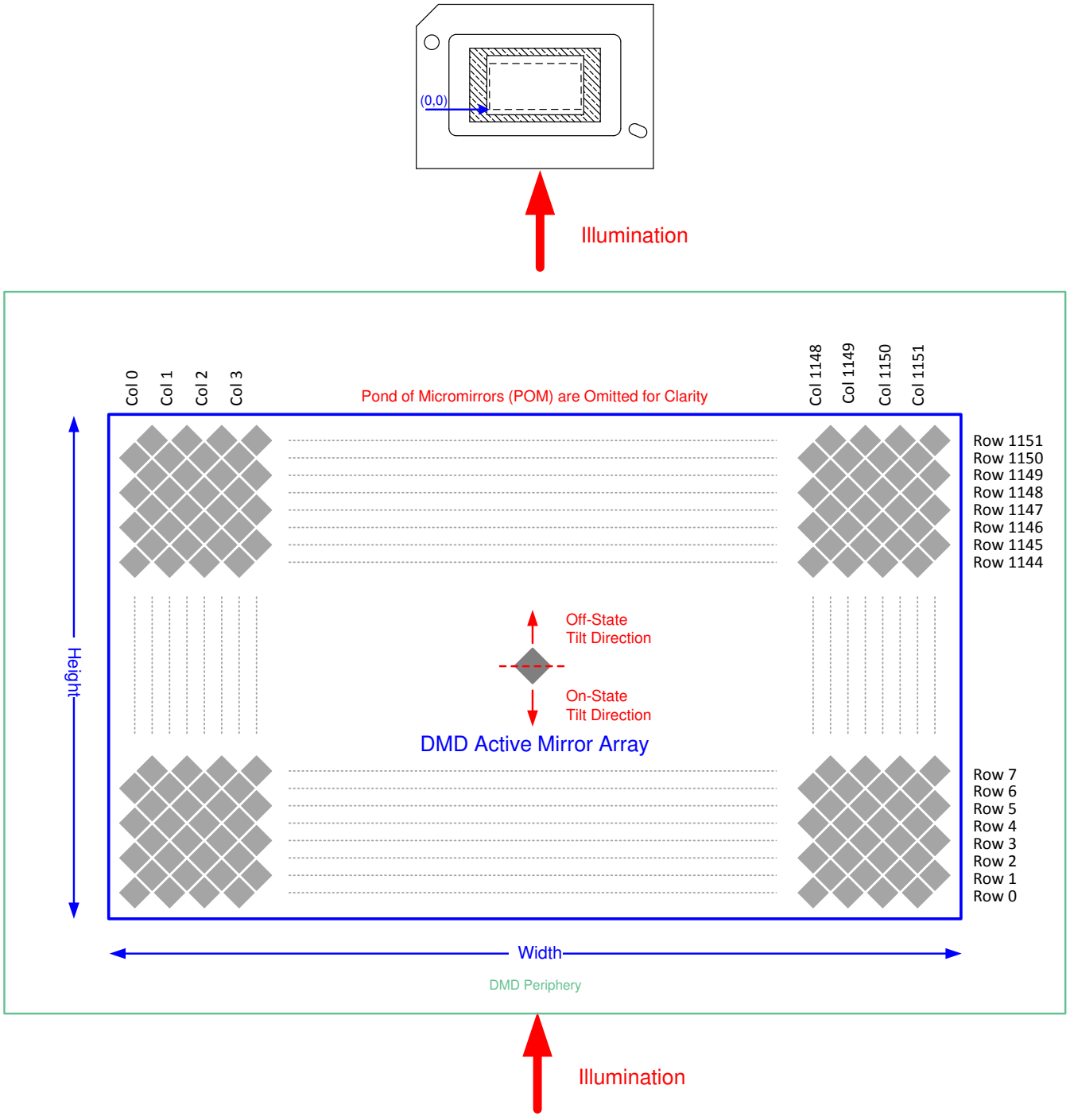

Figure 13. Micromirror Array Physical Characteristics

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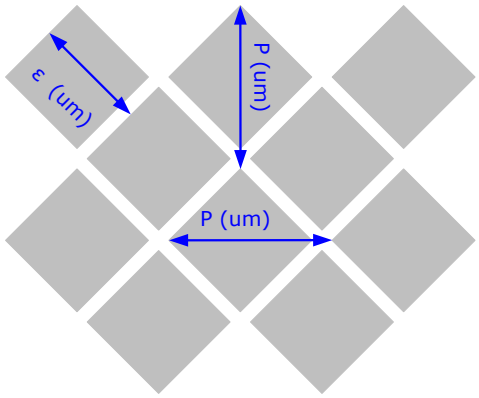

Figure 14. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		12		degree
Micromirror tilt angle tolerance(2)		–1		1	degree
DMD efficiency(3)	400 nm - 700 nm		66%		
Number of non-operational micromirrors(4)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array at 25°C.
(2) For some applications, it is critical to account for the micromirror tilt angle variation in the overall optical system design. With some optical system designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some optical system designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic micromirror landed duty-cycle and do not include system optical efficiency or overfill loss. This number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical system. The factors that can influence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in the *DMD Optical Efficiency Application Note*.
(4) A non-operational micromirror is defined as a micromirror that is unable to transition between the on-state and off-state positions.

6.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(1)				See (1)	

(1) See the mechanical package ICD for details regarding the size and location of the window aperture.

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6.13 Chipset Component Usage Specification

The DLP5534-Q1 is a component of a chipset. Reliable function and operation of the DLP5534-Q1 requires that it be used in conjunction with the TPS99000-Q1 and DLPC230-Q1, and includes components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

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7 Detailed Description

7.1 Overview

The DLP5534-Q1 Automotive DMD consists of 1,327,104 highly reflective, digitally switchable, micrometer-sized mirrors organized in a two-dimensional array. As shown in Figure 15, the micromirror array consists of 1152 micromirror columns × 1152 micromirror rows in a diamond pixel configuration with a 2:1 aspect ratio.

Around the perimeter of the 1152 × 1152 array of micromirrors is a uniform band of border micromirrors called the Pond of Micromirrors (POM). The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1152 × 1152 active array.

Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row. Each mirror is switchable between two discrete angular positions: –12° and +12°. The mirrors are illuminated from the bottom which allows for compact and efficient system optical design.

Although the native resolution of the DLP5534-Q1 is 1152 × 1152, when paired with the DLPC230-Q1 controller, the DLP5534-Q1 can be driven with different resolutions to utilize the 2:1 aspect ratio. For example, display applications typically use a resolution of 1152 × 576. Please see the DLPC230-Q1 automotive DMD controller data sheet (DLPS054) for a list of supported resolutions. Diamond pixel arrays also have the capability to increase display resolution beyond native resolution. Future controllers or video formatters may take advantage of this enhanced resolution.

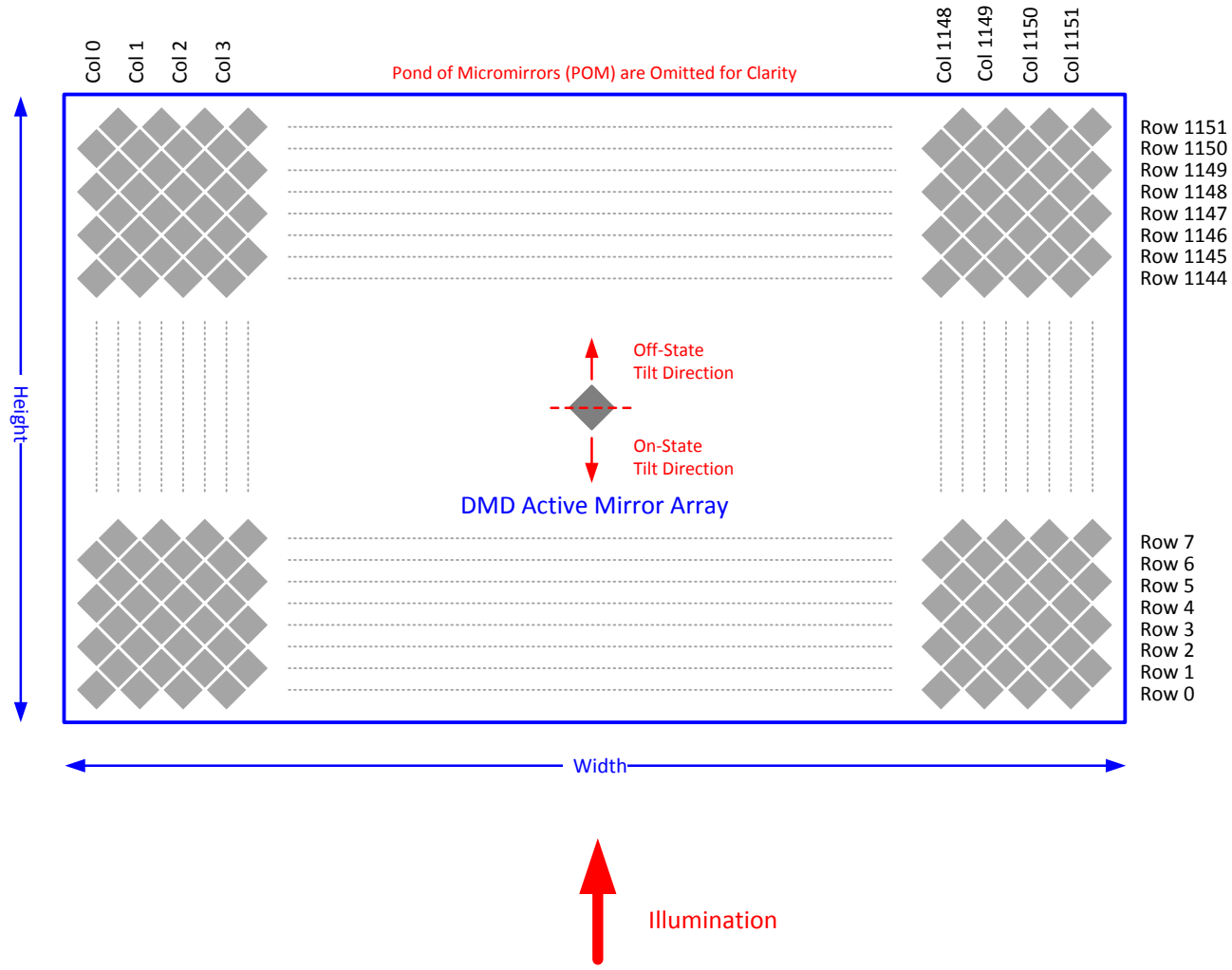

Figure 15. 0.55-in 1.3-MP Micromirror Array

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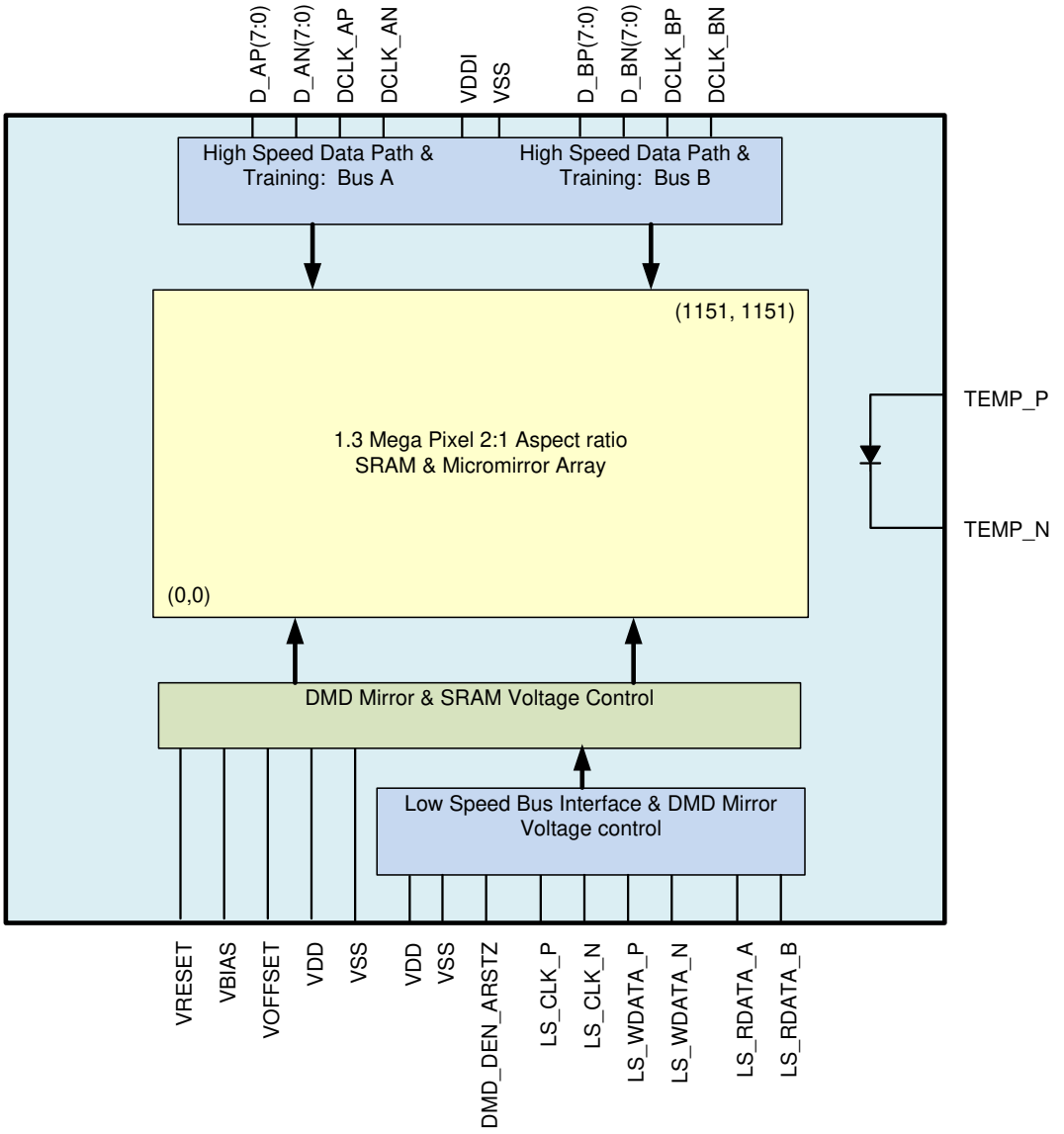
7.2 Functional Block Diagram



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7.3 Feature Description

The DLP5534-Q1 consists of a two-dimensional array of 1-bit CMOS memory cells driven by a sub-LVDS bus from the DLPC230-Q1 and powered by the TPS99000-Q1. The temperature sensing diode is used to continuously monitor the DMD array temperature.

To ensure reliable operation the DLP5534-Q1 must be used with the DLPC230-Q1 DMD display controller and the TPS99000-Q1 system management and illumination controller.

7.3.1 Sub-LVDS Data Interface

The Sub-LVDS signaling protocol was designed to enable very fast DMD data refresh rates while simultaneously maintaining low power and low emission.

Data is loaded into the SRAM under each micromirror using the sub-LVDS interface from the DLPC230-Q1. This interface consists of 16 pairs of differential data signals plus two clock pairs into two separate buses A and B loading the left and right half of the SRAM array. The data is latched on both transitions creating a double data rate (DDR) interface. The sub-LVDS interface also implements a continuous training algorithm to optimize the data and clock timing to allow for a more robust interface.

The entire DMD array of 1.3 million pixels can be updated at a rate of less than 100 µs as a result of the high speed sub-LVDS interface.

7.3.2 Low Speed Interface for Control

The purpose of the low speed interface is to configure the DMD at power up and power down and to control the micromirror reset voltage levels that are synchronized with the data loading. The micromirror reset voltage controls the time when the mirrors are mechanically switched. The low speed differential interface includes 2 pairs of signals for write data and clock, and 2 single-ended signals for output (A and B).

7.3.3 DMD Voltage Supplies

The micromirrors require unique voltage levels to control the mechanical switching from –12° to +12°. These voltage levels are nominally 16 V, 8.5 V, and –10 V (VBIAS, VOFFSET, and VRESET), and are generated by the TPS99000-Q1.

7.3.4 Asynchronous Reset

Reset of the DMD is required and controlled by the DLPC230-Q1 via the signal DMD_DEN_ARSTZ.

7.3.5 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411 temperature monitoring device. The DLPC230-Q1 monitors the DMD array temperature via the TMP411 and temperature sense diode. The DLPC230-Q1 operation of the DMD timing is based in part on the DMD array temperature, therefore this connection is essential to ensure reliable operation of the DMD.

Figure 16 shows the typical connection between the DLPC230-Q1, TMP411, and the DMD.

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Feature Description (continued)

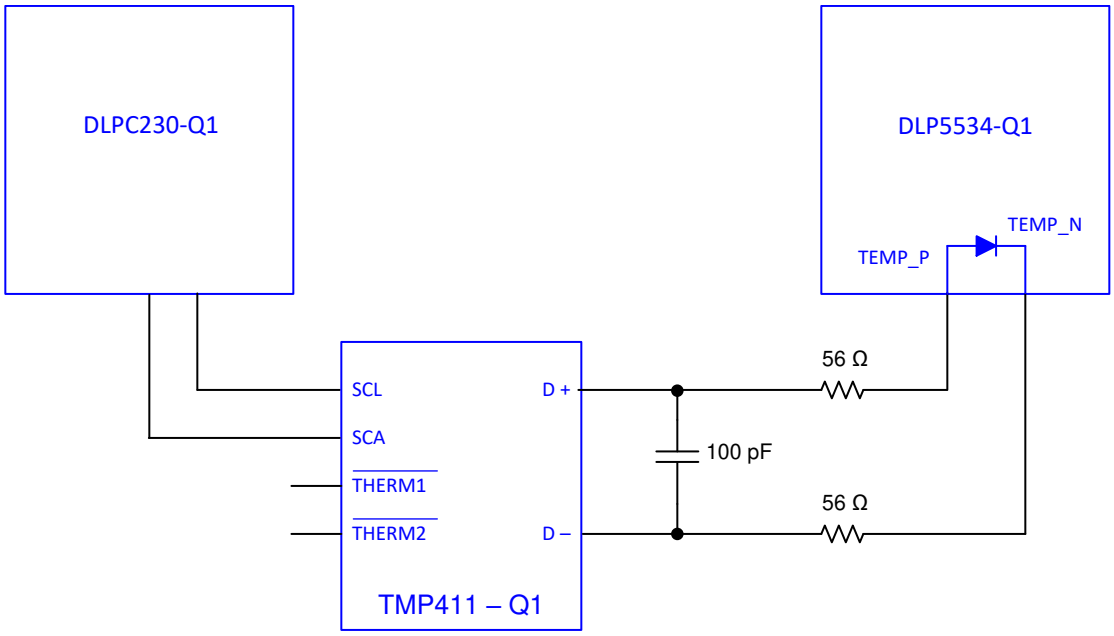

Figure 16. Temperature Sense Diode Typical Circuit Configuration

7.3.5.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Three different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base–emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the TMP411-Q1 data sheet for detailed information about temperature diode theory and measurement. Figure 17 and Figure 18 illustrate the relationships between the current and voltage through the diode.

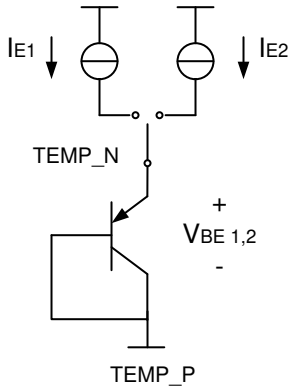

Figure 17. Temperature Measurement Theory

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Feature Description (continued)

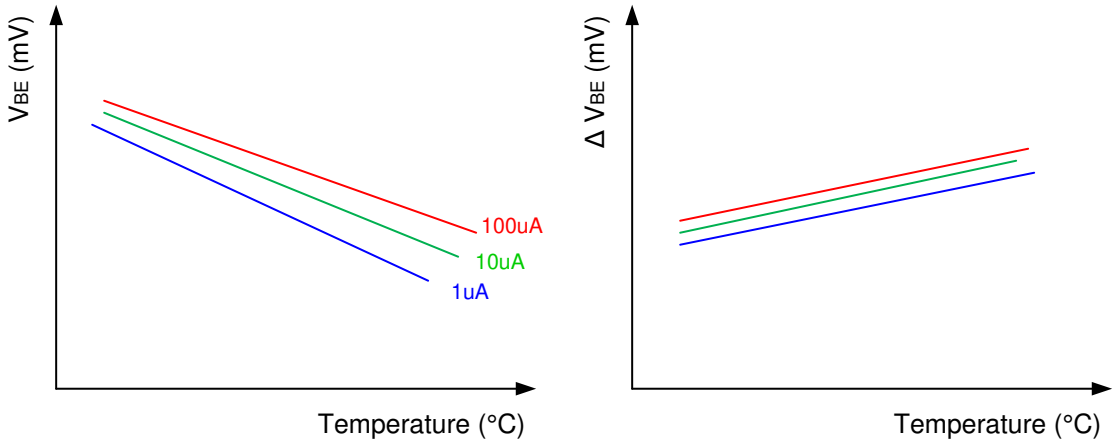

Figure 18. Example of Delta VBE Versus Temperature

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7.4 System Optical Considerations

Optimizing system optical performance and image performance strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.4.1 Numerical Aperture and Stray Light Control

The numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This cone angle defined by the numerical aperture should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines the DMD's capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces.

7.4.2 Pupil Match

TI's optical and image performance specifications assume that the exit pupil of the illumination optics is nominally centered and located at the entrance pupil position of the projection optics. Misalignment of pupils between the illumination and projection optics can degrade screen image uniformity and cause objectionable artifacts in the display's border and/or active area. These artifacts may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

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System Optical Considerations (continued)

7.4.3 Illumination Overfill

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible.

Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Heat load on the aperture in the areas shown in Figure 1 should not exceed the values listed in *Recommended Operating Conditions*. This area is a 0.5-mm wide area the length of the aperture opening. The values listed in *Recommended Operating Conditions* assume a uniform distribution. For a non-uniform distribution please contact TI for additional information.

NOTE

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED PREVIOUSLY.

7.5 Micromirror Array Temperature Calculation

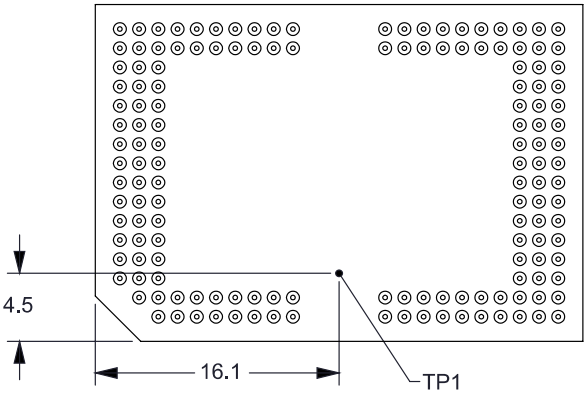

Figure 19. DMD Thermal Test Points

The active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in Figure 19) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + (Q_{INCIDENT} \times \text{DMD Absorption Constant}) \quad (2)$$

where

- T_{ARRAY} = computed DMD array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature, TP1 location in Figure 19 (°C)
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to thermal test point TP1 (°C/W), see *Thermal Information*
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (W)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (W)
- $Q_{INCIDENT}$ = incident optical power to DMD (W)
- DMD Absorption Constant = 0.42

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Micromirror Array Temperature Calculation (continued)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown above are valid for a 1-chip DMD system with illumination distribution of 83.7% on the active array and 16.3% on the array border.

The following is a sample calculation for a typical projection application:

1. $Q_{ELECTRICAL}$ = 0.4 W
2. $T_{CERAMIC}$ = 55°C
3. $Q_{INCIDENT}$ = 3 W
4. Q_{ARRAY} = 0.4 W + (3 W × 0.42) = 1.66 W
5. T_{ARRAY} = 55°C + (1.66 W × 1.1°C/W) = 56.8°C

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7.6 Micromirror Landed-On/Landed-Off Duty Cycle

7.6.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP5534-Q1 chipset is designed to support projection-based automotive applications such as transparent window display systems.

8.2 Typical Application

The chipset consists of three components—the DLP5534-Q1 automotive DMD, the DLPC230-Q1, and the TPS99000-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC230-Q1 is a controller for the DMD; it formats incoming video and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video. The TPS99000-Q1 is a controller for the illumination sources (e.g. LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC230-Q1 and the TPS99000-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features. Figure 20 is a system level block diagram with these devices in the DLP head-uptransparent window display configuration and shows the primary features and functions of each device.

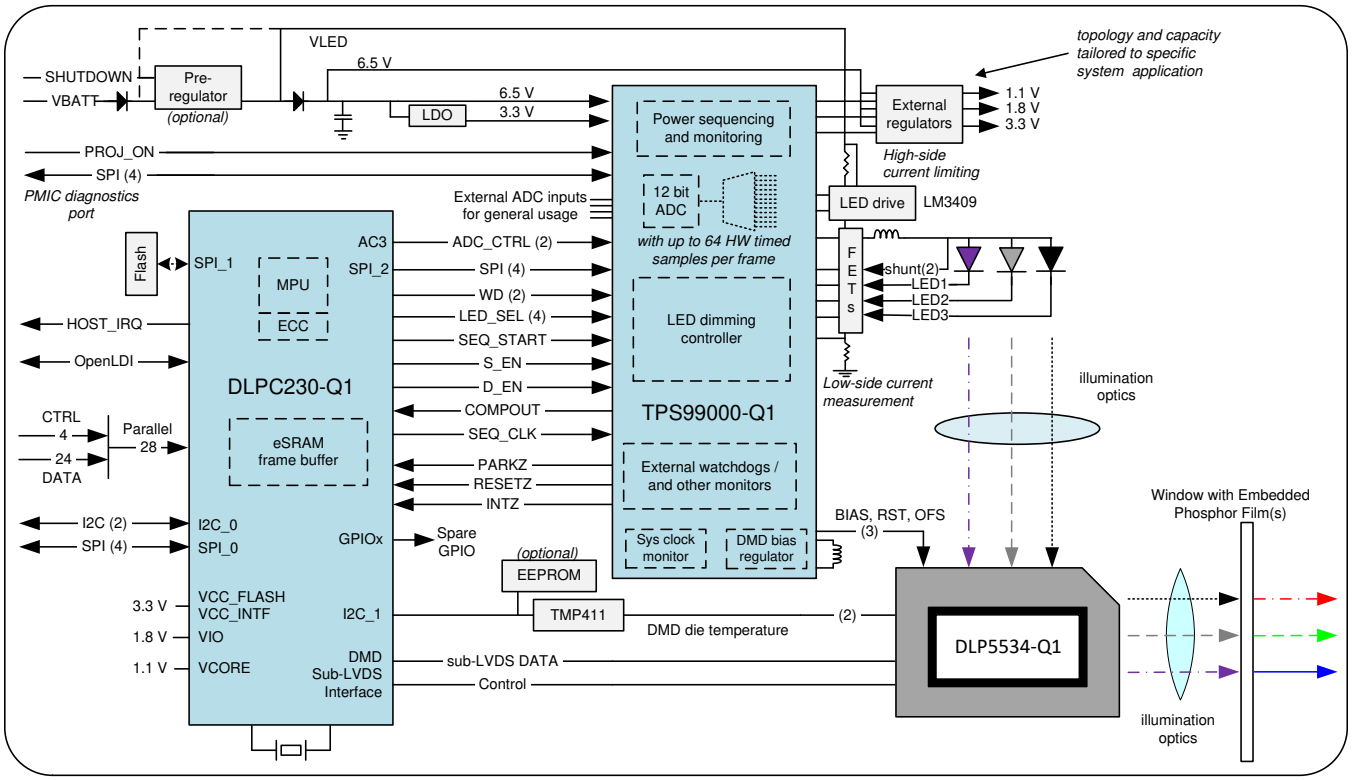

Figure 20. Transparent Window Display System Block Diagram

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Typical Application (continued)

8.2.1 Application Overview

Figure 20 shows the system block diagram for a DLP projector in a 405-nm based transparent window display system. The system uses the DLPC230-Q1, TPS99000-Q1, and the DLP5534-Q1 automotive DMD to enable a transparent window display with high brightness, high efficiency, and high resolution. The combination of the DLPC230-Q1 and TPS99000-Q1 removes the need for external SDRAM and a dedicated microprocessor. The chipset manages the illumination control of LED sources, power sequencing functions, and system management functions. Additionally, the chipset supports numerous system diagnostic and built-in self test (BIST) features. The following paragraphs describe the functionality of the chipset used for a 405-nm projection system in more detail.

The DLPC230-Q1 is a controller for the DMD and the light sources in the DLP projector module. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video. The DLPC230-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create a video with grayscale shading and multiple colors, if applicable.

The DLPC230-Q1 receives inputs from a host processor in the vehicle. The host provides commands and input video data. Host commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for host commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits or 16-bits of data for single light source or dual light source systems depending on the system design. The SPI flash memory provides the embedded software for the DLPC230-Q1's ARM core and default settings. The TPS99000-Q1 provides diagnostic and monitoring information to the DLPC230-Q1 using an SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^2C interface to provide the DMD array temperature to the DLPC230-Q1.

The outputs of the DLPC230-Q1 are configuration and monitoring commands to the TPS99000-Q1, timing controls to the LED or laser driver, control and data signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC230-Q1 communicates with the TPS99000-Q1 over an SPI bus. It uses this to configure the TPS99000-Q1 and to read monitoring and diagnostics information from the TPS99000-Q1. The DLPC230-Q1 sends drive enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a sub-LVDS interface.

The TPS99000-Q1 is a highly integrated mixed-signal IC that controls DMD power and provides monitoring and diagnostics information for the DLP projector module. The power sequencing and monitoring blocks of the TPS99000-Q1 properly power up the DMD and provide accurate DMD voltage rails (–16 V, 8.5 V, and 10 V), and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000-Q1 has several general-purpose ADCs that designers can use for system level monitoring, such as over-brightness detection.

The TPS99000-Q1 receives inputs from the DLPC230-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC230-Q1 sends configuration and control commands to the TPS99000-Q1 over an SPI bus and several other control signals. The DLPC230-Q1's clocks are also monitored by the watchdogs in the TPS99000-Q1 to detect any errors. The power rails are monitored by the TPS99000-Q1 in order to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000-Q1 using a dedicated SPI bus, which enables independent monitoring. Additionally the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000-Q1 has several general-purpose ADCs that can be used to implement system level monitoring functions.

The outputs of the TPS99000-Q1 are diagnostic information and error alerts to the DLPC230-Q1, and control signals to the LED or laser driver. The TPS99000-Q1 can output diagnostic information to the host and the DLPC230-Q1 over two SPI buses. In case of critical system errors, such as power loss, it outputs signals to the DLPC230-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data), and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface with the DLPC230-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system the mirrors are used as pixels in order to display an image.

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Typical Application (continued)

8.2.2 Reference Design

For information about connecting together the DLP5534-Q1 DMD, DLPC230-Q1 controller, and TPS99000-Q1, please contact the TI Application Team for additional information about the DLP5534-Q1 evaluation module (EVM). TI has optical-mechanical reference designs available, see the TI Application team for more information.

8.2.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation, the automotive DMD reliability lifetime estimates Application Report may be provided. Please contact the TI Applications team for more information.

8.2.4 Illumination Mission Profile Considerations

TI has performed evaluations at 405-nm illumination wavelengths under certain conditions. These conditions should be considered when evaluating the final application's implementation. Please contact the TI Applications team for details about this testing.

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9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VDD, VDDI, VOFFSET, VBIAS, and VRESET. All VSS connections are also required. DMD power-up and power-down sequencing is strictly controlled by the TPS99000-Q1 devices.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. VSS must also be connected.

9.1 Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 21.

9.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions* (Refer to Note 2 in Figure 21).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 21.

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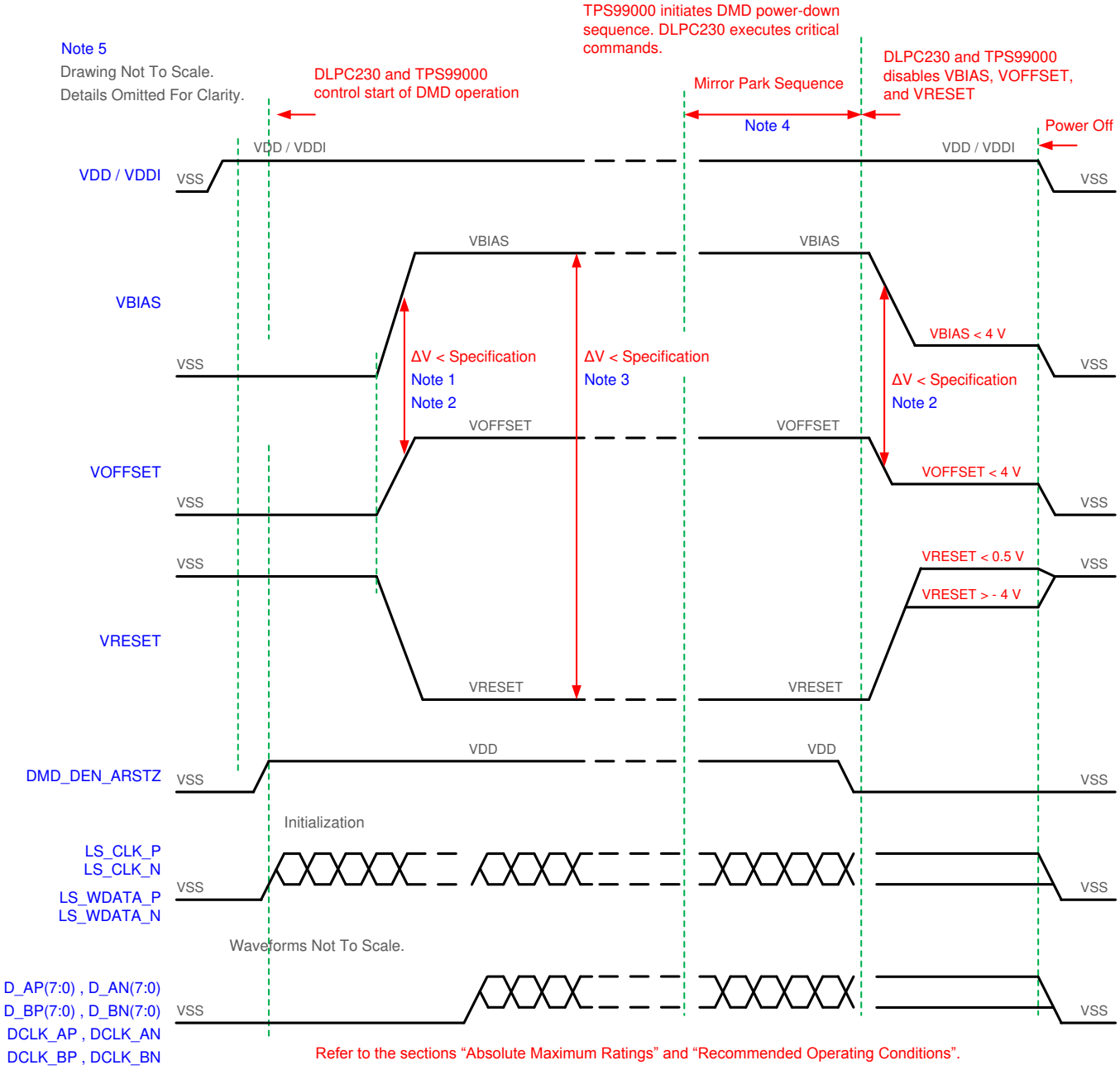
9.3 Power Supply Sequencing Requirements



(1) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in the *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Also, TPS99000-Q1 is capable of managing the timing between VBIAS and VOFFSET.

(2) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified than the limit shown in the *Recommended Operating Conditions*.

(3) When system power is interrupted, the TPS9000 initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the Micromirror Park Sequence.

(4) Drawing is not to scale and details are omitted for clarity.

Figure 21. Power Supply Sequencing Requirements (Power Up and Power Down)

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10 Layout

10.1 Layout Guidelines

Please refer to the DLPC230-Q1 and TPS99000-Q1 data sheets for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals.
- Minimum of two 220-nF decoupling capacitors close to VBIAS.
- Minimum of two 220-nF decoupling capacitors close to VRESET.
- Minimum of two 220-nF decoupling capacitors close to VOFFSET.
- Minimum of four 100-nF decoupling capacitors close to VDDI and VDD.
- Temperature diode pins

  The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411 are sensitive to noise. Please see the TMP411 data sheet for specific routing recommendations.

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの項目表記

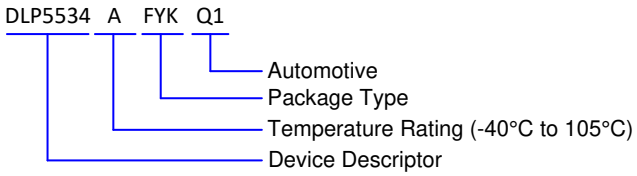

図 22. 型番の説明

11.1.2 デバイスのマーキング

デバイスのマーキングには、人間が読める文字列として「GHJJJJK　DLP5534AFYKQ1」が記載されています。GHJJJJK はロットのトレース・コードです。DLP5534AFYKQ1 は型番です。

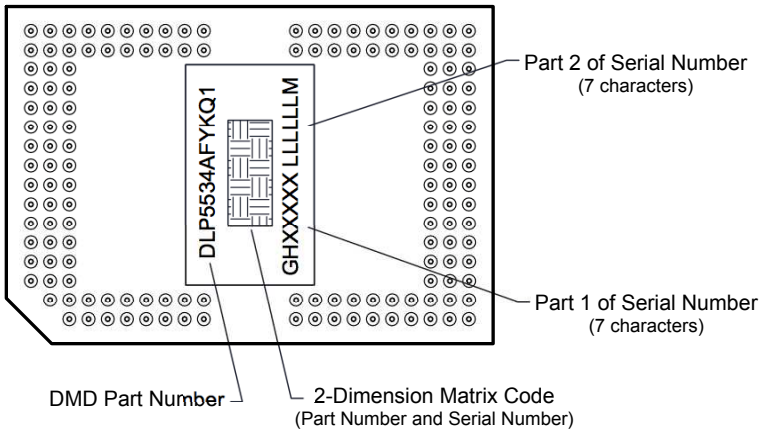

図 23. DMDマーキング

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11.2 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.5 DMD の取り扱い

DMD は光学デバイスであるため、ガラス窓の損傷を避けるために十分注意する必要があります。DMD の正しい取り扱い方法の説明は、『DLPA019 DMD Handling』アプリケーション・ノート (英語) を参照してください。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLP5534AFYKQ1	Active	Production	CPGA (FYK) | 149	33 | JEDEC TRAY (10+1)	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	
DLP5534AFYKQ1.A	Active	Production	CPGA (FYK) | 149	33 | JEDEC TRAY (10+1)	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	
DLP5534AFYKQ1.B	Active	Production	CPGA (FYK) | 149	33 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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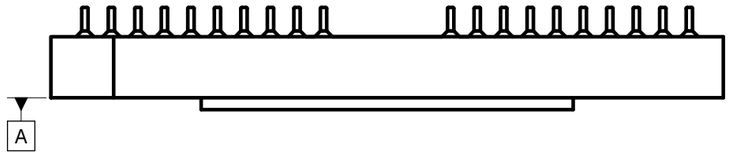
DWG NO.	2514853	SH	1

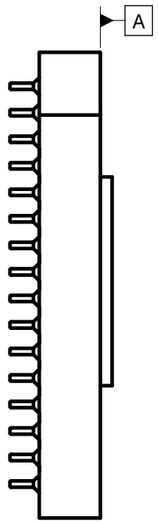
REVISIONS

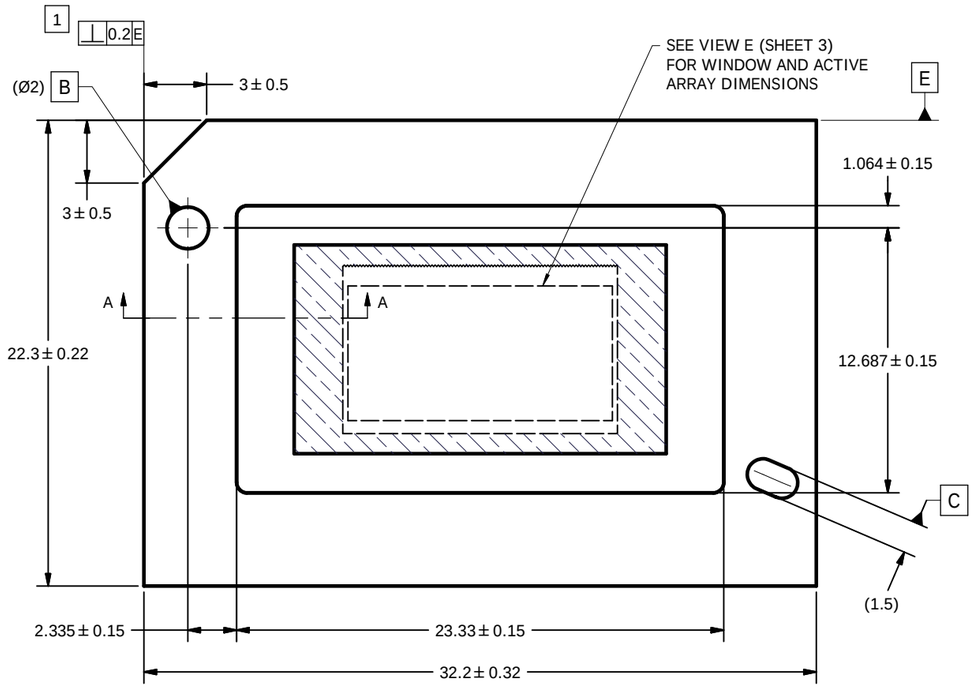
REV	DESCRIPTION	DATE	BY
A	ECO 2155049: INITIAL RELEASE	12/7/2015	BMH
B	ECO 2165903: UPDATE SUBSTRATE BACK MARKING, SH. 4	4/25/2017	BMH
C	ECO 2170159: RELAX DIE HEIGHT TOL., WAS +/-0.08	11/9/2017	BMH

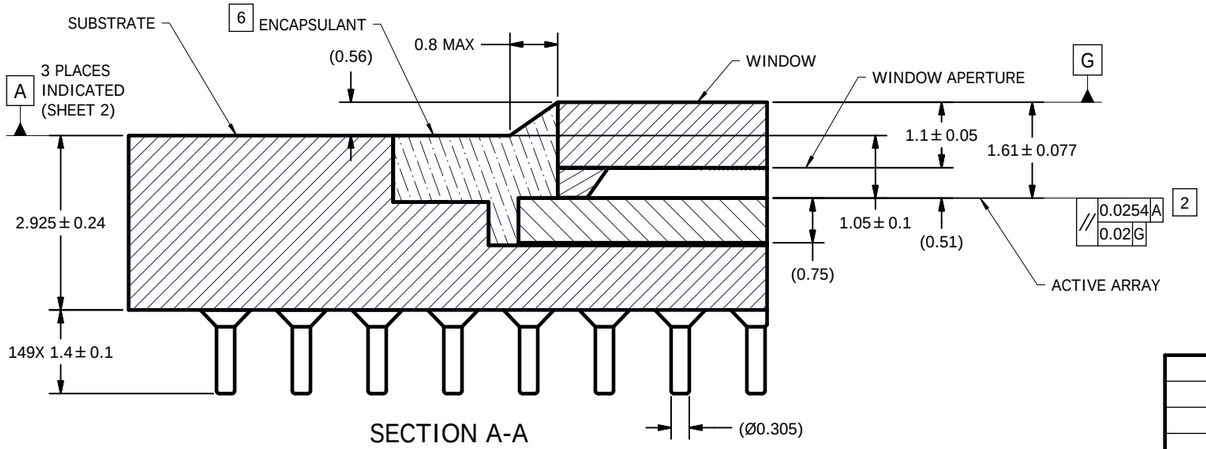
NOTES UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE.
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM VALUE OF 0.8 DEGREES.
4. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE.
5. BOUNDARY MIRRORS SURROUNDING THE ACTIVE ARRAY.
6. MAXIMUM ENCAPSULANT PROFILE SHOWN.
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULATION SHALL NOT EXCEED 0.2 THICKNESS MAXIMUM.
8. INDICATED CERAMIC SUBSTRATE FEATURES TO BE PLATED WITH 0.3 MICROMETERS MINIMUM ELECTROLYTIC GOLD OVER 0.1 MICROMETER MINIMUM PALLADIUM OVER 1.27-8.89 MICROMETERS ELECTROLYTIC NICKEL PER ASTM B488-01, ASTM B679-95(2009), AND AMS-QQ-N-290, RESPECTIVELY.
9. NOTE THAT THE ACTIVE ARRAY CENTER IS IN A DIFFERENT LOCATION FROM ALL PRIOR SERIES 450 DMD'S.









SECTION A-A
SCALE 20 : 1

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	12/7/2015
ENGINEER	B. HASKETT	12/7/2015
QA/CE	P. KONRAD	12/8/2015
CM	S. SUSI	12/8/2015
	M. DORAK	12/8/2015
APPROVED	B. RAY	12/8/2015

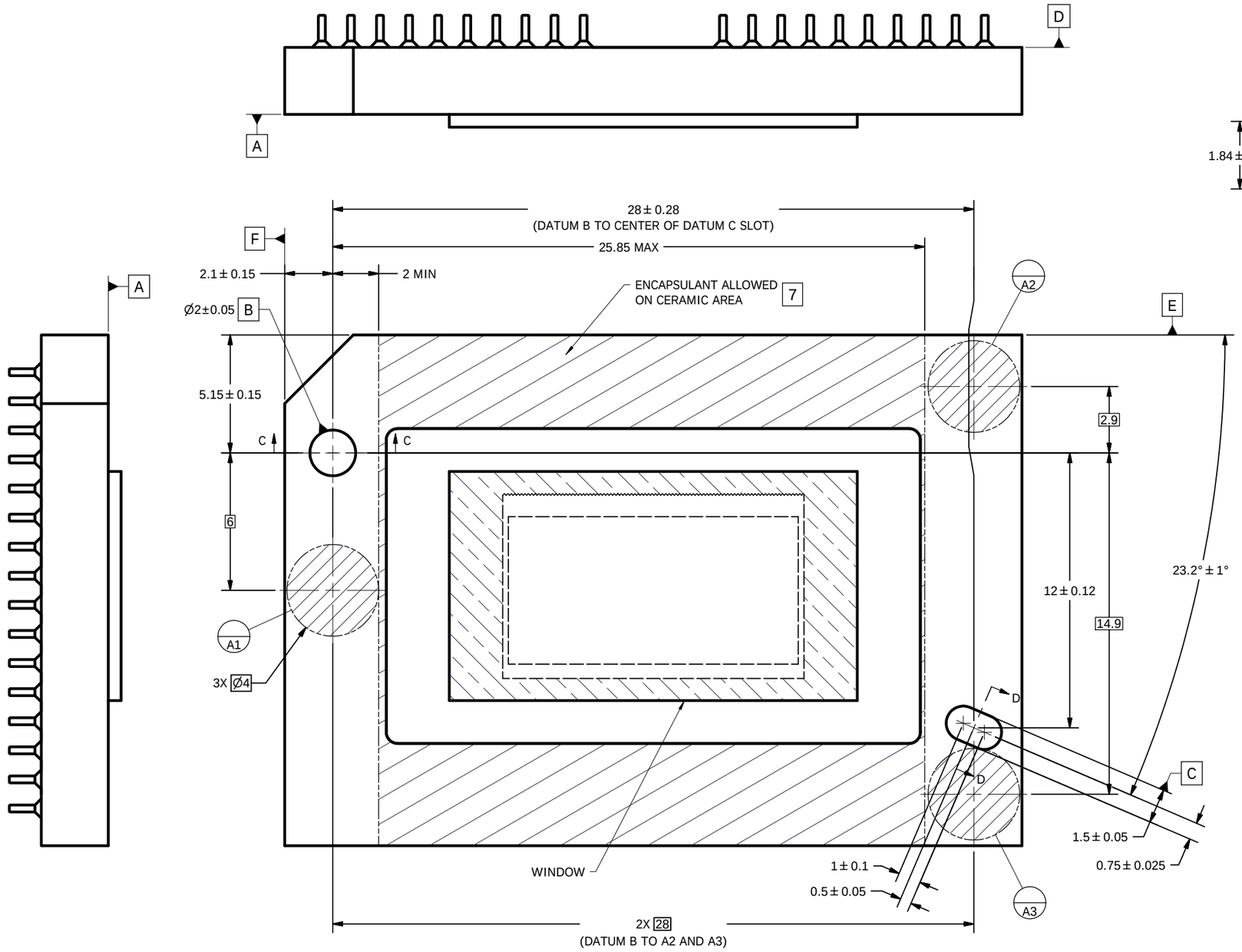
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD
.55 2:1 1.3MP SERIES 450 -A1
(FYK PACKAGE)

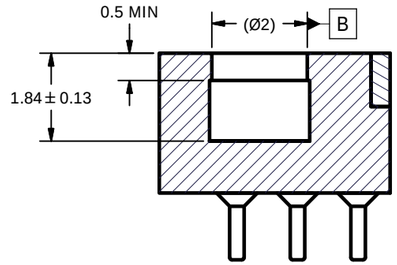
SIZE	DWG NO	REV
D	2514853	C

SCALE 4:1 SHEET 1 OF 4

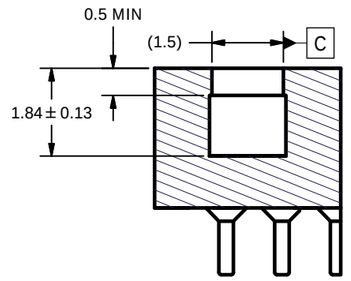
INV2013-DLPa



VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 10 : 1



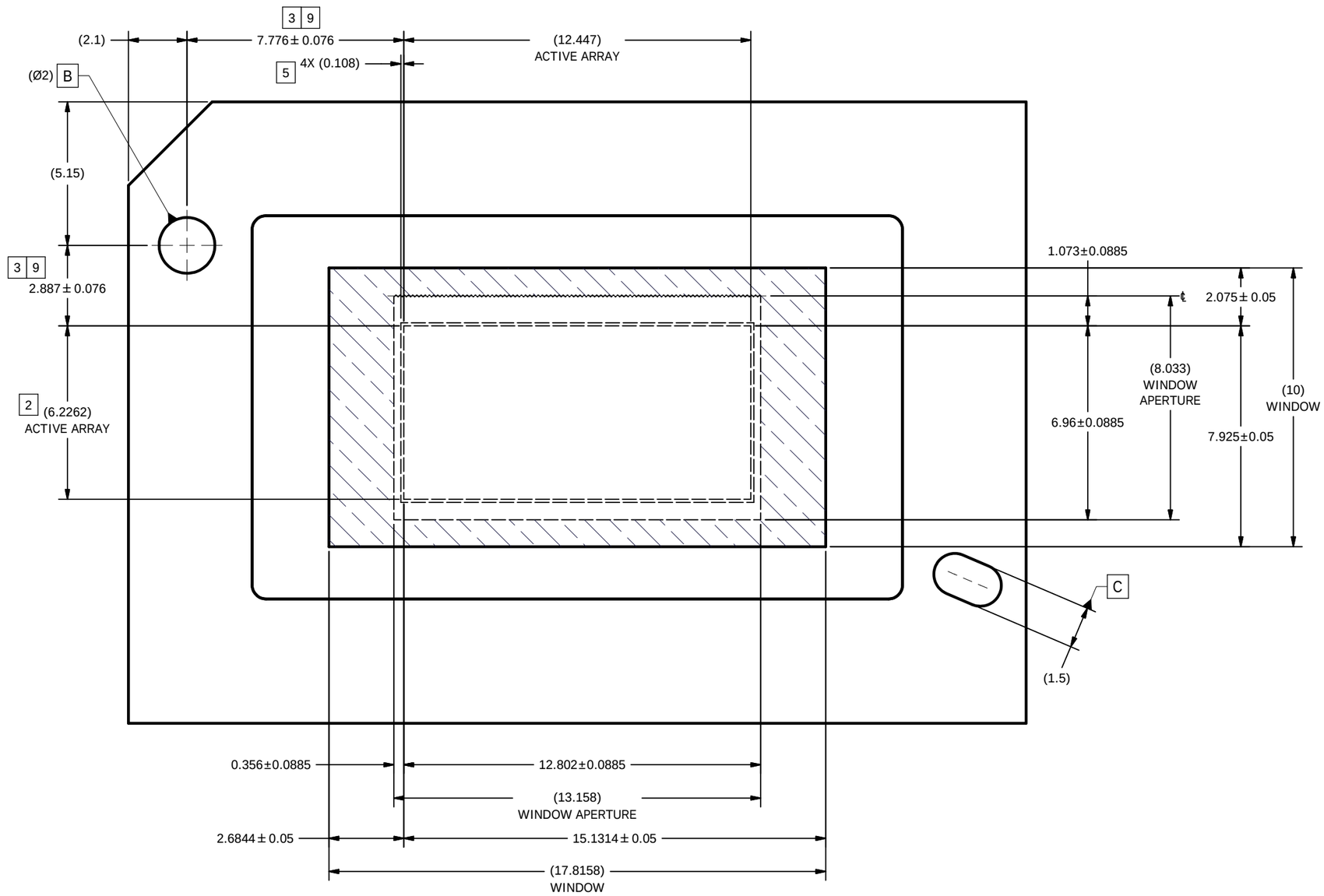
SECTION C-C
DATUM B
SCALE 16 : 1



SECTION D-D
DATUM C
(VIEW ROTATED FOR CLARITY)
SCALE 16 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 12/7/2015	SIZE D	DWG NO 2514853	REV C
			SCALE	SHEET 2 OF 4	

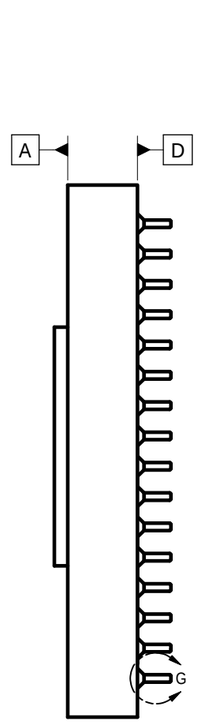
INV2013-DLPa

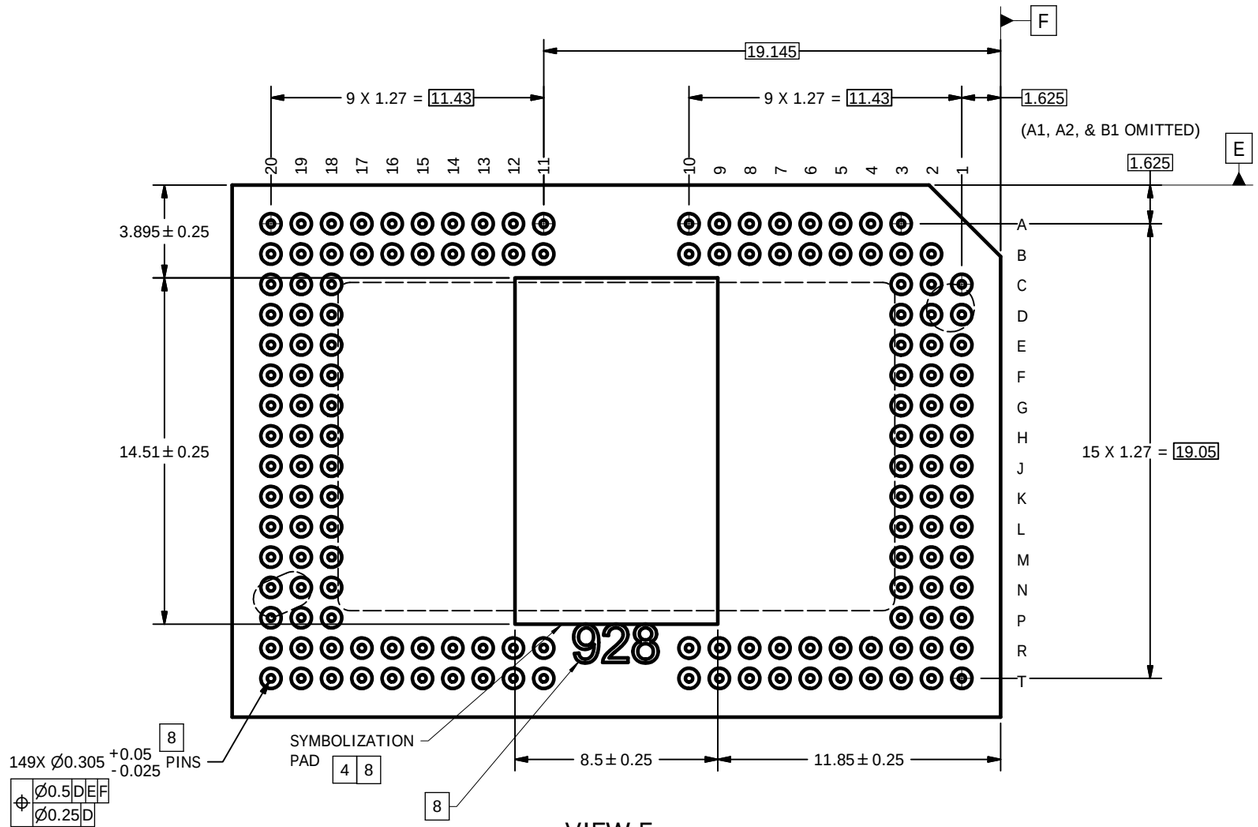


VIEW E
ACTIVE ARRAY AND WINDOW
SCALE 12 : 1

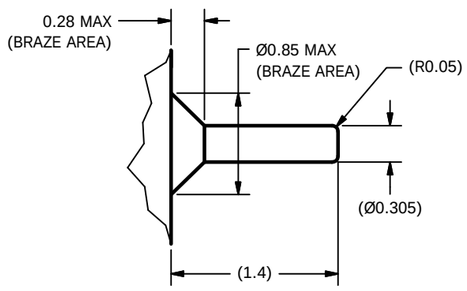
Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 12/7/2015	SIZE D	DWG NO 2514853	REV C
			SCALE	SHEET 3 OF 4	

INV2013-DLPa





VIEW F
PINS AND SYMBOLIZATION PAD
SCALE 8 : 1



DETAIL G
PIN AND BRAZE DIMENSIONS
149 PLACES
SCALE 40 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 12/7/2015	SIZE D	DWG NO 2514853 REV C
			SCALE	SHEET 4 OF 4

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