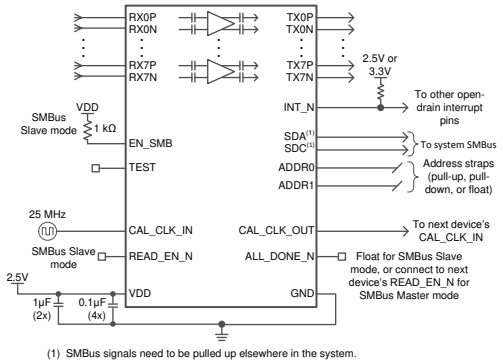
DS280DF810 28Gbps マルチレート 8 チャネル リタイマ

1 特長

- 信号コンディショニング内蔵の 8 チャネル マルチレート リタイマ
- すべてのチャネルが独立に 20.2Gbps～28.4Gbps でロック (10.1376Gbps、10.3125Gbps、12.5Gbps などのサブレートを含む)
- 非常に低いレイテンシ：28.4Gbps のデータ レートで 500ps 未満 (標準値)
- 単一電源で、低ジッタの基準クロックを必要とせず、AC カップリング コンデンサを内蔵しているため基板配線が簡単、BOM コストも低減可能
- 2×2 のクロス ポイントを内蔵
- アダプティブ連続時間リニア イコライザ (CTLE)
- アダプティブ デシジョン フィードバック イコライザ (DFE)
- 3 タップ FIR フィルタ付きの低ジッタ トランスミッタ
- 結合イコライゼーションにより、12.9GHz で 35dB 以上、14GHz で 30dB 以上のチャネル損失に対応
- 可変送信振幅：205mVppd～1225mVppd (標準値)
- オンチップのアイ オープニング モニタ (EOM)、PRBS パターン チェッカ/ジェネレータ
- フロースルー配線が簡単な小型の 8.00mm × 13.00mm BGA パッケージ
- 独自のピン配置により、パッケージの下に高速信号を配線可能
- ピン互換のリピータを使用可能
- 拡張温度範囲：-40 °C～85 °C

2 アプリケーション

- バックプレーンおよびミッドプレーンの範囲拡張
- フロント ポート光学系のジッタ クリーニング
- IEEE802.3bj 100GbE、Infiniband EDR、OIF-CEI-25G-LR/MR/SR/VSR の電気的インターフェイス
- SFP28、QSFP28、CFP2/CFP4、CDFP



概略回路図

3 概要

DS280DF810 は、信号コンディショニング機能を備えた 8 チャネル、マルチレート リタイマです。10^{-15} 以下のビット エラー レート (BER) を達成しながら、長距離で、損失が大きく、クロストークの影響を受ける高速シリアル リンクの到達距離と堅牢性を拡張するために使用します。

DS280DF810 の各チャネルは、20.2Gbps～28.4Gbps の連続した範囲のシリアル データ レート、またはサポートされている任意のサブレート (÷2 および ÷4、10.1376Gbps、10.3125Gbps、12.5Gbps などの主要データ レートを含む) に独立してロックします。これにより、DS280DF810 はレーンごとの前方誤り訂正 (FEC) パススルーをサポートできます。

物理的な AC カップリング コンデンサ (TX および RX) を内蔵しているため、PCB 上の外付けコンデンサは不要です。DS280DF810 は単一電源を備え、必要な外付け部品は最小限です。これらの特長により、PCB 配線の複雑性と BOM コストが低減されます。

DS280DF810 の高度なイコライゼーション機能には、低ジッタの 3 タップ送信有限インパルス応答 (FIR) フィルタ、アダプティブ連続時間リニア イコライザ (CTLE)、アダプティブ デシジョン フィードバック イコライザ (DFE) が含まれています。これにより、複数のコネクタやクロストークが存在する、損失の多い相互接続およびバックプレーンにおいて、到達距離を延長できます。内蔵の CDR 機能は、フロントポート光学モジュール アプリケーションで、ジッタ バジェットをリセットし、高速シリアル データをリタイムするのに最適です。DS280DF810 は、各チャネル ペアに 2x2 のクロスポイントを実装しているため、ホストはレーンクロスとファンアウトのどちらの方法も使用できます。

DS280DF810 は SMBus 経由または外付け EEPROM により構成できます。単一の EEPROM を、最大 16 個のデバイスで共有できます。非破壊的なオンチップのアイ モニタと PRBS ジェネレータ / チェッカにより、インシステム診断が可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
DS280DF810	ABV (fcBGA、135)	13mm × 8mm
	ABW (fcBGA、135)	13mm × 8mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

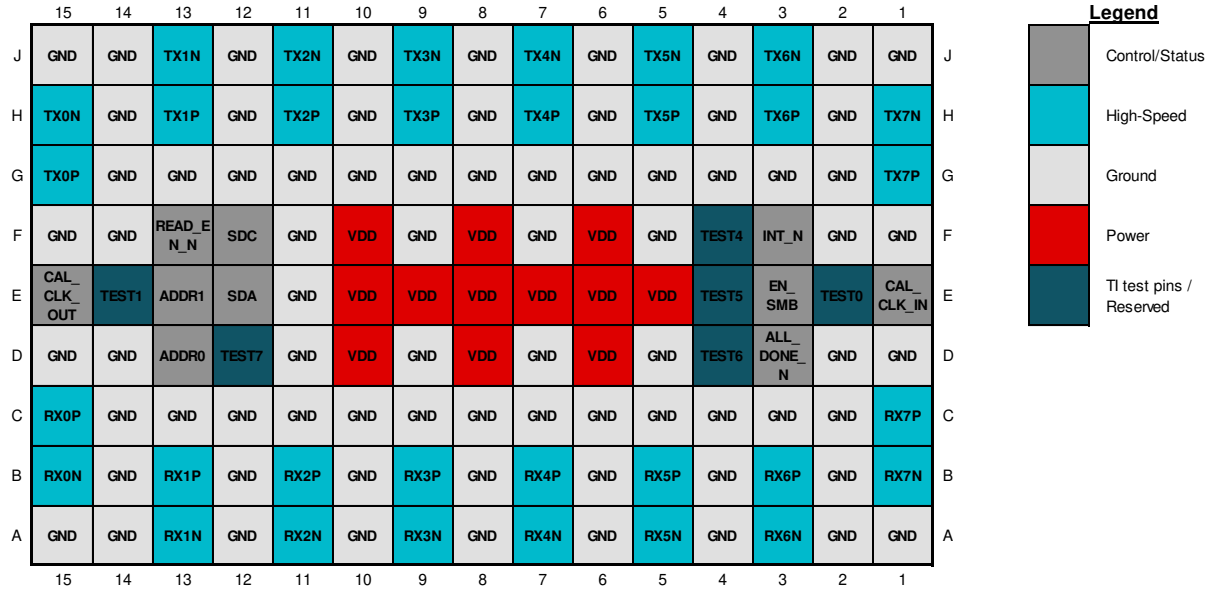

図 4-1. 135-Pin fcBGA, 0.8mm BGA Pin Pitch (Top View)

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表 4-1. Pin Functions

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
HIGH SPEED DIFFERENTIAL I/Os				
RX0P	C15	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX0N	B15	Input	None	
RX1P	B13	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX1N	A13	Input	None	
RX2P	B11	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX2N	A11	Input	None	
RX3P	B9	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX3N	A9	Input	None	
RX4P	B7	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX4N	A7	Input	None	
RX5P	B5	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX5N	A5	Input	None	
RX6P	B3	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX6N	A3	Input	None	
RX7P	C1	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220nF capacitors.
RX7N	B1	Input	None	
TX0P	G15	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX0N	H15	Output	None	
TX1P	H13	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX1N	J13	Output	None	
TX2P	H11	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX2N	J11	Output	None	
TX3P	H9	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX3N	J9	Output	None	
TX4P	H7	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX4N	J7	Output	None	
TX5P	H5	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX5N	J5	Output	None	
TX6P	H3	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX6N	J3	Output	None	
TX7P	G1	Output	None	Inverting and non-inverting 50Ω driver outputs. These outputs are AC coupled on-chip with physical 220nF capacitors.
TX7N	H1	Output	None	
CALIBRATION CLOCK PINS				
CAL_CLK_IN	E1	Input, 2.5V CMOS	Weak pull-down	25MHz (±100 PPM) 2.5V single-ended clock from external oscillator. No stringent phase noise or jitter requirements on this clock. Used to calibrate VCO frequency range. This clock is not used to recover data.
CAL_CLK_OUT	E15	Output, 2.5V CMOS	None	2.5V buffered replica of calibration clock input (pin E1) for connecting multiple devices in a daisy-chained fashion.

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表 4-1. Pin Functions (続き)

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
SYSTEM MANAGEMENT BUS (SMBUS) PINS				
ADDR0	D13	Input, 4-level	None	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1kΩ to GND R: 10kΩ to GND F: Float 1: 1kΩ to VDD Refer to セクション 6.4.4 for more information.
ADDR1	E13	Input, 4-level	None	
EN_SMB	E3	Input, 4-level	None	Four-level 2.5V input used to select between SMBus controller mode (float) and SMBus target mode (high). The four defined levels are: 0: 1kΩ to GND - RESERVED, TI test mode . R: 10kΩ to GND - RESERVED, TI test mode F: Float - SMBus Controller Mode 1: 1kΩ to VDD - SMBus Target Mode
SDA	E12	I/O, 3.3V LVCMOS, Open Drain	None	SMBus data input and open drain output. External 2kΩ to 5kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3V LVCMOS tolerant.
SDC	F12	I/O, 3.3V LVCMOS, Open Drain	None	SMBus clock input and open drain clock output. External 2kΩ to 5kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3V LVCMOS tolerant.
SMBUS MASTER MODE PINS				
READ_EN_N	F13	Input, 3.3V LVCMOS	Weak pull-up	SMBus Controller Mode (EN_SMB=Float): When asserted low, initiates the SMBus controller mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. This pin is 3.3V tolerant. SMBus Target Mode (EN_SMB=1): When asserted low, this causes the device to be held in reset (I^2C state machine reset and register reset). This pin should be pulled high or left floating for normal operation in SMBus Target Mode. This pin is 3.3V tolerant.
ALL_DONE_N	D3	Output, LVCMOS	None	Indicates the completion of a valid EEPROM register load operation when in SMBus Controller Mode (EN_SMB=Float): High = External EEPROM load failed or incomplete Low = External EEPROM load successful and complete When in SMBus target mode (EN_SMB=1), this output reflects the status of READ_EN_N input.
MISCELLANEOUS PINS				
INT_N	F3	Output, LVCMOS, Open-Drain	None	Open-drain 3.3V tolerant active-low interrupt output. It pulls low when an interrupt occurs. The events which trigger an interrupt are programmable through SMBus registers. This pin can be connected in a wired-OR fashion with other device's interrupt pin. A single pull-up resistor in the 2kΩ to 5kΩ range is adequate for the entire INT_N net.
TEST0	E2	Input, LVCMOS	Weak pull-up	Reserved TI test pins. During normal (non-test-mode) operation, these pins are configured as inputs and therefore they are not affected by the presence of a signal. These pins may be left floating, tied to GND, or connected to a 2.5V (max) output.
TEST1	E14	Input, LVCMOS	Weak pull-up	
TEST4	F4	Input, LVCMOS	Weak pull-up	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin should be tied to GND or left floating.
TEST5	E4	Input, LVCMOS	Weak pull-up	Reserved TI test pin. During normal (non-test-mode) operation, this pin is configured as an input and therefore is not affected by the presence of a signal. This pin may be left floating, tied to GND, or connected to a 2.5V (max) output.
TEST6	D4	Input, LVCMOS	Weak pull-up	
TEST7	D12	Input, LVCMOS	Weak pull-up	

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表 4-1. Pin Functions (続き)

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
POWER				
VDD	D6, D8, D10, E5, E6, E7, E8, E9, E10, F6, F8, F10	Power	None	Power supply, VDD = 2.5V ±5%. TI recommends connecting at least six de-coupling capacitors between the Retimer's VDD plane and GND as close to the Retimer as possible. For example, four 0.1µF capacitors and two 1µF capacitors directly beneath the device or as close to the VDD pins as possible. The VDD pins on this device should be connected through a low-resistance path to the board VDD plane.
GND	A1, A2, A4, A6, A8, A10, A12, A14, A15, B2, B4, B6, B8, B10, B12, B14, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, D1, D2, D5, D7, D9, D11, D14, D15, E11, F1, F2, F5, F7, F9, F11, F14, F15, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, H2, H4, H6, H8, H10, H12, H14, J1, J2, J4, J6, J8, J10, J12, J14, J15	Power	None	Ground reference. The GND pins on this device should be connected through a low-resistance path to the board GND plane.

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). (1)

		MIN	MAX	UNIT
VDD_{ABSMAX}	Supply voltage (VDD)	-0.5	2.75	V
$VIO_{2.5V,ABSMAX}$	2.5V I/O voltage (LVCMOS, CMOS and Analog)	-0.5	2.75	V
$VIO_{3.3V,ABSMAX}$	Open Drain Voltage (SDA, SDC, INT_N) and LVCMOS Input Voltage (READ_EN_N)	-0.5	4.0	V
VIN_{ABSMAX}	Signal input voltage (RXnP, RXnN)	-0.5	2.75	V
$VOUT_{ABSMAX}$	Signal output voltage (TXnP, TXnN)	-0.5	2.75	V
TJ_{ABSMAX}	Junction temperature		150	°C
Tstg	Storage temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2,000V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1,000V may actually have higher performance.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
VDD	Supply voltage, VDD to GND. DC plus AC power should not exceed these limits.	2.375	2.625	V
NVDD	Supply noise, DC to < 50Hz, sinusoidal(2)		250	mVpp
NVDD	Supply noise, 50Hz to 10MHz, sinusoidal(2)		20	mVpp
NVDD	Supply noise, >10MHz, sinusoidal(2)		10	mVpp
$T_{rampVDD}$	VDD supply ramp time, from 0V to 2.375V	150		µs
T_J	Operating junction temperature	-40	110	°C
T_A	Operating ambient temperature	-40	85(1)	°C
$VIO_{2.5V}$	2.5V I/O voltage (LVCMOS, CMOS and Analog)	2.375	2.625	V
$VIO_{3.3V,INT_N}$	Open Drain LVCMOS I/O voltage (INT_N)		3.6	V
$VIO_{3.3V}$	Open Drain LVCMOS I/O voltage (SDA, SDC)	2.375	3.6	V

(1) Steps must be taken so that the operating junction temperature range and ambient temperature stay-in-lock range ($TEMP_{LOCK+}$, $TEMP_{LOCK-}$) are met. Refer to セクション 5.6 for more details concerning $TEMP_{LOCK+}$ and $TEMP_{LOCK-}$.
(2) Steps must be taken to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.

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5.4 Thermal Information

THERMAL METRIC(1)		CONDITIONS/ASSUMPTIONS(2)	DS280DF810 FC/CSP (ABV) 135 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4-Layer JEDEC Board	26.4	°C/W
		10-Layer 8-in x 6-in Board	9.3	
		20-Layer 8-in x 6-in Board	8.5	
		30-Layer 8-in x 6-in Board	8.2	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4-Layer JEDEC Board	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4-Layer JEDEC Board	9.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4-Layer JEDEC Board	0.1	°C/W
		10-Layer 8-in x 6-in Board	0.1	
		20-Layer 8-in x 6-in Board	0.1	
		30-Layer 8-in x 6-in Board	0.1	
Ψ_{JB}	Junction-to-board characterization parameter	4-Layer JEDEC Board	9.3	°C/W
		10-Layer 8-in x 6-in Board	5.0	
		20-Layer 8-in x 6-in Board	4.9	
		30-Layer 8-in x 6-in Board	4.6	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) No heat sink or airflow was assumed for these estimations. Depending on the application, a heat sink, faster airflow, or reduced ambient temperature (<85 C) may be required in order to meet the maximum junction temperature specification per the *セクション 5.3*.

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5.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rbaud	Input data rate	Full-rate	20.2		28.4	Gbps
		Half-rate	10.1		14.2	Gbps
		Quarter-rate	5.05		7.1	Gbps
t_{EEPROM}	EEPROM configuration load time	Single device reading its configuration from an EEPROM. Common channel configuration. This time scales with the number of devices reading from the same EEPROM.			15[2]	ms
t_{EEPROM}	EEPROM configuration load time	Single device reading its configuration from an EEPROM. Unique channel configuration. This time scales with the number of devices reading from the same EEPROM.			40[2]	ms
t_{POR}	Power-on reset assertion time	Internal power-on reset (PoR) stretch between stable power supply and de-assertion of internal PoR. The SMBus address is latched on the completion of the PoR stretch, and SMBus accesses are permitted.			50	ms
POWER SUPPLY						
$W_{channel}$	Power consumption per active channel	With CTLE, full DFE, Tx FIR, Driver, and Cross-point enabled. Idle power consumption is not included.		241	305	mW
		With CTLE, full DFE, Tx FIR, and Driver enabled; Cross-point disabled. Idle power consumption is not included.		233		mW
		With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; Cross-point and DFE taps 3-5 disabled. Idle power consumption is not included.		220		mW
		With CTLE, Tx FIR, Driver, and Cross-point enabled; DFE disabled. Idle power consumption is not included.		211	290	mW
		Assuming CDR acquiring lock with CTLE, full DFE, Tx FIR, Driver, and Cross-point enabled. Idle power consumption is not included.		365	430	mW
		Assuming CDR acquiring lock with CTLE, Tx FIR, Driver, and Cross-point enabled; DFE disabled. Idle power consumption is not included.		318	393	mW
		PRBS checker power consumption only[1]		220	302	mW
		PRBS generator power consumption only[1]		230	315	mW
W_{static_total}	Total idle power consumption	Idle or static mode, power supplied, no high-speed data present at inputs, all channels automatically powered down.		658	1050	mW

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5.5 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{total}	Active mode total device supply current consumption	With CTLE, full DFE, Tx FIR, Driver, and Cross-point enabled.		1036	1330	mA
		With CTLE, full DFE, Tx FIR, and Driver enabled; Cross-point disabled.		1010		mA
		With CTLE, partial DFE (taps 1-2 only), Tx FIR, and Driver enabled; Cross-point and DFE taps 3-5 disabled.		970		mA
		With CTLE, Tx FIR, Driver, and Cross-point enabled. DFE disabled.		940	1278	mA
I_{static_total}	Idle mode total device supply current consumption	Idle or static mode. Power supplied, no high-speed data present at inputs, all channels automatically powered down.		263	400	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Input high level voltage	2.5V LVCMOS pins	1.75		VDD	V
		3.3V LVCMOS pin (READ_EN_N)	1.75		3.6	V
V_{IL}	Input low level voltage	2.5V LVCMOS pins	GND		0.7	V
		3.3V LVCMOS pin (READ_EN_N)	GND		0.8	V
V_{TH}	High level (1) input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.95 * VDD		V
	Float level input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.67 * VDD		V
	10 K to GND input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.33 * VDD		V
	Low level (0) input voltage	4-level pins ADDR0, ADDR1, and EN_SMB		0.1		V
V_{OH}	High level output voltage	IOH = 4 mA	2			V
V_{OL}	Low level output voltage	IOL = -4 mA			0.4	V
I_{IH}	Input high leakage current	Vinput = VDD, Open drain pins			70	µA
I_{IH}	Input high leakage current	Vinput = VDD and CAL_CLK_IN pin			65	µA
I_{IH}	Input high leakage current	Vinput = VDD, ADDR[1:0] and EN_SMB pins			120	µA
I_{IH}	Input high leakage current	Vinput = VDD, READ_EN_N			75	µA
I_{IL}	Input low leakage current	Vinput = 0V, Open drain pins	-15			µA
I_{IL}	Input low leakage current	Vinput = 0V, CAL_CLK_IN pins	-45			µA
I_{IL}	Input low leakage current	Vinput = 0V, ADDR[1:0], READ_EN_N, and EN_SMB pins	-230			µA
RECEIVER INPUTS (RXnP, RXnN)						
V_{IDMax}	Maximum input differential voltage	For normal operation		1225		mVppd
RL_{SDD11}	Differential input return loss, SDD11	Between 50MHz and 3.69GHz		<-16		dB
RL_{SDD11}	Differential input return loss, SDD11	Between 3.69GHz and 12.9GHz		<-12		dB
RL_{SDC11}	Differential to common-mode input return loss, SDC11	Between 50MHz and 12.9GHz		<-23		dB
RL_{SCD11}	Differential to common-mode input return loss, SCD11	Between 50MHz and 12.9GHz		<-24		dB
RL_{SCC11}	Common-mode input return loss, SCC11	Between 150MHz and 10GHz		<-10		dB

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5.5 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{SCC11}	Common-mode input return loss, SCC11	Between 10GHz and 12.9GHz		<-10		dB
V_{SDAT}	AC signal detect assert (ON) threshold level	Minimum input peak-to-peak amplitude level at device pins required to assert signal detect. 25.78125Gbps with PRBS7 pattern and 20dB loss channel		196		mVppd
V_{SDDT}	AC signal detect de-assert (OFF) threshold level	Maximum input peak-to-peak amplitude level at device pins which causes signal detect to de-assert. 25.78125Gbps with PRBS7 pattern and 20dB loss channel		147		mVppd
TRANSMITTER OUTPUTS (TXnP, TXnN)						
VOD	Output differential voltage amplitude	Measured with c(0)=7 setting (Reg_0x3D[6:0]=0x07, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1 s followed by eight 0 s) at 25.78125Gbps with TXPn and TXNn terminated by 50Ω to GND.		525		mVppd
VOD	Output differential voltage amplitude	Measured with c(0)=31 setting (Reg_0x3D[6:0]=0x1F, Reg_0x3E[6:0]=0x40, REG_0x3F[6:0]=0x40). Differential measurement using an 8T pattern (eight 1 s followed by eight 0 s) at 25.78125Gbps with TXPn and TXNn terminated by 50Ω to GND.		1225		mVppd
VOD_{idle}	Differential output amplitude with TX disabled			< 11		mVppd
VOD_{res}	Output VOD resolution	Difference in VOD between two adjacent c(0) settings. Applies to VOD in the 525mVppd to 1225mVppd range [c(0)>4].		< 50		mVppd
$V_{cm\text{-}TX\text{-}AC}$	Common-mode AC output noise	With respect to signal ground. Measured with PRBS9 data pattern. Measured with a 33GHz (-3dB) low-pass filter.		6.5		mV, RMS
t_r, t_f	Output transition time	20%-to-80% rise time and 80%-to-20% fall time on a clock-like {11111 00000} data pattern at 25.78125Gbps. Measured for ~800mVppd output amplitude and no equalization: Reg_0x3D=+13, Reg_0x3E=0, REG_0x3F=0		17		ps
RL_{SDD22}	Differential output return loss, SDD22	Between 50MHz and 5GHz		<-12		dB
RL_{SDD22}	Differential output return loss, SDD22	Between 5GHz and 12.9GHz		<-9		dB
RL_{SCD22}	Common-mode to differential output return loss, SCD22	Between 50MHz and 12.9GHz		<-22		dB
RL_{SDC22}	Differential-to-common-mode output return loss, SDC22	Between 50MHz and 12.9GHz		<-22		dB
RL_{SCC22}	Common-mode output return loss, SCC22	Between 50MHz and 10GHz		<-9		dB

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5.5 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL_{SCC22}	Common-mode output return loss, SCC22	Between 10GHz and 12.9GHz		<-9		dB
SMBus ELECTRICAL CHARACTERISTICS (SLAVE MODE)						
V_{IH}	Input high level voltage	SDA and SDC	1.75		3.6	V
V_{IL}	Input low level voltage	SDA and SDC	GND		0.8	V
C_{IN}	Input pin capacitance			15		pF
V_{OL}	Low level output voltage	SDA or SDC, IOL = 1.25 mA			0.4	V
I_{IN}	Input current	SDA or SDC, VINPUT = VIN, VDD, GND	-15		15	µA
T_R	SDA rise time, read operation	Pull-up resistor = 1kΩ, Cb = 50pF		150		ns
T_F	SDA fall time, read operation	Pull-up resistor = 1kΩ, Cb = 50pF		4.5		ns

(1) For optimal performance, it is recommended to not enable more than two PRBS blocks (checker or generator) per channel quad.
(2) From low assertion of READ_EN_N to low assertion of ALL_DONE_N. Does not include Power-On Reset time.

5.6 Timing Requirements, Retimer Jitter Specifications

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
J_{TJ}	Output Total jitter (TJ)	Measured at 28.4Gbps to a probability level of 1E-15 with PRBS9 data pattern an evaluation board traces de-embedded.		0.24		UIpp @ 1E-12
J_{RJ}	Output Random Jitter (RJ)	Measured at 28.4Gbps to a probability level of 1E-15 with PRBS9 data pattern an evaluation board traces de-embedded		8		mUI RMS
J_{DCD}	Output Duty Cycle Distortion (DCD)	Measured at 28.4Gbps to a probability level of 1E-15 with PRBS9 data pattern an evaluation board traces de-embedded		15		mUIpp
J_{TJ}	Output Total jitter (TJ)	Measured at 25.78125Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded.		0.17		UIpp @ 1E-12
J_{RJ}	Output Random Jitter (RJ)	Measured at 25.78125Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded		6		mUI RMS
J_{DCD}	Output Duty Cycle Distortion (DCD)	Measured at 25.78125Gbps to a probability level of 1E-12 with PRBS11 data pattern an evaluation board traces de-embedded		4		mUIpp
J_{PEAK}	Jitter peaking	Measured at 10.3125Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 6MHz.		0.8		dB
J_{PEAK}	Jitter peaking	Measured at 25.78125Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 17MHz.		0.4		dB
J_{PEAK}	Jitter peaking	Measured at 28.4Gbps with PRBS7 data pattern. Peaking frequency in the range of 1 to 17MHz.		0.4		dB

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5.6 Timing Requirements, Retimer Jitter Specifications (続き)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BWPLL	PLL bandwidth	Data rate of 10.3125Gbps with PRBS7 pattern		5		MHz
BWPLL	PLL bandwidth	Data rate of 25.78125Gbps with PRBS7 pattern		5.5		MHz
BWPLL	PLL bandwidth	Data rate of 28.4Gbps with PRBS7 pattern		5		MHz
J_{TOL}	Input jitter tolerance	Measured at 28.4Gbps with SJ frequency > 10MHz, 29dB input channel loss, PRBS31 data pattern, 800mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		0.32		UIpp
J_{TOL}	Input jitter tolerance	Measured at 25.78125Gbps with SJ frequency = 190 KHz, 30dB input channel loss, PRBS31 data pattern, 800mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		9		UIpp
J_{TOL}	Input jitter tolerance	Measured at 25.78125Gbps with SJ frequency = 940 KHz, 30dB input channel loss, PRBS31 data pattern, 800mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		1		UIpp
J_{TOL}	Input jitter tolerance	Measured at 25.78125Gbps with SJ frequency > 10MHz, 32dB input channel loss, PRBS31 data pattern, 800mVppd launch amplitude, and 0.078 UIpp total uncorrelated output jitter in addition to the applied SJ. BER < 1E-12.		0.38		UIpp
$TEMP_{LOCK-}$	CDR stay-in-lock ambient temperature range, negative ramp. Maximum temperature change below initial CDR lock acquisition temperature.	85 °C starting ambient temperature, ramp rate -3 °C/minute, 1.7 liters/sec airflow, 12 layer PCB.		115		°C
$TEMP_{LOCK+}$	CDR stay-in-lock ambient temperature range, positive ramp. Maximum temperature change above initial CDR lock acquisition temperature.	-40 °C starting ambient temperature, ramp rate +3 °C/minute, 1.7 liters/sec airflow, 12 layer PCB.		125		°C

5.7 Timing Requirements, Retimer Specifications

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	Input-to-output latency (propagation delay) through a channel	No cross-point; CDR enabled and locked.		3.5UI + 125ps		ps
t_D	Input-to-output latency (propagation delay) through a channel	Cross-point enabled; CDR enabled and locked.		3.5UI + 145ps		ps
t_D	Input-to-output latency (propagation delay) through a channel	No cross-point; CDR in raw mode. 25.78125Gbps data rate.		< 145		ps

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5.7 Timing Requirements, Retimer Specifications (続き)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SK}	Channel-to-channel inter-pair skew	Latency difference between channels at full-rate. 25.78125Gbps data rate		< 30		ps
t_{lock}	CDR lock acquisition time	Measured at 25.78125Gbps, Adapt Mode = 1 (Reg_0x31[6:5]=0x1), EOM timer = 0x5 (Reg_0x2A[7:4]=0x5).		< 100		ms
t_{lock}	CDR lock acquisition time	Measured at 10.3125Gbps, Adapt Mode = 1 (Reg_0x31[6:5]=0x1), EOM timer = 0x5 (Reg_0x2A[7:4]=0x5).		< 100		ms

5.8 Timing Requirements, Recommended Calibration Clock Specifications

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK_f	Calibration clock frequency			25		MHz
CLK_{PPM}	Calibration clock PPM tolerance		-100		100	PPM
CLK_{IDC}	Recommended/tolerable input duty cycle		40%	50%	60%	
CLK_{ODC}	Intrinsic calibration clock duty cycle distortion	Intrinsic duty cycle distortion of chip calibration clock output at the CAL_CLK_OUT pin, assuming 50% duty cycle on CAL_CLK_IN pin.	45%		55%	
CLKnum	Number of devices which can be cascaded from CAL_CLK_OUT to CAL_CLK_IN	Assumes worst-case 60% and 40% input duty cycle on the first device. CAL_CLK_OUT from first device connects to CAL_CLK_IN of second device, and so on until the last device.		20		N/A

5.9 Recommended SMBus Switching Characteristics (Target Mode)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SDC}	SDC clock frequency		10	100	400	kHz
t_{HD-DAT}	Data hold time			0.75		ns
t_{SU-DAT}	Data setup time			100		ns

5.10 Recommended SMBus Switching Characteristics (Controller Mode)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SDC}	SDC clock frequency		260	303	346	kHz
T_{LOW}	SDC low period		1.66	1.90	2.21	µs
T_{HIGH}	SDC high period		1.22	1.40	1.63	µs
T_{HD-STA}	Hold time start operation			0.6		µs
T_{SU-STA}	Setup time start operation			0.6		µs
T_{HD-DAT}	Data hold time			0.6		µs
T_{SD-DAT}	Data setup time			0.1		µs
T_{SU-STO}	Stop condition setup time			0.6		µs

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Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{BUF}	Bus free time between Stop-Start			1.3		µs
T_R	SDC rise time	Pull-up resistor = 1kΩ		300		ns
T_F	SDC fall time	Pull-up resistor = 1kΩ		300		ns

5.11 Typical Characteristics

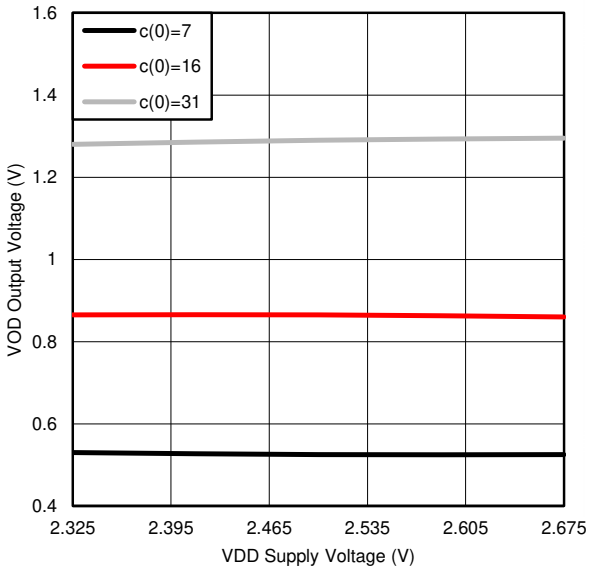

図 5-1. Typical VOD versus Supply Voltage

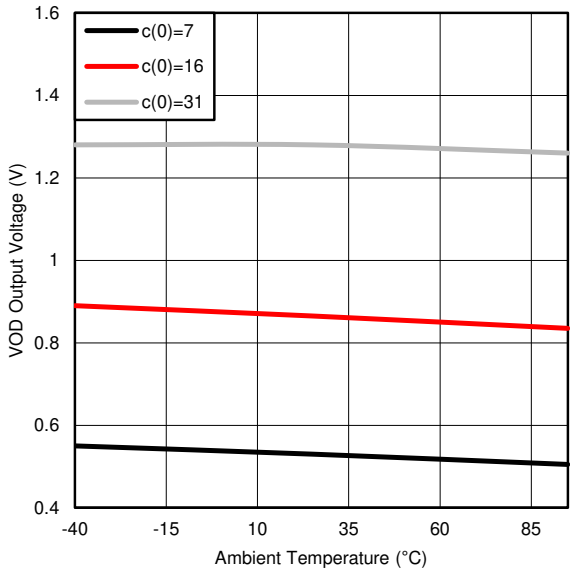

図 5-2. Typical VOD versus Temperature

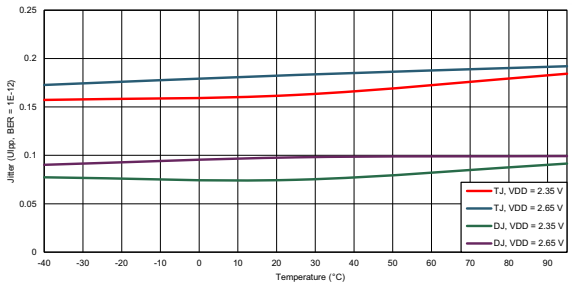

図 5-3. Typical VOD versus FIR Main-Cursor

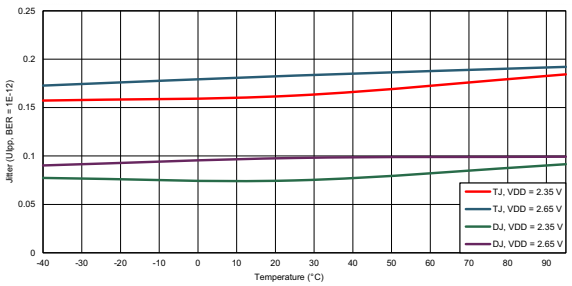

図 5-4. Typical Output Jitter versus Temperature at 25.78125Gbps

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6 Detailed Description

6.1 Overview

The DS280DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. Each of the eight channels operates independently. Each channel includes a continuous-time linear equalizer (CTLE) and a Decision Feedback Equalizer (DFE), which together compensate for the presence of a dispersive transmission channel between the source transmitter and the DS280DF810 receiver. The CTLE and DFE are self-adaptive.

Each channel includes an independent voltage-controlled oscillator (VCO) and phase-locked loop (PLL) which produce a clean clock that is frequency-locked to the clock embedded in the input data stream. The high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially-reduced jitter. This clean clock is used to re-time the incoming data, removing high-frequency jitter from the data stream and reproducing the data on the output with significantly-reduced jitter.

Each channel of the DS280DF810 features an output driver with adjustable differential output voltage and output equalization in the form of a three-tap finite impulse response (FIR) filter. The output FIR compensates for dispersion in the transmission channel at the output of the DS280DF810.

All transmit and receive channels on the DS280DF810 are AC-coupled with physical AC-coupling capacitors (220nF +/- 20%) on the package substrate. This allows for common mode voltage compatibility with all link partners and eliminates the need for AC coupling capacitors on the system PCB, thereby saving cost and greatly reducing PCB routing complexity.

Between each group of two adjacent channels (for example, between channels 0–1, 2–3, 4–5, and 6–7) is a full 2x2 cross-point switch. This allows multiplexing and de-multiplexing and fanout applications for fail-over redundancy, as well as cross-over applications to aid PCB routing.

Each channel also includes diagnostic features such as a Pseudo Random Bit Sequence (PRBS) pattern generator and checker, as well as a non-destructive eye opening monitor (EOM). The EOM can be used to plot the post-equalized eye at the input to the decision slicer or simply to read the horizontal eye opening (HEO) and vertical eye opening (VEO).

The DS280DF810 is configurable through a single SMBus port. The DS280DF810 can also act as an SMBus controller to configure itself from an EEPROM. Up to sixteen DS280DF810 devices can share a single SMBus.

The sections which follow describe the functionality of various circuits and features within the DS280DF810. For more information about how to program or operate these features, consult the DS280DF810 Programming Guide.

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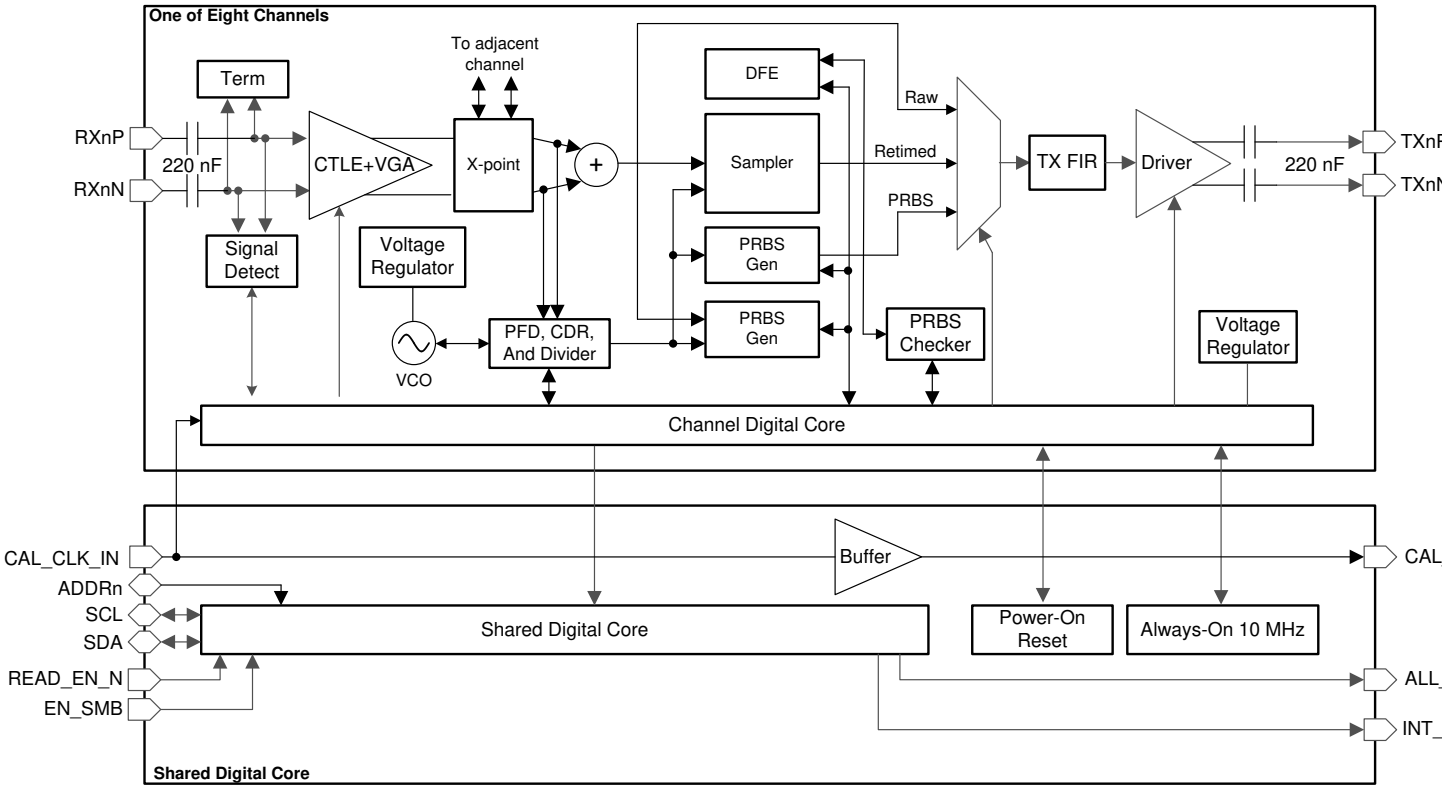
6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Device Data Path Operation

The DS280DF810 data path consists of several key blocks as shown in the functional block diagram. These key circuits are:

- セクション 6.3.1.1
- セクション 6.3.1.2
- セクション 6.3.1.3
- セクション 6.3.1.4
- セクション 6.3.1.5
- セクション 6.3.1.6
- セクション 6.3.1.7
- セクション 6.3.1.8
- セクション 6.3.1.9
- セクション 6.3.1.9

6.3.1.1 AC-Coupled Receiver and Transmitter

The differential receiver for each DS280DF810 channel contains on-package AC coupling capacitors. The differential transmitter for each DS280DF810 channel also implement on-package AC coupling capacitors. The AC coupling capacitors have a value of 220nF +/- 20%.

6.3.1.2 Signal Detect

The DS280DF810 receiver contains a signal detect circuit. The signal detect circuit monitors the energy level on the receiver inputs and powers on or off the rest of the high-speed data path if a signal is detected or not. By default, each channel allows the signal detect circuit to automatically power on or off the rest of the high speed data path depending on the presence of an input signal. The signal detect block can be manually controlled in the SMBus channel registers. This can be useful if it is desired to manually force channels to be disabled. For information on how to manually operate the signal detect circuit refer to the DS280DF810 Programming Guide.

6.3.1.3 Continuous Time Linear Equalizer (CTLE)

The CTLE in the DS280DF810 is a fully-adaptive equalizer. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. The FOM calculation is based upon the horizontal eye opening (HEO) and vertical eye opening (VEO). Once the CDR locks and the CTLE adapts, the CTLE boost level is frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE can be re-adapted by resetting the CDR.

The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 16 of these boost combinations. These 16 boost combinations comprise the EQ Table in the channel registers. See channel registers 0x40 through 0x4F. This EQ Table can be reprogrammed to support up to 16 of the 256 boost settings.

The boost levels can be set between 8dB and 25dB (at 14GHz).

6.3.1.4 Variable Gain Amplifier (VGA)

The DS280DF810 receiver implements a VGA. The VGA assists in the recovery of extremely small signals, working in conjunction with the CTLE to equalize and scale amplitude. The VGA has 1-bit control via Register 0x8E[0], and the VGA is enabled by default. In addition to the VGA, the CTLE implements its own gain control via register 0x13[5] to adjust the DC amplitude similar to the VGA. For more information on how to configure the VGA refer to the DS280DF810 Programming Guide.

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6.3.1.5 2x2 Cross-Point Switch

Between each group of two adjacent channels (for example, between channels 0–1, 2–3, 4–5, and 6–7) is a full 2×2 cross-point switch. The cross-point can be configured through SMBus registers to operate as follows:

- Straigh-thru mode
- Multiplex two inputs to one output
- Fanout one input to two outputs
- Cross two inputs to two outputs

図 6-1 shows the four 2x2 cross-points available in the DS280DF810, and 図 6-2 shows how each cross-point can be configured for straight-thru, multiplex, de-multiplex, or cross-over applications. Refer to the DS280DF810 Programming Guide for details on how to program the cross-point through SMBus registers.

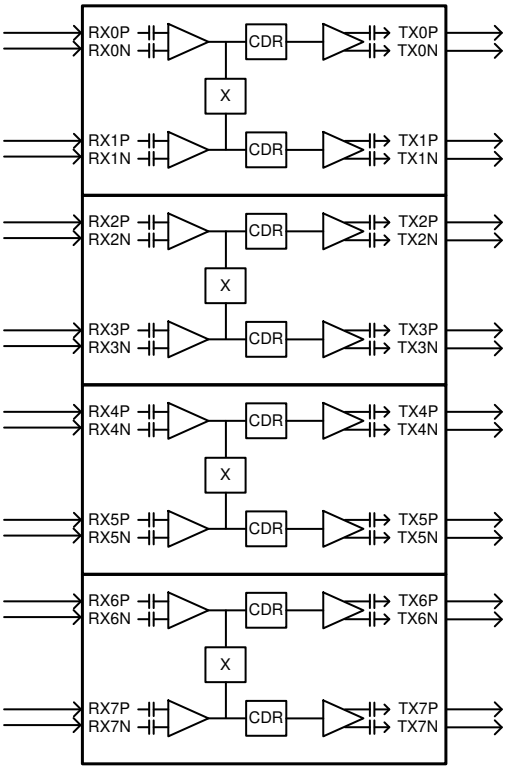

図 6-1. Block diagram showing all four 2x2 cross-points in the DS280DF810

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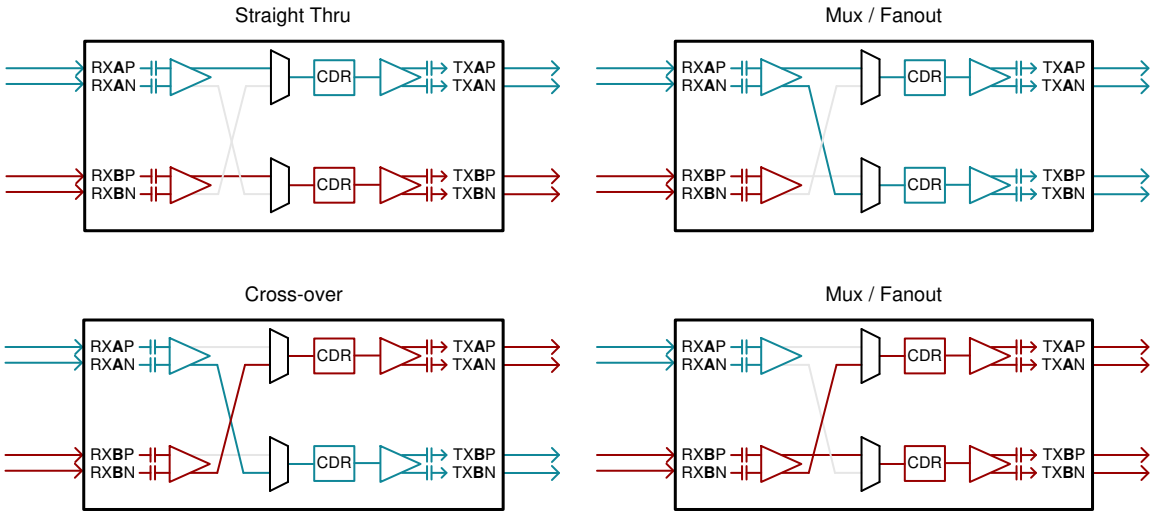

図 6-2. Signal distribution options available in each 2x2 cross-point (channel A can be 0, 2, 4, or 6; channel B can be 1, 3, 5, or 7)

6.3.1.6 Decision Feedback Equalizer (DFE)

A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. Once the DFE has been enabled it can be configured to adapt only during lock acquisition or to adapt continuously. The DFE can also be manually configured to specified tap polarities and tap weights. However, when the DFE is configured manually the DFE auto-adaption should be disabled. For many applications with lower insertion loss (for example,. < 30dB) lower crosstalk, or lower reflections, part or all of the DFE can be disabled to reduce power consumption. The DFE can either be fully enabled (taps 1-5), partially enabled (taps 1-2 only), or fully disabled (no taps).

The DFE taps are all feedback taps with 1 UI spacing. Each tap has a specified boost weight range and polarity bit.

表 6-1. DFE Tap Weights

DFE PARAMETER	DECIMAL (REGISTER VALUE)	VALUE (mV) (TYP)
Tap 1 Weight Range	0 - 31	0 – 217
Tap 2-5 Weight Range	0 - 15	0 – 105
Tap Weight Step Size	NA	7
Polarity	0: (+) positive; feedback value creates a low-pass filter response, thus providing attenuation to correct for negative-sign post-cursor ISI 1: (-) negative; Feedback value creates a high-pass filter response, thus providing boost to correct for positive-sign post-cursor ISI.	

6.3.1.7 Clock and Data Recovery (CDR)

The CDR consists of a Phase Locked Loop (PLL), PPM counter, and Input and Output Data Multiplexers (mux) allowing for retimed data, un-retimed data, PRBS generator and output muted modes.

By default, the equalized data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver together with the recovered clock which has been cleaned of any high-frequency jitter outside the bandwidth of the CDR clock recovery loop. The bandwidth of the CDR defaults to 5.5MHz (typical) in full-rate (divide-by-1) mode and 5.3MHz (typical) in sub-rate mode. The CDR bandwidth is adjustable. Refer to the DS280DF810 Programming Guide for more information on adjusting the CDR bandwidth. Users can configure the CDR data to route the recovered clock and data to the PRBS checker. Users

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also have the option of configuring the output of the CDR to send raw non-retimed data, or data from the pattern generator.

The CDR requires the following in order to be properly configured:

- 25MHz calibration clock to run the PPM counter (CAL_CLK_IN).
- Expected data rates must be programmed into the CDR either through the rate table or entered manually with the corrected divider settings. Refer to the Programming Guide for more information on configuring the CDR for different data rates.

6.3.1.8 Calibration Clock

The calibration clock is not part of the CDR's PLL and thus is not used for clock and data recovery. The calibration clock is connected only to the PPM counter for each CDR. The PPM counter constrains the allowable lock ranges of the CDR according to the programmed values in the rate table or the manually entered data rates. The host should provide an input calibration clock signal of 25MHz frequency. Because this clock is not used for clock and data recovery, there are no stringent jitter requirements placed on this 25MHz calibration clock.

6.3.1.9 Differential Driver with FIR Filter

The DS280DF810 output driver has a three-tap finite impulse response (FIR) filter which allows for pre- and post-cursor equalization to compensate for a wide variety of output channel media. The filter consists of a weighted sum of three consecutive retimed bits as shown in the following diagram. C[0] can take on values in the range [-31, +31]. C[-1] and C[+1] can take on values in the range [-15, 15].

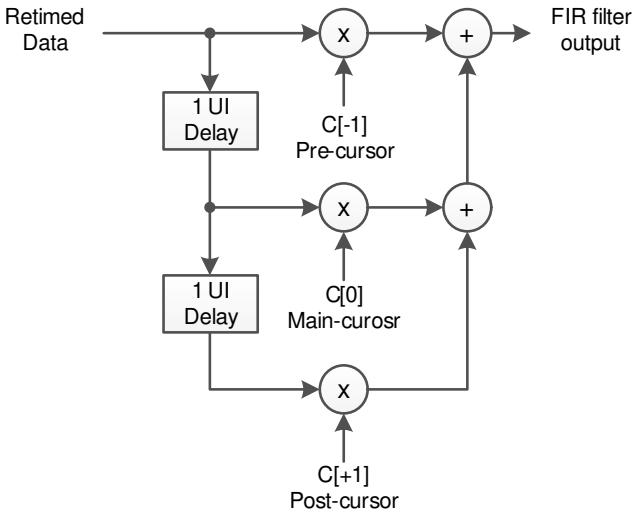

図 6-3. FIR filter functional model

When utilizing the FIR filter, it is important to abide by the following general rules:

- |C[-1]| + |C[0]| + |C[+1]| ≤ 31; the FIR tap coefficients absolute sum must be less or equal to 31).
- sgn(C[-1]) = sgn(C[+1]) ≠ sgn(C[0]), for high-pass filter effect; the sign for the pre-cursor or post-cursor tap must be different from main-cursor tap to realize boost effect.
- sgn(C[-1]) = sgn(C[+1]) = sgn(C[0]), for low-pass filter effect; the sign for the pre-cursor or post-cursor tap must be equal to the main-cursor tap to realize attenuation effect.

The FIR filter is used to pre-distort the transmitted waveform in order to compensate for frequency-dependant loss in the output channel. The most common way of pre-distorting the signal is to accentuate the transitions and de-emphasize the non-transitions. The bit before a transition is accentuated via the pre-cursor tap, and the bit after the transition is accentuated via the post-cursor tap. The figures below give a conceptual illustration of how the FIR filter affects the output waveform. The following characteristics can be derived from the example waveforms.

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- $VOD_{pk-pk}=v_7 - v_8$
- $VOD_{low-frequency} = v_2 - v_5$
- $Rpre_{dB} = 20 * \log_{10} (v_3/v_2)$
- $Rpst_{dB} = 20 * \log_{10} (v_1/v_2)$

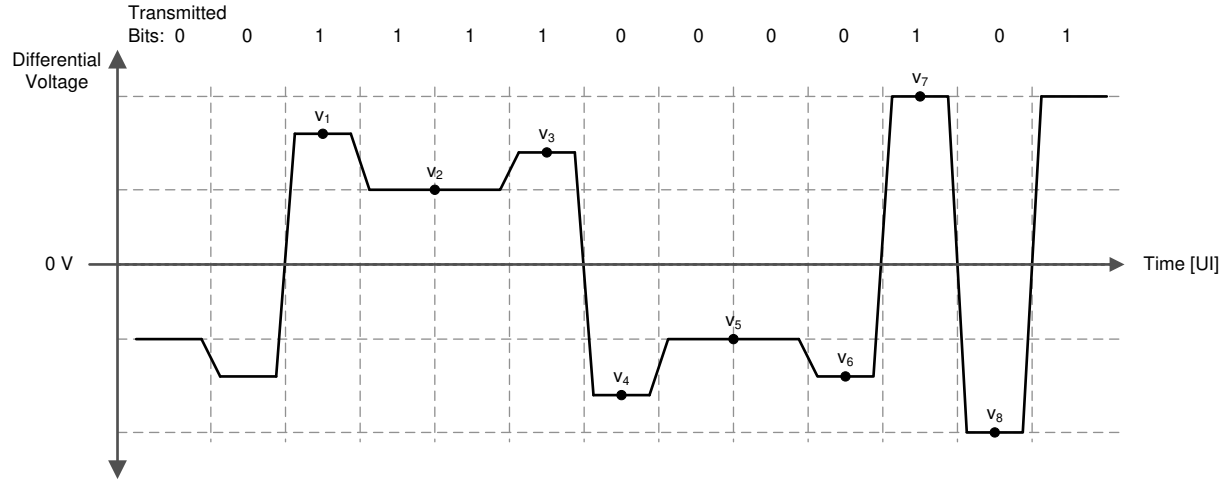

図 6-4. Conceptual FIR Waveform With Post-Cursor Only

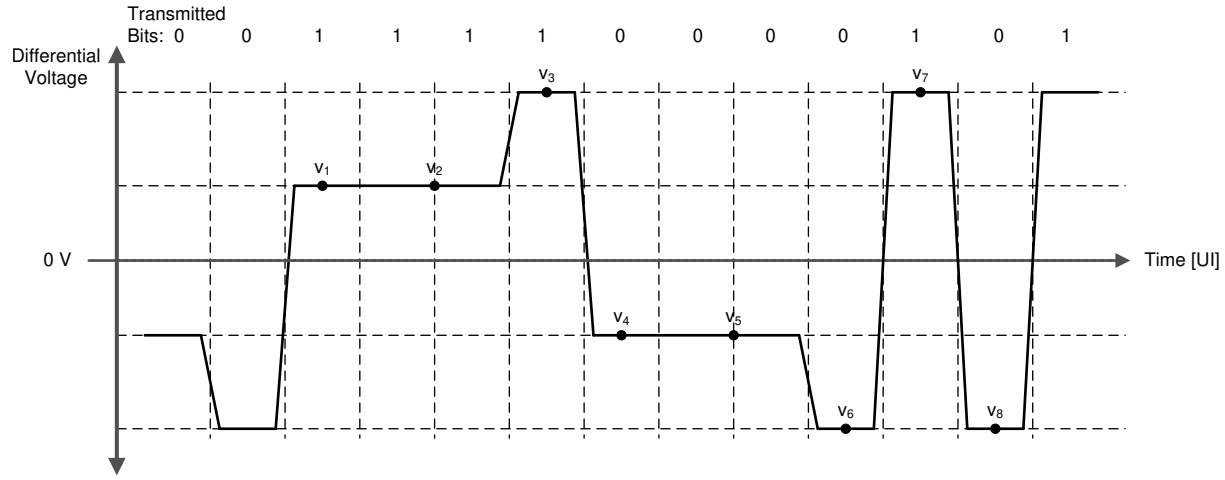

図 6-5. Conceptual FIR Waveform With Pre-Cursor Only

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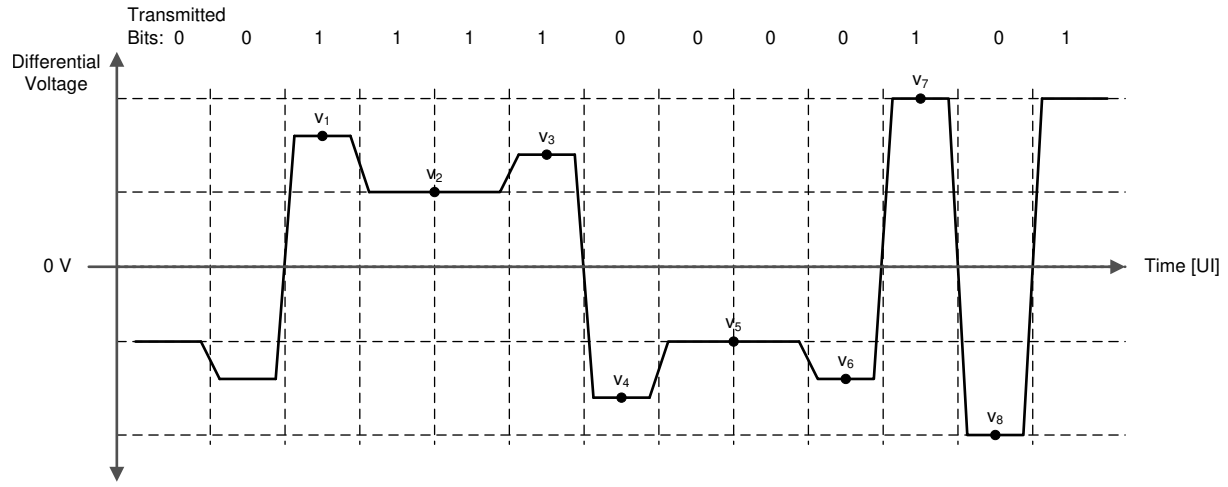

図 6-6. Conceptual FIR Waveform With Both Pre-Cursor and Post-Cursor

6.3.1.9.1 Setting the Output V_{OD}, Pre-Cursor, and Post-Cursor Equalization

The output differential voltage (V_{OD}) of the driver is controlled by manipulating the FIR tap settings. The main cursor tap is the primary knob for amplitude adjustment. The pre and post cursor FIR tap settings can then be adjusted to provide equalization. To maintain a constant peak-to-peak VOD, the user should adjust the main cursor tap value relative to the pre tap or post tap changes so as to maintain a constant absolute sum of the FIR tap values. The table below shows various settings for V_{OD} settings ranging from 205 mVpp to 1225 mVpp (typical). Note that the output peak-to-peak amplitude is a function of the sum of the absolute values of the taps, whereas the low-frequency amplitude is purely a function of the main-cursor value.

表 6-2. Typical VOD and FIR Values

FIR SETTINGS			PEAK-TO PEAK VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSOR: REG_0x3E[6:0]	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	0	0	0.205	NA	NA
0	+1	0	0.260	NA	NA
0	+2	0	0.305	NA	NA
0	+3	0	0.355	NA	NA
0	+4	0	0.395	NA	NA
0	+5	0	0.440	NA	NA
0	+6	0	0.490	NA	NA
0	+7	0	0.525	NA	NA
0	+8	0	0.565	NA	NA
0	+9	0	0.610	NA	NA
0	+10	0	0.650	NA	NA
0	+11	0	0.685	NA	NA
0	+12	0	0.720	NA	NA
0	+13	0	0.760	NA	NA
0	+14	0	0.790	NA	NA
0	+15	0	0.825	NA	NA
0	+16	0	0.860	NA	NA
0	+17	0	0.890	NA	NA
0	+18	0	0.925	NA	NA
0	+19	0	0.960	NA	NA

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表 6-2. Typical VOD and FIR Values (続き)

FIR SETTINGS			PEAK-TO PEAK VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSOR: REG_0x3E[6:0]	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
0	+20	0	0.985	NA	NA
0	+21	0	1.010	NA	NA
0	+22	0	1.040	NA	NA
0	+23	0	1.075	NA	NA
0	+24	0	1.095	NA	NA
0	+25	0	1.125	NA	NA
0	+26	0	1.150	NA	NA
0	+27	0	1.165	NA	NA
0	+28	0	1.190	NA	NA
0	+29	0	1.205	NA	NA
0	+30	0	1.220	NA	NA
0	+31	0	1.225	NA	NA
0	+18	-1	0.960	NA	2.1
0	+17	-2	0.960	NA	2.5
0	+16	-3	0.960	NA	3.1
0	+15	-4	0.960	NA	3.8
0	+14	-5	0.960	NA	4.7
0	+13	-6	0.960	NA	5.8
0	+12	-7	0.960	NA	7.2
0	+11	-8	0.960	NA	9.0
0	+10	-9	0.960	NA	11.6
-1	18	0	0.960	1.0	NA
-2	17	0	0.960	1.6	NA
-3	16	0	0.960	2.4	NA
-4	15	0	0.960	3.3	NA
0	26	-1	1.165	NA	1.1
0	25	-2	1.165	NA	1.3
0	24	-3	1.165	NA	1.8
0	23	-4	1.165	NA	2.2
0	22	-5	1.165	NA	2.7
0	21	-6	1.165	NA	3.3
0	20	-7	1.165	NA	3.9
0	19	-8	1.165	NA	4.7
0	18	-9	1.165	NA	5.7
0	17	-10	1.165	NA	6.9
0	16	-11	1.165	NA	8.4
0	15	-12	1.165	NA	10.1
-1	26	0	1.165	0.7	NA
-2	25	0	1.165	1.2	NA
-3	24	0	1.165	1.5	NA
-4	23	0	1.165	2.0	NA
-5	22	0	1.165	2.6	NA
-6	21	0	1.165	3.2	NA

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表 6-2. Typical VOD and FIR Values (続き)

FIR SETTINGS			PEAK-TO PEAK VOD(V)	RPRE(dB)	RPST(dB)
PRE-CURSOR: REG_0x3E[6:0]	MAIN-CURSOR: REG_0x3D[6:0]	POST-CURSOR: REG_0x3F[6:0]			
-7	20	0	1.165	4.0	NA

The recommended pre-cursor and post-cursor settings for a given channel will depend on the channel characteristics (mainly insertion loss) as well as the equalization capabilities of the downstream receiver. The DS280DF810 receiver, with its highly-capable CTLE and DFE, does not require a significant amount of pre-cursor or post-cursor. The figures below give general recommendations for pre- and post-cursor for different channel loss conditions. The insertion loss (IL) in these plots refers to the total loss between the link partner transmitter and the DS280DF810 receiver.

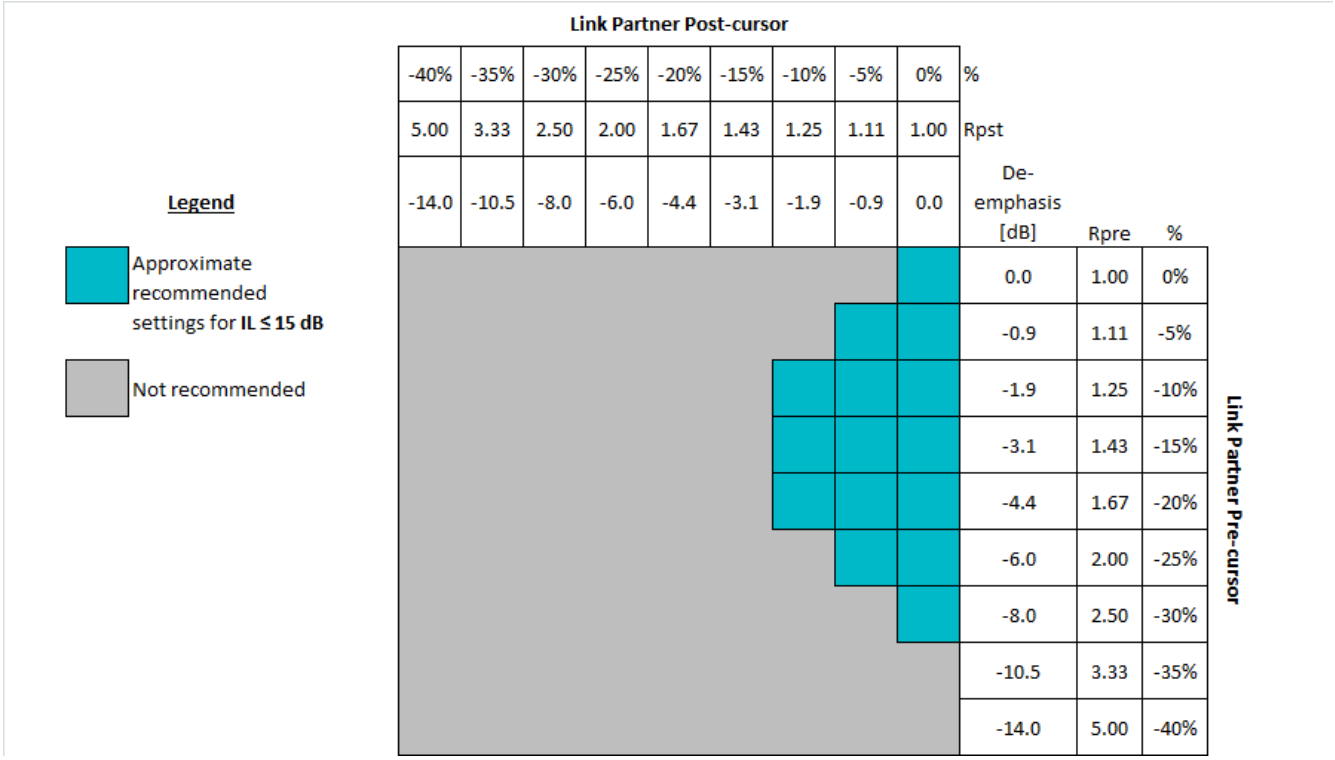

図 6-7. Guideline for Link partner FIR Settings When IL ≤ 15dB

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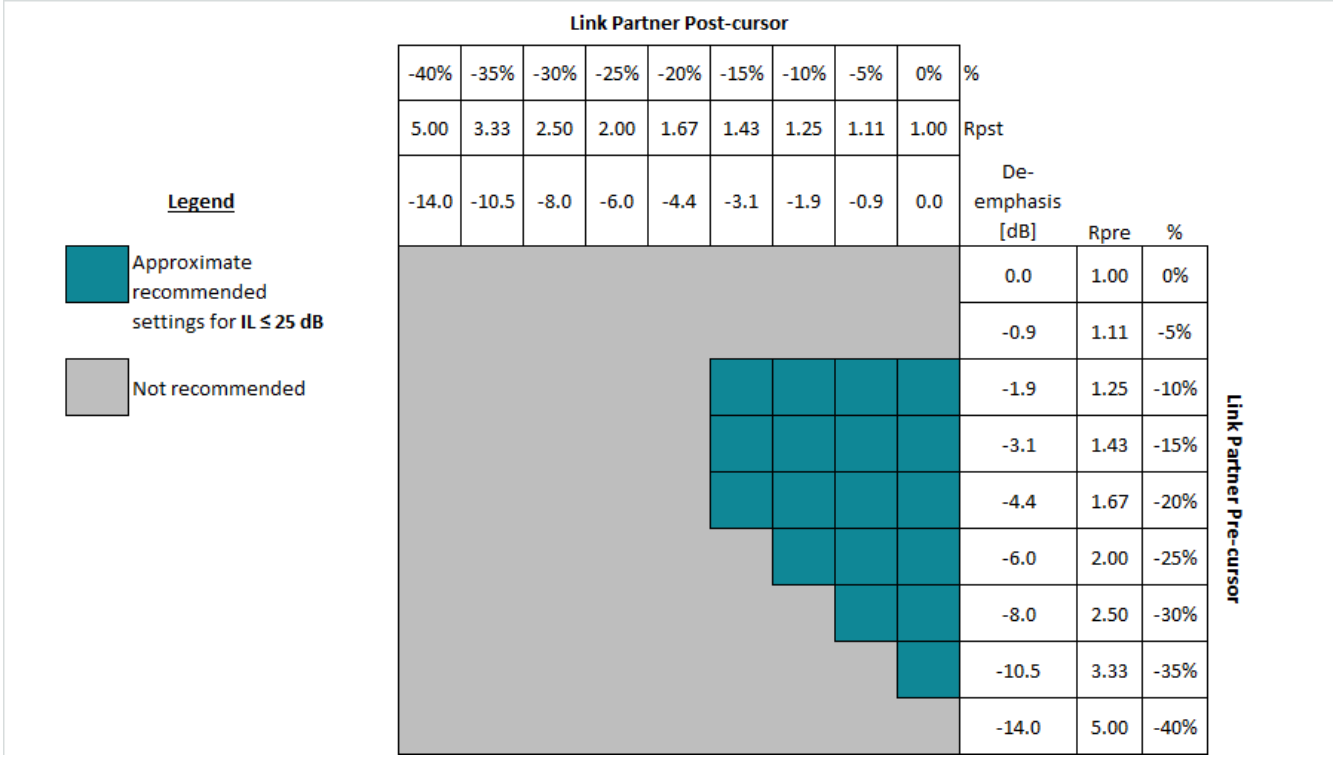

図 6-8. Guideline for Link partner FIR Settings When IL ≤ 25dB

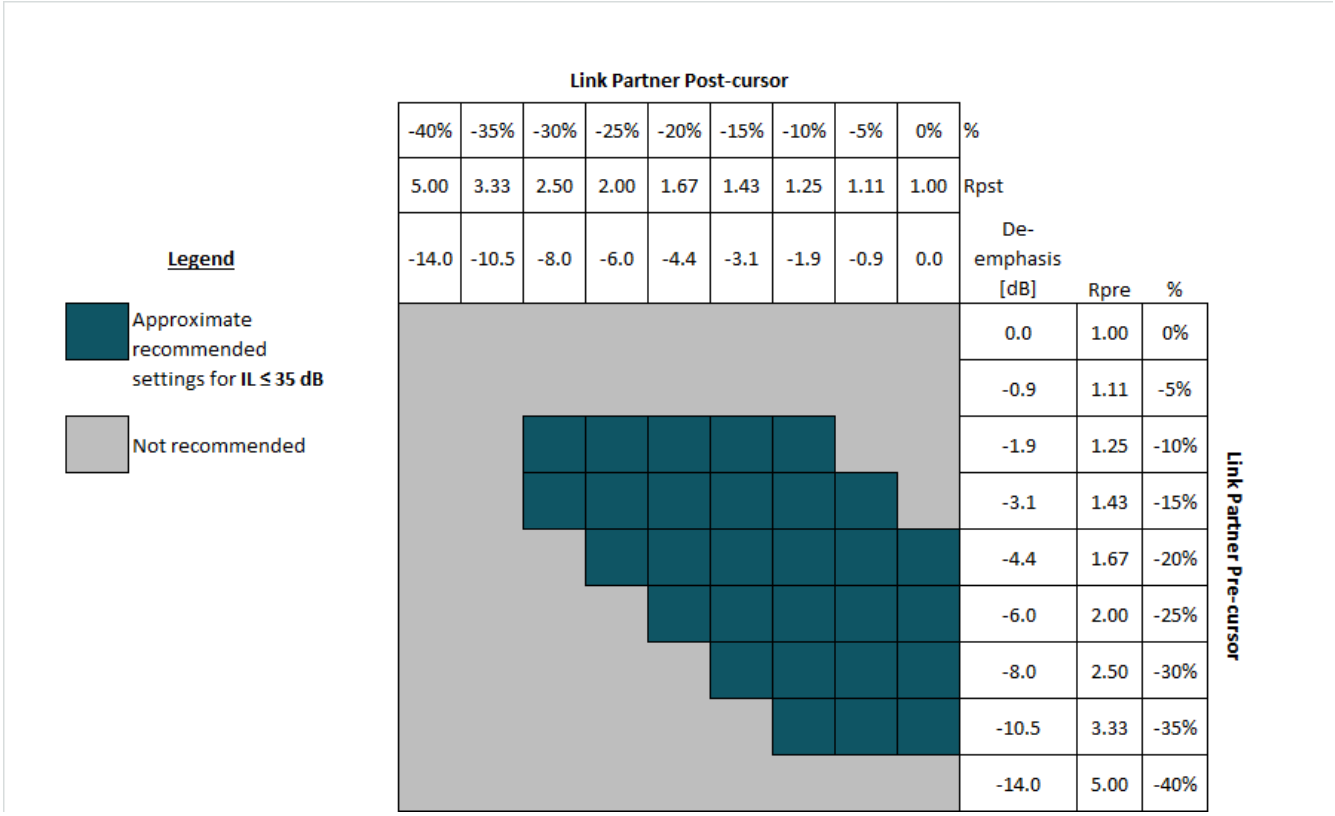

図 6-9. Guideline for Link partner FIR Settings When IL ≤ 35dB

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6.3.1.9.2 Output Driver Polarity Inversion

In some applications, it may be necessary to invert the polarity of the data transmitted from the retimer. To invert the polarity of the data, read back the FIR polarity settings for the pre-cursor, main-cursor, and post-cursor taps and then invert all of these polarities. Refer to the DS280DF810 Programming Guide for more details.

6.3.2 Debug Features

The DS280DF810 has multiple features to aid diagnostics, board manufacturing, and system debug. These key features are:

- セクション 6.3.2.1
- セクション 6.3.2.2
- セクション 6.3.2.3
- セクション 6.3.2.4

6.3.2.1 Pattern Generator

Each channel in the DS280DF810 can be configured to generate a 16-bit user-defined data pattern or a pseudo random bit sequence (PRBS). The user defined pattern can also be set to automatically invert every other 16-bit symbol for DC balancing purposes. The DS280DF810 pattern generator supports the following PRBS sequences:

- PRBS – 2^7 - 1
- PRBS – 2^9 - 1
- PRBS – 2^{11} - 1
- PRBS – 2^{15} - 1
- PRBS – 2^{23} - 1
- PRBS – 2^{31} - 1
- PRBS – 2^{58} - 1
- PRBS – 2^{63} - 1

6.3.2.2 Pattern Checker

The pattern checker can be manually set to look for specific PRBS sequences and polarities or it can be set to automatically detect the incoming pattern and polarity. The PRBS checker supports the same set of PRBS patterns as the PRBS generator.

The pattern checker consists of an 11-bit error counter. The pattern checker uses 32- bit words, but every bit in the word is checked for error, so the error count represents the count of single bit errors.

In order to read out the bit and error counters, the pattern checker must first be frozen. Continuous operation with simultaneous read out of the bit and error counters is not supported in this implementation. Once the bit and error counter is read, they can be not frozen to continue counting.

6.3.2.3 Eye Opening Monitor

The DS280DF810's Eye Opening Monitor (EOM) measures the internal data eye at the input of the decision slicer and can be used for 2 functions:

1. Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) measurement
2. Full Eye Diagram Capture

The HEO measurement is made at the 0V crossing and is read in channel register 0x27. The VEO measurement is made at the 0.5 UI mark and is read in channel register 0x28. The HEO and VEO registers can be read from channel registers 0x27 and 0x28 at any time while the CDR is locked. The following equations are used to convert the contents of channel registers 0x27 and 0x28 into their appropriate units:

- HEO [UI] = Reg_0x27 ÷ 32
- VEO [mV] = Reg_0x28 x 3.125

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A full eye diagram capture can be performed when the CDR is locked. The eye diagram is constructed within a 64 x 64 array, where each cell in the matrix consists of an 16-bit word representing the total number of hits recorded at that particular phase and voltage offset. Users can manually adjust the vertical scaling of the EOM or allow the state machine to control the scaling which is the default option. The horizontal scaling controlled by the state machine and is always directly proportional to the data rate.

When a full eye diagram plot is captured, the retimer will shift out four 16-bit words of junk data that should be discarded followed by 4096 16-bit words that make up the 64 × 64 eye plot. The first actual word of the eye plot from the retimer is for (X, Y) position (0,0), which is the earliest position in time and the most negative position in voltage. Each time the eye plot data is read out the voltage position is incremented. Once the voltage position has incremented to position 63 (the most positive voltage), the next read will cause the voltage position to reset to 0 (the most negative voltage) and the phase position to increment. This process will continue until the entire 64 × 64 matrix is read out. 図 6-10 below shows the EOM read out sequence overlaid on top of a simple eye opening plot. In this plot any hits are shown in green. This type of plot is helpful for quickly visualizing the HEO and VEO. Users can apply different algorithms to the output data to plot density or color gradients to the output data.

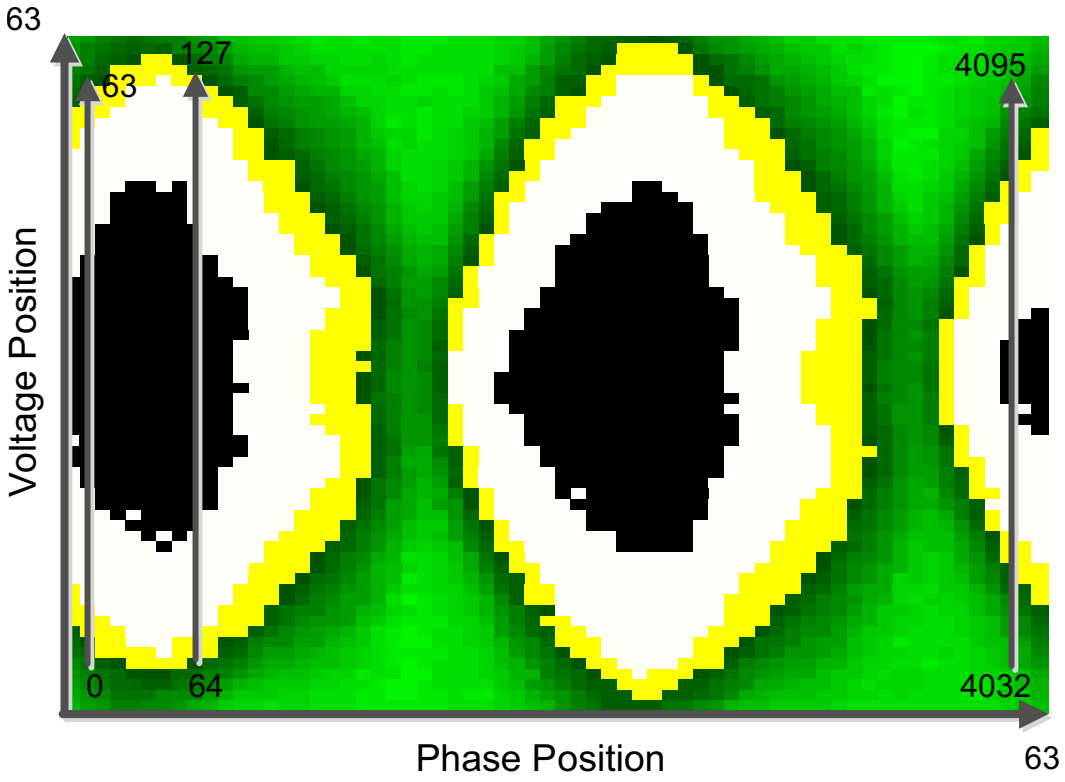

図 6-10. EOM Full Eye Capture Readout

To manually control the EOM vertical range, remove scaling control from the state machine then select the desired range:

Channel Reg 0x2C[6] → 0 (see 表 6-3).

表 6-3. Eye Opening Monitor Vertical Range Settings

CH REG 0x11[7:6] VALUE	EOM VERTICAL RANGE [mV]
2'b00	±100
2'b01	±200
2'b10	±300

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表 6-3. Eye Opening Monitor Vertical Range Settings (続き)

CH REG 0x11[7:6] VALUE	EOM VERTICAL RANGE [mV]
2'b11	±400

The EOM operates as an under-sampled circuit. This allows the EOM to be useful in identifying over equalization, ringing and other gross signal conditioning issues. However, the EOM cannot be correlated to a bit error rate.

The EOM can be accessed in two ways to read out the entire eye plot:

- Multi-byte reads can be used such that data is repeatedly latched out from channel register 0x25.
- With single byte reads, the MSB are located in register 0x25 and the LSB are located in register 0x26. In this mode, the device must be addressed each time a new byte is read.

To perform a full eye capture with the EOM, follow these steps below within the desired channel register set:

表 6-4. Eye Opening Monitor Full Eye Capture Instructions

STEP	REGISTER [bits]	OPERATION	VALUE	DESCRIPTION
1	0x67[5]	Write	0	Disable lock EOM lock monitoring
2	0x2C[6]	Write	0	Set the desired EOM vertical range
	0x11[7:6]	Write	2'b--	
3	0x11[5]	Write	0	Power on the EOM
4	0x24[7]	Write	1	Enable fast EOM
5	0x24[0] 0x25 0x26	Read	1	Begin read out of the 64 x 64 array, discard first 4 words Ch reg 0x24[0] is self-clearing.
				0x25 is the MSB of the 16-bit word
				0x26 is the LSB of the 16-bit word
6	0x25	Read		Continue reading information until the 64 x 64 array is complete.
	0x26			
7	0x67[5]	Write	1	Return the EOM to its original state. Undo steps 1-4
	0x2C[6]	Write	1	
	0x11[5]	Write	1	
	0x24[7]	Write	0	

6.3.2.4 Interrupt Signals

The DS280DF810 can be configured to report different events as interrupt signals. These interrupt signals do not impact the operation of the device, but merely report that the selected event has occurred. The interrupt bits in the register sets are all sticky bits. This means that when an event triggers an interrupt the status bit for that interrupt is set to logic HIGH. This interrupt status bit will remain at logic HIGH until the bit has been read. Once the bit has been read it will be automatically cleared, which allows for new interrupts to be detected. The DS280DF810 will report the occurrence of an interrupt through the INT_N pin. The INT_N pin is an open drain output that will pull the line low when an interrupt signal is triggered.

Note that all available interrupts are disabled by default. Users must activate the various interrupts before they can be used.

The interrupts available in the DS280DF810 are:

- CDR loss of lock
- CDR locked
- Signal detect loss
- Signal detected
- PRBS pattern checker bit error detected
- HEO/VEO threshold violation

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When an interrupt occurs, share register 0x08 reports which channel generated the interrupt request. Users can then select the channels that generated the interrupt request and service the interrupt by reading the appropriate interrupt status bits in the corresponding channel registers. For more information on reading interrupt status, refer to the DS280DF810 Programming Guide.

6.4 Device Functional Modes

6.4.1 Supported Data Rates

The DS280DF810 supports a wide range of input data rates, including divide-by-2 and divide-by-4 sub-rates. The supported data rates are listed in 表 6-5. Refer to the DS280DF810 Programming Guide for information on configuring the DS280DF810 for different data rates.

表 6-5. Supported Data Rates

DATA RATE RANGE		DIVIDER	CDR MODE	COMMENT
MIN	MAX			
≥ 20.2Gbps	≤ 28.4Gbps	1	Enabled	
≥ 10.1Gbps	≤ 14.2Gbps	2	Enabled	
> 7.1Gbps	< 10.1Gbps	N/A	Disabled	Output jitter will be higher with CDR disabled.
≥ 5.05Gbps	≤ 7.1Gbps	4	Enabled	
≥ 1.25Gbps	< 5.05Gbps	N/A	Disabled	Output jitter will be higher with CDR disabled.

6.4.2 SMBus Controller Mode

SMBus controller mode allows the DS280DF810 to program itself by reading directly from an external EEPROM. When using the SMBus controller mode, the DS280DF810 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines:

- Maximum EEPROM size is 2048 Bytes
- Minimum EEPROM size for a single DS280DF810 with individual channel configuration is 595 Bytes (3 base header bytes + 12 address map bytes + 8 x 72 channel register bytes + 2x2 share register bytes; bytes are defined to be 8-bits)
- Set ENSMB = Float, for SMBus controller mode
- The external EEPROM device address byte must be 0xA0
- The external EEPROM device must support 400 kHz operation at 2.5V or 3.3V supply
- Set the SMBus address of the DS280DF810 by configuring the ADDR0 and ADDR1 pins

When loading multiple DS280DF810 devices from the same EEPROM, use these guidelines to configure the devices:

- Configure the SMBus addresses for each DS280DF810 to be sequential. The first device in the sequence must have an address of 0x30
- Daisy chain READ_EN_N and ALL_DONE_N from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
- If all of the DS280DF810 devices share the same EEPROM channel and share register settings, configure the common channel bit in the base header to 1. With common channel configuration enabled, each DS280DF810 device will configure all 8 channels with the same settings.

When loading a single DS280DF810 from an EEPROM, use these guidelines to configure the device:

6.4.3

- Set the common channel bit to 0 to allow for individual channel configuration, or set the common channel bit to 1 to load the same configuration settings to all channels.
- When configuring individual channels, a 1024 Byte or 2048 Byte EEPROM must be used.

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- If there are more than three DS280DF810 devices on a PCB that require individual channel configuration, then each device must have its own EEPROM.

6.4.4 Device SMBus Address

The DS280DF810's SMBus target address is strapped at power up using the ADDR[1:0] pins. The pin state is read on power up, after the internal power-on reset signal is de-asserted. The ADDR[1:0] pins are four-level LVCMOS IOs, which provides for 16 unique SMBus addresses. The four levels are achieved by pin strap options as follows:

- 0: 1kΩ to GND
- R: 10kΩ to GND
- F: Float
- 1: 1kΩ to VDD

表 6-6. SMBus Address Map

8-BIT WRITE ADDRESS [HEX]	REQUIRED ADDRESS PIN STRAP VALUE	
	ADDR1	ADDR0
0x30	0	0
0x32	0	R
0x34	0	F
0x36	0	1
0x38	R	0
0x3A	R	R
0x3C	R	F
0x3E	R	1
0x40	F	0
0x42	F	R
0x44	F	F
0x46	F	1
0x48	1	0
0x4A	1	R
0x4C	1	F
0x4E	1	1

6.5 Programming

6.5.1 Bit Fields in the Register Set

Many of the registers in the DS280DF810 are divided into bit fields. This allows a single register to serve multiple purposes which may be unrelated. Often, configuring the DS280DF810 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged. The procedure for accomplishing this task is to read in the current value of the register to be written, modify only the desired bits in this value, and write the modified value back to the register. Of course, if the entire register is to be changed, rather than just a bit field within the register, it is not necessary to read in the current value of the register first. In all register configuration procedures described in the following sections, this procedure should be kept in mind. In some cases, the entire register is to be modified. When only a part of the register is to be changed, however, the procedure described above should be used.

Each bit or field within a register has one of the following access properties:

- **R**: Read-only
- **RW**: Read or Write
- **RWSC**: Read or Write, self-clearing

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6.5.2 Writing to and Reading from the Global/Shared/Channel Registers

The DS280DF810 has 3 types of registers:

1) Global Registers – These registers can be accessed at any time and are used to select individual channel registers, the shared registers or to read back the TI ID and version information.

2) Shared Registers – These registers are used for device-level configuration, status read back or control.

3) Channel Registers – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

The global registers can be accessed at any time, regardless of whether the shared or channel register set is selected. The DS280DF810 global registers are located on addresses 0xEF-0xFF. The function of the global registers falls into the following categories:

- Channel selection and share enabling – Registers 0xFC and 0xFF
- Device and version information – Registers 0xEF-0xF3
- Reserved or unused registers – all other addresses

Register 0xFF[5:4] selects the share registers of either Quad 0 (channels 0-3) or Quad 1 (channels 4-7).

Register 0xFC is used to select the channel registers to be written to. To select a channel, write a 1 to its corresponding bit in register 0xFC. Note that more than one channel may be written to by setting multiple bits in register 0xFC. However, when performing an SMBus read transaction only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0xFF.

Register 0xFF bit 1 can be used to perform broadcast register writes to all channels. A single channel read-modify broadcast write type commands can be accomplished by setting register 0xFF to 0x03 and selecting a single channel in register 0xFC. This type of configuration allows for the reading of a single channel's register information and then writing to all channels with the modified value. Register 0xFF bit 0 is used to select the shared register page or the channel register page for the channels selected in register 0xFC.

TI repeaters and retimers have a vendor ID register (0xFE) which will always read back 0x03. In addition, there are three device ID registers (0xF0, 0xF1, and 0xF3). These are useful to verify that there is a good SMBus connection between the SMBus controller and the DS280DF810.

6.6 Register Maps

Refer to the DS280DF810 Programming Guide (SNLU182) for the complete register map and example programming sequences.

The DS280DF810 has a vendor ID register (0xFE), which will always read back 0x03. In addition, there are four device ID registers (0xEF, 0xF0, 0xF1, and 0xF3). Reading these five registers and confirming the expected value is a good way to verify SMBus communications between the SMBus Controller and the DS280DF810. In addition, writing a value to channel select Reg_0xFC and confirming the correct value is read back is a good way to verify SMBus write communications with the DS280DF810.

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7 Application and Implementation

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7.1 Application Information

The DS280DF810 is a high-speed retimer which extends the reach of differential channels and cleans jitter and other signal impairments in the process. It can be deployed in a variety of different systems from backplanes to front ports to active cable assemblies. The following sections outline typical applications and their associated design considerations.

7.2 Typical Application

The DS280DF810 is typically used in the following application scenarios:

1. Backplane and Mid-Plane Reach Extension Application
2. Front-Port Jitter Cleaning Application

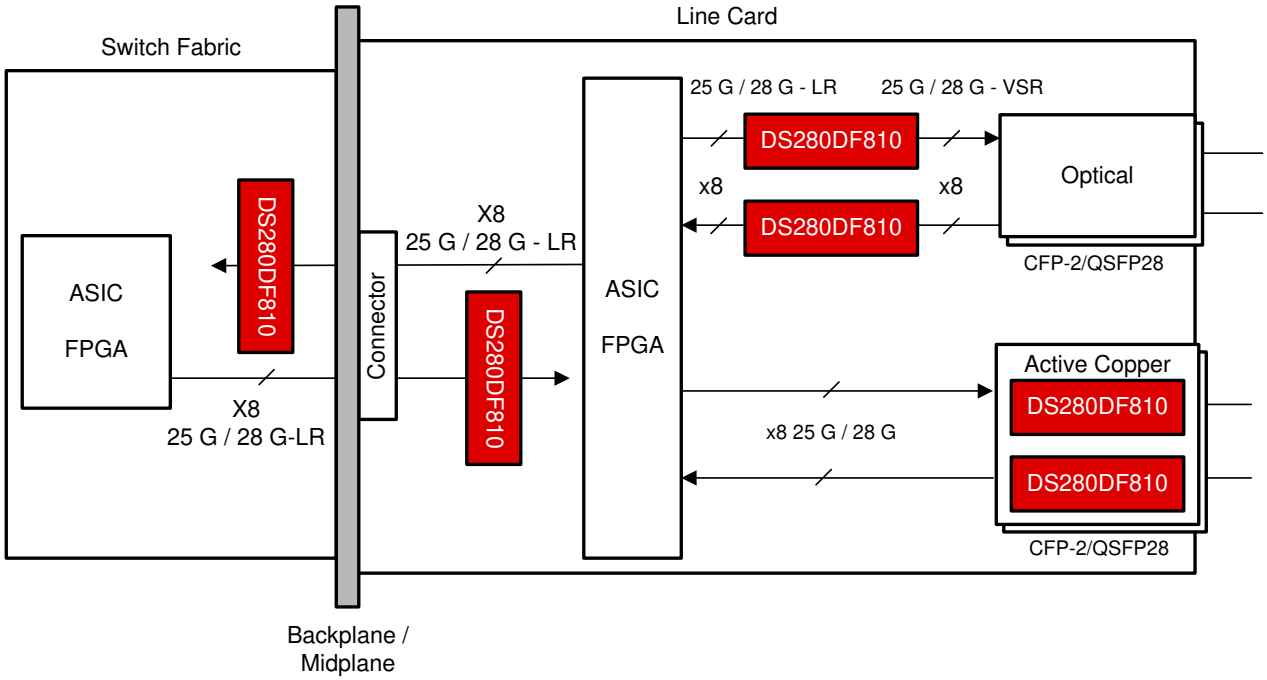

図 7-1. Typical uses for the DS280DF810 in a system

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7.2.1 Backplane and Mid-Plane Reach Extension Application

The DS280DF810 has strong equalization capabilities that allow it to recover data over channels up to 35dB insertion loss (at 12.9GHz). As a result, the optimum placement for the DS280DF810 in a backplane and mid-plane application is with the higher-loss channel segment at the input and the lower-loss channel segment at the output. This reduces the equalization burden on the downstream ASIC/FPGA, as the DS280DF810 is equalizing a majority of the overall channel. This type of asymmetric placement is not a requirement, but when an asymmetric placement is required due to the presence of a passive backplane or mid-plane, then this becomes the recommended placement.

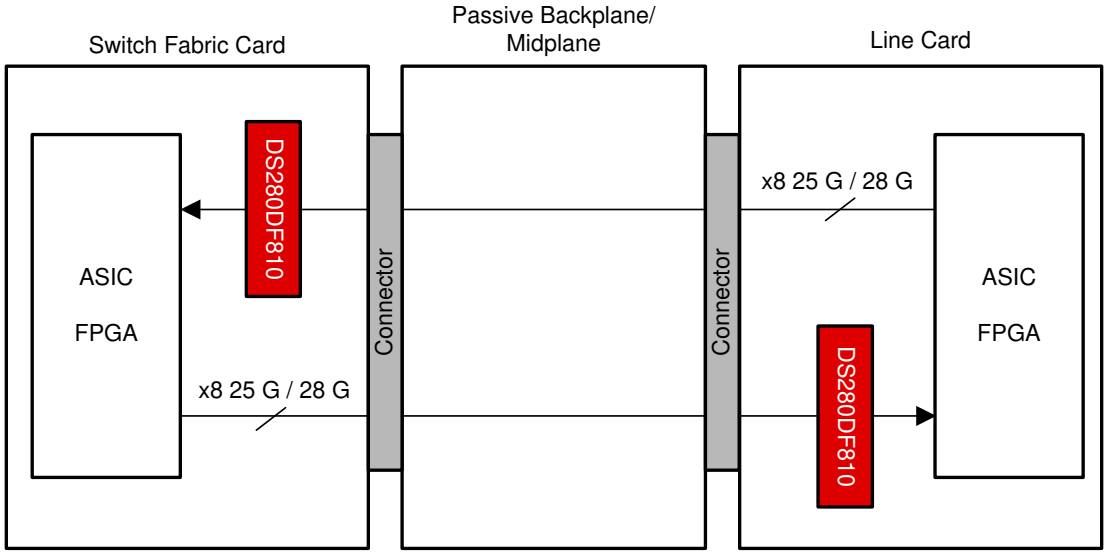
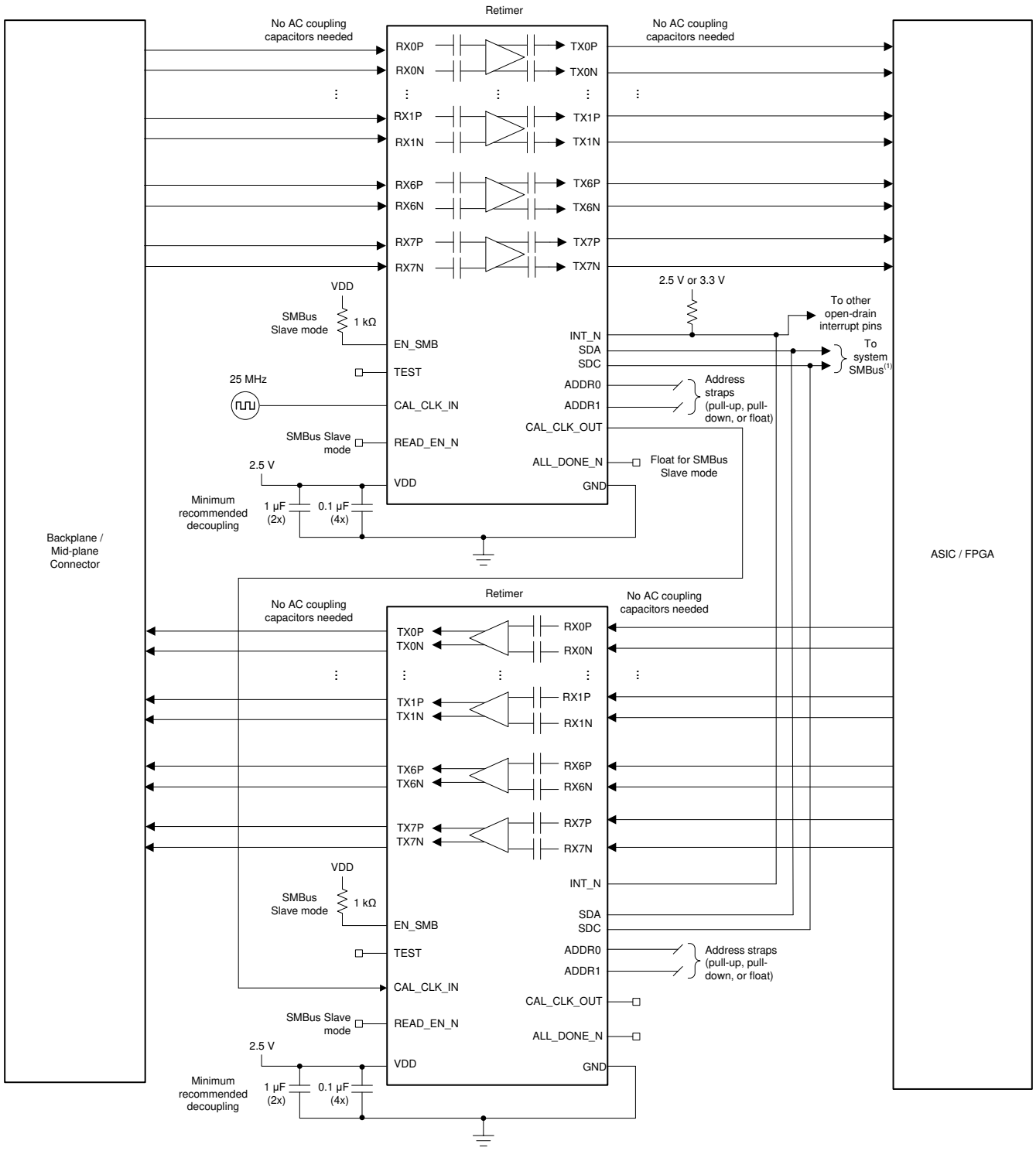


図 7-2. Backplane and Mid-Plane Application Block Diagram



(1) SMBus signals need to be pulled up elsewhere in the system.

図 7-3. Backplane and Mid-Plane Application Schematic

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7.2.1.1 Design Requirements

For this design example, the following guidelines outlined in 表 7-1 apply.

表 7-1. Backplane and Mid-Plane Application Design Guidelines

DESIGN PARAMETER	REQUIREMENT
AC coupling capacitors	Not required. AC coupling capacitors are included in the device package.
Input channel insertion loss	≤ 35dB at 25.78125Gbps Nyquist frequency ≤ 30dB at 28Gbps Nyquist frequency
Output channel insertion loss	Depends on downstream ASIC and FPGA capabilities. The DS280DF810 has a low-jitter output driver with 3-tap FIR filter for equalizing a portion of the output channel.
Link partner TX launch amplitude	800mVppd to 1200mVppd
Link partner TX FIR filter	Depends on channel loss

7.2.1.2 Detailed Design Procedure

The design procedure for backplane and mid-plane applications is as follows:

1. Determine the total number of channels on the board which require a DS280DF810 for signal conditioning. This will dictate the total number of DS280DF810 devices required for the board. It is generally recommended that channels with similar total insertion loss on the board be grouped together in the same DS280DF810 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280DF810 retimers. This may impact the selection of the regulator for the 2.5V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS280DF810 devices.
3. Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
   a. Maximum mission-mode operational power consumption is when all channels are locked and retransmitting the data which is received. PRBS pattern checkers and generators are not used in this mode since normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS280DF810 devices.
   b. Maximum debug-mode operational power consumption is when all channels are locked and retransmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS280DF810 devices.
4. Determine the SMBus address scheme needed to uniquely address each DS280DF810 device on the board. Each DS280DF810 can be strapped with one of 16 unique SMBus addresses. If there are more DS280DF810 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I^2C expander like the **TCA/PCA family of I^2C/SMBus switches and multiplexers** to split up the SMBus into multiple busses.
5. Determine if the device will be configured from EEPROM (SMBus Controller Mode) or from the system I^2C bus (SMBus Target Mode).
   a. If SMBus Controller Mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
   b. If SMBus Target Mode will be used for all device configurations, an EEPROM is not needed.
6. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in *セクション 4* for more details.

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7. Make provisions in the schematic and layout for a 25MHz (±100 ppm) single-ended CMOS clock. Each DS280DF810 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) retimers' calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5V CMOS output, then no AC coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one retimer's CAL_CLK_OUT output and the next retimer's CAL_CLK_IN input. The final retimer's CAL_CLK_OUT output can be left floating.
8. Connect the INT_N open-drain output to an FPGA or CPU if interrupt monitoring is desired. Note that multiple retimers' INT_N outputs can be connected together since this is an open-drain output. The common INT_N net should be pulled high.
9. If the application requires initial CDR lock acquisition at the ambient temperature extremes defined in *セクション 5.6*, then care should be taken so that the operating junction temperature is met as well as the CDR stay-in-lock ambient temperature range defined in *セクション 5.6*. For example, if initial CDR lock acquisition occurs at an ambient temperature of 85 °C, then maintaining CDR lock would require the ambient temperature surrounding the DS280DF810 to be kept above (85 °C - $TEMP_{LOCK-}$).

7.2.2 Front-Port Jitter Cleaning Application

The DS280DF810 has strong equalization capabilities that allow it to equalize insertion loss, reduce jitter, and extend the reach of front-port interfaces. A single DS280DF810 can be used to support all eight *egress* channels for a stacked QSFP cage. Another DS280DF810 can be used to support all eight *ingress* channels for the same stacked QSFP cage. Alternatively, a single DS280DF810 can be used to support all egress and ingress channels for a single QSFP port.

For applications which require IEEE802.3 100GBASE-CR4 or 25GBASE-CR auto-negotiation and link training, a linear repeater device such as the DS280BR820 (or similar) is recommended.

図 7-4 illustrates this configuration, and セクション 5.6 shows an example simplified schematic for a typical front-port application.

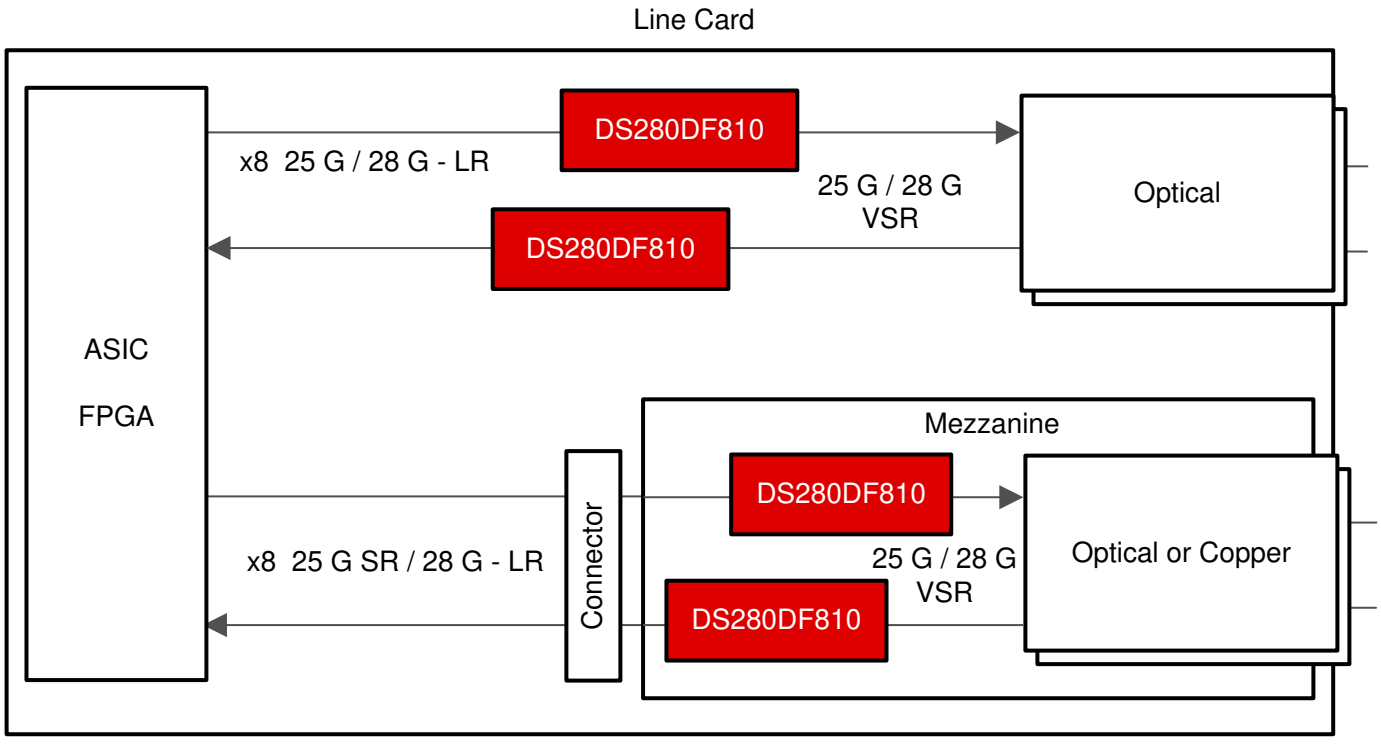

図 7-4. Front-Port Application Block Diagram

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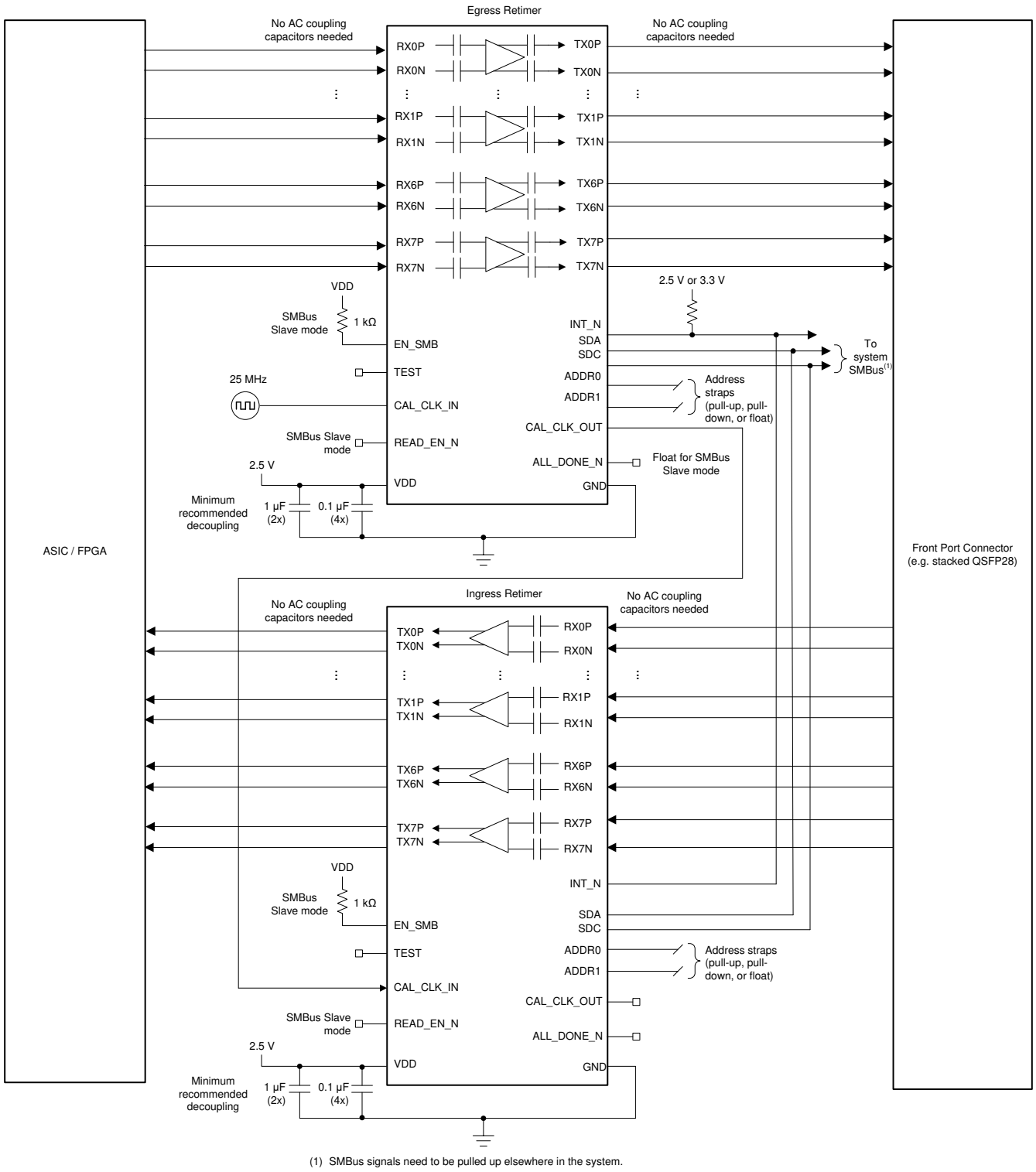

(1) SMBus signals need to be pulled up elsewhere in the system.

図 7-5. Front-Port Application Schematic

7.2.2.1 Design Requirements

For this design example, the following guidelines outlined in 表 7-2 apply.

表 7-2. Front-Port Application Design Guidelines

DESIGN PARAMETER	REQUIREMENT
AC coupling capacitors	Not required. AC coupling capacitors are included in the device package.
Input channel insertion loss	≤ 35dB at 25.78125Gbps Nyquist frequency. ≤ 30dB at 28Gbps Nyquist frequency.
Output channel insertion loss	*Egress (ASIC-to-module) direction*: Follow CAUI-4 / CEI-25G-VSR host channel requirements (approximately 7dB at 12.9GHz). *Ingress (module-to-ASIC) direction*: Depends on downstream ASIC and FPGA capabilities. The DS280DF810 has a low-jitter output driver with 3-tap FIR filter for equalizing a portion of the output channel.
Host ASIC TX launch amplitude	800mVppd to 1200mVppd
Hos ASIC TX FIR filter	Depends on channel loss. Refer to セクション 6.3.1.9.1.

7.2.2.2 Detailed Design Procedure

The design procedure for front-port applications is as follows:

1. Determine the total number of channels on the board which require a DS280DF810 for signal conditioning. This will dictate the total number of DS280DF810 devices required for the board. It is generally recommended that channels with similar total insertion loss on the board be grouped together in the same DS280DF810 device. This will simplify the device settings, as similar loss channels generally utilize similar settings.
2. Determine the maximum current draw required for all DS280DF810 retimers. This may impact the selection of the regulator for the 2.5V supply rail. To calculate the maximum current draw, multiply the maximum transient power supply current by the total number of DS280DF810 devices.
3. Determine the maximum operational power consumption for the purpose of thermal analysis. There are two ways to approach this calculation:
   a. Maximum mission-mode operational power consumption is when all channels are locked and retransmitting the data which is received. PRBS pattern checkers and generators are not used in this mode since normal traffic cannot be checked with a PRBS checker. For this calculation, multiply the worst-case power consumption in mission mode by the total number of DS280DF810 devices.
   b. Maximum debug-mode operational power consumption is when all channels are locked and retransmitting the data which is received. At the same time, some channels' PRBS checkers or generators may be enabled. For this calculation, multiply the worst-case power consumption in debug mode by the total number of DS280DF810 devices.
4. Determine the SMBus address scheme needed to uniquely address each DS280DF810 device on the board. Each DS280DF810 can be strapped with one of 16 unique SMBus addresses. If there are more DS280DF810 devices on the board than the number of unique SMBus addresses which can be assigned, then use an I^2C expander like the **TCA/PCA family of I^2C/SMBus switches and multiplexers** to split up the SMBus into multiple busses.
5. Determine if the device will be configured from EEPROM (SMBus Controller Mode) or from the system I^2C bus (SMBus Target Mode).
   a. If SMBus Controller Mode will be used, provisions should be made for an EEPROM on the board with 8-bit SMBus address 0xA0.
   b. If SMBus Target Mode will be used for all device configurations, an EEPROM is not needed.
6. Make provisions in the schematic and layout for standard decoupling capacitors between the device VDD supply and GND. Refer to the pin function description in *セクション 4* for more details.

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7. Make provisions in the schematic and layout for a 25MHz (±100 ppm) single-ended CMOS clock. Each DS280DF810 retimer buffers the clock on the CAL_CLK_IN pin and presents the buffered clock on the CAL_CLK_OUT pin. This allows multiple (up to 20) retimers' calibration clocks to be daisy chained to avoid the need for multiple oscillators on the board. If the oscillator used on the board has a 2.5V CMOS output, then no AC coupling capacitor or resistor ladder is required at the input to CAL_CLK_IN. No AC coupling or resistor ladder is needed between one retimer's CAL_CLK_OUT output and the next retimer's CAL_CLK_IN input. The final retimer's CAL_CLK_OUT output can be left floating.
8. Connect the INT_N open-drain output to an FPGA or CPU if interrupt monitoring is desired. Note that multiple retimers' INT_N outputs can be connected together since this is an open-drain output. The common INT_N net should be pulled high.
9. If the application requires initial CDR lock acquisition at the ambient temperature extremes defined in *セクション 5.6*, care should be taken so that the operating junction temperature is met as well as the CDR stay-in-lock ambient temperature range defined in *セクション 5.6*. For example, if initial CDR lock acquisition occurs at an ambient temperature of 85 °C, then maintaining CDR lock would require the ambient temperature surrounding the DS280DF810 to be kept above (85 °C - $TEMP_{LOCK-}$).

7.2.3 Application Curves

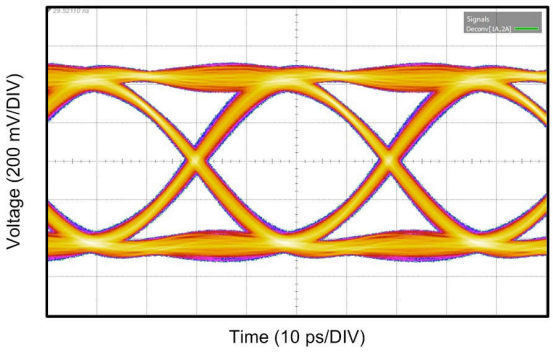

図 7-6. DS280DF810 Operating at 25.78125Gbps

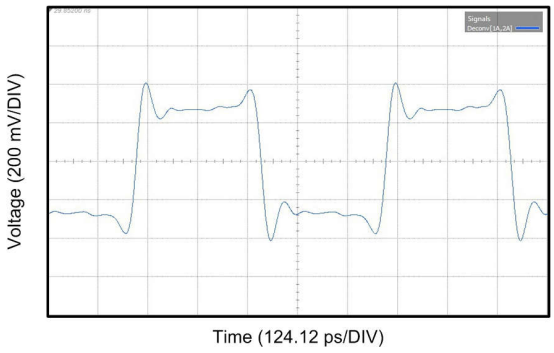

図 7-7. DS280DF810 FIR Transmit Equalization while Operating at 25.78125Gbps

図 7-6 shows a typical output eye diagram for the DS280DF810 operating at 25.78125Gbps with PRBS9 pattern using FIR main-cursor of +18, pre-cursor of -1 and post-cursor of +2. All other device settings are left at default.

図 7-7 shows an example of DS280DF810 FIR transmit equalization while operating at 25.78125Gbps. In this example, the Tx FIR filter main-cursor is set to +15, post-cursor to -3 and pre-cursor to -3. An 8T pattern is used to evaluate the FIR filter, which consists of 0xFF00. All other device settings are left at default.

7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions outlined in セクション 5 in terms of DC voltage, AC noise, and start-up ramp time.
2. The maximum current draw for the DS280DF810 is provided in *セクション 5* . This figure can be used to calculate the maximum current the supply must provide. Typical mission-mode current draw can be inferred from the typical power consumption in *セクション 5*.
3. The DS280DF810 does not require any special power supply filtering (that is, ferrite bead) provided the recommended operating conditions are met. Only standard supply decoupling is required. Refer to セクション 4 for details concerning the recommended supply decoupling.

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7.4 Layout

7.4.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VDD pins as possible. Placing them directly underneath the device is one option if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, care should be taken to minimize the via stub, either by transitioning through most or all layers, or by back drilling.
4. GND relief can be used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board
6. BGA landing pads for a 0.8mm pitch flip-chip BGA are typically 0.4mm in diameter (exposed). The actual size of the copper pad will depend on whether solder-mask-defined (SMD) or non-solder-mask-defined solder land pads are used. For more information, refer to TI's Surface Mount Technology (SMT) References at http://focus.ti.com/quality/docs under the "Quality and Lead (Pb)-Free Data" menu.
7. If vias are used for the high-speed signals, ground via should be implemented adjacent to the signal via to provide return path and isolation. For differential pair, the typical via configuration is "ground-signal-signal-ground."

7.4.2 Layout Example

The following example layout demonstrates how all signals can be escaped from the BGA array using stripline routing on a generic 28-layer stackup. This example layout assumes the following:

- Trace width: 0.127mm (5 mil)
- Trace edge-to-edge spacing: 0.152mm (6 mil)
- VIA finished hole size (diameter): 0.203mm (8 mil)
- VIA drilled hole size: 0.254mm (10 mil)
- VIA-to-VIA spacing: 1.0mm (39 mil), to enhance PCB manufacturability
- No VIA-in-pad used

Note that many other escape routing options exist using different trace width and spacing combinations. The optimum trace width and spacing will depend on the PCB material, PCB routing density, and other factors.

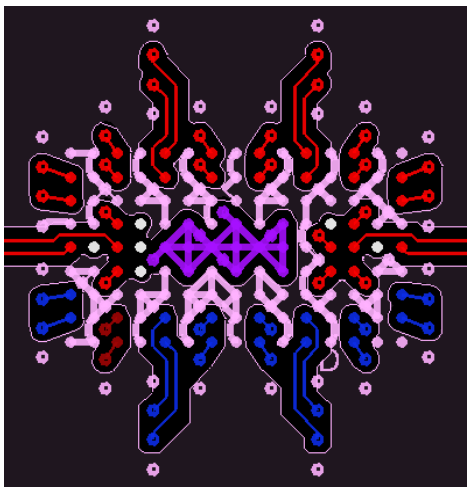

図 7-8. Top Layer

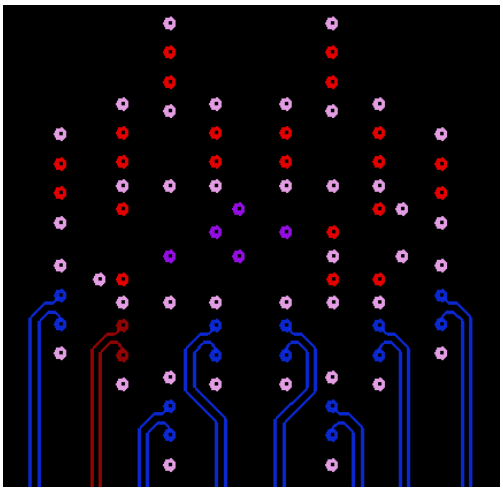

図 7-9. Internal Signal Layer 1

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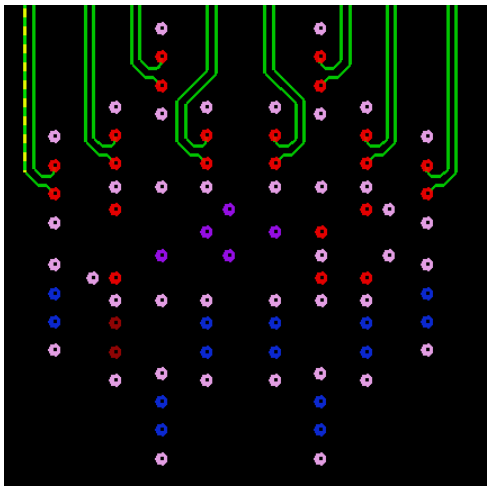

図 7-10. Internal Signal Layer 2

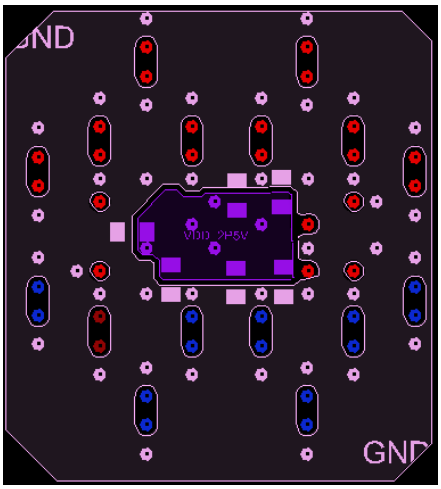

図 7-11. Bottom Layer

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

-
- Texas Instruments, *25G/28G Retimer Programmer's Guide*
- Texas Instruments, *DS280DF810EVM User's Guide*
- Texas Instruments, *Understanding EEPROM Programming for 25G and 28G Repeaters and Retimers Application Report*
- Texas Instruments, *Implementation of TI 25G/28G Retimers for CPRI-7 Applications Application Report*
- Texas Instruments, *DS2X0DF810 Adaption Parameters Optimization Proceed Application Report*
- Texas Instruments, *DS2X0DFX10 25Gbps/28Gbps Retimer Functional Guide Application Report*
- Texas Instruments, *25G/28G Retimer CDR Lock Optimization for Outlier Data Rate PPM Check Scenario Application Report*
- Texas Instruments, *Implementation of TI 25G/28G Retimers for OTU4 Applications Application Report*
- Texas Instruments, *Selection Guide for TI 25G and 28G Retimers and Repeaters Application Report*

Click here to request access the Programmers Guide in the DS280DF810 MySecure folder.

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2019) to Revision B (February 2024)	Page
• 概略回路図を変更し、TX AC カップリング コンデンサを追加	1

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- データシート全体にわたって包括的な用語を追加 1
- Removed Table 7 31

Changes from Revision * (February 2019) to Revision A (October 2019) **Page**

- 最初の公開リリース 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS280DF810ABVR	Active	Production	FCCSP (ABV) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8
DS280DF810ABVR.A	Active	Production	FCCSP (ABV) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8
DS280DF810ABVR.B	Active	Production	FCCSP (ABV) | 135	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS280DF810ABVT	Active	Production	FCCSP (ABV) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8
DS280DF810ABVT.A	Active	Production	FCCSP (ABV) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8
DS280DF810ABVT.B	Active	Production	FCCSP (ABV) | 135	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
DS280DF810ABWR	Active	Production	FCCSP (ABW) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8W
DS280DF810ABWR.A	Active	Production	FCCSP (ABW) | 135	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8W
DS280DF810ABWR.B	Active	Production	FCCSP (ABW) | 135	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS280DF810ABWT	Active	Production	FCCSP (ABW) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8W
DS280DF810ABWT.A	Active	Production	FCCSP (ABW) | 135	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	DS280DF8W
DS280DF810ABWT.B	Active	Production	FCCSP (ABW) | 135	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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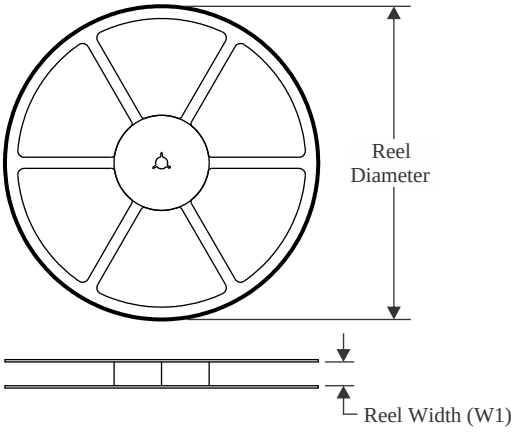
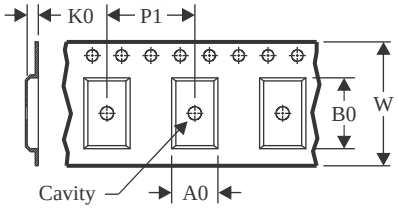
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

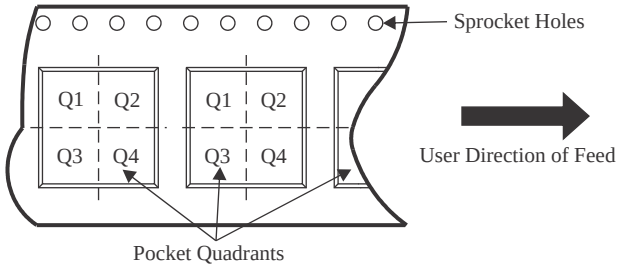


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

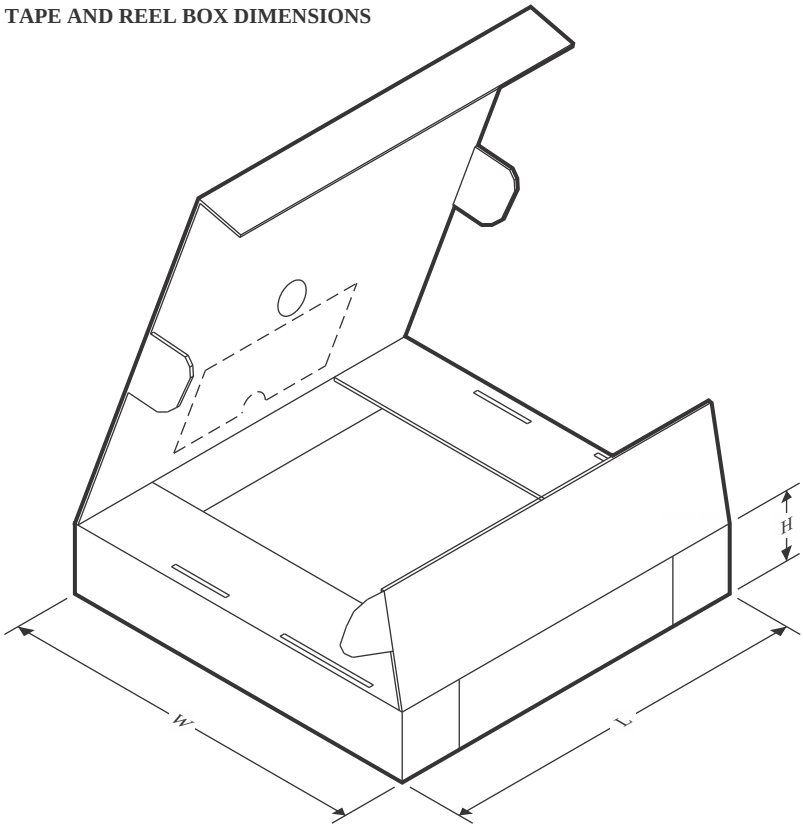
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS280DF810ABVR	FCCSP	ABV	135	1000	330.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2
DS280DF810ABVT	FCCSP	ABV	135	250	178.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2
DS280DF810ABWR	FCCSP	ABW	135	1000	330.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2
DS280DF810ABWT	FCCSP	ABW	135	250	178.0	24.4	8.4	13.4	3.0	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

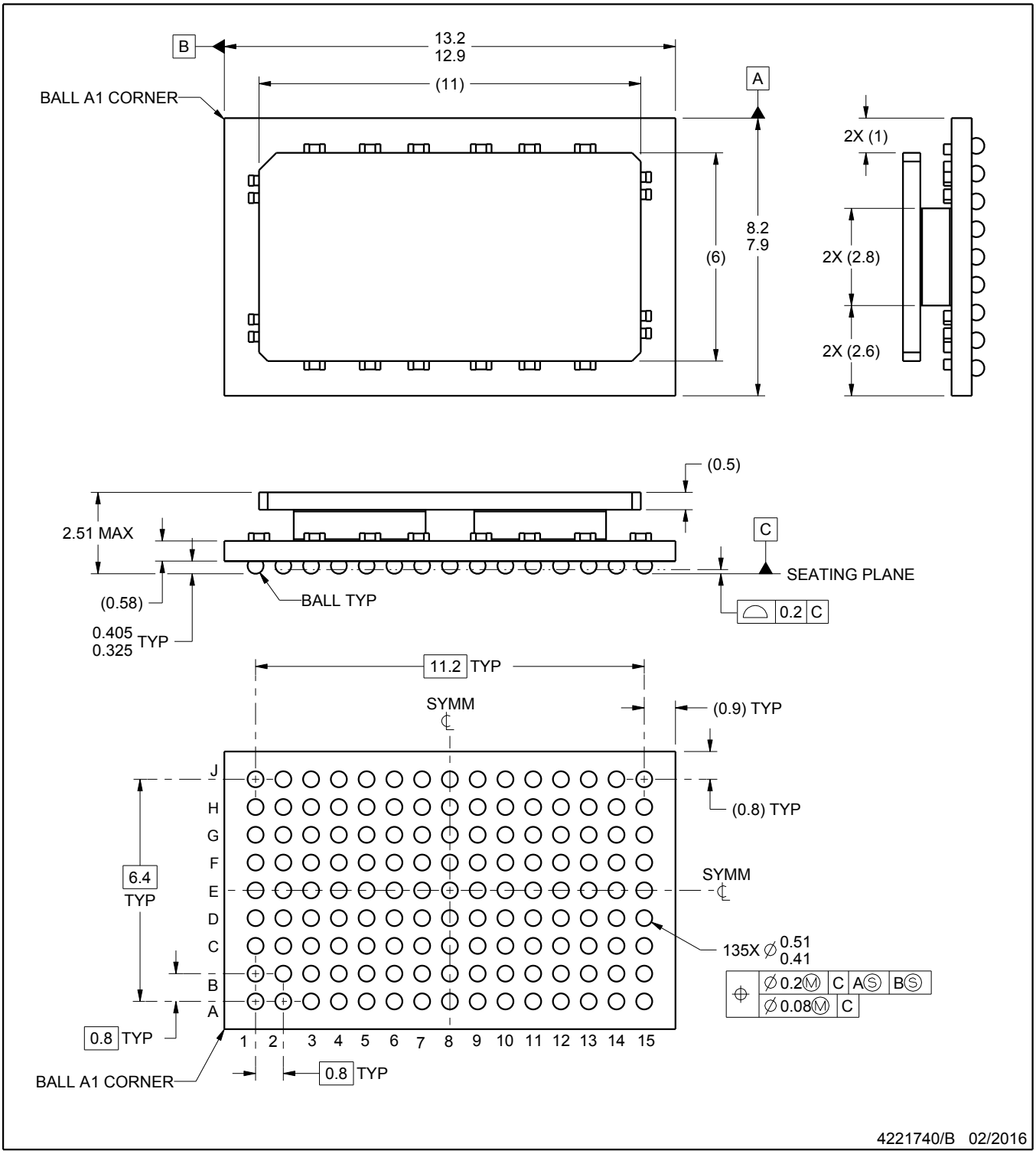
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS280DF810ABVR	FCCSP	ABV	135	1000	356.0	356.0	45.0
DS280DF810ABVT	FCCSP	ABV	135	250	213.0	191.0	55.0
DS280DF810ABWR	FCCSP	ABW	135	1000	356.0	356.0	45.0
DS280DF810ABWT	FCCSP	ABW	135	250	213.0	191.0	55.0

PACKAGE OUTLINE

ABV0135A

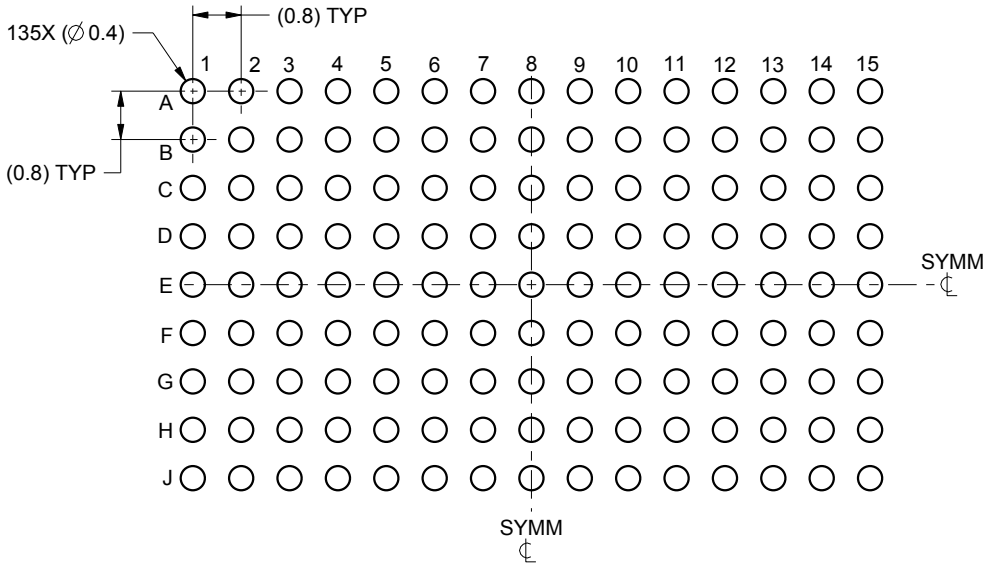
FCBGA - 2.51 mm max height

BALL GRID ARRAY

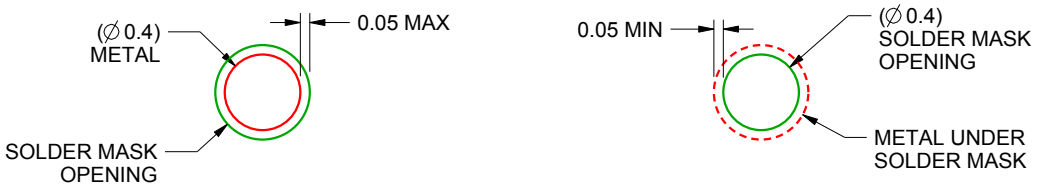


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



NON-SOLDER MASK
DEFINED
(PREFERRED)

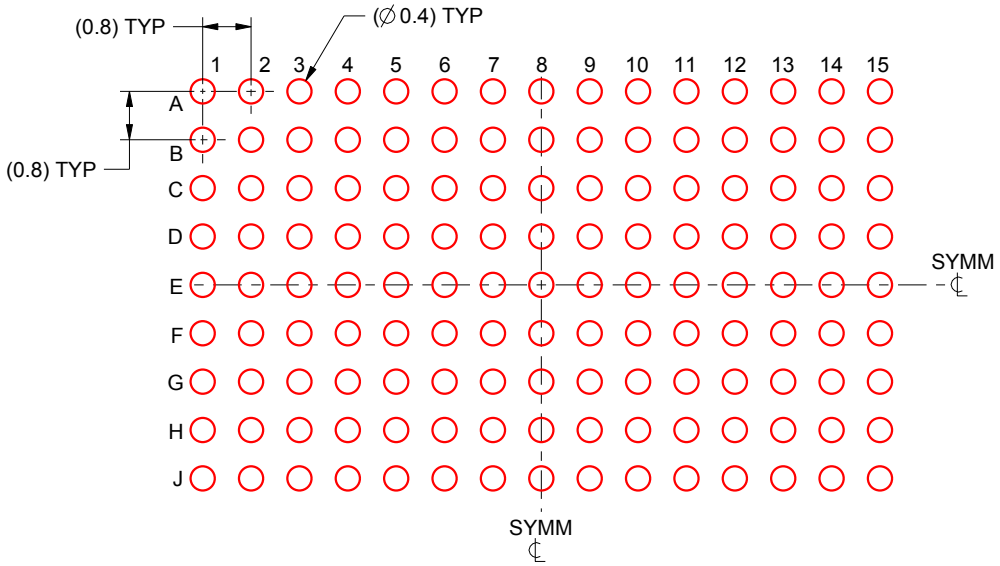
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221740/B 02/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221740/B 02/2016

NOTES: (continued)

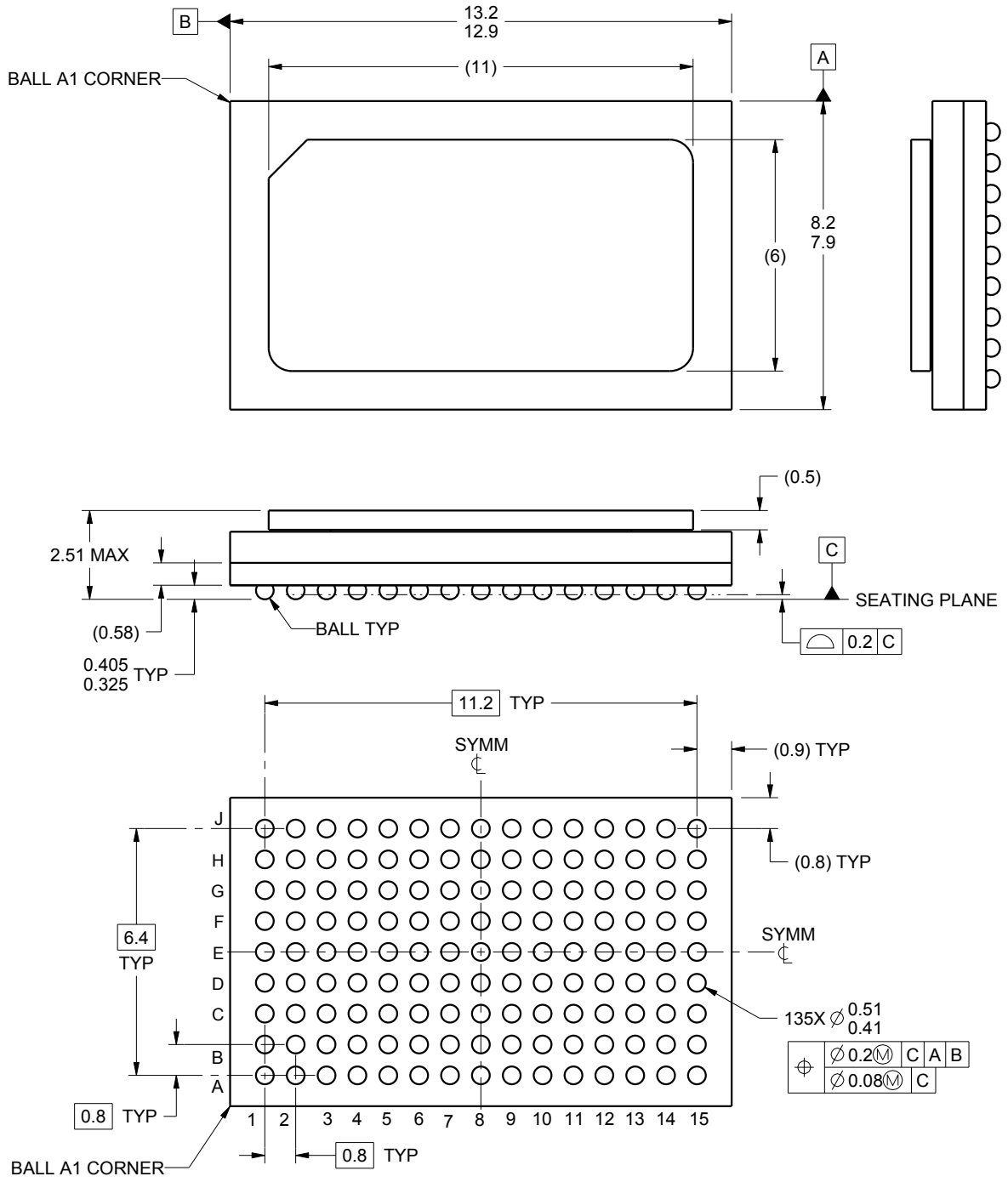
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ABW0135A

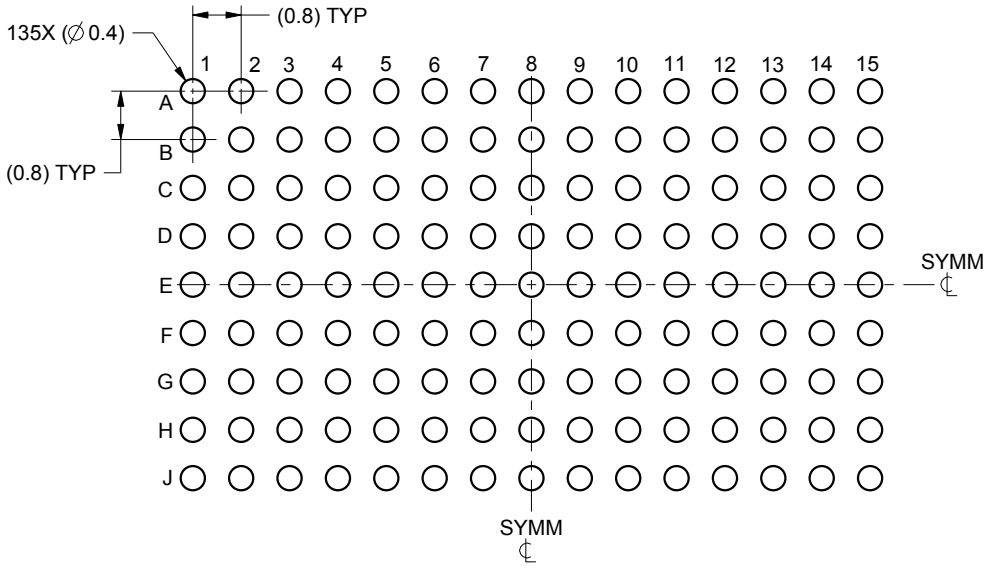
FCBGA - 2.51 mm max height

BALL GRID ARRAY

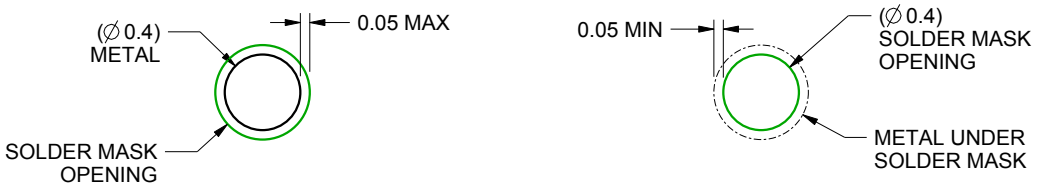


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



NON-SOLDER MASK
DEFINED
(PREFERRED)

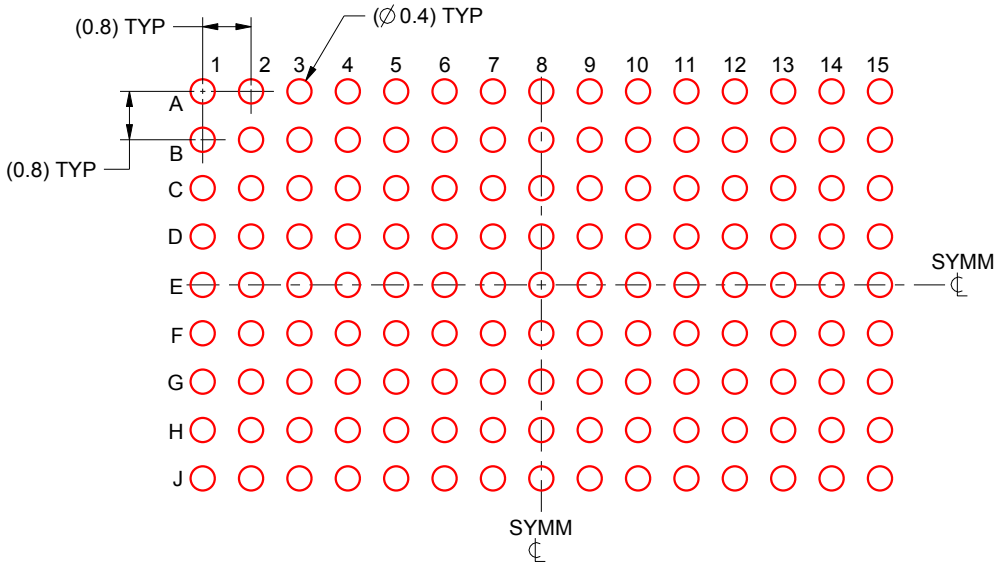
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223026/A 05/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4223026/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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