TEXAS INSTRUMENTS
DS90CF366, DS90CF386
JAJS673J – NOVEMBER 1999 – REVISED MAY 2016

# DS90CF3x6 3.3V LVDSレシーバ、24ビットまたは18ビットのフラット・パネル・ディスプレイ(FPD)リンク、85MHz

## 1 特長

- 20MHz～85MHzのシフト・クロックをサポート
- 85MHzのグレイスケールにおいてRx消費電力が142mW未満(標準値)
- Rxパワーダウン・モードで1.44mW未満(最大値)
- ESD定格7kV超(HBM)、700V超(EIAJ)
- VGA、SVGA、XGA、およびシングル・ピクセルSXGAをサポート
- PLLに外部コンポーネントが不要
- TIA/EIA-644 LVDS標準と互換
- 低プロファイルの56ピンまたは48ピンTSSOPパッケージ
- DS90CF386は64ピン、0.8mm、ファインピッチ・ボール・グリッド・アレイ(NFBGA)パッケージでも利用可能

## 2 アプリケーション

- ビデオ・ディスプレイ
- プリンタおよび画像処理
- デジタル・ビデオの転送
- マシン・ビジョン
- Open LDIからRGBへのブリッジ

## 3 概要

DS90CF386レシーバは、4つのLVDS (低電圧差分信号)データ・ストリームを、パラレルの28ビットLVCMOSデータへ戻します。3つのLVDSデータ・ストリームをパラレルの21ビットLVCMOSデータへ戻す、DS90CF366レシーバも利用できます。どちらのレシーバの出力も、立ち下がりエッジにストローブします。立ち上がりエッジまたは立ち下がりエッジのストローブ・トランスミッタは、変換ロジックなしで、立ち下がりエッジのストローブ・レシーバと相互に動作します。

レシーバのLVDSクロックは、20MHz～85MHzで動作します。

デバイスは入力LVDSクロックにフェーズロックし、LVDSデータ・ラインのシリアル・ビット・ストリームをサンプリングして、パラレルの出力データへ変換します。

供給されるクロックが85MHzの場合、各LVDS入力ラインは595Mbpsのビット転送速度で動作し、最大スループットはDS90CF386で2.38Gbps、DS90CF366で1.785Gbpsになります。

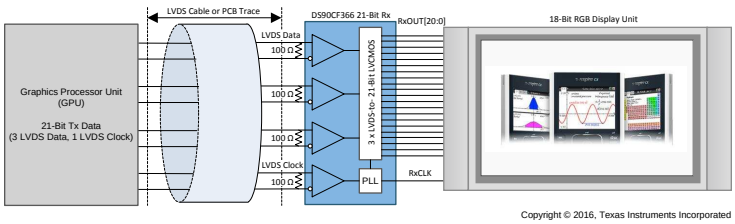
これらのシリアル・リンク・デバイスの使用は、幅広で高速のパラレルLVCMOSインターフェイス上でデータを伝送する場合に発生するEMIやケーブル・サイズの問題を解決するために理想的です。どちらのデバイスも、TSSOPパッケージで提供されます。DS90CF386は64ピン、0.8mmのファイン・ピッチ・ボール・グリッド・アレイ(NFBGA)パッケージでも提供され、56ピンのTSSOPパッケージと比較してPCBの占有面積を44%削減できます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| DS90CF366 | TSSOP (48) | 12.50mm×6.10mm |
| DS90CF386 | TSSOP (56) | 14.00mm×6.10mm |
| | NFBGA (64) | 8.00mm×8.00mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

**代表的なアプリケーションのブロック図(DS90CF366)**

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision I (April 2013)** から **Revision J** に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Changed Figure 8 and Figure 9 to clarify that TxIN on Tx is the same as RxOUT on Rx ... 12
- Changed title of DS90CF366 mapping to clarify the make-up of the LVDS lines ... 13
- Deleted references to power sequencing requirements for FPD-Link I transmitters ... 19

**Revision H (April 2013)** から **Revision I** に変更 **Page**

- ナショナルのデータシートのレイアウトをTIフォーマットへ 変更 ... 1


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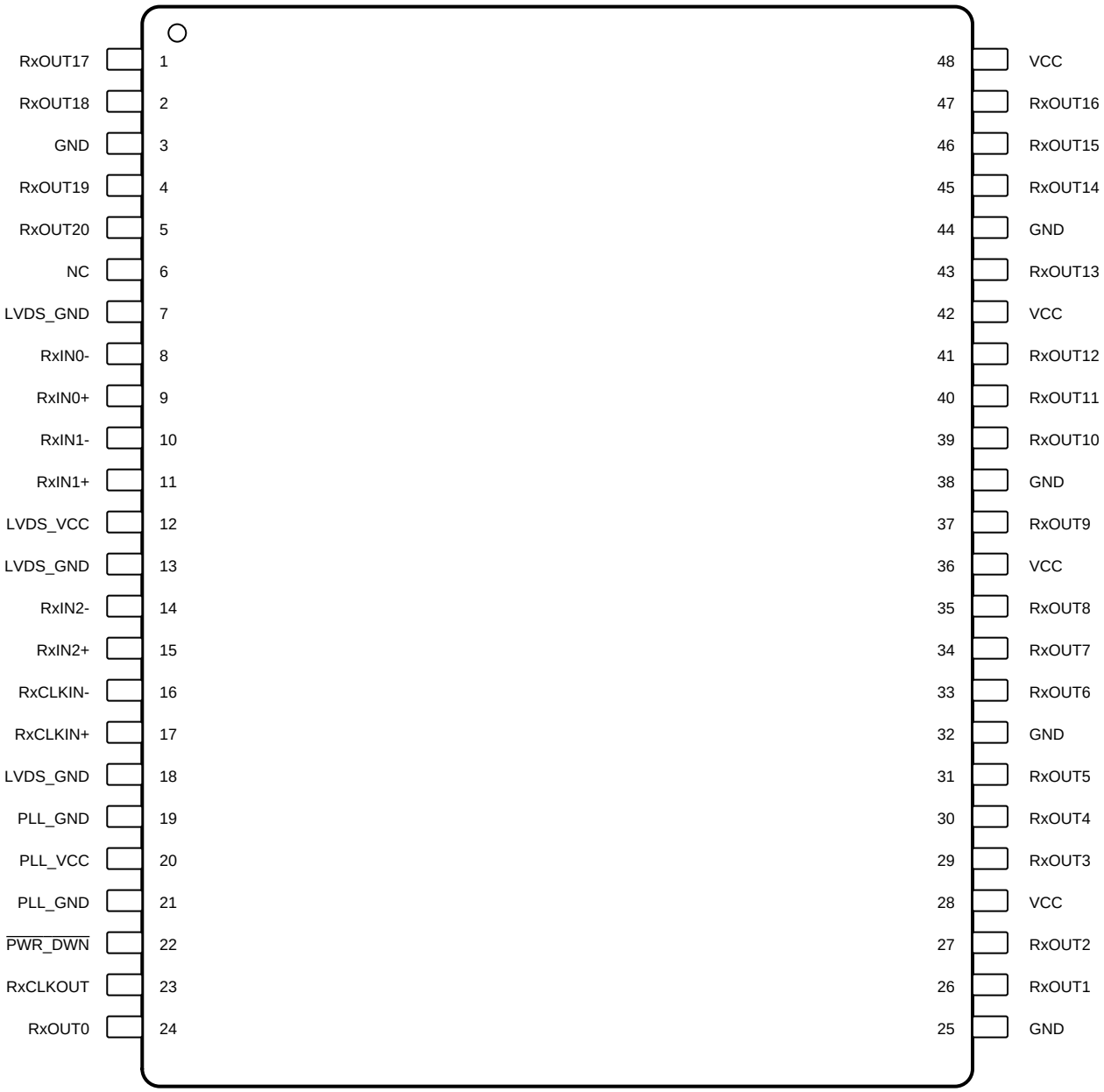
# 5 Pin Configuration and Functions

**DGG Package**
**48-Pin TSSOP**
**Top View**

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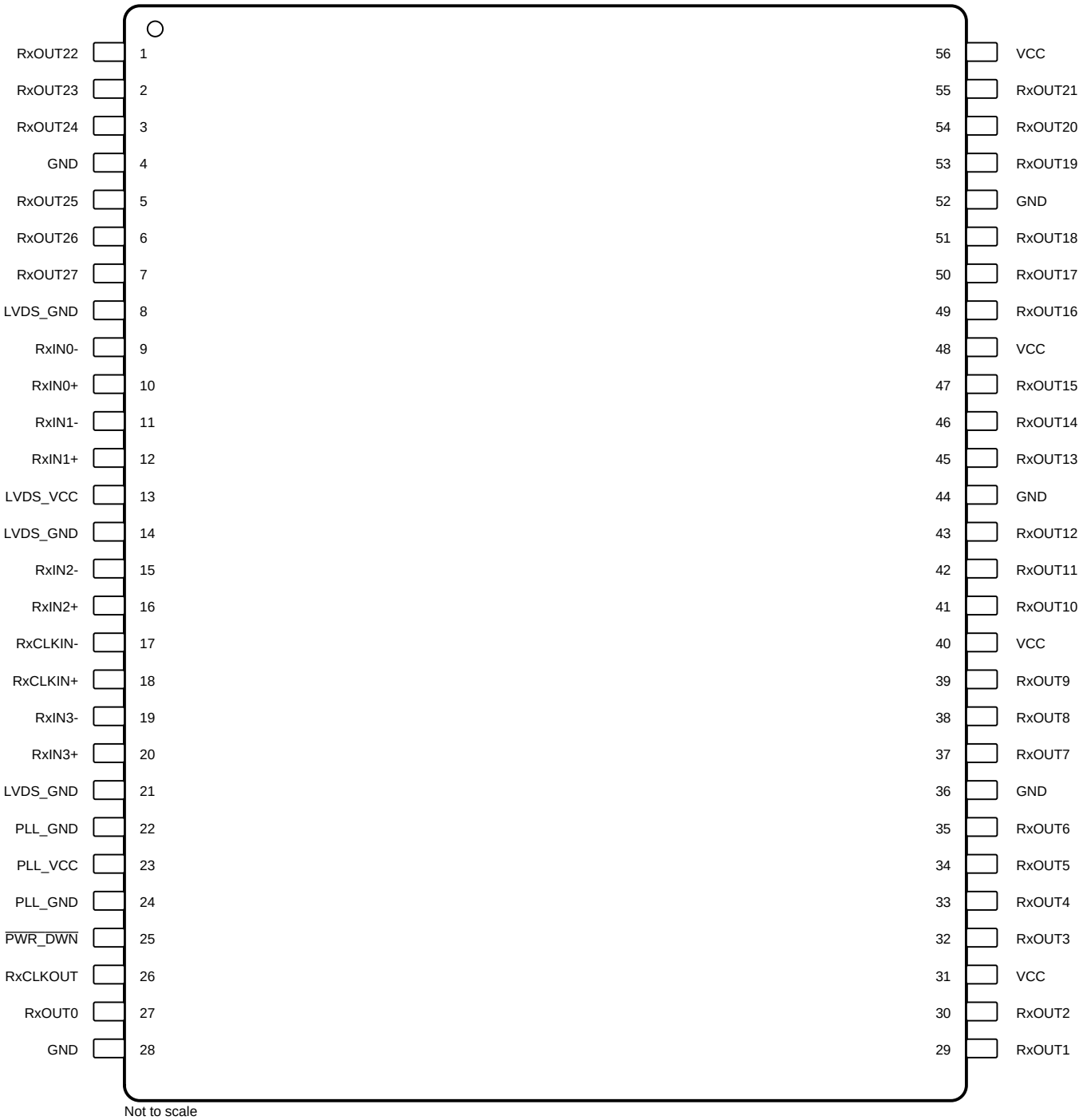
**DGG Package**
**56-Pin TSSOP**
**Top View**

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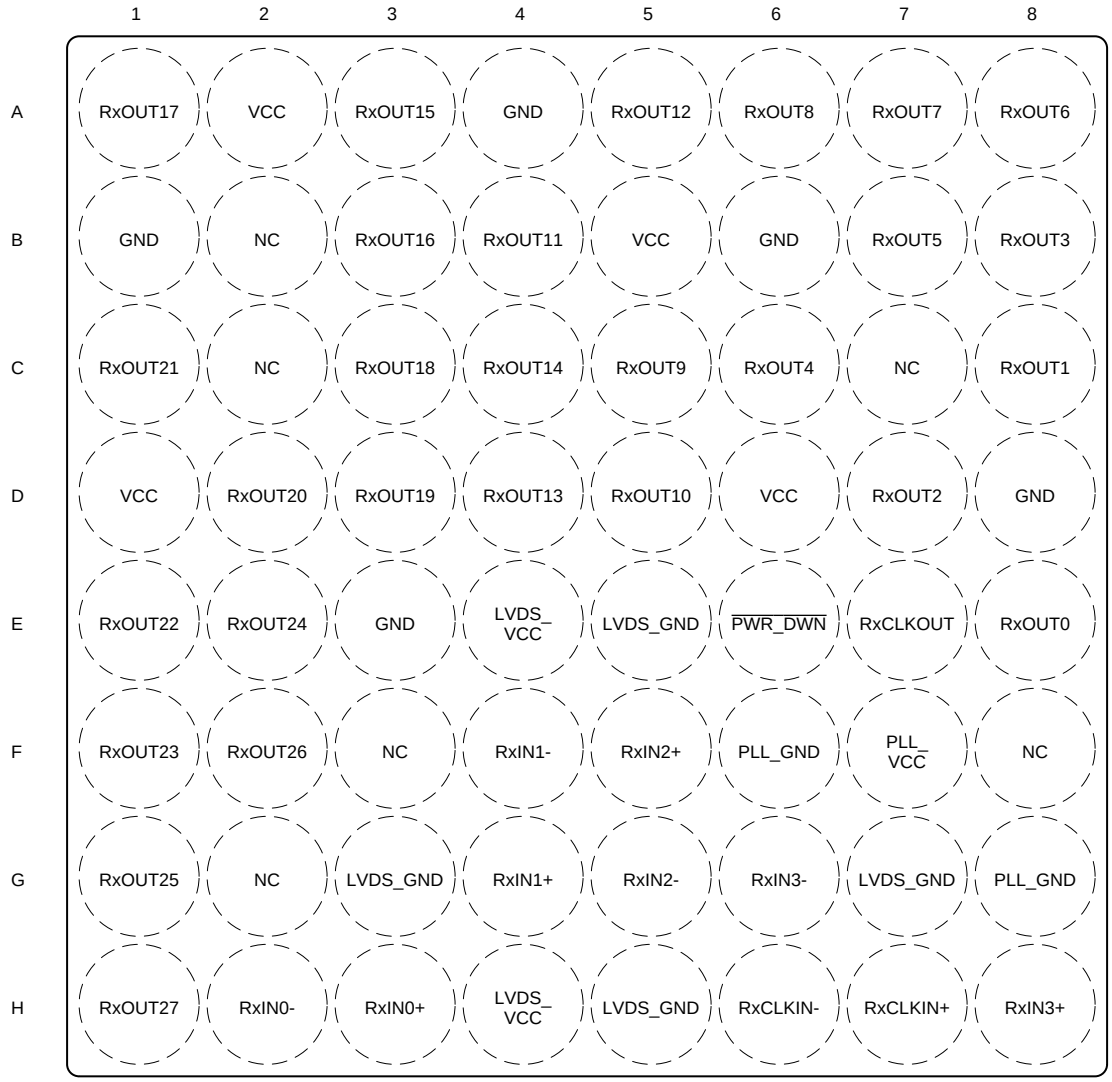
**NZC Package**
**64-Pin NFBGA**
**Top View**

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## Pin Functions

| PIN | | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DS90CF366 | DS90CF386 | | | |
| | TSSOP | TSSOP | NFBGA | | |
| GND | 3, 25, 32, 38, 44 | 4, 28, 36, 44, 52 | A4, B1, B6, D8, E3 | G | Ground pins for LVCMOS outputs. |
| LVDS GND | 7, 13, 18 | 8, 14, 21 | E5, G3, G7, H5 | G | Ground pins for LVDS inputs. |
| LVDS $V_{CC}$ | 12 | 13 | E4, H4 | P | Power supply pin for LVDS inputs. |
| NC | 6 | — | B2, C2, C7, F3, F8, G2 | — | Pins not connected. |
| PLL GND | 19, 21 | 22, 24 | F6, G8 | G | Ground pin for PLL. |
| PLL $V_{CC}$ | 20 | 23 | F7 | P | Power supply for PLL. |

(1) G = Ground, I = Input, O = Output, and P = Power

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## Pin Functions (continued)

| PIN | | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DS90CF366 | DS90CF386 | | | |
| | TSSOP | TSSOP | NFBGA | | |
| $\overline{\text{PWR DWN}}$ | 22 | 25 | E6 | I | LVCMOS level input. When asserted (low input) the receiver outputs are low. |
| RxCLKIN+ | 17 | 18 | H7 | I | Positive LVDS differential clock input. |
| RxCLKIN- | 16 | 17 | H6 | I | Negative LVDS differential clock input. |
| RxCLKOUT | 23 | 26 | E7 | O | LVCMOS level clock output. The falling edge acts as data strobe. |
| RxIN0+ | 9 | 10 | H3 | I | Positive LVDS differential data inputs. |
| RxIN0- | 8 | 9 | H2 | I | Negative LVDS differential data inputs. |
| RxIN1+ | 11 | 12 | G4 | I | Positive LVDS differential data inputs. |
| RxIN1- | 10 | 11 | F4 | I | Negative LVDS differential data inputs. |
| RxIN2+ | 15 | 16 | F5 | I | Positive LVDS differential data inputs. |
| RxIN2- | 14 | 15 | G5 | I | Negative LVDS differential data inputs. |
| RxIN3+ | — | 20 | H8 | I | Positive LVDS differential data inputs. |
| RxIN3- | — | 19 | G6 | I | Negative LVDS differential data inputs. |
| RxOUT0 | 24 | 27 | E8 | O | LVCMOS level data output. |
| RxOUT1 | 26 | 29 | C8 | O | LVCMOS level data output. |
| RxOUT2 | 27 | 30 | D7 | O | LVCMOS level data output. |
| RxOUT3 | 29 | 32 | B8 | O | LVCMOS level data output. |
| RxOUT4 | 30 | 33 | C6 | O | LVCMOS level data output. |
| RxOUT5 | 31 | 34 | B7 | O | LVCMOS level data output. |
| RxOUT6 | 33 | 35 | A8 | O | LVCMOS level data output. |
| RxOUT7 | 34 | 37 | A7 | O | LVCMOS level data output. |
| RxOUT8 | 35 | 38 | A6 | O | LVCMOS level data output. |
| RxOUT9 | 37 | 39 | C5 | O | LVCMOS level data output. |
| RxOUT10 | 39 | 41 | D5 | O | LVCMOS level data output. |
| RxOUT11 | 40 | 42 | B4 | O | LVCMOS level data output. |
| RxOUT12 | 41 | 43 | A5 | O | LVCMOS level data output. |
| RxOUT13 | 43 | 45 | D4 | O | LVCMOS level data output. |
| RxOUT14 | 45 | 46 | C4 | O | LVCMOS level data output. |
| RxOUT15 | 46 | 47 | A3 | O | LVCMOS level data output. |
| RxOUT16 | 47 | 49 | B3 | O | LVCMOS level data output. |
| RxOUT17 | 1 | 50 | A1 | O | LVCMOS level data output. |
| RxOUT18 | 2 | 51 | C3 | O | LVCMOS level data output. |
| RxOUT19 | 4 | 53 | D3 | O | LVCMOS level data output. |
| RxOUT20 | 5 | 54 | D2 | O | LVCMOS level data output. |
| RxOUT21 | — | 55 | C1 | O | LVCMOS level data output. |
| RxOUT22 | — | 1 | E1 | O | LVCMOS level data output. |
| RxOUT23 | — | 2 | F1 | O | LVCMOS level data output. |
| RxOUT24 | — | 3 | E2 | O | LVCMOS level data output. |
| RxOUT25 | — | 5 | G1 | O | LVCMOS level data output. |
| RxOUT26 | — | 6 | F2 | O | LVCMOS level data output. |
| RxOUT27 | — | 7 | H1 | O | LVCMOS level data output. |
| $V_{CC}$ | 28, 36, 42, 48 | 31, 40, 48, 56 | A2, B5, D1, D6 | P | Power supply pins for LVCMOS outputs. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | –0.3 | 4 | V |
| CMOS/LVCMOS output voltage | | | –0.3 | $V_{CC}$ + 0.3 | V |
| LVDS receiver input voltage | | | –0.3 | $V_{CC}$ + 0.3 | V |
| Power dissipation capacity at 25°C | DS90CF366, TSSOP package | | | 1.61 | W |
| | DS90CF386 | TSSOP package | | 1.89 | |
| | | NFBGA package | | 2 | |
| Lead temperature | TSSOP soldering (4 s) | | | 260 | °C |
| | NFBGA soldering, reflow (20 s) | | | 220 | |
| Operating junction temperature, $T_J$ | | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±7000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±700 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| | Receiver input | 0 | | 2.4 | V |
| $V_{NOISE}$ | Supply noise voltage | | | 100 | $mV_{PP}$ |
| $T_A$ | Operating free-air temperature | –10 | 25 | 70 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DS90CF366 | DS90CF386 | | UNIT |
|---|---|---|---|---|---|
| | | DGG (TSSOP) | DGG (TSSOP) | NZC (NFBGA) | |
| | | 48 PINS | 56 PINS | 64 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 67.8 | 64.6 | 65.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 22.1 | 20.6 | 23.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 34.8 | 33.3 | 44.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.1 | 1 | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 34.5 | 33 | 44.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LVCMOS DC SPECIFICATIONS** | | | | | | | |
| $V_{IH}$ | High level input voltage | | | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low level input voltage | | | GND | | 0.8 | V |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –0.4 mA | | 2.7 | 3.3 | | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 2 mA | | | 0.06 | 0.3 | V |
| $V_{CL}$ | Input clamp voltage | $I_{CL}$ = –18 mA | | | –0.79 | –1.5 | V |
| $I_{IN}$ | Input current | $V_{IN}$ = 0.4 V, 2.5 V or $V_{CC}$ | | | 1.8 | 15 | uA |
| | | $V_{IN}$ = GND | | –10 | 0 | | uA |
| $I_{OS}$ | Output short circuit current | $V_{OUT}$ = 0 V | | | –60 | –120 | mA |
| **LVDS RECEIVER DC SPECIFICATIONS** | | | | | | | |
| $V_{TH}$ | Differential input high threshold | $V_{CM}$ = 1.2 V | | | | 100 | mV |
| $V_{TL}$ | Differential input low threshold | | | –100 | | | mV |
| $I_{IN}$ | Input current | $V_{IN}$ = 2.4 V, $V_{CC}$ = 3.6 V | | | | ±10 | µA |
| | | $V_{IN}$ = 0 V, $V_{CC}$ = 3.6 V | | | | ±10 | µA |
| **RECEIVER SUPPLY CURRENT** | | | | | | | |
| ICCRW | Receiver supply current worst case | $C_L$ = 8 pF, worst case pattern, DS90CF386, see Figure 1 and Figure 4 | f = 32.5 MHz | | 49 | 70 | mA |
| | | | f = 37.5 MHz | | 53 | 75 | mA |
| | | | f = 65 MHz | | 81 | 114 | mA |
| | | | f = 85 MHz | | 96 | 135 | mA |
| | | $C_L$ = 8 pF, worst case pattern, DS90CF366, see Figure 1 and Figure 4 | f = 32.5 MHz | | 49 | 60 | mA |
| | | | f = 37.5 MHz | | 53 | 65 | mA |
| | | | f = 65 MHz | | 78 | 100 | mA |
| | | | f = 85 MHz | | 90 | 115 | mA |
| ICCRG | Receiver supply current, 16 grayscale | $C_L$ = 8 pF, 16 grayscale pattern, see Figure 2, Figure 3, and Figure 4 | f = 32.5 MHz | | 28 | 45 | mA |
| | | | f = 37.5 MHz | | 30 | 47 | mA |
| | | | f = 65 MHz | | 43 | 60 | mA |
| | | | f = 85 MHz | | 43 | 70 | mA |
| ICCRZ | Receiver supply current power down(2) | $\overline{\text{Power Down}}$ = low receiver outputs stay low during power down mode | | | 140 | 400 | µA |

(1) Typical values are given for $V_{CC}$ = 3.3 V and $T_A$ = 25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except $V_{OD}$ and $\Delta V_{OD}$).


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## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| CLHT | CMOS or LVCMOS low-to-high transition time | See Figure 4 | | 2 | 3.5 | ns |
| CHLT | CMOS or LVCMOS high-to-low transition time | See Figure 4 | | 1.8 | 3.5 | ns |
| RSPos0 | Receiver input strobe position for bit 0 | f = 85 MHz, see Figure 11 and Figure 12 | 0.49 | 0.84 | 1.19 | ns |
| RSPos1 | Receiver input strobe position for bit 1 | f = 85 MHz | 2.17 | 2.52 | 2.87 | ns |
| RSPos2 | Receiver input strobe position for bit 2 | f = 85 MHz | 3.85 | 4.2 | 4.55 | ns |
| RSPos3 | Receiver input strobe position for bit 3 | f = 85 MHz | 5.53 | 5.88 | 6.23 | ns |
| RSPos4 | Receiver input strobe position for bit 4 | f = 85 MHz | 7.21 | 7.56 | 7.91 | ns |
| RSPos5 | Receiver input strobe position for bit 5 | f = 85 MHz | 8.89 | 9.24 | 9.59 | ns |
| RSPos6 | Receiver input strobe position for bit 6 | f = 85 MHz | 10.57 | 10.92 | 11.27 | ns |
| RSKM | RxIN skew margin(2) | f = 85 MHz, see Figure 13 | 290 | | | ps |
| RCOP | RxCLK OUT period | See Figure 5 | 11.76 | T | 50 | ns |
| RCOH | RxCLK OUT high time | f = 85 MHz, see Figure 5 | 4.5 | 5 | 7 | ns |
| RCOL | RxCLK OUT low time | f = 85 MHz, see Figure 5 | 4 | 5 | 6.5 | ns |
| RSRC | RxOUT setup to RxCLK OUT | f = 85 MHz, see Figure 5 | 2 | | | ns |
| RHRC | RxOUT hold to RxCLK OUT | f = 85 MHz, see Figure 5 | 3.5 | | | ns |
| RCCD | RxCLK IN to RxCLK OUT delay | 25°C, $V_{CC}$ = 3.3 V, see Figure 6 | 5.5 | 7 | 9.5 | ns |
| RPLLS | Receiver phase lock loop set | See Figure 7 | | | 10 | ms |
| RPDD | Receiver power down delay | See Figure 10 | | | 1 | µs |

(1) Typical values are given for $V_{CC}$ = 3.3 V and $T_A$ = 25°C.
(2) Receiver skew margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 150 ps).

## 6.7 Timing Diagrams

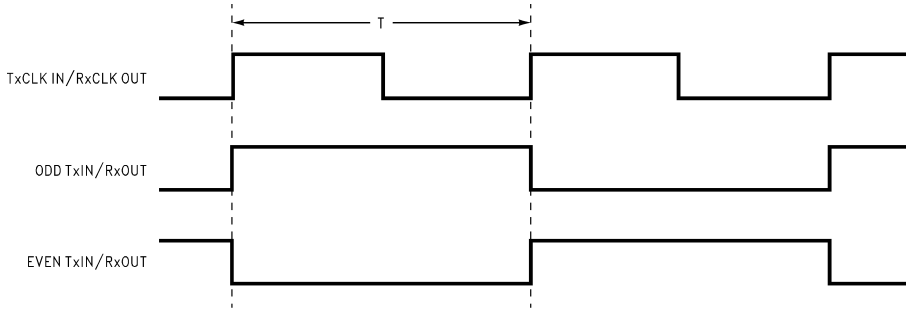


**Figure 1. Test Pattern, Worst Case**

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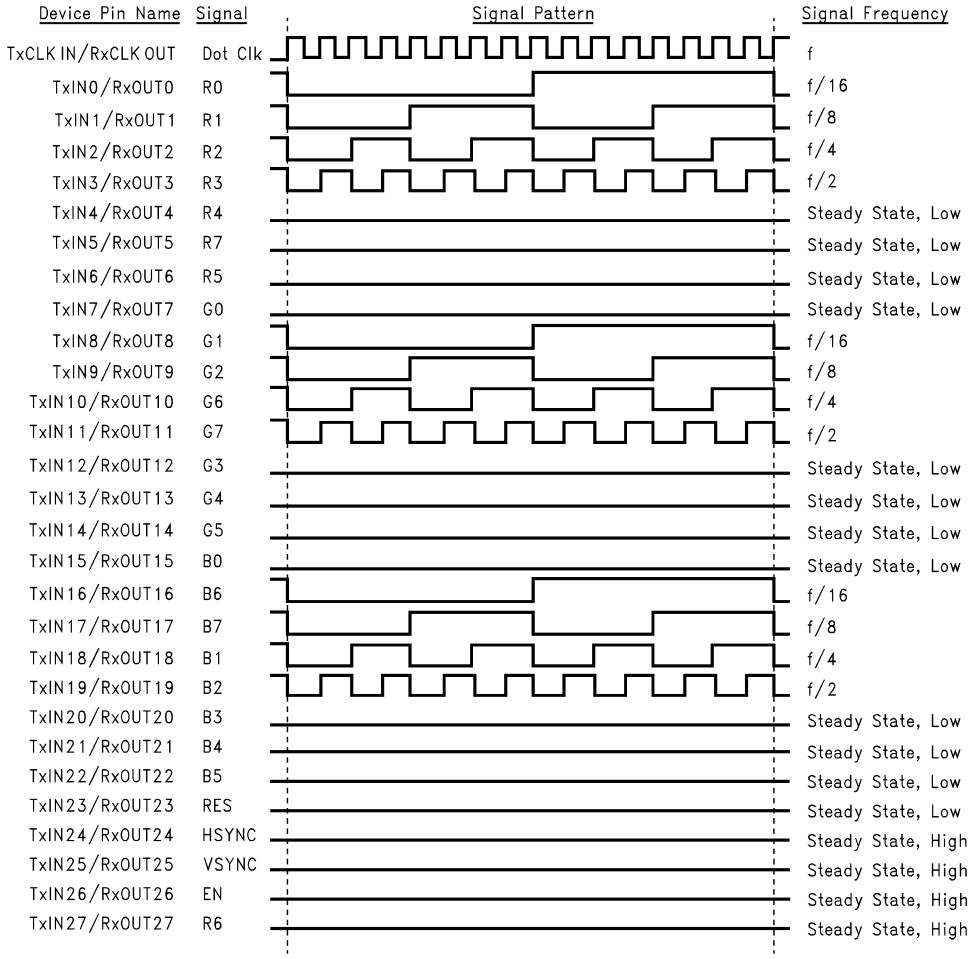
## Timing Diagrams (continued)




(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O, and CMOS or LVCMOS I/O.

(2) The 16 grayscale test pattern tests device power consumption for a *typical* LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

(3) Figure 1 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

**Figure 2. Test Pattern, 16 Grayscale (DS90CF386)**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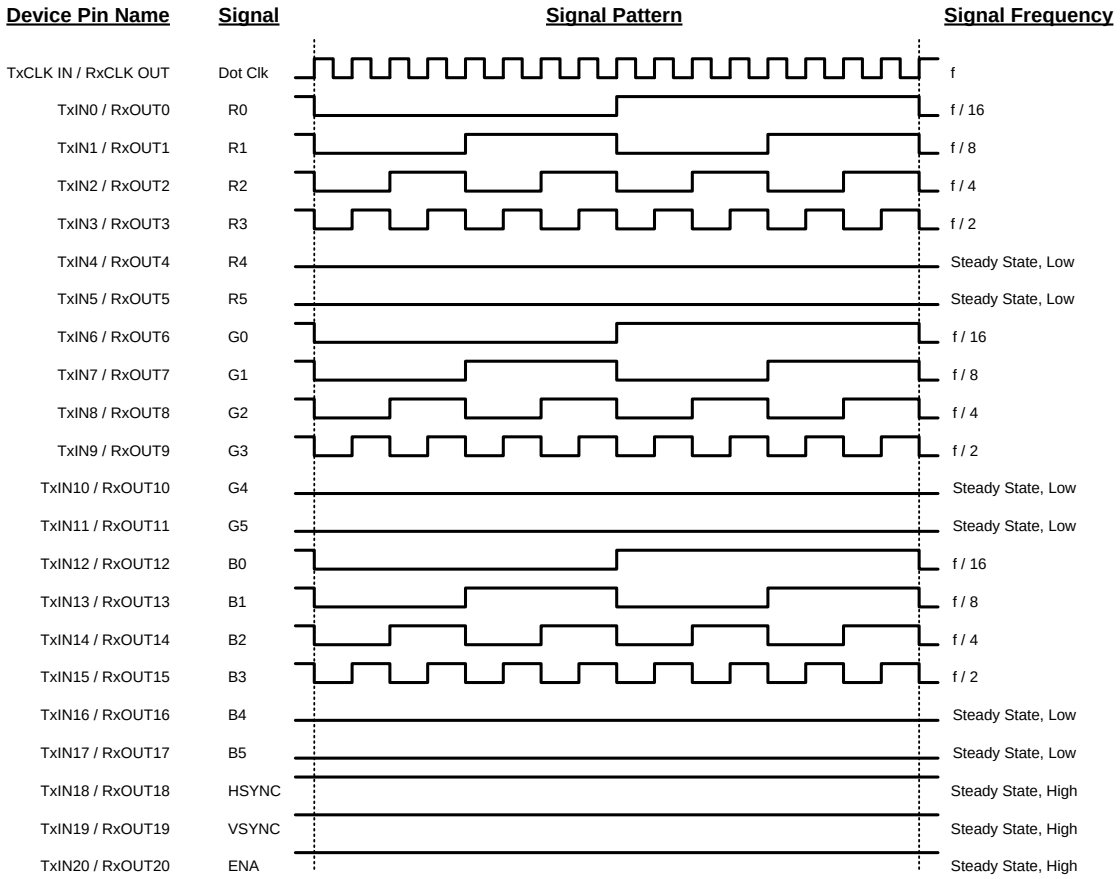
## Timing Diagrams (continued)

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(3) Figure 1 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

**Figure 3. Test Pattern, 16 Grayscale (DS90CF366)**

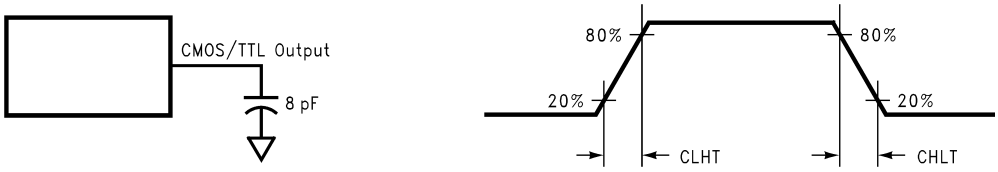


**Figure 4. DS90CF3x6 (Receiver) CMOS or LVCMOS Output Load and Transition Times**

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## Timing Diagrams (continued)

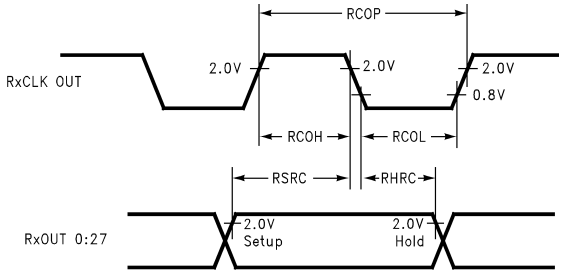


**Figure 5. DS90CF3x6 (Receiver) Setup or Hold and High or Low Times**

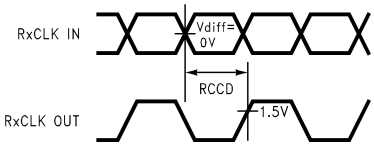


**Figure 6. DS90CF3x6 (Receiver) Clock In to Clock Out Delay**

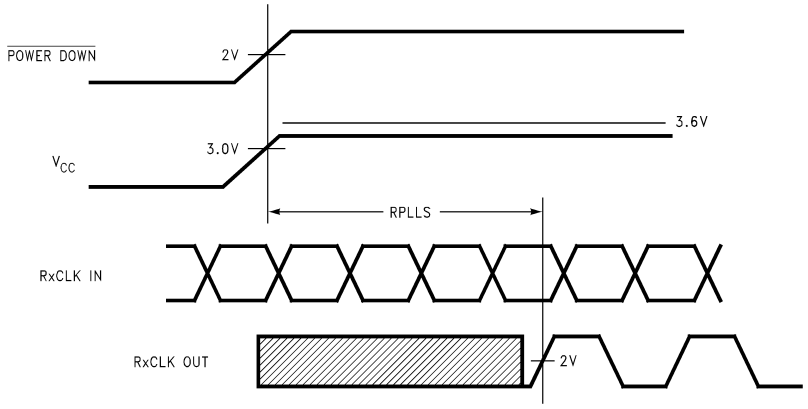


**Figure 7. DS90CF3x6 (Receiver) Phase Lock Loop Set Time**

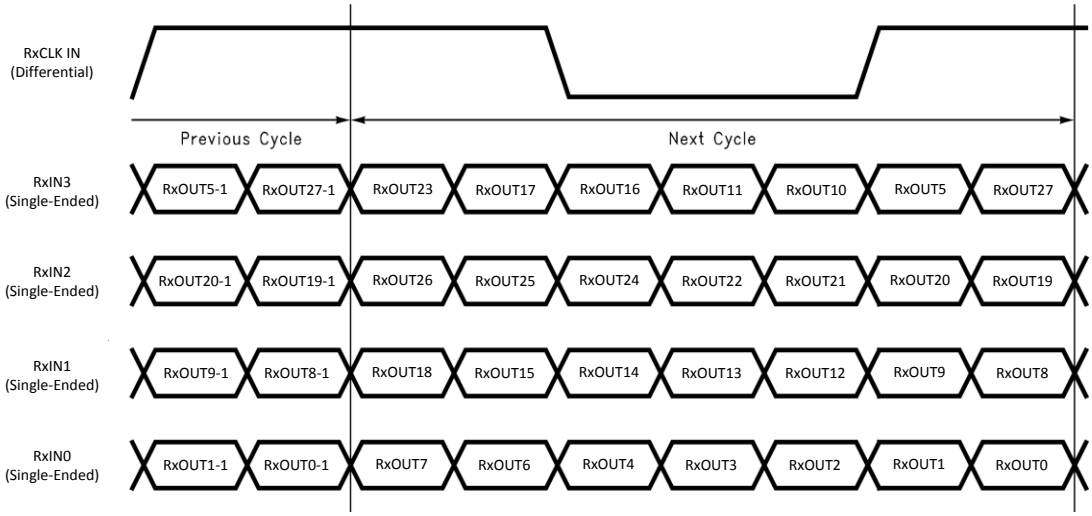


**Figure 8. DS90CF386 Mapping of 28 LVCMOS Parallel Data to 4D + C LVDS Serialzied Data**


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## Timing Diagrams (continued)

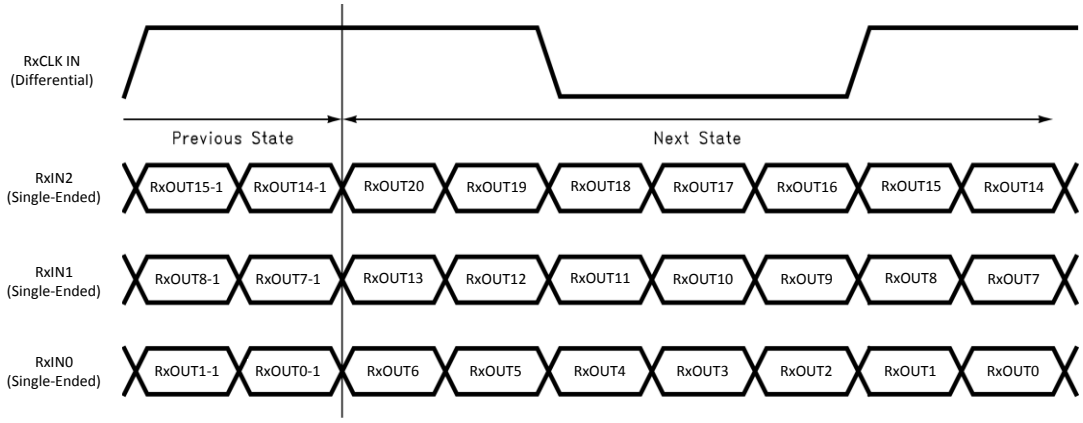


**Figure 9. DS90CF366 Mapping of 21 LVCMOS Parallel Data to 3D + C LVDS Serialized Data**

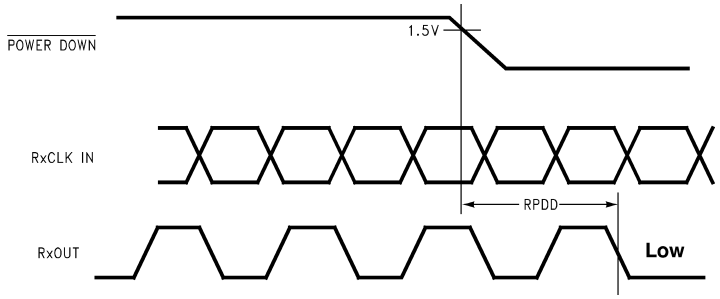


**Figure 10. DS90CF3x6 (Receiver) Power Down Delay**

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## Timing Diagrams (continued)

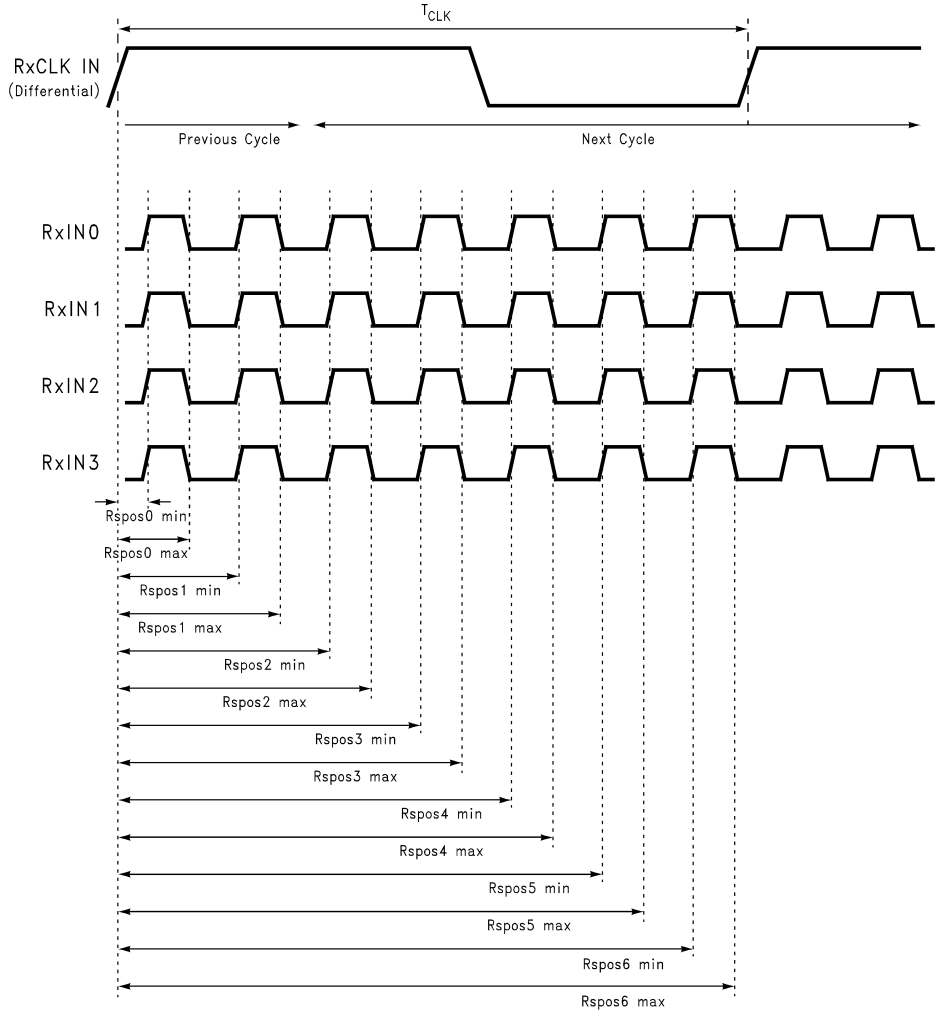


**Figure 11. DS90CF386 (Receiver) LVDS Input Strobe Position**


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## Timing Diagrams (continued)

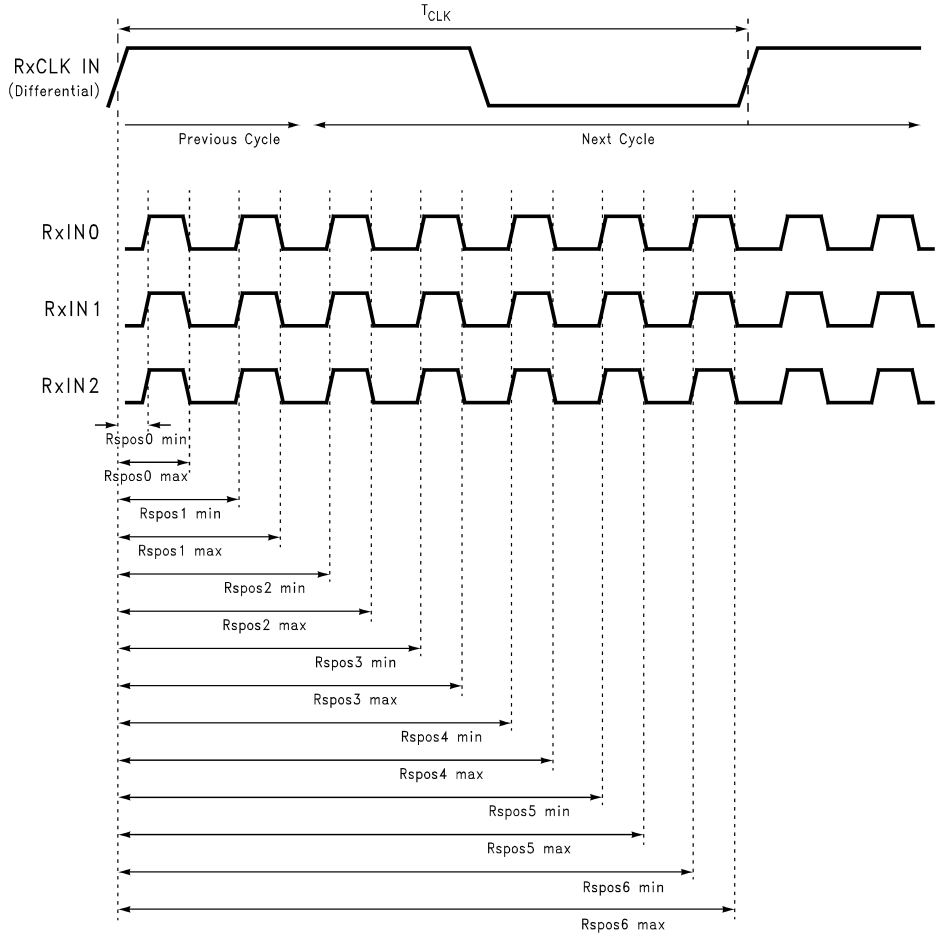
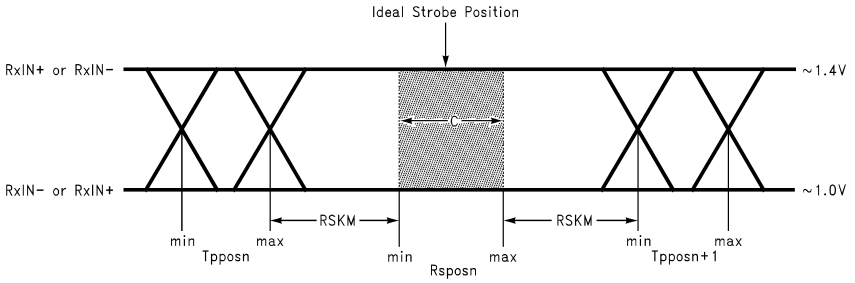



**Figure 12. DS90CF366 (Receiver) LVDS Input Strobe Position**




C: Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos: Transmitter output pulse position (min and max)
Cable skew: Typically 10 ps–40 ps per foot, media dependent
RSKM = Cable skew (type, length) + source clock jitter (cycle-to-cycle)(1) + ISI (inter-symbol interference)(2)

(1) Cycle-to-cycle jitter depends on the Tx source. Clock jitter should be maintained to less than 250 ps at 85 MHz.

(2) ISI is dependent on interconnect length; may be zero.

**Figure 13. Receiver LVDS Input Skew Margin**

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## 6.8 Typical Characteristics

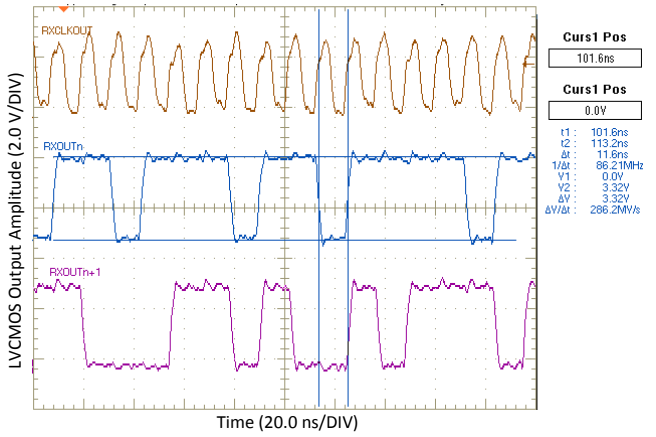


**Figure 14. Parallel PRBS-7 on LVCMOS Outputs at 85 MHz**

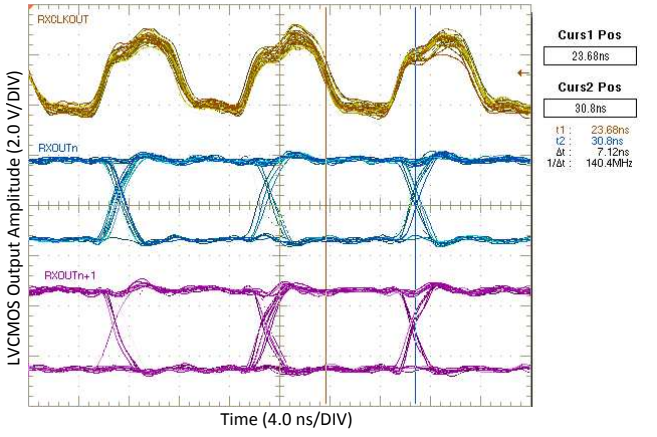


**Figure 15. Typical RxOUT Strobe Position at 85 MHz**

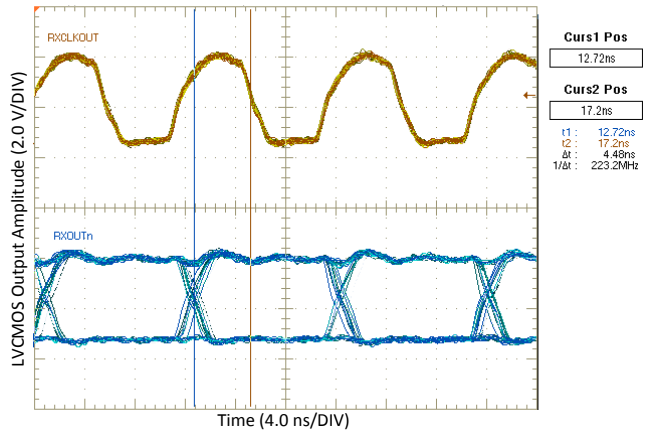


**Figure 16. Typical RxOUT Setup Time at 85 MHz (RSRC = 4.5 ns)**

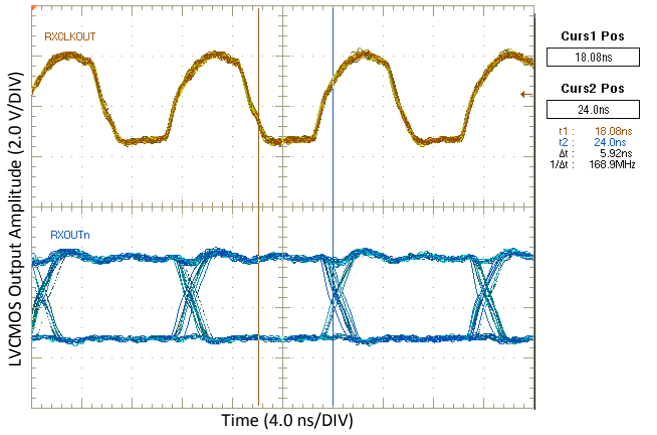


**Figure 17. Typical RxOUT Hold Time at 85 MHz (RHRC = 5.9 ns)**


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# 7 Detailed Description

## 7.1 Overview

The DS90CF386 is a receiver that converts four LVDS (Low Voltage Differential Signaling) data streams into parallel 28 bits of LVCMOS data (24 bits of RGB and 4 bits of HSYNC, VSYNC, DE, and CNTL). The DS90CF366 is a receiver that converts three LVDS data streams into parallel 21 bits of LVCMOS data (18 bits of RGB and 3 bits of HSYNC, VSYNC, and DE). An internal PLL locks to the incoming LVDS clock ranging from 20 to 85 MHz. The locked PLL ensures a stable clock to sample the output LVCMOS data on the Receiver Clock Out falling edge. These devices feature a PWR DWN pin to put the device into low power mode when there is no active input data.

## 7.2 Functional Block Diagrams

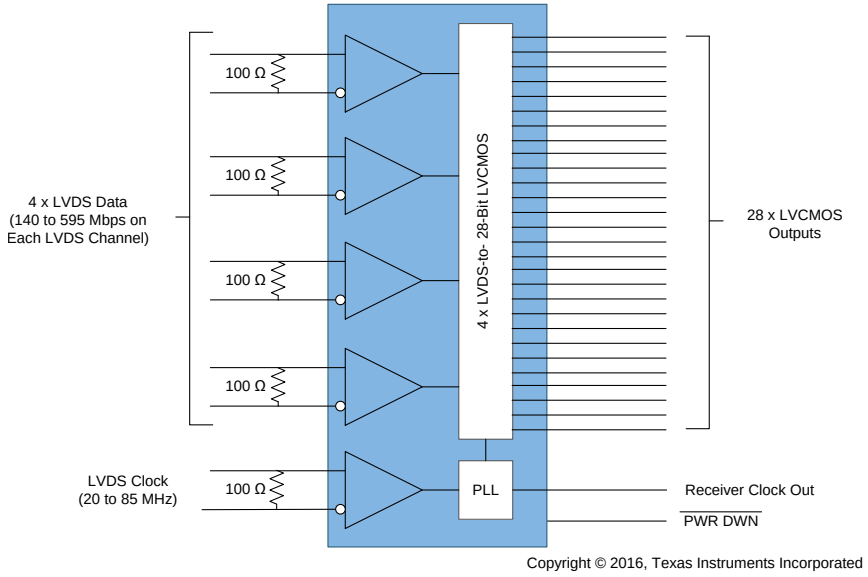


**Figure 18. DS90CF386 Block Diagram**

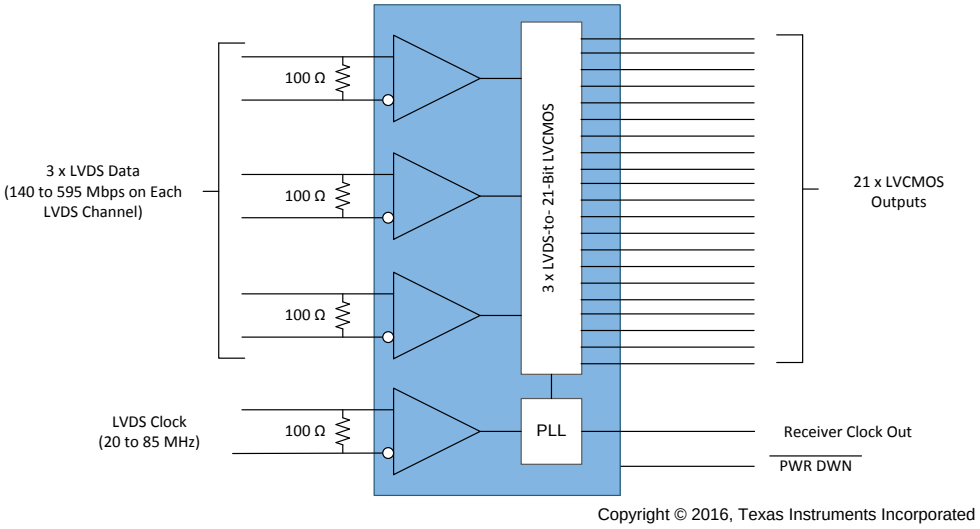


**Figure 19. DS90CF366 Block Diagram**

## 7.3 Feature Description

The DS90CF386 and DS90CF366 consist of several key blocks:

- LVDS Receivers
- Phase Locked Loop (PLL)
- Serial LVDS-to-Parallel LVCMOS Converter
- LVCMOS Drivers

### 7.3.1 LVDS Receivers

There are five differential LVDS inputs to the DS90CF386 and four differential LVDS inputs to the DS90CF366. For the DS90CF386, four of the LVDS inputs contain serialized data originating from a 28-bit source transmitter. For the DS90CF366, three of the LVDS inputs contain serialized data originating from a 21-bit source transmitter. The remaining LVDS input contains the LVDS clock associated with the data pairs.

#### *7.3.1.1 LVDS Input Termination*

The DS90CF386 and DS90CF366 require a single 100-Ω terminating resistor across the true and complement lines on each differential pair of the receiver input. To prevent reflections due to stubs, this resistor should be placed as close to the device input pins as possible. Figure 20 shows an example.

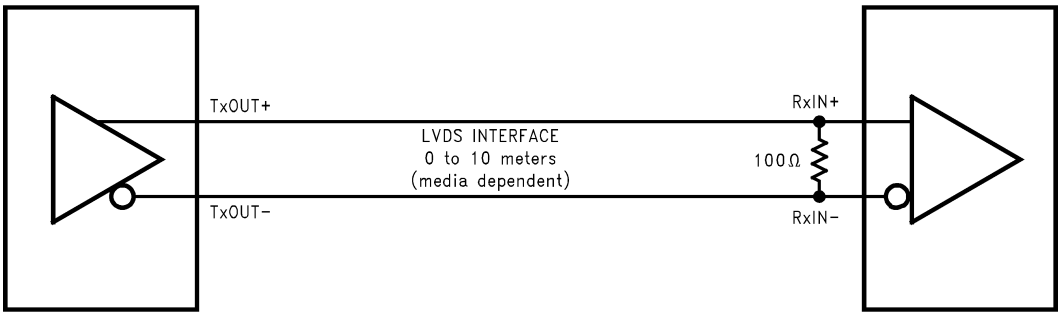


**Figure 20. LVDS Serialized Link Termination**

### 7.3.2 Phase Locked Loop (PLL)

The FPD Link I devices use an internal PLL to recover the clock transmitted across the LVDS interface. The recovered clock is then used as a reference to determine the sampling position of the seven serial bits received per clock cycle. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another), and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Individual bypassing of each $V_{CC}$ to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock to improve the overall jitter budget.

### 7.3.3 Serial LVDS-to-Parallel LVCMOS Converter

After the PLL locks to the incoming LVDS clock, the receiver deserializes each LVDS differential data pair into seven parallel LVCMOS data outputs per clock cycle. For the DS90CF386, the LVDS data inputs map to LVCMOS outputs according to Figure 8. For the DS90CF366, the LVDS data inputs map to LVCMOS outputs according to Figure 9.

### 7.3.4 LVCMOS Drivers

The LVCMOS outputs from the DS90CF386 and DS90CF366 are the deserialized parallel single-ended data from the serialized LVDS differential data pairs. Each LVCMOS output is clocked by the PLL and strobes on the RxCLKOUT falling edge. All unused DS90CF386 and DS90CF366 RxOUT outputs can be left floating.


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## 7.4 Device Functional Modes

### 7.4.1 Power Sequencing and Power-Down Mode

The DS90CF386 and DS90CF366 may be placed into a power down mode at any time by asserting the $\overline{\text{PWR DWN}}$ pin (active low). The DS90CF386 and DS90CF366 are also designed to protect themselves from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are controlled by a failsafe bias circuitry. The LVDS inputs are High-Z during initial power on and power off conditions. Current is limited to 5 mA per input, thus avoiding the potential for latch-up when powering the device.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DS90F386 and DS90CF366 are designed for a wide variety of data transmission applications. The use of serialized LVDS data lines in these applications allows for efficient signal transmission over a narrow bus width, thereby reducing cost, power, and space.

## 8.2 Typical Applications

Figure 21 and Figure 22 show typical applications of the DS90CF386 and DS90CF366 for displays when used as an OpenLDI-to-RGB bridge.

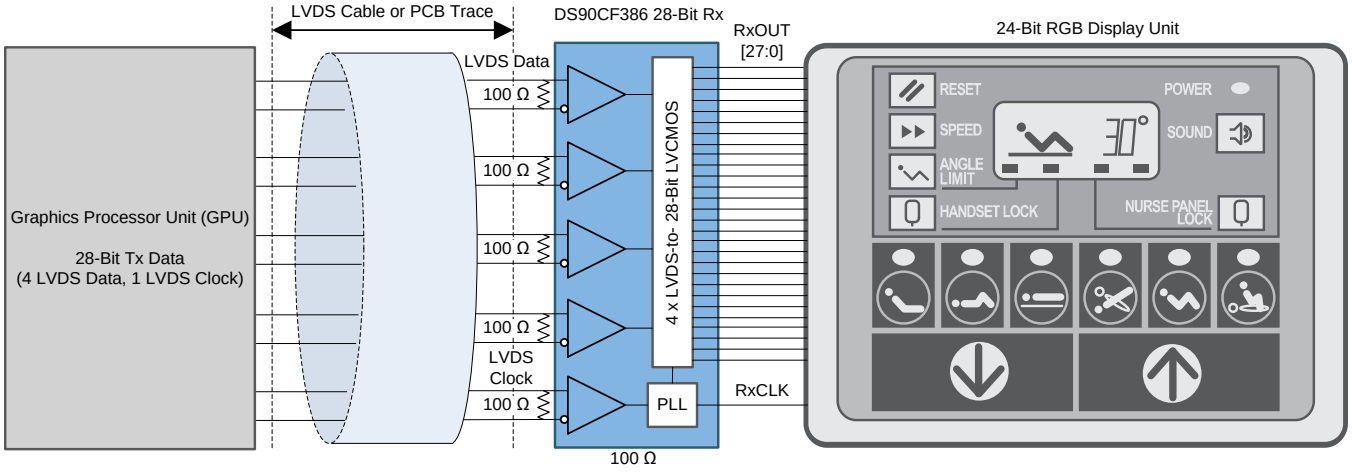


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**Figure 21. Typical DS90CF386 Application Block Diagram**

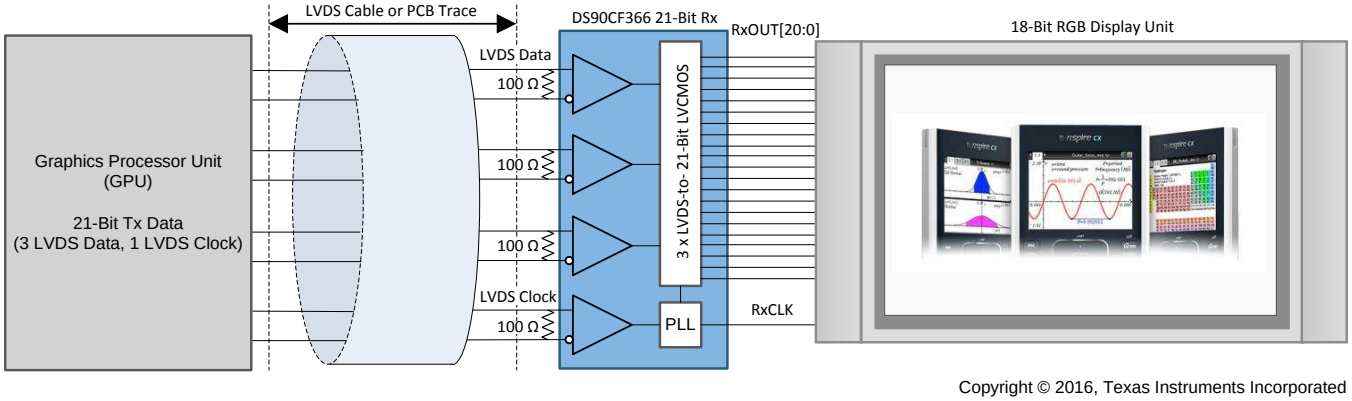


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**Figure 22. Typical DS90CF366 Application Block Diagram**


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## Typical Applications (continued)

### 8.2.1 Design Requirements

For this design example, follow the requirements in Table 1.

**Table 1. Design Parameters**

| PARAMETER | DESIGN REQUIREMENTS |
|---|---|
| Operating frequency | LVDS clock must be within 20 MHz to 85 MHz. |
| Bit resolution | DS90CF386: No higher than 24 bpp. The maximum supported resolution is 8-bit RGB.<br>DS90CF366: No higher than 18 bpp. The maximum supported resolution is 6-bit RGB. |
| Bit data mapping | Determine the appropriate mapping required by the panel display following the DS90CF386 or DS90CF366 outputs. |
| RSKM (Receiver skew margin) | Ensure that there is acceptable margin between Tx pulse position and Rx strobe position. |
| Input termination for RxIN± | Inputs require a 100 Ω ± 10% resistor across each LVDS differential pair. Place as close as possible to IC input pins. |
| RxIN± board trace impedance | Design differential trace impedance with 100 Ω ±5% |
| LVCMOS outputs | If unused, leave pins floating. Series resistance on each LVCMOS output optional to reduce reflections from long board traces. If used, 33-Ω series resistance is typical. |
| DC power supply coupling capacitors | Use a 0.1-µF capacitor to minimize power supply noise. Place as close as possible to $V_{CC}$ pins. |

### 8.2.2 Detailed Design Procedure

To design with the DS90CF386 or DS90CF366, determine the following:

- Cable Interface
- Bit Resolution and Operating Frequency
- Bit Mapping from Receiver to Endpoint Panel Display
- RSKM Interoperability with Transmitter Pulse Position Margin

#### *8.2.2.1 Cables*

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The DS90CF366 requires four pairs of signal wires and the DS90CF386 requires five pairs of signal wires. The ideal cable interface has a constant 100-Ω differential impedance throughout the path. It is also recommended that cable skew remain below 120 ps (assuming 85 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

Depending upon the application and data rate, the interconnecting media between Tx and Rx may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed or long distance applications, the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). For example, twin-coax cables have been demonstrated at distances as long as five meters and with the maximum data transfer of 2.38 Gbps (DS90CF366) and 1.785 Gbps (DS90CF386).

#### *8.2.2.2 Bit Resolution and Operating Frequency Compatibility*

The bit resolution of the endpoint panel display reveals whether there are enough bits available in the DS90CF386 or DS90CF366 to output the required data per pixel. The DS90CF386 has 28 parallel LVCMOS outputs and can therefore provide a bit resolution up to 24 bpp (bits per pixel). In each clock cycle, the remaining bits are the three control signals (HSync, VSync, DE) and one spare bit. The DS90CF366 has 21 parallel LVCMOS outputs and can therefore provide a bit resolution up to 18 bpp (bits per pixel). In each clock cycle, the remaining bits are the three control signals (HSync, VSync, DE).

The number of pixels per frame and the refresh rate of the endpoint panel display indicate the required operating frequency of the deserializer clock. To determine the required clock frequency, refer to Equation 1.

$$f_Clk = [H_Active + H_Blank] \times [V_Active + V_Blank] \times f_Vertical$$

where

- H_Active = Active Display Horizontal Lines

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- H_Blank = Blanking Period Horizontal Lines
- V_Active = Active Display Vertical Lines
- V_Blank = Blanking Period Vertical Lines
- f_Vertical = Refresh Rate (in Hz)
- f_Clk = Operating Frequency of LVDS clock (1)

In each frame, there is a blanking period associated with horizontal rows and vertical columns that are not actively displayed on the panel. These blanking period pixels must be included to determine the required clock frequency. Consider the following example to determine the required LVDS clock frequency:

- H_Active = 640
- H_Blank = 40
- V_Active = 480
- V_Blank = 41
- f_Vertical = 59.95 Hz

Thus, the required operating frequency is determined with Equation 2.

$$[640 + 40] \times [480 + 41] \times 59.95 = 21239086 \text{ Hz} \approx 21.24 \text{ MHz} \quad (2)$$

Since the operating frequency for the PLL in the DS90CF386 and DS90CF366 ranges from 20 to 85 MHz, the DS90CF386 and DS90CF366 can support a panel display with the aforementioned requirements.

If the specific blanking interval is unknown, the number of pixels in the blanking interval can be approximated to 20% of the active pixels. Equation 3 can be used as a conservative approximation for the operating LVDS clock frequency:

$$f_Clk \approx H_Active \times V_Active \times f_Vertical \times 1.2 \quad (3)$$

Using this approximation, the operating frequency for the example in this section is estimated with Equation 4.

$$640 \times 480 \times 59.95 \times 1.2 = 22099968 \text{ Hz} \approx 22.10 \text{ MHz} \quad (4)$$

#### *8.2.2.3 Data Mapping between Receiver and Endpoint Panel Display*

Ensure that the LVCMOS outputs are mapped to align with the endpoint display RGB mapping requirements following the deserializer. See the following for two popular mapping topologies for 8-bit RGB data.

1. LSBs are mapped to RxIN3±.
2. MSBs are mapped to RxIN3±.

Table 2 and Table 3 depict how these two popular topologies can be mapped to the DS90CF386 outputs.

**Table 2. 8-Bit Color Mapping with LSBs on RxIN3±**

| LVDS INPUT CHANNEL | LVDS BIT STREAM POSITION | LVCMOS OUTPUT CHANNEL | COLOR MAPPING | COMMENTS |
|---|---|---|---|---|
| RxIN0 | TxIN0 | RxOUT0 | R2 | |
| | TxIN1 | RxOUT1 | R3 | |
| | TxIN2 | RxOUT2 | R4 | |
| | TxIN3 | RxOUT3 | R5 | |
| | TxIN4 | RxOUT4 | R6 | |
| | TxIN6 | RxOUT6 | R7 | MSB |
| RxIN1 | TxIN7 | RxOUT7 | G2 | |
| | TxIN8 | RxOUT8 | G3 | |
| | TxIN9 | RxOUT9 | G4 | |
| | TxIN12 | RxOUT12 | G5 | |
| | TxIN13 | RxOUT13 | G6 | |
| | TxIN14 | RxOUT14 | G7 | MSB |
| | TxIN15 | RxOUT15 | B2 | |
| | TxIN18 | RxOUT18 | B3 | |


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**Table 2. 8-Bit Color Mapping with LSBs on RxIN3± (continued)**

| LVDS INPUT CHANNEL | LVDS BIT STREAM POSITION | LVCMOS OUTPUT CHANNEL | COLOR MAPPING | COMMENTS |
|---|---|---|---|---|
| RxIN2 | TxIN19 | RxOUT19 | B4 | |
| | TxIN20 | RxOUT20 | B5 | |
| | TxIN21 | RxOUT21 | B6 | |
| | TxIN22 | RxOUT22 | B7 | MSB |
| | TxIN24 | RxOUT24 | HSYNC | Horizontal sync |
| | TxIN25 | RxOUT25 | VSYNC | Vertical sync |
| | TxIN26 | RxOUT26 | DE | Data enable |
| RxIN3 | TxIN27 | RxOUT27 | R0 | LSB |
| | TxIN5 | RxOUT5 | R1 | |
| | TxIN10 | RxOUT10 | G0 | LSB |
| | TxIN11 | RxOUT11 | G1 | |
| | TxIN16 | RxOUT16 | B0 | LSB |
| | TxIN17 | RxOUT17 | B1 | |
| | TxIN23 | RxOUT23 | GP | General purpose |

**Table 3. 8-Bit Color Mapping with MSBs on RxIN3±**

| LVDS INPUT CHANNEL | LVDS BIT STREAM POSITION | LVCMOS OUTPUT CHANNEL | COLOR MAPPING | COMMENTS |
|---|---|---|---|---|
| RxIN0 | TxIN0 | RxOUT0 | R0 | LSB |
| | TxIN1 | RxOUT1 | R1 | |
| | TxIN2 | RxOUT2 | R2 | |
| | TxIN3 | RxOUT3 | R3 | |
| | TxIN4 | RxOUT4 | R4 | |
| | TxIN6 | RxOUT6 | R5 | |
| RxIN1 | TxIN7 | RxOUT7 | G0 | LSB |
| | TxIN8 | RxOUT8 | G1 | |
| | TxIN9 | RxOUT9 | G2 | |
| | TxIN12 | RxOUT12 | G3 | |
| | TxIN13 | RxOUT13 | G4 | |
| | TxIN14 | RxOUT14 | G5 | |
| | TxIN15 | RxOUT15 | B0 | LSB |
| | TxIN18 | RxOUT18 | B1 | |
| RxIN2 | TxIN19 | RxOUT19 | B2 | |
| | TxIN20 | RxOUT20 | B3 | |
| | TxIN21 | RxOUT21 | B4 | |
| | TxIN22 | RxOUT22 | B5 | |
| | TxIN24 | RxOUT24 | HSYNC | Horizontal sync |
| | TxIN25 | RxOUT25 | VSYNC | Vertical sync |
| | TxIN26 | RxOUT26 | DE | Data enable |
| RxIN3 | TxIN27 | RxOUT27 | R6 | |
| | TxIN5 | RxOUT5 | R7 | MSB |
| | TxIN10 | RxOUT10 | G6 | |
| | TxIN11 | RxOUT11 | G7 | MSB |
| | TxIN16 | RxOUT16 | B6 | |
| | TxIN17 | RxOUT17 | B7 | MSB |
| | TxIN23 | RxOUT23 | GP | General purpose |

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In the case where either DS90CF386 or DS90CF366 is used to support 18 bpp, Table 2 is commonly used, where RxIN3± (if applicable) is left as *No Connect*. With this mapping, MSBs of RGB data are retained on RXIN0±, RXIN1±, and RXIN2± while the two LSBs for the original 8-bit RGB resolution are ignored from RxIN3±.

#### *8.2.2.4 RSKM Interoperability*

One of the most important factors when designing the receiver into a system application is assessing how much RSKM (Receiver Skew Margin) is available. In each LVDS clock cycle, the LVDS data stream carries seven serialized data bits. Ideally, the Transmit Pulse Position for each bit will occur every (n × T)/7 seconds, where n = Bit Position and T = LVDS Clock Period. Likewise, ideally the Rx Strobe Position for each bit will occur every ((n + 0.5) × T)/7 seconds. However, in real systems, both LVDS Tx and Rx will have non-ideal pulse and strobe position for each bit position due to the effects of cable skew, clock jitter, and ISI. This concept is illustrated in Figure 23.

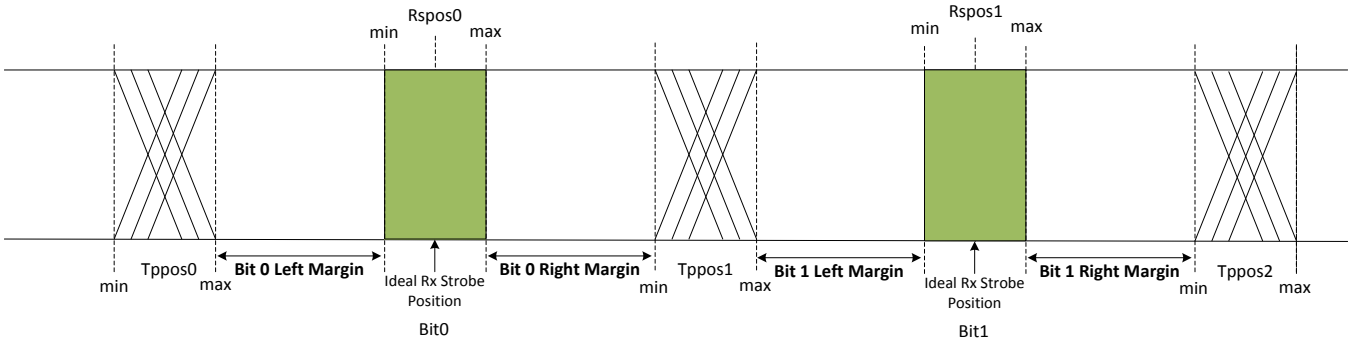


**Figure 23. RSKM Measurement Example**

All left and right margins for Bits 0-6 must be considered in order to determine the absolute minimum for the whole LVDS bit stream. This absolute minimum corresponds to the RSKM.

To improve RSKM performance between LVDS transmitter and receiver, designers often either advance or delay the LVDS clock compared to the LVDS data. Moving the LVDS clock compared to the LVDS data can improve the location of the setup and hold time for the transmitter compared to the setup and hold time for the receiver.

If there is less left bit margin than right bit margin, the LVDS clock can be delayed so that the Rx strobe position for incoming data appears to be delayed. If there is less right bit margin than left bit margin, all the LVDS data pairs can be delayed uniformly so that the LVDS clock and Rx strobe position for incoming data appear to advance. To delay an LVDS data or clock pair, designers either add more PCB trace length or install a capacitor between the LVDS transmitter and receiver. It is important to note that when using these techniques, all serialized bit positions are shifted right or left uniformly.

When designing the DS90CF386 or DS90CF366 receiver with a third-party OpenLDI transmitter, users must calculate the skew margin budget (RSKM) based on the Tx pulse position and the Rx strobe position to ensure error-free transmission. For more information about calculating RSKM, refer to Application Note, *Receiver Skew Margin for Channel Link I and FPD Link I Devices* (SNLA249).


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### 8.2.3 Application Curves

The following application curves are examples taken with a DS90C385A serializer interfacing to a DS90CF386 deserializer with nominal temperature (25ºC) and voltage supply (3.3 V) at an operating frequency of 85 MHz.

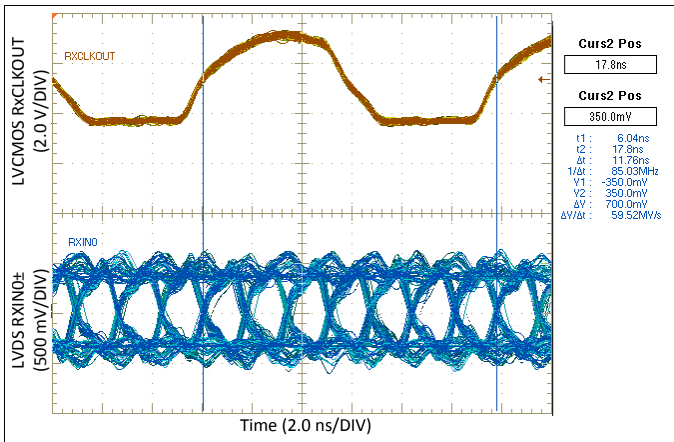


**Figure 24. LVDS RxIN0± Aligned With LVCMOS RxCLKOUT**

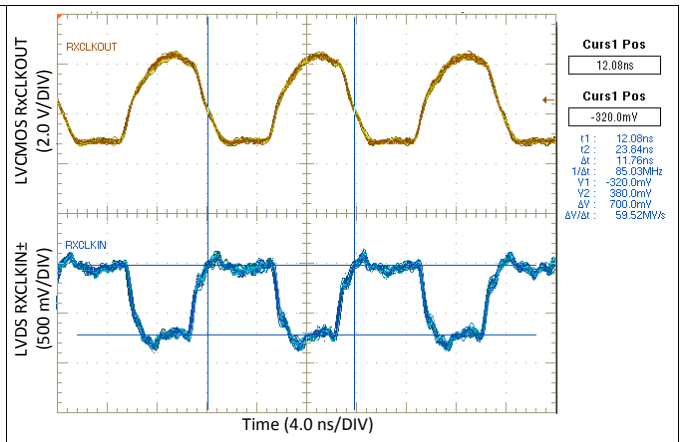


**Figure 25. LVDS CLKIN Aligned With LVCMOS RxCLKOUT**

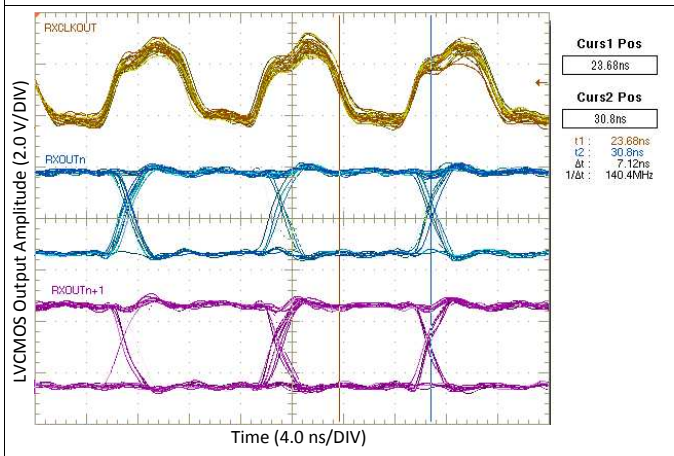


**Figure 26. RxOUT Strobe On Falling Edge Of RxCLKOUT**

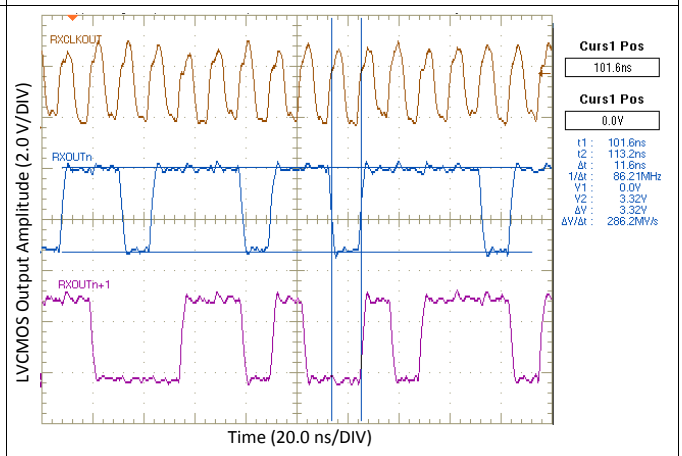


**Figure 27. PRBS-7 Output On RxOUT Channels**

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# 9 Power Supply Recommendations

Proper power supply decoupling is important to ensure a stable power supply with minimal power supply noise. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach, three parallel-connected decoupling capacitors (multi-layered ceramic type in surface mount form factor) between each $V_{CC}$ ($V_{CC}$, PLL $V_{CC}$, LVDS $V_{CC}$) and the ground plane(s) are recommended. The three capacitor values are 0.1 μF, 0.01 μF, and 0.001 μF. The preferred capacitor size is 0402. An example is shown in Figure 28. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. This helps to reduce overall inductance with regards to power supply filtering. If board space is limiting the number of bypass capacitors, the PLL $V_{CC}$ should receive the most filtering. Next would be the LVDS $V_{CC}$ pins and finally the logic $V_{CC}$ pins.

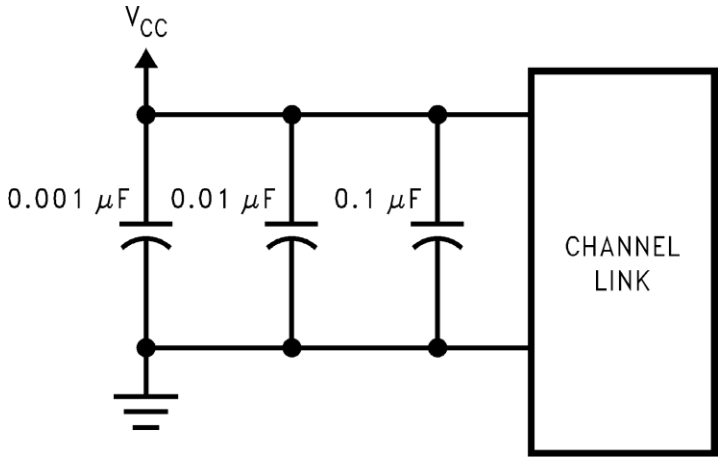


**Figure 28. Recommended Bypass Capacitor Decoupling Configuration for $V_{CC}$, PLL $V_{CC}$, and LVDS $V_{CC}$**

# 10 Layout

## 10.1 Layout Guidelines

As with any high speed design, board designers must maximize signal integrity by limiting reflections and crosstalk that can adversely affect high frequency and EMI performance. The following practices are recommended layout guidelines to optimize device performance.

- Ensure that differential pair traces are always closely coupled to eliminate noise interference from other signals and take full advantage of the common mode noise canceling effect of the differential signals.
- Maintain equal length on signal traces for a given differential pair.
- Limit impedance discontinuities by reducing the number of vias on signal traces.
- Eliminate any 90º angles on traces and use 45º bends instead.
- If a via must exist on one signal polarity, mirror the via implementation on the other polarity of the differential pair.
- Match the differential impedance of the selected physical media. This impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input.
- When possible, use short traces for LVDS inputs.

## 10.2 Layout Examples

The following images show an example layout of the DS90CF386. Traces in blue correspond to the top layer and the traces in green correspond to the bottom layer. Note that differential pair inputs to the DS90CF386 are tightly coupled and close to the connector pins. In addition, observe that the power supply decoupling capacitors are placed as close as possible to the power supply pins with through vias in order to minimize inductance. The principles illustrated in this layout can also be applied to the 48-pin DS90CF366.


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## Layout Examples (continued)

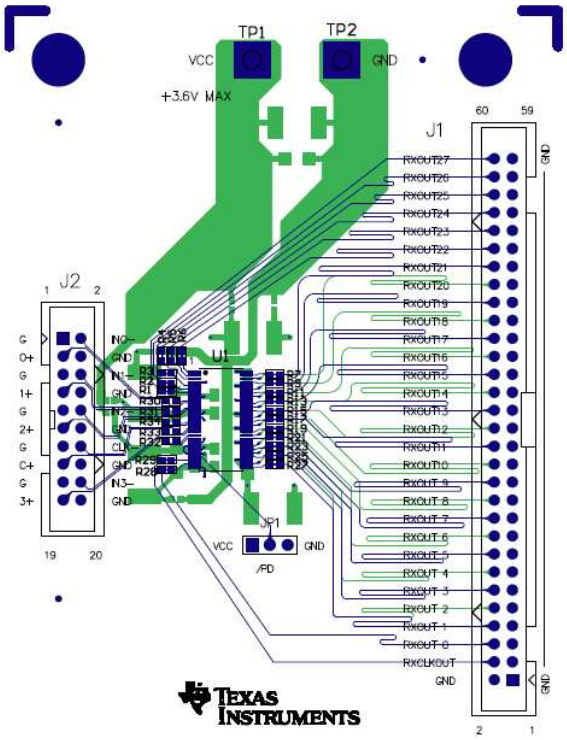


**Figure 29. Example Layout With DS90CF386 (U1)**

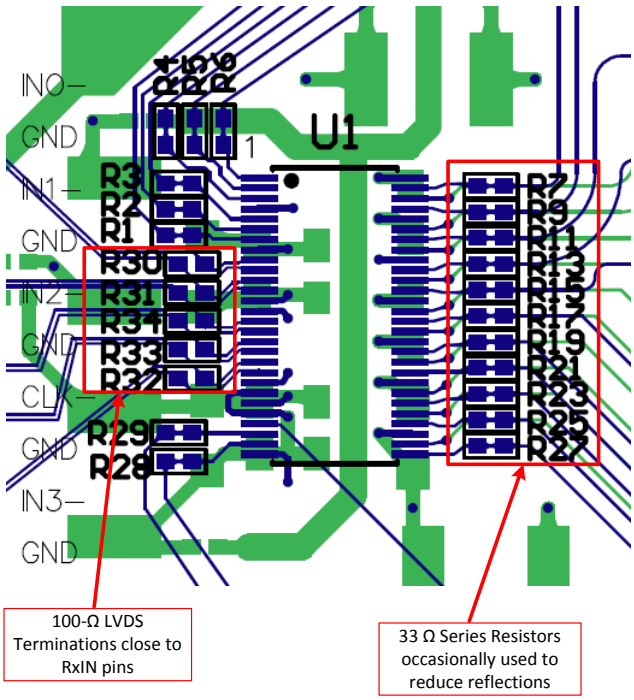


**Figure 30. Example Layout Close-Up**

# 11 デバイスおよびドキュメントのサポート

## 11.1 ドキュメントのサポート

### 11.1.1 関連資料

関連資料については、以下を参照してください。

- アプリケーション・ノート、「チャネル・リンクIおよびFPDリンクIデバイスのレシーバのスキュー・マージン」、SNLA249

## 11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 商標

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## 11.4 静電気放電に関する注意事項

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## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DS90CF366MTD/NOPB | Active | Production | TSSOP (DGG) \| 48 | 38 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF366MTD >B |
| DS90CF366MTD/NOPB.A | Active | Production | TSSOP (DGG) \| 48 | 38 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF366MTD >B |
| DS90CF366MTD/NOPB.B | Active | Production | TSSOP (DGG) \| 48 | 38 \| TUBE | - | Call TI | Call TI | -10 to 70 | |
| DS90CF366MTDX/NOPB | Active | Production | TSSOP (DGG) \| 48 | 1000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF366MTD >B |
| DS90CF366MTDX/NOPB.A | Active | Production | TSSOP (DGG) \| 48 | 1000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF366MTD >B |
| DS90CF366MTDX/NOPB.B | Active | Production | TSSOP (DGG) \| 48 | 1000 \| LARGE T&R | - | Call TI | Call TI | -10 to 70 | |
| DS90CF386MTD/NOPB | Active | Production | TSSOP (DGG) \| 56 | 34 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF386MTD >B |
| DS90CF386MTD/NOPB.A | Active | Production | TSSOP (DGG) \| 56 | 34 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF386MTD >B |
| DS90CF386MTD/NOPB.B | Active | Production | TSSOP (DGG) \| 56 | 34 \| TUBE | - | Call TI | Call TI | -10 to 70 | |
| DS90CF386MTDX/NOPB | Active | Production | TSSOP (DGG) \| 56 | 1000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF386MTD >B |
| DS90CF386MTDX/NOPB.A | Active | Production | TSSOP (DGG) \| 56 | 1000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90CF386MTD >B |
| DS90CF386MTDX/NOPB.B | Active | Production | TSSOP (DGG) \| 56 | 1000 \| LARGE T&R | - | Call TI | Call TI | -10 to 70 | |
| DS90CF386SLC/NOPB | Active | Production | NFBGA (NZC) \| 64 | 360 \| JEDEC TRAY (10+1) | Yes | SNAGCU | Level-4-260C-72 HR | -10 to 70 | DS90CF386 SLC >B |
| DS90CF386SLC/NOPB.A | Active | Production | NFBGA (NZC) \| 64 | 360 \| JEDEC TRAY (10+1) | Yes | SNAGCU | Level-4-260C-72 HR | -10 to 70 | DS90CF386 SLC >B |
| DS90CF386SLCX/NOPB | Active | Production | NFBGA (NZC) \| 64 | 2000 \| LARGE T&R | Yes | SNAGCU | Level-4-260C-72 HR | -10 to 70 | DS90CF386 SLC >B |
| DS90CF386SLCX/NOPB.A | Active | Production | NFBGA (NZC) \| 64 | 2000 \| LARGE T&R | Yes | SNAGCU | Level-4-260C-72 HR | -10 to 70 | DS90CF386 SLC >B |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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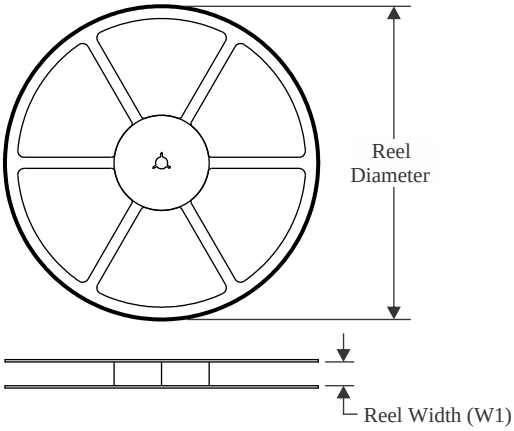
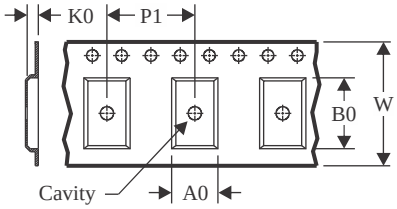
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

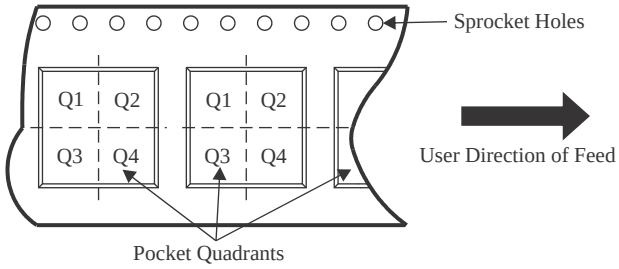



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

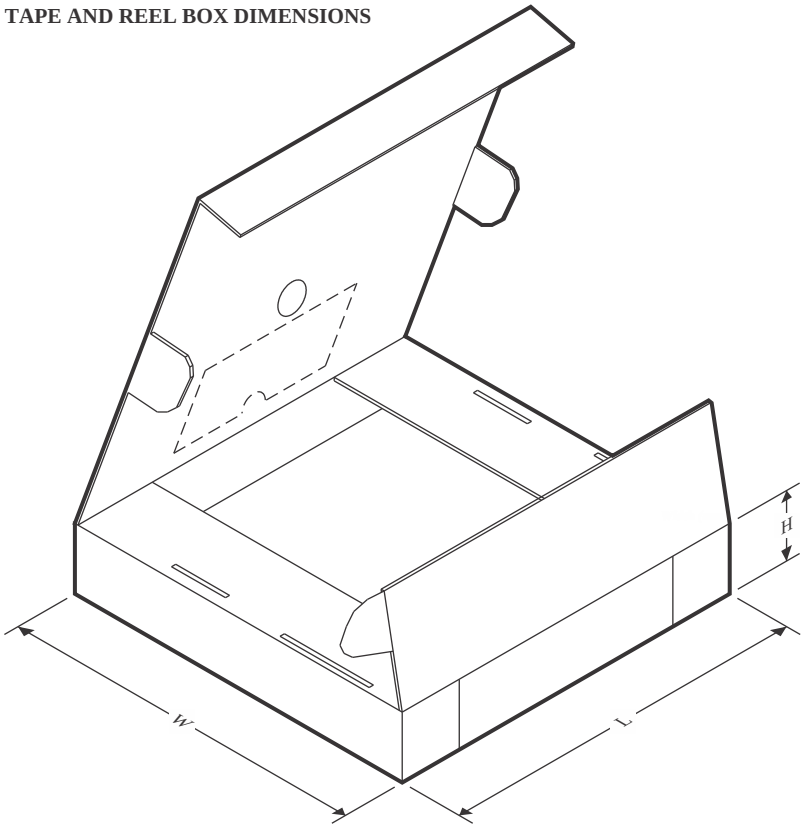
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS90CF366MTDX/NOPB | TSSOP | DGG | 48 | 1000 | 330.0 | 24.4 | 8.6 | 13.2 | 1.6 | 12.0 | 24.0 | Q1 |
| DS90CF386MTDX/NOPB | TSSOP | DGG | 56 | 1000 | 330.0 | 24.4 | 8.6 | 14.5 | 1.8 | 12.0 | 24.0 | Q1 |
| DS90CF386SLCX/NOPB | NFBGA | NZC | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 2.3 | 12.0 | 16.0 | Q1 |

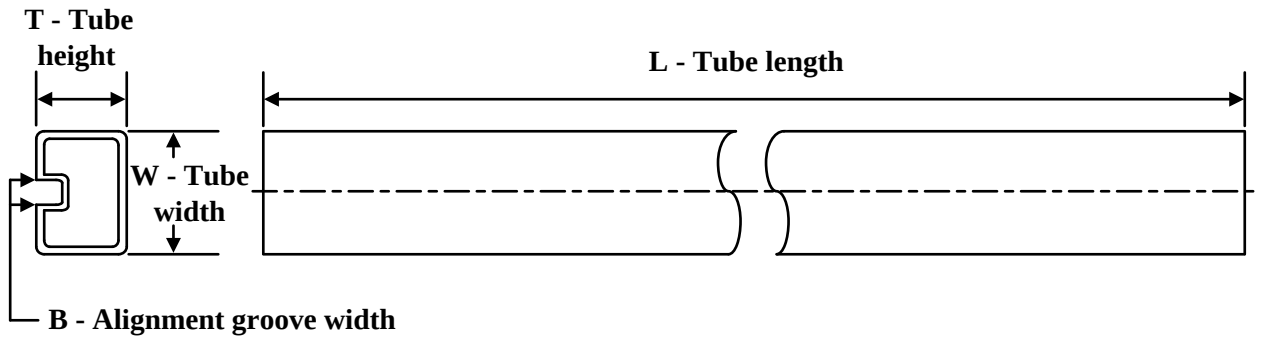
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS90CF366MTDX/NOPB | TSSOP | DGG | 48 | 1000 | 356.0 | 356.0 | 45.0 |
| DS90CF386MTDX/NOPB | TSSOP | DGG | 56 | 1000 | 356.0 | 356.0 | 45.0 |
| DS90CF386SLCX/NOPB | NFBGA | NZC | 64 | 2000 | 356.0 | 356.0 | 36.0 |

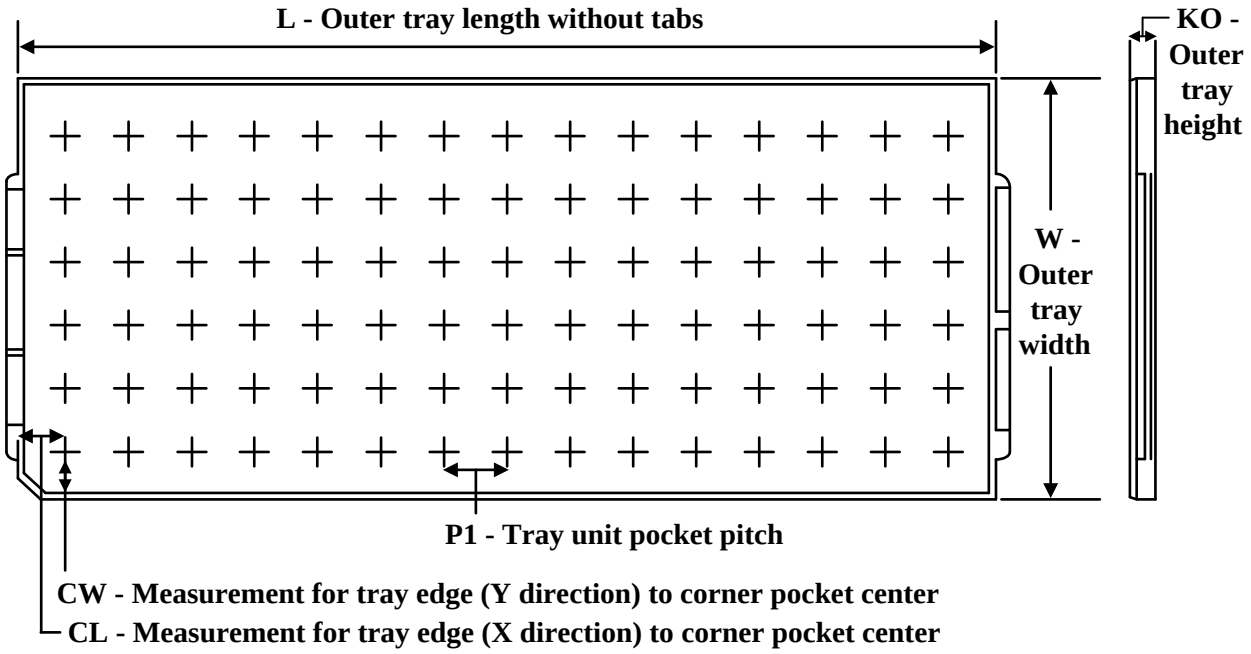
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| DS90CF366MTD/NOPB | DGG | TSSOP | 48 | 38 | 495 | 10 | 2540 | 5.79 |
| DS90CF366MTD/NOPB.A | DGG | TSSOP | 48 | 38 | 495 | 10 | 2540 | 5.79 |
| DS90CF386MTD/NOPB | DGG | TSSOP | 56 | 34 | 495 | 10 | 2540 | 5.79 |
| DS90CF386MTD/NOPB.A | DGG | TSSOP | 56 | 34 | 495 | 10 | 2540 | 5.79 |

## TRAY

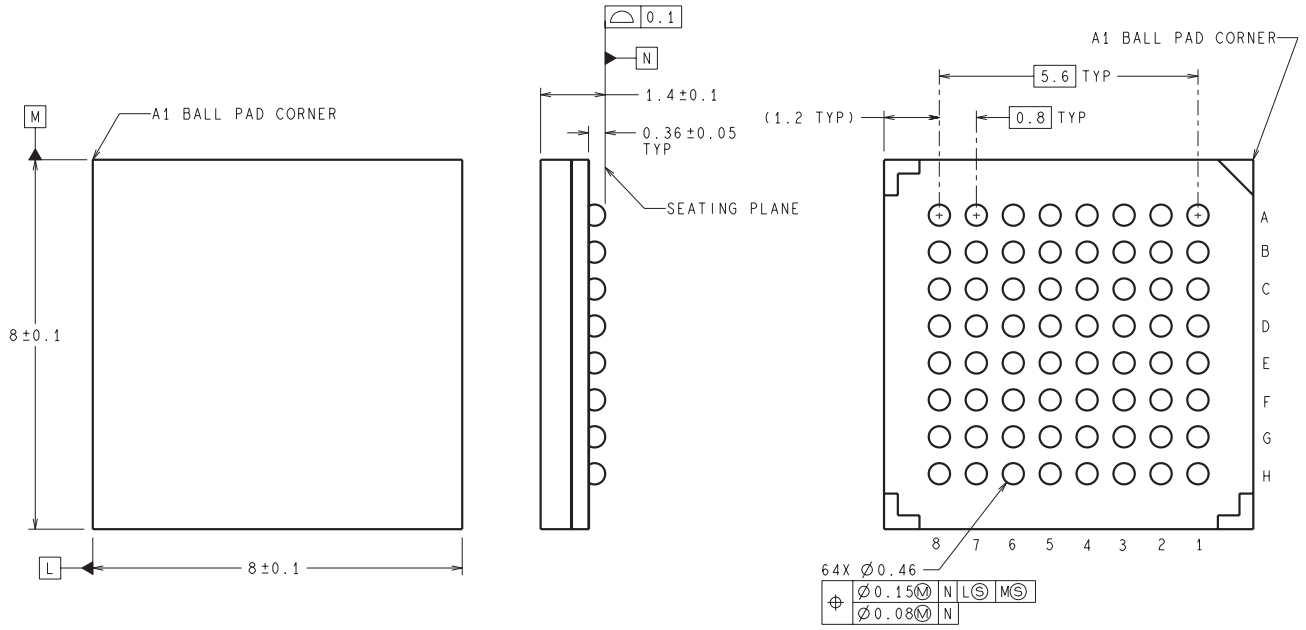



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS90CF386SLC/NOPB | NZC | NFBGA | 64 | 360 | 12 x 30 | 150 | 322.6 | 135.9 | 7620 | 10 | 12.5 | 12.95 |
| DS90CF386SLC/ NOPB.A | NZC | NFBGA | 64 | 360 | 12 x 30 | 150 | 322.6 | 135.9 | 7620 | 10 | 12.5 | 12.95 |

NZC0064A




**DIMENSIONS ARE IN MILLIMETERS**

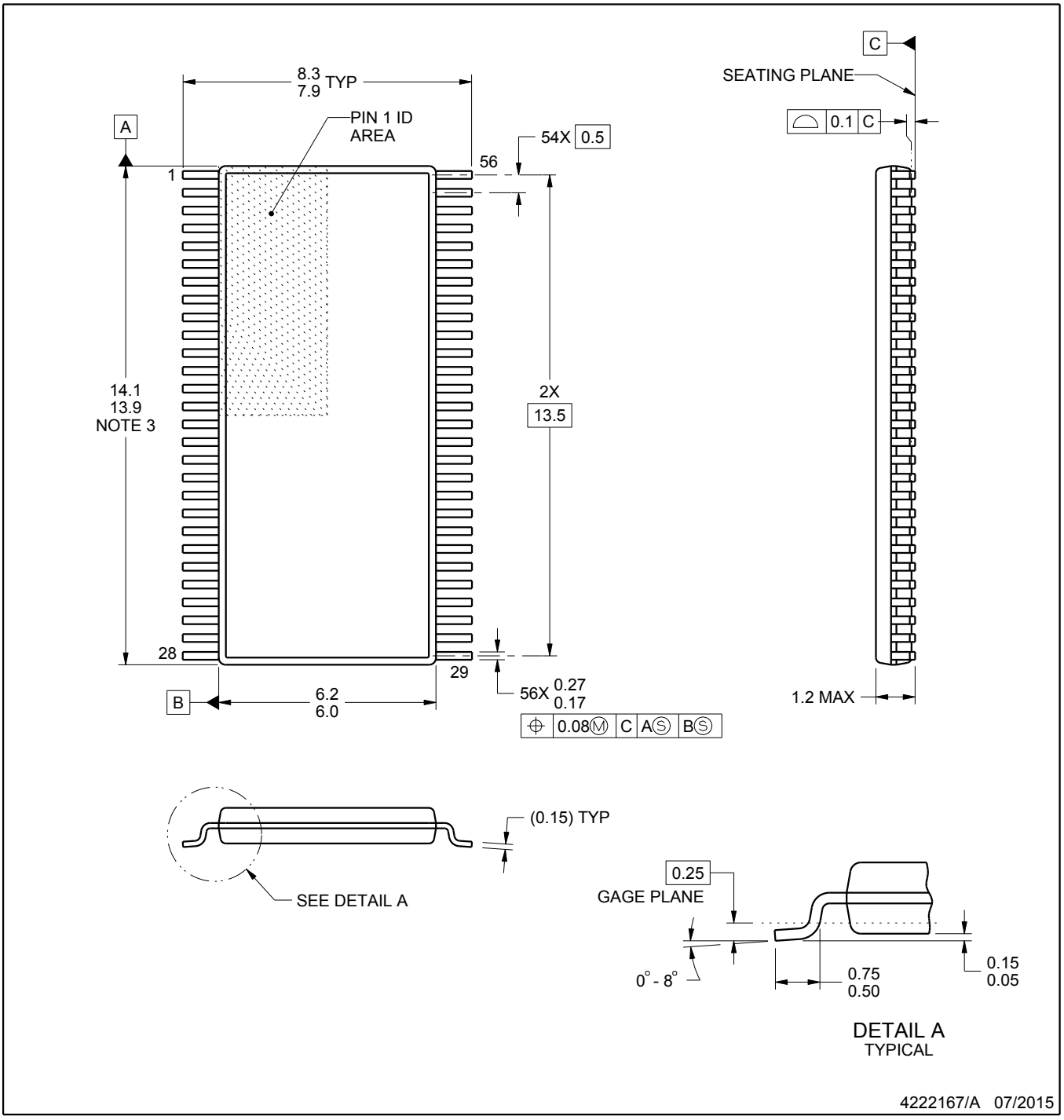
SLC64A (Rev C)

# PACKAGE OUTLINE

## DGG0056A

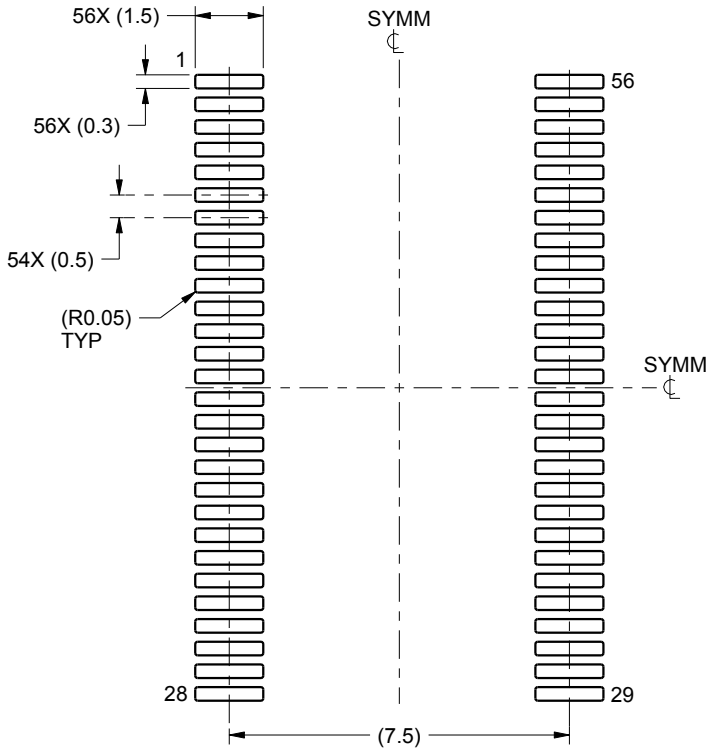
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

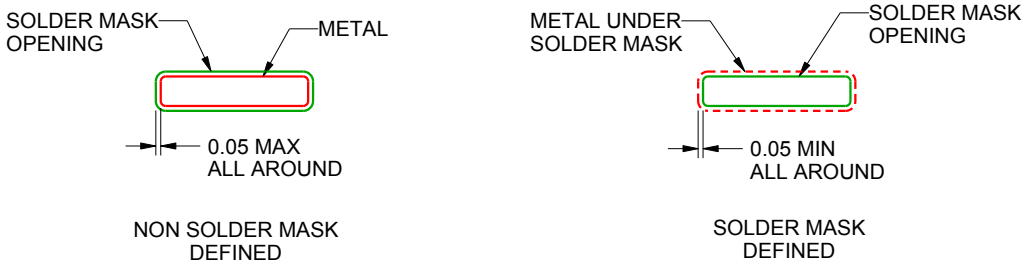



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

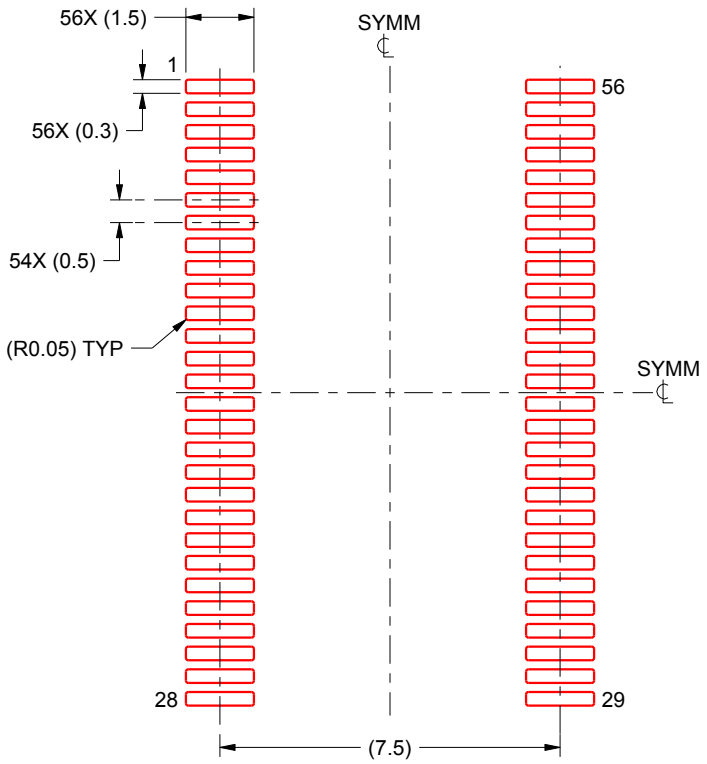



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

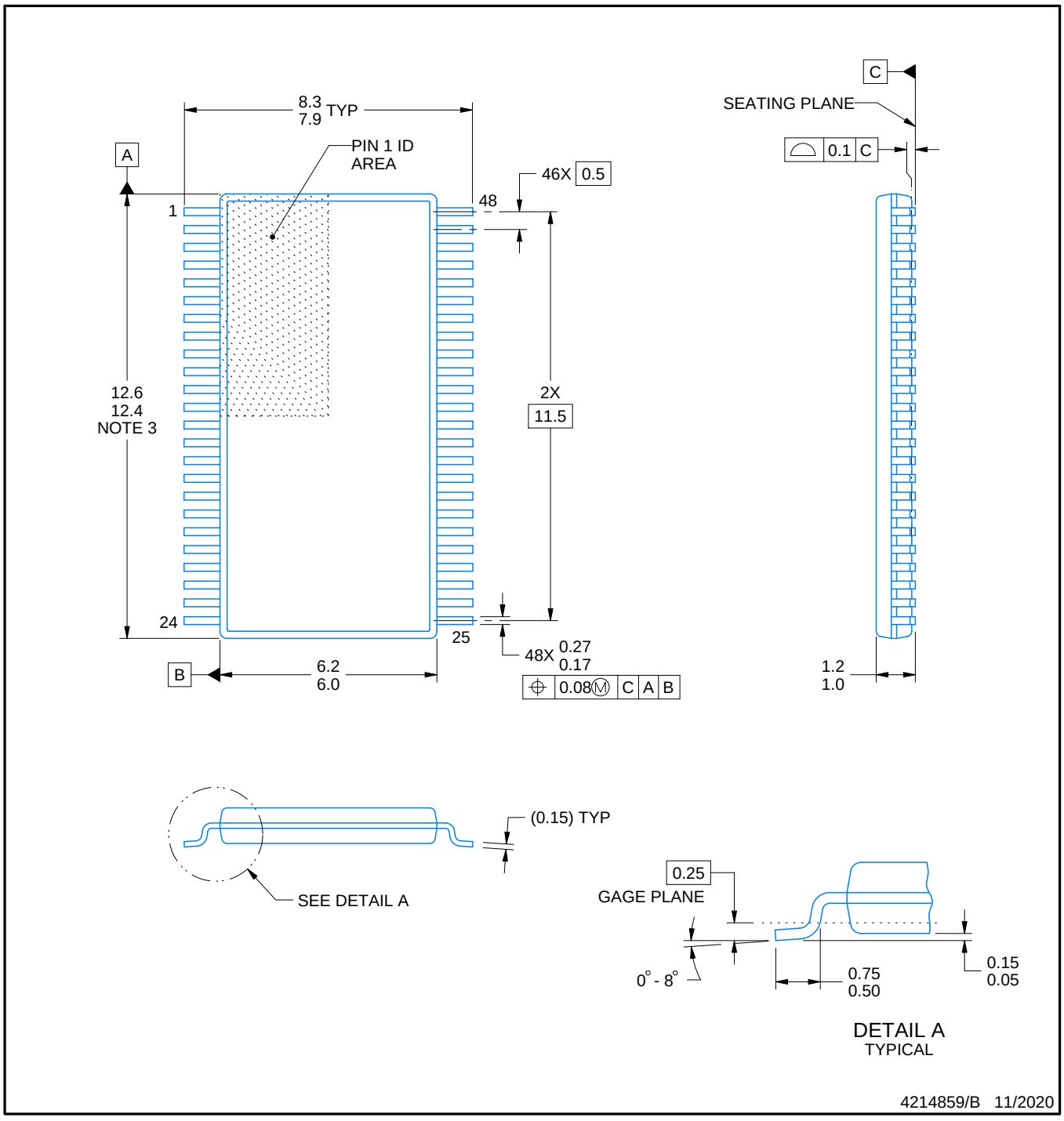
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGG0048A

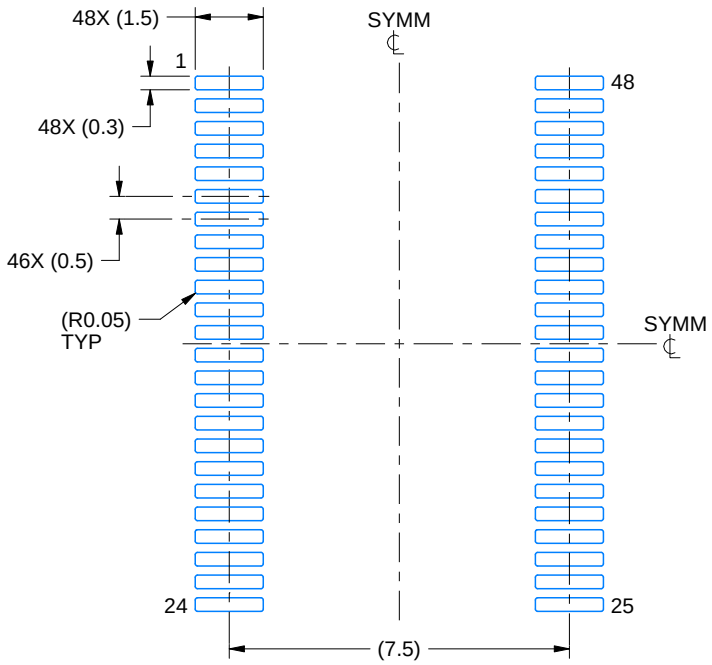
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

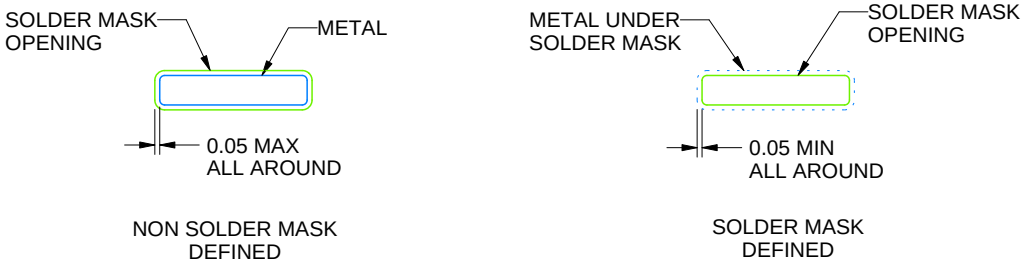



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

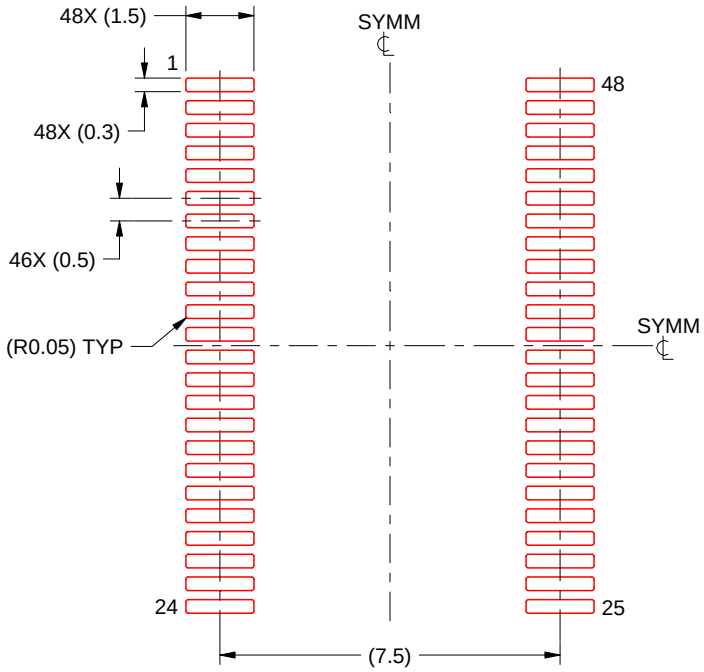



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

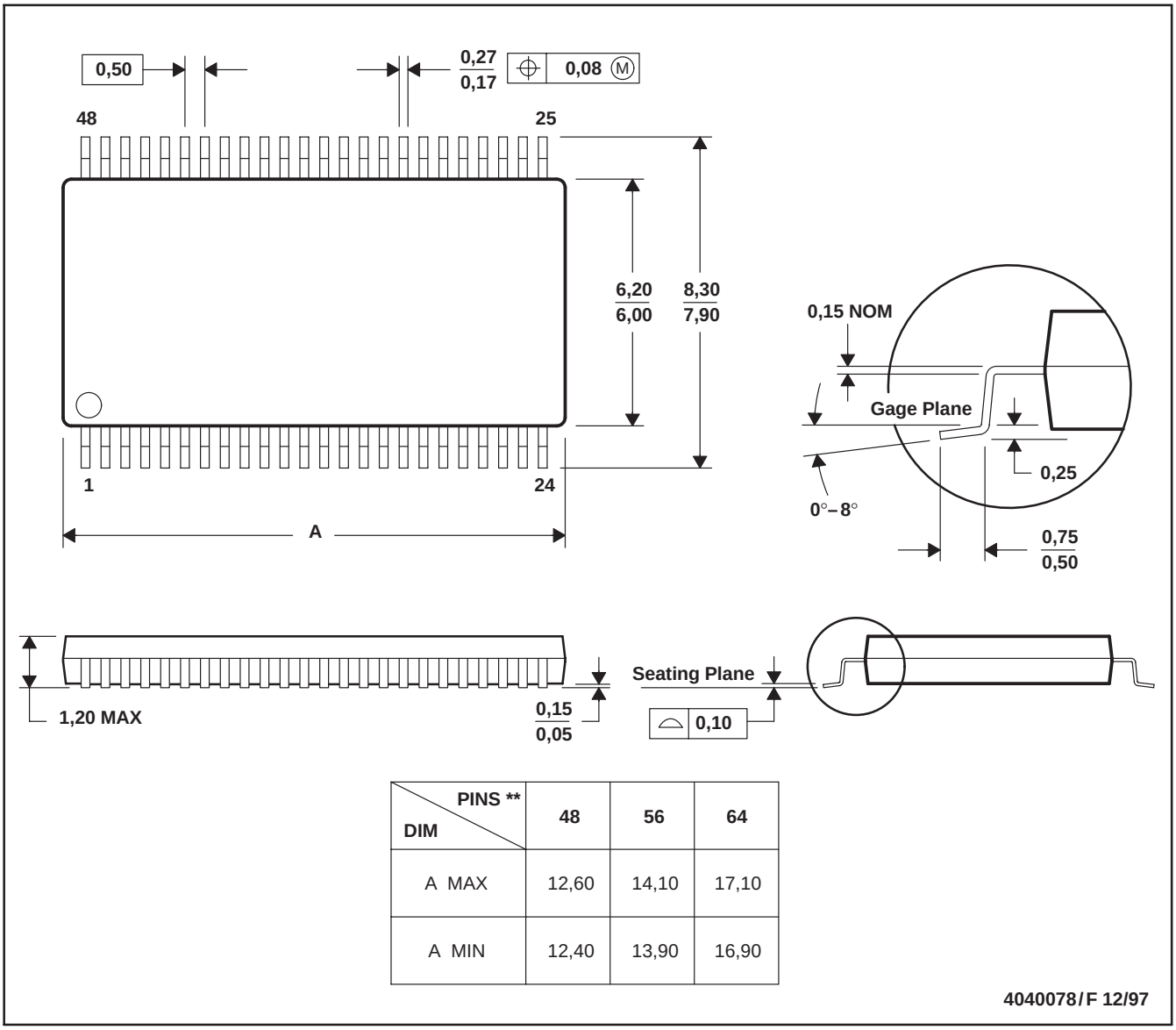
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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