# DSLVDS1048 3.3V LVDSクワッド・チャネル高速差分ライン・レシーバ

## 1 特長

- 最大400Mbpsの信号速度用に設計
- フロースルーのピン配置によりPCBレイアウトを簡素化
- チャネル間スキュー: 150ps (標準値)
- 差動スキュー: 100ps (標準値)
- 最大伝搬遅延: 2.7ns
- 3.3V電源の設計
- 電源オフ時にLVDS入力が高インピーダンス
- 低消費電力の設計(3.3V静的で40mW)
- 既存の5V LVDSドライバと相互運用可能
- 小振幅(標準値350mV)の差動信号レベルを許容
- 入力フェイルセーフのサポート
  - オープン、短絡、および終端
- 0V～−100mVのスレッショルド領域
- 動作温度範囲: -40°C～+85°C
- ANSI/TIA/EIA-644規格を満たすか上回る
- TSSOPパッケージで供給

## 2 アプリケーション

- 多機能プリンタ
- 基板間通信
- 試験/測定機器
- プリンタ
- データ・センターの相互接続
- ラボ計測機器
- 超音波スキャナ

## 3 概要

DSLVDS1048デバイスは、クワッドCMOSフロースルー差動ライン・レシーバで、非常に低い消費電力と高いデータ速度を必要とするアプリケーション用に設計されています。このデバイスは、低電圧差動信号(LVDS)テクノロジを活用し、400Mbps (200MHz)を超えるデータ転送速度をサポートするよう設計されています。

DSLVDS1048は低電圧(標準値350mV)の差動入力信号を受け付け、3V CMOS出力レベルに変換します。レシーバはTRI-STATE機能をサポートしており、出力の多重化に使用できます。また、レシーバはオープン、短絡、終端(100Ω)の入力フェイルセーフもサポートします。すべてのフェイルセーフ条件において、レシーバの出力はHIGHになります。DSLVDS1048はフロースルーのピン配置を採用しているため、PCBレイアウトが簡単になります。

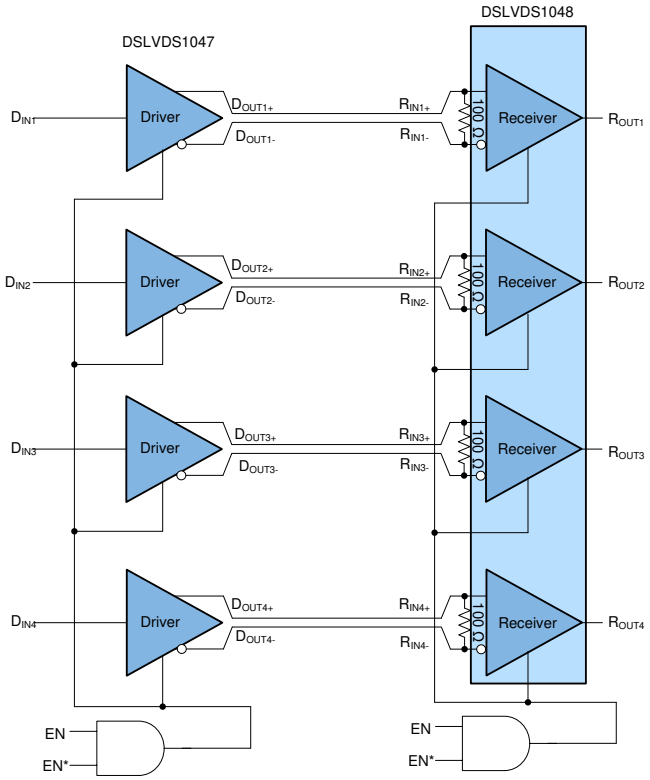
ENおよびEN*入力は互いにAND接続され、TRI-STATE出力を制御します。イネーブルは4つのレシーバすべてに共通です。DSLVDS1048およびコンパニオンLVDSライン・ドライバ(例: DSLVDS1047)は、大電力のPECL/ECLデバイスの新しい代替品として、高速のポイント・ツー・ポイント・インターフェイス・アプリケーションに使用できます。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| DSLVDS1048 | TSSOP (16) | 5.00mm×4.40mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**図 1. アプリケーション図**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# 目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Switching Characteristics ... 5
6.7 Typical Characteristics ... 6
7 Parameter Measurement Information ... 9
8 Detailed Description ... 10
8.1 Overview ... 10
8.2 Functional Block Diagram ... 10
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
9 Application and Implementation ... 12
9.1 Application Information ... 12
9.2 Typical Application ... 12
10 Power Supply Recommendations ... 14
11 Layout ... 14
11.1 Layout Guidelines ... 14
11.2 Layout Example ... 15
12 デバイスおよびドキュメントのサポート ... 16
12.1 ドキュメントの更新通知を受け取る方法 ... 16
12.2 コミュニティ・リソース ... 16
12.3 商標 ... 16
12.4 静電気放電に関する注意事項 ... 16
12.5 Glossary ... 16
13 メカニカル、パッケージ、および注文情報 ... 17

## 4 改訂履歴

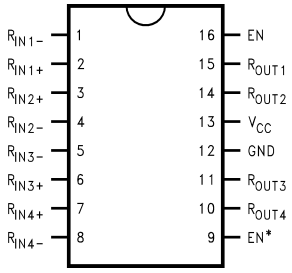
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| 日付 | リビジョン | 注 |
|---|---|---|
| 2018年9月 | * | 初版 |


Copyright © 2018, Texas Instruments Incorporated

# 5 Pin Configuration and Functions

**PW Package**
**16-Pin TSSOP**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 16 | I | Receiver enable pin: When EN is low, the receiver is disabled. When EN is high and EN* is low or open, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled. |
| EN* | 9 | I | Receiver enable pin: When EN* is high, the receiver is disabled. When EN* is low or open and EN is high, the receiver is enabled. If both EN and EN* are open circuit, then the receiver is disabled. |
| GND | 12 | — | Ground pin |
| $R_{IN+}$ | 2, 3, 6, 7 | I | Noninverting receiver input pin |
| $R_{IN-}$ | 1, 4, 5, 8 | I | Inverting receiver input pin |
| $R_{OUT}$ | 10, 11, 14, 15 | O | Receiver output pin |
| $V_{CC}$ | 13 | — | Power supply pin, +3.3V ± 0.3V |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

See (1)(2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage ($V_{CC}$) | | | –0.3 | 4 | V |
| Input voltage ($R_{IN+}$, $R_{IN-}$) | | | –0.3 | 3.6 | V |
| Enable input voltage (EN, EN*) | | | –0.3 | $V_{CC}$ + 0.3 | V |
| Output voltage ($R_{OUT}$) | | | –0.3 | $V_{CC}$ + 0.3 | V |
| Maximum package power dissipation at +25°C | PW0016A package | | | 866 | mW |
| | Derate PW0016A package | above +25°C | | 6.9 | mW/°C |
| Lead temperature soldering | (4 s) | | | 260 | °C |
| Maximum junction temperature | | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Copyright © 2018, Texas Instruments Incorporated

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge(1) | Human-body model (HBM) | ±10000 | V |
| | | Machine model | ±1200 | |

(1) ESD Rating:
HBM (1.5 kΩ, 100 pF)
EIAJ (0 Ω, 200 pF)

## 6.3 Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3 | 3.3 | 3.6 | V |
| Receiver input voltage | GND | | 3 | V |
| Operating free air temperature, $T_A$ | −40 | 25 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | DSLVDS1048 PW (TSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 110.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

| PARAMETER | | TEST CONDITIONS | | PIN | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential input high threshold | $V_{CM}$ = +1.2 V, 0.05 V, 2.95 V(3) | | $R_{IN+}$, $R_{IN-}$ | | | 100 | mV |
| $V_{TL}$ | Differential input low threshold | | | | −100 | | | mV |
| VCMR | Common-mode voltage range | VID = 200 mV peak to peak?(4) | | | 0.1 | | 2.3 | V |
| $I_{IN}$ | Input current | $V_{IN}$ = +2.8 V | $V_{CC}$ = 3.6 V or 0 V | | −10 | ±5 | 10 | µA |
| | | $V_{IN}$ = 0 V | | | −10 | ±1 | 10 | |
| | | $V_{IN}$ = +3.6 V | $V_{CC}$ = 0 V | | –20 | ±1 | 20 | |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = −0.4 mA, $V_{ID}$ = +200 mV, input terminated, input shorted | | $R_{OUT}$ | 2.7 | 3.3 | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2 mA, $V_{ID}$ = −200 mV | | | | | 0.25 | V |
| $I_{OS}$ | Output short-circuit current | Enabled, $V_{OUT}$ = 0 V(5) | | | −15 | −47 | −100 | mA |
| $I_{OZ}$ | Output TRI-STATE current | Disabled, $V_{OUT}$ = 0 V or $V_{CC}$ | | | −10 | ±1 | 10 | µA |

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for: $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(3) $V_{CC}$ is always higher than $R_{IN+}$ and $R_{IN-}$ voltage. $R_{IN-}$ and $R_{IN+}$ are allowed to have a voltage range −0.2 V to $V_{CC}$− VID/2. However, to be compliant with AC specifications, the common voltage range is 0.1 V to 2.3 V.
(4) The VCMR range is reduced for larger VID. Example: if VID = 400 mV, the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0 V to 2.4 V, but is supported only with inputs shorted and no external common-mode voltage applied. A VID up to $V_{CC}$ – 0 V may be applied to the $R_{IN+}$/ $R_{IN-}$ inputs with the Common-Mode voltage set to $V_{CC}$/2. Propagation delay and Differential Pulse skew decrease when VID is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ VID ≤ 800 mV over the common-mode range.
(5) Output short-circuit current ($I_{OS}$) is specified as magnitude only; minus sign indicates direction only. Only one output should be shorted at a time; do not exceed maximum junction temperature specification.


Copyright © 2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)

| PARAMETER | | TEST CONDITIONS | PIN | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | EN, EN* | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Input low voltage | | | GND | | 0.8 | V |
| $I_I$ | Input current | $V_{IN}$ = 0 V or $V_{CC}$, other Input = $V_{CC}$ or GND | | −10 | ±5 | 10 | μA |
| $V_{CL}$ | Input clamp voltage | $I_{CL}$ = −18 mA | | −1.5 | −0.8 | | V |
| $I_{CC}$ | No load supply current receivers enabled | EN = $V_{CC}$, inputs open | $V_{CC}$ | | 9 | 15 | mA |
| $I_{CCZ}$ | No load supply current receivers disabled | EN = GND, inputs open | | | 1 | 5 | mA |

## 6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)(4)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHLD}$ | Differential propagation delay high to low | $C_L$ = 15 pF<br>$V_{ID}$ = 200 mV<br>(Figure 16 and Figure 17) | 1.2 | 2 | 2.7 | ns |
| $t_{PLHD}$ | Differential propagation delay low to high | | 1.2 | 2 | 2.7 | ns |
| $t_{SKD1}$ | Differential pulse skew $\|t_{PHLD} - t_{PLHD}\|$(5) | | | 0.1 | 0.4 | ns |
| $t_{SKD2}$ | Differential channel-to-channel skew; same device(3) | | | 0.15 | 0.5 | ns |
| $t_{SKD3}$ | Differential part-to-part skew(4) | | | | 1 | ns |
| $t_{SKD4}$ | Differential part-to-part skew(6) | | | | 1.5 | ns |
| $t_{TLH}$ | Rise time | | | 0.5 | 1 | ns |
| $t_{THL}$ | Fall time | | | 0.5 | 1 | ns |
| $t_{PHZ}$ | Disable time high to Z | $R_L$ = 2 kΩ<br>$C_L$ = 15 pF<br>(Figure 18 and Figure 19) | | 8 | 14 | ns |
| $t_{PLZ}$ | Disable time low to Z | | | 8 | 14 | ns |
| $t_{PZH}$ | Enable time Z to high | | | 9 | 14 | ns |
| $t_{PZL}$ | Enable time Z to low | | | 9 | 14 | ns |
| $f_{MAX}$ | Maximum operating frequency(7) | All channels switching | 200 | 250 | | MHz |

(1) All typicals are given for: $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O$ = 50 Ω, $t_r$ and $t_f$ (0% to 100%) ≤ 3 ns for $R_{IN}$.
(3) $t_{SKD2}$, channel-to-channel skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
(4) $t_{SKD3}$, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same $V_{CC}$, and within 5°C of each other within the operating temperature range.
(5) $t_{SKD1}$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
(6) $t_{SKD4}$, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SKD4}$ is defined as |Max−Min| differential propagation delay.
(7) $f_{MAX}$ generator input conditions: $t_r$ = $t_f$ < 1 ns (0% to 100%), 50% duty cycle, differential (1.05-V to 1.35-V peak to peak). Output criteria: 60 / 40% duty cycle, $V_{OL}$ (maximum 0.4 V), $V_{OH}$ (minimum 2.7 V), Load = 15 pF (stray plus probes).

Copyright © 2018, Texas Instruments Incorporated

## 6.7 Typical Characteristics

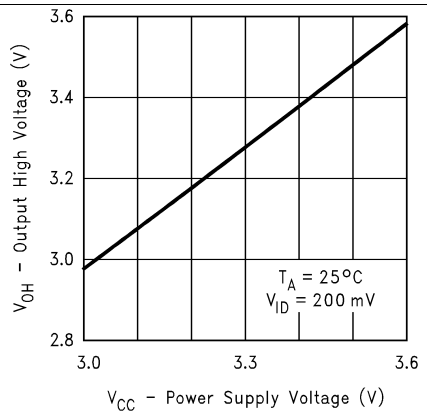



**Figure 2. Output High Voltage vs Power Supply Voltage**

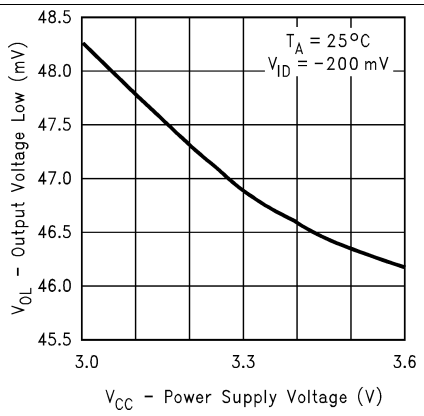



**Figure 3. Output Low Voltage vs Power Supply Voltage**

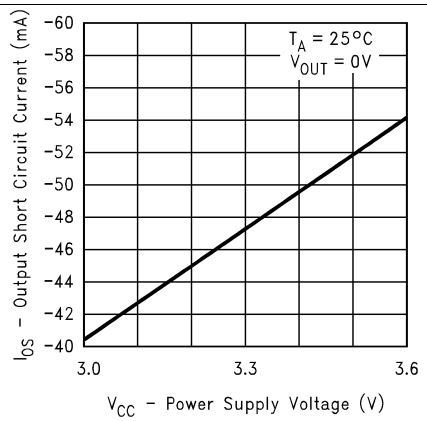



**Figure 4. Output Short-Circuit Current vs Power Supply Voltage**

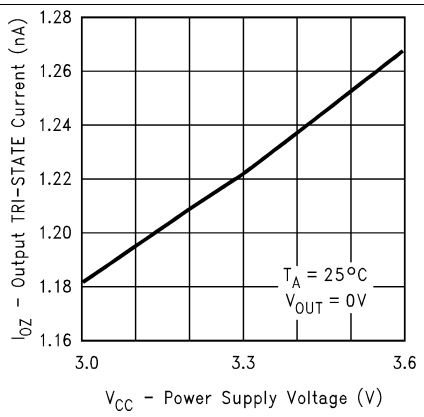



**Figure 5. Output TRI-STATE Current vs Power Supply Voltage**

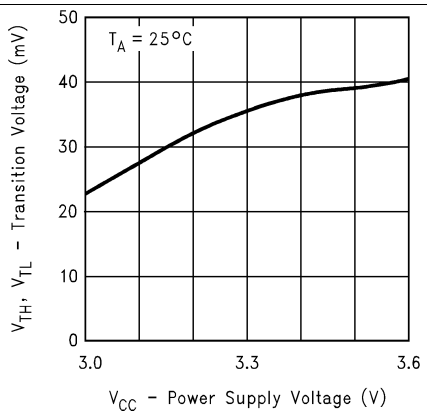



**Figure 6. Differential Transition Voltage vs Power Supply Voltage**

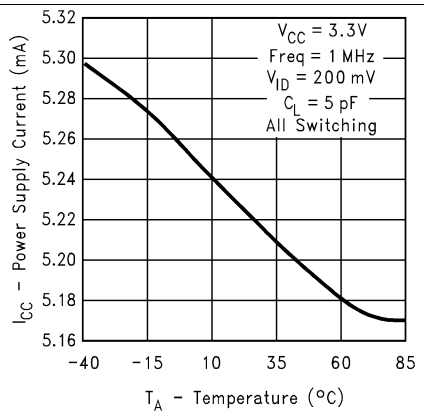



**Figure 7. Power Supply Current vs Ambient Temperature**


Copyright © 2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

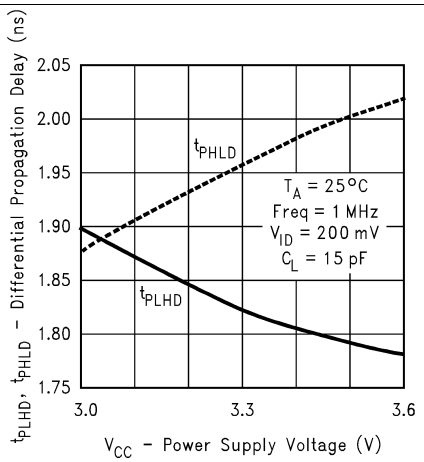



**Figure 8. Differential Propagation Delay vs Power Supply Voltage**

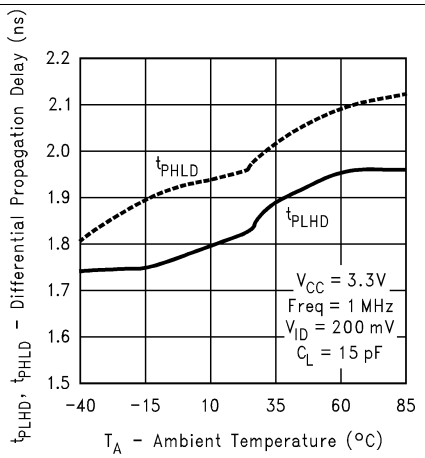



**Figure 9. Differential Propagation Delay vs Ambient Temperature**

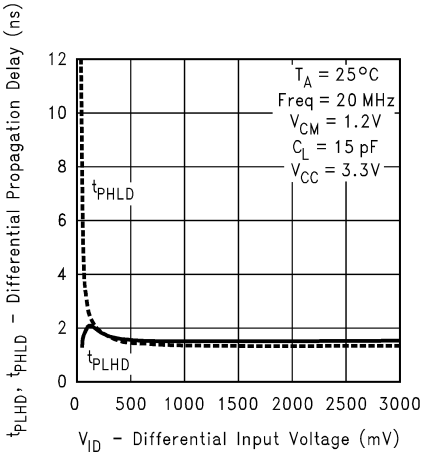



**Figure 10. Differential Propagation Delay vs Differential Input Voltage**

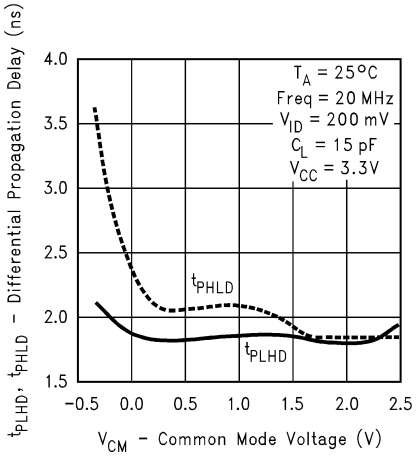



**Figure 11. Differential Propagation Delay vs Common-Mode Voltage**

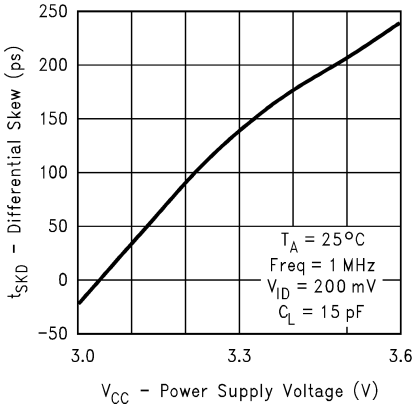



**Figure 12. Differential Skew vs Power Supply Voltage**

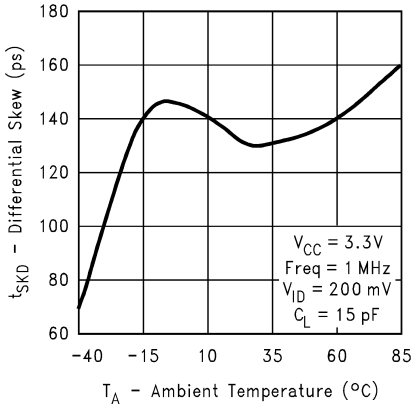



**Figure 13. Differential Skew vs Ambient Temperature**

Copyright © 2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

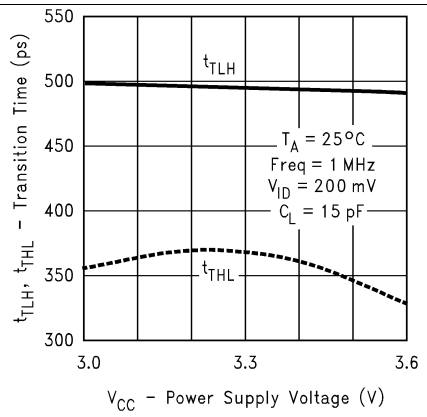



**Figure 14. Transition Time vs Power Supply Voltage**

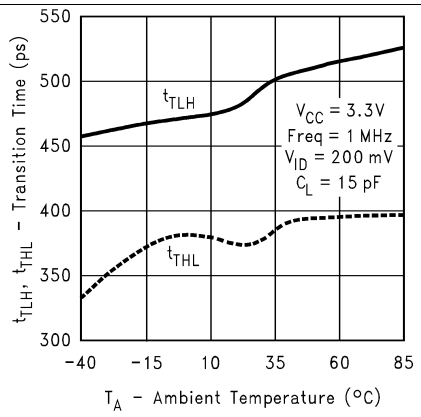



**Figure 15. Transition Time vs Ambient Temperature**


Copyright © 2018, Texas Instruments Incorporated

# 7 Parameter Measurement Information

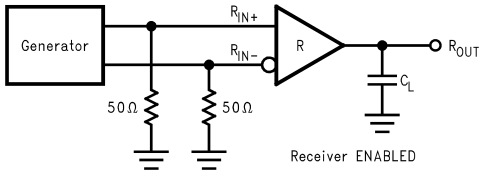



**Figure 16. Receiver Propagation Delay and Transition Time Test Circuit**

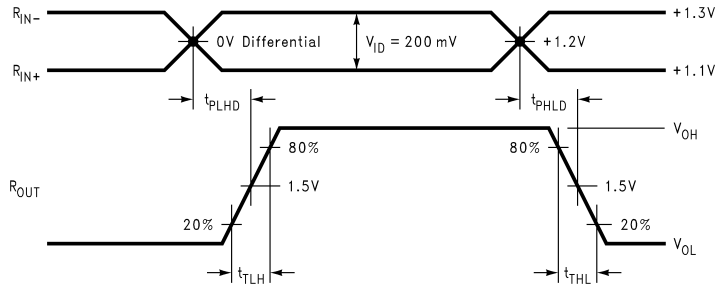
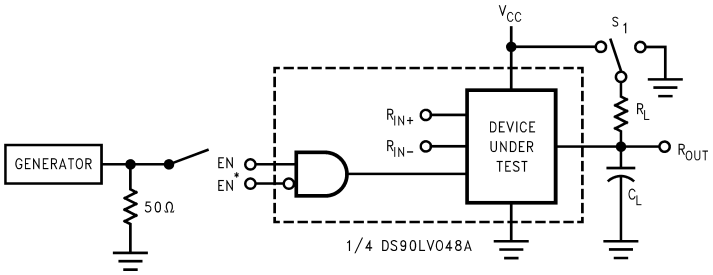



**Figure 17. Receiver Propagation Delay and Transition Time Waveforms**




$C_L$ includes load and test jig capacitance.
$S_1$ = $V_{CC}$ for $t_{PZL}$ and $t_{PLZ}$ measurements.
$S_1$ = GND for $t_{PZH}$ and $t_{PHZ}$ measurements.

**Figure 18. Receiver TRI-STATE Delay Test Circuit**

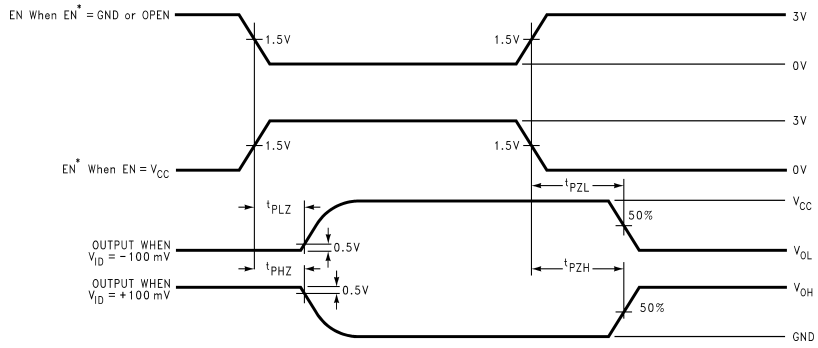



**Figure 19. Receiver TRI-STATE Delay Waveforms**

Copyright © 2018, Texas Instruments Incorporated

# 8 Detailed Description

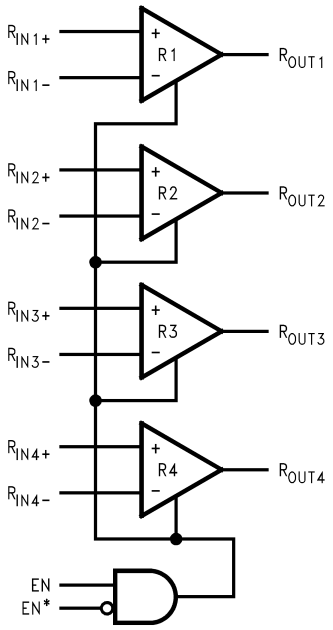
## 8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as shown in Figure 20. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media) is located as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

The DSLVDS1048 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1-V common-mode range centered around +1.2 V. This is related to the driver offset voltage which is typically +1.2 V. The driven signal is centered around this voltage and may shift ±1 V around this center point. The ±1-V shifting may be the result of a ground potential difference between the ground reference of the driver and the ground reference of the receiver, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0 V to +2.4 V (measured from each pin to ground). The device operates for receiver input voltages up to $V_{CC}$, but exceeding $V_{CC}$ turns on the ESD protection circuitry, which clamps the bus voltages.

The DSLVDS1048 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

## 8.2 Functional Block Diagram




Copyright © 2016, Texas Instruments Incorporated


Copyright © 2018, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Fail-Safe Feature

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DSLVDS1048 is a quad receiver device, and if an application requires only 1, 2, or 3 receivers, the unused channel(s) inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pullup and pulldown resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output is again in a HIGH state, even with the end of cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To ensure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors must be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point must be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

Additional information on fail-safe biasing of LVDS devices may be found in *AN-1194 Failsafe Biasing of LVDS Interfaces* (SNLA051).

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the DSLVDS1048.

**Table 1. Truth Table**

| ENABLES | | INPUT | OUTPUT |
|---|---|---|---|
| EN | EN* | $R_{IN+} - R_{IN-}$ | $R_{OUT}$ |
| H | L or Open | $V_{ID} \geq 0$ V | H |
| | | $V_{ID} \leq -0.1$ V | L |
| | | Full Fail-safe OPEN/SHORT or Terminated | H |
| All other combinations of ENABLE inputs | | X | Z |

Copyright © 2018, Texas Instruments Incorporated

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The DSLVDS1048 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

## 9.2 Typical Application

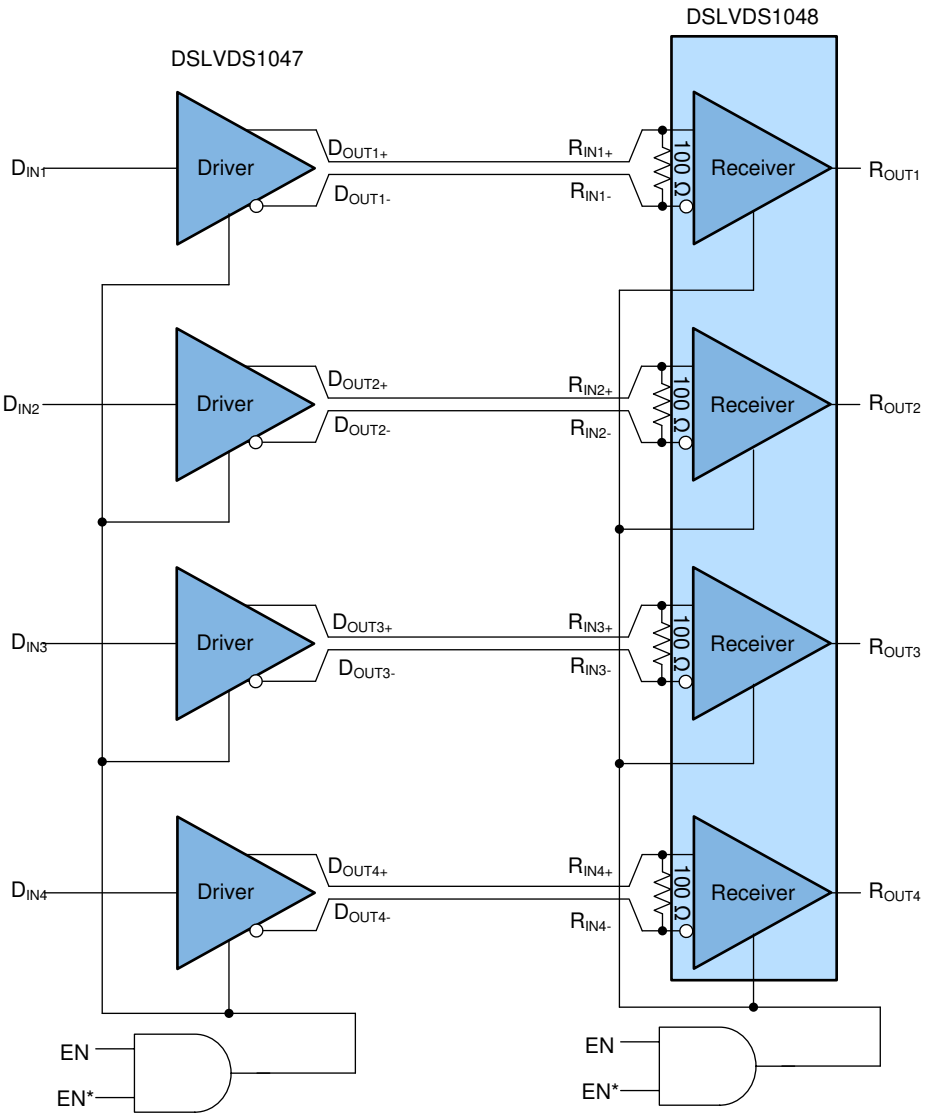



**Figure 20. Balanced System Point-to-Point Application**


Copyright © 2018, Texas Instruments Incorporated

## Typical Application (continued)

### 9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT5 (Category 5) twisted pair cable works well, is readily available, and relatively inexpensive.

**Table 2. Design Requirements**

| DESIGN PARAMETERS | EXAMPLE VALUE |
|---|---|
| Receiver Supply Voltage ($V_{CC}$) | 3.0 to 3.6 V |
| Receiver Output Voltage | 0 to 3.6 V |
| Signaling Rate | 0 to 400 Mbps |
| Interconnect Characteristic Impedance | 100 Ω |
| Termination Resistance | 100 Ω |
| Number of Receiver Nodes | 1 |
| Ground shift between driver and receiver | ±1 V |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Probing LVDS Transmission Lines*

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

#### *9.2.2.2 Threshold*

The LVDS Standard (ANSI/TIA/EIA-644) specifies a maximum threshold of ±100 mV for the LVDS receiver. The DSLVDS1048 supports an enhanced threshold region of −100 mV to 0 V. This is useful for fail-safe biasing. The threshold region is shown in the Voltage Transfer Curve (VTC) in Figure 21. The typical DSLVDS1048 LVDS receiver switches at about −35 mV.

**NOTE**

With $V_{ID}$ = 0 V, the output is in a HIGH state. With an external fail-safe bias of +25 mV applied, the typical differential noise margin is now the difference from the switch point to the bias point.

In the following example, this would be 60 mV of Differential Noise Margin (+25 mV − (−35 mV)). With the enhanced threshold region of −100 mV to 0 V, this small external fail-safe biasing of +25 mV (with respect to 0 V) gives a DNM of a comfortable 60 mV. With the standard threshold region of ±100 mV, the external fail-safe biasing would need to be +25 mV with respect to +100 mV or +125 mV, giving a DNM of 160 mV which is stronger fail-safe biasing than is necessary for the DSLVDS1048. If more DNM is required, then a stronger fail-safe bias point can be set by changing resistor values.

Copyright © 2018, Texas Instruments Incorporated

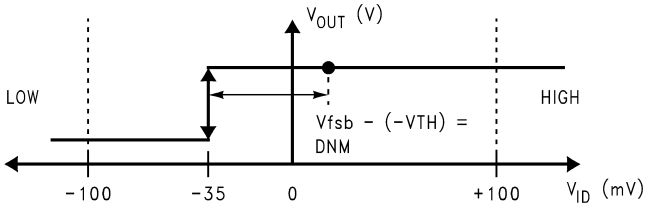



**Figure 21. VTC of the DSLVDS1048 LVDS Receiver**

### 9.2.3 Application Curve

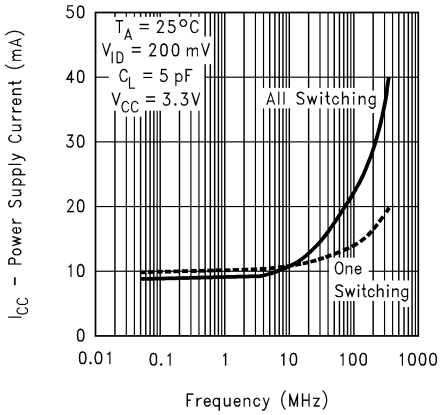



**Figure 22. Power Supply Current vs Frequency**

## 10 Power Supply Recommendations

Although the DSLVDS1047 draws very little power while at rest, its overall power consumption increases due to a dynamic current component. The DSLVDS1048 power supply connection must take this additional current consumption into consideration for maximum power requirements.

## 11 Layout

### 11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom): LVDS signals, ground, power, and TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. Best practice is to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

#### 11.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high-frequency ceramic (surface mount is recommended) 0.1-μF and 0.001-μF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-μF (35-V) or greater solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.


Copyright © 2018, Texas Instruments Incorporated

## Layout Guidelines (continued)

### 11.1.2 Differential Traces

Use controlled impedance traces that match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be < 10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals, which destroys the magnetic field cancellation benefits of differential signals and EMI, results. Remember the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps.

Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

### 11.1.3 Termination

Use a termination resistor that best matches the differential impedance or your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS does not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be < 10 mm (12 mm maximum).

## 11.2 Layout Example

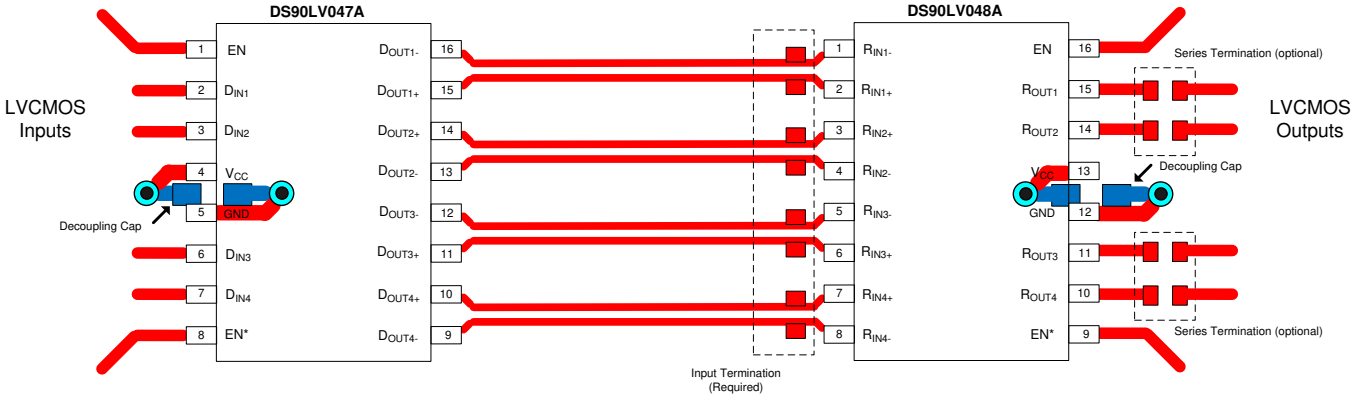



**Figure 23. Layout Recommendation**

Copyright © 2018, Texas Instruments Incorporated

# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™オンライン・コミュニティ** ***TIのE2E ( Engineer-to-Engineer ) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

**設計サポート** ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.


Copyright © 2018, Texas Instruments Incorporated

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

Copyright © 2018, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DSLVDS1048PWR | Active | Production | TSSOP (PW) \| 16 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DSLVDS 1048 |
| DSLVDS1048PWR.B | Active | Production | TSSOP (PW) \| 16 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DSLVDS 1048 |
| DSLVDS1048PWT | Active | Production | TSSOP (PW) \| 16 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DSLVDS 1048 |
| DSLVDS1048PWT.B | Active | Production | TSSOP (PW) \| 16 | 1000 \| SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DSLVDS 1048 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

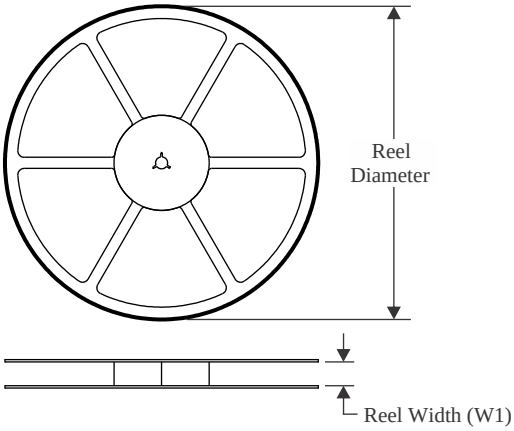
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

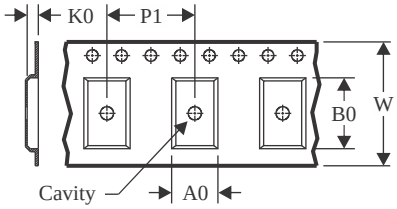
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

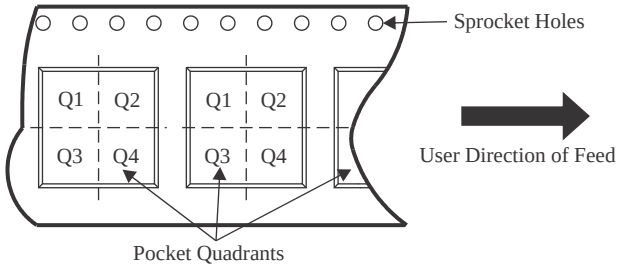



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

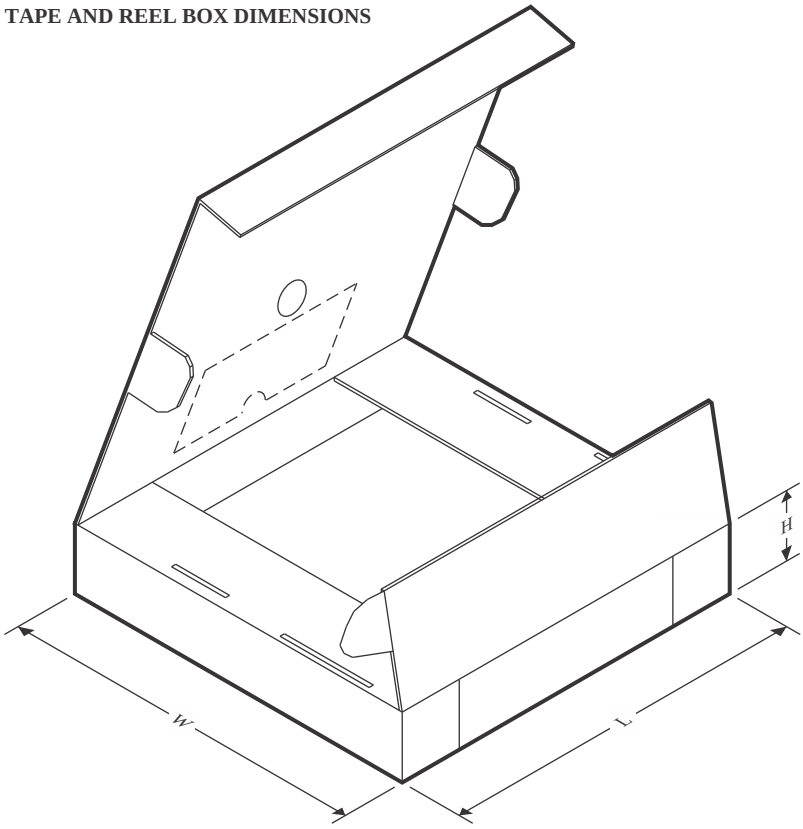
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DSLVDS1048PWR | TSSOP | PW | 16 | 2500 | 330.0 | 12.4 | 6.95 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| DSLVDS1048PWT | TSSOP | PW | 16 | 1000 | 330.0 | 12.4 | 6.95 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

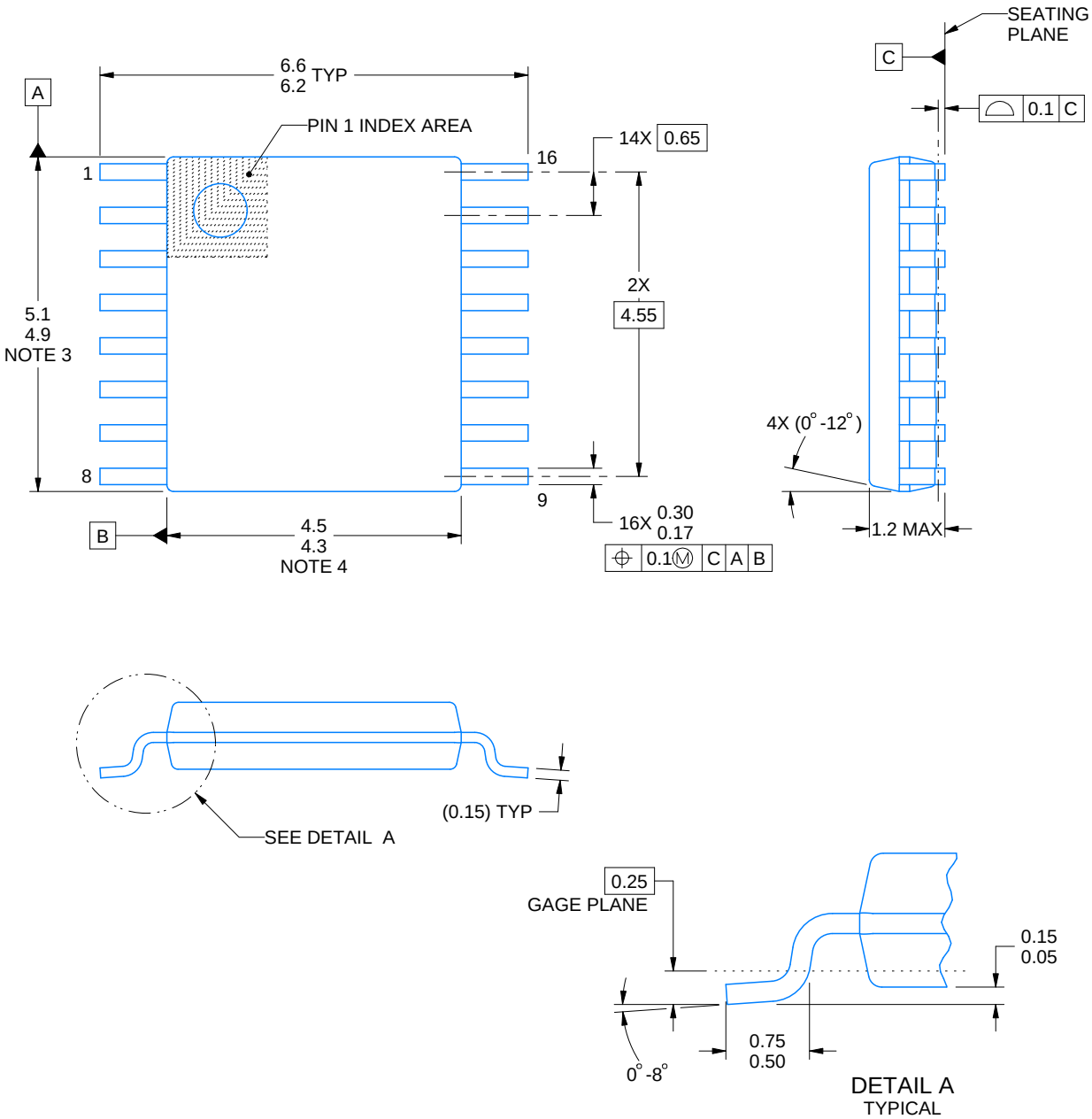
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DSLVDS1048PWR | TSSOP | PW | 16 | 2500 | 367.0 | 367.0 | 35.0 |
| DSLVDS1048PWT | TSSOP | PW | 16 | 1000 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## PW0016A

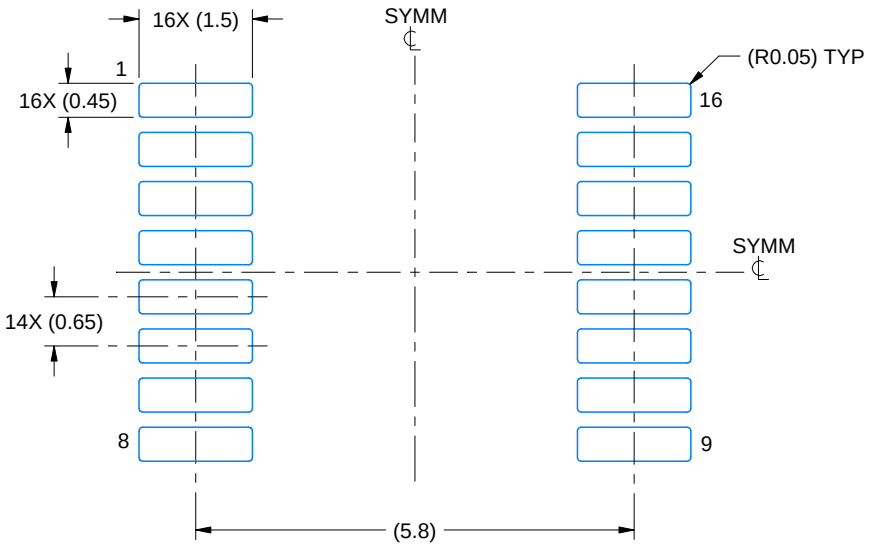
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

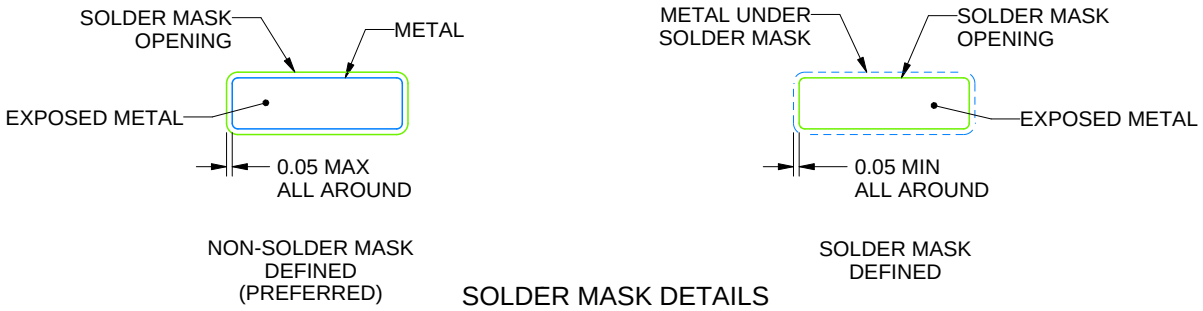



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

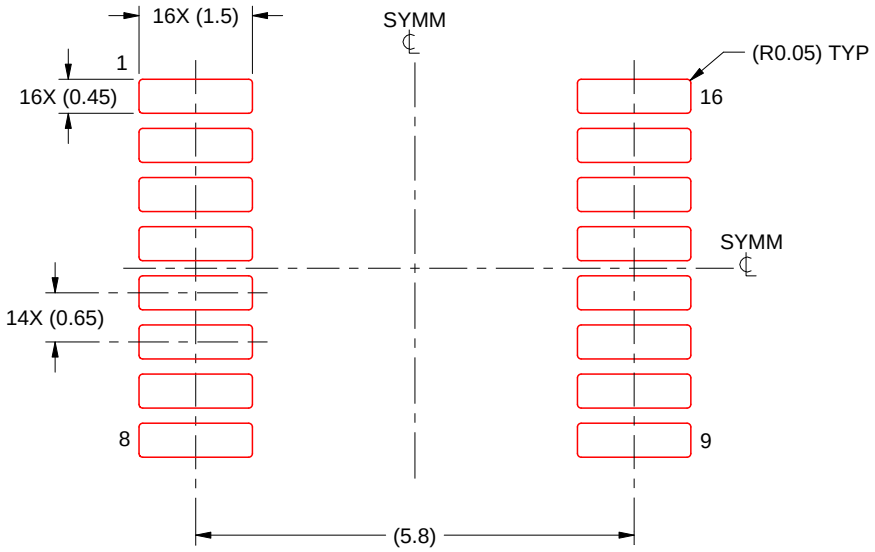



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月