TEXAS INSTRUMENTS
ISO7021
JAJSHO2C – JULY 2019 – REVISED MAY 2024

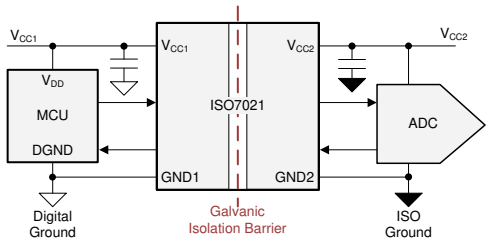
ISO7021 超低消費電力 2 チャネル・デジタル・アイソレータ

1 特長

- 超低消費電力
  - チャネルあたり 4.8μA の静止電流 (3.3V)
  - 100kbps でチャネルあたり 15μA (3.3V)
  - 1Mbps でチャネルあたり 120μA (3.3V)
- 堅牢な絶縁バリア
  - 推定寿命：100 年超
  - 定格絶縁電圧：3000V_{RMS}
  - CMTI：±100kV/μs (代表値)
- 幅広い電源電圧範囲：1.71V～1.89V、2.25V～5.5V
- 幅広い温度範囲：-55℃～125℃
- 小型の 8-SOIC パッケージ (8-D)
- 信号速度：最大 4Mbps
- デフォルト出力 HIGH (ISO7021) および LOW (ISO7021F) のオプション
- 堅牢な電磁両立性 (EMC)
  - システム レベルでの ESD、EFT、サージ耐性
  - 絶縁バリアの両側で ±8kV の IEC 61000-4-2 接触放電保護
  - 超低エミッション
- 安全関連認証：
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 62368-1、IEC 61010-1、および GB 4943.1
  - IECEx (IEC 60079-0 & IEC 60079-11) および ATEX (EN IEC60079-0 & EN 60079-11)

2 アプリケーション

- 4mA～20mA ループ駆動のフィールド トランスミッタ
- ファクトリ オートメーションとプロセス オートメーション
- 低消費電力 GPIO、UART 絶縁



アプリケーション概略回路図

3 概要

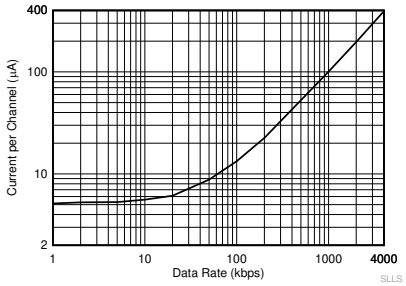
ISO7021 デバイスは超低消費電力の デジタル アイソレータで、CMOS または LVCMOS デジタル I/O を絶縁できます。それぞれの絶縁チャネルにはロジック入力および出力バッファがあり、二重の容量性二酸化ケイ素 (SiO_2) 絶縁バリアによって分離されています。革新的なエッジ ベースのアーキテクチャとオン/オフ変調方式の組み合わせにより、超低消費電力でありながら、UL1577 に準拠した 3000V_{RMS} の定格絶縁電圧を実現しています。デバイスのチャネルごとの動的な消費電流は 120μA/Mbps 未満、チャネルごとの静的な消費電流は 3.3V において 4.8μA なので、ISO7021 は電力と熱の両方において制約のあるシステム設計で使用できます。

このデバイスは最低 1.71V、最高 5.5V で動作し、絶縁バリアの両側の電源電圧が異なる場合も完全に機能します。2 チャネル アイソレータは、8 SOIC パッケージに封止された 1 つの順方向チャネルと 1 つの逆方向チャネルを備えたナロー ボディ 8-SOIC パッケージで供給されます。このデバイスには、デフォルト出力が HIGH と LOW のオプションがあります。入力電力または信号が失われた場合、接尾辞 F のない ISO7021 デバイスでは high、接尾辞 F のある ISO7021F デバイスでは low がデフォルト出力です。詳細については、「デバイスの機能モード」を参照してください。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ISO7021	SOIC (8-D)	4.90mm × 6.00mm

(1) 詳細については、セクション 14 を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



3.3V 時のデータ レートと消費電力との関係

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Device Comparison Table ... 3
5 Pin Configuration and Functions ... 3
Pin Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Power Ratings ... 5
6.6 Insulation Specifications ... 6
6.7 Safety-Related Certifications ... 7
6.8 Safety Limiting Values ... 7
6.9 Electrical Characteristics 5V Supply ... 8
6.10 Supply Current Characteristics 5V Supply ... 8
6.11 Electrical Characteristics 3.3V Supply ... 9
6.12 Supply Current Characteristics 3.3V Supply ... 9
6.13 Electrical Characteristics 2.5V Supply ... 10
6.14 Supply Current Characteristics 2.5V Supply ... 10
6.15 Electrical Characteristics 1.8V Supply ... 11
6.16 Supply Current Characteristics 1.8V Supply ... 11
6.17 Switching Characteristics ... 12
7 Parameter Measurement Information ... 13
8 Detailed Description ... 14
8.1 Overview ... 14
8.2 Functional Block Diagram ... 14
8.3 Feature Description ... 15
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Application ... 19
10 Power Supply Recommendations ... 22
11 Layout ... 23
11.1 Layout Guidelines ... 23
11.2 Layout Example ... 23
12 Device and Documentation Support ... 24
12.1 Documentation Support ... 24
12.2 Receiving Notification of Documentation Updates ... 24
12.3 サポート・リソース ... 24
12.4 Trademarks ... 24
12.5 静電気放電に関する注意事項 ... 24
12.6 用語集 ... 24
13 Revision History ... 25
14 Mechanical, Packaging, and Orderable Information ... 25

Copyright © 2024 Texas Instruments Incorporated

4 Device Comparison Table

表 4-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7021	1 Forward, 1 Reverse	4Mbps	High	SOIC-8	$3000V_{RMS}$ / $4242V_{PK}$
ISO7021 with F suffix	1 Forward, 1 Reverse	4Mbps	Low	SOIC-8	$3000V_{RMS}$ / $4242V_{PK}$

5 Pin Configuration and Functions

Pin Functions

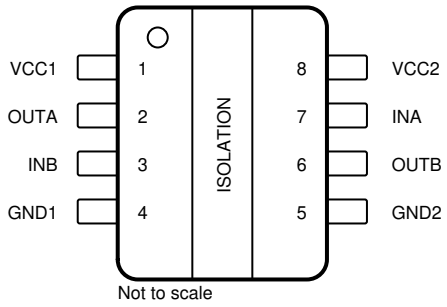


図 5-1. D Package 8-Pin SOIC Top View

PIN		Type(1)	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground connection for V_{CC1}
GND2	5	—	Ground connection for V_{CC2}
INA	7	I	Input, channel A
INB	3	I	Input, channel B
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	—	Power supply, side 1
V_{CC2}	8	—	Power supply, side 2

(1) I = Input, O = Output

Copyright © 2024 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply Voltage	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5	
Output Current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6V.

6.2 ESD Ratings

(1) (2)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)	±8000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

Copyright © 2024 Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1	V_{CCO} (2)= 1.8V	1.71		1.89	V
V_{CC1} (1)	Supply Voltage Side 1	V_{CCO} = 2.5V to 5V	2.25		5.5	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CCO} = 1.8V	1.71		1.89	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CCO} = 2.5V to 5V	2.25		5.5	V
V_{IH}	High level Input voltage		0.7 x V_{CCI}		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} = 5V	-4			mA
		V_{CCO} = 3.3V	-2			mA
		V_{CCO} = 2.5V	-1			mA
		V_{CCO} = 1.8V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5V			4	mA
		V_{CCO} = 3.3V			2	mA
		V_{CCO} = 2.5V			1	mA
		V_{CCO} = 1.8V			1	mA
DR	Data Rate		0		4	Mbps
T_A	Ambient temperature		-55		125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

6.4 Thermal Information

THERMAL METRIC(1)		ISO7021 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 2MHz 50% duty cycle square wave			8.4	mW
P_{D1}	Maximum power dissipation (side-1)				4.2	mW
P_{D2}	Maximum power dissipation (side-2)				4.2	mW

Copyright © 2024 Texas Instruments Incorporated

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS 8-D	UNIT
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	4	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 150V_{RMS}	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test;	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} , t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	4242	V_{PK}
V_{IMP}	Maximum impulse voltage(2)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	V_{IOSM} ≥ 1.3 x V_{IMP}; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.2 × V_{IORM} , t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60s; $V_{pd(m)}$ = 1.6 × V_{IORM} , t_m = 10s	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 150°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} , t = 60s (qualification); V_{TEST} = 1.2 × V_{ISO} , t = 1s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air to determine the surge immunity of the package.
(3) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

Copyright © 2024 Texas Instruments Incorporated

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV	IECEx / ATEX
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 62368-1 and EN 61010-1	Certified for use in intrinsic safety (IS) to IS applications under ATEX and IECEx.
Maximum transient isolation voltage, 4242V_{PK}; Maximum repetitive peak isolation voltage, 566V_{PK}; Maximum surge isolation voltage, 10000V_{PK}	3000V_{RMS} insulation rating; 400V_{RMS} basic insulation working voltage per CSA 62368-1 and IEC 62368-1; 300V_{RMS} basic insulation working voltage per CSA 61010-1 and IEC 61010-1	Single protection, 3000V_{RMS}	Basic insulation, Altitude ≤ 5000m, Tropical Climate, 250V_{RMS} maximum working voltage	3000V_{RMS} insulation per EN 62368-1 up to basic working voltage of 400V_{RMS} and EN 61010-1 up to basic working voltage of 300V_{RMS}	ATEX: EN IEC60079-0:2018 and EN 60079-11:2012 IECEx:IEC 60079-0:2017 (7th Ed) and IEC60079-11:2011 (6th Ed) Markings: II 1G Ex ia IIC Ga See the セクション 9.1.2
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001305151	Client ID number: 77311	IECEx certificate: IECEx CSA 20.012U ATEX certificate: CSANe 20ATEX2090U

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 94.3°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			241	mA
		$R_{\theta JA}$ = 94.3°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			368	mA
		$R_{\theta JA}$ = 94.3°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			482	
		$R_{\theta JA}$ = 94.3°C/W, V_I = 1.89V, T_J = 150°C, T_A = 25°C			701	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 94.3°C/W, T_J = 150°C, T_A = 25°C			1325	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

Copyright © 2024 Texas Instruments Incorporated

6.9 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -4mA	V_{CCO} - 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V	50	100		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	I_{CC1}		5.9	11.8	µA
		I_{CC2}		5.9	11.8	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		6.5	11.9	µA
		I_{CC2}		6.5	11.9	µA
Supply current - AC signal	10kbps, No Load	I_{CC1}		7.2	12.2	µA
		I_{CC2}		7.2	12.2	µA
	100kbps, No Load	I_{CC1}		15.9	27.7	µA
		I_{CC2}		15.9	27.7	µA
	1Mbps, No Load	I_{CC1}		129.0	175.0	µA
		I_{CC2}		129.0	175.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.9	11.4	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		6.5	11.8	µA
	10kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		7.2	12.2	µA
	100kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		15.9	27.8	µA
	1Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		129.0	175.0	µA

Copyright © 2024 Texas Instruments Incorporated

6.11 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -2mA	V_{CCO} - 0.3			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.3	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V	50	100		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 3.3V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	I_{CC1}		4.8	7.8	µA
		I_{CC2}		4.8	7.8	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		5.2	8.4	µA
		I_{CC2}		5.2	8.4	µA
Supply current - AC signal	10kbps, No Load	I_{CC1}		5.7	8.8	µA
		I_{CC2}		5.7	8.8	µA
	100kbps, No Load	I_{CC1}		15.0	23.0	µA
		I_{CC2}		15.0	23.0	µA
	1Mbps, No Load	I_{CC1}		120.0	153.0	µA
		I_{CC2}		120.0	155.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.8	7.8	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.2	8.4	µA
	10kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.7	8.8	µA
	100kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		15.0	23.0	µA
	1Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		120.0	153.0	µA

Copyright © 2024 Texas Instruments Incorporated

6.13 Electrical Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V	50	100		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics 2.5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	I_{CC1}		4.4	6.9	µA
		I_{CC2}		4.3	6.9	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		4.8	7.4	µA
		I_{CC2}		4.8	7.4	µA
Supply current - AC signal	10kbps, No Load	I_{CC1}		5.0	7.8	µA
		I_{CC2}		5.0	7.8	µA
	100kbps, No Load	I_{CC1}		12.4	21.2	µA
		I_{CC2}		12.4	21.2	µA
	1Mbps, No Load	I_{CC1}		112.0	144.0	µA
		I_{CC2}		113.0	144.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.4	6.9	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		4.8	7.4	µA
	10kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		5.0	7.8	µA
	100kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		12.4	21.2	µA
	1Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		113.0	144.0	µA

Copyright © 2024 Texas Instruments Incorporated

6.15 Electrical Characteristics 1.8V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
V_{OH}	High-level output voltage	I_{OH} = -1mA	V_{CCO} - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA			0.2	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			1	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx	-1			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0V, V_{CM} = 1200V	50	100		kV/µs
C_i	Input Capacitance(2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 1.8V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.16 Supply Current Characteristics 1.8V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7021						
Supply current - DC signal	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	I_{CC1}		3.4	5.7	µA
		I_{CC2}		3.4	5.7	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	I_{CC1}		3.8	6.2	µA
		I_{CC2}		3.8	6.2	µA
Supply current - AC signal	10kbps, No Load	I_{CC1}		4.1	6.7	µA
		I_{CC2}		4.1	6.7	µA
	100kbps, No Load	I_{CC1}		9.9	19.3	µA
		I_{CC2}		9.9	19.3	µA
	1Mbps, No Load	I_{CC1}		90.0	134.0	µA
		I_{CC2}		90.0	134.0	µA
Total Supply Current Per Channel	V_I = V_{CC1} (ISO7021); V_I = 0V (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.4	5.7	µA
	V_I = 0V (ISO7021); V_I = V_{CC1} (ISO7021 with F suffix)	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.8	6.2	µA
	10kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		3.9	6.7	µA
	100kbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		9.9	19.3	µA
	1Mbps, No Load	$I_{CC1(ch)}$ + $I_{CC2(ch)}$		90.0	134.0	µA

Copyright © 2024 Texas Instruments Incorporated

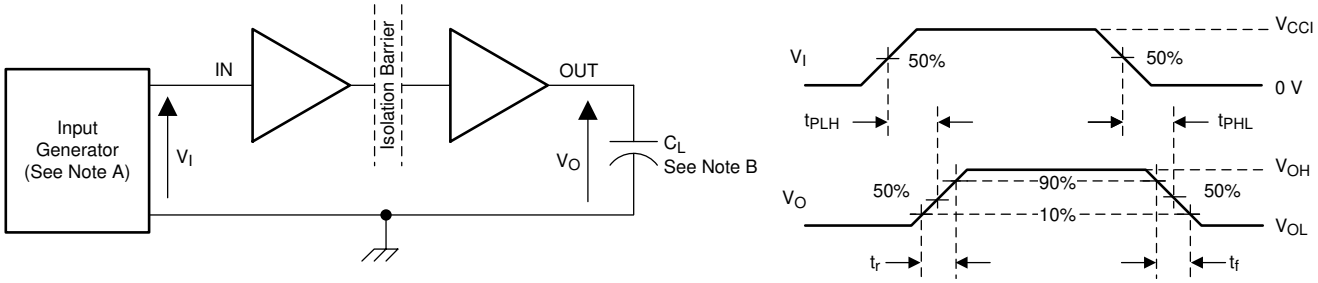
6.17 Switching Characteristics

V_{CC1}, V_{CC2} = 1.71 V to 1.89 V or 2.25 V to 5.5 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See 図 7-1		140	165	ns
$t_{P(dft)}$	Propagation delay drift			15		ps/℃
t_{UI}	Minimum pulse width	See 図 7-1	250			ns
PWD	Pulse width distortion				10	ns
$t_{sk(o)}$	Channel to channel output skew time				10	ns
$t_{sk(p-p)}$	Part to part skew time				70	ns
t_r	Output signal rise time	V_{CC} = 1.71V to 1.9V, See 図 7-1			8	ns
		V_{CC} = 2.25V to 5.5V, See 図 7-1			5	ns
t_f	Output signal fall time	V_{CC} = 1.71V to 1.9V, See 図 7-1			8	ns
		V_{CC} = 2.25V to 5.5V, See 図 7-1			5	ns
t_{DO}	Default output delay time from input power loss	See 図 7-2		400	750	µs
t_{PU}	Time from UVLO to valid output data		1		5	ms
F_R	Refresh rate		5	10		kbps

Copyright © 2024 Texas Instruments Incorporated

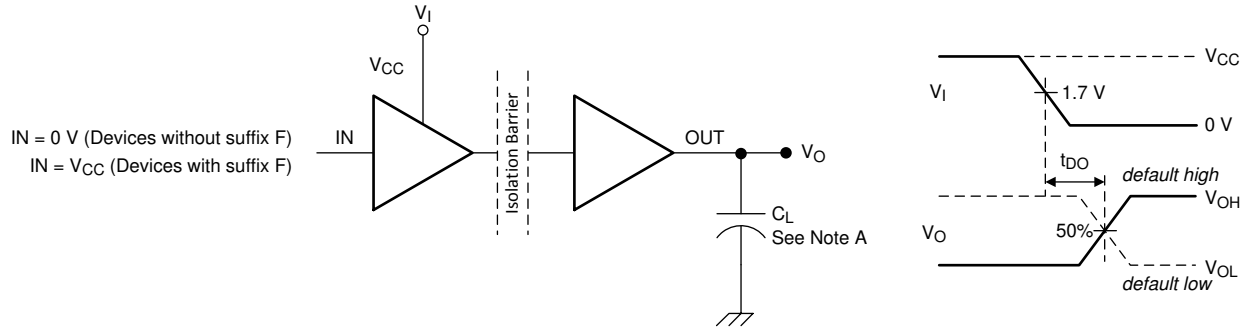
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, a 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

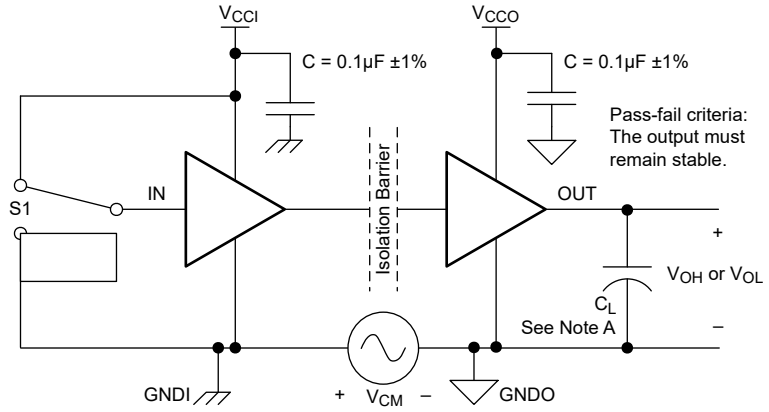
図 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

図 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

図 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7021 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 図 8-2, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

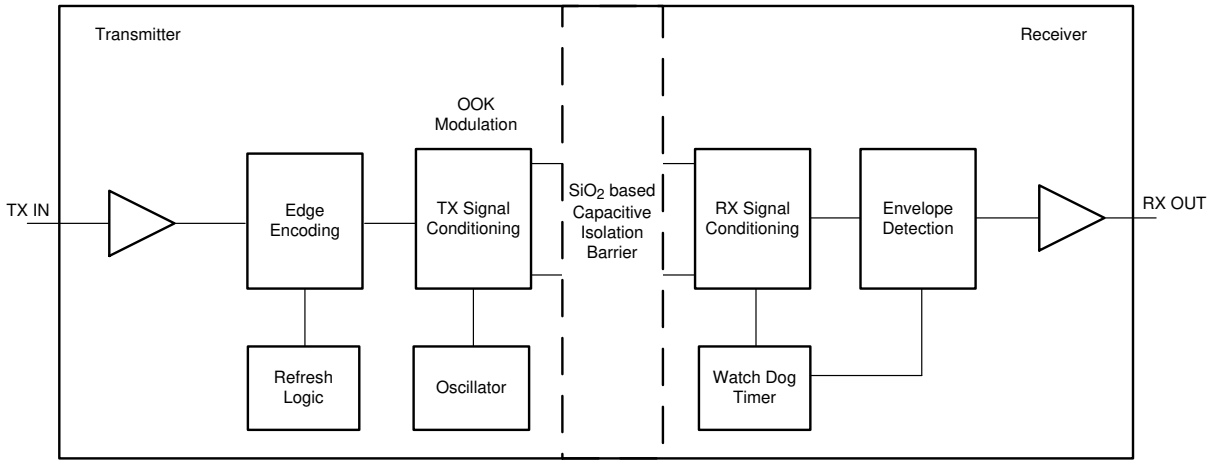


図 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Copyright © 2024 Texas Instruments Incorporated

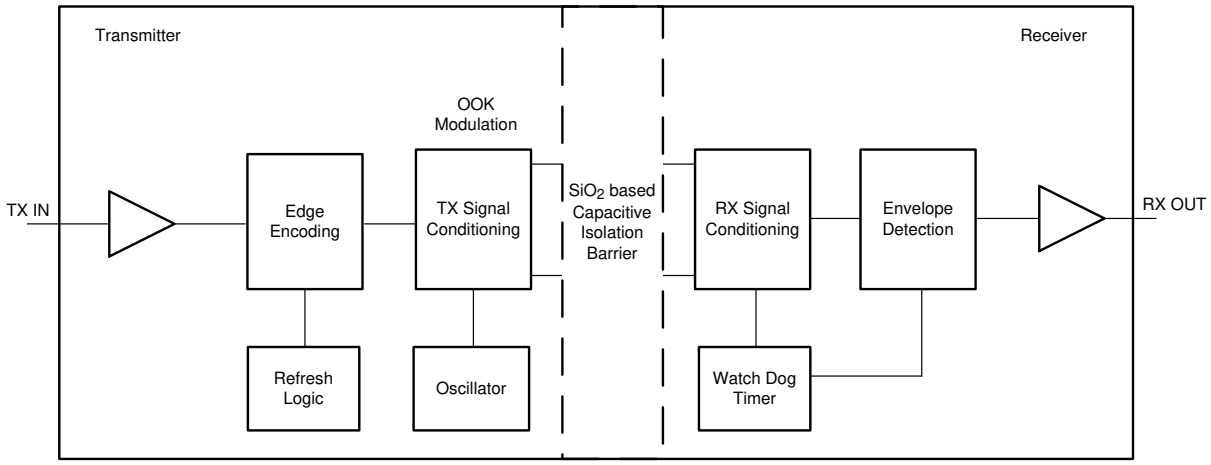


図 8-2. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Refresh

The ISO7021 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. The built in refresh function consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100µs. This design verifies that the input and output state of the isolator always match.

8.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

Copyright © 2024 Texas Instruments Incorporated

8.4 Device Functional Modes

表 8-1 shows the functional modes for the device.

表 8-1. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx)(3)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		X	Default	The channel output assumes the selected default option.
PD	PU	X	Default	When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for the device without the F suffix and *Low* for device with the F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined and tri-state(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the selected default option.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 1.54V); PD = Powered down (V_{CC} ≤ 1.54); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
(2) The outputs are in undetermined state when 1.54V < V_{CCI}, V_{CCO} < 1.54V.
(3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

8.4.1 Device I/O Schematics

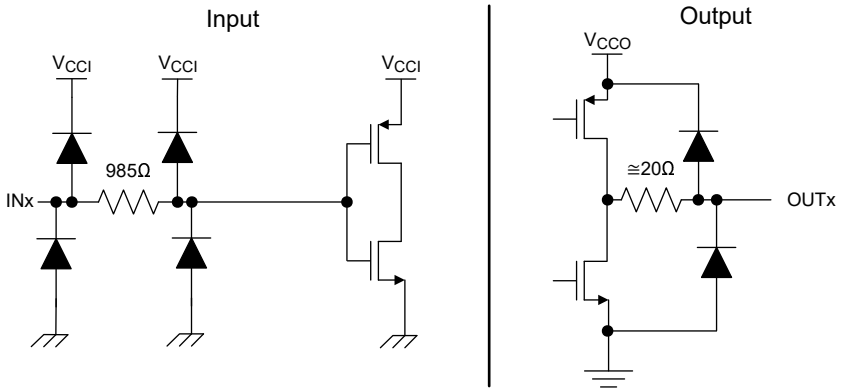


図 8-3. Device I/O Schematics

Copyright © 2024 Texas Instruments Incorporated

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7021 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 1.71V to 1.89V and 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}, and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See *Isolated power and data interface for low-power applications reference design* TI Design for detailed information on designing the ISO70xx in low-power applications.

9.1.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see 図 9-1 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 50% for insulation lifetime which translates into minimum required life time of 30 years.

図 9-2 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is $400V_{RMS}$ with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the D-8 package is specified up to $400V_{RMS}$. At the lower working voltages, the corresponding insulation barrier life time is much longer.

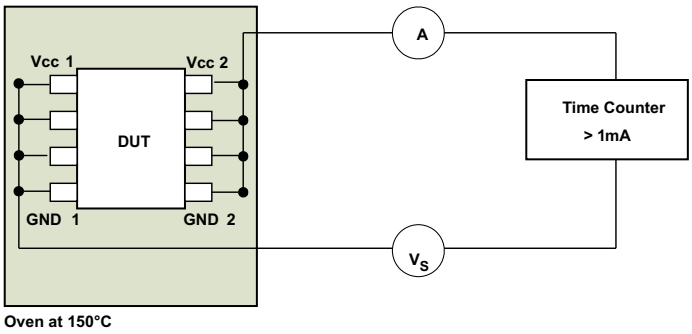


図 9-1. Test Setup for Insulation Lifetime Measurement

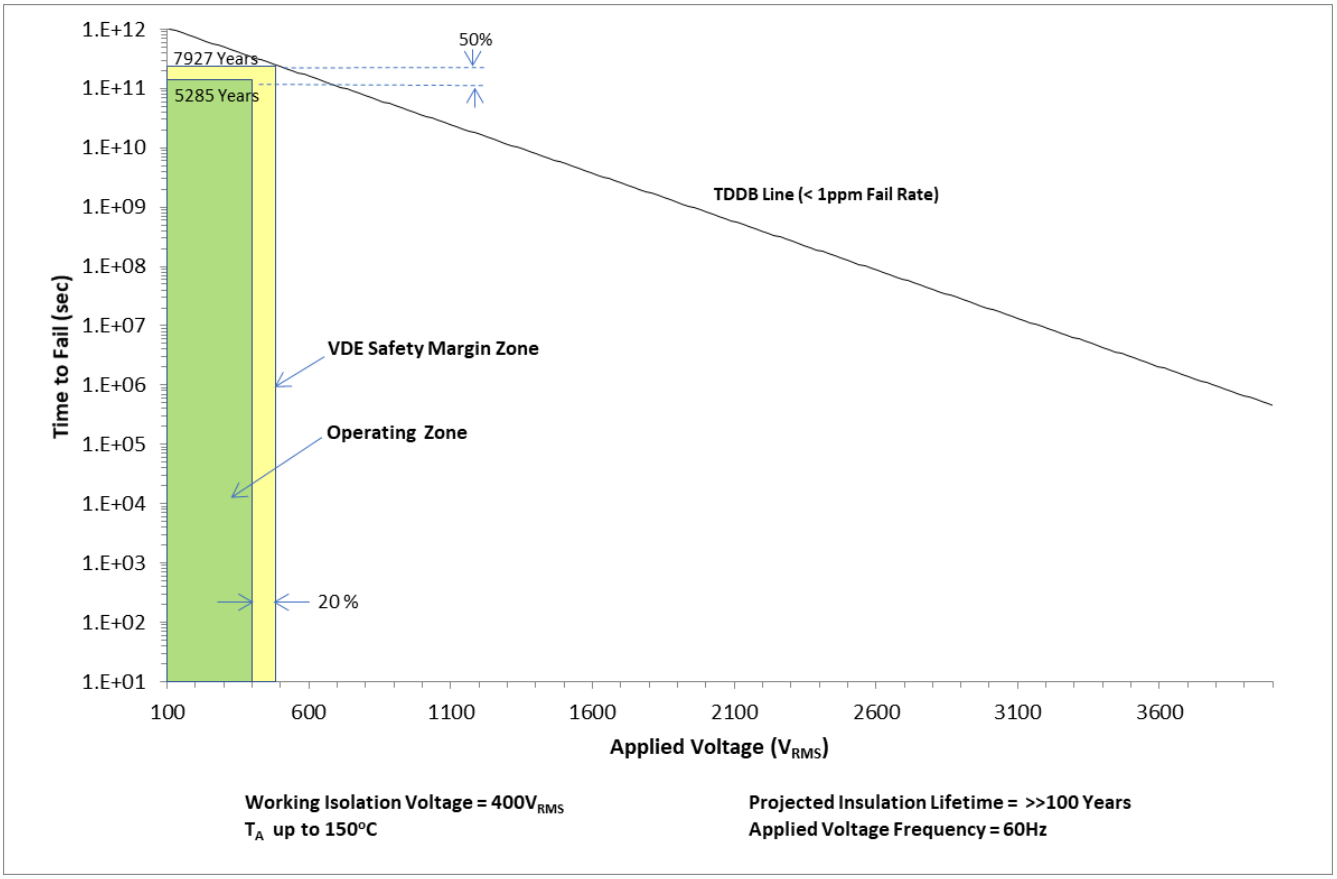


図 9-2. Insulation Lifetime Projection Data

Copyright © 2024 Texas Instruments Incorporated

9.1.2 Intrinsic Safety

The ISO7021 supports Intrinsically Safe (IS) to IS applications and carry IECEx and ATEX certifications. These devices do not currently support IS to non-IS galvanic isolation applications due to the minimum insulation thickness requirements of IEC 60079-11.

9.1.2.1 Schedule of Limitations

These components are certified to comply with IEC 60079-0, Edition 7, IEC 60079-11, Edition 6, EN IEC60079-0:2018 and EN 60070-11:2012. When one of these components is used in an equipment, the component is to be soldered on a PCB inside a suitable enclosure and re-evaluated as an equipment. The operating temperature range of these components is -55°C to 85°C. The creepage and clearance distances across the isolating component have been evaluated, but the distance to other circuitry remain the responsibility of the user of the final equipment.

This assembly is an isolating component between separate intrinsically safe circuits. The assembly must be connected to suitably certified intrinsically safe circuits considering the entity parameters and temperature ratings in the application scenario shown in 表 9-1.

表 9-1. Entity Parameters and Temperature Ratings

APPLICATION	ENTITY PARAMETERS SIDE 1	ENTITY PARAMETERS SIDE 2	AMBIENT TEMPERATURE RANGE	MAXIMUM COMPONENT TEMPERATURE
IS to IS	Ui = 50V	Ui = 50V	-55°C to 85°C	183°C
	Ii = 300mA	Ii = 300mA		
	Pi = 1.0W	Pi = 1.0W		
	Li = 0H	Li = 0H		
	Ci = 4pF	Ci = 4pF		

9.2 Typical Application

図 9-3 shows the isolated UART.

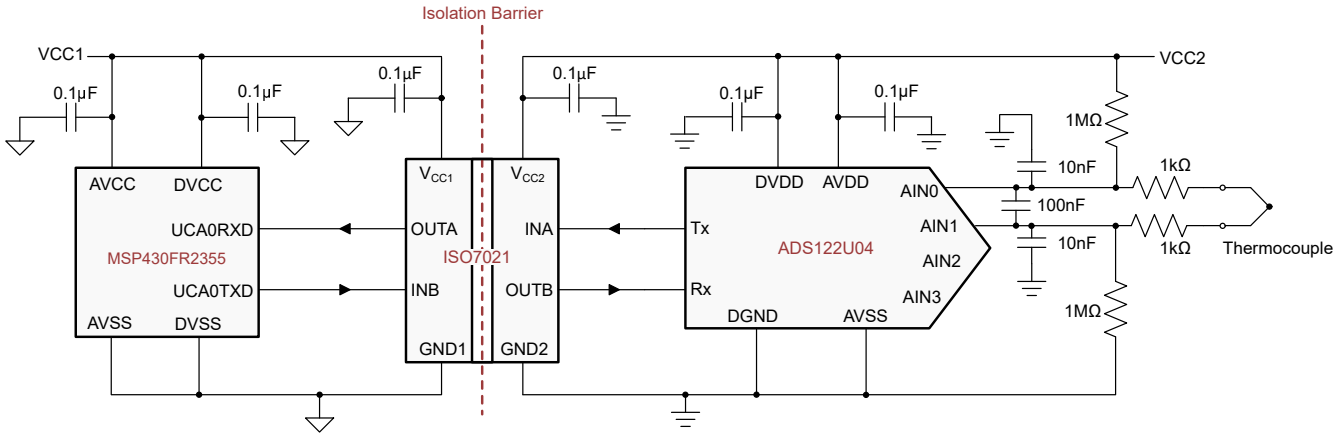


図 9-3. Isolated UART for a Temperature Field Transmitter

9.2.1 Design Requirements

To design with these devices, use the parameters listed in 表 9-2.

表 9-2. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71V to 1.89V or 2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

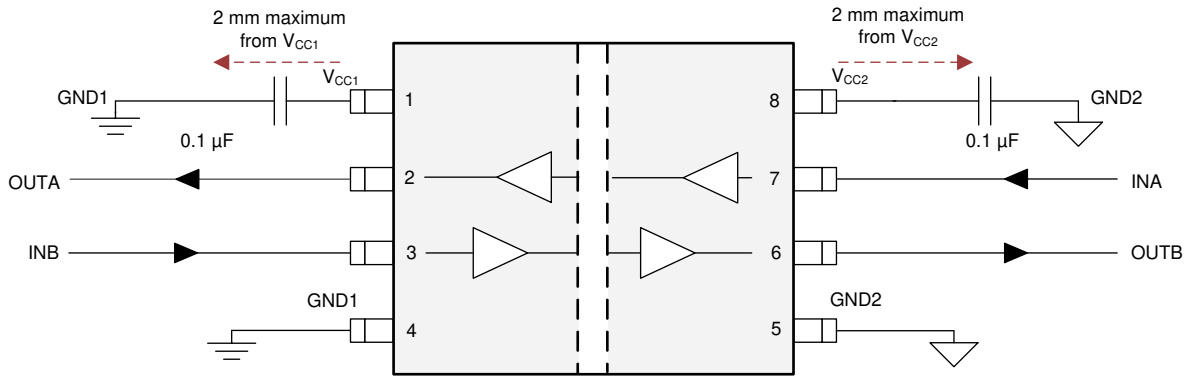


図 9-4. Typical ISO7021 Circuit Hook-up

Copyright © 2024 Texas Instruments Incorporated

9.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 4Mbps.

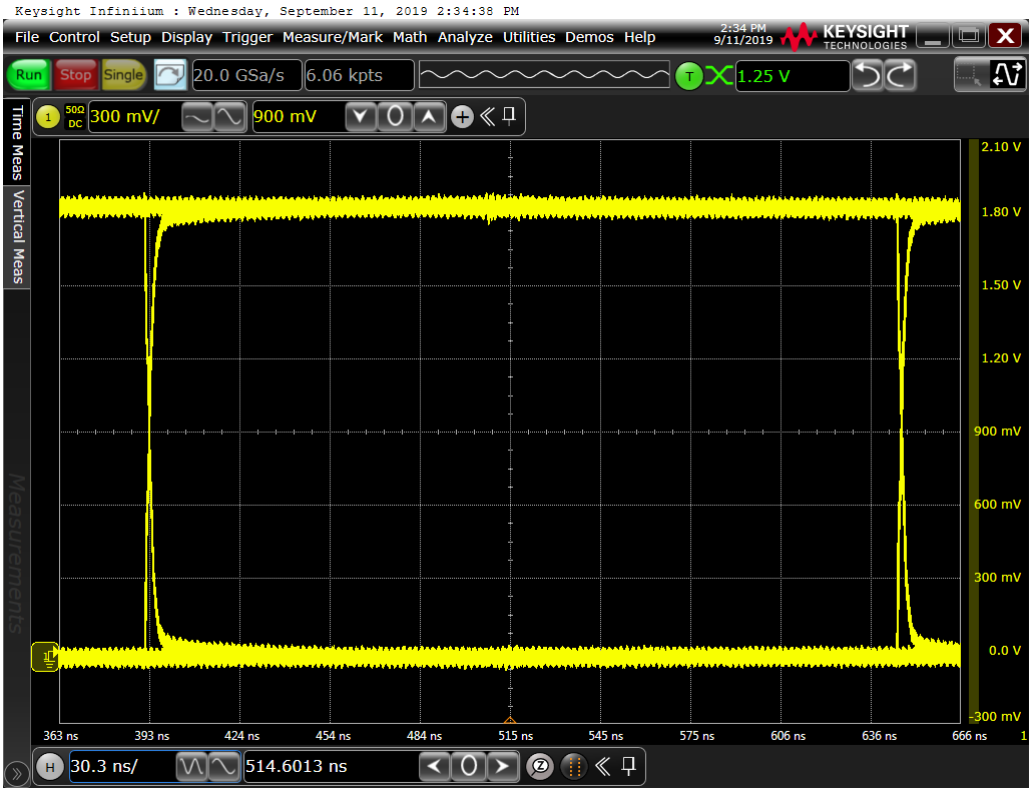


図 9-5. Eye Diagram at 4Mbps PRBS 2^{16} – 1, 1.8V and 25°C

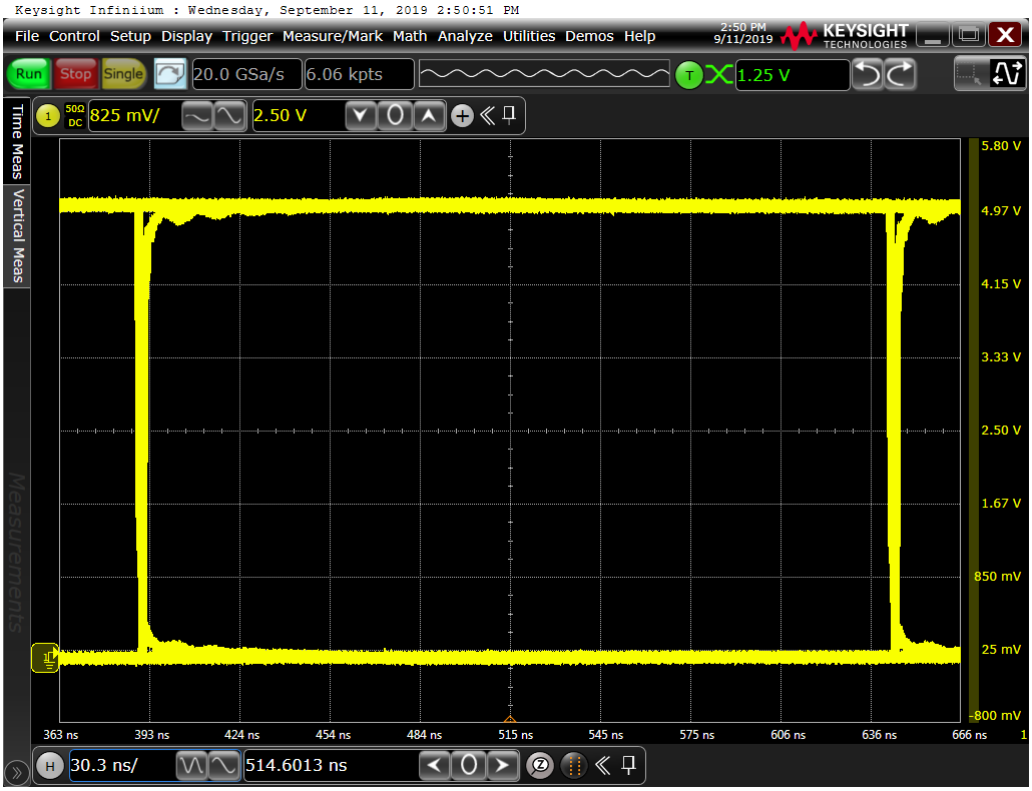


図 9-6. Eye Diagram at 4Mbps PRBS 2^{16} – 1, 5V and 25°C

10 Power Supply Recommendations

Put a 0.1µF bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the SN6501 device or SN6505A device. Refer to the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet for detailed power supply design and transformer selection recommendations.

Copyright © 2024 Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 11-1). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the layers symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the *Digital Isolator Design Guide* for detailed layout recommendations.

11.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

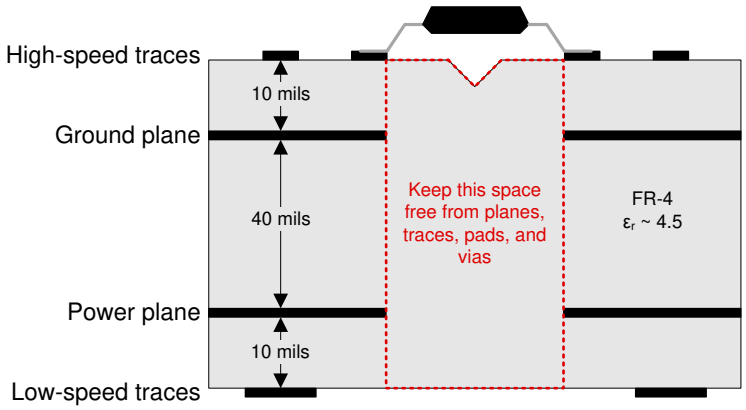


図 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *ADS1220 4-Channel, 2-kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference*, data sheet
- Texas Instruments, *ADS122U04 24-Bit, 4-Channel, 2-kSPS, Delta-Sigma ADC With UART Interface*, data sheet
- Texas Instruments, *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference*, data sheet
- Texas Instruments, *Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications*, Design Guide
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*, data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies, data sheet*
- Texas Instruments, *Isolated power and data interface for low-power applications reference design*, Design Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

12.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2024 Texas Instruments Incorporated

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2020) to Revision C (May 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- ドキュメント全体を通して標準名を以下のように変更:「DIN VDE V 0884-11:2017-01」から「DIN EN IEC 60747-17 (VDE 0884-17)」 1
- ドキュメント全体を通して、IEC/EN/CSA 60950-1 規格への参照を削除 1
- Added Maximum impulse voltage (V_{IMP}) specification per DIN EN IEC 60747-17 (VDE 0884-17) 6
- Changed test conditions and values of Maximum surge isolation voltage (V_{IOSM}) specification per DIN EN IEC 60747-17 (VDE 0884-17) 6
- Added clarification for method b test conditions of Apparent charge (q^{PD}) 6
- Changed working voltage lifetime margin from 87.5% to 50%, minimum required insulation lifetime from 37.5 years to 30 years in *Insulation Lifetime* per DIN EN IEC 60747-17 (VDE 0884-17) 17
- Updated 図 9-2 per DIN EN IEC 60747-17 (VDE 0884-17) 17

Changes from Revision A (October 2019) to Revision B (August 2020) **Page**

- 認証の名前を変更し、完了した ATEX 認証を追加し (予定)、記載して、最初のページを更新。 1
- Added IECEx and ATEX to Safety-Related Certifications 7
- Added セクション 9.1.2 section 19
- Updated pin numbers to reflect 8D package 20

Changes from Revision * (July 2019) to Revision A (October 2019) **Page**

- RTM リリース 1

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7021D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021
ISO7021D.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7021DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021
ISO7021DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
ISO7021FD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021F
ISO7021FD.B	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-55 to 125	
ISO7021FDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7021F
ISO7021FDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

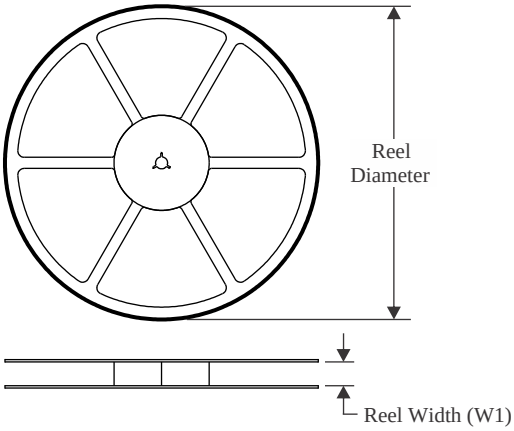
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

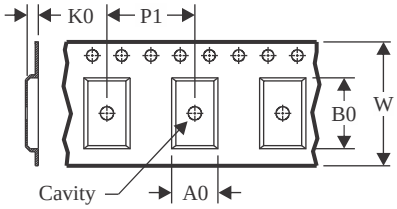
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

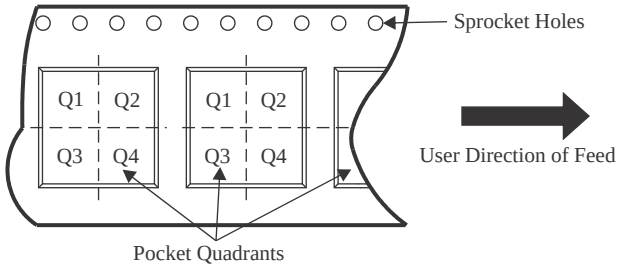


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

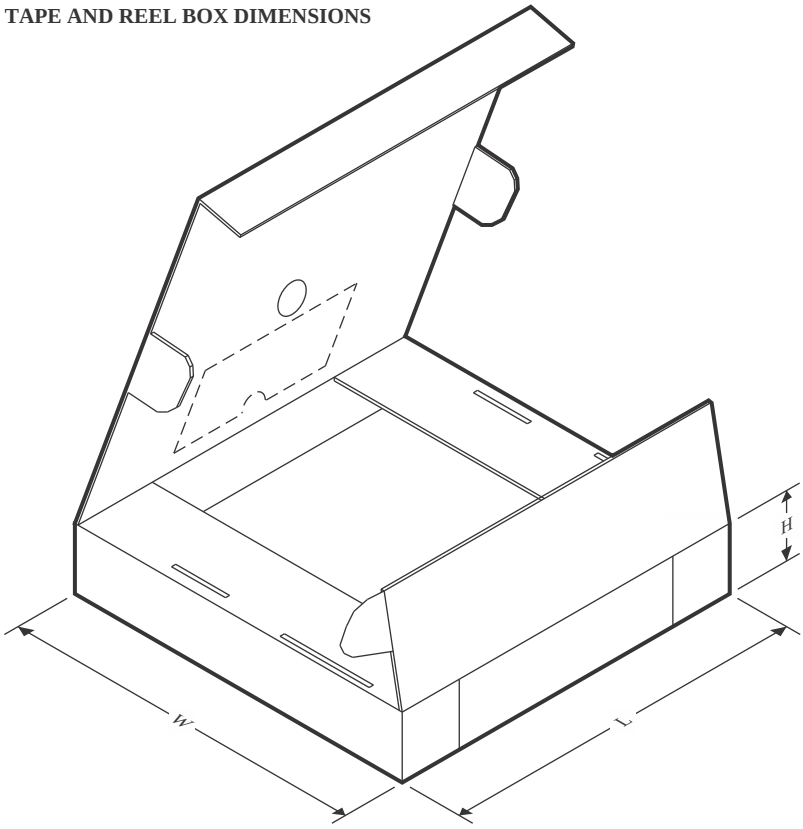
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7021DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7021FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

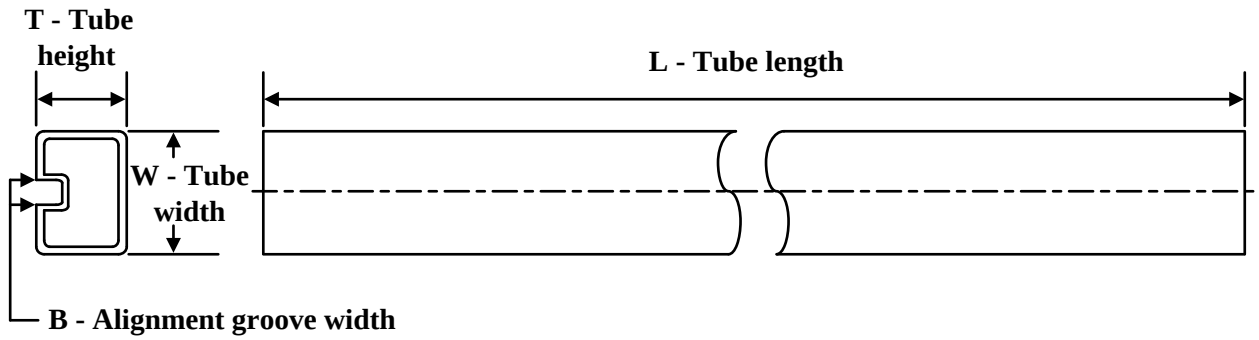
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

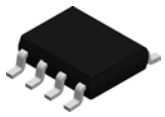
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7021DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7021FDR	SOIC	D	8	2500	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7021D	D	SOIC	8	75	505.46	6.76	3810	4
ISO7021FD	D	SOIC	8	75	505.46	6.76	3810	4

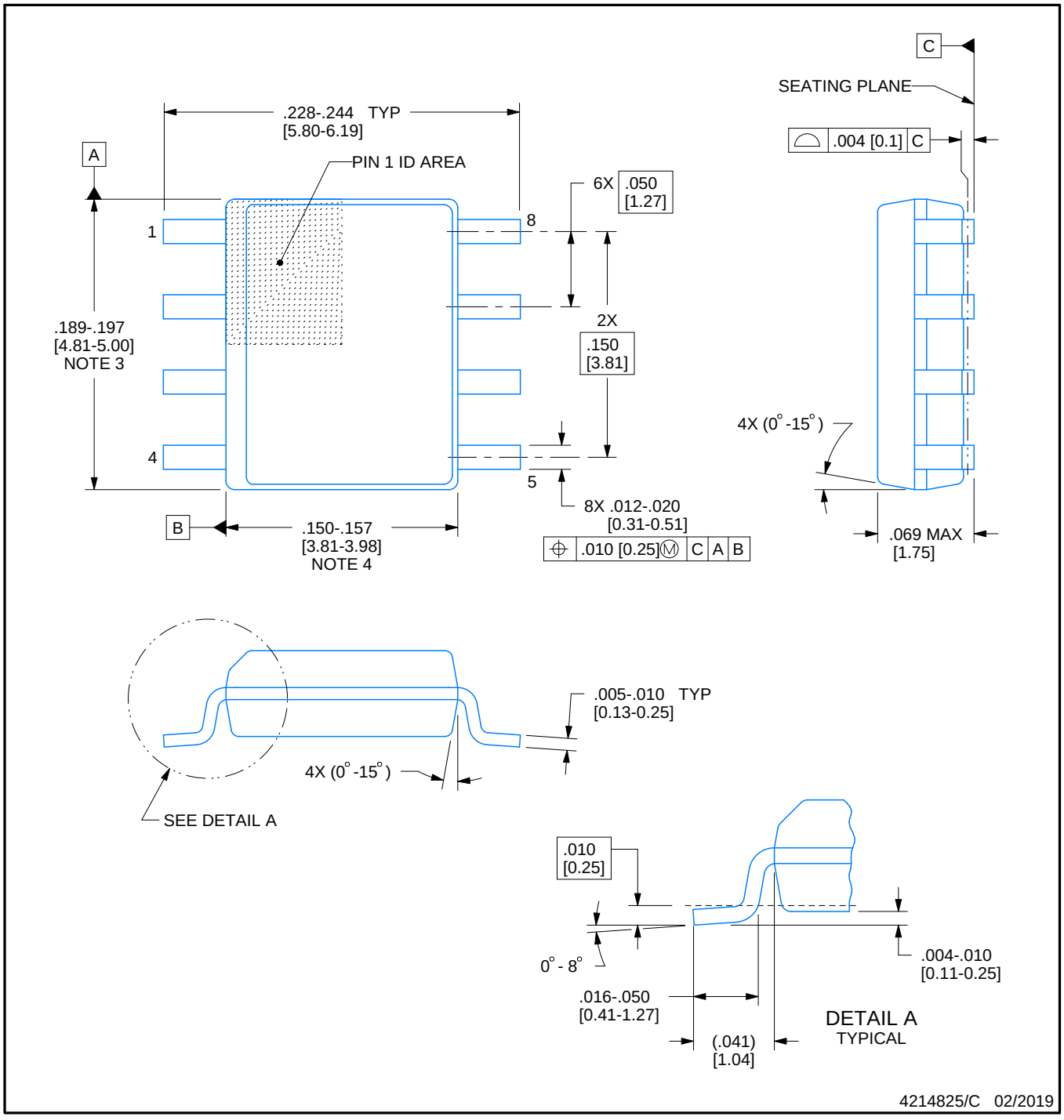


PACKAGE OUTLINE

D0008A

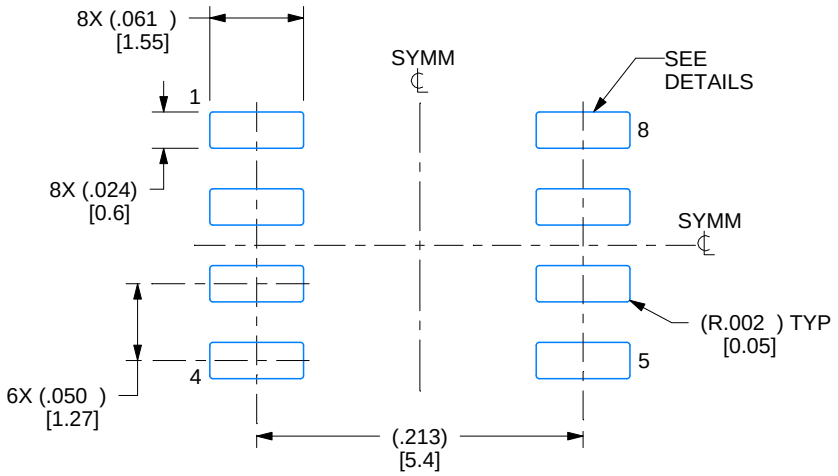
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

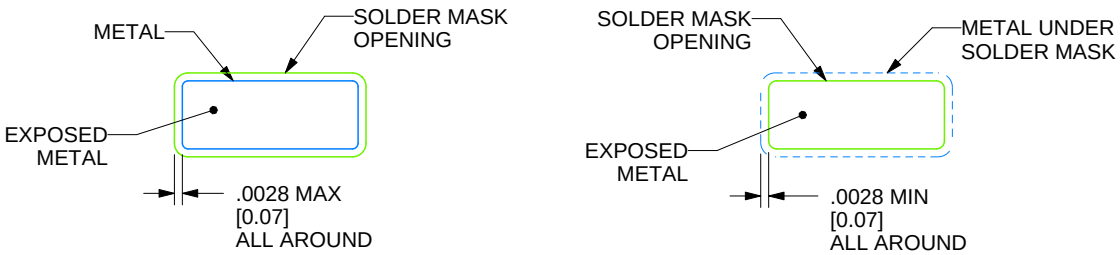


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

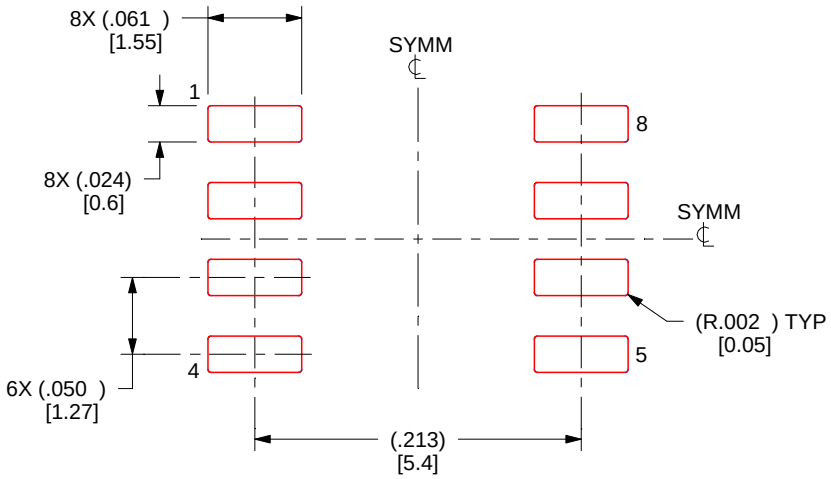
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月