

## ISO724x 高速、クワッドチャンネル デジタル アイソレータ

### 1 特長

- 25 および 150Mbps の信号速度オプション
  - 低いチャンネル間の出力スキュー:  
最大値 1ns
  - 低いパルス幅歪み (PWD) :  
最大値 2ns
  - 低ジッタ成分: 150Mbps で標準値 1ns
- デフォルト出力を選択可能 (ISO7240CF)
- 定格動作電圧で寿命 25 年超 (絶縁寿命予測を参照)
- 4kV の ESD 保護
- 3.3V または 5V 電源で動作
- 高い電磁界耐性  
(『ISO72x デジタル アイソレータの磁界耐性』を参照)
- -40°C ~ +125°C の動作温度範囲
- 安全関連の認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1 認定、IEC 62368-1 認定

### 2 アプリケーション

- ファクトリ オートメーション
  - Modbus
  - Profibus™
  - DeviceNet™ データバス
- コンピュータ ペリフェラル インターフェイス
- サーボ制御インターフェイス
- データ アクイジション

### 3 概要

ISO7240x, ISO7241x, and ISO7242x の各デバイスは、複数のチャンネル構成と出力イネーブル機能を備えたクワッドチャンネル デジタル アイソレータです。これらのデバイスは、テキサス インストルメンツ独自の二酸化ケイ素 (SiO<sub>2</sub>) 絶縁バリアで分離されたロジック入出力バッファを備えています。これらのデバイスは、絶縁型電源と組み合わせて使用することで、高電圧を遮断し、グランドを絶縁し、ノイズ電流がローカル グランドに入り込んでノイズに敏感な回路に干渉したり損傷を与えたりすることを防止します。

ISO7240x ファミリのデバイスは、同じ方向に 4 チャンネルを備えています。ISO7241x ファミリのデバイスは、同じ方向に 3 チャンネル、反対方向に 1 チャンネルを備えています。ISO7242x ファミリのデバイスは、各方向に 2 チャンネルを備えています。

接尾辞 C (C オプション) のデバイスには、TTL 入力スレッショルドと、遷移パルスがデバイスの出力に渡されるのを防ぐノイズ フィルタが入力に備わっています。接尾辞 M (M オプション) のデバイスには、CMOS V<sub>CC</sub>/2 入力スレッショルドが備わっていますが、入力ノイズ フィルタはなく、追加の伝搬遅延も発生しません。

ISO7240CF デバイスは、ピン 7 に入力ディスエーブル機能を備え、CTRL ピン (ピン 10) に High または Low が選択可能なフェイルセーフ出力機能を備えています。フェイルセーフ出力は、CTRL ピンにロジック High が印加された場合、またはピンが未接続のままである場合、ロジック High になります。CTRL ピンにロジック Low 信号が印加されると、フェイルセーフ出力はロジック Low 出力状態になります。ISO7240CF デバイスの入力ディスエーブル機能により、絶縁バリアを通過してデータが出力に渡されるのを防ぎます。入力がディセーブルされるか、V<sub>CC1</sub> がパワーダウンすると、出力は CTRL ピンによって設定されます。

これらのデバイスは、どちらの側でも 3.3V または 5V 電源から電力を供給でき、任意の組み合わせが可能です。信号入力ピンは、使用される電源電圧レベルに関係なく 5V 許容です。

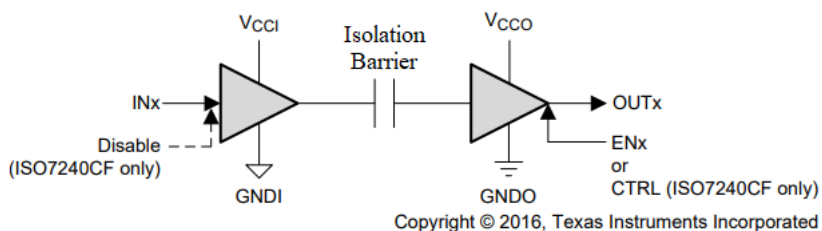
これらのデバイスは、-40°C ~ +125°C の周囲温度範囲で動作するように特性評価されています。



### パッケージ情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)	パッケージサイズ <sup>(2)</sup>
ISO7240CF	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7240C			
ISO7240M			
ISO7241C			
ISO7241M			
ISO7242C			
ISO7242M			

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。  
 (2) パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



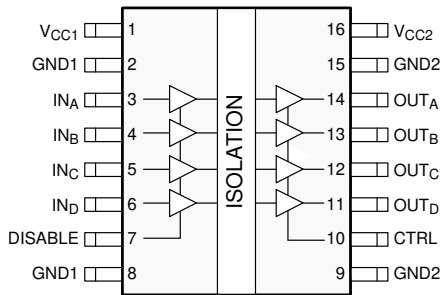
VCCI および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。  
 VCCO および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

### 概略回路図

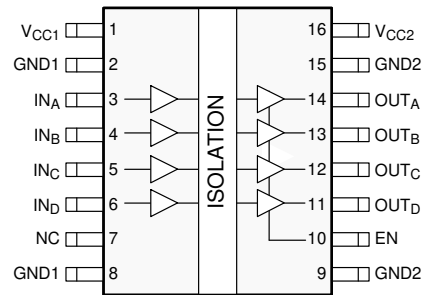
## Table of Contents

<b>1 特長</b> .....	1	5.18 Switching Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation.....	12
<b>2 アプリケーション</b> .....	1	5.19 Switching Characteristics: $V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V Operation.....	13
<b>3 概要</b> .....	1	5.20 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3-V Operation.....	13
<b>4 Pin Configurations and Functions</b> .....	4	5.21 Insulation Characteristics Curves.....	14
<b>5 Specifications</b> .....	5	5.22 Typical Characteristics.....	15
5.1 Absolute Maximum Ratings.....	5	<b>6 Parameter Measurement Information</b> .....	17
5.2 ESD Ratings.....	5	<b>7 Detailed Description</b> .....	20
5.3 Recommended Operating Conditions.....	5	7.1 Overview.....	20
5.4 Thermal Information.....	6	7.2 Functional Block Diagram.....	20
5.5 Power Ratings.....	6	7.3 Feature Description.....	21
5.6 Insulation Specifications.....	6	7.4 Device Functional Modes.....	21
5.7 Safety-Related Certifications.....	7	<b>8 Application and Implementation</b> .....	22
5.8 Safety Limiting Values.....	7	8.1 Application Information.....	22
5.9 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation.....	8	8.2 Typical Application.....	22
5.10 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation.....	8	8.3 Power Supply Recommendations.....	26
5.11 Electrical Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation.....	9	8.4 Layout.....	27
5.12 Supply Current Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation.....	9	<b>9 Device and Documentation Support</b> .....	28
5.13 Electrical Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation.....	10	9.1 Documentation Support.....	28
5.14 Supply Current Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation.....	10	9.2 ドキュメントの更新通知を受け取る方法.....	28
5.15 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation.....	11	9.3 サポート・リソース.....	28
5.16 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation.....	11	9.4 Trademarks.....	28
5.17 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation.....	12	9.5 静電気放電に関する注意事項.....	28
		9.6 用語集.....	28
		<b>10 Revision History</b> .....	28
		<b>11 Mechanical, Packaging, and Orderable Information</b> .....	29

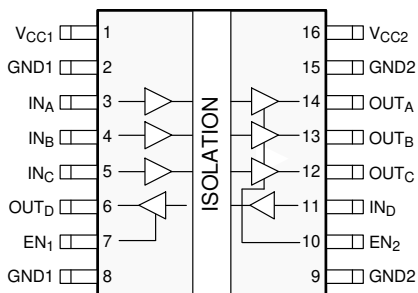
## 4 Pin Configurations and Functions



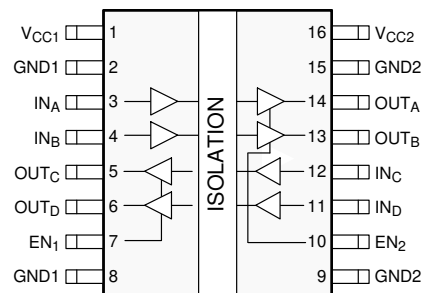
4-1. ISO7240CF DW Package 16-Pin SOIC Top View



4-2. ISO7240C DW Package 16-Pin SOIC Top View



4-3. ISO7241C DW Package 16-Pin SOIC Top View



4-4. ISO7242C DW Package 16-Pin SOIC Top View

表 4-1. Pin Functions

NAME	PIN NO.				Type <sup>(1)</sup>	DESCRIPTION3
	ISO7240CF	ISO7240C	ISO7241C	ISO7242C		
CTRL	10	—	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V <sub>CC1</sub> is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	10	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN <sub>1</sub>	—	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN <sub>1</sub> is high or open and disabled when EN <sub>1</sub> is low.
EN <sub>2</sub>	—	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN <sub>2</sub> is high or open and disabled when EN <sub>2</sub> is low.
GND1	2, 8	2, 8	2, 8	2, 8	—	Ground connection for V <sub>CC1</sub>
GND2	9, 15	9, 15	9, 15	9, 15	—	Ground connection for V <sub>CC2</sub>
IN <sub>A</sub>	3	3	3	3	I	Input, channel A
IN <sub>B</sub>	4	4	4	4	I	Input, channel B
IN <sub>C</sub>	5	5	5	12	I	Input, channel C
IN <sub>D</sub>	6	6	11	11	I	Input, channel D
NC	—	7	—	—	—	No Connect pins are floating with no internal connection
OUT <sub>A</sub>	14	14	14	14	O	Output, channel A
OUT <sub>B</sub>	13	13	13	13	O	Output, channel B
OUT <sub>C</sub>	12	12	12	5	O	Output, channel C
OUT <sub>D</sub>	11	11	6	6	O	Output, channel D
V <sub>CC1</sub>	1	1	1	1	—	Power supply, V <sub>CC1</sub>
V <sub>CC2</sub>	16	16	16	16	—	Power supply, V <sub>CC2</sub>

(1) I = Input; O = Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup> , V <sub>CC1</sub> , V <sub>CC2</sub>	-0.5	6	V
V <sub>I</sub>	Voltage at IN, OUT, EN, DISABLE, CTRL	-0.5	V <sub>CC</sub> + 0.5 <sup>(3)</sup>	V
I <sub>O</sub>	Output current	-15	15	mA
T <sub>J</sub>	Maximum junction temperature		170	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup> , V <sub>CC1</sub> , V <sub>CC2</sub>	3.15		5.5	V
I <sub>OH</sub>	High-level output current	-4			mA
I <sub>OL</sub>	Low-level output current			4	mA
t <sub>ui</sub>	Input pulse width	ISO724xC		40	ns
		ISO724xM	6.67	5	
1/t <sub>ui</sub>	Signaling rate	ISO724xC	0	30 <sup>(1)</sup>	Mbps
		ISO724xM	0	200 <sup>(1)</sup>	
V <sub>IH</sub>	High-level input voltage (IN)			V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage (IN)	0		0.3 x V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage (IN, DISABLE, CTRL, EN on all devices)			5.5	V
V <sub>IL</sub>	Low-level input voltage (IN, DISABLE, CTRL, EN on all devices)	0		0.8	V
T <sub>J</sub>	Junction temperature			150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

- (1) Typical value at room temperature and well-regulated power supply.
- (2) For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V.  
For the 3.3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>			ISO724xx	UNIT
			DW (SOIC)	
			16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	Low-K board	168	°C/W
		High-K board	68.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance		33.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance		33.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter		14.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter		32.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance		n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Power Ratings

V<sub>CC1</sub> = V<sub>CC2</sub> = 5.5 V, T<sub>J</sub> = 150°C, C<sub>L</sub> = 15 pF, Input a 50% duty cycle 25-Mbps square wave (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Maximum power dissipation			220	mW

## 5.6 Insulation Specifications

PARAMETER	TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>			
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	8 mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	8 mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008 mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0884-17); IEC 60112	≥ 400 V
		Material group	II
	Overvoltage Category	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV
		Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-III
<b>DIN EN IEC 60747-17 (VDE 0884-17):<sup>(2)</sup></b>			
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560 V <sub>PK</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	4000 V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(3)</sup>	Method a: After I/O safety test subgroup 2/3. V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s,	≤ 5 pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s,	≤ 5 pC
		Method b1: At routine test (100% production) V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.5 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s,	≤ 5 pC
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(4)</sup>	V <sub>I</sub> = 0.4 sin(2πft), f = 1 MHz	2 pF
R <sub>IO</sub>	Isolation resistance, input to output <sup>(4)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup> Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup> Ω
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup> Ω
	Pollution degree		2
	Climatic category		40/125/21
<b>UL 1577</b>			

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 2500 V <sub>RMS</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 3000 V <sub>RMS</sub> , t = 1 s (100% production)	2500	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-terminal device

## 5.7 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

## 5.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 168°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 170°C, T <sub>A</sub> = 25°C, see <a href="#">5-2</a>			156	mA
		R <sub>θJA</sub> = 168°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 170°C, T <sub>A</sub> = 25°C, see <a href="#">5-2</a>			239	
T <sub>S</sub>	Safety temperature				150	°C

- (1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air [thermal impedance](#) of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

### 5.9 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OFF}$	Sleep mode output current	EN at 0 V, Single channel		0		$\mu$ A
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">6-1</a>	$V_{CCO} - 0.8$			V
		$I_{OH} = -20$ $\mu$ A, See <a href="#">6-1</a>	$V_{CCO} - 0.1$			
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA, See <a href="#">6-1</a>			0.4	V
		$I_{OL} = 20$ $\mu$ A, See <a href="#">6-1</a>			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
$I_{IH}$	High-level input current	IN at $V_{CCI}$			10	$\mu$ A
$I_{IL}$	Low-level input current	IN at 0 V	-10			
$C_I$	Input capacitance to ground	IN at $V_{CC}$ , $V_I = 0.4 \sin(2\pi ft)$ , $f=2$ MHz		2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">6-5</a>	25	50		kV/ $\mu$ s

### 5.10 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ISO7240C/M</b>						
$I_{CC1}$	Supply current, side 1	Quiescent, All channels, no load, EN at 3 V, $V_I = V_{CC}$ or 0 V		1	3	mA
		25 Mbps, All channels, no load, EN at 3 V, 12.5-MHz input-clock signal		7	10.5	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	15	22	mA
			25 Mbps, 12.5-MHz input-clock signal	17	25	
<b>ISO7241C/M</b>						
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6.5	11	mA
			25 Mbps, 12.5-MHz input-clock signal	12	18	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	13	20	mA
			25 Mbps, 12.5-MHz input-clock signal	18	28	
<b>ISO7242C/M</b>						
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	10	16	mA
			25 Mbps, 12.5-MHz input-clock signal	15	24	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	10	16	mA
			25 Mbps, 12.5-MHz input-clock signal	15	24	



### 5.11 Electrical Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OFF}$	Sleep mode output current	EN at 0 V, Single channel		0			$\mu$ A
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">6-1</a>	3.3-V side	$V_{CCO} - 0.4$		V	
			5-V side	$V_{CCO} - 0.8$			
$V_{OL}$	Low-level output voltage	$I_{OH} = -20$ $\mu$ A, See <a href="#">6-1</a>		$V_{CCO} - 0.1$		V	
			$I_{OL} = 4$ mA, See <a href="#">6-1</a>	0.4			
$I_{OL}$		$I_{OL} = 20$ $\mu$ A, See <a href="#">6-1</a>			0.1		
$V_{I(HYS)}$	Input voltage hysteresis			150		mV	
$I_{IH}$	High-level input current	IN at $V_{CCI}$				10	
$I_{IL}$	Low-level input current	IN at 0 V		-10		$\mu$ A	
$C_I$	Input capacitance to ground	IN at $V_{CC}$ , $V_I = 0.4 \sin(2\pi ft)$ , $f=2$ MHz		2		pF	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">6-5</a>		25	50	kV/ $\mu$ s	

### 5.12 Supply Current Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>ISO7240C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	1	3	mA	
			25 Mbps, 12.5-MHz input-clock signal	7	10.5		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	9.5	15	mA	
			25 Mbps, 12.5-MHz input-clock signal	10.5	17		
<b>ISO7241C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6.5	11	mA	
			12.5-MHz input-clock signal	12	18		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	8	13	mA	
			25 Mbps, 12.5-MHz input-clock signal	11.5	18		
<b>ISO7242C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	10	16	mA	
			12.5-MHz input-clock signal	15	24		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6	10	mA	
			25 Mbps, 12.5-MHz input-clock signal	9	14		

### 5.13 Electrical Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{OFF}$	Sleep mode output current	EN at 0 V, Single channel		0			$\mu$ A
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">6-1</a>	3.3-V side	$V_{CCO} - 0.4$			V
			5-V side	$V_{CCO} - 0.8$			
$V_{OL}$	Low-level output voltage	$I_{OH} = -20$ $\mu$ A, See <a href="#">6-1</a>	$V_{CCO} - 0.1$			0.4	V
						0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150			mV
$I_{IH}$	High-level input current	IN at $V_{CC1}$					10
$I_{IL}$	Low-level input current	IN at 0 V		-10			$\mu$ A
$C_I$	Input capacitance to ground	IN at $V_{CC}$ , $V_I = 0.4 \sin(2\pi ft)$ , $f=2$ MHz		2			pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">6-5</a>		25	50		kV/ $\mu$ s

### 5.14 Supply Current Characteristics: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V Operation

For the 5-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 4.5 V to 5.5 V. For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>ISO7240C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	0.5	1.2		mA
			25 Mbps, 12.5-MHz input-clock signal	3	5		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	15	22		mA
			25 Mbps, 12.5-MHz input-clock signal	17	25		
<b>ISO7241C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	4	7		mA
			25 Mbps, 12.5-MHz input-clock signal	6.5	11		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	13	20		mA
			25 Mbps, 12.5-MHz input-clock signal	18	28		
<b>ISO7242C/M</b>							
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6	10		mA
			25 Mbps, 12.5-MHz input-clock signal	9	14		
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	10	16		mA
			25 Mbps, 12.5-MHz input-clock signal	15	24		

### 5.15 Electrical Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation

For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OFF}$	Sleep mode output current	EN at 0 V, single channel		0		$\mu$ A
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">6-1</a>	$V_{CCO} - 0.4$			V
		$I_{OH} = -20$ $\mu$ A, See <a href="#">6-1</a>	$V_{CCO} - 0.1$			
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA, See <a href="#">6-1</a>			0.4	V
		$I_{OL} = 20$ $\mu$ A, See <a href="#">6-1</a>			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
$I_{IH}$	High-level input current	IN at $V_{CCI}$			10	$\mu$ A
$I_{IL}$	Low-level input current	IN at 0 V	-10			
$C_I$	Input capacitance to ground	IN at $V_{CC}$ , $V_I = 0.4 \sin(2\pi ft)$ , $f = 2$ MHz		2		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">6-5</a>	25	50		kV/ $\mu$ s

### 5.16 Supply Current Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3 V Operation

For the 3.3-V operation,  $V_{CC1}$  or  $V_{CC2}$  is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ISO7240C/M</b>						
$I_{CC1}$	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	0.5	1.2	mA
			25 Mbps, 12.5-MHz input-clock signal	3	5	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	9.5	15	mA
			25 Mbps, 12.5-MHz input-clock signal	10.5	17	
<b>ISO7241C/M</b>						
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	4	7	mA
			25 Mbps, 12.5-MHz input-clock signal	6.5	11	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	8	13	mA
			25 Mbps, 12.5-MHz input-clock signal	11.5	18	
<b>ISO7242C/M</b>						
$I_{CC1}$	Supply current, side 1	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6	10	mA
			25 Mbps, 12.5-MHz input-clock signal	9	14	
$I_{CC2}$	Supply current, side 2	All channels, no load, EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V	Quiescent, $V_I = V_{CC}$ or 0 V	6	10	mA
			25 Mbps, 12.5-MHz input-clock signal	9	14	

### 5.17 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 5-V Operation over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xC	See <a href="#">6-1</a>	18		42	ns
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $					2.5	
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xM		8	23	ns	
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $			1	2		
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>	ISO724xC				8	ns
		ISO724xM				0	
$t_{sk(o)}$	Channel-to-channel output skew <sup>(3)</sup>	ISO724xC				2	ns
		ISO724xM				0	
$t_r$	Output signal rise time		See <a href="#">6-1</a>		2.4		ns
$t_f$	Output signal fall time			2.3			
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output		See <a href="#">6-2</a>		15	25	ns
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output			15	25		
$t_{PLZ}$	Propagation delay, low-level-to-high-impedance output			15	25		
$t_{PZL}$	Propagation delay, high-impedance-to-low-level output			15	25		
$t_{fs}$	Failsafe output delay time from input power loss		See <a href="#">6-3</a>		12		$\mu$ s
$t_{wake}$	Wake time from input disable		See <a href="#">6-4</a>		15		$\mu$ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See <a href="#">6-6</a>		1		ns

- (1) Also referred to as pulse skew.  
 (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.  
 (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

### 5.18 Switching Characteristics: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V Operation over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xC	See <a href="#">6-1</a>	20		50	ns
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $					3	
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xM		8	29	ns	
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $			1	2		
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>	ISO724xC				10	ns
		ISO724xM				0	
$t_{sk(o)}$	Channel-to-channel output skew <sup>(3)</sup>	ISO724xC				3	ns
		ISO724xM				0	
$t_r$	Output signal rise time		See <a href="#">6-1</a>		2.4		ns
$t_f$	Output signal fall time			2.3			
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output		See <a href="#">6-2</a>		15	25	ns
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output			15	25		
$t_{PLZ}$	Propagation delay, low-level-to-high-impedance output			15	25		
$t_{PZL}$	Propagation delay, high-impedance-to-low-level output			15	25		
$t_{fs}$	Failsafe output delay time from input power loss		See <a href="#">6-3</a>		18		$\mu$ s
$t_{wake}$	Wake time from input disable		See <a href="#">6-4</a>		15		$\mu$ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See <a href="#">6-6</a>		1		ns

- (1) Also known as pulse skew

- (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

### 5.19 Switching Characteristics: $V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xC	See <a href="#">6-1</a>	22		51	ns	
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $					3		
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xM		8		30	ns	
PWD	Pulse-width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $				1	2		
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>	ISO724xC					10	ns
		ISO724xM			0		5	
$t_{sk(o)}$	Channel-to-channel output skew <sup>(3)</sup>	ISO724xC				2.5	ns	
		ISO724xM		0		1		
$t_r$	Output signal rise time		See <a href="#">6-1</a>		2.4		ns	
$t_f$	Output signal fall time				2.3			
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output		See <a href="#">6-2</a>		15	25	ns	
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output				15	25		
$t_{PLZ}$	Propagation delay, low-level-to-high-impedance output				15	25		
$t_{PZL}$	Propagation delay, high-impedance-to-low-level output				15	25		
$t_{fs}$	Failsafe output delay time from input power loss		See <a href="#">6-3</a>		12		$\mu$ s	
$t_{wake}$	Wake time from input disable		See <a href="#">6-4</a>		15		$\mu$ s	
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See <a href="#">6-6</a>		1		ns	

- (1) Also known as pulse skew
- (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

### 5.20 Switching Characteristics: $V_{CC1}$ and $V_{CC2}$ at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

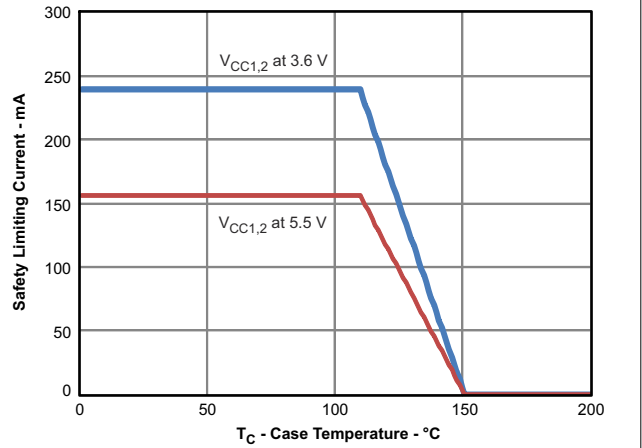
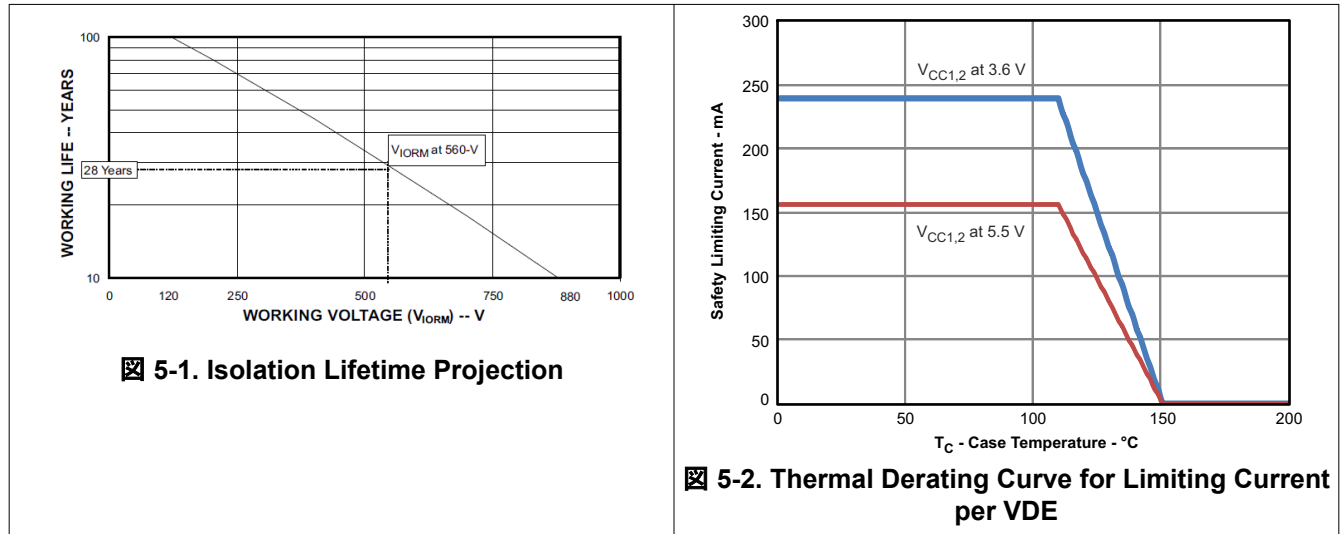
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xC	See <a href="#">6-1</a>	25		56	ns	
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} $ <sup>(1)</sup>					4		
$t_{PLH}$ , $t_{PHL}$	Propagation delay	ISO724xM		8		34	ns	
PWD	Pulse-width distortion $ t_{PHL} - t_{PLH} $ <sup>(1)</sup>				1	2		
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>	ISO724xC					10	ns
		ISO724xM			0		5	
$t_{sk(o)}$	Channel-to-channel output skew <sup>(3)</sup>	ISO724xC				3.5	ns	
		ISO724xM		0		1		
$t_r$	Output signal rise time		See <a href="#">6-1</a>		2.4		ns	
$t_f$	Output signal fall time				2.3		ns	
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output		See <a href="#">6-2</a>		15	25	ns	
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output				15	25		
$t_{PLZ}$	Propagation delay, low-level-to-high-impedance output				15	25		
$t_{PZL}$	Propagation delay, high-impedance-to-low-level output				15	25		
$t_{fs}$	Failsafe output delay time from input power loss		See <a href="#">6-3</a>		18		$\mu$ s	
$t_{wake}$	Wake time from input disable		See <a href="#">6-4</a>		15		$\mu$ s	

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See <a href="#">6-6</a>		1		ns

- (1) Also referred to as pulse skew.
- (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
- (3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## 5.21 Insulation Characteristics Curves



## 5.22 Typical Characteristics

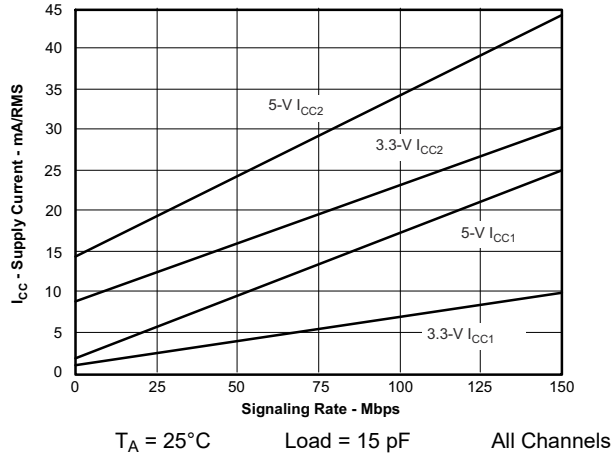


Figure 5-3. ISO7240C/M RMS Supply Current vs Signaling Rate

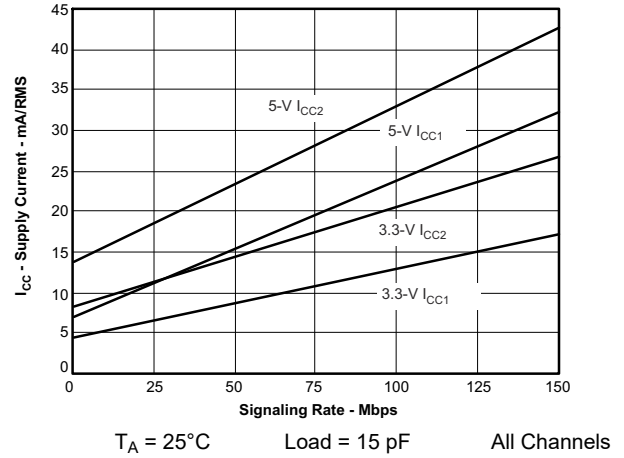


Figure 5-4. ISO7241C/M RMS Supply Current vs Signaling Rate

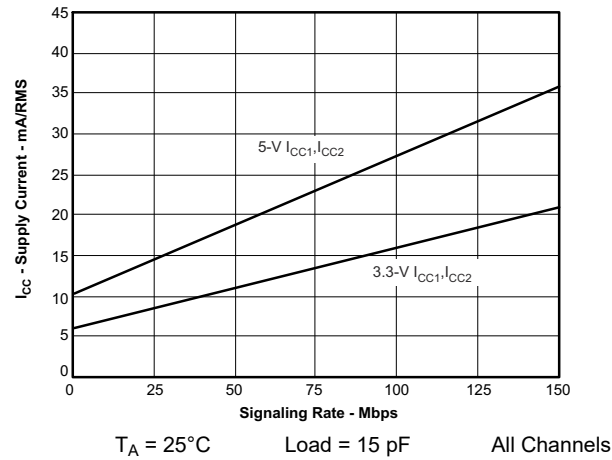


Figure 5-5. ISO7242C/M RMS Supply Current vs Signaling Rate

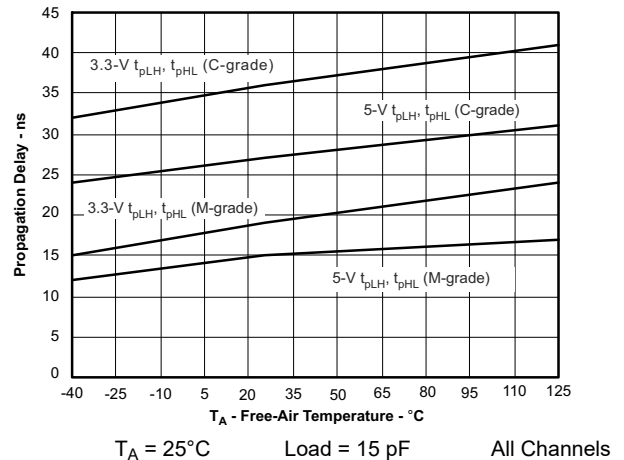


Figure 5-6. Propagation Delay vs Free-Air Temperature

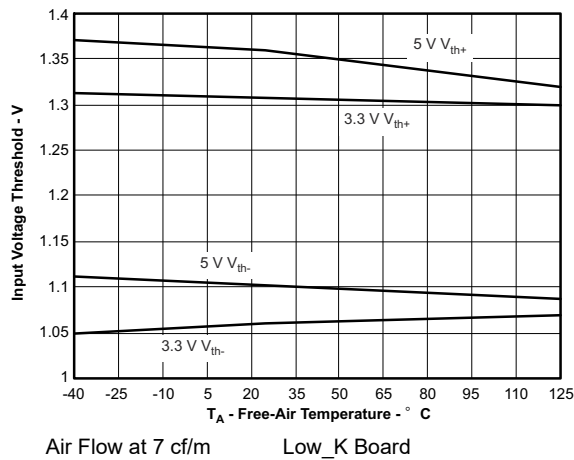


Figure 5-7. Input Voltage Threshold vs Free-Air Temperature

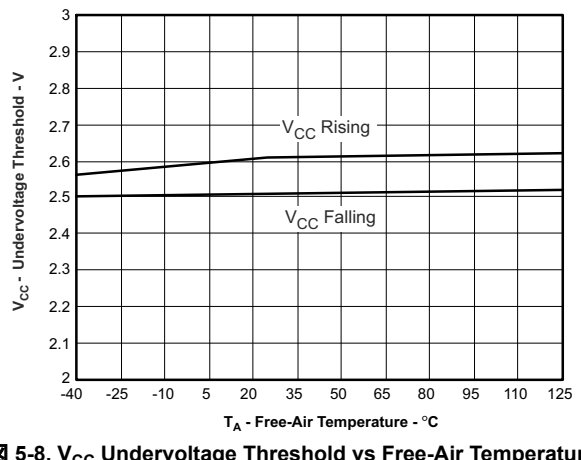
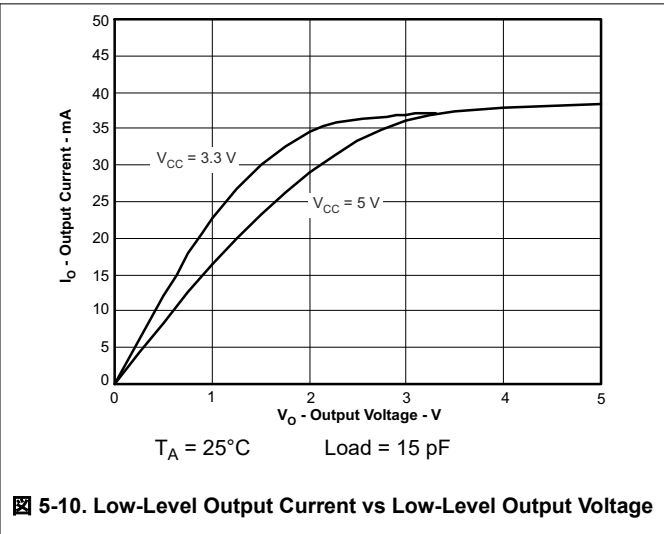
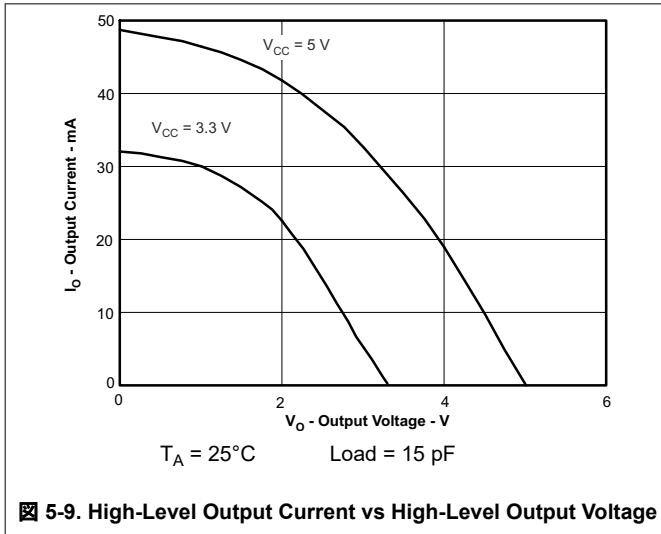


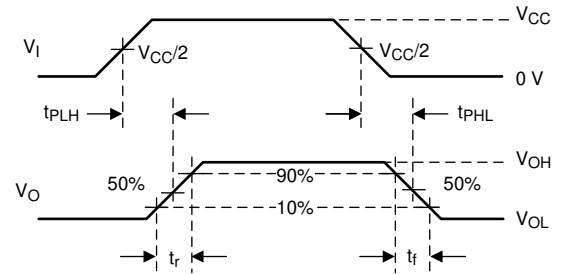
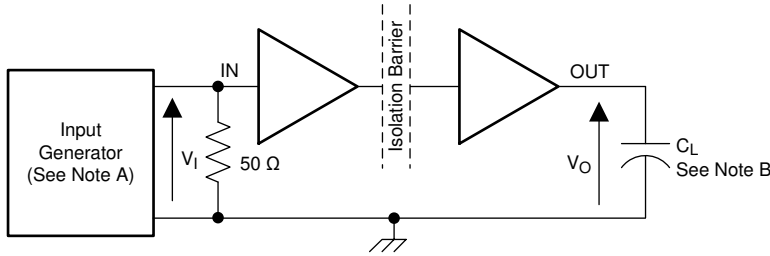
Figure 5-8. VCC Undervoltage Threshold vs Free-Air Temperature

## 5.22 Typical Characteristics (continued)





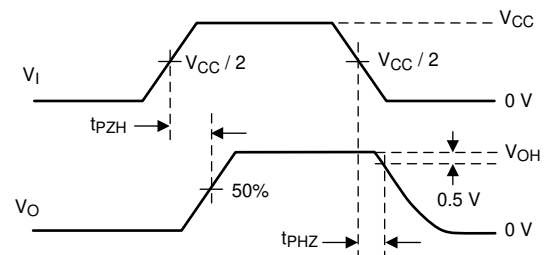
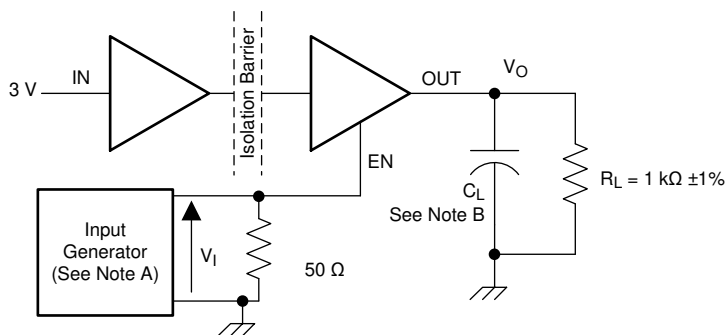
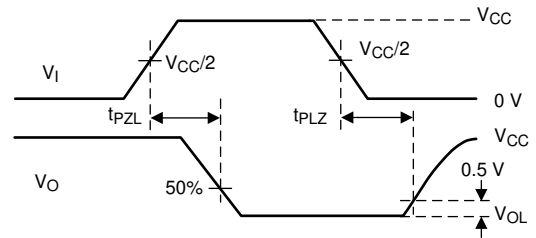
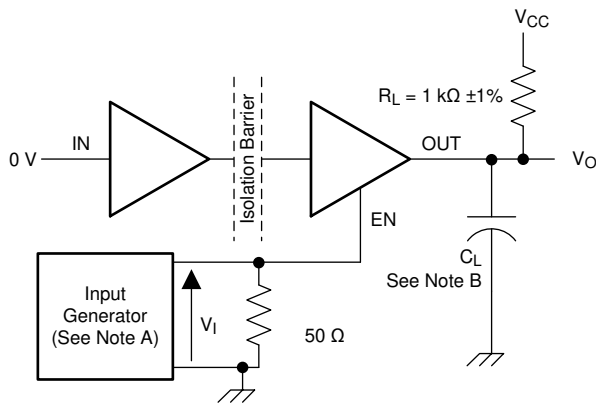
## 6 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated

- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

**6-1. Switching Characteristic Test Circuit and Voltage Waveforms**

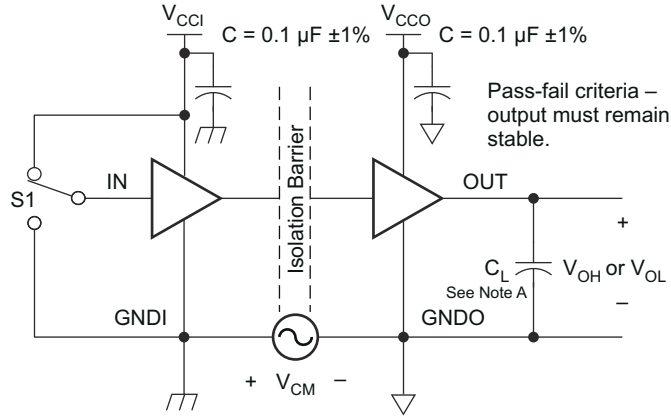


Copyright © 2016, Texas Instruments Incorporated

- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

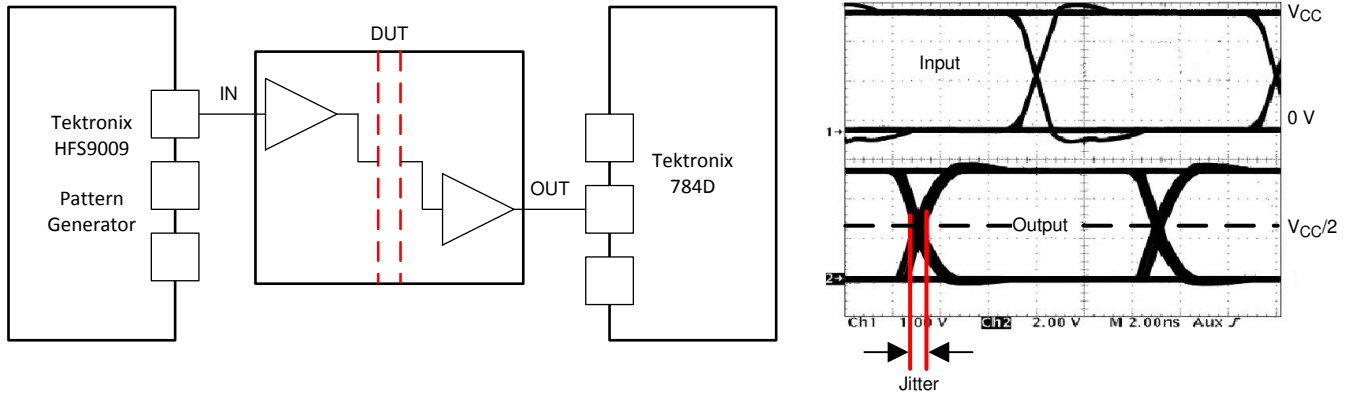
**6-2. Enable or Disable Propagation-Delay Time Test Circuit and Waveform**





- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 50 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ ,  $Z_0 = 50 \Omega$ .

6-5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



Copyright © 2016, Texas Instruments Incorporated

PRBS bit pattern run length is  $2^{16} - 1$ . Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

6-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

## 7 Detailed Description

### 7.1 Overview

The ISO724x family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

### 7.2 Functional Block Diagram

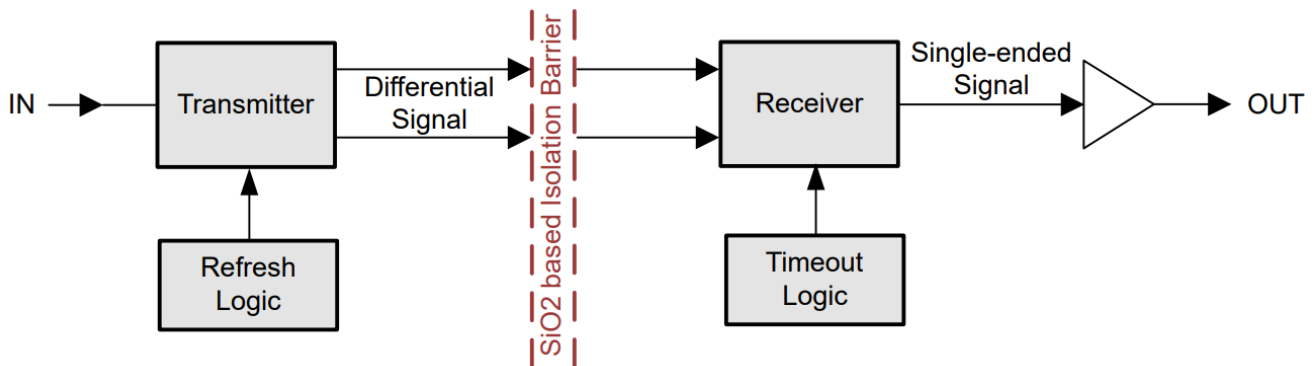


図 7-1. Conceptual Block Diagram of a Digital Isolator

### 7.3 Feature Description

The ISO724x-Q1 family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. 表 7-1 lists these device features.

表 7-1. Device Features

PRODUCT <sup>(1)</sup>	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240CF	25 Mbps	≈1.5 V (TTL)	4/0
ISO7241C	25 Mbps	≈1.5 V (TTL)	3/1
ISO7242C	25 Mbps	≈1.5 V (TTL)	2/2

### 7.4 Device Functional Modes

List of ISO7231C-Q1 functional modes.

表 7-2. Device Function Table ISO7231C-Q1

INPUT V <sub>CC</sub>	OUTPUT V <sub>CC</sub>	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

#### 7.4.1 Device I/O Schematics

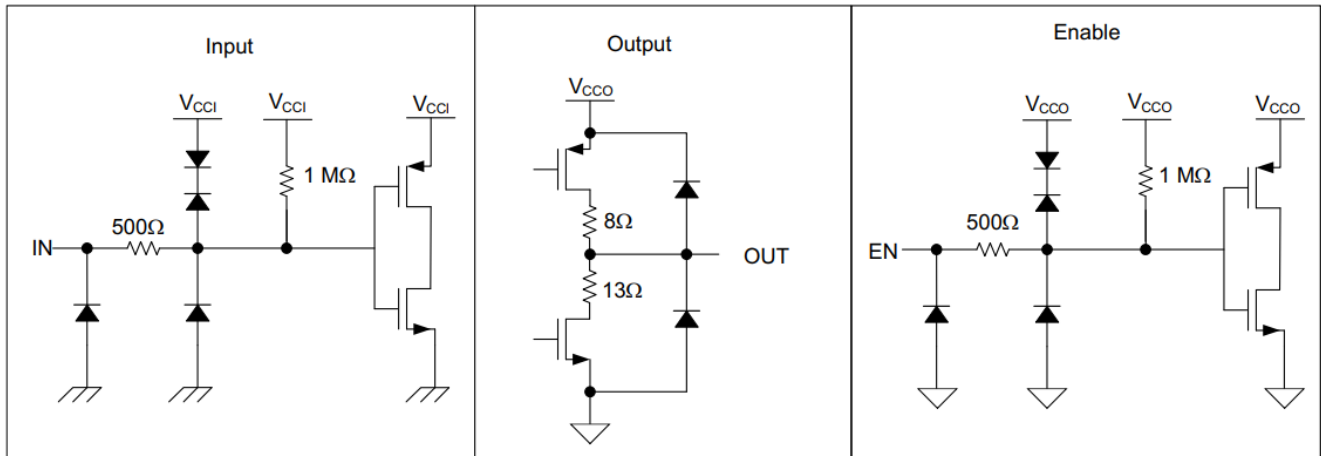


図 7-2. Device I/O Schematics

## 8 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

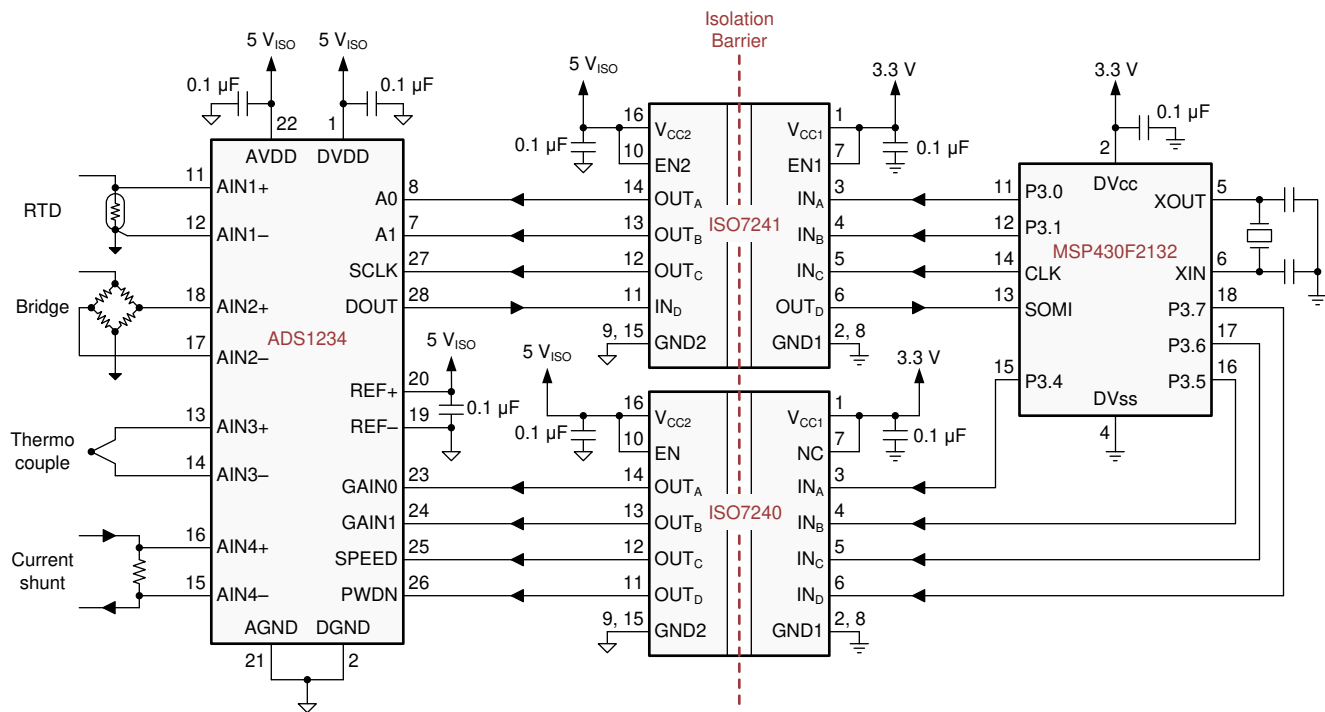
### 8.1 Application Information

The ISO724x family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu$ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

### 8.2 Typical Application

#### 8.2.1 Isolated Data Acquisition System for Process Control

The ISO724x family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in [図 8-1](#).



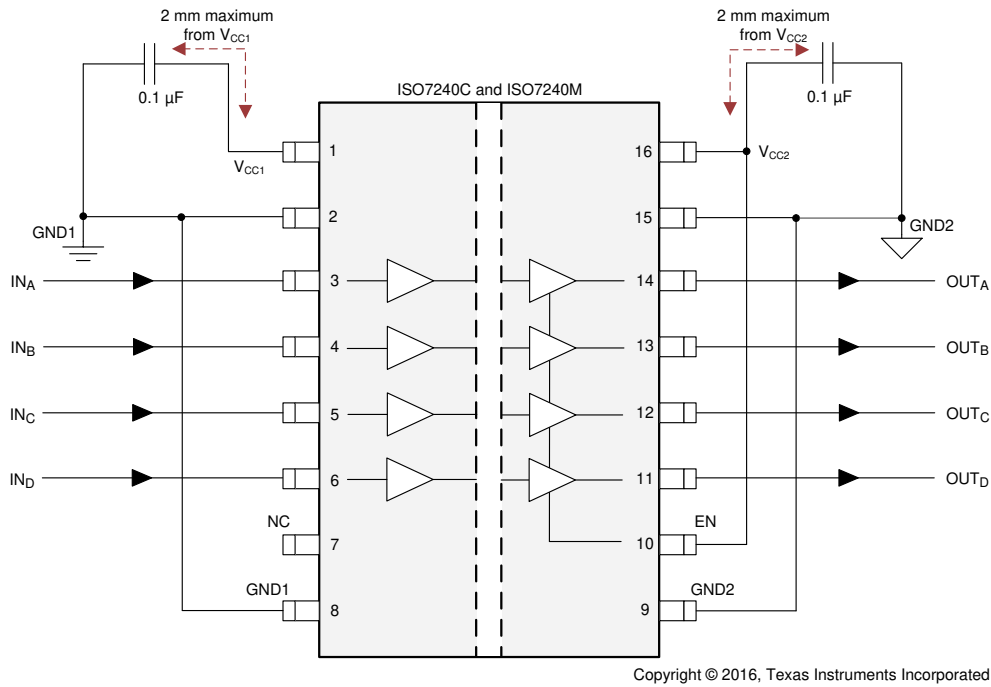
Copyright © 2016, Texas Instruments Incorporated

**図 8-1. Isolated Data Acquisition System for Process Control**

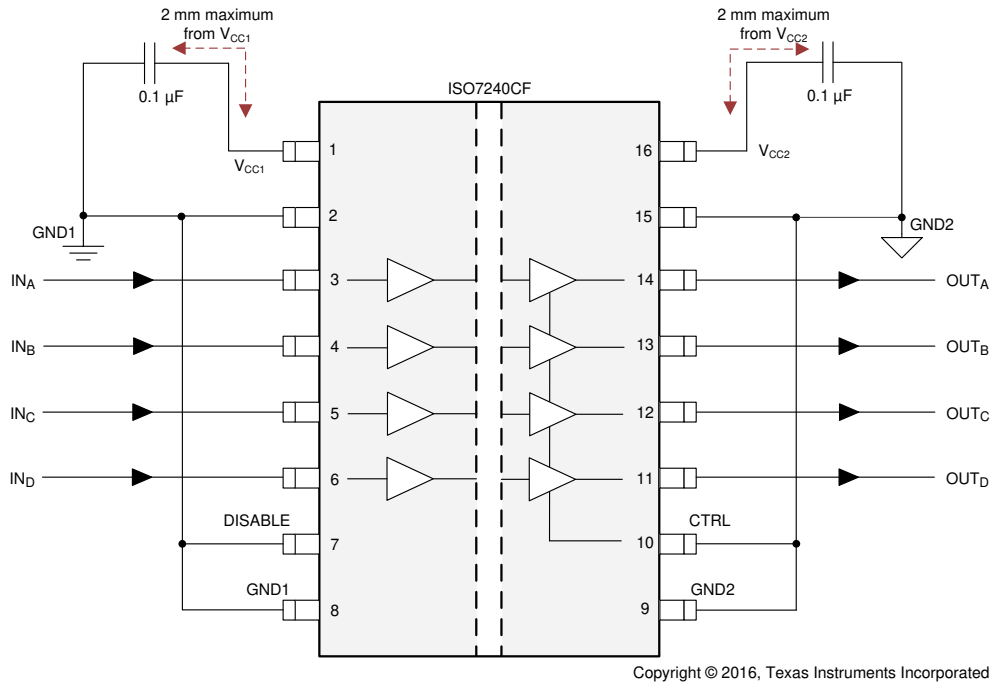
#### 8.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x family of devices only require two external bypass capacitors to operate.

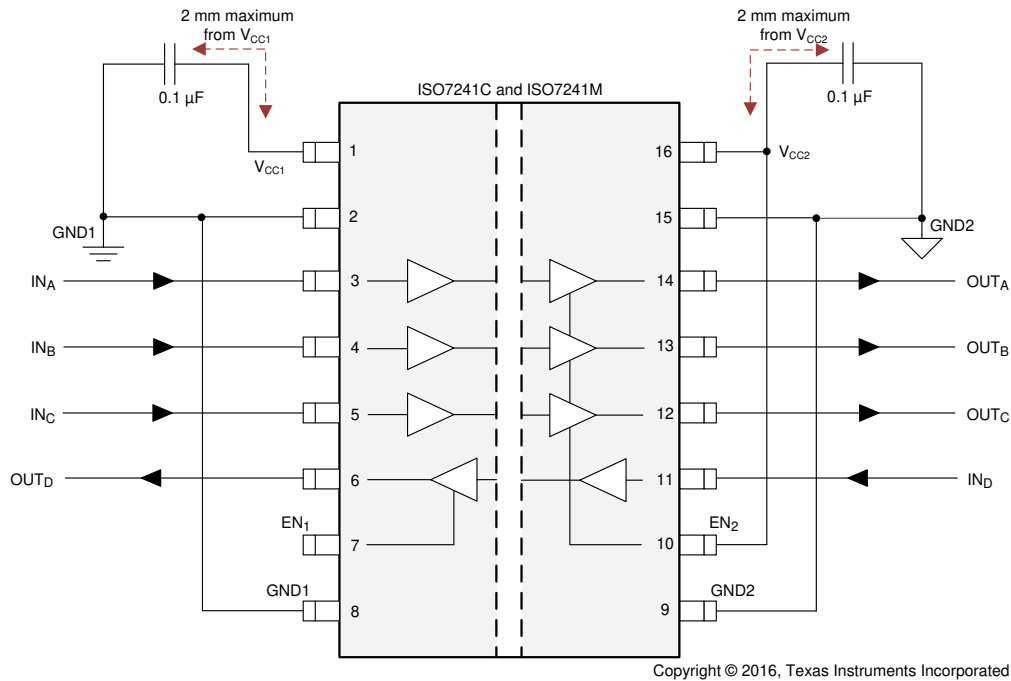
### 8.2.1.2 Detailed Design Procedure



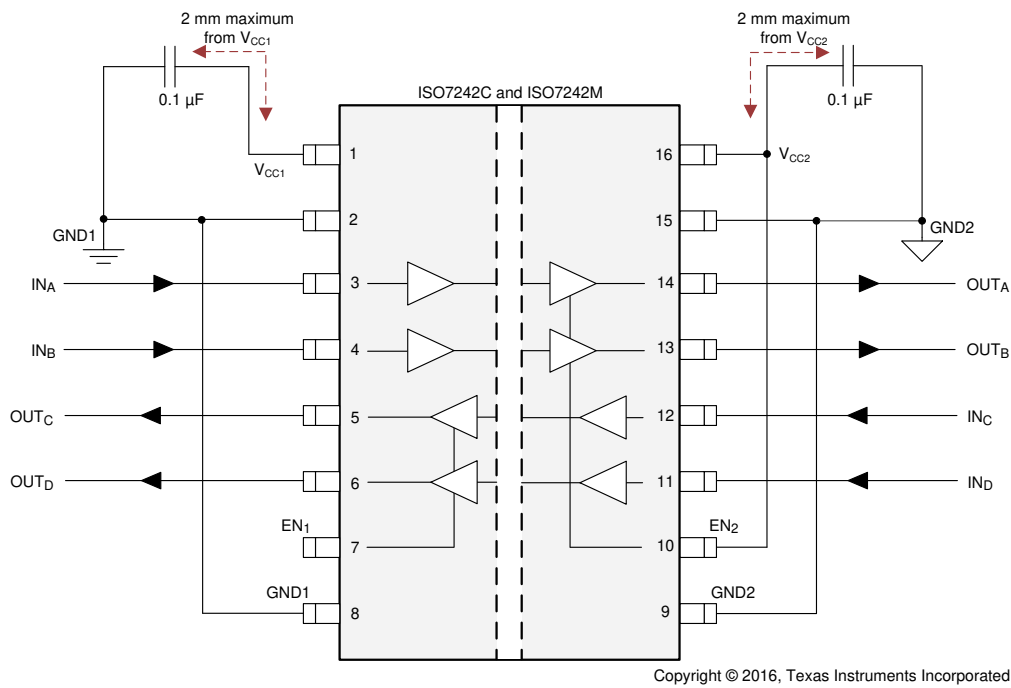
**8-2. ISO7240x Typical Circuit Hook-Up**



**8-3. ISO7240CF Typical Circuit Hook-Up**



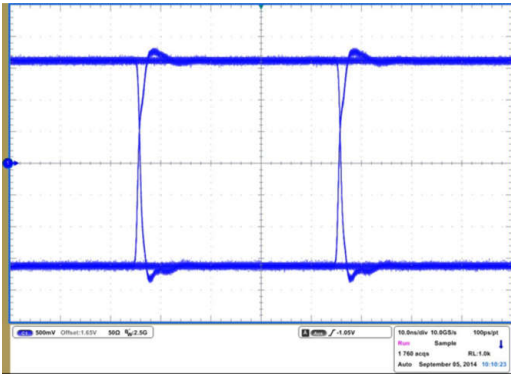
**8-4. ISO7241x Typical Circuit Hook-Up**



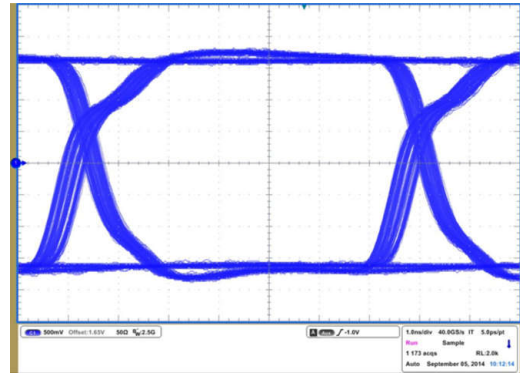
**8-5. ISO7242x Typical Circuit Hook-Up**



### 8.2.1.3 Application Curves



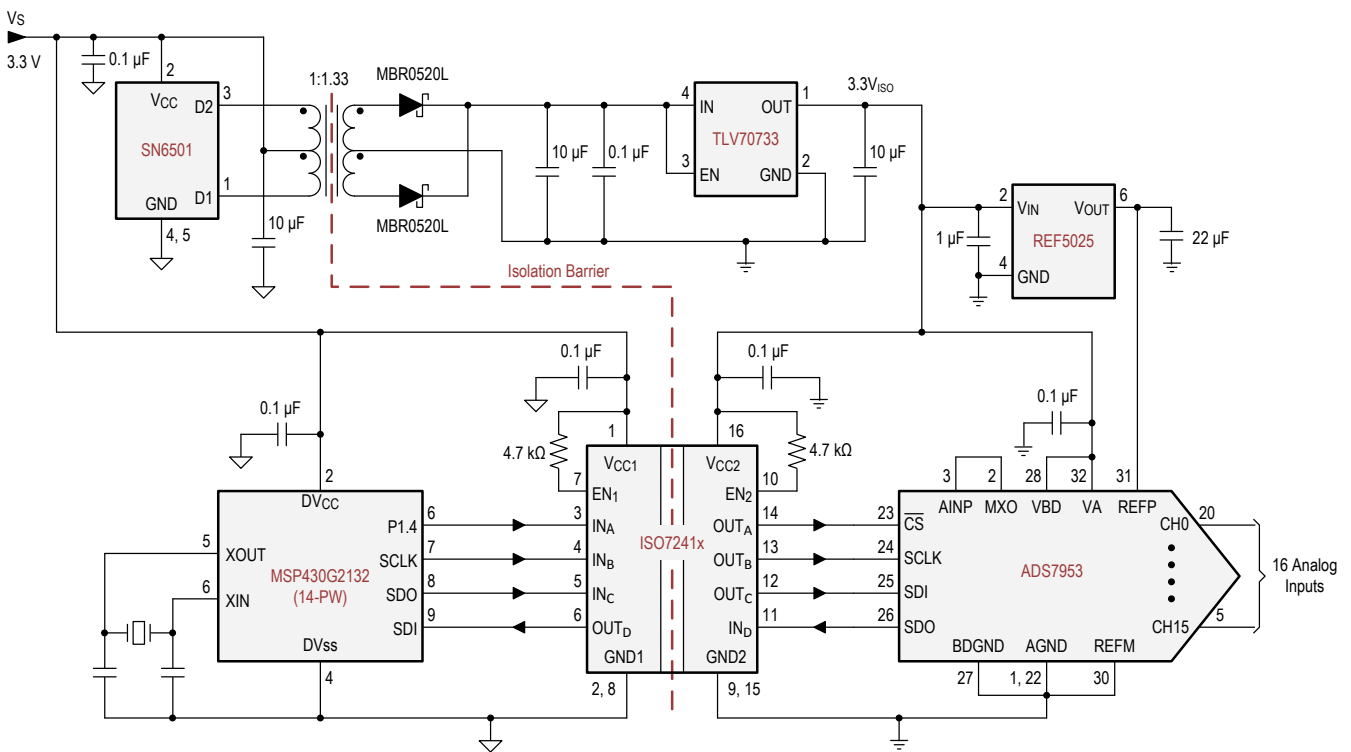
8-6. ISO7242M Eye Diagram at 25 Mbps, 3.3 V and 25°C



8-7. ISO7242M Eye Diagram at 150 Mbps, 3.3 V and 25°C

### 8.2.2 Isolated SPI for an Analog Input Module With 16 Inputs

The ISO7241x family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.



Copyright © 2016, Texas Instruments Incorporated

8-8. Isolated SPI for an Analog Input Module With 16 Inputs

#### 8.2.2.1 Design Requirements

See the [Design Requirements](#) in [セクション 8.2.1](#).

#### 8.2.2.2 Detailed Design Procedure

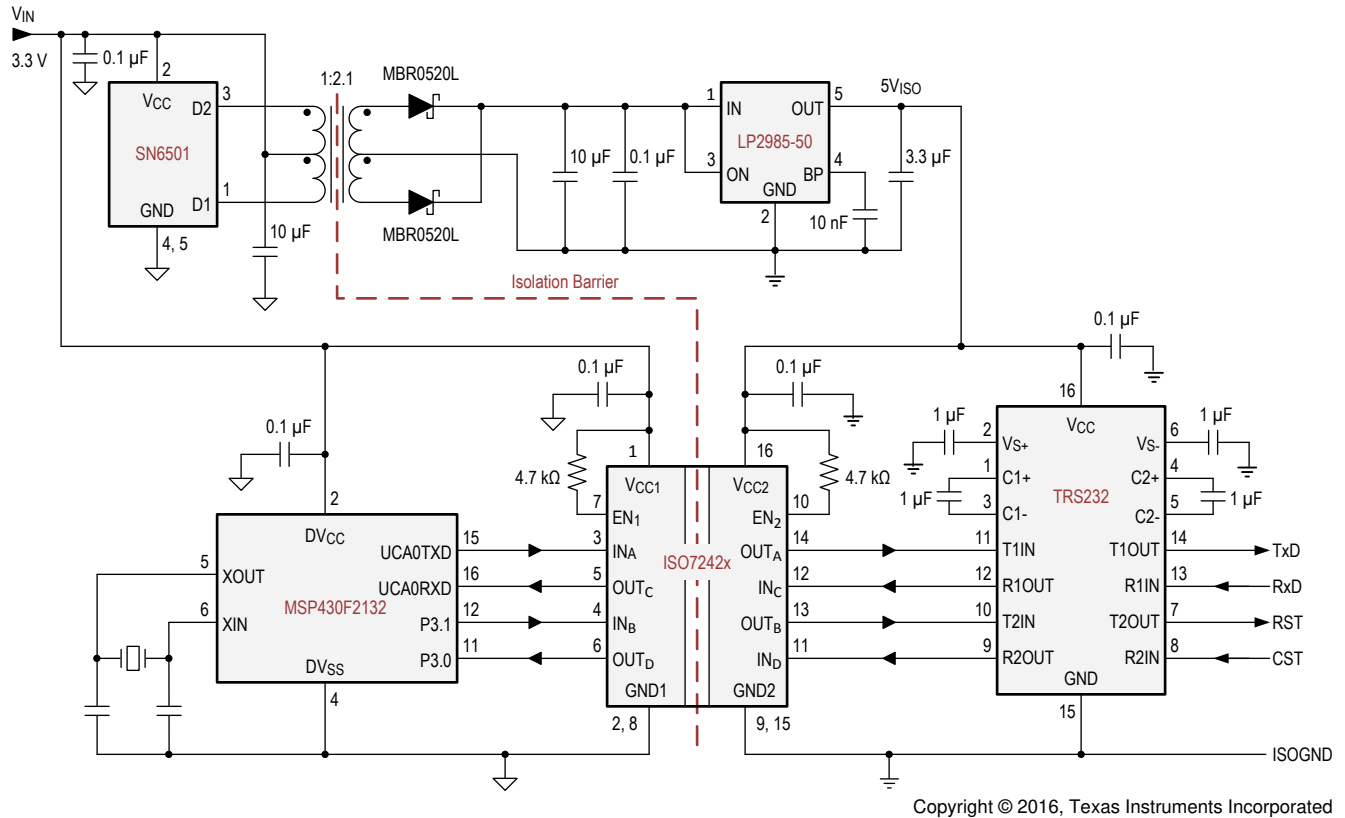
See the [Detailed Design Procedure](#) in [セクション 8.2.1](#).

### 8.2.2.3 Application Curve

See the [Application Curves](#) in [セクション 8.2.1](#).

### 8.2.3 Isolated RS-232 Interface

 8-9 shows a typical isolated RS-232 interface implementation.



Copyright © 2016, Texas Instruments Incorporated

 8-9. Isolated RS-232 Interface

#### 8.2.3.1 Design Requirements

See the [Design Requirements](#) in [セクション 8.2.1](#).

#### 8.2.3.2 Detailed Design Procedure

See the [Detailed Design Procedure](#) in [セクション 8.2.1](#).

#### 8.2.3.3 Application Curve

See the [Application Curves](#) in [セクション 8.2.1](#).

### 8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#).

## 8.4 Layout

### 8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 8-10](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

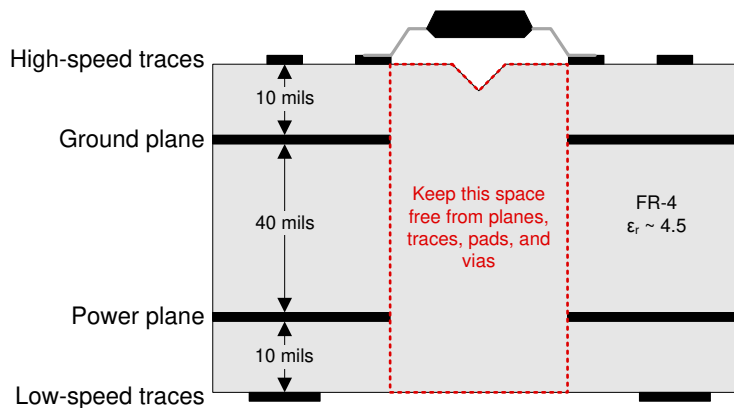
If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to [Digital Isolator Design Guide](#).

#### 8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

#### 8.4.2 Layout Example



**Figure 8-10. Recommended Layer Stack**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- [Digital Isolator Design Guide](#)
- [Isolation Glossary](#)

### 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 9.4 Trademarks

Profibus™ is a trademark of Profibus.

DeviceNet™ is a trademark of Open DeviceNet Vendors Association.

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision U (October 2024) to Revision V (February 2025)

Page

- |                                      |   |
|--------------------------------------|---|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新..... | 1 |
|--------------------------------------|---|

### Changes from Revision T (March 2017) to Revision U (October 2024)

Page

- |  |   |
|--|---|
| • ドキュメント全体を通して容量性絶縁から絶縁バリアに参照を更新.....                | 1 |
| • ドキュメント全体で VDE V 0884-11 を DIN VDE 0884-17 に更新..... | 1 |
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....                 | 1 |

- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations..... 6
- Updated electrical and switching characteristics to match device performance..... 8

<b>Changes from Revision S (April 2016) to Revision T (March 2017)</b>	<b>Page</b>
• Added isolation resistance for $100^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ in the <i>Insulation Specifications</i> table.....	6
• Deleted the maximum transient overvoltage from VDE in the <i>Safety-Related Certifications</i> table.....	7
• Added the <i>Receiving Notification of Documentation Updates</i> and the <i>Community Resources</i> section.....	28

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7240C	
ISO7240CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CFDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7240CF	
ISO7240CFDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240CF	Samples
ISO7240MDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7240M	
ISO7240MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7240MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7241CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7241C	
ISO7241CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241CDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241MDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7241M	
ISO7241MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7241MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7242CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7242C	
ISO7242CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242C	Samples
ISO7242MDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7242M	
ISO7242MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples
ISO7242MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :**

- Automotive : [ISO7240CF-Q1](#), [ISO7241C-Q1](#), [ISO7242C-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240CFDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240CFDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

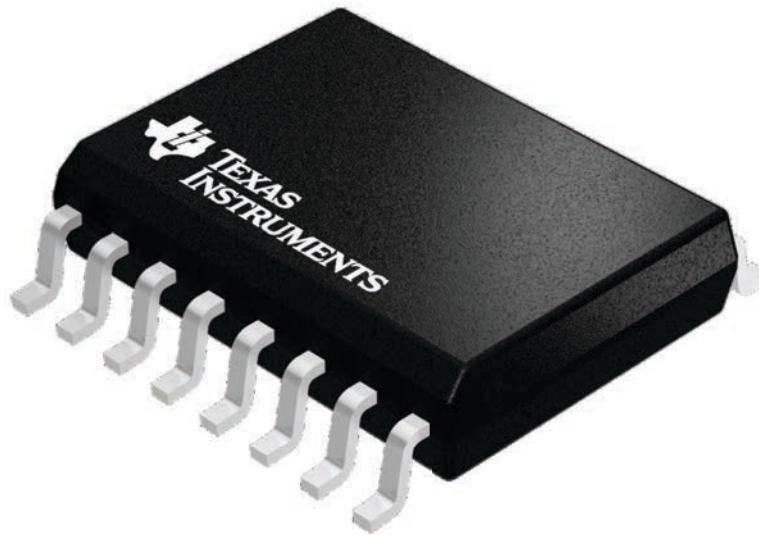
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



# DW0016B

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

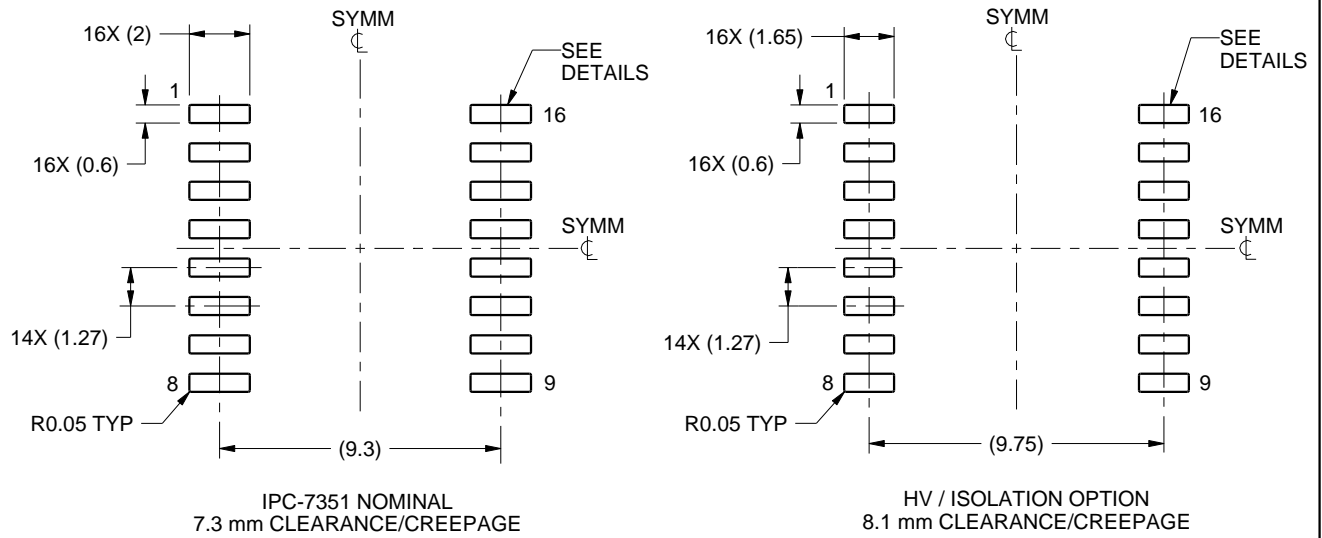
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

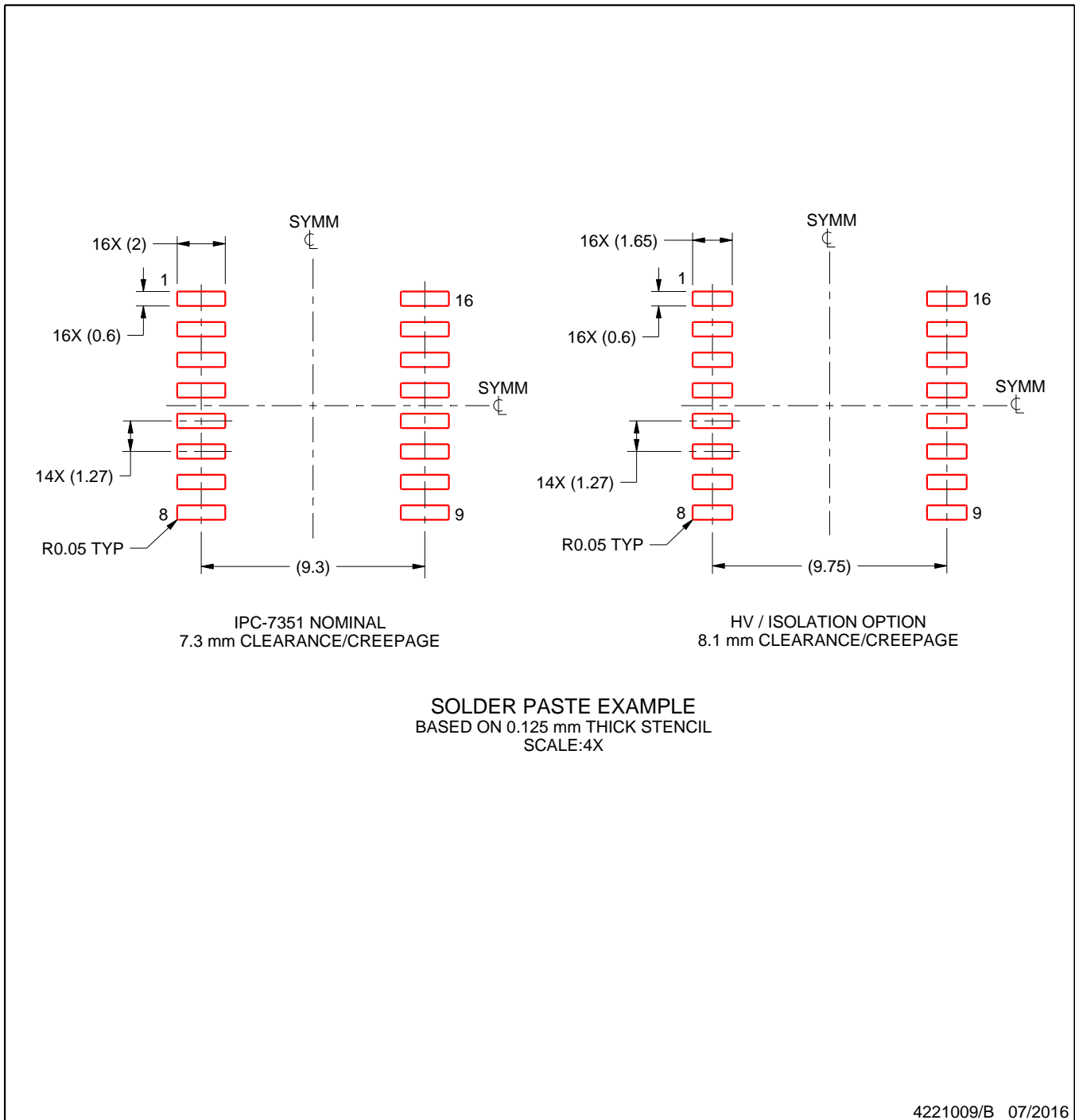
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、ます。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated