LF356-MIL JFET入力オペアンプ

1 特長

- **利点**
  - 高価なハイブリッドおよびモジュールFETオペアンプの代替
  - 堅牢なJFETにより、MOSFET入力デバイスと比較してブローアウトなしの動作
  - ソースのインピーダンスが高くても低くても、低ノイズ・アプリケーション用に最適 - 非常に低い1/fコーナー
  - ほとんどのモノリシック・アンプと異なり、オフセット調整によりドリフトや同相除去の劣化なし
  - 新しい出力段により、安定性の問題なしに大きな容量性負荷(5,000pF)を使用可能
  - 内部補償および大きな差動入力電圧能力
- **共通機能**
  - 低い入力バイアス電流: 30pA
  - 低い入力オフセット電流: 3pA
  - 高い入力インピーダンス: $10^{12}\Omega$
  - 低い入力ノイズ電流: $0.01pA/\sqrt{Hz}$
  - 高い同相除去率: 100dB
  - 大きなDC電圧ゲイン: 106dB
- **非共通機能**
  - 非常に短いセトリング時間: 0.01%まで1.5µs
  - 高いスルー・レート: 12V/µs
  - 広いゲイン帯域幅: 5MHz
  - 低い入力ノイズ電圧: $12nV/\sqrt{Hz}$

2 アプリケーション

- **高精度の高速インテグレータ**
- **高速D/AおよびA/Dコンバータ**
- **高インピーダンスのバッファ**
- **広帯域、低ノイズ、低ドリフト係数のアンプ**
- **対数アンプ**
- **フォトセル・アンプ**
- **サンプル・アンド・ホールド回路**

3 概要

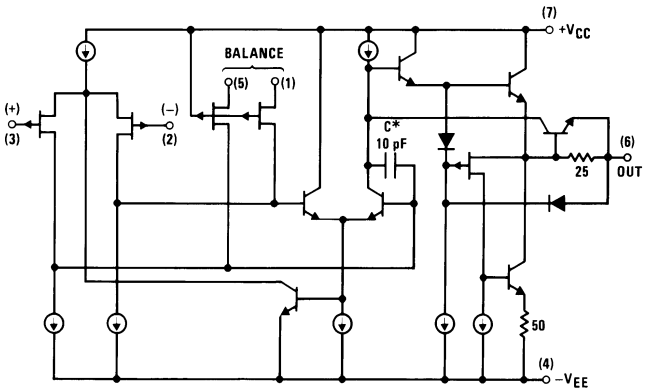
LF356-MILデバイスは、適切に一致した高電圧JFETを、標準バイポーラ・トランジスタと同じチップに組み入れた(BI-FET™テクノロジ)、最初のモノリシックJFET入力オペアンプです。これらのアンプは低い入力バイアス電流とオフセット電流、低いオフセット電圧とオフセット電圧ドリフト係数を特長とし、オフセット調整によってドリフト係数や同相除去が劣化しません。また、これらのデバイスは高いスルー・レート、広い帯域幅、非常に短いセトリング時間、低い電圧および電流ノイズ、低い1/fノイズ・コーナーも実現するよう設計されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LF356-MIL	SOIC (8)	4.90mm×3.91mm
	TO-CAN (8)	9.08mm×9.08mm
	PDIP (8)	9.81mm×6.35mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



LF357シリーズで3pF

目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 AC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V ... 4
6.6 DC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V ... 4
6.7 DC Electrical Characteristics ... 5
6.8 Power Dissipation Ratings ... 5
6.9 Typical Characteristics ... 6
7 **Detailed Description** ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 12
8 **Application and Implementation** ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 14
8.3 System Examples ... 15
9 **Power Supply Recommendations** ... 22
10 **Layout** ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 23
11 デバイスおよびドキュメントのサポート ... 24
11.1 ドキュメントの更新通知を受け取る方法 ... 24
11.2 コミュニティ・リソース ... 24
11.3 商標 ... 24
11.4 静電気放電に関する注意事項 ... 24
11.5 Glossary ... 24
12 メカニカル、パッケージ、および注文情報 ... 24

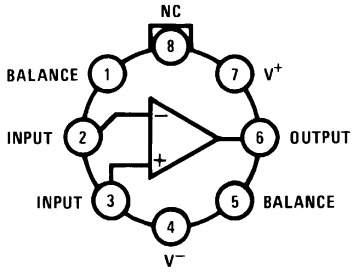
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年6月	*	初版

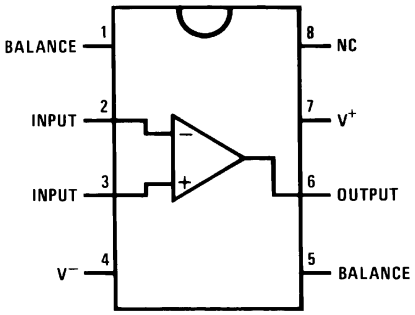
5 Pin Configuration and Functions

LMC Package
8-Pin TO-99
Top View



Available per JM38510/11401 or JM38510/11402

D or P Package
8-Pin SOIC or PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BALANCE	1, 5	I	Balance for input offset voltage
+INPUT	3	I	Noninverting input
–INPUT	2	I	Inverting input
NC	8	—	No connection
OUTPUT	6	O	Output
V+	7	—	Positive power supply
V–	4	—	Negative power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

			MIN	MAX	UNIT
Supply voltage				±18	V
Differential input voltage				±30	V
Input voltage(4)				±16	V
Output short circuit duration			Continuous		—
T_{JMAX}		LMC package		115	°C
		P package		100	
		D package		100	
Soldering information (lead temp.)	TO-99 package	Soldering (10 sec.)		300	°C
	PDIP package	Soldering (10 sec.)		260	
	SOIC package	Vapor phase (60 sec.)		215	
		Infrared (15 sec.)		220	
Storage temperature, T_{stg}			−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.
(3) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(4) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) 100 pF discharged through 1.5-kΩ resistor

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S			±15	V
T_A	0	T_A	70	°C

6.4 Thermal Information

THERMAL METRIC (1)		LF356-MIL		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.5	55.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	44.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.8	32.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	21.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.3	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 AC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew Rate	$A_V = 1$			12		V/μs
GBW	Gain Bandwidth Product				5		MHz
t_s	Settling Time to 0.01% (1)				1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\ \Omega$	f = 100 Hz		15		nV/√Hz
			f = 1000 Hz		12		nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz			0.01		pA/√Hz
		f = 1000 Hz			0.01		pA/√Hz
C_{IN}	Input Capacitance				3		pF

(1) Settling time is defined here, for a unity gain inverter connection using 2-kΩ resistors for the LF15x. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10-V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10 V (See *Settling Time Test Circuit*).

6.6 DC Electrical Characteristics, $T_A = T_J = 25°C$, $V_S = ±15$ V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current			5	10	mA

6.7 DC Electrical Characteristics

See (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	R_S = 50 Ω	T_A = 25°C		3	10	mV
			Over temperature			13	
$\Delta V_{OS}/\Delta T$	Average TC of input offset voltage	R_S = 50 Ω			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in average TC with V_{OS} adjust	R_S = 50 Ω(2)			0.5		µV/°C per mV
I_{OS}	Input offset current	T_J = 25°C(1) (3)			3	50	pA
		$T_J \le T_{HIGH}$				2	nA
I_B	Input bias current	T_J = 25°C(1) (3)			30	200	pA
		$T_J \le T_{HIGH}$				8	nA
R_{IN}	Input resistance	T_J = 25°C			10^{12}		Ω
A_{VOL}	Large signal voltage gain	V_S = ±15 V, V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Over temperature	15			
V_O	Output voltage swing	V_S = ±15 V, R_L = 10 kΩ		±12	±13		V
		V_S = ±15 V, R_L= 2 kΩ		±10	±12		
V_{CM}	Input common-mode voltage range	V_S = ±15 V	$V_{CM, High}$	10	15.1		V
			$V_{CM, Low}$		−12	−10	
CMRR	Common-mode rejection ratio			80	100		dB
PSRR	Supply voltage rejection ratio(1)			80	100		dB

(1) Unless otherwise stated, these test conditions apply:

Supply Voltage, V_S	V_S = ±15 V
T_A	0°C ≤ T_A ≤ +70°C
T_{HIGH}	+70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open-loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(1) Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

6.8 Power Dissipation Ratings

		MIN	MAX	UNIT
Power Dissipation at T_A = 25°C (1) (2)	LMC Package (Still Air)		400	mW
	LMC Package (400 LF/Min Air Flow)		1000	
	P Package		670	
	D Package		380	

(1) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.

(2) Maximum power dissipation is defined by the package characteristics. Operating the part near the maximum power dissipation may cause the part to operate outside specified limits.

6.9 Typical Characteristics

6.9.1 Typical AC Performance Characteristics

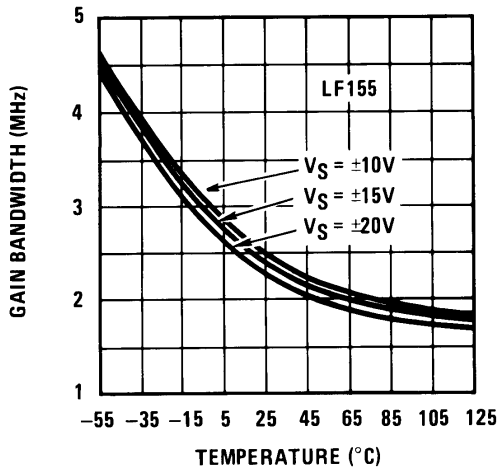


Figure 1. Gain Bandwidth

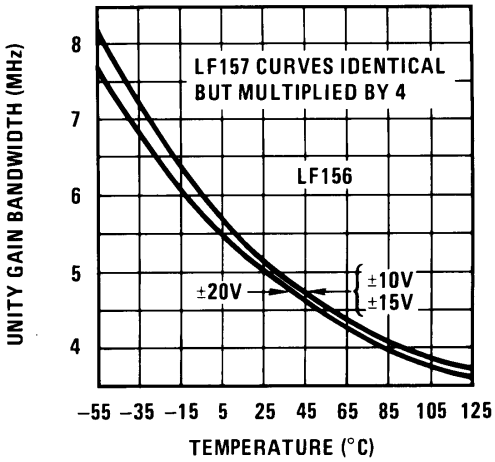


Figure 2. Gain Bandwidth

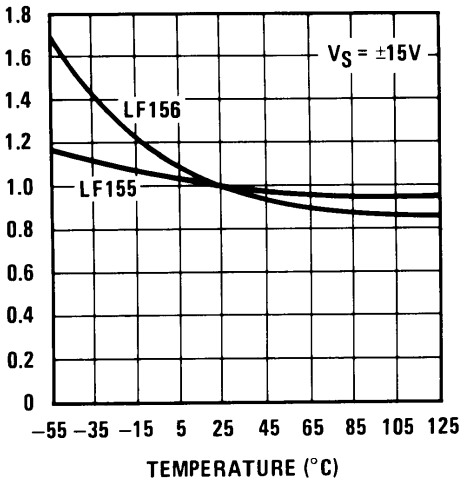


Figure 3. Normalized Slew Rate

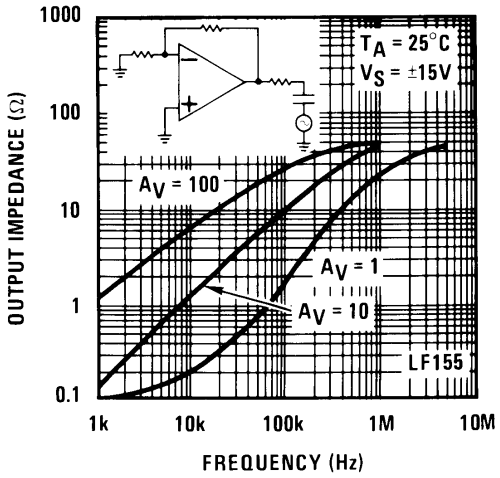


Figure 4. Output Impedance

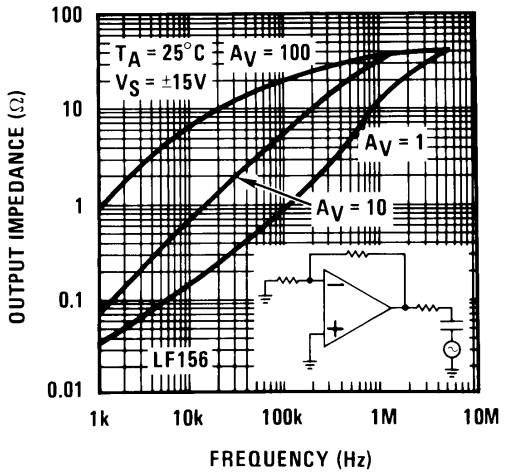


Figure 5. Output Impedance

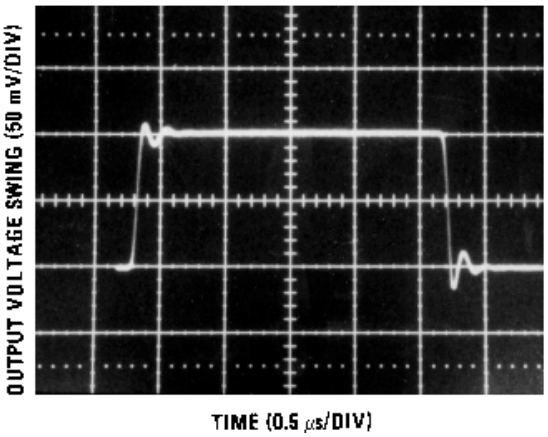


Figure 6. LF155 Small Signal Pulse Response, A_V = +1

Typical AC Performance Characteristics (continued)

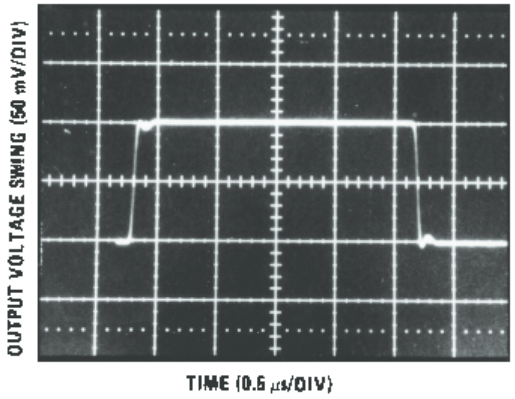


Figure 7. LF156 Small Signal Pulse Response, A_V = +1

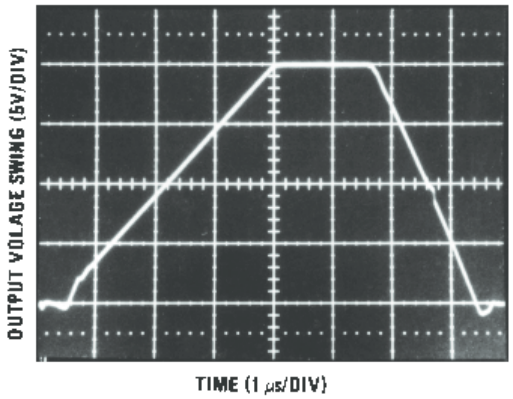


Figure 8. LF155 Large Signal Pulse Response, A_V = +1

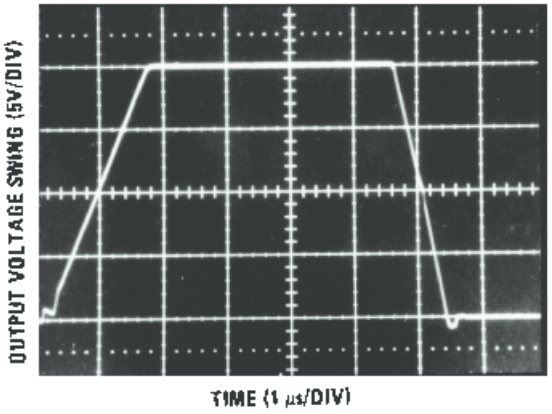


Figure 9. LF156 Large Signal Puls Response, A_V = +1

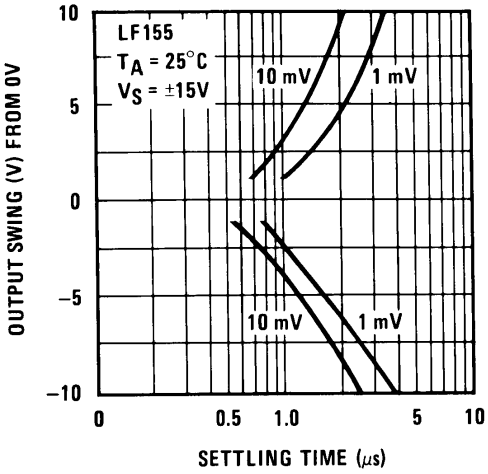


Figure 10. Inverter Settling Time

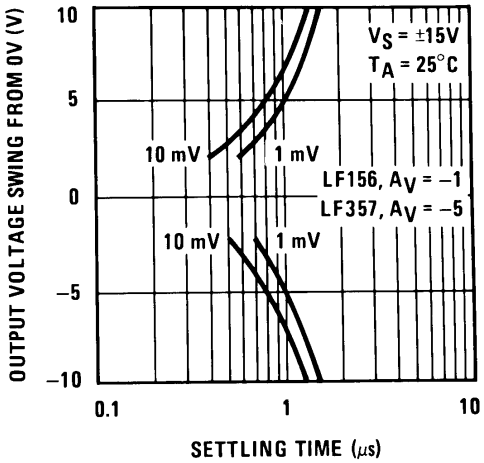


Figure 11. Inverter Settling Time

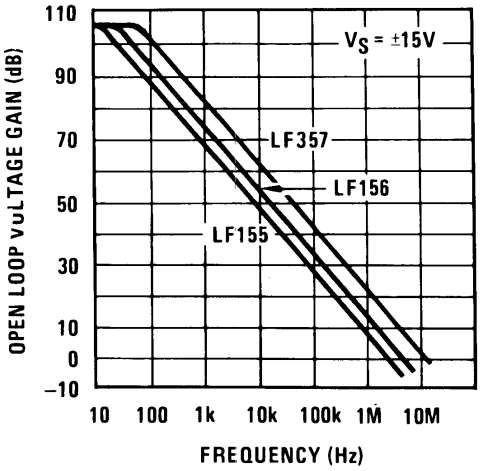


Figure 12. Open-Loop Frequency Response

Typical AC Performance Characteristics (continued)

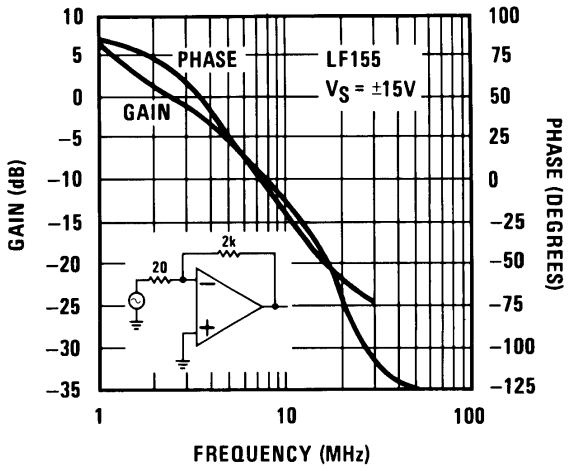


Figure 13. Bode Plot

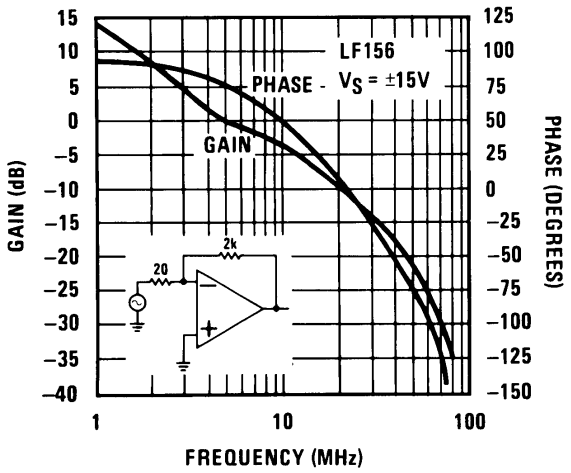


Figure 14. Bode Plot

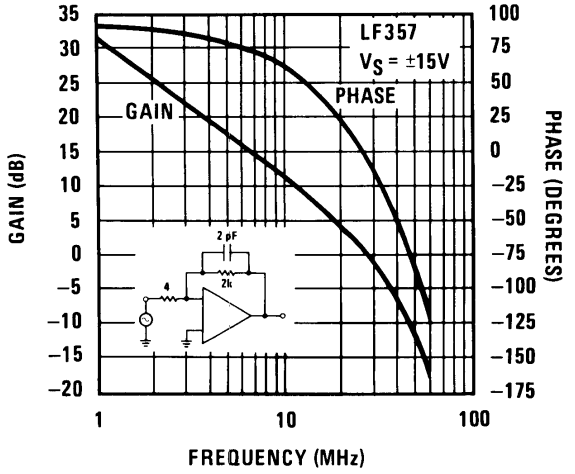


Figure 15. Bode Plot

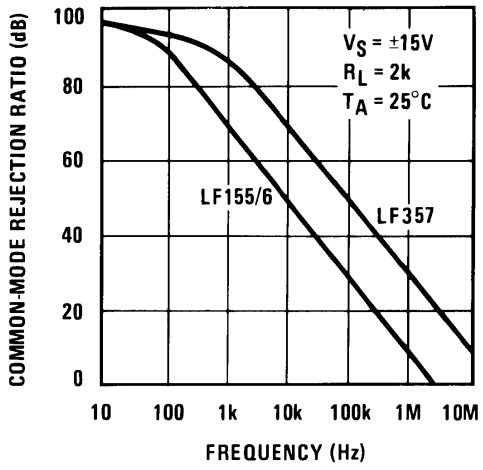


Figure 16. Common-Mode Rejection Ratio

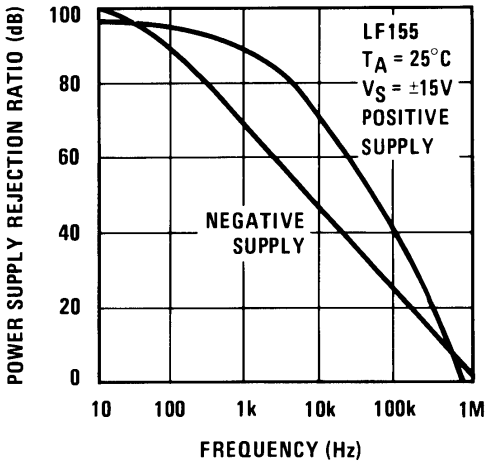


Figure 17. Power Supply Rejection Ratio

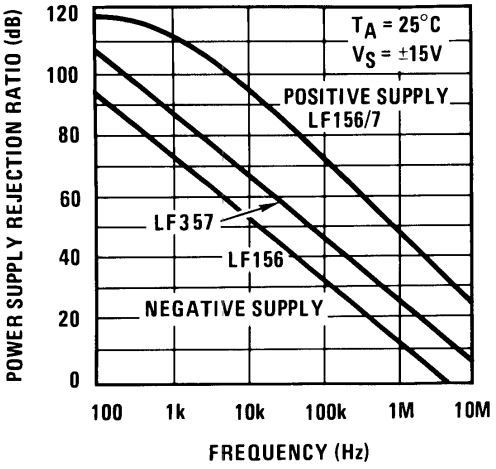


Figure 18. Power Supply Rejection Ratio

Typical AC Performance Characteristics (continued)

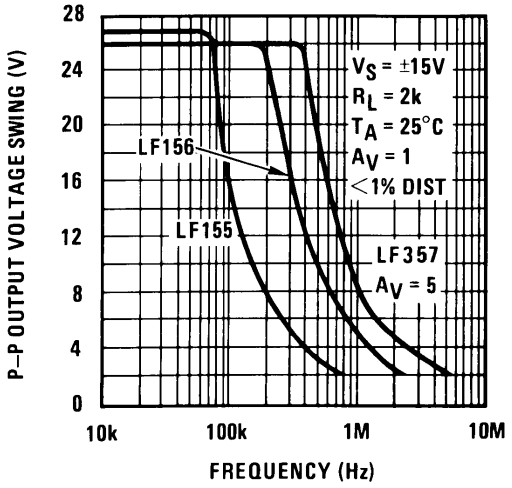


Figure 19. Undistorted Output Voltage Swing

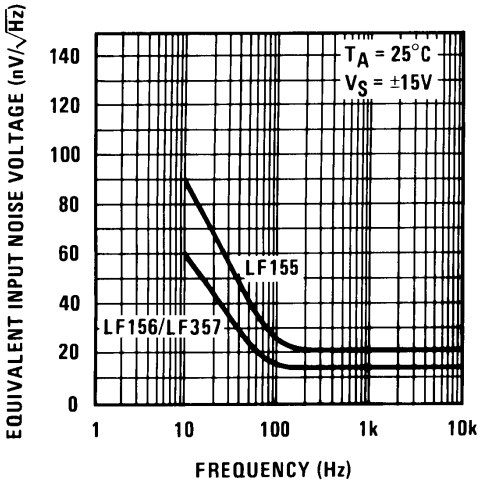


Figure 20. Equivalent Input Noise Voltage

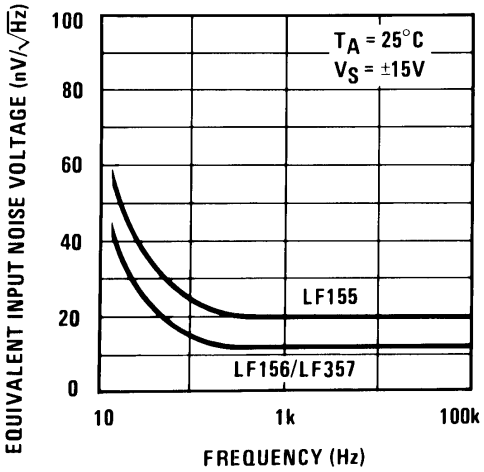


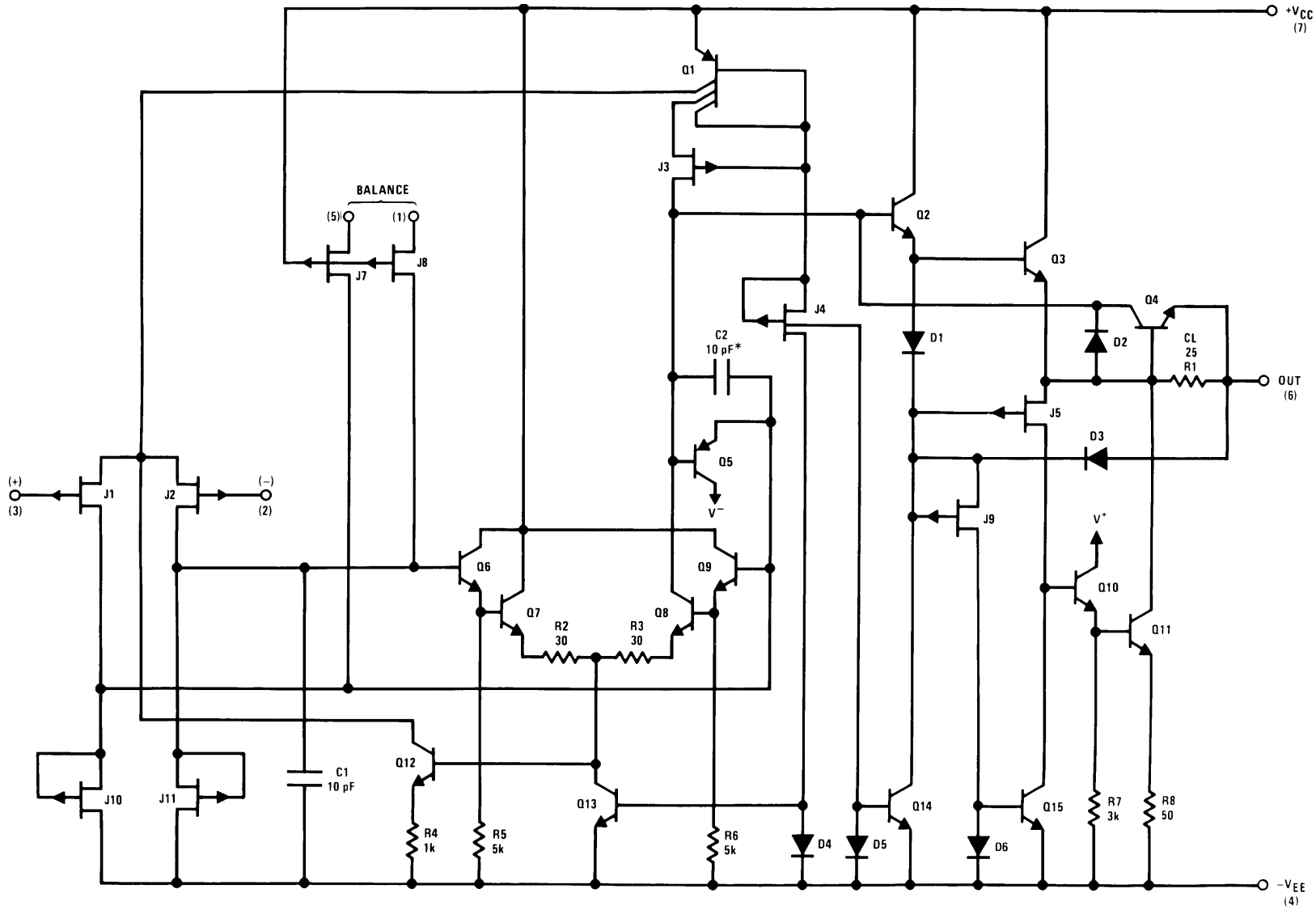
Figure 21. Equivalent Input Noise Voltage (Expanded Scale)

7 Detailed Description

7.1 Overview

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, as well as low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. These devices can replace expensive hybrid and module FET operational amplifiers. Designed for low voltage and current noise and a low 1/f noise corner, these devices are excellent for low noise applications using either high or low source impedance.

7.2 Functional Block Diagram



*C = 3 pF in LF357 series.

Figure 22. Detailed Schematic

7.3 Feature Description

7.3.1 Large Differential Input Voltage

These are operational amplifiers with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

7.3.2 Large Common-Mode Input Voltage

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

7.4 Device Functional Modes

The LF356-MIL has a single functional mode and operates according to the conditions listed in the *Recommended Operating Conditions*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize pick-up and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3-dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3-dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

8.2 Typical Application

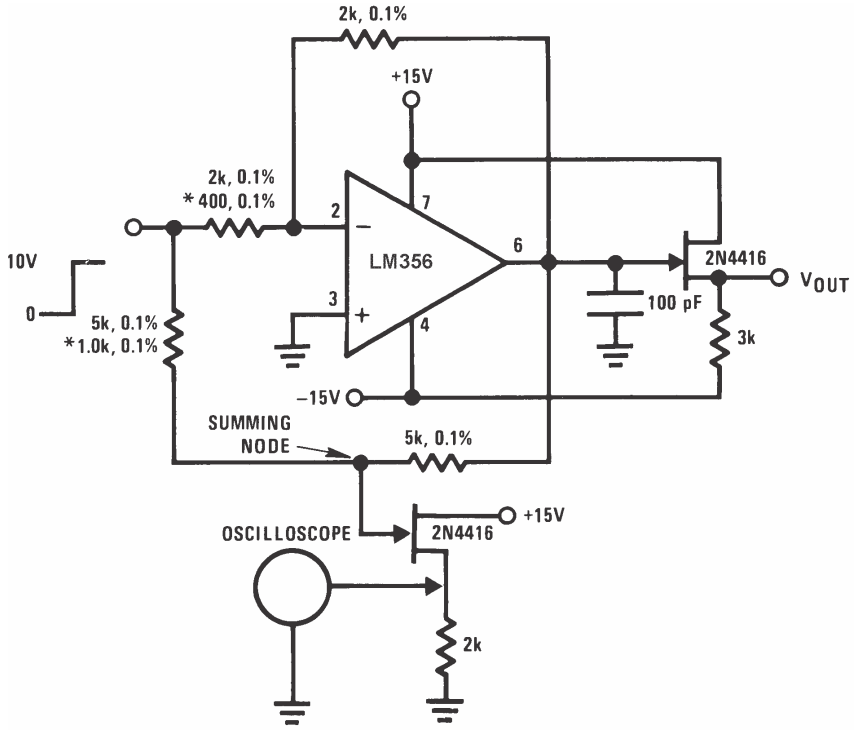


Figure 23. Settling Time Test Circuit

8.2.1 Design Requirements

Settling time is tested with the LF35x connected as unity gain inverter and LF357 connected for $A_V = -5$

8.2.2 Detailed Design Procedure

Connect the circuit components as shown in Figure 23. In particular, use FET to isolate the probe capacitance.

Apply a 10-V step function to the input.

Use an oscilloscope to probe the circuit as shown in Figure 23.

8.2.3 Application Curve

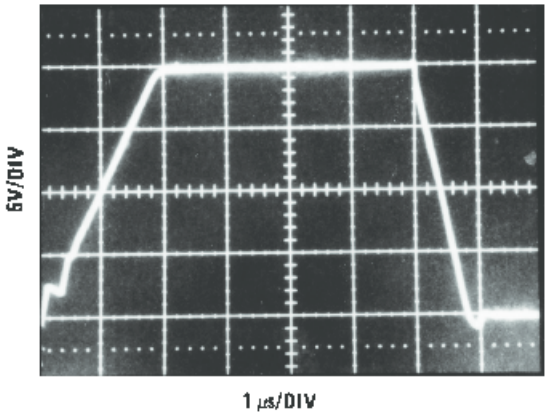


Figure 24. Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

8.3 System Examples

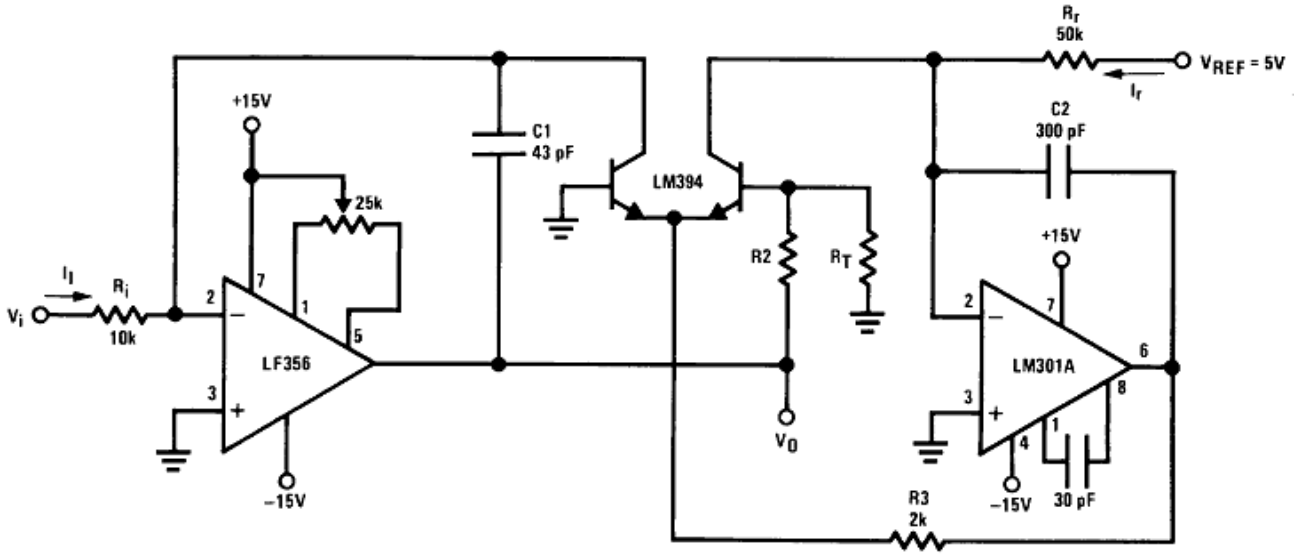


Figure 25. Fast Logarithmic Converter

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1 V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/^{\circ}C \text{ (for temperature compensation)} \tag{1}$$

System Examples (continued)

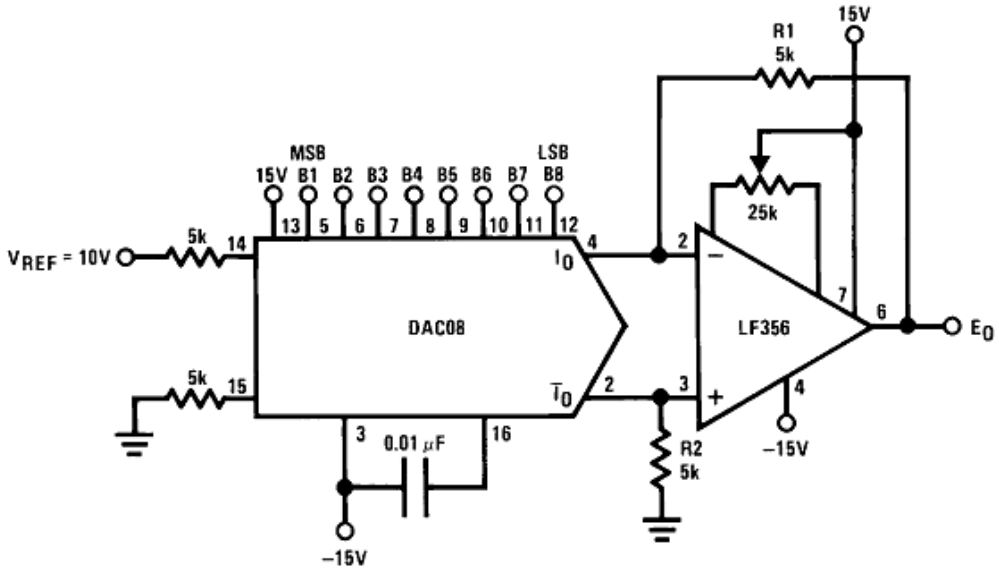


Figure 26. 8-Bit D/A Converter With Symmetrical Offset Binary Operation

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

Table 1. Bit Illustration of the 8-Bit D/A Converter

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

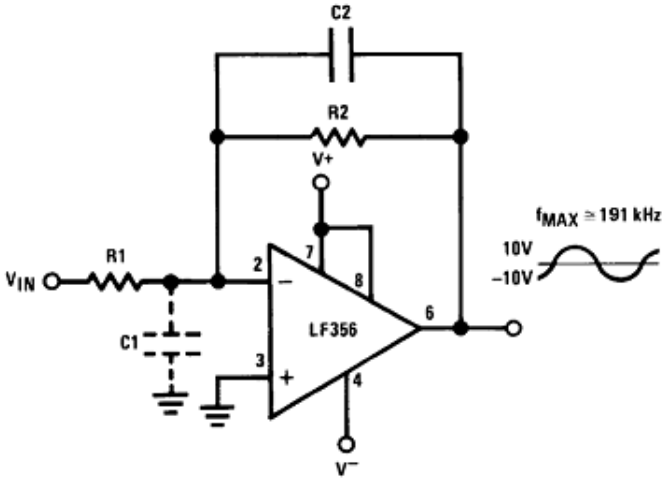


Figure 27. Wide BW Low Noise, Low Drift Amplifier

- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$ (2)

Parasitic input capacitance C1 ≃ (3 pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

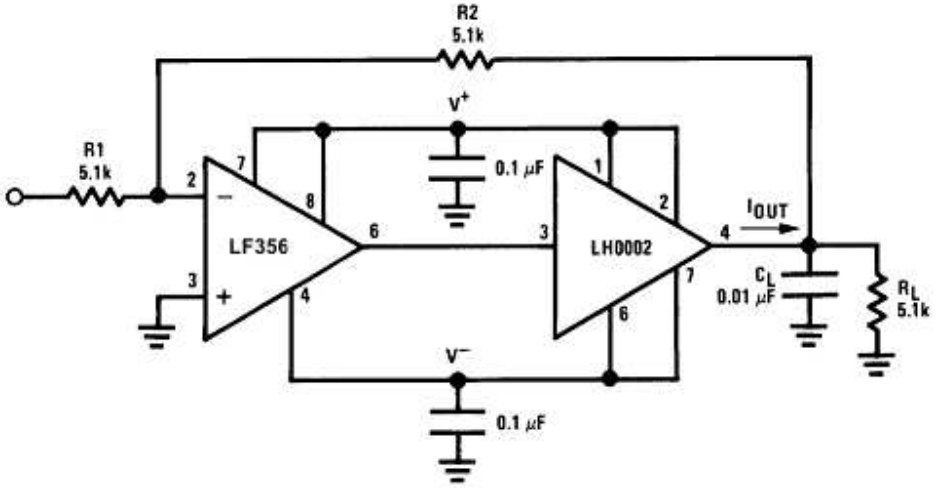


Figure 28. Boosting the LF156 With a Current Amplifier

- $I_{OUT(MAX)}$ ≃ 150 mA (will drive $R_L \geq 100\ \Omega$)
  - $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s\ (\text{with } C_L \text{ shown})$ (3)
- No additional phase shift added by the current amplifier

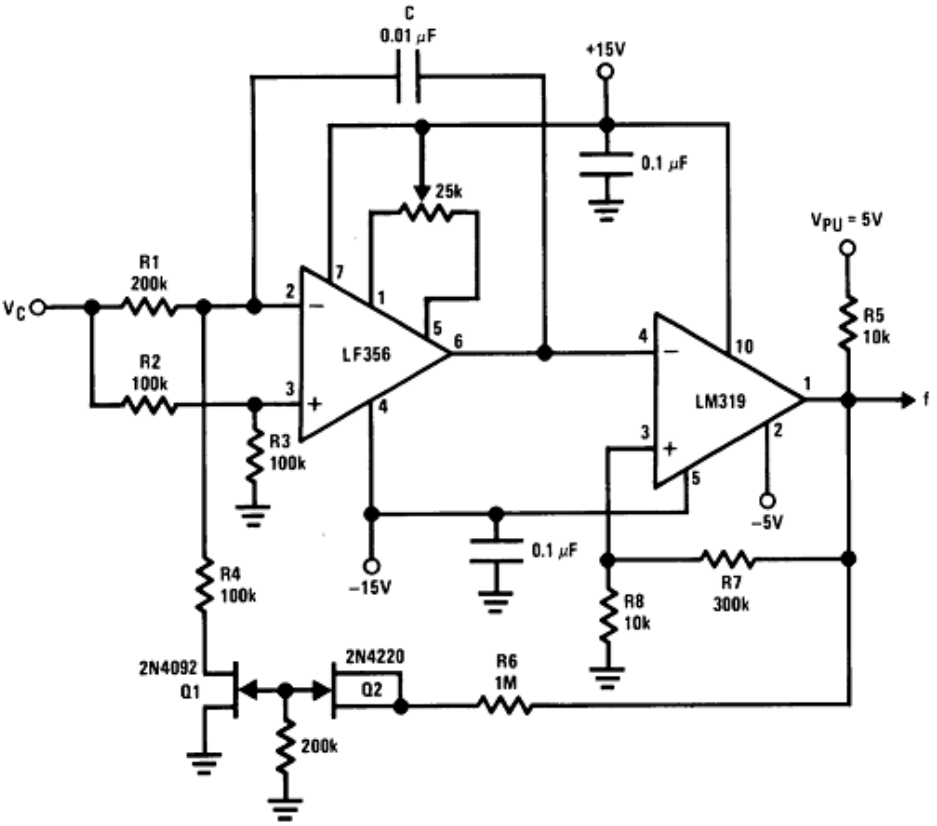


Figure 29. Decades VCO

R1, R4 matched. Linearity 0.1% over 2 decades.

$$f = \frac{V_C (R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \leq V_C \leq 30V,\ 10\,Hz \leq f \leq 10\,kHz \tag{4}$$

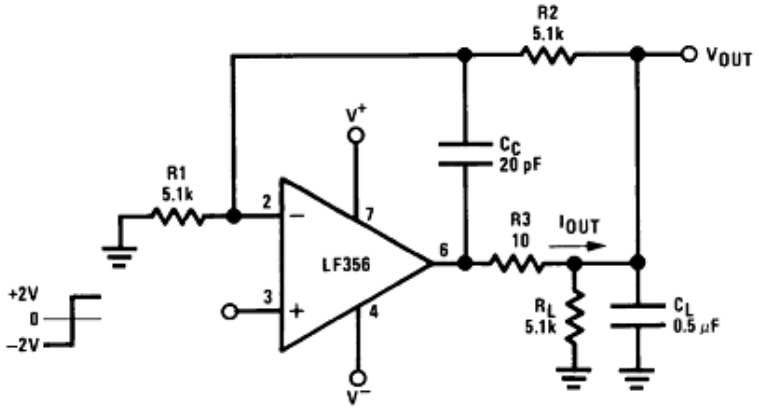


Figure 30. Isolating Large Capacitive Loads

- Overshoot 6%
- t_s 10 μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\,V/\mu s = 0.04\,V/\mu s \text{ (with } C_L \text{ shown)} \tag{5}$$

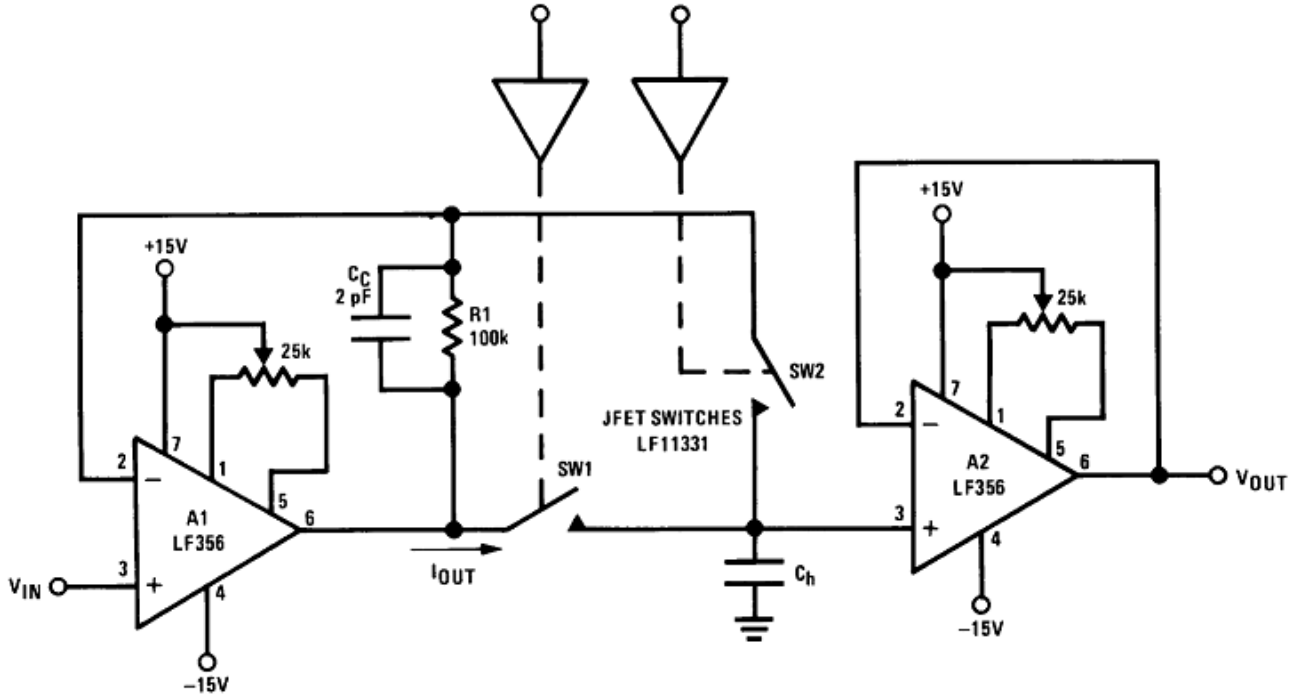


Figure 31. Fast Sample and Hold

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON},\ V_{IN},\ C_h}{S_r}\right] \text{ 1/2 provided that:}$$

$$V_{IN} < 2\pi S_r\, R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA} \tag{6}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1$ V
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

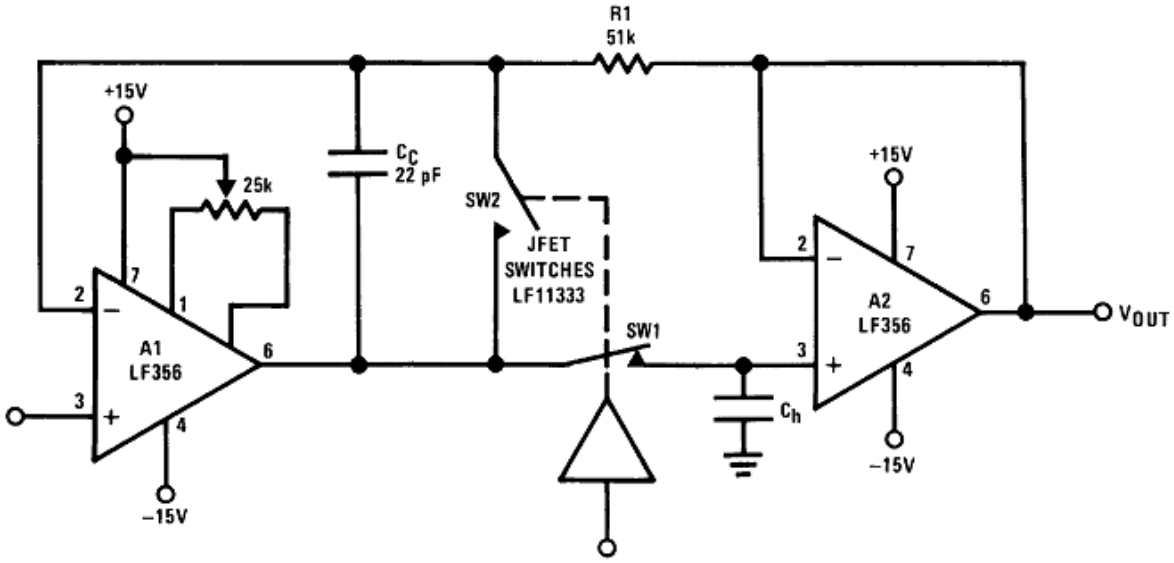


Figure 32. High Accuracy Sample and Hold

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
  - No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added
  - propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

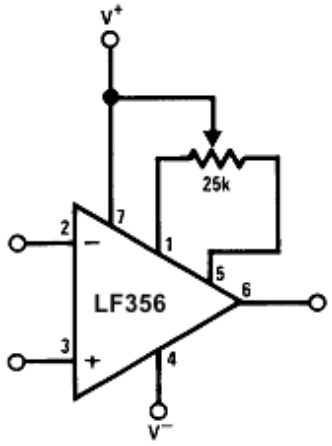


Figure 33. V_{OS} Adjustment

- V_{OS} is adjusted with a 25-k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

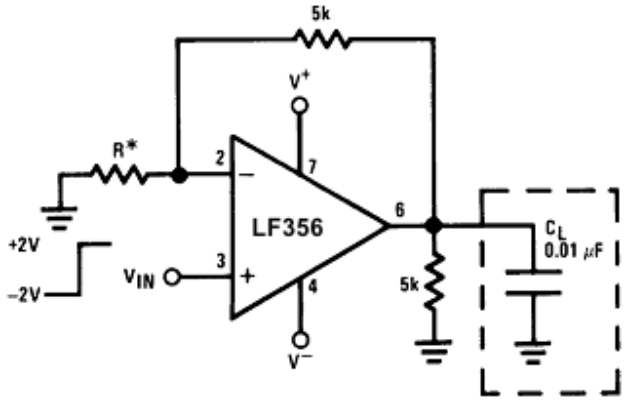


Figure 34. Driving Capacitive Loads

- *LF15x R = 5k, LF357 R = 1.25 k
- Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\ \mu F$.
- Overshoot ≤ 20%, Settling time (t_s) ≈ 5 µs

9 Power Supply Recommendations

See the *Recommended Operating Conditions* for the minimum and maximum values for the supply input voltage and operating junction temperature.

10 Layout

10.1 Layout Guidelines

10.1.1 Printed-Circuit-Board Layout For High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PCB. When one wishes to take advantage of the low input bias current of the LF356-MIL, typically less than 30 pA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PCB, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the inputs of the LF356-MIL and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth, connected to the inputs of the op amp, as in Figure 39. To have a significant effect, guard rings must be placed on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10 TΩ, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. If a guard ring is used and held close to the potential of the amplifier inputs, it will significantly reduce this leakage current.

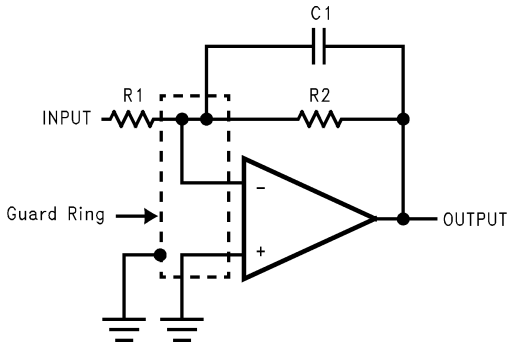


Figure 35. Inverting Amplifier

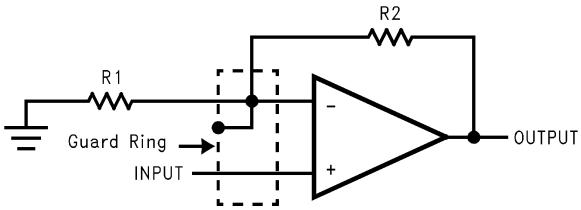


Figure 36. Noninverting Amplifier

Layout Guidelines (continued)

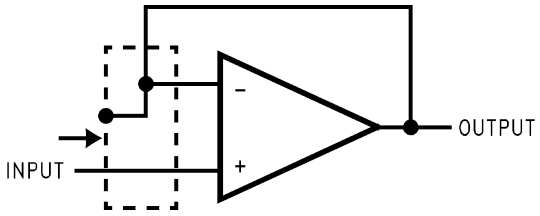
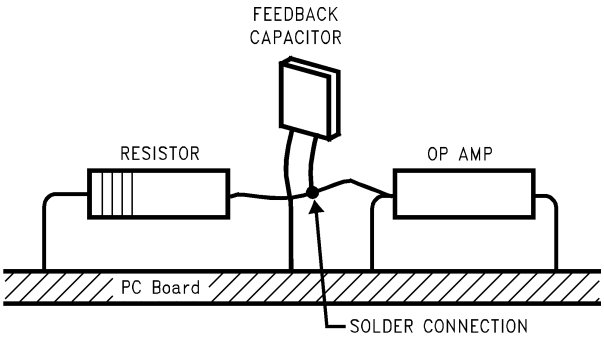


Figure 37. Typical Connections Of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 38.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB).

Figure 38. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LF356-MIL is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

10.2 Layout Example

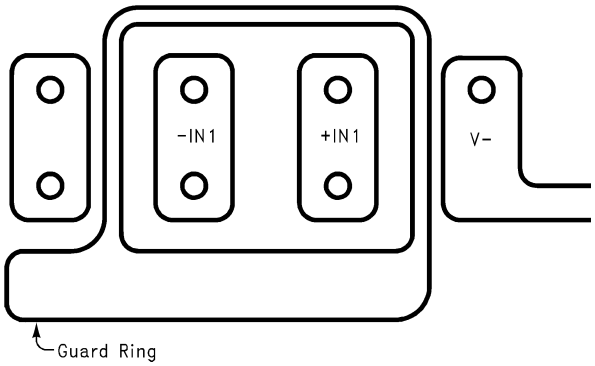


Figure 39. Examples Of Guard Ring In PCB Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*****エンジニア間の共同作業を促進するために開設されたものです。**e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.3 商標

BI-FET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LF356 MWC	Active	Production	WAFERSALE (YS) | 0	1 | NOT REQUIRED	-	Call TI	Level-1-NA-UNLIM	-40 to 85	
LF356H	Active	Production	TO-99 (LMC) | 8	500 | OTHER	No	Call TI	Level-1-NA-UNLIM	0 to 70	(LF356H, LF356H)
LF356H/NOPB	Active	Production	TO-99 (LMC) | 8	500 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	0 to 70	(LF356H, LF356H)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

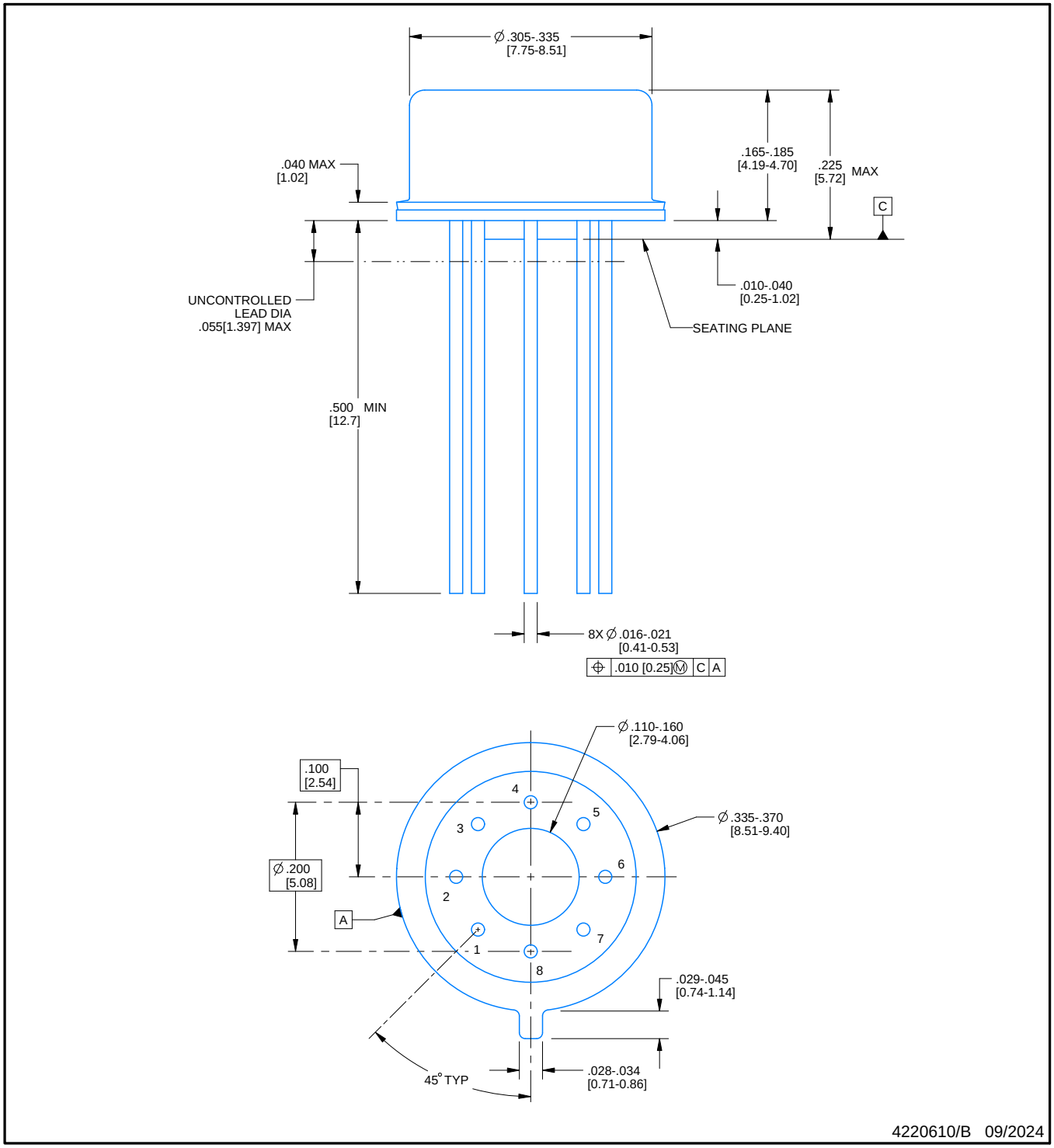
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

LMC0008A

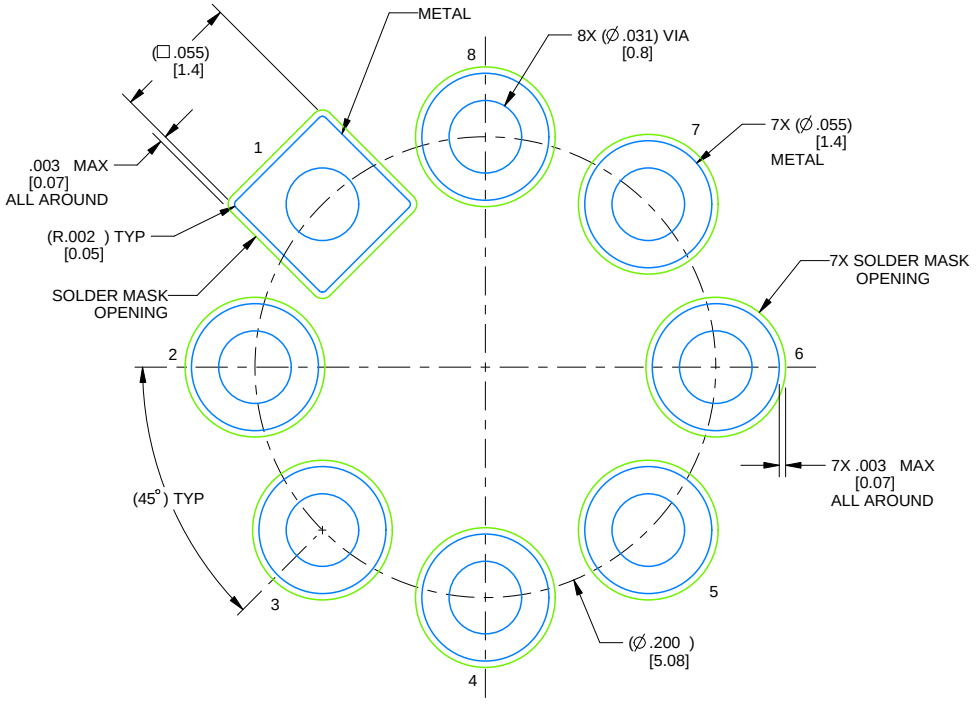
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月