LM101AJAN Operational Amplifiers

Check for Samples: LM101AJAN

FEATURES

- **Offset Voltage 3 mV Maximum Over Temperature**
- **Input Current 100 nA Maximum Over Temperature**
- **Offset Current 20 nA Maximum Over Temperature**
- **Ensured Drift Characteristics**
- **Offsets Ensured Over Entire Common Mode and Supply Voltage Ranges**
- **Slew Rate of 10 V/μS as a Summing Amplifier**

DESCRIPTION

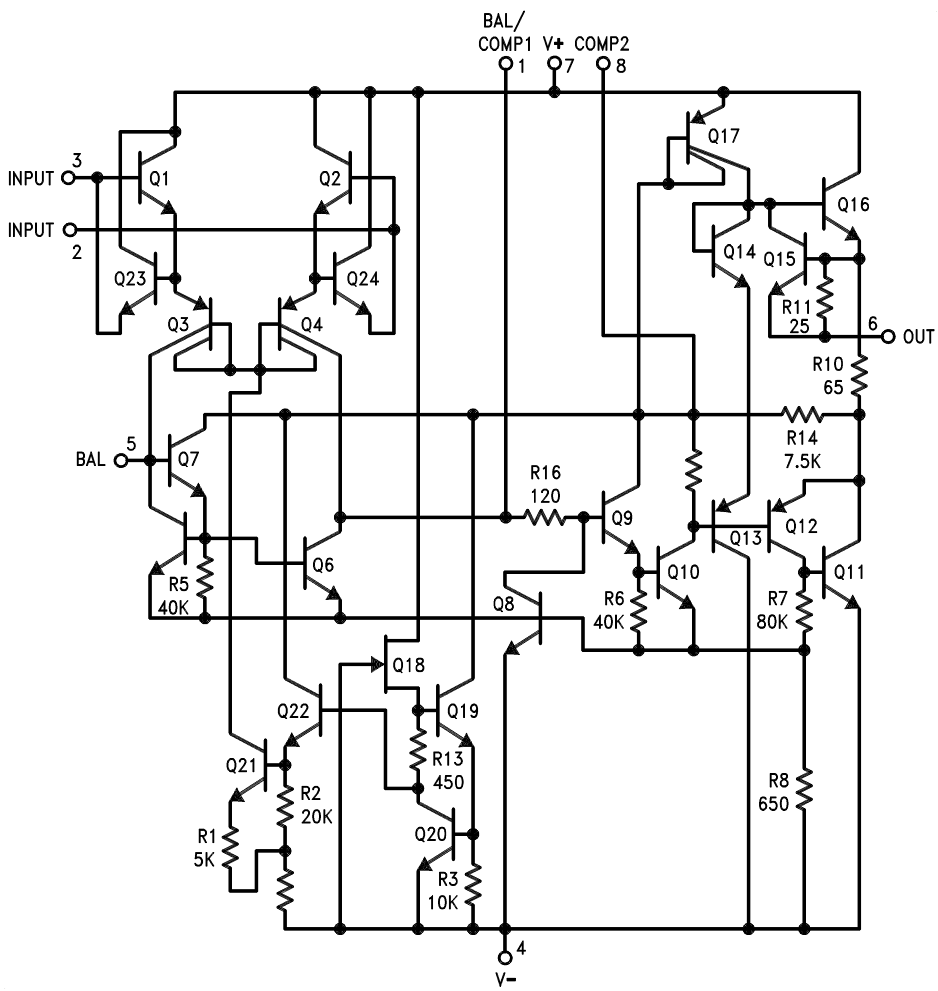
The LM101A is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Ensured drift characteristics
- Offsets ensured over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

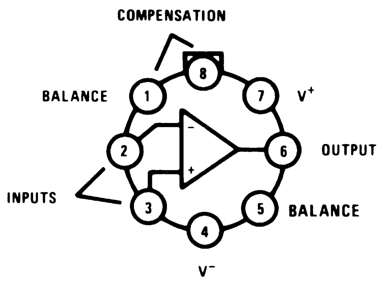
In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

Schematic



Pin connections shown are for 8-pin packages

Connection Diagrams



Pin 4 connected to case.

Figure 1. (Top View)
TO-99 Package
See Package Number LMC

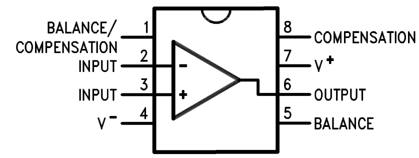


Figure 2. (Top View)
CDIP Package
See Package Number NAB0008A

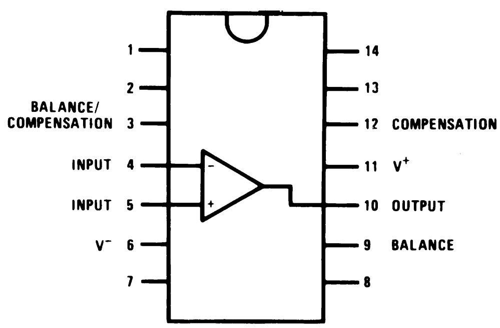


Figure 3. (Top View)
CDIP Package
See NS Package Number J

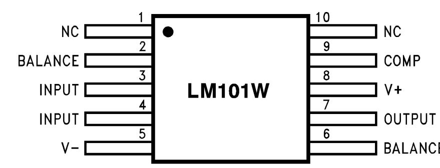
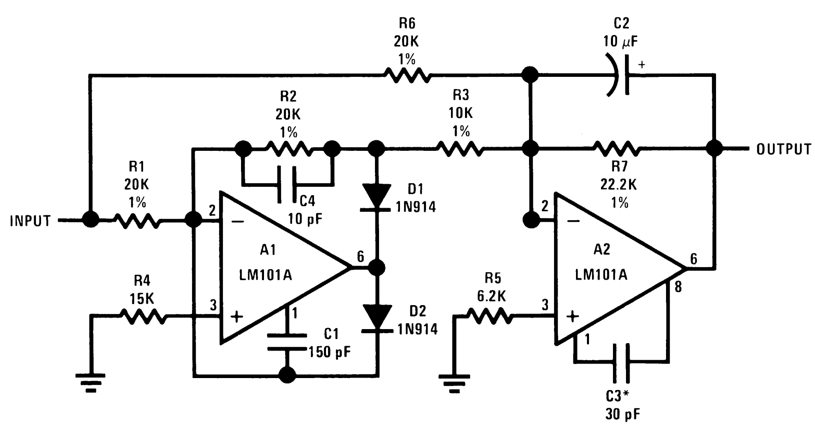


Figure 4. (Top View)
CLGA Package
See NS Package Number NAD0010A

Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage				±22V
Differential Input Voltage				±30V
Input Voltage(2)				±15V
Output Short Circuit Duration				Continuous
Operating Ambient Temp. Range				−55°C ≤ T_A ≤ +125°C
T_J Max				150°C
Power Dissipation at T_A = 25°C(3)	LMC-Package		Still Air)	750 mW
			(500 LF / Min Air Flow)	1,200 mW
	NAB0008A-Package		(Still Air)	1,000 mW
			(500 LF / Min Air Flow)	1,500 mW
	J-Package		(Still Air)	1,200mW
			(500 LF / Min Air Flow)	2,000mW
	NAD0010A-Package		(Still Air)	500mW
			(500 LF / Min Air Flow)	800mW
Thermal Resistance	$θ_{JA}$	LMC-Package	(Still Air)	165°C/W
			(500 LF / Min Air Flow)	89°C/W
		NAB0008A-Package	(Still Air)	128°C/W
			(500 LF / Min Air Flow)	75°C/W
		J-Package	(Still Air)	98°C/W
			(500 LF / Min Air Flow)	59°C/W
		NAD0010A-Package	(Still Air)	233°C/W
			(500 LF / Min Air Flow)	155°C/W
	$θ_{JC}$ (Typical)	LMC-Package		39°C/W
		NAB0008A-Package		26°C/W
		J-Package		24°C/W
		NAD0010A-Package		26°C/W
Storage Temperature Range				−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering, 10 sec.)				300°C
ESD Tolerance(4)				3000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do no ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), $θ_{JA}$ (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} − T_A) / θ_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(4) Human body model, 100 pF discharged through 1.5 kΩ.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LM101JAN Electrical Characteristics DC Parameters

The following conditions apply to all parameters, unless otherwise specified
V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V		-50	+50	μV/V	1
				-100	+100	μV/V	2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V		-50	+50	μV/V	1
				-100	+100	μV/V	2, 3

LM101JAN Electrical Characteristics DC Parameters (continued)

The following conditions apply to all parameters, unless otherwise specified
V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
CMRR	Common Mode Rejection Ratio	V_{CC} = ±35V to ±5V, V_{CM} = ±15V		80		dB	1, 2, 3
$+V_{IO}$ Adj	Adjustment for Input Offset Voltage			4.0		mV	1, 2, 3
$-V_{IO}$ Adj	Adjustment for Input Offset Voltage				-4.0	mV	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = -15V		-60		mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = +15V			+60	mA	1, 2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			3.0	mA	1
					2.32	mA	2
					3.5	mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient of Input Offset Voltage	-55°C ≤ T_A ≤ +25°C	See [1]	-18	+18	µV/°C	2
		+25°C ≤ T_A ≤ +125°C	See [1]	-15	+15	µV/°C	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient of Input Offset Current	-55°C ≤ T_A ≤ +25°C	See [2]	-200	+200	pA/°C	2
		+25°C ≤ T_A ≤ +125°C	See [2]	-100	+100	pA/°C	3
$-A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = -15V	See [3]	50		V/mV	4
			See [3]	25		V/mV	5, 6
		R_L = 10KΩ, V_O = -15V	See [3]	50		V/mV	4
			See [3]	25		V/mV	5, 6
$+A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = +15V	See [3]	50		V/mV	4
			See [3]	25		V/mV	5, 6
		R_L = 10KΩ, V_O = +15V	See [3]	50		V/mV	4
			See [3]	25		V/mV	5, 6
A_{VS}	Large Signal (Open Loop) Voltage Gain	V_{CC} = ±5V, R_L = 2KΩ, V_O = ±2V	See [3]	10		V/mV	4, 5, 6
		V_{CC} = ±5V, R_L = 10KΩ, V_O = ±2V	See [3]	10		V/mV	4, 5, 6
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = -20V		+16		V	4, 5, 6
		R_L = 2KΩ, V_{CM} = -20V		+15		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = 20V			-16	V	4, 5, 6
		R_L = 2KΩ, V_{CM} = 20V			-15	V	4, 5, 6

(1) Calculated parameter
(2) Calculated parameter
(3) Datalog reading of K = V/mV.

LM101AJAN Electrical Characteristics AC Parameters

The following conditions apply to all parameters, unless otherwise specified
V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		0.3		V/µS	7
-SR	Slew Rate	A_V = 1, V_I = +5V to -5V		0.3		V/µS	7
TR_{TR}	Rise Time	A_V = 1, V_I = 50mV			800	nS	7
TR_{OS}	Overshoot	A_V = 1, V_I = 50mV			25	%	7
NI_{BB}	Noise Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			15	μV_{RMS}	7
NI_{PC}	Noise Popcorn	BW = 10Hz to 5KHz, R_S = 100KΩ			80	μV_{PK}	7

LM101AJAN Electrical Characteristics DC Parameters: Drift Values

The following conditions apply to all parameters, unless otherwise specified
V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω
Delta calculations performed on JAN S devices at group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V		-0.5	0.5	mV	1
± I_{IB}	Input Bias Current	V_{CM} = 0V, R_S = 100KΩ		-7.5	7.5	nA	1

Typical Performance Characteristics LM101A

Input Voltage Range

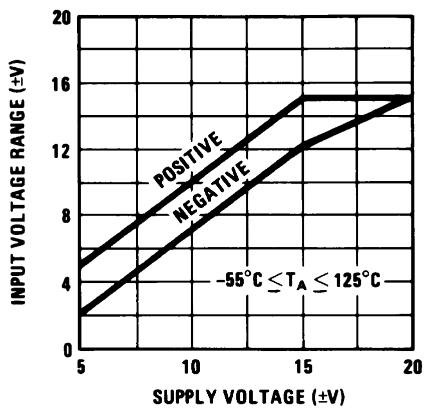


Figure 5.

Output Swing

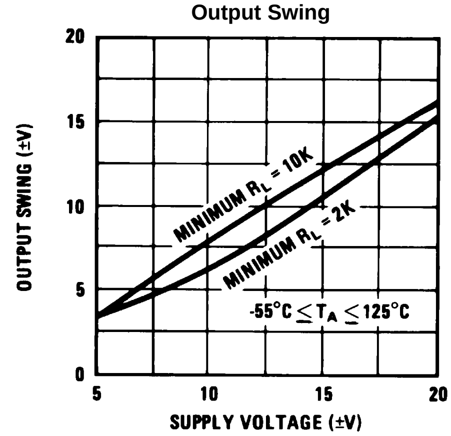


Figure 6.

Voltage Gain

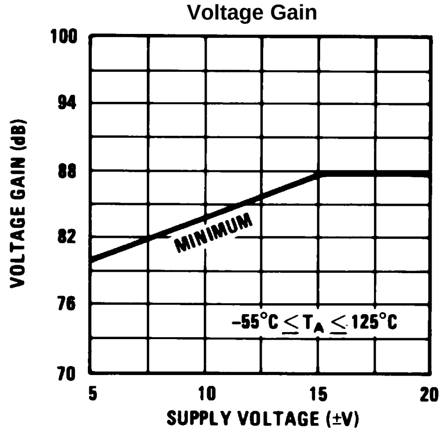


Figure 7.

Supply Current

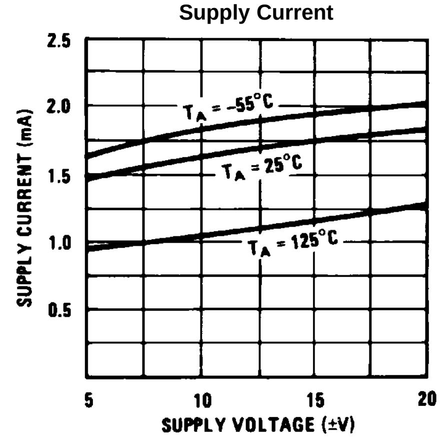


Figure 8.

Voltage Gain

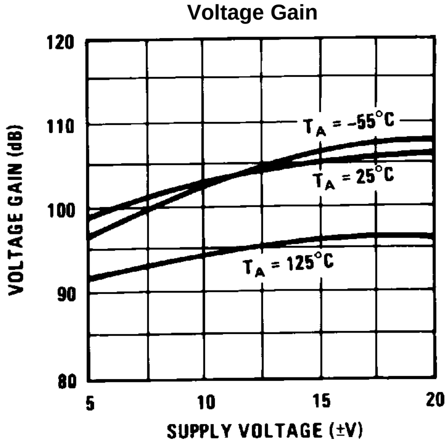


Figure 9.

Maximum Power Dissipation

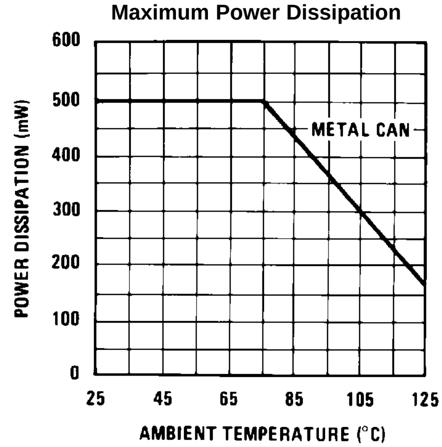


Figure 10.

Typical Performance Characteristics LM101A (continued)

Input Current, LM101A

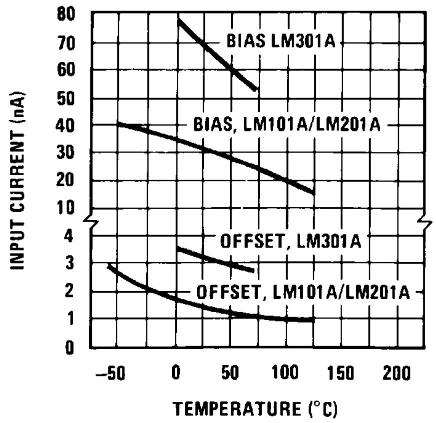


Figure 11.

Input Noise Voltage

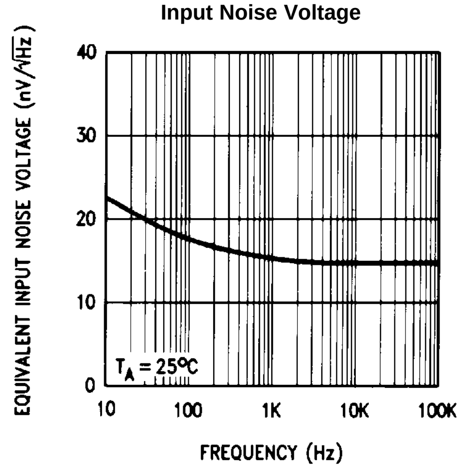


Figure 12.

Input Noise Current

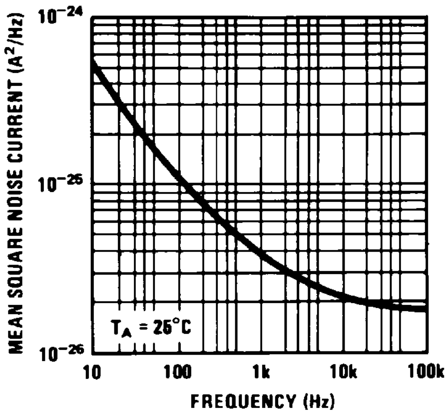


Figure 13.

Common Mode Rejection

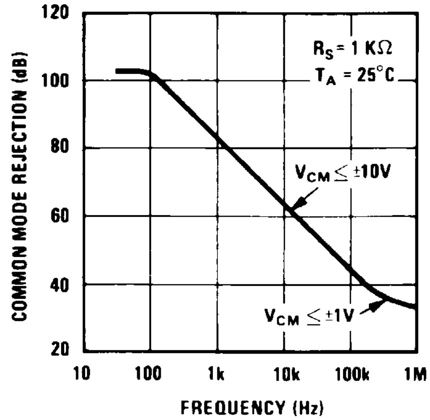


Figure 14.

Power Supply Rejection

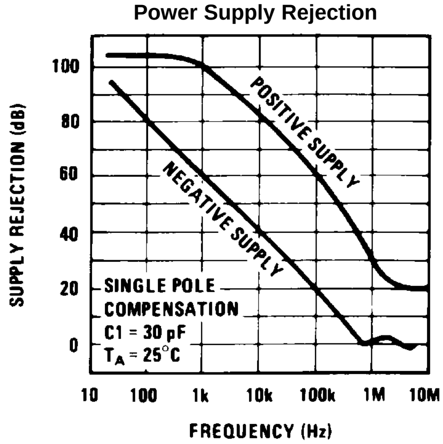


Figure 15.

Closed Loop Output Impedance

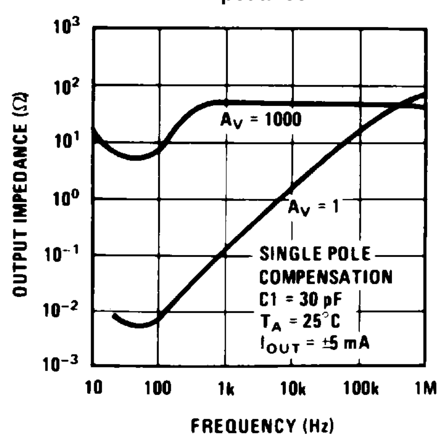
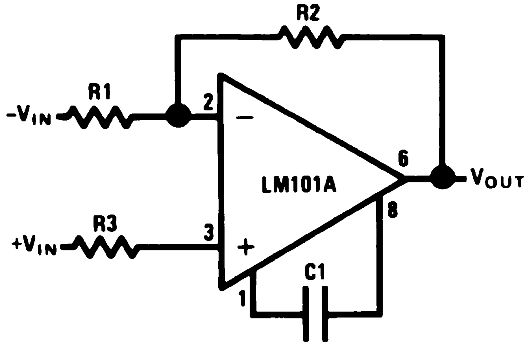


Figure 16.

Typical Performance Characteristics for Various Compensation Circuits(1)

Single Pole Compensation

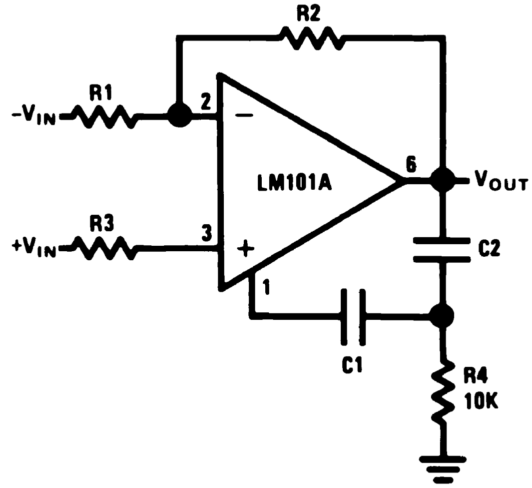


$C1 \geq \frac{R1\ C_S}{R1 + R2}$

C_S= 30 pF

Figure 17.

Two Pole Compensation



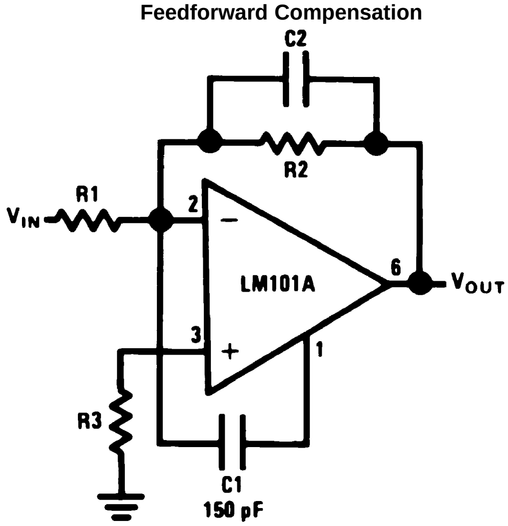
$C1 \geq \frac{R1\ C_S}{R1 + R2}$

C_S= 30 pF

C2 = 10 C1

Figure 18.

Feedforward Compensation



$C2 = \frac{1}{2\pi\ f_o\ R2}$

f_o= 3 MHz

Figure 19.

Open Loop Frequency Response

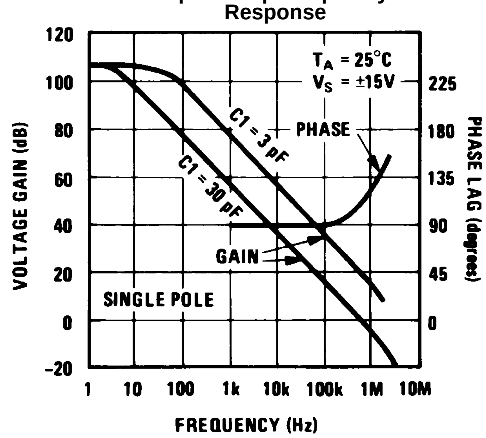


Figure 20.

(1) Pin connections shown are for 8-pin packages.

Typical Performance Characteristics for Various Compensation Circuits(1) (continued)

Open Loop Frequency Response

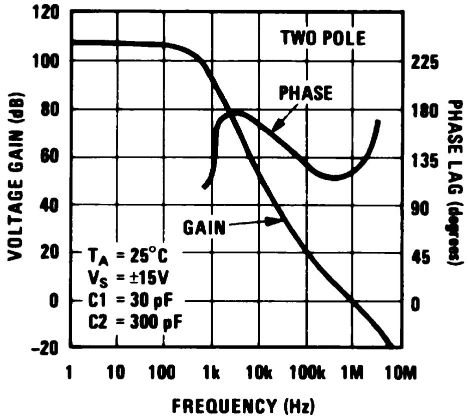


Figure 21.

Open Loop Frequency Response

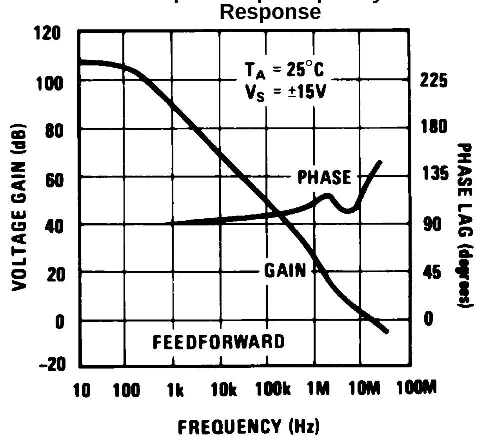


Figure 22.

Large Signal Frequency Response

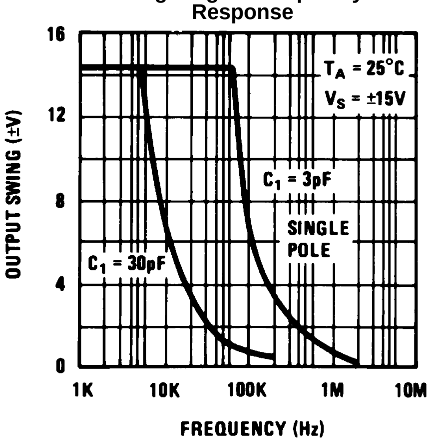


Figure 23.

Large Signal Frequency Response

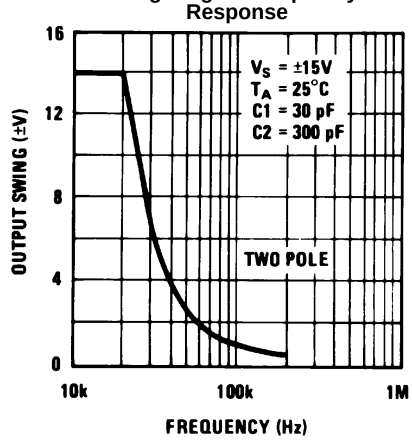


Figure 24.

Large Signal Frequency Response

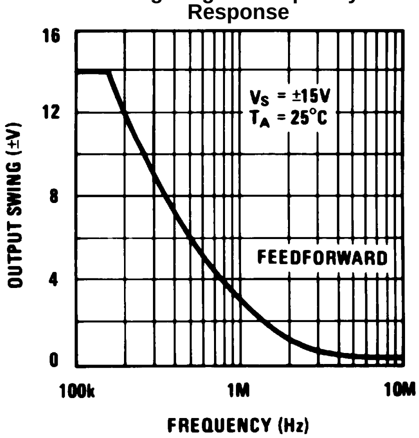


Figure 25.

Voltage Follower Pulse Response

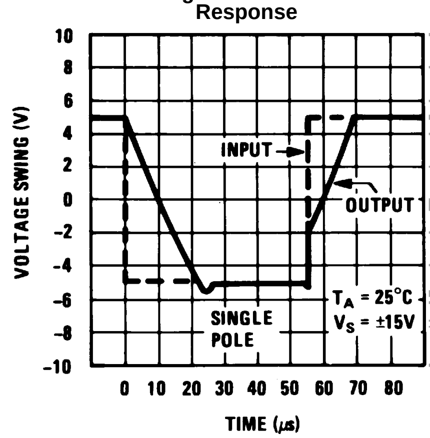


Figure 26.

Typical Performance Characteristics for Various Compensation Circuits[1] (continued)

Voltage Follower Pulse Response

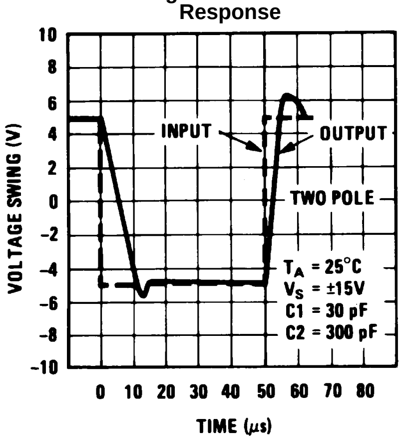


Figure 27.

Inverter Pulse Response

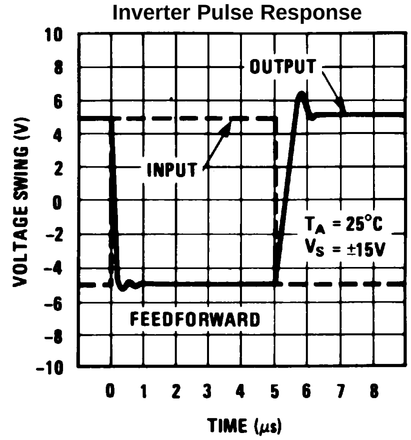
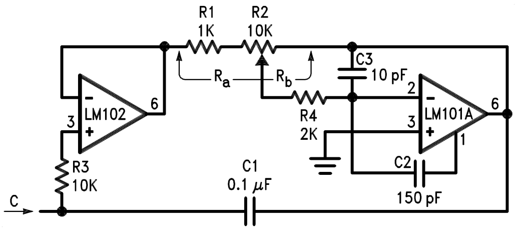


Figure 28.

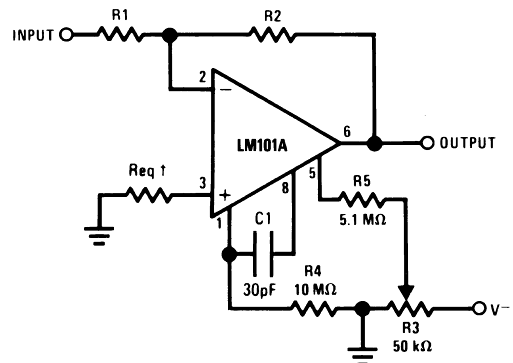
TYPICAL APPLICATIONS(2)

Variable Capacitance Multiplier



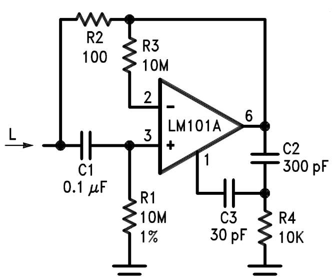
$C = 1 + \frac{R_b}{R_a} C1$

Inverting Amplifier with Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Simulated Inductor

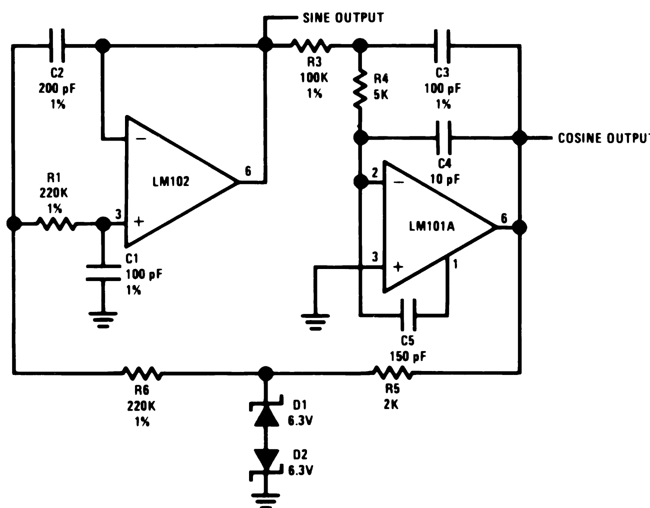


L ≃ R1 R2 C1

R_S = R2

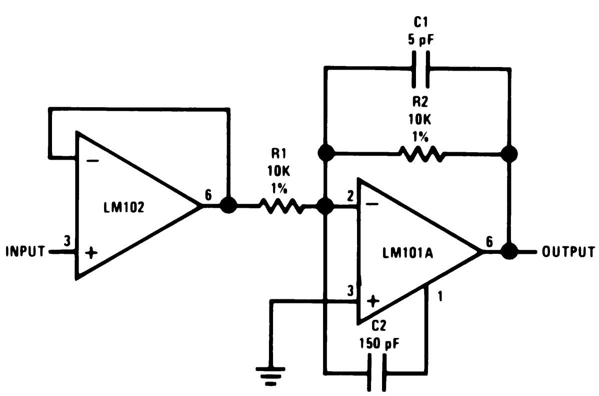
R_P = R1

Sine Wave Oscillator

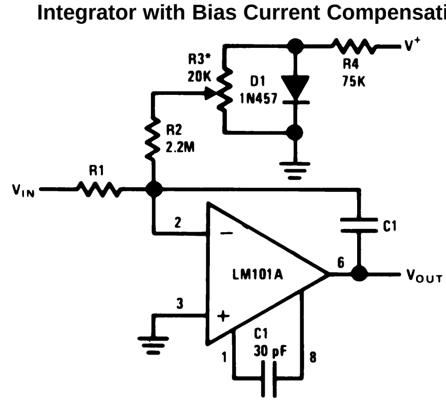


f_o = 10 kHz

Fast Inverting Amplifier with High Input Impedance



Integrator with Bias Current Compensation

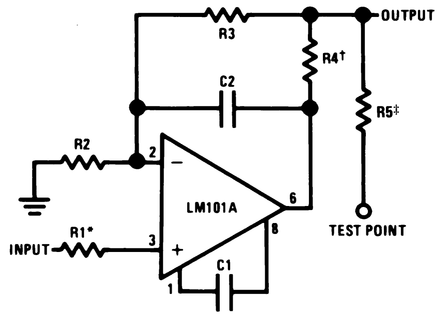


*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

(2) Pin connections shown are for 8-pin packages.

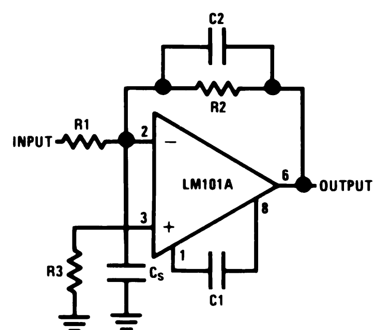
Application Hints[2]

Protecting Against Gross Fault Conditions



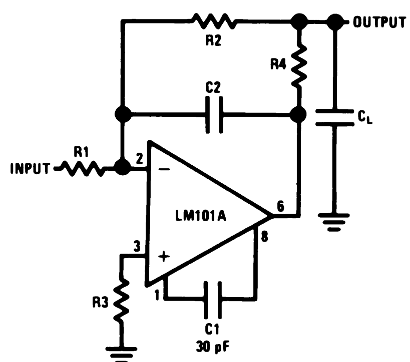
*Protects input
†Protects output
‡Protects output—not needed when R4 is used.

Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\ C_S}{R2}$$

Isolating Large Capacitive Loads



Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

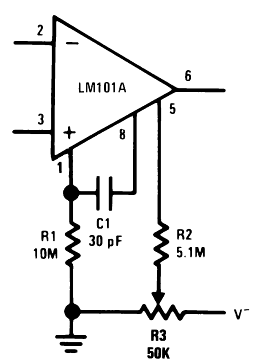
Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

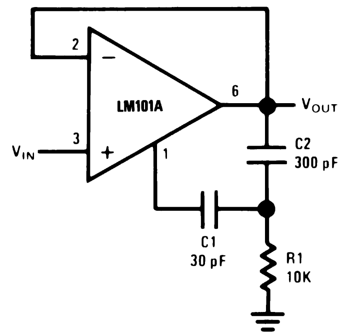
Typical Applications(3)

Standard Compensation and Offset Balancing Circuit



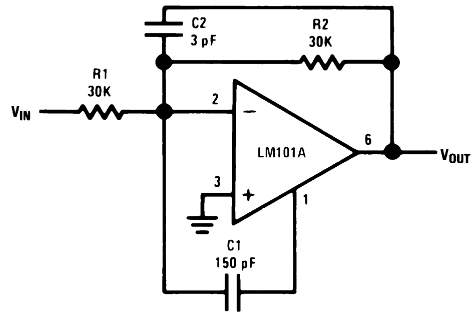
(3) Pin connections shown are for 8-pin packages.

Fast Voltage Follower



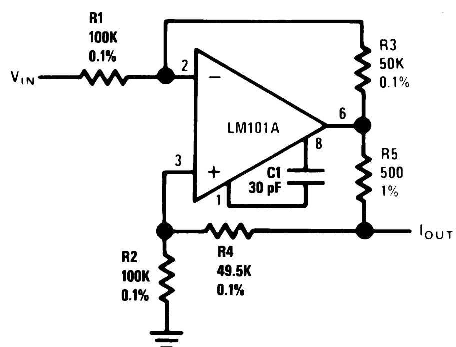
Power Bandwidth: 15 kHz
Slew Rate: 1V/µs

Fast Summing Amplifier



Power Bandwidth: 250 kHz
Small Signal Bandwiidth: 3.5 MHz
Slew Rate: 10V/µs

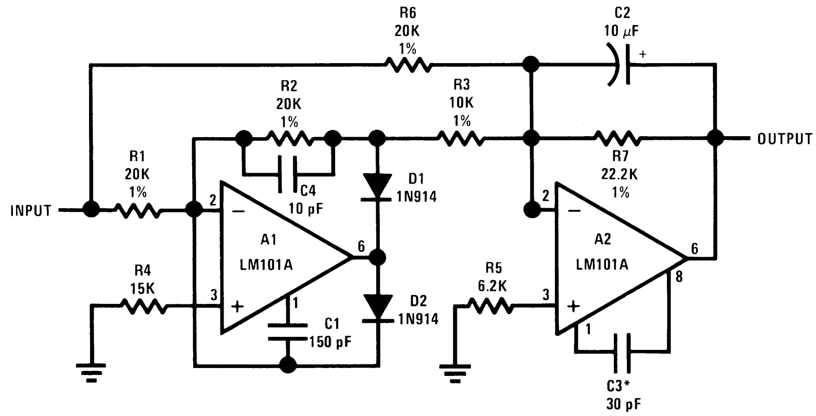
Bilateral Current Source



$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

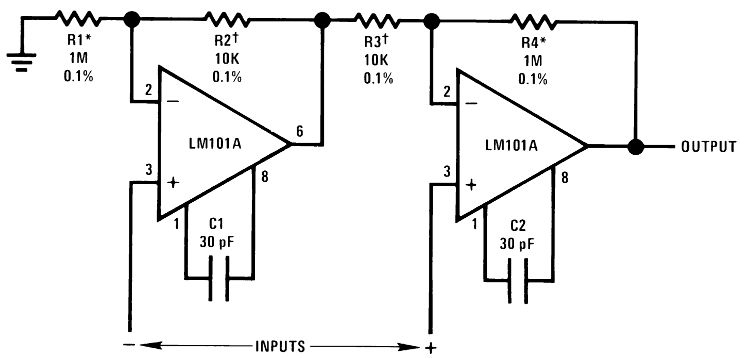
R3 = R4 + R5
R1 = R2

Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Instrumentation Amplifier

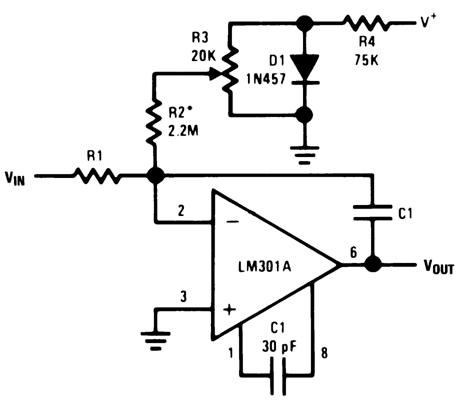


R1 = R4; R2 = R3

$A_V = 1 + \frac{R1}{R2}$

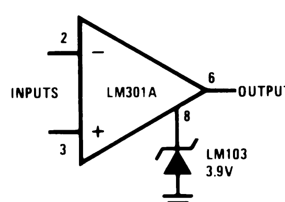
*,† Matching determines CMRR.

Integrator with Bias Current Compensation

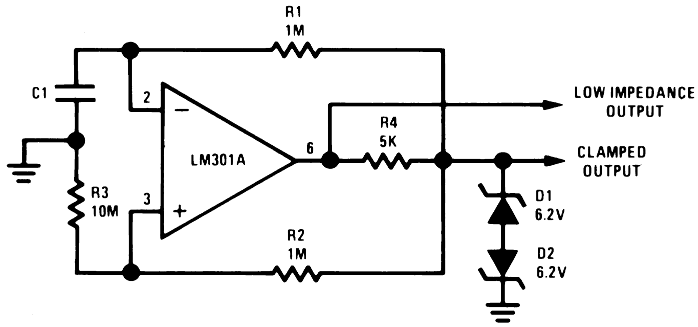


*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to +70°C temperature range.

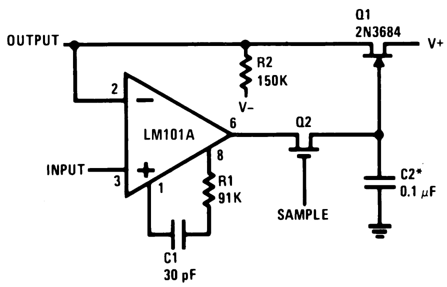
Voltage Comparator for Driving RTL Logic or High Current Driver



Low Frequency Square Wave Generator

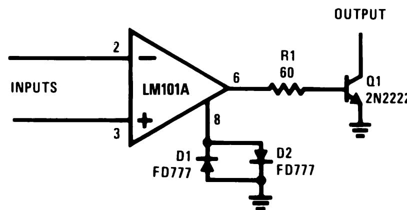


Low Drift Sample and Hold



*Polycarbonate-dielectric capacitor

Voltage Comparator for Driving DTL or TTL Integrated Circuits



REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
01/05/06	A	New Release to corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. MJLM101A-X Rev 1A0 datasheet will be archived.
03/20/13	A	All	-	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JL101ABCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q
JL101ABGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T
JL101ABPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T
JM38510/10103BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q
JM38510/10103BGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T
JM38510/10103BPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T
M38510/10103BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABCA JM38510/10103BCA Q
M38510/10103BGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	JL101ABGA JM38510/10103BGA Q ACO JM38510/10103BGA Q >T
M38510/10103BPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	JL101ABPA Q JM38510/ 10103BPA ACO 10103BPA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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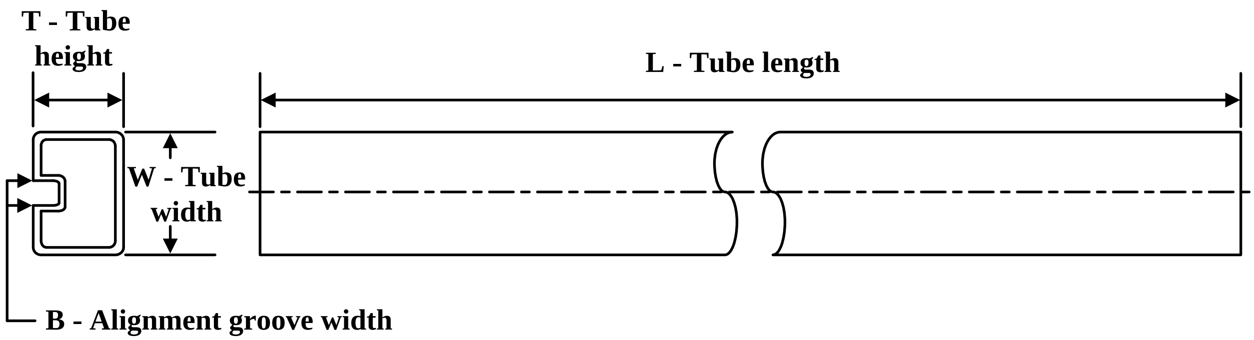
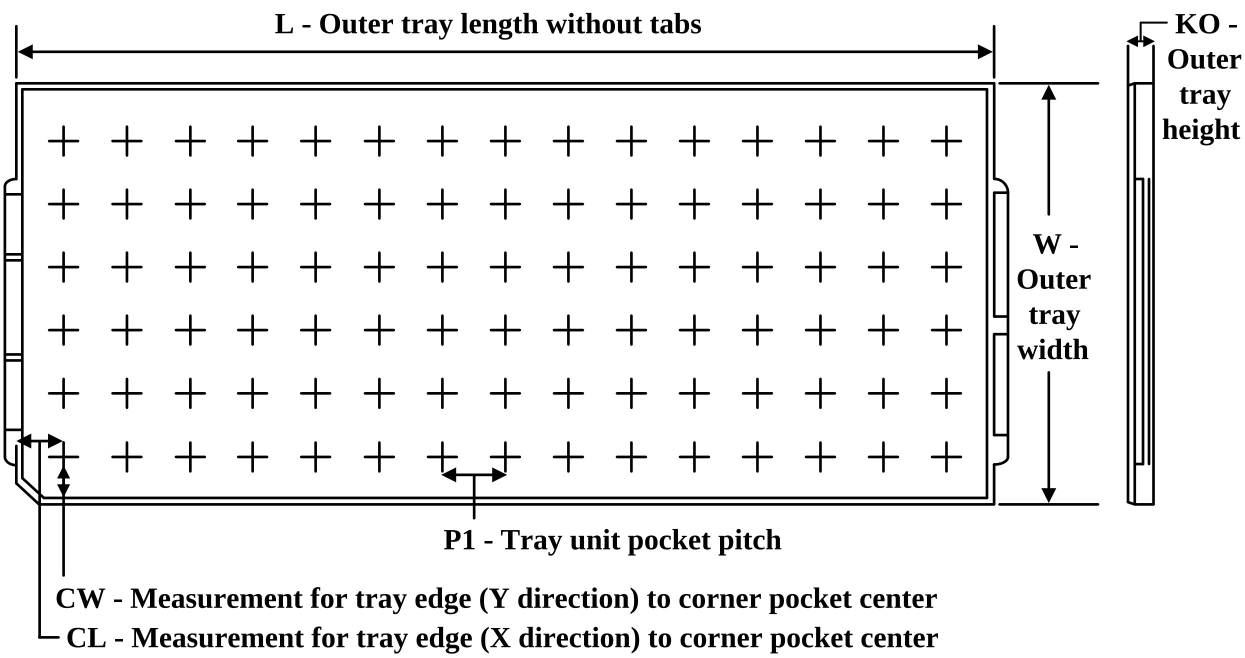
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
JL101ABCA	J	CDIP	14	25	506.98	15.24	13440	NA
JL101ABPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
JM38510/10103BCA	J	CDIP	14	25	506.98	15.24	13440	NA
JM38510/10103BPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
M38510/10103BCA	J	CDIP	14	25	506.98	15.24	13440	NA
M38510/10103BPA	NAB	CDIP	8	40	506.98	15.24	13440	NA

TRAY

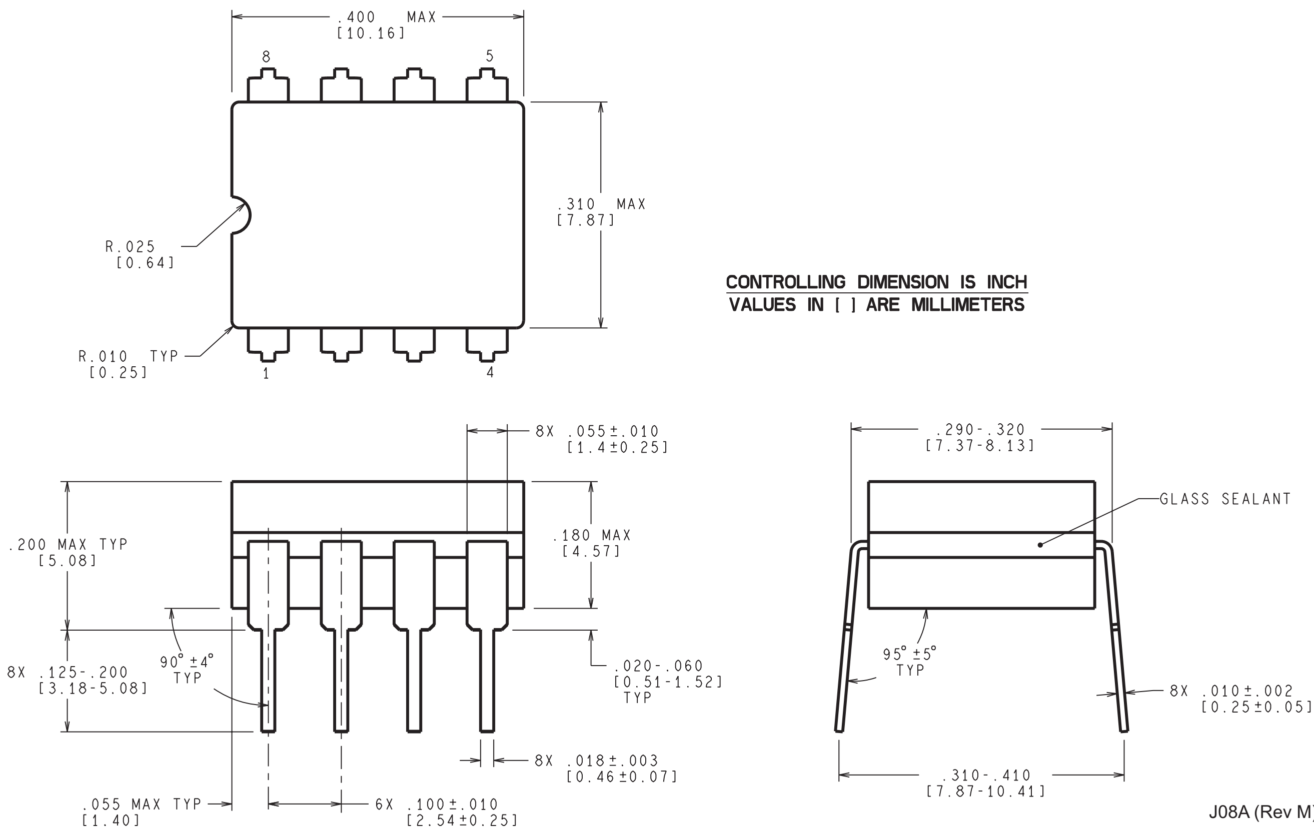


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

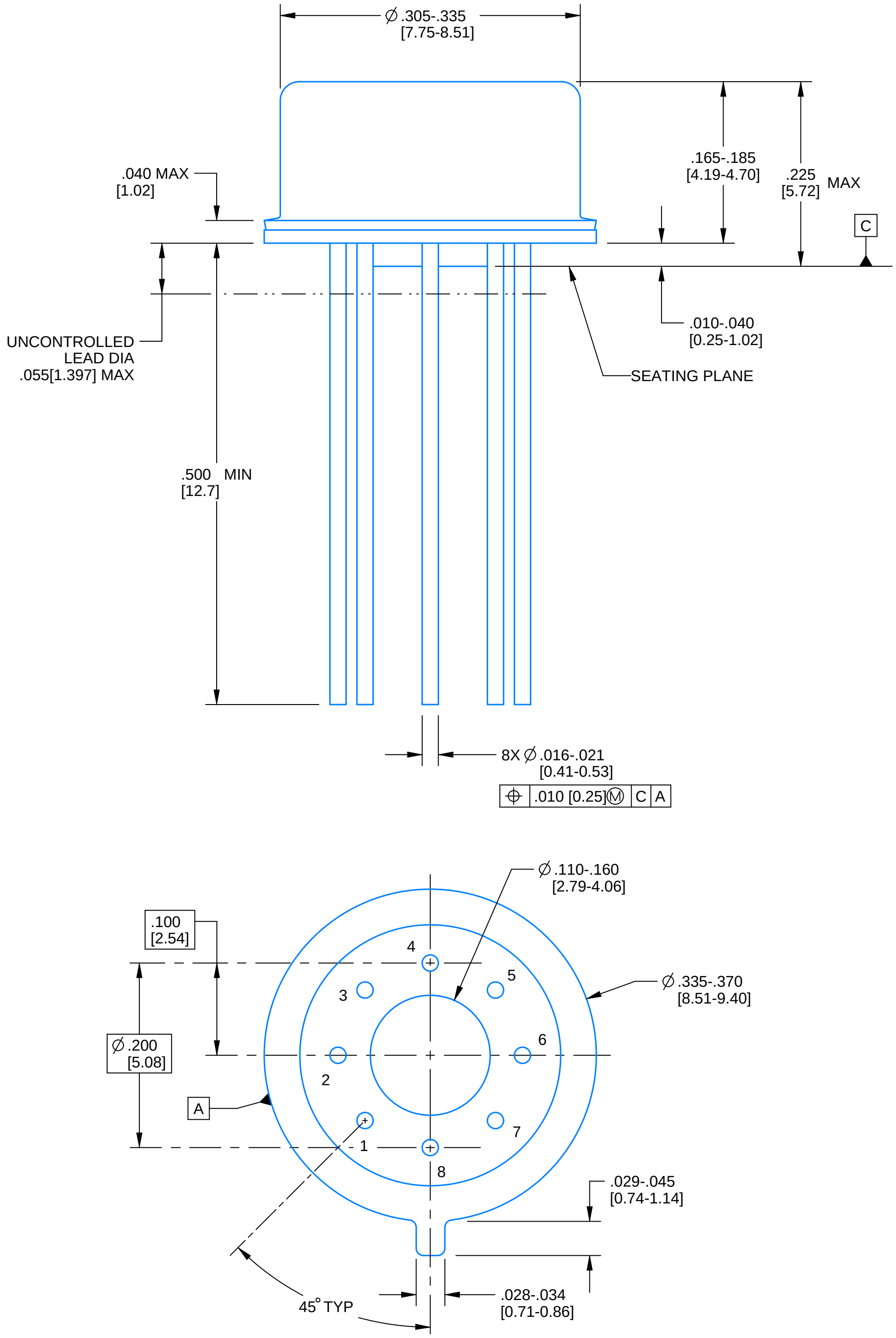
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
JL101ABGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
JM38510/10103BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
M38510/10103BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAB0008A



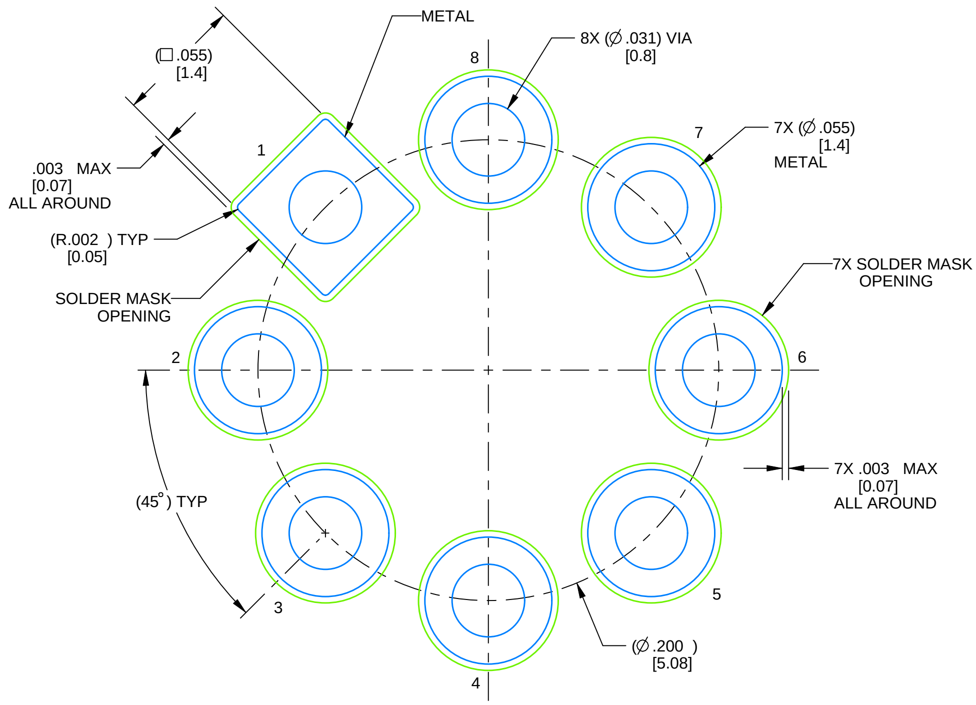
J08A (Rev M)



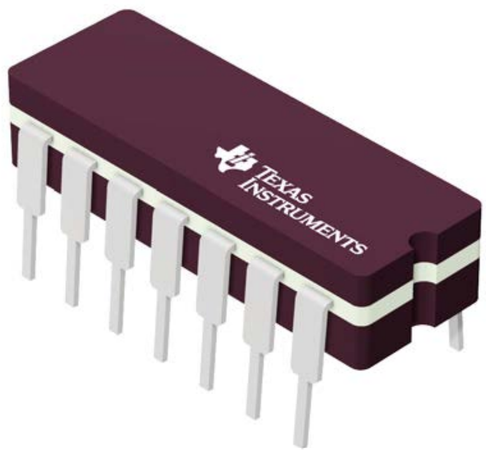
4220610/B 09/2024

NOTES:

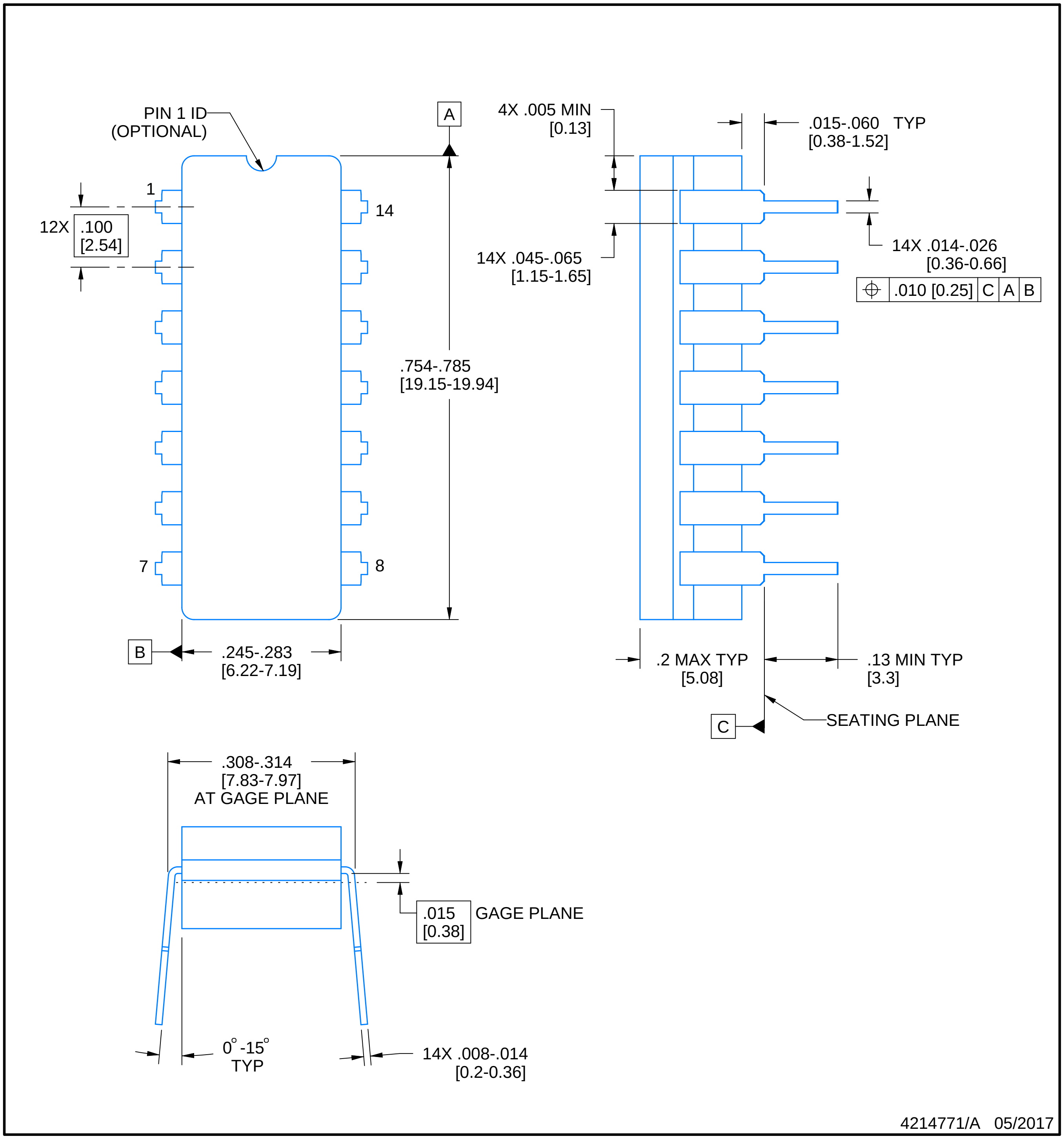
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

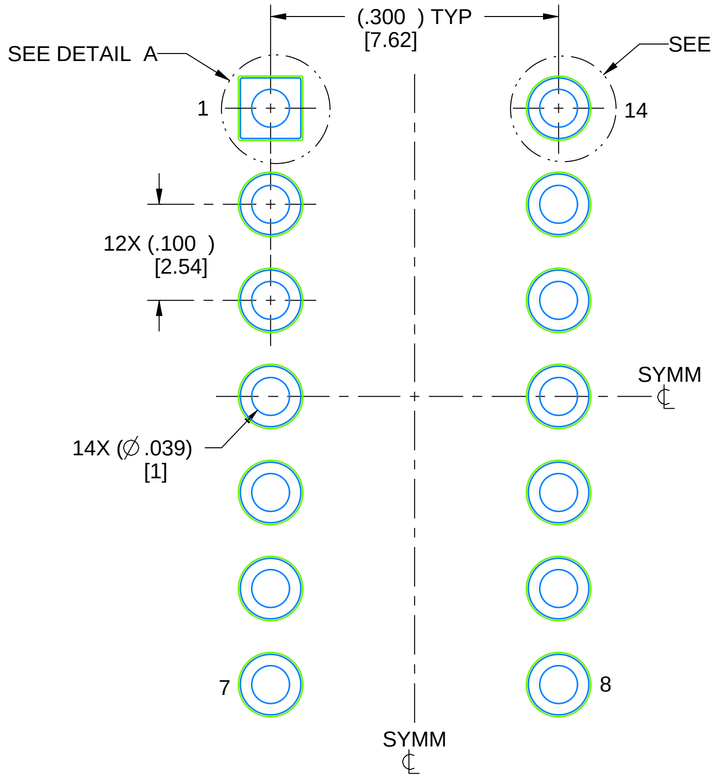


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

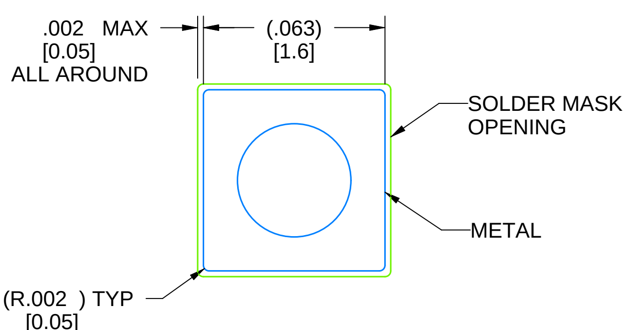


NOTES:

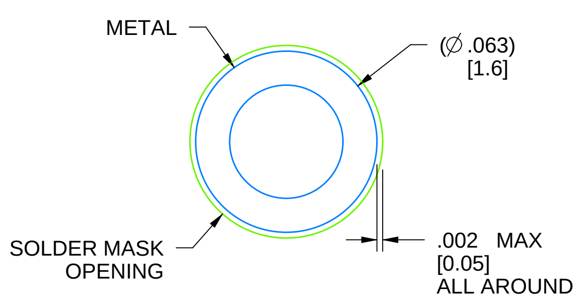
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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