LM10504 Triple Buck and LDO Power Management Unit

1 Features

- Three High-Efficiency Programmable Buck Regulators
  - Integrated FETs With Low R_{DSON}
  - Bucks Operate With Their Phases Shifted to Reduce the Input Current Ripple and Capacitor Size
  - Programmable Output Voltage Through the SPI Interface
  - Overvoltage and Undervoltage Lockout
  - Automatic Internal Soft Start With Power-On Reset
  - Current Overload and Thermal Shutdown Protection
  - PFM Mode for Low-Load, High-Efficiency Operation
- Power-Down Data Protection Enhances Data Integrity
  - Bypass Mode Available on Bucks 1 and 2
- Deep Sleep Mode to Save Power During Idle Times With DevSLP Function
- Programmable Low-Dropout LDO 1.2 V to 3.1 V, up to 250 mA
- SPI-Programmable Interrupt Comparator (2 V to 4 V)
- Alternate Buck V_{OUTS} Selectable Through V_{SELECT} Logic Pins
- Customizable Start-Up Sequencing for Varied Controllers
- RESET Pin
- Programmable Buck Regulators:
  - Buck 1: 1.1 V to 3.6 V at 1.6 A
  - Buck 2: 1.1 V to 3.6 V at 1 A
  - Buck 3: 0.7 V to 1.335 V at 1 A
- ±3% Feedback Voltage Accuracy
- Up to 95% Efficient Buck Regulators
- 2-MHz Switching Frequency for Smaller Inductor Size

2 Applications

Solid-State Drives

3 Description

The LM10504 is an advanced PMU containing three configurable, high-efficiency buck regulators for supplying variable voltages. The device is ideal for supporting ASIC and SOC designs for solid-state and flash drives.

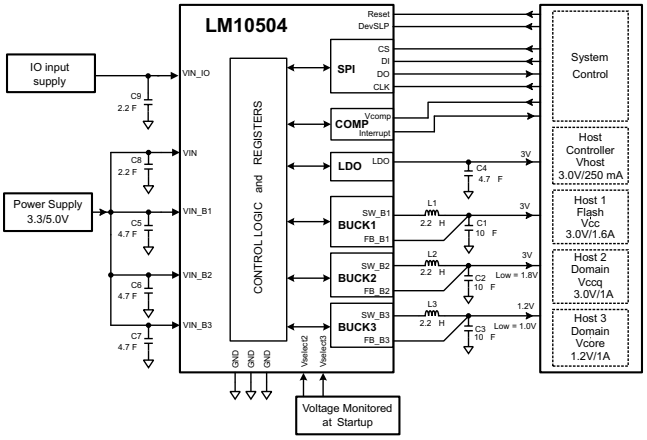
The LM10504 operates cooperatively with ASIC to optimize the supply voltage for low-power conditions and power saving modes through the SPI interface. It also supports a 250-mA LDO and a programmable interrupt comparator.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM10504	DSBGA (34)	2.80 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F — **Page**

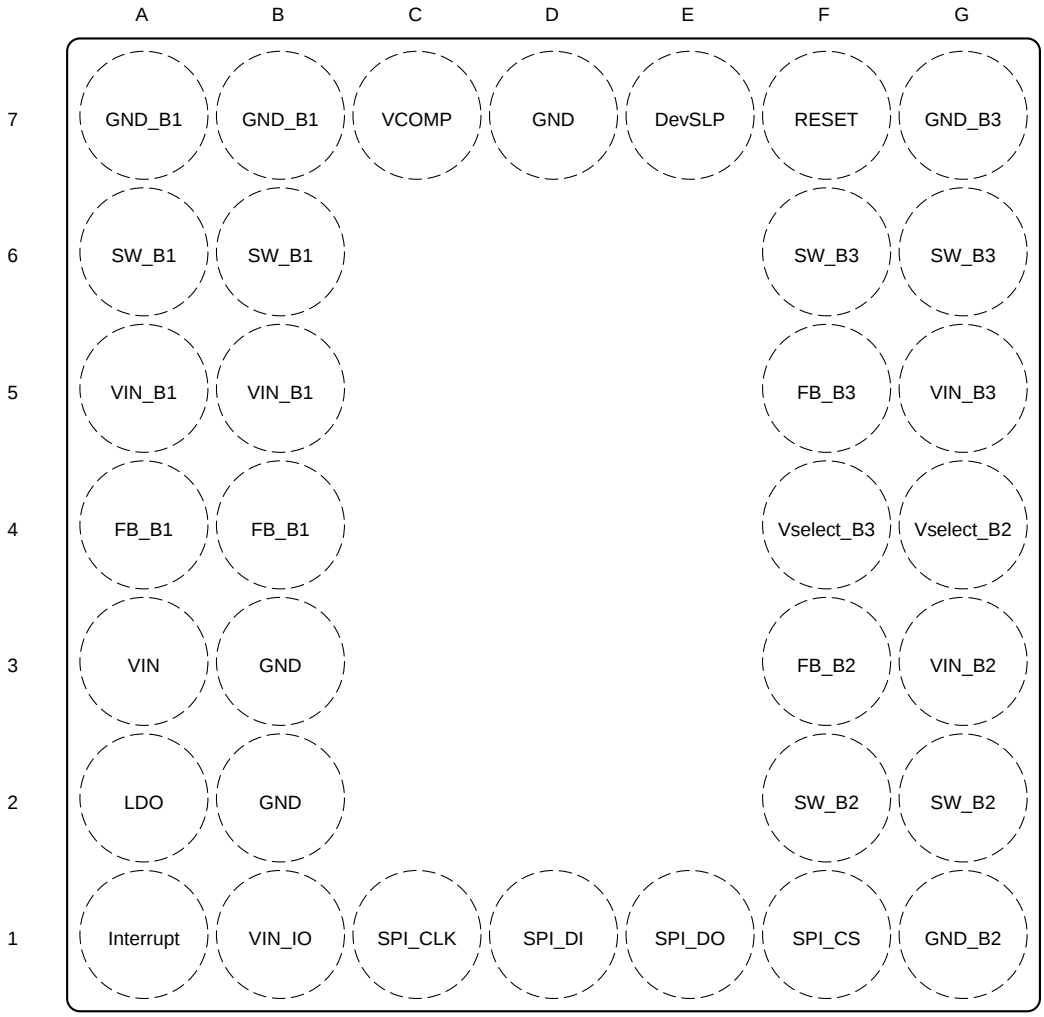
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed $R_{\theta JA}$ value in the *Thermal Information* table From: 44.5 To: 65.5 ... 5

Changes from Revision D (March 2013) to Revision E — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Pin Configuration and Functions

YFR Package
34-Pin DSBGA
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	Interrupt	O	Digital output of comparator to signal interrupt condition.
A2	LDO	P	LDO regulator output voltage.
A3	VIN	P	Power supply input voltage. Must be present for device to work; decouple closely to D7.
A4, B4	FB_B1	I/O	Buck switcher regulator 1: Voltage output feedback plus bypass power.
A5, B5	VIN_B1	P	Buck switcher regulator 1: Power supply voltage input for power stage PFET, if Buck 1 is not used, tie to ground to reduce leakage.
A6, B6	SW_B1	P	Buck switcher regulator 1: Power switching node, connect to inductor.
A7, B7	GND_B1	P	Buck switcher regulator 1: Power ground for buck regulator.
B1	VIN_IO	I	Supply voltage for digital interface.
B2	GND	G	Connect to system ground.

(1) G = Ground, I = Input, O = Output, and P = Power

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
B3	GND	G	Connect to system ground.
C1	SPI_CLK	I	SPI interface: Serial clock input.
C7	VCOMP	I	Analog input for comparator.
D1	SPI_DI	I	SPI interface: Serial data input.
D7	GND	G	Connect to system ground; decouple closely to A3.
E1	SPI_DO	O	SPI interface: Serial data output.
E7	DevSLP	I	Digital input control signal for entering device sleep mode. This is an active high pin with an internal pulldown resistor. Lowers core ASIC voltage and turns off the FLASH and I/O bucks.
F1	SPI_CS	I	SPI interface: Chip select.
F2, G2	SW_B2	P	Buck switcher regulator 2: Power switching node, connect to inductor.
F3	FB_B2	I	Buck switcher regulator 2: Voltage output feedback.
F4	Vselect_B3	I	Digital input start-up control signal to change predefined output voltage of buck 3, internally pulled up as a default.
F5	FB_B3	I	Buck switcher regulator 3: Voltage output feedback.
F6, G6	SW_B3	P	Buck switcher regulator 3: Power switching node, connect to inductor.
F7	RESET	I	Digital input control signal to abort SPI transactions; resets the PMIC to default voltages. This is an active low pin with an internal pullup.
G1	GND_B2	P	Buck switcher regulator 2: Power ground for buck regulator.
G3	VIN_B2	P	Buck switcher regulator 2: Power supply voltage input for power stage PFET, if buck 2 is not used, tie to ground to reduce leakage.
G4	Vselect_B2	I	Digital input start-up control signal to change predefined output voltage of buck 2, internally pulled down as a default.
G5	VIN_B3	P	Buck switcher regulator 3: Power supply voltage input for power stage PFET.
G7	GND_B3	P	Buck switcher regulator 3: Power ground for buck regulator.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN, VCOMP	–0.3	6	V
VIN_IO, VIN_B1, VIN_B2, VIN_B3, SPI_CS, SPI_DI, SPI_CLK, SPI_DO, Vselect_B2,Vselect_B3, RESET, SW_1, SW_2, SW_3, FB_1, FB_2, FB_3, LDO, Interrupt, DevSLP	–0.3	6	V
Junction temperature, $T_{J\text{-}MAX}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
	VIN_B1, VIN_B2_VIN_B3, VIN	3	5.5	V
	VIN_IO	1.72	3.63	V
	All pins other than VIN_IO	0	V_{IN}	V
$P_{D\text{-}MAX}$	Maximum continuous power dissipation		0.9	W
T_A	Ambient temperature	–30	85	°C
T_J	Junction temperature	–30	125	°C

(1) Internal thermal shutdown protects device from permanent damage. Thermal shutdown engages at T_J = 140°C and disengages at T_J = 120°C (typically). Thermal shutdown is ensured by design.
(2) In applications where high power dissipation or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.
(3) The amount of absolute maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A) / R_{\theta JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance. $R_{\theta JA}$ is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage (see *Electrical Characteristics – General*).

6.4 Thermal Information

THERMAL METRIC(1)		LM10504 YFR (DSBGA) 34 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – General

T_J = 25°C and V_{IN} = 5 V where V_{IN} = V_{IN_B1} = V_{IN_B2} = V_{IN_B3} (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q(DEVSLP)}$	Quiescent supply current	DevSLP = HIGH, no load	T_J = 25°C		100		µA
			–30°C ≤ T_J ≤ 85°C			200	
UNDERVOLTAGE OR OVERVOLTAGE LOCKOUT							
V_{UVLO_RISING}	Undervoltage lockout, rising	T_J = 25°C			2.9		V
		–30°C ≤ T_J ≤ 85°C		2.75		3.05	
$V_{UVLO\_FALLING}$	Undervoltage lockout, falling	T_J = 25°C			2.6		V
		–30°C ≤ T_J ≤ 85°C		2.45		2.75	
V_{OVLO_RISING}	Overvoltage lockout, rising				5.64		V
$V_{OVLO\_FALLING}$	Overvoltage lockout, falling				5.54		V
DIGITAL INTERFACE							
V_{IL}	Logic input low	SPI_CS, SPI_DI, SPI_CLK, RESET, DevSLP, –30°C ≤ T_J ≤ 85°C		0.7 × VIN_IO		0.3 × VIN_IO	V
V_{IH}	Logic input high	SPI_CS, SPI_DI, SPI_CLK, RESET, DevSLP, –30°C ≤ T_J ≤ 85°C					
V_{IL}	Logic input low	Vselect_B2, Vselect_B3, –30°C ≤ T_J ≤ 85°C		0.7 × VIN		0.3 × VIN	V
V_{IH}	Logic input high	Vselect_B2, Vselect_B3, –30°C ≤ T_J ≤ 85°C					
V_{OL}	Logic output low	SPI_DO, –30°C ≤ T_J ≤ 85°C		0.8 × VIN_IO		0.2 × VIN_IO	V
V_{OH}	Logic output high	SPI_DO, –30°C ≤ T_J ≤ 85°C					
I_{IL}	Input current, pin driven low	SPI_CS, SPI_DI, SPI_CLK, Vselect_B2, DevSLP		–2			µA
		Vselect_B3, RESET		–5			
I_{IH}	Input current, pin driven high	SPI_CS, SPI_DI, SPI_CLK, Vselect_B3, RESET				2	µA
		Vselect_B2, DevSLP				5	
f_{SPI_MAX}	SPI max frequency	–30°C ≤ T_J ≤ 85°C				10	MHz
t_{RESET}	Minimum pulse width(3)	–30°C ≤ T_J ≤ 85°C			2		µs
t_{DEVSLP}							

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

6.6 Electrical Characteristics – Buck 1

T_J = 25°C and V_{IN} = 5 V where V_{IN}=V_{IN_B1} = V_{IN_B2} = V_{IN_B3} (unless otherwise noted)(1)(2)(3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	V_{IN} DC bias current	No load, PFM mode	T_J = 25°C		15		µA
			–30°C ≤ T_J ≤ 85°C			50	
I_{OUT_MAX}	Continuous maximum load current(4)(5)	Buck 1 enabled, switching in PWM, –30°C ≤ T_J ≤ 85°C		1.6			A
I_{PEAK}	Peak switching current limit	Buck 1 enabled, switching in PWM	T_J = 25°C		2.1		A
			–30°C ≤ T_J ≤ 85°C	1.9		2.6	
η	Peak efficiency(4)	I_{OUT} = 0.3 A			90%		
F_{SW}	Switching frequency	T_J = 25°C			2		MHz
		–30°C ≤ T_J ≤ 85°C		1.75		2.3	
C_{IN}	Input capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			4.7		µF
C_{OUT}	Output filter capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		10	10	100	
	Output capacitor ESR(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$				20	mΩ
L	Output filter inductance(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			2.2		µH
ΔVOUT	DC line regulation(4)	3.3 V ≤ V_{IN} ≤ 5 V, I_{OUT} = $I_{OUT-MAX}$			0.5%		V
	DC load regulation(4)	100 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			0.3%		A
I_{FB}	Feedback pin input bias current	V_{FB} = 3 V	T_J = 25°C		2.1		µA
			–30°C ≤ T_J ≤ 85°C			5	
$R_{DS-ON-HS}$	High-side switch on resistance				135		mΩ
		V_{IN} = 2.6 V			215		
$R_{DS-ON-LS}$	Low-side switch on resistance	T_J = 25°C			85		mΩ
		–30°C ≤ T_J ≤ 85°C				190	
$R_{DS-ON-BYPASS}$	Bypass FET on resistance	Used in parallel with the high-side FET while in bypass mode. Resistance (DCR) of inductor = 100 mΩ					
		V_{IN} = 3.3 V			85		mΩ
		V_{IN} = 2.6 V			120		
START-UP							
T_{START}	Internal soft-start (turnon time)(4)	Start up from shutdown, V_{OUT} = 0 V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value			0.1		ms

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT} + 1 V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.7 Electrical Characteristics – Buck 2

T_J = 25°C and V_{IN} = 5 V where V_{IN}=V_{IN_B1} = V_{IN_B2} = V_{IN_B3} (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	V_{IN} DC bias current	No load, PFM mode	T_J = 25°C		15		µA
			–30°C ≤ T_J ≤ 85°C			50	
I_{OUT_MAX}	Continuous maximum load current(4)(5)	Buck 2 enabled, switching in PWM, –30°C ≤ T_J ≤ 85°C		1			A
I_{PEAK}	Peak switching current limit	Buck 2 enabled, switching in PWM	T_J = 25°C		1.56		A
			–30°C ≤ T_J ≤ 85°C	1.35		1.8	
η	Peak efficiency(4)	I_{OUT} = 0.3 A			90%		
F_{SW}	Switching frequency	T_J = 25°C			2		MHz
		–30°C ≤ T_J ≤ 85°C		1.75		2.3	
C_{IN}	Input capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			4.7		µF
C_{OUT}	Output filter capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		10	10	100	
	Output capacitor ESR(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$				20	mΩ
L	Output filter inductance(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			2.2		µH
ΔVOUT	DC line regulation(4)	3.3 V ≤ V_{IN} ≤ 5 V, I_{OUT} = $I_{OUT-MAX}$			0.5%		V
	DC load regulation(4)	100 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			0.3%		A
I_{FB}	Feedback pin input bias current	V_{FB} = 1.8 V	T_J = 25°C		1.8		µA
			–30°C ≤ T_J ≤ 85°C			5	
$R_{DS-ON-HS}$	High-side switch on resistance				135		mΩ
		V_{IN} = 2.6 V			260		
$R_{DS-ON-LS}$	Low-side switch on resistance	T_J = 25°C			85		
		–30°C ≤ T_J ≤ 85°C				190	
START-UP							
T_{START}	Internal soft-start (turnon time)(4)	Start up from shutdown, V_{OUT} = 0 V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value			0.1		ms

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if V_{IN} ≥ V_{OUT} + 1 V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part or package in the application ($R_{\theta JA}$), as given by the following equation: T_{A-MAX} = $T_{J-MAX-OP}$ – ($R_{\theta JA}$ × P_{D-MAX}).

6.8 Electrical Characteristics – Buck 3

T_J = 25°C and V_{IN} = 5 V where $V_{IN} = V_{IN\_B1} = V_{IN\_B2} = V_{IN\_B3}$ (unless otherwise noted)(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	V_{IN} DC bias current	No load, PFM mode	T_J = 25°C		15		µA
			–30°C ≤ T_J ≤ 85°C			50	
I_{OUT_MAX}	Continuous maximum load current(4)(5)	Buck 3 enabled, switching in PWM, –30°C ≤ T_J ≤ 85°C		1			A
I_{PEAK}	Peak switching current limit	Buck 3 enabled, switching in PWM	T_J = 25°C		1.56		A
			–30°C ≤ T_J ≤ 85°C	1.35		1.8	
η	Peak efficiency(4)	I_{OUT} = 0.3 A			90%		
F_{SW}	Switching frequency	T_J = 25°C			2		MHz
		–30°C ≤ T_J ≤ 85°C		1.75		2.3	
C_{IN}	Input capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			4.7		µF
C_{OUT}	Output filter capacitor(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		10	10	100	
	Output capacitor ESR(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$				20	mΩ
L	Output filter inductance(4)	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			2.2		µH
ΔVOUT	DC line regulation(4)	3.3 V ≤ V_{IN} ≤ 5 V, I_{OUT} = $I_{OUT-MAX}$			0.5%		V
	DC load regulation(4)	100 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$			0.3%		A
I_{FB}	Feedback pin input bias current	V_{FB} = 1.2 V	T_J = 25°C		0.9		µA
			–30°C ≤ T_J ≤ 85°C			5	
$R_{DS-ON-HS}$	High-side switch on resistance				135		mΩ
		V_{IN} = 2.6 V			260		
$R_{DS-ON-LS}$	Low-side switch on resistance	T_J = 25°C			85		
		–30°C ≤ T_J ≤ 85°C				190	
START-UP							
T_{START}	Internal soft-start (turnon time)(4)	Start up from shutdown, V_{OUT} = 0 V, no load, LC = recommended circuit, using software enable, to V_{OUT} = 95% of final value			0.1		ms

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if $V_{IN} \geq V_{OUT}$ + 1 V.
(4) Specification ensured by design. Not tested during production.
(5) In applications where high power dissipation or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.9 Electrical Characteristics – LDO

T_J = 25°C and V_{IN} = 5 V where: $V_{IN} = V_{IN\_B1} = V_{IN\_B2} = V_{IN\_B3}$ (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage accuracy	I_{OUT} = 1 mA, –30°C ≤ T_J ≤ 85°C		–3%		3%	
I_{OUT}	Maximum output current			250			mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			0.5		A
V_{DO}	Dropout voltage	I_{OUT} = 250 mA	T_J = 25°C		160		mV
			–30°C ≤ T_J ≤ 85°C			220	
ΔV_{OUT}	Line regulation	3.3 V ≤ V_{IN} ≤ 5 V, I_{OUT} = 1 mA			5		
	Load regulation	1 mA ≤ I_{OUT} ≤ 250 mA, V_{IN} = 3.3 V, 5 V			5		
e_N	Output noise voltage(3)	10 Hz ≤ f ≤ 100 kHz	V_{IN} = 5 V		10		μV_{RMS}
			V_{IN} = 3.3 V		35		
PSRR	Power supply rejection ratio(3)	F = 10 kHz, C_{OUT} = 4.7 µF, I_{OUT} = 20 mA	V_{IN} = 5 V		65		dB
			V_{IN} = 3.3 V		40		
T_{START}	Start-up time from shutdown(3)	C_{OUT} = 4.7 µF, I_{OUT} = 250 mA	V_{IN} = 5 V		45		µs
			V_{IN} = 3.3 V		60		
$T_{TRANSIENT}$	Start-up transient overshoot(3)	C_{OUT} = 4.7 µF, I_{OUT} = 250 mA, –30°C ≤ T_J ≤ 85°C				30	mV

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

6.10 Electrical Characteristics – Comparators

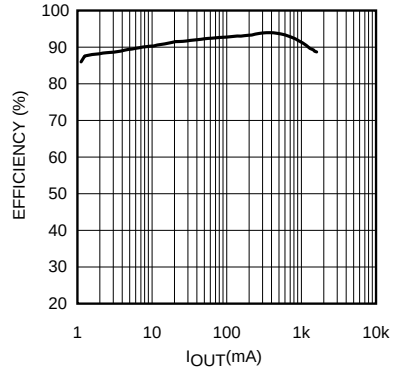
T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VCOMP}	VCOMP pin bias current	V_{COMP} = 0 V	T_J = 25°C		0.1		µA
			–30°C ≤ T_J ≤ 85°C			2	
		V_{COMP} = 5 V	T_J = 25°C		0.1		
			–30°C ≤ T_J ≤ 85°C			2	
V_{COMP_RISE}	Comparator rising edge trigger level				2.79		V
V_{COMP_FALL}	Comparator falling edge trigger level				2.74		
	Hysteresis	T_J = 25°C			60		mV
		–30°C ≤ T_J ≤ 85°C		30		80	
$Interrupt_{VOH}$	Output voltage high	–30°C ≤ T_J ≤ 85°C				0.8 × VIN_IO	V
$Interrupt_{VOL}$	Output voltage low	–30°C ≤ T_J ≤ 85°C		0.2 × VIN_IO			
t_{COMP}	Transition time of interrupt output	T_J = 25°C			6		µs
		–30°C ≤ T_J ≤ 85°C				15	

(1) All limits are ensured by design, test, or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR surface-mount ceramic capacitors (MLCCs) are used in setting electrical characteristics.

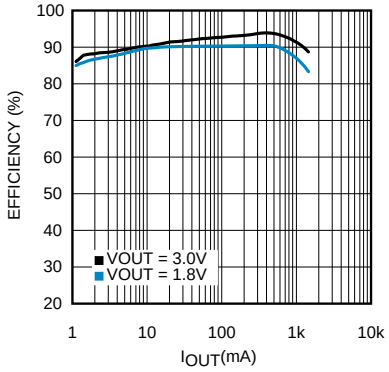
6.11 Typical Characteristics

T_A = 25°C (unless otherwise noted)



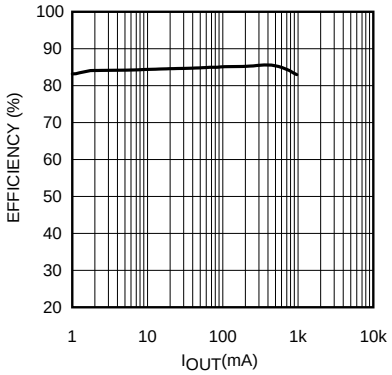
V_{IN}= 5 V V_{OUT} = 3 V

Figure 1. Efficiency of Buck 1



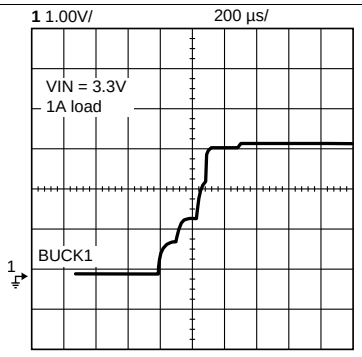
V_{IN} = 5 V

Figure 2. Efficiency of Buck 2



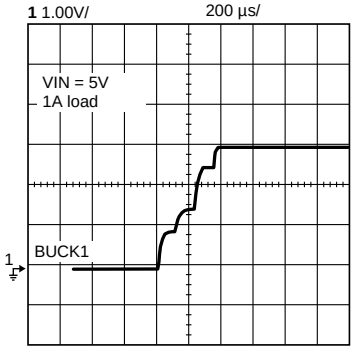
V_{IN} = 5 V V_{OUT} = 1 V

Figure 3. Efficiency of Buck 3



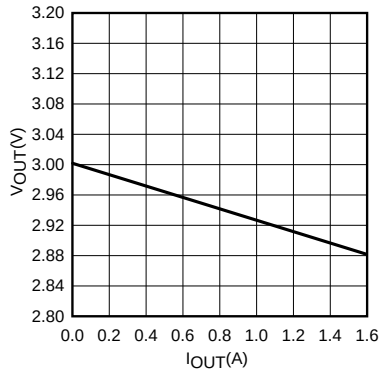
V_{IN} = 3.3 V V_{OUT} = 3 V

Figure 4. Start-Up of Buck 1



V_{IN} = 5 V V_{OUT} = 3 V

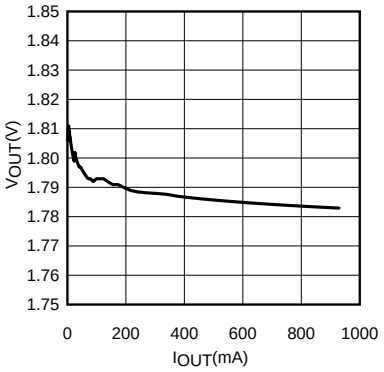
Figure 5. Start-Up of Buck 1



V_{IN} = 5 V V_{OUT} = 3 V

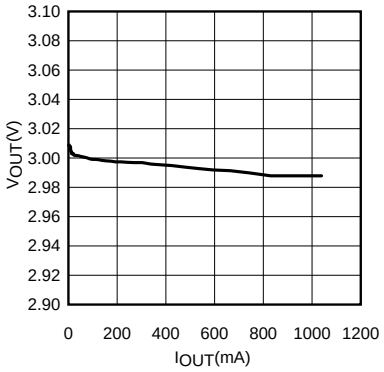
Figure 6. Buck 1 V_{OUT} vs I_{OUT}

Typical Characteristics (continued)



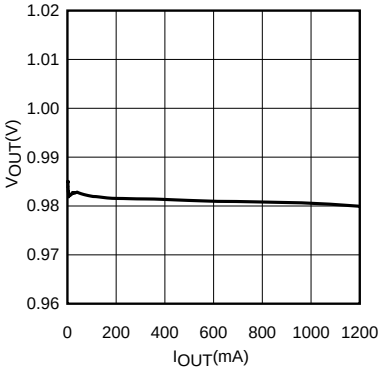
V_{IN} = 5 V V_{OUT} = 1.8 V

Figure 7. Buck 2 V_{OUT} vs I_{OUT}



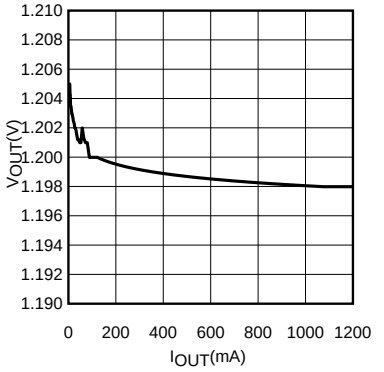
V_{IN} = 5 V V_{OUT} = 3 V

Figure 8. Buck 2 V_{OUT} vs I_{OUT}



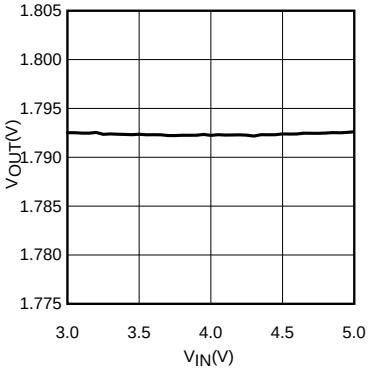
V_{IN} = 5 V V_{OUT} = 1 V

Figure 9. Buck 3 V_{OUT} vs I_{OUT}



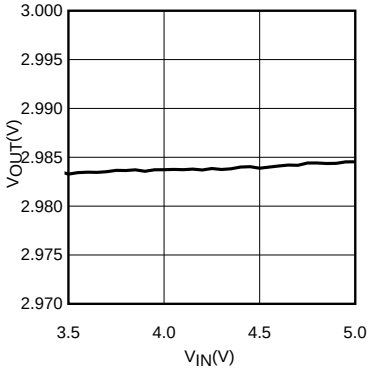
V_{IN} = 5 V V_{OUT} = 1.2 V

Figure 10. Buck 3 V_{OUT} vs I_{OUT}



V_{OUT} = 1.8 V I_{OUT} = 1 A

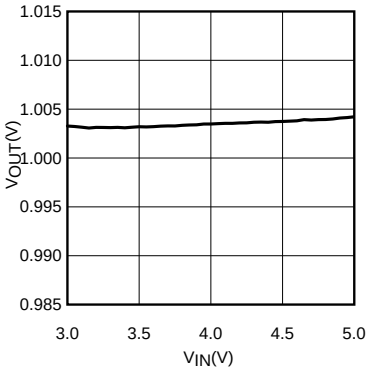
Figure 11. Buck 2 V_{OUT} vs V_{IN}



V_{OUT} = 3 V I_{OUT}= 1 A

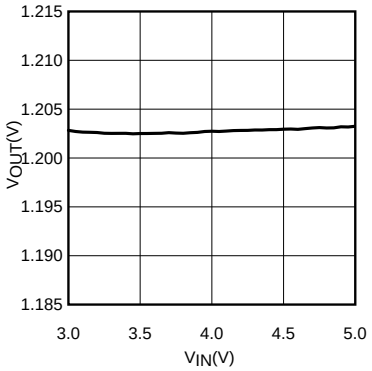
Figure 12. Buck 2 V_{OUT} vs V_{IN}

Typical Characteristics (continued)



V_{OUT}= 1 V I_{OUT}= 1 A

Figure 13. Buck 3 V_{OUT} vs V_{IN}



V_{OUT}= 1.2 V I_{OUT} = 1 A

Figure 14. Buck 3 V_{OUT} vs V_{IN}

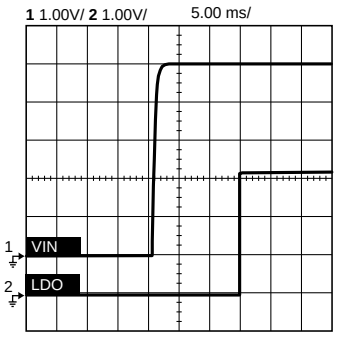


Figure 15. LDO Start-Up Time from V_{IN} Rise

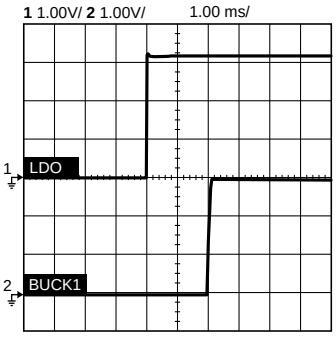


Figure 16. From LDO Start-Up to Buck 1 Start-Up

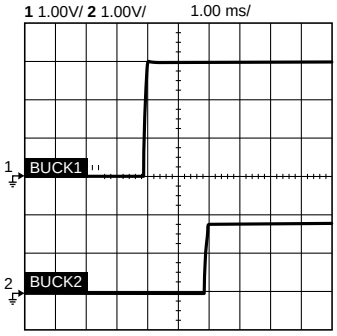


Figure 17. From Buck 1 Start-Up to Buck 2 Start-Up

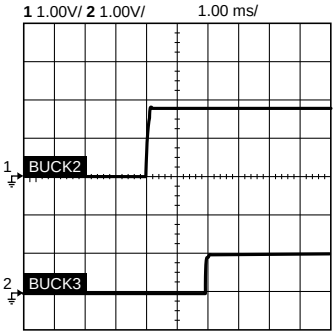


Figure 18. From Buck 2 Start-Up to Buck 3 Start-Up

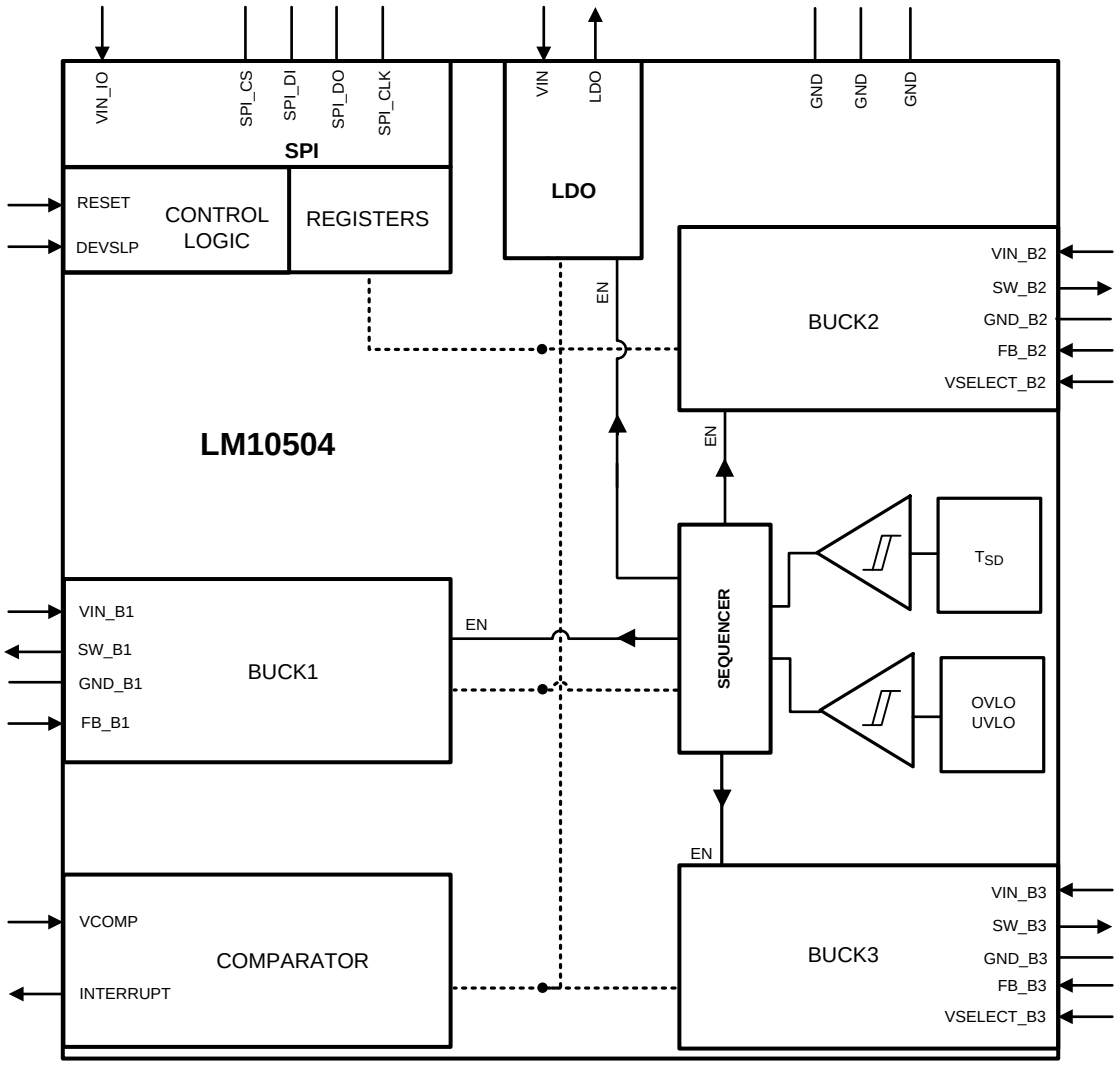
7 Detailed Description

7.1 Overview

LM10504 is a highly efficient and integrated power management unit for systems-on-a-chip (SoCs), ASICs, and processors. It operates cooperatively and communicates with processors over an SPI interface with output voltage programmability.

The device incorporates three high-efficiency synchronous buck regulators and one LDO that deliver four output voltages from a single power source. The device also includes a SPI-programmable comparator block that provides an interrupt output signal.

7.2 Functional Block Diagram



7.3 Feature Description

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground and a feedback path. Figure 19 shows the block diagram of each of the three buck regulators integrated in the device.

Feature Description (continued)

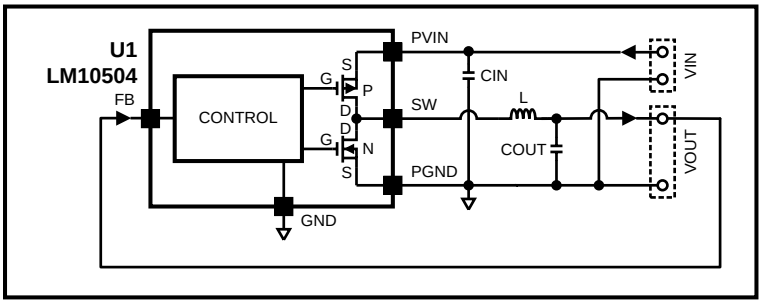


Figure 19. Buck Functional Diagram

During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN} – V_{OUT}) / L by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of (–V_{OUT}) / L.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

7.3.1 Buck Regulators Description

The LM10504 incorporates three high-efficiency synchronous switching buck regulators that deliver various voltages from a single DC input voltage. They include many advanced features to achieve excellent voltage regulation, high efficiency, and fast transient response time. The bucks feature voltage mode architecture with synchronous rectification.

Each of the switching regulators is specially designed for high-efficiency operation throughout the load range. With a 2MHz typical switching frequency, the external L-C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

All bucks can operate up to a 100% duty cycle allowing for the lowest possible input voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on.

Additional features include soft start, undervoltage lockout, bypass, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the 3 bucks at 120° phase. These bucks are nearly identical in performance and mode of operation. They can operate in FPWM (forced PWM) or automatic mode (PWM/PFM).

7.3.2 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feedforward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, a feedforward voltage inversely proportional to the input voltage is introduced.

In forced PWM mode the bucks always operate in PWM mode regardless of the output current.

Feature Description (continued)

In automatic mode, if the output current is less than 70 mA (typical), the bucks automatically transition into Pulse Frequency Modulation (PFM) operation to reduce the current consumption. At higher than 100 mA (typical), they operate in PWM mode. This increases the efficiency at lower output currents. The 30-mA (typical) hysteresis is designed in for stable mode transition.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. In this case the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

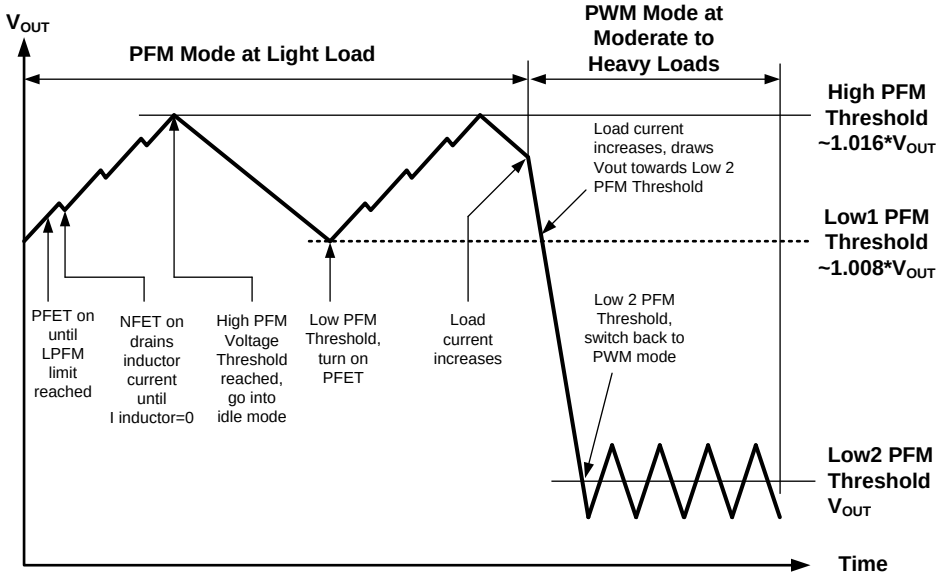


Figure 20. PFM vs PWM Operation

7.3.3 PFM Operation

At very light loads, Bucks 1, 2, and 3 enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Bucks 1, 2, and 3 automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous
2. The peak PMOS switch current drops below the I_{MODE} level.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage through the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode.

Feature Description (continued)

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 20), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the *high* PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this *idle* mode is less than 100 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to approximately 1.6% above the nominal PWM output voltage.

If the load current must increase during PFM mode causing the output voltage to fall below the 'low2' PFM threshold, the part automatically transitions into fixed-frequency PWM mode.

7.3.4 Soft Start

Each of the buck converters has an internal soft-start circuit that limits the in-rush current during start-up. This allows the converters to gradually reach the steady-state operating point, thus reducing start-up stresses and surges. During start-up, the switch current limit is increased in steps.

For Bucks 1, 2, and 3 the soft start is implemented by increasing the switch current limit in steps that are gradually set higher. The start-up time depends on the output capacitor size, load current, and output voltage. Typical start-up time with the recommended output capacitor of 10 µF is 0.2 to 1ms. It is expected that in the final application the load current condition is more likely in the lower load current range during start-up.

7.3.5 Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

7.3.6 Internal Synchronous Rectification

While in PWM mode, the bucks use an internal NFET as a synchronous rectifier to reduce the rectifier forward voltage drop and the associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

7.3.7 Bypass-FET Operation on Buck 1 and Buck 2

There is an additional bypass FET used on Buck 1. The FET is connected in parallel to high-side FET and inductor. Buck 2 has no extra bypass FET; it uses high-side FET (PFET) for bypass operation. If Buck 1 input voltage is greater than 3.5 V (2.6 V for Buck 2), the bypass function is disabled. The determination of whether or not the Buck regulators are in bypass mode or standard switching regulation is constantly monitored while the regulators are enabled. If at any time the input voltage goes above 3.5 V (2.6 V for Buck 2) while in bypass mode, the regulators transitions to normal operation.

When the bypass mode is enabled, the output voltage of the buck that is in bypass mode is not regulated, but instead, the output voltage follows the input voltage minus the voltage drop seen across the FET and DCR of the inductor. The voltage drop is a direct result of the current flowing across those resistive elements. When Buck 1 transitions into bypass mode, there is an extra FET used in parallel along with the high-side FET for transmission of the current to the load. This added FET helps reduce the resistance seen by the load and decrease the voltage drop. For Buck 2, the bypass function uses the same high-side FET.

Feature Description (continued)

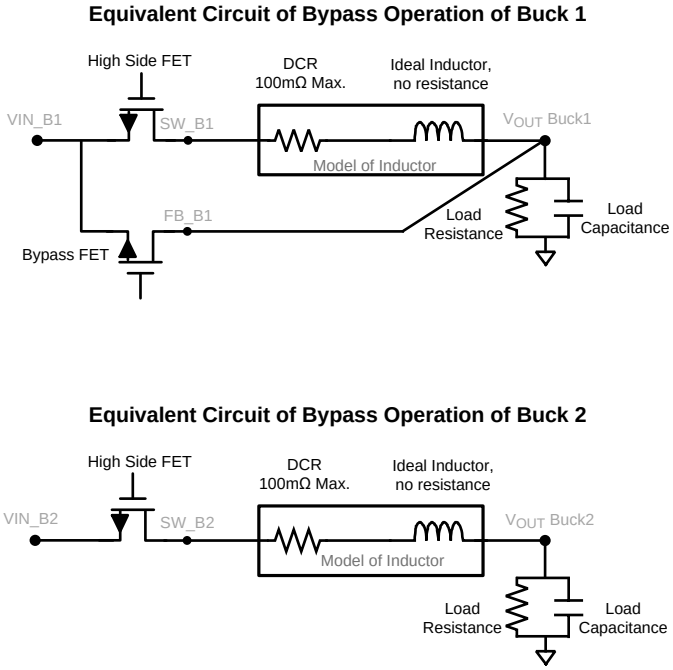


Figure 21. Bypass Operations for Buck 1 and Buck 2

7.3.8 Low Dropout Operation

The device can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support. In this way, the output voltage is controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage is calculated with Equation 1.

$$V_{IN\_MIN} = V_{OUT} + I_{LOAD} \times (R_{DSON\_PFET} + R_{IND}) \quad (1)$$

where

- I_{LOAD} is the load current
- R_{DSON_PFET} is the drain to source resistance of PFET (high-side)
- R_{IND} is the inductor resistance

7.3.9 Out of Regulation

When any of the Buck outputs are taken out of regulation (below 85% of the output level), the device starts a shutdown sequence and all other outputs switch off normally. The device restarts when the forced out-of-regulation condition is removed.

7.4 Device Functional Modes

7.4.1 Start-Up Sequence

The start-up mode of the LM10504 depends on the input voltage. Once VIN reaches the UVLO threshold, there is a 15-ms delay before the LM10504 determines how to set up the buck regulators. If V_{IN} is below 3.6 V, then Buck 1 and Buck 2 are in bypass mode; see *Bypass-FET Operation on Buck 1 and Buck 2* for functionality description. If the VIN voltage is greater than 3.6 V, the bucks start up as standard regulators. The 3 buck regulators are staggered during start-up to avoid large inrush currents. There is a fixed delay of 2 ms between the start-up of each regulator.

Device Functional Modes (continued)

The start-up sequence is:

1. 15 msec (±30%) delay after V_{IN} above UVLO
2. LDO → 3.2 V
3. 2-ms delay
4. Buck 1 → 3 V
5. 2-ms delay
6. Buck 2 → 3 V or if Vselect_B2 = Low → 1.8 V
7. 2-ms delay
8. Buck 3 → 1.2 V or if Vselect_B3 = Low → 1 V

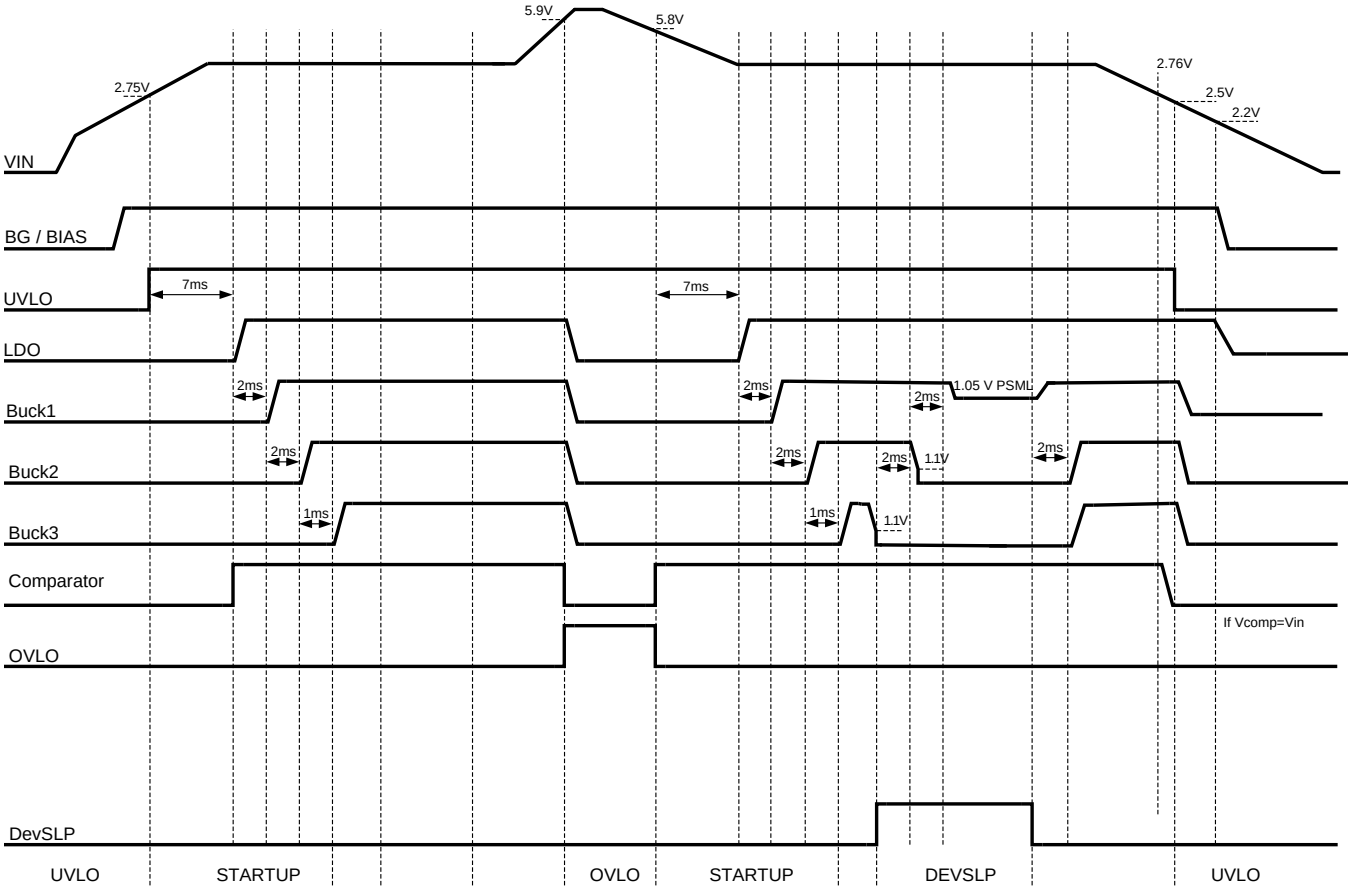


Figure 22. Operating Modes

7.4.2 Power-On Default and Device Enable

The device is always enabled and the LDO is always on, unless outside of operating voltage range. There is no LM10504 Enable pin. Once V_{IN} reaches a minimum required input voltage, the power-up sequence is started automatically and the start-up sequence is initiated. Once the device is started, the output voltage of the Bucks 1 and 2 can be individually disabled by accessing their corresponding BKEN register bits (BUCK CONTROL).

7.4.3 Reset Pin Function

The RESET pin is internally pulled high. If the RESET pin is pulled low, the device performs a complete reset of all the registers to their default states. This means that all of the voltage settings on the regulators go back to their default states.

Device Functional Modes (continued)

7.4.4 DevSLP Function

The device can be placed into sleep (DevSLP) mode. There are two ways for doing that:

1. DevSLP pin
2. Programming through the SPI

Bucks 1 and 2 are ramped down when the disable signal is given. Buck 1 starts ramping 2 ms after Buck 2 has started ramping.

To enter the DevSLP sequence:

1. Buck 3 → PSML (Programmable DevSLP Mode Level)
2. 2-ms delay
3. Buck 2 → Disabled
4. 2-ms delay
5. Buck 1 → Disabled

7.4.4.1 DevSLP Pin

When the DevSLP pin is asserted high, the LM10504 enters sleep mode. While in sleep mode, Buck 1 and Buck 2 are disabled. Buck 3's output voltage is transitioned to the programmable sleep mode level (PSML) as set by LM10504 register 0x09. The DevSLP pin is internally pulled down, and there is a 1-s delay during power up before the state of the DevSLP pin is checked.

NOTE

If Buck 1 and Buck 2 are already disabled, and the DevSLP pin is asserted high, then Buck 3 does not go to PSML. For further instructions, see *DevSLP Programming Through SPI*. Bucks 1 and 2 are ramped down when the disable signal is given. Buck 1 starts ramping 2 ms after Buck 2 has started ramping.

To enter the sleep sequence:

1. Buck 3 → PSML
2. 2-ms delay
3. Buck 2 → Disabled
4. 2-ms delay
5. Buck 1 → Disabled

An internal 22-kΩ pulldown resistor (±30%) is attached to the FB pin of Buck 1 and Buck 2. Buck 1 and 2 outputs are pulled to ground level when they are disabled to discharge any residual charge present in the output circuitry. When Sleep transitions to a low, Buck 1 is again enabled followed by Buck 2. Buck 3 goes back to its previous state.

When waking up from sleep mode, the sequence is:

1. Buck 1 → Previous state
2. 2-ms delay
3. Buck 2 and Buck 3 transition together → Previous state

7.4.4.2 DevSLP Programming Through SPI

There is no bit which has the same function as DevSLP pin. There is only one requirement programming LM10504 into DevSLP mode through SPI. Setting LDO sleep mode bit high must be the last move when entering DevSLP mode and programming the bit low when waking from DevSLP mode must be the first move. Disabling or programming the Bucks to new level is the user's decision based on power consumption and other requirements.

Device Functional Modes (continued)

The following section describes how to program the chip into sleep mode corresponding to DevSLP pin function. To program the LM10504 to sleep mode through SPI, Buck 1 and Buck 2 must be disabled by host device (Register 0x0A bit 1 and 0). Buck 3 must be programmed to desired level using Register 0x00. After Buck 3 has finished ramping, LDO sleep mode bit must be set high (Register 0x0E bit 1). To wake LM10504 from sleep mode, LDO sleep mode bit must be set low (Register 0x0E bit 1). Buck 1 and 2 must be enabled. Buck 3 voltage must be programmed to previous output level.

7.4.4.3 DevSLP Operational Constraints

In sleep mode the device is in a low power mode. All internal clocks are turned off to conserve power and Buck 3 only operates in PFM mode. While limited to PFM mode the loading on Buck 3 must be kept below 80 mA (typical) to remain below the PFM/PWM threshold and avoid device shutdown. The device loading must be lowered accordingly before entering sleep mode through DevSLP.

7.4.5 Vselect_B2, Vselect_B3 Function

The Vselect_B2/3 pins are digital pins which control alternate voltage selections of Buck 2 and Buck 3, respectively. Vselect_B2 has an internal pulldown which defaults to a 1.8-V output voltage selection for Buck 2. Alternatively, if Vselect_B2 is driven high, an output voltage of 3 V is selected. Vselect_B3 has an internal pullup which defaults to a 1.2-V output voltage selection for Buck 3. Alternatively, if Vselect_B3 is driven low, an output voltage of 1 V is selected. The pullup resistor is connected to the main input voltage. Transitions of the pins does not affect the output voltage, the state is only checked during start-up.

7.4.6 Undervoltage Lockout (UVLO)

The V_{IN} voltage is monitored for a supply under voltage condition, for which the operation of the device can not be ensured. The part automatically disables Buck 3. To prevent unstable operation, the undervoltage lockout (UVLO) has a hysteresis window of about 300 mV. An UVLO forces the device into the reset state, all internal registers are reset. Once the supply voltage is above the UVLO hysteresis, the device initiates a power-up sequence and then enter the active state.

Buck 1 and Buck 2 remain in bypass mode after V_{IN} passes the UVLO until V_{IN} reaches approximately 1.9 V. When Buck 2 is set to 1.8 V, the voltage jumps from 1.8 V to $V_{UVLO\_FALLING}$, and then follow V_{IN}.

The LDO and the comparator remains functional past the UVLO threshold until V_{IN} reaches approximately 2.25 V.

7.4.7 Overvoltage Lockout (OVLO)

The V_{IN} voltage is monitored for a supply overvoltage condition, for which the operation of the device cannot be ensured. The purpose of overvoltage lockout (OVLO) is to protect the part and all other consumers connected to the PMU outputs from any damage and malfunction. Once V_{IN} rises over 5.64 V all the Bucks, and LDO is disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window of about 100 mV. An OVLO forces the device into the reset state; all internal registers are reset. Once the supply voltage is below the OVLO hysteresis, the device initiates a power-up sequence, and then enter the active state. Operating maximum input voltage at which parameters are ensured is 5.5 V. Absolute maximum of the device is 6 V.

7.4.8 Device Status, Interrupt Enable

The LM10504 has 2 interrupt registers, INTERRUPT ENABLE and INTERRUPT STATUS. These registers can be read through the serial interface. The interrupts are not latched to the register, always represents the current state, and does not clear on read.

If interrupt condition is detected, then corresponding bit in the INTERRUPT STATUS register (0x0D) is set to '1', and Interrupt output is asserted. There are 5 interrupt generating conditions:

- Buck 3 output is over flag level (90% when rising, 85% when falling)
- Buck 2 output is over flag level (90% when rising, 85% when falling)
- Buck 1 output is over flag level (90% when rising, 85% when falling)
- LDO is over flag level (90% when rising, 85% when falling
- Comparator input voltage crosses over selected threshold

Device Functional Modes (continued)

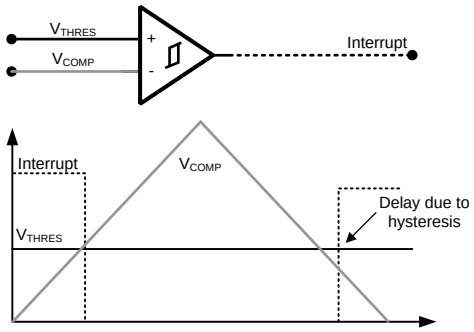
Reading the interrupt register does not release interrupt output. Interrupt generation conditions can be individually enabled or disabled by writing respective bits in INTERRUPT ENABLE register (0x0C) to *1* or *0*.

7.4.9 Thermal Shutdown (TSD)

The temperature of the silicon die is monitored for an overtemperature condition, for which the operation of the device can not be ensured. The part is automatically disabled if the temperature is too high (>140°C). The thermal shutdown (TSD) forces the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device initiates a power-up sequence and then enter the active state. In the active state, the part starts up as if for the first time, all registers are in their default state.

7.4.10 Comparator

The comparator on the LM10504 takes its inputs from the VCOMP pin and an internal threshold level which is programmed by the user. The threshold level is programmable between 2 and 4 V with a step of 31 mV and a default comp code of 0x19. The output of the comparator is the Interrupt pin. Its polarity can be changed using Register 0x0E bit 0. If Interrupt_polarity = 0 → Active low (default) is selected, then the output is low if V_{COMP} value is greater than the threshold level. The output is high if the V_{COMP} value is less than the threshold level. If Interrupt_polarity = 1 → Active high is selected then the output is high if V_{COMP} value is greater than the threshold level. The output is low if the V_{COMP} value is less than the threshold level. There is some hysteresis when V_{COMP} transitions from high to low, typically 60 mV. There is a control bit in register 0x0B, comparator control, that can double the hysteresis value.



7.5 Programming

The device is programmable through 4-wire SPI Interface. The signals associated with this interface are CS, DI, DO and CLK. Through this interface, the user can enable or disable the device, program the output voltages of the individual Bucks, and of course read the status of Flag registers.

By accessing the registers in the device through this interface, the user can access and control the operation of the buck controllers and program the reference voltage of the comparator in the device.

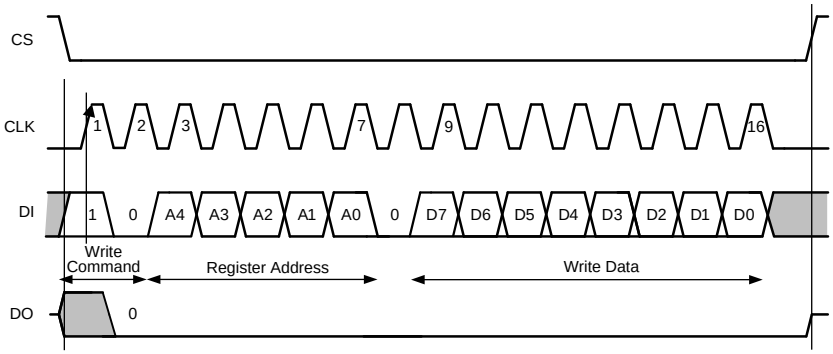


Figure 23. SPI Interface Write

Programming (continued)

- Data In (DI)
  - 1 to 0 Write Command
  - $A_4$to A_0 Register address to be written
  - D_7 to D_0 Data to be written
- Data Out (DO)
  - All Os

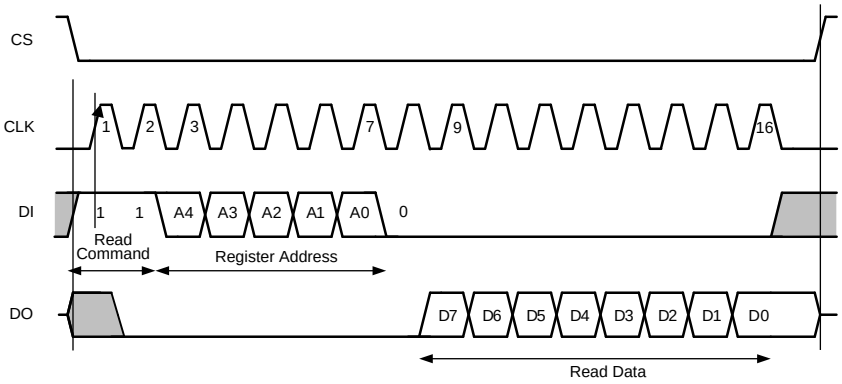


Figure 24. SPI Interface Read

- Data In (DI)
  - 1 to 1 Read Command
  - $A_4$to A_0 Register address to be read
- Data Out (DO)
  - D_7 to D_0 Data Read
- Data In (DI)
  - Don't Care after A0

7.6 Register Maps

Table 1. Registers Configurable Through SPI Interface

ADDR	REG NAME	BIT	R/W	DEFAULT	DESCRIPTION	NOTES
0x00	Buck 3 voltage	7	—	See Table 3		Reset default:
		6	R/W		Buck 3 Voltage Code[6]	Vselect_B3 = 1 → 0x64 (1.2 V)
		5	R/W		Buck 3 Voltage Code[5]	Vselect_B3 = 0 → 0x3C (1 V)
		4	R/W		Buck 3 Voltage Code[4]	
		3	R/W		Buck 3 Voltage Code[3]	Range: 0.7 V to 1.335 V
		2	R/W		Buck 3 Voltage Code[2]	
		1	R/W		Buck 3 Voltage Code[1]	
		0	R/W		Buck 3 Voltage Code[0]	
0x07	Buck 1 voltage	7	—	See Table 2		Reset default:
		6	—			0x26 (3 V)
		5	R/W		Buck 1 Voltage Code[5]	
		4	R/W		Buck 1 Voltage Code[4]	Range: 1.1 V to 3.6 V
		3	R/W		Buck 1 Voltage Code[3]	
		2	R/W		Buck 1 Voltage Code[2]	
		1	R/W		Buck 1 Voltage Code[1]	
		0	R/W		Buck 1 Voltage Code[0]	

Register Maps (continued)

Table 1. Registers Configurable Through SPI Interface (continued)

ADDR	REG NAME	BIT	R/W	DEFAULT	DESCRIPTION	NOTES
0x08	Buck 2 voltage	7	—	See Table 2		Reset default:
		6	—			Vselect_B2 = 1 → 0x26 (3 V)
		5	R/W		Buck 2 Voltage Code[5]	Vselect_B2 = 0 → 0x0E (1.8 V)
		4	R/W		Buck 2 Voltage Code[4]	
		3	R/W		Buck 2 Voltage Code[3]	Range: 1.1 V to 3.6 V
		2	R/W		Buck 2 Voltage Code[2]	
		1	R/W		Buck 2 Voltage Code[1]	
		0	R/W		Buck 2 Voltage Code[0]	
0x09	DevSLP mode for Buck 3	7	R/W	See Table 3		Reset default:
		6			Buck 3 Voltage Code[6]	Vselect_B3 = 1 → 0x53 (1.115 V)
		5			Buck 3 Voltage Code[5]	Vselect_B3 = 0 → 0x0E (0.93 V)
		4			Buck 3 Voltage Code[4]	
		3			Buck 3 Voltage Code[3]	
		2			Buck 3 Voltage Code[2]	
		1			Buck 3 Voltage Code[1]	
		0			Buck 3 Voltage Code[0]	
0x0A	Buck control	7	R	1	BK3EN	Reads Buck 3 enable status
		6	—			
		5	—			
		4	R/W	0	BK1FPWM	Buck 1 forced PWM mode when high
		3	R/W	0	BK2FPWM	Buck 2 forced PWM mode when high
		2	R/W	0	BK3FPWM	Buck 3 forced PWM mode when high
		1	R/W	1	BK1EN	Enables Buck 1 0-disabled, 1-enabled
		0	R/W	1	BK2EN	Enables Buck 2 0-disabled, 1-enabled
0x0B	Comparator control (see Table 4)	7	R/W	0	Comp_hyst[0]	Doubles Comparator hysteresis
		6	R/W	0	Comp_thres[5]	Programmable range of 2 V to 4 V, step size = 31.75 mV
		5	R/W	1	Comp_thres[4]	Comparator Threshold reset default: 0x19
		4	R/W	1	Comp_thres[3]	
		3	R/W	0	Comp_thres[2]	Comp_hyst = 1 → min 80 mV hysteresis
		2	R/W	0	Comp_thres[1]	Comp_hyst = 0 → min 40 mV hysteresis
		1	R/W	1	Comp_thres[0]	
		0	R/W	1	COMPEN	Comparator enable
0x0C	Interrupt enable	7	—			
		6	—			
		5	—			
		4	R/W	0	LDO OK	
		3	R/W	0	Buck 3 OK	
		2	R/W	0	Buck 2 OK	
		1	R/W	0	Buck 1 OK	
		0	R/W	1	Comparator	Interrupt comp event

Register Maps (continued)

Table 1. Registers Configurable Through SPI Interface (continued)

ADDR	REG NAME	BIT	R/W	DEFAULT	DESCRIPTION	NOTES
0x0D	Interrupt status	7	—			
		6	—			
		5	—			
		4	R		LDO OK	LDO is greater than 90% of target
		3	R		Buck 3 OK	Buck 3 is greater than 90% of target
		2	R		Buck 2 OK	Buck 2 is greater than 90% of target
		1	R		Buck 1 OK	Buck 1 is greater than 90% of target
		0	R		Comparator	Comparator output is high
0x0E	MISC control	7	—			
		6	—			
		5	—			
		4	—			
		3	—			
		2	—			
		1	R/W	0	LDO sleep mode	LDO goes into extra power save mode
		0	R/W	0	Interrupt Polarity	Interrupt_polarity= 0 → Active low Interrupt Interrupt_polarity= 1 → Active high Interrupt

Table 2. ADDR 0x07 and 0x08 – Buck 1 and Buck 2 Voltage Code and V_{OUT} Level Mapping

VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE
0x00	1.1	0x20	2.7
0x01	1.15	0x21	2.75
0x02	1.2	0x22	2.8
0x03	1.25	0x23	2.85
0x04	1.3	0x24	2.9
0x05	1.35	0x25	2.95
0x06	1.4	0x26	3
0x07	1.45	0x27	3.05
0x08	1.5	0x28	3.1
0x09	1.55	0x29	3.15
0x0A	1.6	0x2A	3.2
0x0B	1.65	0x2B	3.25
0x0C	1.7	0x2C	3.3
0x0D	1.75	0x2D	3.35
0x0E	1.8	0x2E	3.4
0x0F	1.85	0x2F	3.45
0x10	1.9	0x30	3.5
0x11	1.95	0x31	3.55
0x12	2	0x32	3.6
0x13	2.05	0x33	3.6
0x14	2.1	0x34	3.6
0x15	2.15	0x35	3.6
0x16	2.2	0x36	3.6
0x17	2.25	0x37	3.6
0x18	2.3	0x38	3.6
0x19	2.35	0x39	3.6

Table 2. ADDR 0x07 and 0x08 – Buck 1 and Buck 2 Voltage Code and V_{OUT} Level Mapping (continued)

VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE
0x1A	2.4	0x3A	3.6
0x1B	2.45	0x3B	3.6
0x1C	2.5	0x3C	3.6
0x1D	2.55	0x3D	3.6
0x1E	2.6	0x3E	3.6
0x1F	2.65	0x3F	3.6

Table 3. ADDR 0x00 and 0x09 – Buck 3 Voltage Code and V_{OUT} Level Mapping

VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE
0x00	0.7	0x20	0.86	0x40	1.02	0x60	1.18
0x01	0.705	0x21	0.865	0x41	1.025	0x61	1.185
0x02	0.71	0x22	0.87	0x42	1.03	0x62	1.19
0x03	0.715	0x23	0.875	0x43	1.035	0x63	1.195
0x04	0.72	0x24	0.88	0x44	1.04	0x64	1.2
0x05	0.725	0x25	0.885	0x45	1.045	0x65	1.205
0x06	0.73	0x26	0.89	0x46	1.05	0x66	1.21
0x07	0.735	0x27	0.895	0x47	1.055	0x67	1.215
0x08	0.74	0x28	0.9	0x48	1.06	0x68	1.22
0x09	0.745	0x29	0.905	0x49	1.065	0x69	1.225
0x0A	0.75	0x2A	0.91	0x4A	1.07	0x6A	1.23
0x0B	0.755	0x2B	0.915	0x4B	1.075	0x6B	1.235
0x0C	0.76	0x2C	0.92	0x4C	1.08	0x6C	1.24
0x0D	0.765	0x2D	0.925	0x4D	1.085	0x6D	1.245
0x0E	0.77	0x2E	0.93	0x4E	1.09	0x6E	1.25
0x0F	0.775	0x2F	0.935	0x4F	1.095	0x6F	1.255
0x10	0.78	0x30	0.94	0x50	1.1	0x70	1.26
0x11	0.785	0x31	0.945	0x51	1.105	0x71	1.265
0x12	0.79	0x32	0.95	0x52	1.11	0x72	1.27
0x13	0.795	0x33	0.955	0x53	1.115	0x73	1.275
0x14	0.8	0x34	0.96	0x54	1.12	0x74	1.28
0x15	0.805	0x35	0.965	0x55	1.125	0x75	1.285
0x16	0.81	0x36	0.97	0x56	1.13	0x76	1.29
0x17	0.815	0x37	0.975	0x57	1.135	0x77	1.295
0x18	0.82	0x38	0.98	0x58	1.14	0x78	1.3
0x19	0.825	0x39	0.985	0x59	1.145	0x79	1.305
0x1A	0.83	0x3A	0.99	0x5A	1.15	0x7A	1.31
0x1B	0.835	0x3B	0.995	0x5B	1.155	0x7B	1.315
0x1C	0.84	0x3C	1	0x5C	1.16	0x7C	1.32
0x1D	0.845	0x3D	1.005	0x5D	1.165	0x7D	1.325
0x1E	0.85	0x3E	1.01	0x5E	1.17	0x7E	1.33
0x1F	0.855	0x3F	1.015	0x5F	1.175	0x7F	1.335

Table 4. ADDR 0x0B – Comparator Threshold Mapping

VOLTAGE CODE	VOLTAGE	VOLTAGE CODE	VOLTAGE
0x00	2	0x20	3.016
0x01	2.032	0x21	3.048
0x02	2.064	0x22	3.08
0x03	2.095	0x23	3.111
0x04	2.127	0x24	3.143
0x05	2.159	0x25	3.175
0x06	2.191	0x26	3.207
0x07	2.222	0x27	3.238
0x08	2.254	0x28	3.27
0x09	2.286	0x29	3.302
0x0A	2.318	0x2A	3.334
0x0B	2.349	0x2B	3.365
0x0C	2.381	0x2C	3.397
0x0D	2.413	0x2D	3.429
0x0E	2.445	0x2E	3.461
0x0F	2.476	0x2F	3.492
0x10	2.508	0x30	3.524
0x11	2.54	0x31	3.556
0x12	2.572	0x32	3.588
0x13	2.603	0x33	3.619
0x14	2.635	0x34	3.651
0x15	2.667	0x35	3.683
0x16	2.699	0x36	3.715
0x17	2.73	0x37	3.746
0x18	2.762	0x38	3.778
0x19	2.794	0x39	3.81
0x1A	2.826	0x3A	3.842
0x1B	2.857	0x3B	3.873
0x1C	2.889	0x3C	3.905
0x1D	2.921	0x3D	3.937
0x1E	2.953	0x3E	3.969
0x1F	2.984	0x3F	4

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM10504 contains three buck converters and one LDO.

8.2 Typical Application

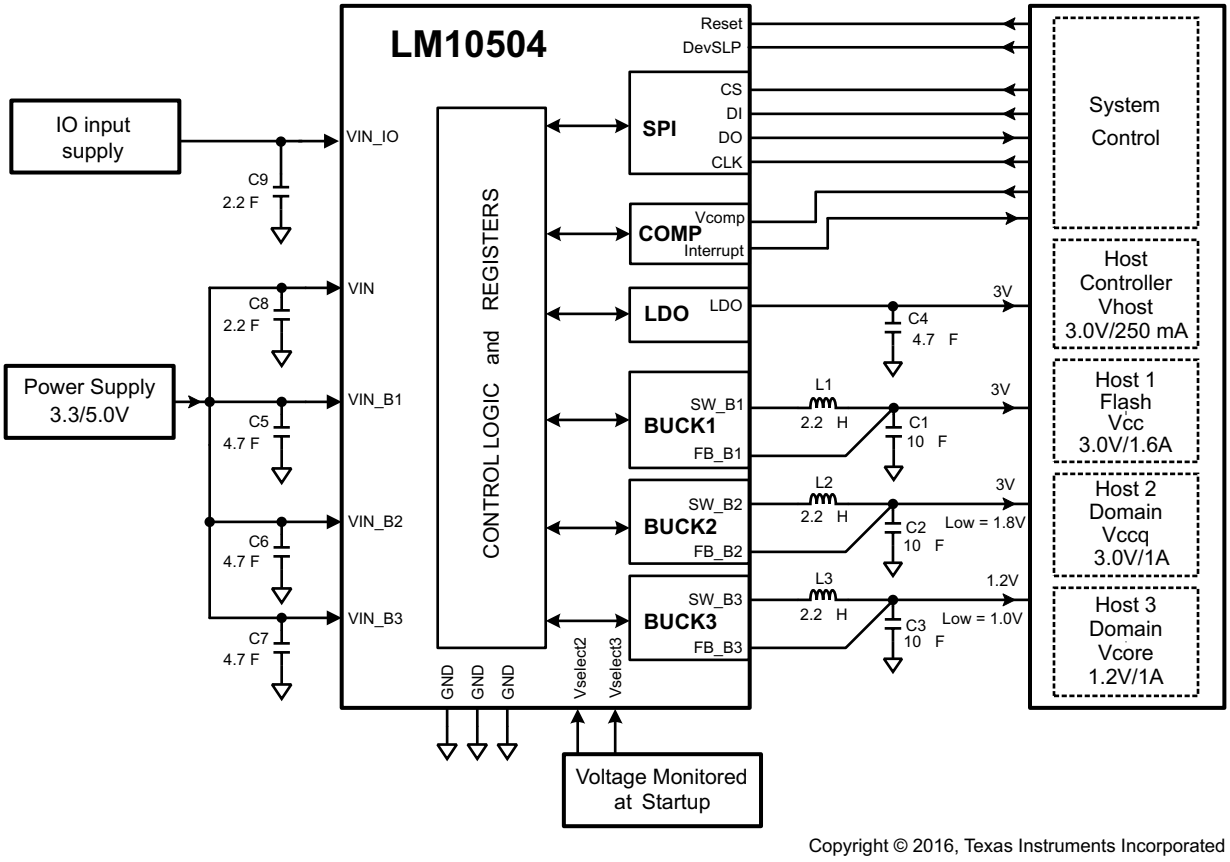


Figure 25. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

Table 5 lists the output characteristics of the power regulators.

Table 5. Output Voltage Configurations for LM10504

REGULATOR	V_{OUT} IF Vselect=HIGH (B2, B3)	V_{OUT} IF Vselect=LOW (B2, B3)	V_{OUT} IF DevSLP=HIGH (DevSLP MODE)	V_{OUT}	MAXIMUM OUTPUT CURRENT	TYPICAL APPLICATION	COMMENTS
Buck 1	3 V	3 V	Off	1.1 V to 3.6, 50 mV steps	1.6 A	V_{CC}	Flash
Buck 2	3 V	1.8 V	Off	1.1 V to 3.6, 50 mV steps	1 A	V_{CCQ}	Interface
Buck 3	1.2 V	1 V	Vnominal –7%	0.7 V to 1.335 V, 5 mV steps	1 A	V_{CORE}	Core
LDO	3 V	3 V	3 V	3 V	250 mA	V_{HOST} controller	Reference for host

8.2.2 Detailed Design Procedure

8.2.2.1 External Components Selection

All three switchers require an input capacitor and an output inductor-capacitor filter. These components are critical to the performance of the device. All three switchers are internally compensated and do not require external components to achieve stable operation. The output voltages of the bucks can be programmed through the SPI pins.

8.2.2.1.1 Output Inductors and Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Overcurrent ruggedness

The device has been optimized for use with nominal LC values as shown in Figure 25.

8.2.2.1.2 Inductor Selection

The recommended inductor values are shown in Figure 25. It is important to ensure the inductor core does not saturate during any foreseeable operational situation. The inductor must be rated to handle the peak load current plus the ripple current in Equation 2.

Care must be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application must be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta I_{RIPPLE}$$
$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} = V_{OUT})}{2 \times L \times F_S}$$
$$\approx I_{LOAD(MAX)} + \frac{D \times (V_{IN} = V_{OUT})}{2 \times 2.2 \times 2.0} \text{ (A typ.)},$$
$$D = \frac{V_{OUT}}{V_{IN}}, F_S = 2\,\text{MHz}, L = 2.2\,\mu\text{H} \quad (2)$$

The two methods of selecting the inductor saturation are in *Recommended Method for Inductor Selection* and *Alternate Method for Inductor Selection*.

8.2.2.1.2.1 Recommended Method for Inductor Selection

The best way to ensure the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in *Electrical Characteristics – General*. In this case, the device prevents inductor saturation by going into current limit before the saturation level is reached.

8.2.2.1.2.2 Alternate Method for Inductor Selection

If the recommended approach cannot be used, care must be taken to ensure that the saturation current is greater than the peak inductor current as calculated in Equation 3.

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

- I_{SAT} is the inductor saturation current at operating temperature
- I_{LPEAK} is the peak inductor current during worst case conditions
- I_{OUTMAX} is the maximum average inductor current
- I_{RIPPLE} is the peak-to-peak inductor current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- L is the inductor value in Henries at I_{OUTMAX}
- F is the switching frequency, Hertz
- D is the estimated duty factor
- EFF is the estimated power supply efficiency (3)

I_{SAT} may not be exceeded during any operation, including transients, start-up, high temperature, worst-case conditions, and so forth.

8.2.2.1.2.2.1 Suggested Inductors and Their Suppliers

The designer must choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, and so forth. In general, smaller physical size inductors have higher series resistance (DCR), and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. The designer must try to find the best compromise between system performance and cost.

Table 6. Recommended Inductors

VALUE	MANUFACTURER	PART NUMBER	DCR	CURRENT	PACKAGE
2.2 µH	Murata	LQH55PN2R2NR0L	31 mΩ	2.5 A	2220
2.2 µH	TDK	NLC565050T-2R2K-PF	60 mΩ	1.3 A	2220
2.2 µH	Murata	LQM2MPN2R2NG0	110 mΩ	1.2 A	806

8.2.2.1.3 Output and Input Capacitors Characteristics

Special attention must be paid when selecting these components. As shown in Figure 26, the DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in Table 7. The graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. TI recommends that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

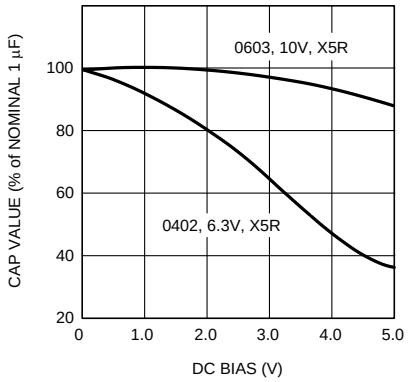


Figure 26. Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to 125°C, only varies the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to 85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 44 µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It must also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −30°C, so some guard band must be allowed.

8.2.2.1.3.1 Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can usually be neglected at the frequency ranges at which the switcher operates.

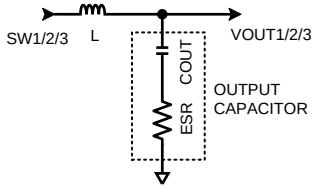


Figure 27. Basic Schematic of Feedback Components

The output-filter capacitor smooths out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR_{COUT}). Also note that the actual value of the capacitor's ESR_{COUT} is frequency and temperature dependent, as specified by its manufacturer. The ESR must be calculated at the applicable switching frequency and ambient temperature with Equation 4.

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \text{ where } \Delta I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \text{ and } D = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor with Equation 5 and Equation 6.

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \sqrt{V^2_{ROUT} + V^2_{COUT}} \quad (5)$$

where

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT} \text{ and } V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \quad (6)$$

- $V_{OUT\text{-}RIPPLE\text{-}PP}$ is the estimated output ripple
- V_{ROUT} is the estimated real output ripple
- V_{COUT} is the estimated reactive output ripple

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22 µF, 6.3 V with an ESR of 2 mΩ or less. The output capacitors need to be mounted as close as possible to the output or ground pins of the device.

Table 7. Recommended Output Capacitors

MODEL	TYPE VENDOR	VENDOR	VOLTAGE RATING	CASE SIZE
08056D226MAT2A	Ceramic, X5R	AVX Corporation	6.3 V	0805, (2012)
C0805L226M9PACTU	Ceramic, X5R	Kemet	6.3 V	0805, (2012)
ECJ-2FB0J226M	Ceramic, X5R	Panasonic - ECG	6.3 V	0805, (2012)
JMK212BJ226MG-T	Ceramic, X5R	Taiyo Yuden	6.3 V	0603, (1608)
C2012X5R0J226M	Ceramic, X5R	TDK Corporation	6.3 V	0603, (1608)

8.2.2.1.3.2 Input Capacitor Selection

There are 3 buck regulators in the LM10504 device. Each of these buck regulators has its own input capacitor which must be located as close as possible to their corresponding SWx_VIN and SWx_GND pins, where x designates Buck 1, 2, or 3. The 3 buck regulators operate at 120° out of phase, which means that they switch on at equally spaced intervals, to reduce the input power rail ripple. TI recommends connecting all the supply and ground pins of the buck regulators, SWx_VIN to two solid internal planes located under the device. In this way, the 3 input capacitors work together and further reduce the input current ripple. A larger tantalum capacitor can also be located in the proximity of the device.

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The input capacitor must be rated to handle this current with Equation 7.

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT}\,(V_{IN} - V_{OUT})}}{V_{IN}} \quad (7)$$

The power dissipated in the input capacitor is given by Equation 8.

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \quad (8)$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10 µF with an ESR of 10 mΩ or less. The input capacitors need to be mounted as close as possible to the power and ground input pins of the device.

The input power source supplies the average current continuously. However, during the PFET switch on-time, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified *worst-case* assumption is that all of the PFET current is supplied by the input capacitor. This results in conservative estimates of input ripple voltage and capacitor RMS current.

Input ripple voltage is estimated with Equation 9.

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times ESR_{CIN}$$

where

- V_{PPIN} is the estimated peak-to-peak input ripple voltage
- I_{OUT} is the output current
- C_{IN} is the input capacitor value
- ESR_{CIN} is the input capacitor ESR (9)

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated with Equation 10.

$$I_{RMSCIN} = \sqrt{D \times \left(I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right)}$$

where

- I_{RMSCIN} is the estimated input capacitor RMS current (10)

8.2.2.2 Recommendations For Unused Functions and Pins

If any function is not used in the end application, see Table 8 for tying off the associated pins on the circuit boards must be used.

Table 8. Unused Pin Recommendations

FUNCTION	PIN	IF UNUSED
BUCK1	VIN_B1	Connect to GND
	SW_B1	Floating
	FB_B1	Connect to GND
BUCK2	VIN_B2	Connect to GND
	SW_B2	Floating
	FB_B2	Connect to GND
BUCK3	VIN_B3	Connect to VIN
	SW_B3	Floating
	FB_B3	Connect to VIN
SPI	SPI_CS	Connect to VIN_IO
	SPI_DI	Connect to GND
	SPI_DO	Connect to GND
	SPI_CK	Connect to GND
Vselect_B2		Connect to GND or leave open
Vselect_B3		Connect to VIN or leave open
DevSLP		Connect to GND or leave open
RESET		Connect to VIN_IO
COMPARATOR	VCOMP	Connect to VIN
	Interrupt	Leave open

8.2.3 Application Curves

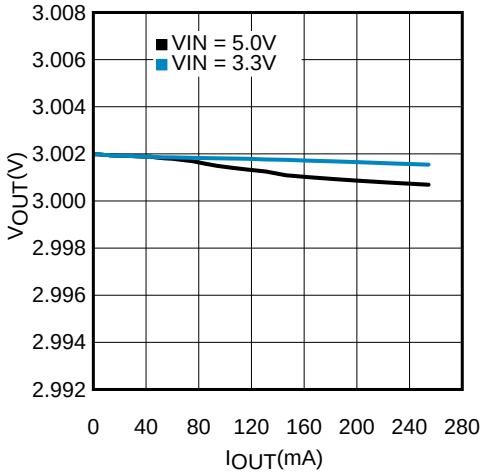


Figure 28. LDO V_{OUT} vs I_{OUT}

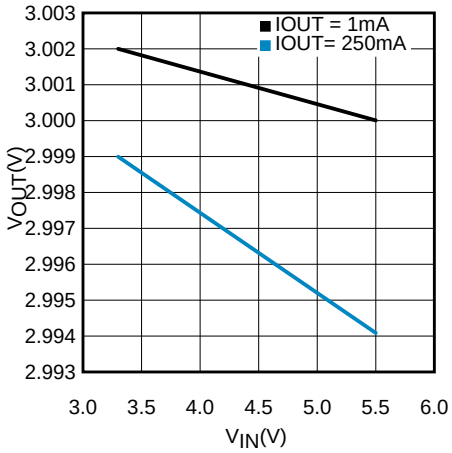


Figure 29. LDO V_{IN} vs V_{OUT}

9 Power Supply Recommendations

The device is designed to operate from a fixed input voltage supply at 3.3 V or 5 V, but is capable of operating at input voltages from 3 V to 5.5 V.

10 Layout

10.1 Layout Guidelines

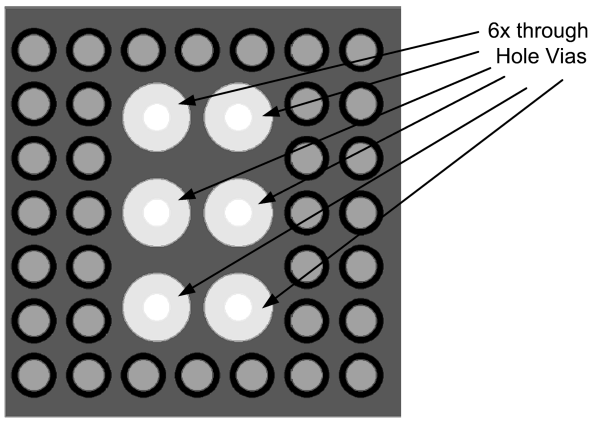
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the C_{IN} input capacitor, to the regulator SWx_VIN pin, to the regulator SW pin, to the inductor then out to the output capacitor $C_{OUT}$and load. The second loop starts from the output capacitor ground, to the regulator SWx_GND pins, to the inductor and then out to C_{OUT} and the load (see Figure 31). To minimize both loop areas, the input capacitor must be placed as close as possible to the VIN pin. Grounding for both the input and output capacitors must consist of a small localized top-side plane that connects to PGND. The inductor must be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW pins must be directly connected with a trace that runs on top-side directly to the inductor. To minimize IR losses this trace must be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils increases the copper area and cause too much capacitive loading on the SW pin. The inductors must be placed as close as possible to the SW pins to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components must be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB pin. The feedback trace must be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so corrects for voltage drops at the load and provide the best output accuracy.

10.1.1 PCB Layout Thermal Dissipation For DSGBA Package

1. Position ground layer as close as possible to DSBGA package. Second PCB layer is usually good option. LM10504 evaluation board is a good example.
2. Draw power traces as wide as possible. Bumps which carry high currents must be connected to wide traces. This helps the silicon to cool down.

10.2 Layout Example



Outside 7×7 array, 0.4-mm DSBGA 34-bump with 24 peripheral and 6 inner vias = 30 individual signals

Figure 30. Possible PCB Layout Configuration

Layout Example (continued)

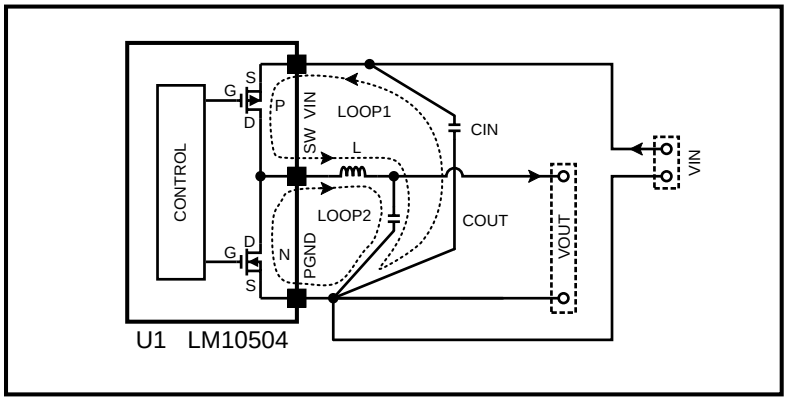


Figure 31. Schematic of LM10504 Highlighting Layout Sensitive Nodes

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10504TME/NOPB	NRND	DSBGA	YFR	34	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 0	V039	
LM10504TMX/NOPB	NRND	DSBGA	YFR	34	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 0	V039	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

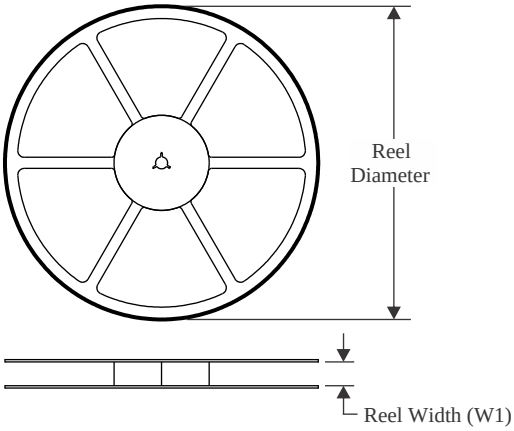
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

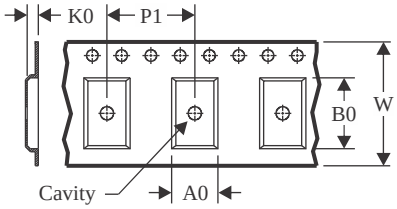
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

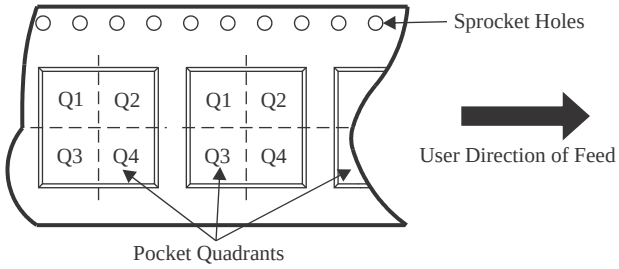


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

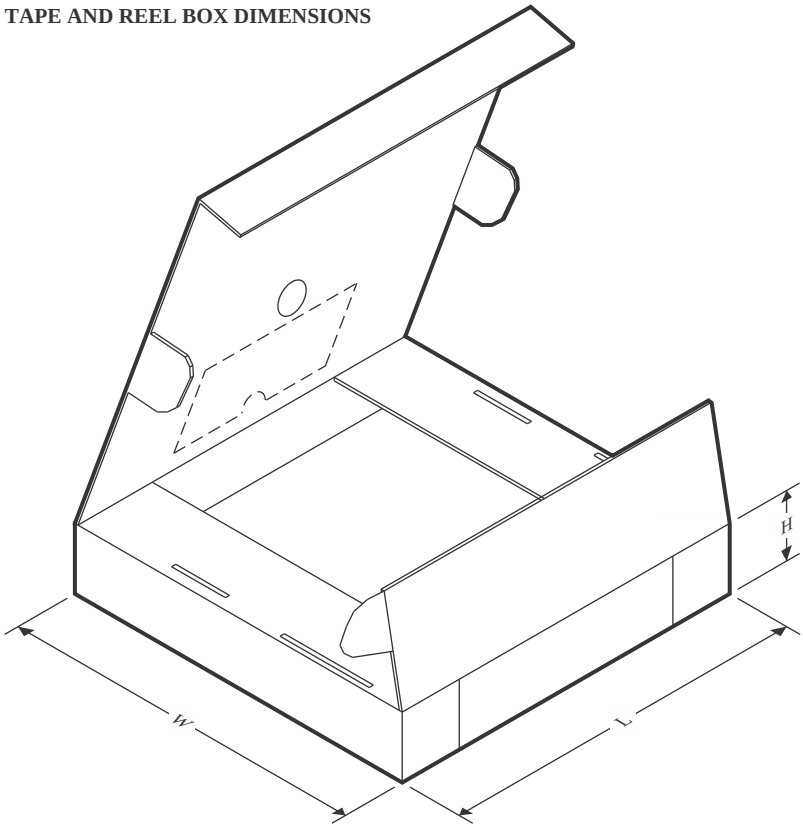
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10504TME/NOPB	DSBGA	YFR	34	250	178.0	8.4	3.02	3.02	0.76	4.0	8.0	Q1
LM10504TMX/NOPB	DSBGA	YFR	34	3000	178.0	8.4	3.02	3.02	0.76	4.0	8.0	Q1

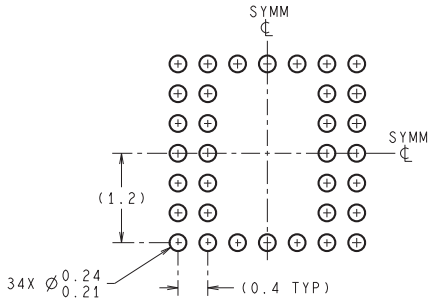
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

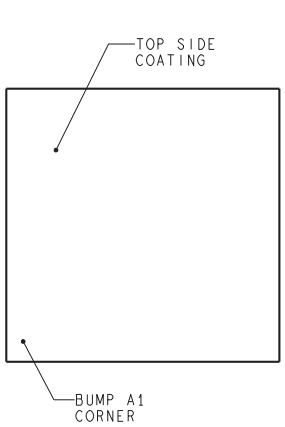
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10504TME/NOPB	DSBGA	YFR	34	250	210.0	185.0	35.0
LM10504TMX/NOPB	DSBGA	YFR	34	3000	210.0	185.0	35.0

YFR0034

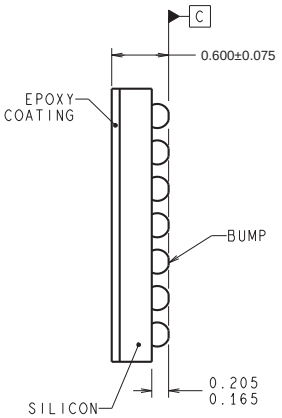


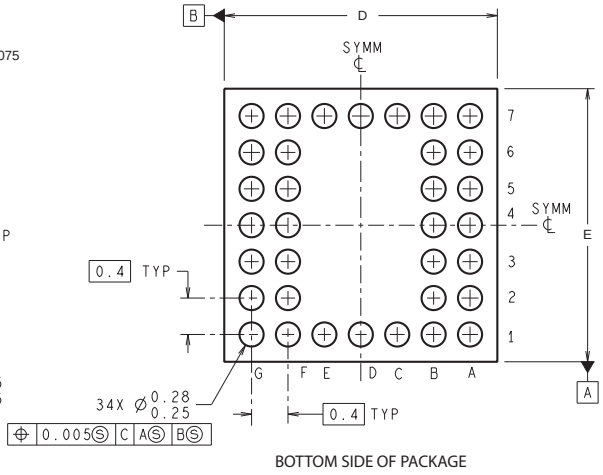
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TOP SIDE OF PACKAGE





BOTTOM SIDE OF PACKAGE

TME34XXX (Rev B)

D: Max = 2.84 mm, Min = 2.78 mm

E: Max = 2.84 mm, Min = 2.78 mm

4215092/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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