LM2705 Micropower昇圧型DC/DCコンバータ、ピーク電流制限150mA

1 特長

- 入力電圧範囲: 2.2V～7V
- 150mA、0.7Ωの内部スイッチ
- 最大20Vの可変出力電圧
- 入力低電圧誤動作防止
- シャットダウン時電流: 0.01µA
- 小型の表面実装部品を使用
- 小型の5ピンSOT-23パッケージ

2 アプリケーション

- LCDバイアス電源
- 白色LEDのバックライト
- ハンドヘルド機器
- デジタル・カメラ
- 携帯用アプリケーション

3 概要

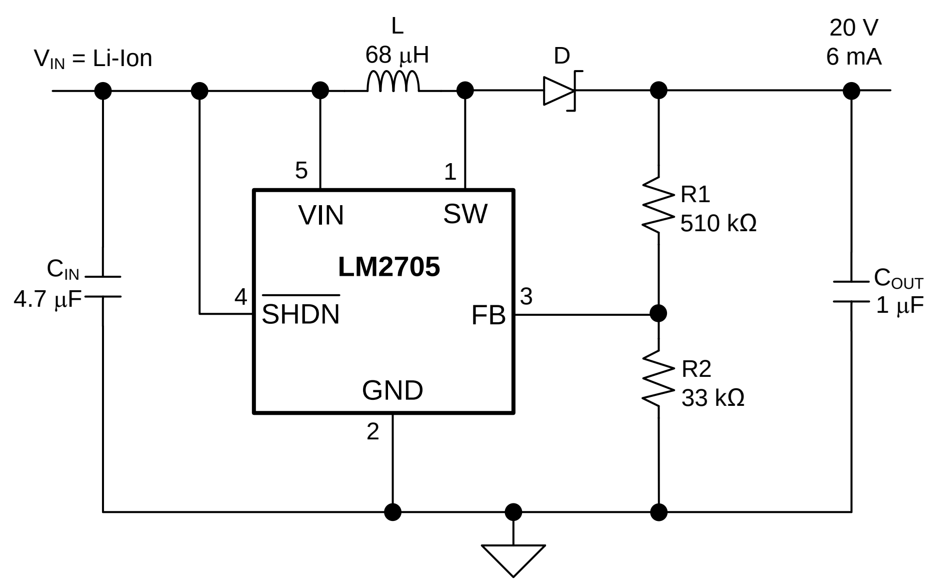
LM2705はMicropower昇圧型DC/DCコンバータで、小型の5ピンSOT-23パッケージで供給されます。電流制限付き、固定オフ時間の制御方式により、動作電流が削減され、広い範囲の負荷条件にわたって高い効率が維持されます。21Vのスイッチにより、最高20Vの電圧を出力できます。オフ時間がわずか400nsであるため、小型で低プロファイルのインダクタやコンデンサを使用でき、容積の限られている携帯用アプリケーションにおいて占有面積とコストを最小化できます。LM2705は、低電流と高効率が要求されるLCDパネルや、携帯電話のバックライトに使用される白色LEDアプリケーションに理想的です。LM2705デバイスは、単一のリチウムイオン・バッテリにより、最大3つの白色LEDを駆動できます。LM2705はピーク・インダクタ電流が低いため、USBアプリケーションに理想的です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM2705	SOT-23 (5)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的な20Vのアプリケーション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (May 2013) から Revision F に変更 — **Page**

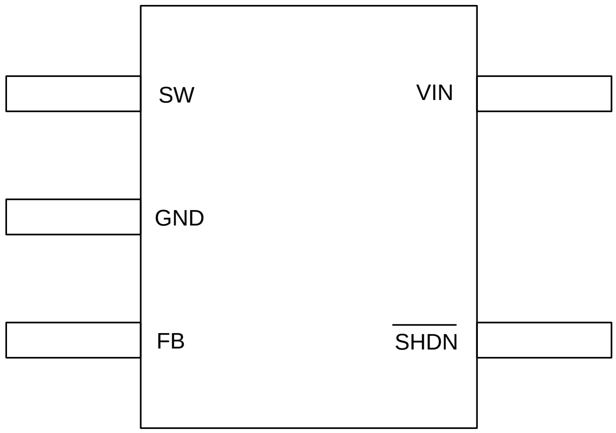
- 「*製品情報*」セクション、「*ピン構成および機能*」セクション、「*ESD定格*」表、「*熱に関する情報*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」のセクション 追加 ... 1
- Deleted pin definition list - added content to *Pin Functions* ... 3
- Changed $R_{\theta JA}$ value from "220°C/W" to "164.9°C/W" ... 4

Revision D (May 2013) から Revision E に変更 — **Page**

- Changed layout of National Semiconductor data sheet to TI format ... 14

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SW	Input	Power switch input. This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.
2	GND	—	Ground - tie directly to ground plane.
3	FB	Input	Output voltage feedback input — set the output voltage by selecting values for R1 and R2 using: $R1 = R2 \times (V_{OUT} / 1.237\ V) - 1$
4	$\overline{SHDN}$	Input	Active low shutdown - drive this pin to > 1.1 V to enable the device. Drive this pin to < 0.3 V to lace the device in a low-power shutdown.
5	VIN	Input	Analog and power input supply pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VIN			7.5	V
SW voltage			21	V
FB voltage			2	V
$\overline{\text{SHDN}}$ voltage			7.5	V
Maximum junction temperature, T_J (3)			150	°C
Lead temperature	Soldering (10 seconds)		300	°C
	Vapor phase (60 seconds)		215	°C
	Infrared (15 seconds)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. See *Thermal Information* for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine model (2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) ESD susceptibility using the machine model is 150 V for SW pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.2		7	V
SW voltage, maximum			20.5	V
Junction temperature (1)	–40		125	°C

(1) All limits specified at room temperature and at *temperature extremes*. All room temperature limits are 100% production tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard statistical quality control (SQC) methods. All limits are used to calculate average outgoing quality level (AOQL).

6.4 Thermal Information

THERMAL METRIC (1)		LM2705 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	116.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Unless otherwise specified, specifications apply for T_J = 25°C and V_{IN} = 2.2 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_Q	Device disabled	FB = 1.3 V		40		µA
		FB = 1.3 V, –40°C to 125°C			70	
	Device enabled	FB = 1.2 V		235		
		FB = 1.2 V, –40°C to 125°C			300	
	Shutdown	$\overline{SHDN}$ = 0 V		0.01	2.5	
V_{FB}	Feedback trip point			1.237		V
		–40°C to 125°C	1.189		1.269	
I_{CL}	Switch current limit			150		mA
		–40°C to 125°C	100		180	
I_B	FB pin bias current	FB = 1.23 V(3)		30		nA
		FB = 1.23 V, –40°C to 125°C(3)			120	
V_{IN}	Input voltage	–40°C to 125°C	2.2		7	V
R_{DSON}	Switch R_{DSON}			0.7		Ω
		–40°C to 125°C			1.6	
T_{OFF}	Switch off time			400		ns
I_{SD}	$\overline{SHDN}$ pin current	$\overline{SHDN}$ = V_{IN}, T_J = 25°C		0	80	nA
		$\overline{SHDN}$ = V_{IN}, T_J = 125°C		15		
		$\overline{SHDN}$ = GND		0		
I_L	Switch leakage current	V_{SW} = 20 V		0.05	5	µA
UVP	Input undervoltage lockout	ON/OFF threshold		1.8		V
V_{FB} hysteresis	Feedback hysteresis			8		mV
$\overline{SHDN}$ threshold	$\overline{SHDN}$ low			0.7		V
		–40°C to 125°C			0.3	
	$\overline{SHDN}$ high			0.7		
		–40°C to 125°C	1.1			

(1) All limits specified at room temperature and at *temperature extremes*. All room temperature limits are 100% production tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard statistical quality control (SQC) methods. all limits are used to calculate average outgoing quality level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Feedback current flows into the pin.

6.6 Typical Characteristics

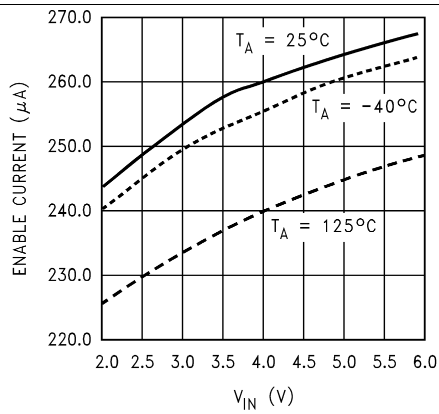


Figure 1. Enable Current vs V_{IN} (Device Switching)

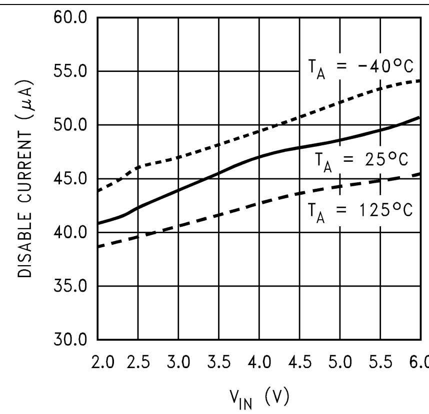


Figure 2. Disable Current vs V_{IN} (Device Not Switching)

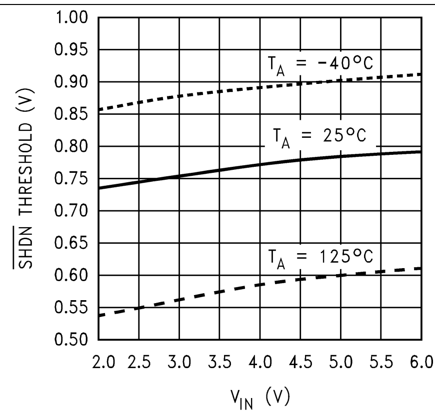


Figure 3. $\overline{SHDN}$ Threshold vs V_{IN}

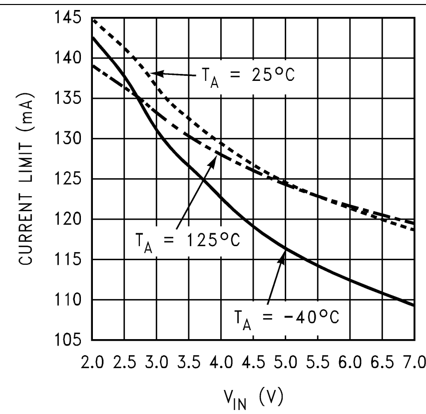


Figure 4. Switch Current Limit vs V_{IN}

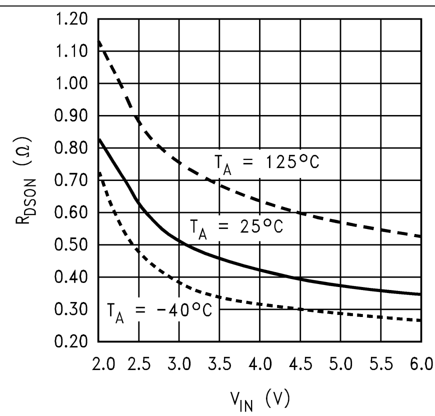


Figure 5. Switch R_{DSON} vs V_{IN}

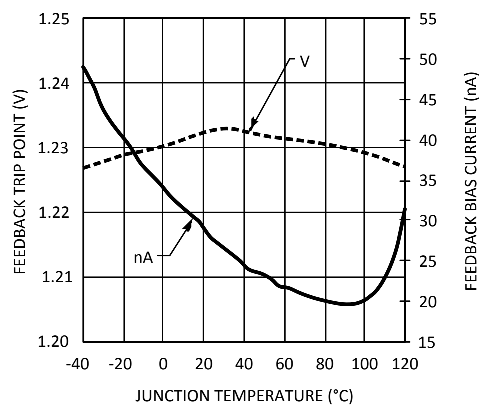


Figure 6. FB Trip Point and FB Pin Current vs Temperature

Typical Characteristics (continued)

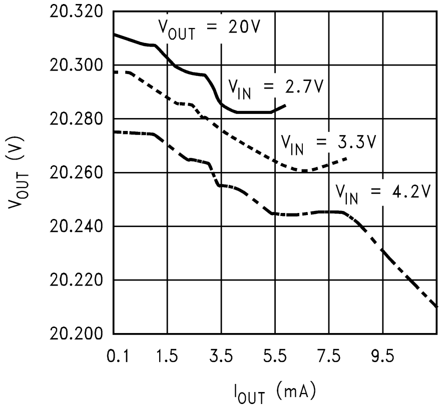


Figure 7. Output Voltage vs Load Current

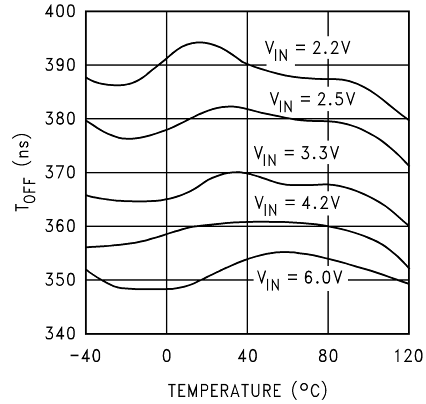
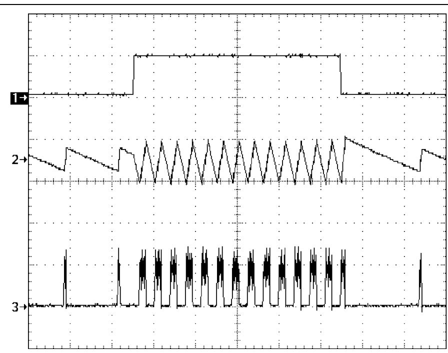
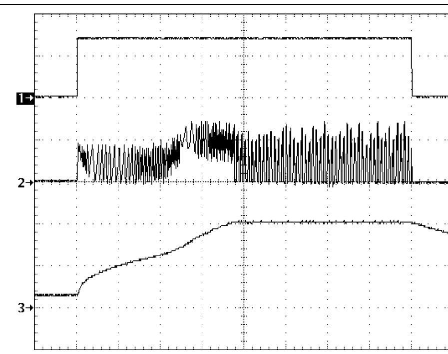


Figure 8. Off Time vs Temperature



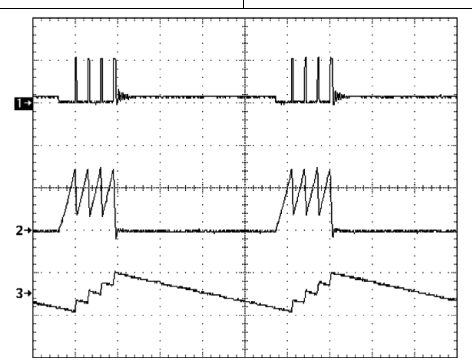
1) Load: 0.5 mA to 5 mA to 0.5 mA, DC V_{OUT} = 20 V
2) V_{OUT}: 200 mV/div, AC V_{IN} = 3 V
3. I_L: 100 mA/div, DC T = 100 µs/div

Figure 9. Step Response



1) SHDN: 1 V/div, DC V_{IN} = 3 V V_{OUT} = 20 V
2) V_{OUT}: 10 V/div, AC T = 100 µs/div R_L = 3.9 kΩ
3. I_L: 100 mA/div, DC

Figure 10. Start-Up and Shutdown



1. V_{SW}: 20 V/div, DC V_{IN} = 2.7 V V_{OUT} = 20 V
2. Inductor Current: 100 mA/div, DC I_{OUT} = 2.5 mA
3. V_{OUT}, 200 mV/div, AC

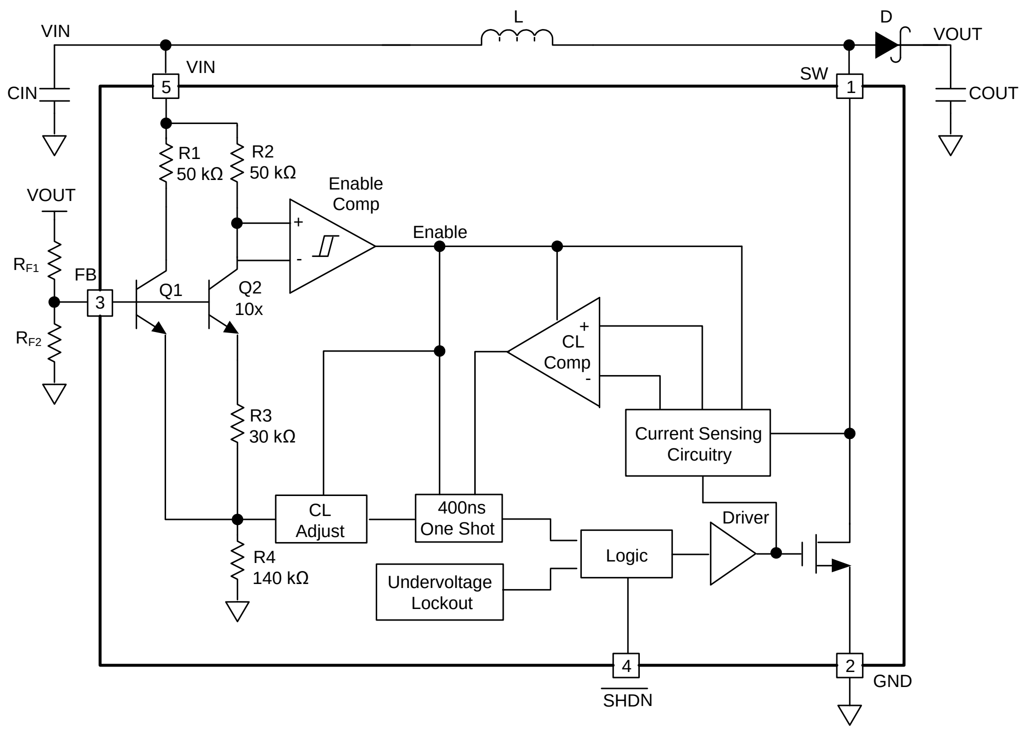
Figure 11. Typical Switching Waveform

7 Detailed Description

7.1 Overview

The LM2705 is a small boost converter utilizing a constant off time architecture. The device can provide up to 20.5 V at the output with up to 150 mA of peak switch current.

7.2 Functional Block Diagram



7.3 Feature Description

The LM2705 device features a constant off-time control scheme. Operation can be best understood by referring to *Functional Block Diagram* and Figure 11. Transistors Q1 and Q2 and resistors R3 and R4 of *Functional Block Diagram* form a bandgap reference used to control the output voltage. When the voltage at the FB pin is less than 1.237 V, the Enable Comp in *Functional Block Diagram* enables the device, and the NMOS switch is turned on pulling the SW pin to ground. When the NMOS switch is on, current begins to flow through inductor L while the load current is supplied by the output capacitor C_{OUT}. Once the current in the inductor reaches the current limit, the CL comp trips, and the 400-ns one shot turns off the NMOS switch.The SW voltage then rises to the output voltage plus a diode drop, and the inductor current begins to decrease as shown in Figure 11. During this time the energy stored in the inductor is transferred to C_{OUT} and the load. After the 400-ns off-time the NMOS switch is turned on, and energy is stored in the inductor again. This energy transfer from the inductor to the output causes a stepping effect in the output ripple as shown in Figure 11.

This cycle is continued until the voltage at FB reaches 1.237 V. When FB reaches this voltage, the Enable Comp disables the device, turning off the NMOS switch and reducing the I_Q of the device to 40 µA. The load current is then supplied solely by C_{OUT} indicated by the gradually decreasing slope at the output as shown in Figure 11. When the FB pin drops slightly below 1.237 V, the Enable Comp enables the device and begins the cycle described previously.

7.4 Device Functional Modes

The $\overline{\text{SHDN}}$ pin can be used to turn off the LM2705 and reduce the I_Q to 0.01 µA. In shutdown mode the output voltage is a diode drop lower than the input voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2705 is a 20-V boost designed for low power boost applications. Typical input voltage range makes this ideal for standard single cell Li+ batteries or 2 to 4 series alkaline batteries.

8.2 Typical Application

Figure 12 shows a typical Li+ voltage range to 20-V application. The 68-µH inductor allows for a low ripple current and high light-load efficiency.

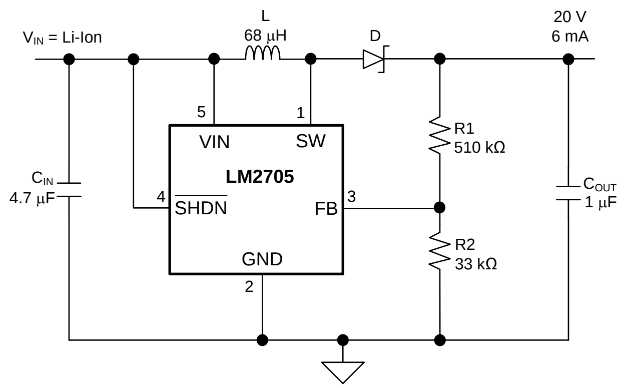


Figure 12. Typical 20-V Application

8.2.1 Design Requirements

For typical DC-DC converter applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 4.2 V
Output voltage	12 V
Output current	up to 8 mA
Inductor	33 µH

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection - Boost Regulator

The appropriate inductor for a given application is calculated using Equation 1:

$$L = \left(\frac{V_{OUT} - V_{IN(min)} + V_D}{I_{CL}}\right) T_{OFF}$$

where

- V_D is the Schottky diode voltage
- I_{CL} is the switch current limit found in the *Typical Characteristics*

- T_{OFF} is the switch off time (1)

When using this equation be sure to use the minimum input voltage for the application, such as for battery powered applications. For the LM2705 constant-off time control scheme, the NMOS power switch is turned off when the current limit is reached. There is approximately a 100-ns delay from the time the current limit is reached in the NMOS power switch and when the internal logic actually turns off the switch. During this 100-ns delay, the peak inductor current increases. This increase in inductor current demands a larger saturation current rating for the inductor. This saturation current can be approximated by Equation 2:

$$I_{PK} = I_{CL} + \left(\frac{V_{IN(max)}}{L}\right) 100\text{ ns} \quad (2)$$

Choosing inductors with low ESR decrease power losses and increase efficiency.

Take care when choosing an inductor. For applications that require an input voltage that approaches the output voltage, such as when converting a Li-Ion battery voltage to 5 V, the 400-ns off time may not be enough time to discharge the energy in the inductor and transfer the energy to the output capacitor and load. This can cause a ramping effect in the inductor current waveform and an increased ripple on the output voltage. Using a smaller inductor causes the I_{PK} to increase and increases the output voltage ripple further.

For typical curves and evaluation purposes the DT1608C series inductors from Coilcraft were used. Other acceptable inductors include, but are not limited to, the SLF6020T series from TDK, the NP05D series from Taiyo Yuden, the CDRH4D18 series from Sumida, and the P1166 series from Pulse.

8.2.2.2 Inductor Selection - SEPIC Regulator

Equation 3 can be used to calculate the approximate inductor value for a SEPIC regulator:

$$L2 = 2\left(\frac{V_{OUT} + V_D}{I_{CL}}\right) T_{OFF} \quad (3)$$

The boost inductor, L1, can be smaller or larger but is generally chosen to be the same value as L2. See Figure 23 and Figure 24 for typical SEPIC applications.

8.2.2.3 Diode Selection

To maintain high efficiency, the average current rating of the Schottky diode should be larger than the peak inductor current, I_{PK}. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the Schottky diode larger than the output voltage.

8.2.2.4 Capacitor Selection

Choose low equivalent series resistance (ESR) capacitors for the output to minimize output voltage ripple. Multilayer ceramic capacitors are the best choice. For most applications, a 1-µF ceramic capacitor is sufficient. For some applications a reduction in output voltage ripple can be achieved by increasing the output capacitor. Output voltage ripple can further be reduced by adding a 4.7-pF feed-forward capacitor in the feedback network placed in parallel with RF1 (see *Functional Block Diagram*).

Local bypassing for the input is needed on the LM2705. Multilayer ceramic capacitors are a good choice for this as well. A 4.7-µF capacitor is sufficient for most applications. For additional bypassing, a 100-nF ceramic capacitor can be used to shunt high frequency ripple on the input.

8.2.3 Application Curves

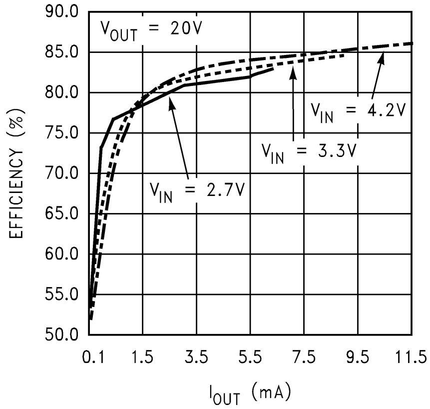


Figure 13. Efficiency vs Load Current

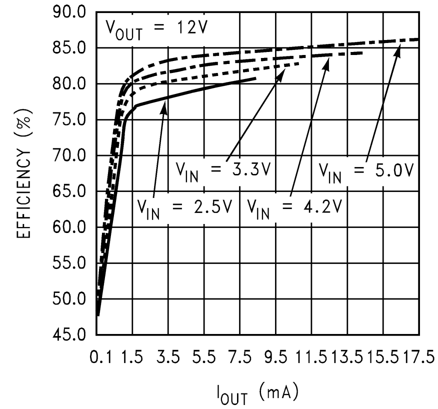


Figure 14. Efficiency vs Load Current

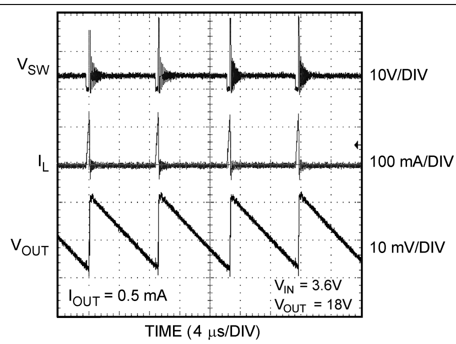


Figure 15. Output Ripple Voltage
Copt, Ropt Included

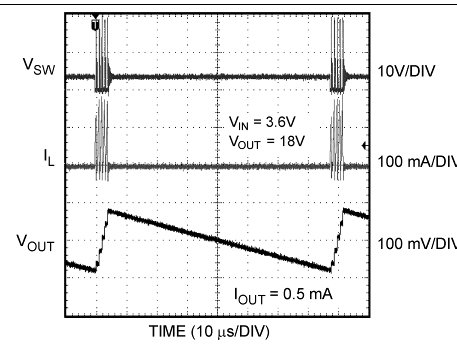


Figure 16. Output Ripple Voltage
Copt, Ropt Excluded

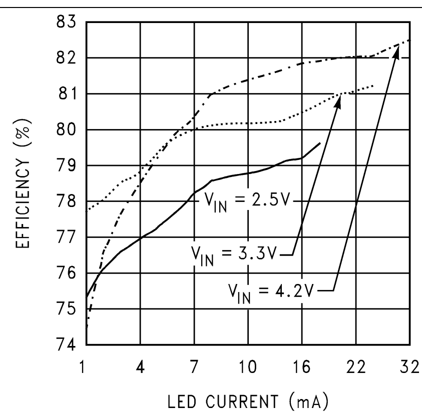


Figure 17. Two White-LED Efficiency

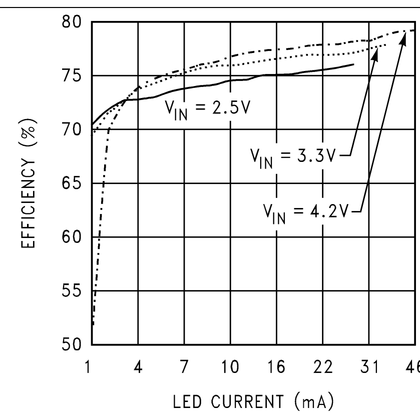


Figure 18. Three White-LED Efficiency

8.3 Additional Applications

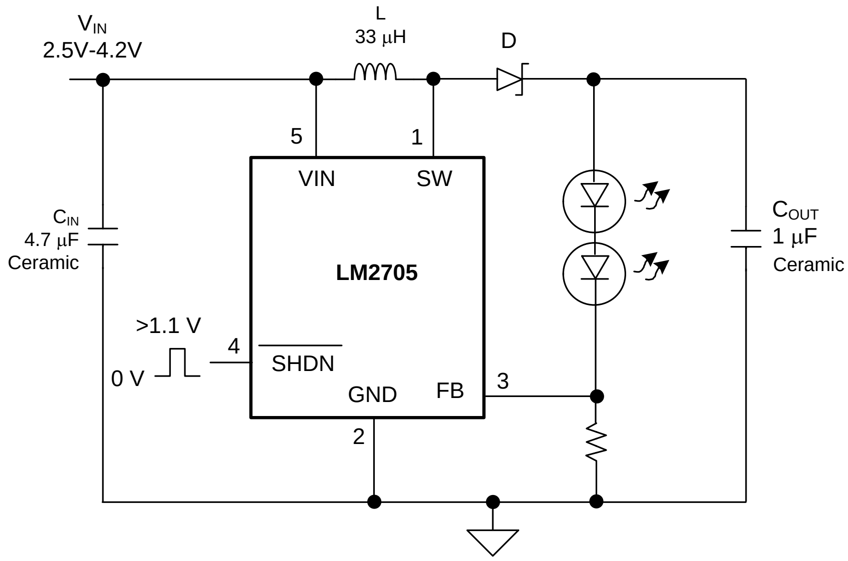


Figure 19. Two White-LED Application

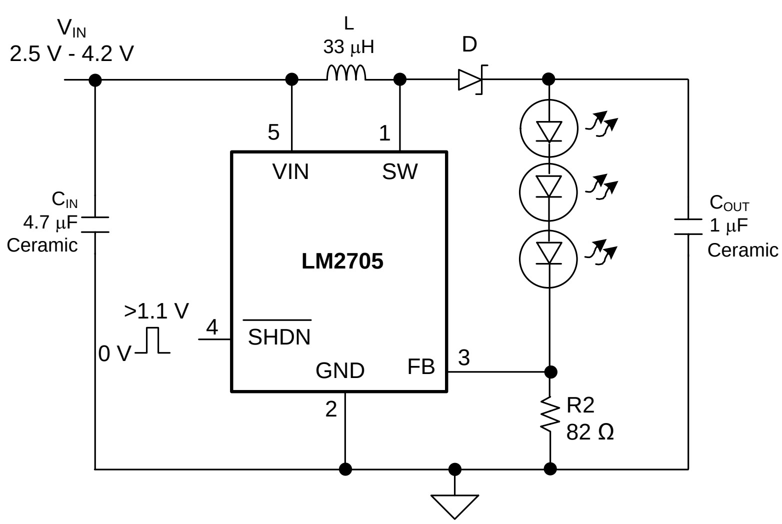


Figure 20. Three White-LED Application

Additional Applications (continued)

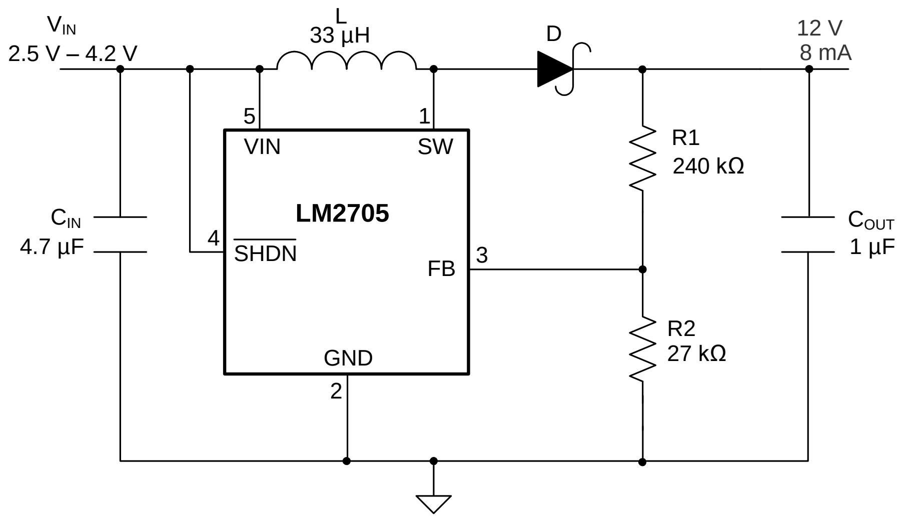


Figure 21. Li-Ion 12-V Application

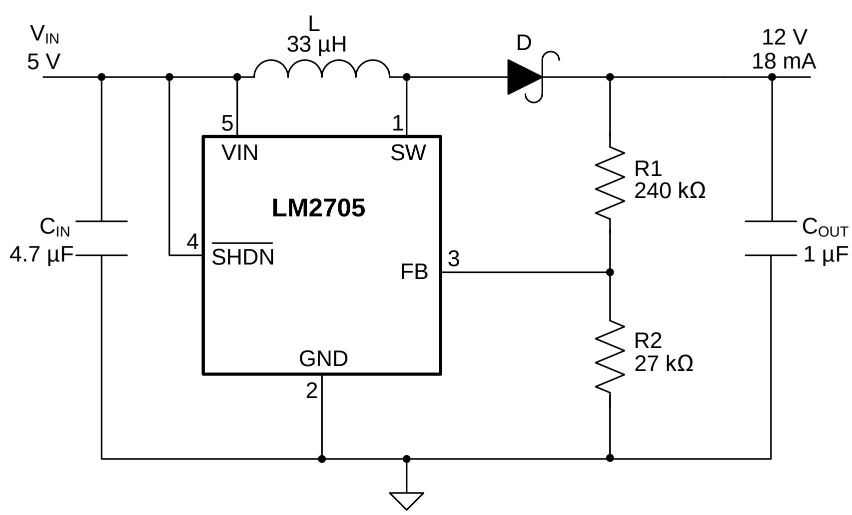


Figure 22. 5-V to 12-V Application

Additional Applications (continued)

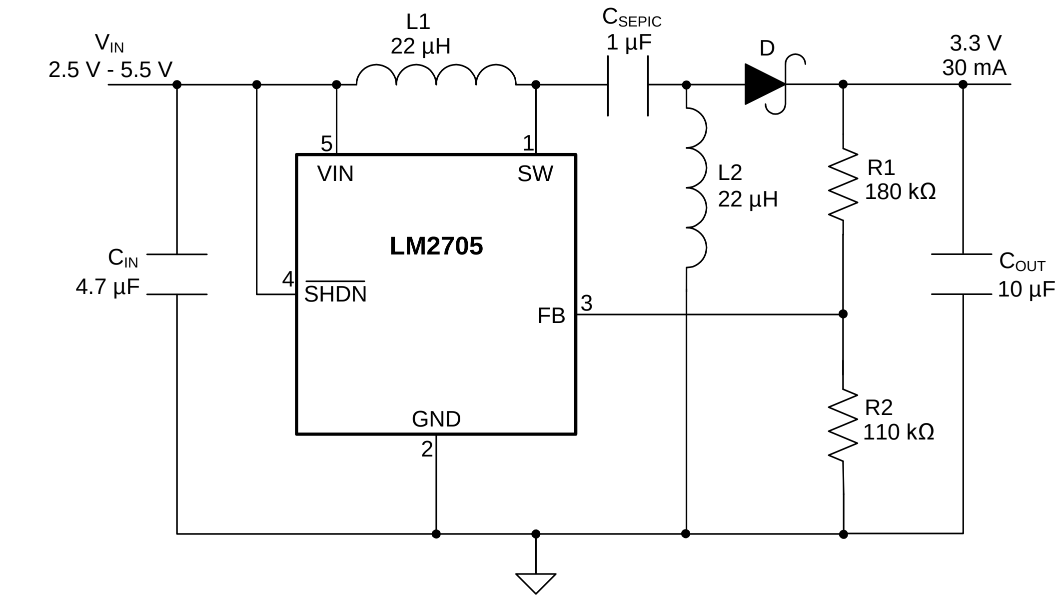


Figure 23. 3.3-V SEPIC Application

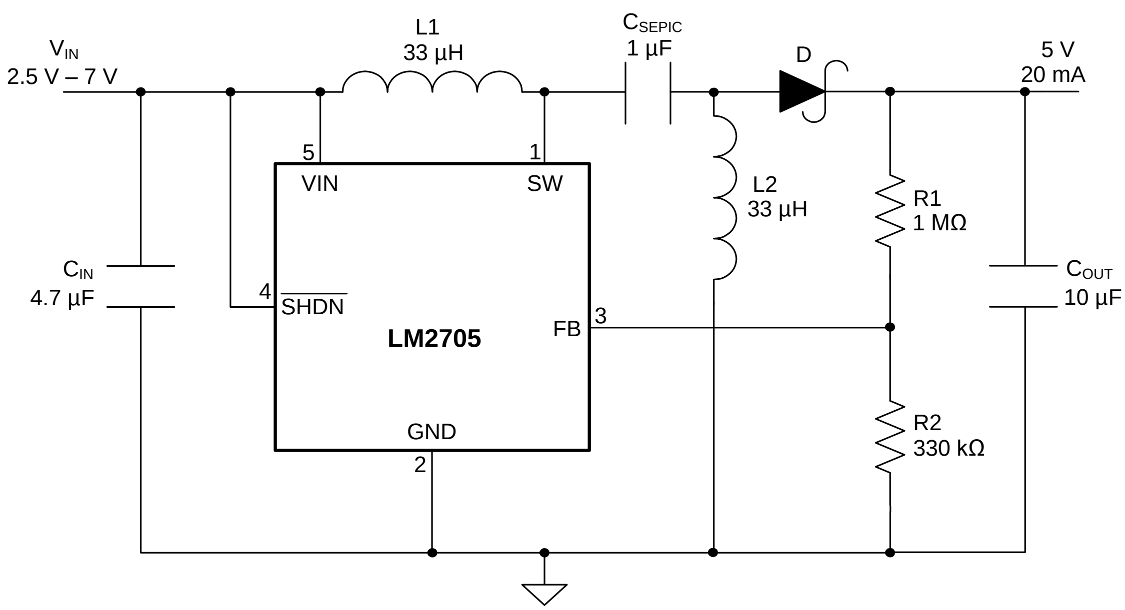


Figure 24. 5-V SEPIC Application

9 Power Supply Recommendations

The LM2705 is designed to operate from an input voltage supply range from 2.2 V to 7 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM2705, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The input bypass capacitor C_{IN}, as shown in Figure 25, must be placed close to the device. This reduces copper trace resistance, which effects input voltage ripple of the LM2705 device. For additional input voltage filtering, a 100-nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, must also be placed close to the device. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. Keep the feedback network, resistors R1 and R2, close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network must connect directly to an analog ground plane. Tie the analog ground plane directly to the GND pin. If no analog ground plane is available, the ground connection for the feedback network must tie directly to the GND pin. Minimize trace connections made to the inductor and Schottky diode to reduce power dissipation and increase overall efficiency.

10.2 Layout Example

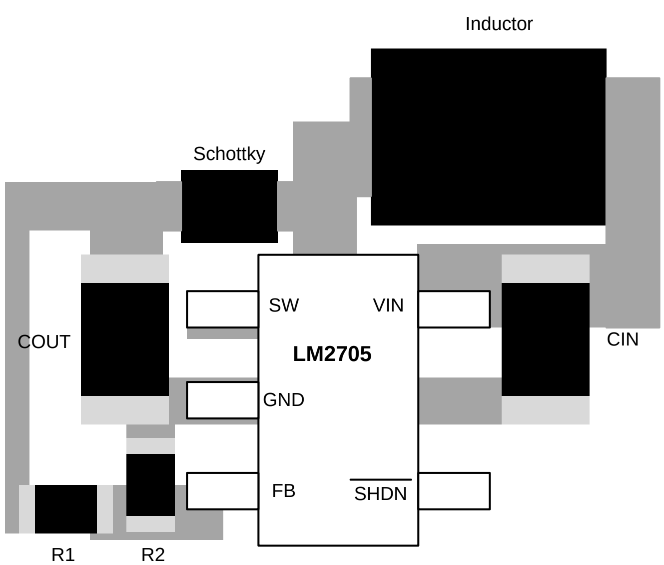


Figure 25. LM2705 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 Third-Party Products Disclaimer

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2705MF-ADJ/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S59B
LM2705MF-ADJ/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	S59B
LM2705MFX-ADJ/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	S59B
LM2705MFX-ADJ/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	S59B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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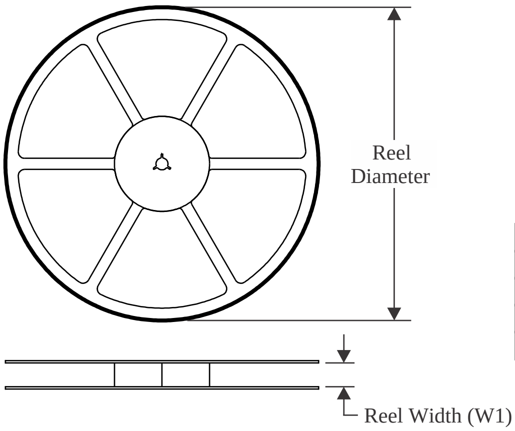
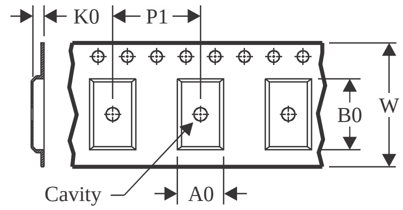
TAPE AND REEL INFORMATION

REEL DIMENSIONS

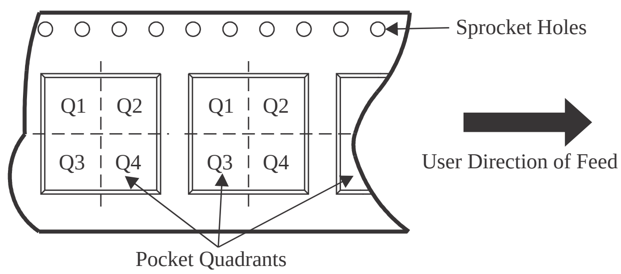


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

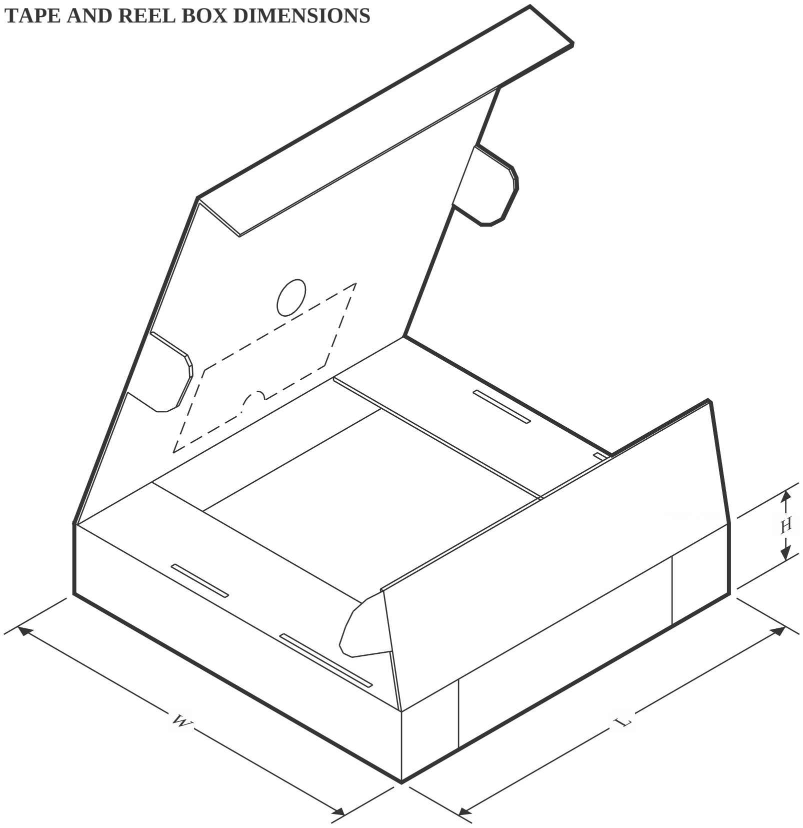
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

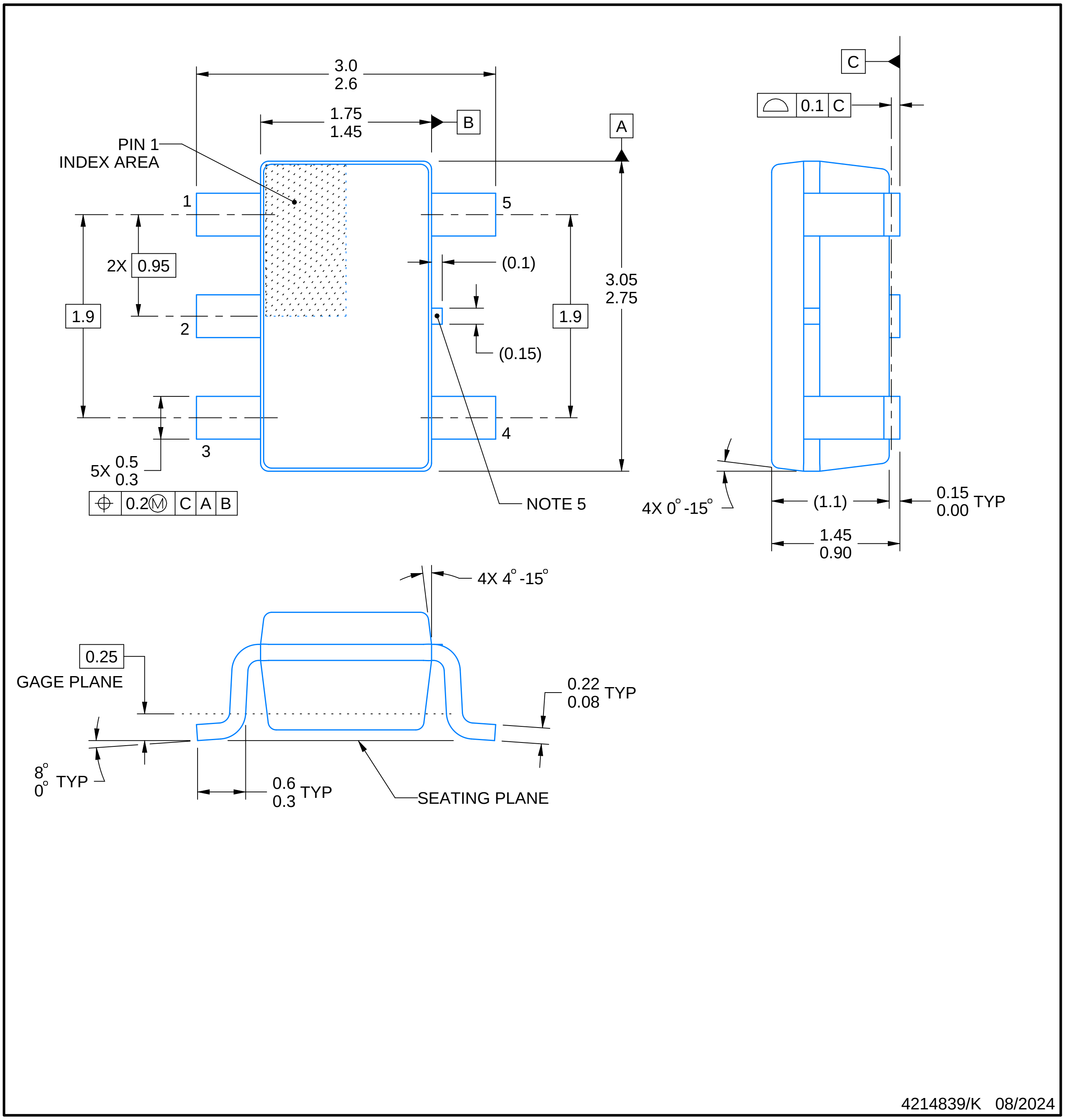
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2705MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2705MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2705MF-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2705MFX-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



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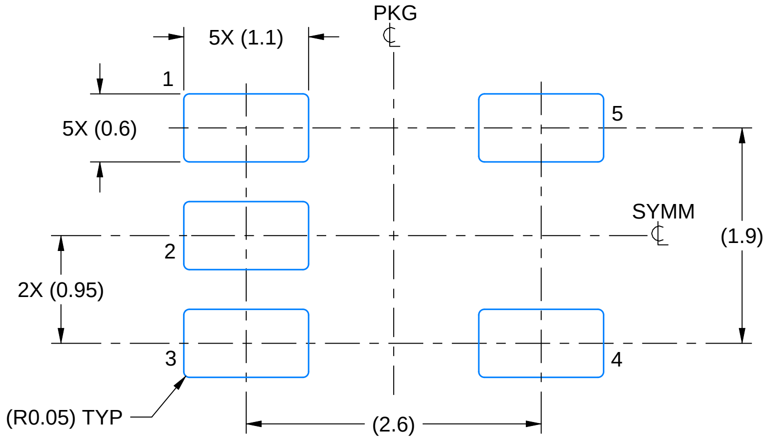
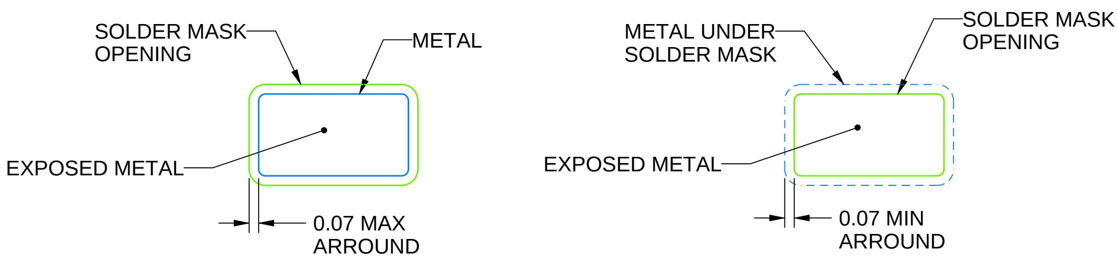
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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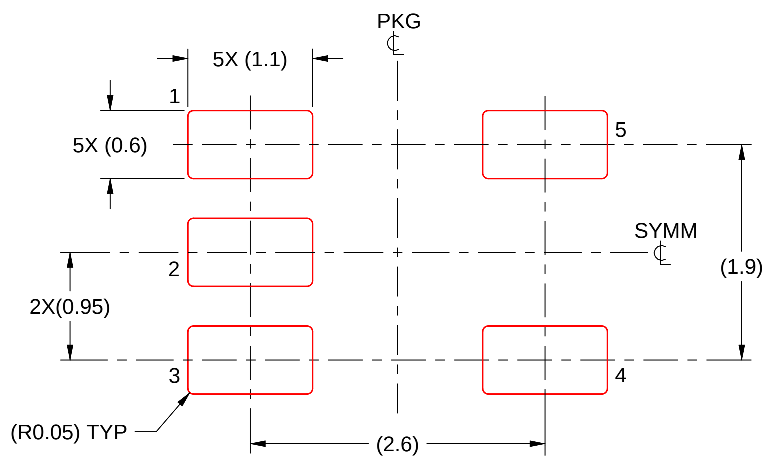
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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