# LM324-MIL クワッド・オペアンプ

## 1 特長

- 広い電源電圧範囲
  - 単一電源: 3V～32V
  - デュアル電源: ±1.5V～±16V
- 電源電圧に影響されない低い電源消費電流: 0.8mA (標準値)
- 同相入力電圧範囲にグランドが含まれるため、グランド近くの直接センシングが可能
- 低い入力バイアスとオフセット・パラメータ
  - 入力オフセット電圧: 3mV (標準値)
  - 入力オフセット電流: 2nA (標準値)
  - 入力バイアス電流: 20nA (標準値)
- 差動入力電圧範囲が最大定格電源電圧と同じ: 32V
- 開ループ差動電圧増幅: 100V/mV (標準値)
- 内部的な周波数補償
- MIL-PRF-38535準拠の製品については、特に記述のない限り、すべてのパラメータはテスト済みです。他のすべての製品については、量産プロセスにすべてのパラメータのテストが含まれているとは限りません。

## 2 アプリケーション

- Blu-Rayプレイヤーおよびホーム・シアター
- 化学およびガス・センサ
- DVDレコーダーおよびプレイヤー
- デジタル・マルチメータ: ベンチおよびシステム
- デジタル・マルチメータ: ハンドヘルド
- フィールド・トランスミッタ: 温度センサ
- モータ制御: AC誘導、ブラシ付きDC、ブラシレスDC、高電圧、低電圧、永久磁石、ステッパー・モータ
- オシロスコープ
- TV: LCDおよびデジタル
- Modbus使用の温度センサまたはコントローラ
- 重量計

## 3 概要

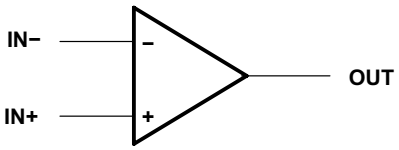
このデバイスは、4つの独立した高ゲインの周波数補償オペアンプで構成され、広い範囲の電圧を持つ単一または分割電源で動作するよう特に設計されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| LM324-MIL | SOIC (14) | 8.65mm×3.91mm |
| | CDIP (14) | 19.56mm×6.67mm |
| | PDIP (14) | 19.30mm×6.35mm |
| | CFP (14) | 9.21mm×5.97mm |
| | TSSOP (14) | 5.00mm×4.40mm |
| | SO (14) | 9.20mm×5.30mm |
| | SSOP (14) | 6.20mm×5.30mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**シンボル(各アンプ)**



# 目次

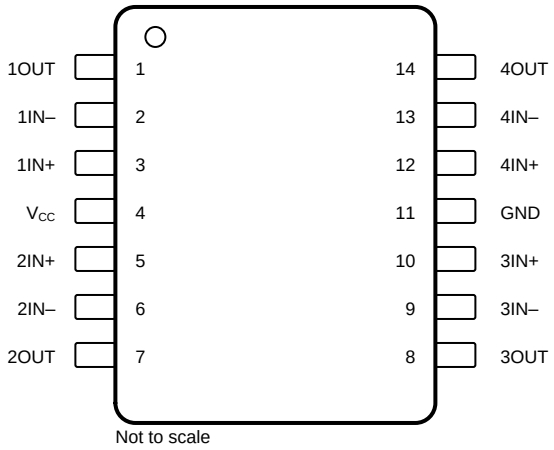


## 4 改訂履歴

| 日付 | 改訂内容 | 注 |
|---|---|---|
| 2017年6月 | * | 初版 |

# 5 Pin Configuration and Functions

**D, DB, J, N, NS, PW, W PACKAGE**
**14-Pin SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP**
**(Top View)**




Not to scale

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1IN– | 2 | I | Negative input |
| 1IN+ | 3 | I | Positive input |
| 1OUT | 1 | O | Output |
| 2IN– | 6 | I | Negative input |
| 2IN+ | 5 | I | Positive input |
| 2OUT | 7 | O | Output |
| 3IN– | 9 | I | Negative input |
| 3IN+ | 10 | I | Positive input |
| 3OUT | 8 | O | Output |
| 4IN– | 13 | I | Negative input |
| 4IN+ | 12 | I | Positive input |
| 4OUT | 14 | O | Output |
| GND | 11 | — | Ground |
| NC | — | — | Do not connect |
| $V_{CC}$ | 4 | — | Power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$(2) | | ±16 | 32 | V |
| Differential input voltage, $V_{ID}$(3) | | | ±32 | V |
| Input voltage, $V_I$ (either input) | | –0.3 | 32 | V |
| Duration of output short circuit (one amplifier) to ground at (or below) $T_A$ = 25°C, $V_{CC}$ ≤ 15 V(4) | | Unlimited | | |
| Operating virtual junction temperature, $T_J$ | | | 150 | °C |
| Case temperature for 60 seconds | FK package | | 260 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and $V_{CC}$ specified for the measurement of $I_{OS}$) are with respect to the network GND.
(3) Differential voltages are at IN+, with respect to IN−.
(4) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 30 | V |
| $V_{CM}$ | Common-mode voltage | 0 | $V_{CC}$ – 2 | V |
| $T_A$ | Operating free air temperature | 0 | 70 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | J (CDIP) | W (CFP) | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$(2)(3) | Junction-to-ambient thermal resistance | 86 | 86 | 80 | 76 | 113 | — | — | °C/W |
| $R_{\theta JC}$(4) | Junction-to-case (top) thermal resistance | — | — | — | — | — | 15.05 | 14.65 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
(3) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/R_{\theta JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(4) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and $T_C$. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_{J(max)} – T_C)/R_{\theta JC}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

## 6.5 Electrical Characteristics

at specified free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | $T_A$(2) | MIN | TYP(3) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = 5 V to MAX, $V_{IC}$ = $V_{ICR}$min, $V_O$ = 1.4 V | | 25°C | | 3 | 7 | mV |
| | | | | Full range | | | 9 | |
| $I_{IO}$ | Input offset current | $V_O$ = 1.4 V | | 25°C | | 2 | 50 | nA |
| | | | | Full range | | | 150 | |
| $I_{IB}$ | Input bias current | $V_O$ = 1.4 V | | 25°C | | –20 | –250 | nA |
| | | | | Full range | | | –500 | |
| $V_{ICR}$ | Common-mode input voltage range | $V_{CC}$ = 5 V to MAX | | 25°C | 0 to $V_{CC}$ – 1.5 | | | V |
| | | | | Full range | 0 to $V_{CC}$ – 2 | | | |
| $V_{OH}$ | High-level output voltage | $R_L$ = 2 kΩ | | 25°C | $V_{CC}$ – 1.5 | | | V |
| | | $R_L$ = 10 kΩ | | 25°C | | | | |
| | | $V_{CC}$ = MAX | $R_L$ = 2 kΩ | Full range | 26 | | | |
| | | | $R_L$ ≥ 10 kΩ | Full range | 27 | 28 | | |
| $V_{OL}$ | Low-level output voltage | $R_L$ ≤ 10 kΩ | | Full range | | 5 | 20 | mV |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{CC}$ = 15 V, $V_O$ = 1 V to 11 V, $R_L$ ≥ 2 kΩ | | 25°C | 25 | 100 | | V/mV |
| | | | | Full range | 15 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min | | 25°C | 65 | 80 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC}$ /ΔVIO) | | | 25°C | 65 | 100 | | dB |
| $V_{O1}$/ $V_{O2}$ | Crosstalk attenuation | f = 1 kHz to 20 kHz | | 25°C | | 120 | | dB |
| $I_O$ | Output current | $V_{CC}$ = 15 V, $V_{ID}$ = 1 V, $V_O$ = 0 | Source | 25°C | –20 | –30 | –60 | mA |
| | | | | Full range | –10 | | | |
| | | $V_{CC}$ = 15 V, $V_{ID}$ = –1 V, $V_O$ = 15 V | Sink | 25°C | 10 | 20 | | |
| | | | | Full range | 5 | | | |
| | | $V_{ID}$ = –1 V, $V_O$ = 200 mV | | 25°C | 12 | 30 | | µA |
| $I_{OS}$ | Short-circuit output current | $V_{CC}$ at 5 V, $V_O$ = 0, GND at –5 V | | 25°C | | ±40 | ±60 | mA |
| $I_{CC}$ | Supply current (four amplifiers) | $V_O$ = 2.5 V, no load | | Full range | | 0.7 | 1.2 | mA |
| | | $V_{CC}$ = MAX, $V_O$ = 0.5 $V_{CC}$, no load | | Full range | | 1.4 | 3 | |

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX $V_{CC}$ for testing purposes is 30 V.
(2) Full range is 0°C to 70°C for LM324-MIL.
(3) All typical values are at $T_A$ = 25°C

## 6.6 Operating Conditions

$V_{CC}$ = ±15 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| SR | Slew rate at unity gain | $R_L$ = 1 MΩ, $C_L$ = 30 pF, $V_I$ = ±10 V (see Figure 7) | 0.5 | V/µs |
| $B_1$ | Unity-gain bandwidth | $R_L$ = 1 MΩ, $C_L$ = 20 pF (see Figure 7) | 1.2 | MHz |
| $V_n$ | Equivalent input noise voltage | $R_S$ = 100 Ω, $V_I$ = 0 V, f = 1 kHz (see Figure 8) | 35 | nV/√Hz |

## 6.7 Typical Characteristics

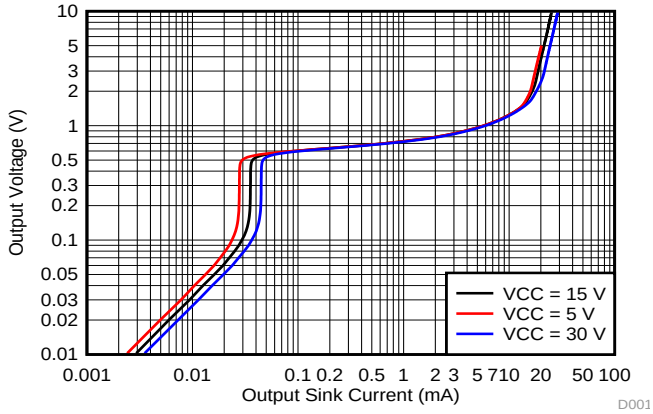



**Figure 1. Output Sinking Characteristics**

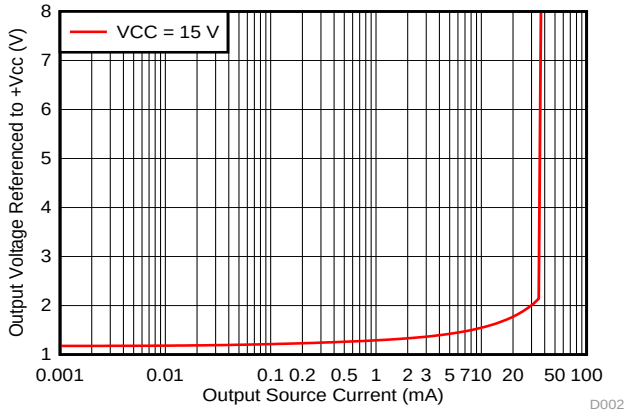



**Figure 2. Output Sourcing Characteristics**

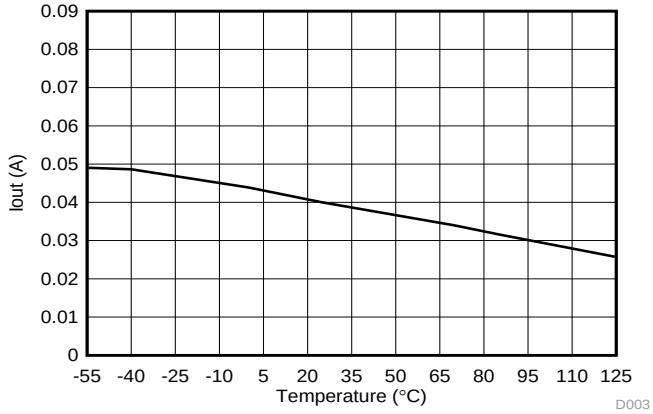



**Figure 3. Source Current Limiting**

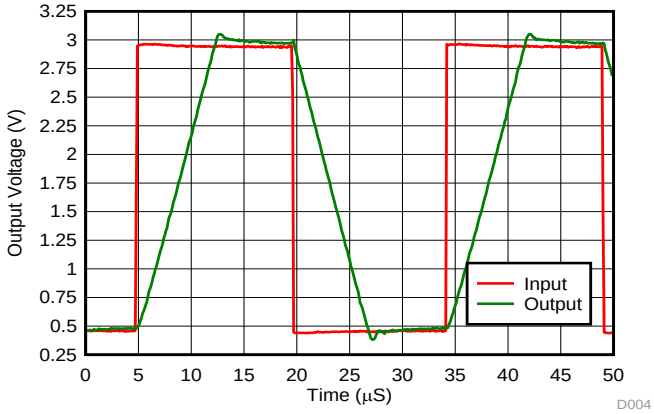



**Figure 4. Voltage Follower Large Signal Response (50 pF)**

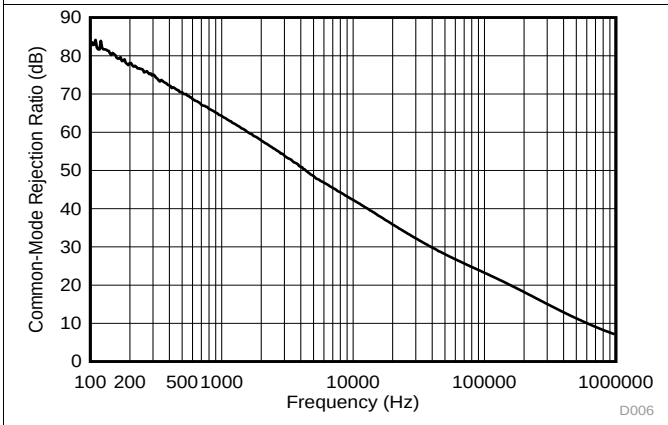



**Figure 5. Common-Mode Rejection Ratio**

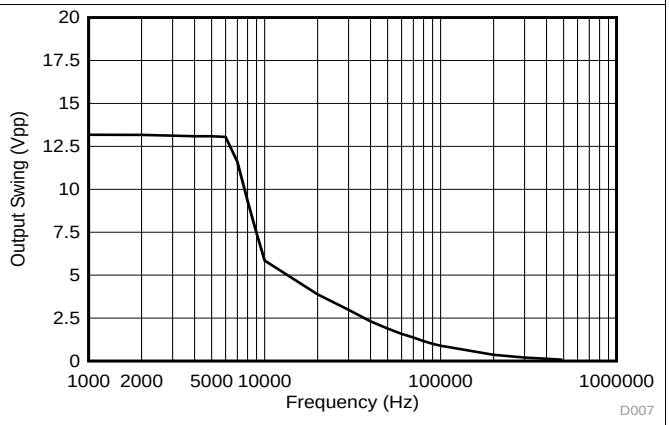



**Figure 6. Maximum Output Swing vs. Frequency (VCC = 15 V)**

# 7 Parameter Measurement Information

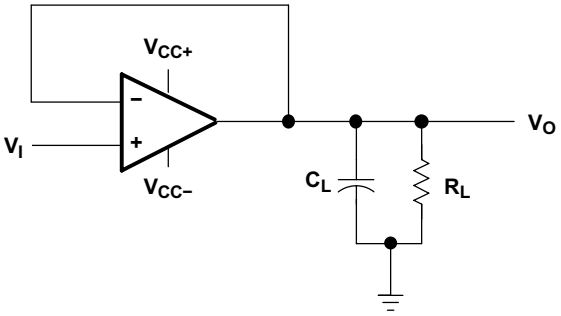



**Figure 7. Unity-Gain Amplifier**

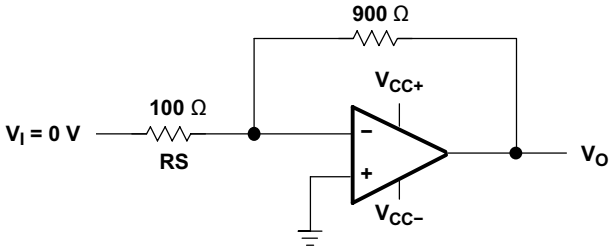



**Figure 8. Noise-Test Circuit**

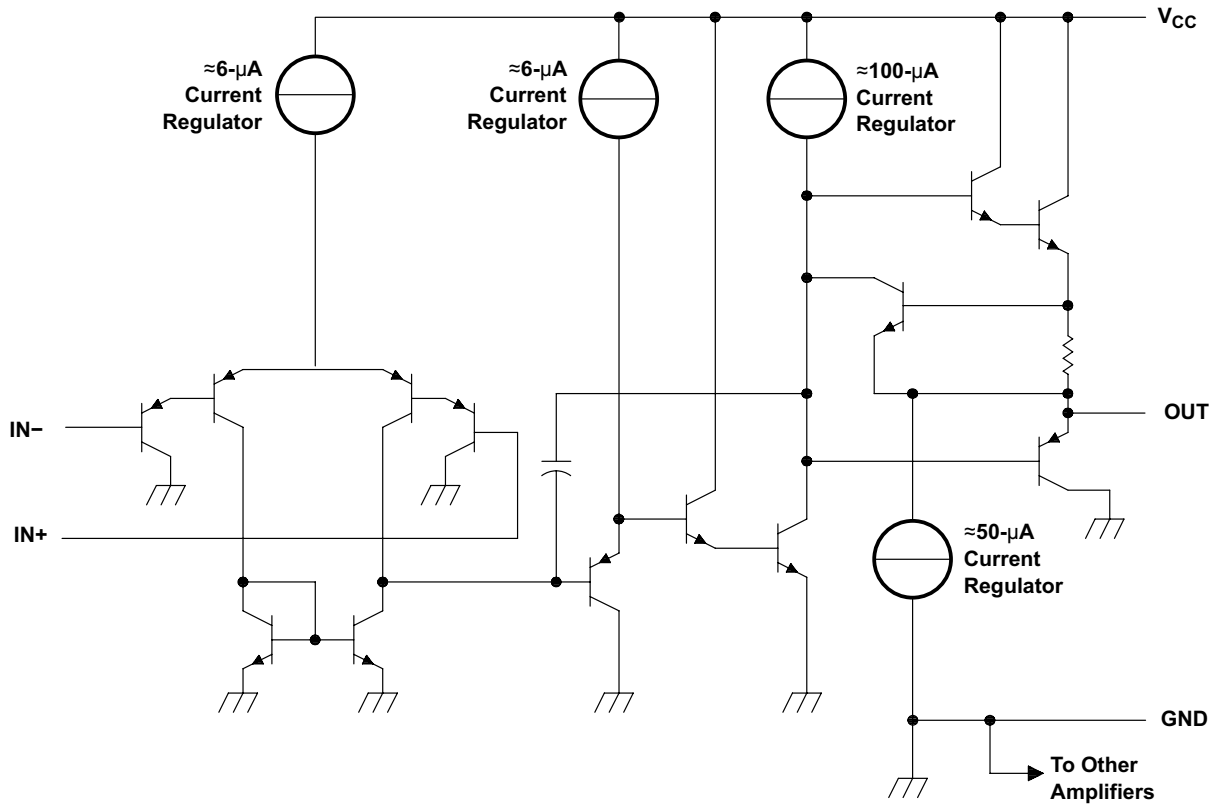
# 8 Detailed Description

## 8.1 Overview

The device consists of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 32 V, and $V_{CC}$ is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM324-MIL device can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional ±15-V supplies.

## 8.2 Functional Block Diagram




| COMPONENT COUNT (total device) | |
|---|---|
| Epi-FET | 1 |
| Transistors | 95 |
| Diodes | 4 |
| Resistors | 11 |
| Capacitors | 4 |

## 8.3 Feature Description

### 8.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/μs slew rate.

### 8.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_{CC}$ – 1.5 V ($V_{CC}$ – 2 V across temperature). Inputs may exceed $V_{CC}$ up to the maximum $V_{CC}$ without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than –0.3 V then input current should be limited to 1 mA and output phase is undefined.

## 8.4 Device Functional Modes

The device is powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The LM324-MIL operational amplifier is useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

## 9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

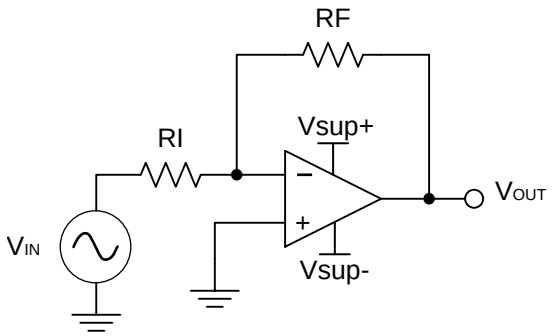





**Figure 9. Application Schematic**

### 9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

## Typical Application (continued)

### 9.2.3 Application Curve

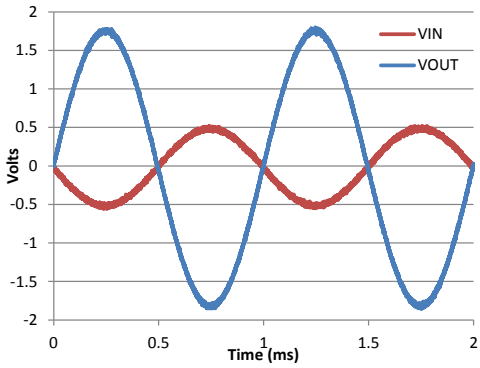



**Figure 10. Input and Output Voltages of the Inverting Amplifier**

## 10 Power Supply Recommendations

**CAUTION**

Supply voltages larger than 32 V for a single supply, or outside the range of ±16 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Examples

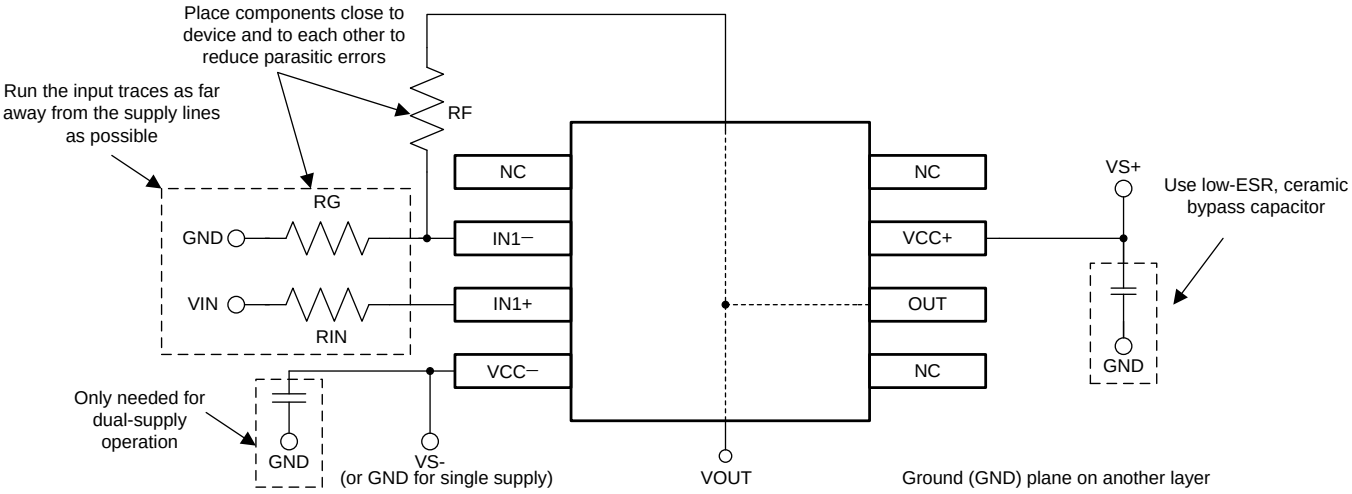



**Figure 11. Operational Amplifier Board Layout for Noninverting Configuration**

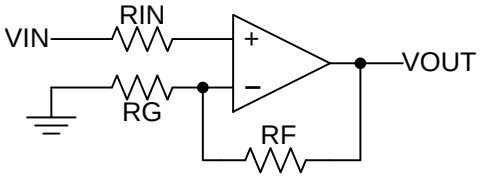



**Figure 12. Operational Amplifier Schematic for Noninverting Configuration**

# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントのサポート

### 12.1.1 関連資料

関連資料については、以下を参照してください。

*『基板のレイアウト技法』*、SLOA089

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.3 コミュニティ・リソース

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## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM324 MWA | Active | Production | WAFERSALE (YS) \| 0 | 1 \| NOT REQUIRED | - | Call TI | Level-1-NA-UNLIM | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

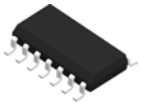
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

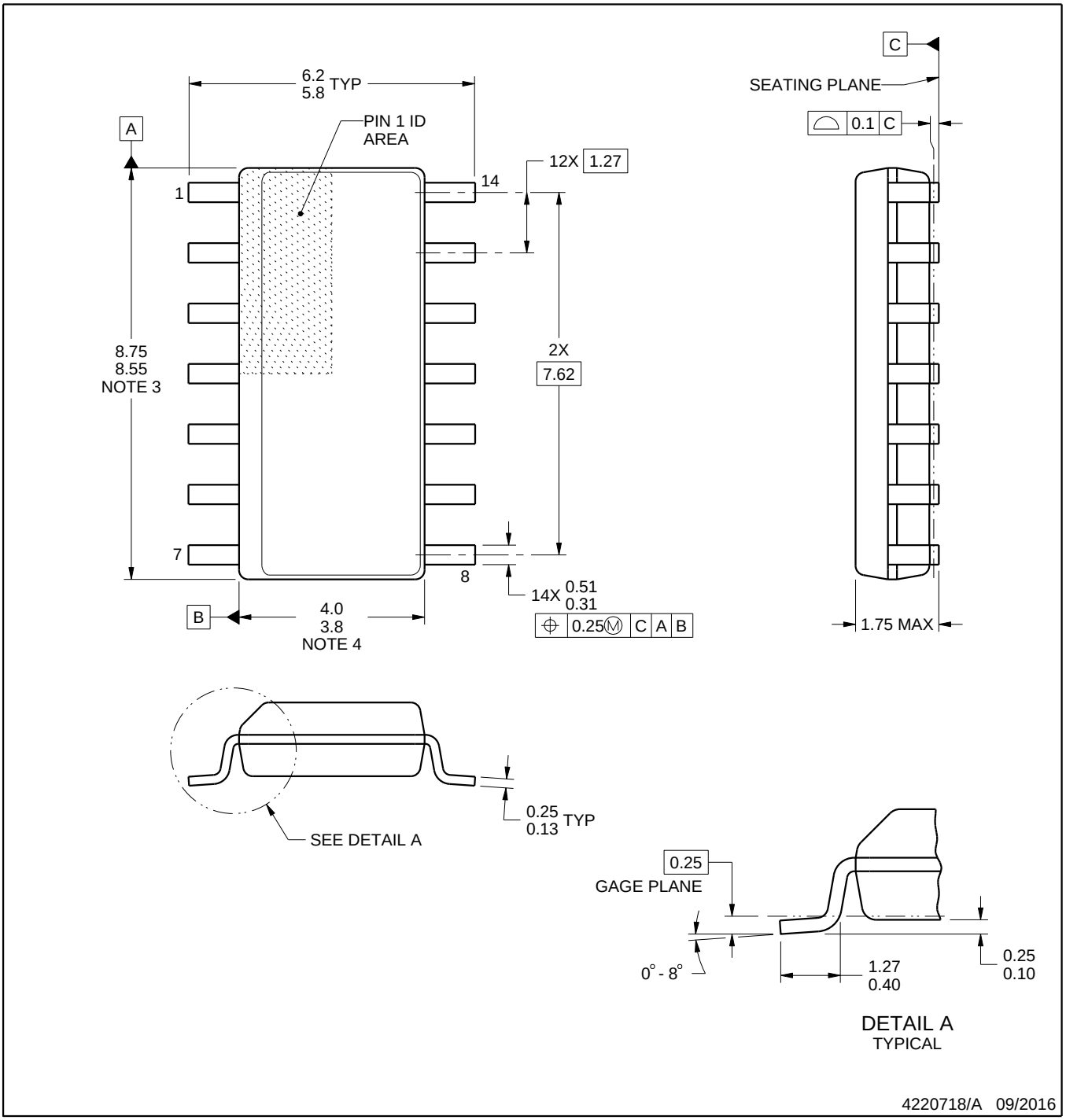


# PACKAGE OUTLINE

## D0014A

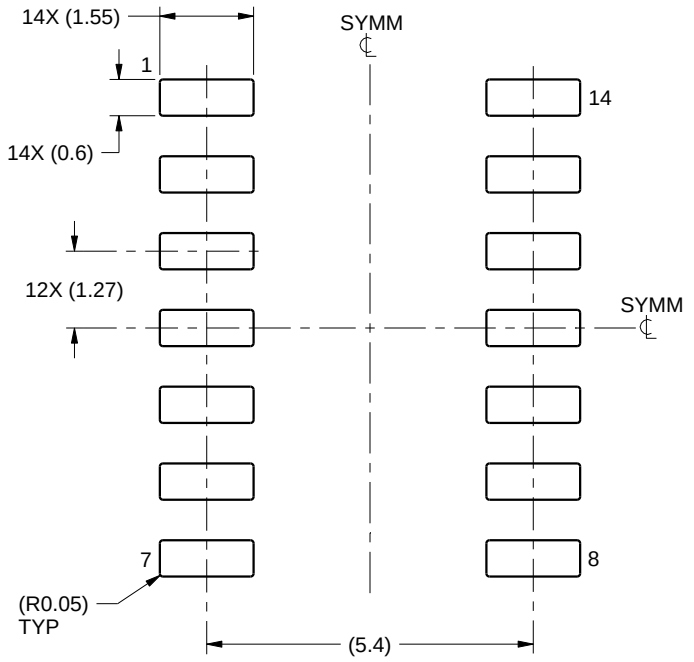
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

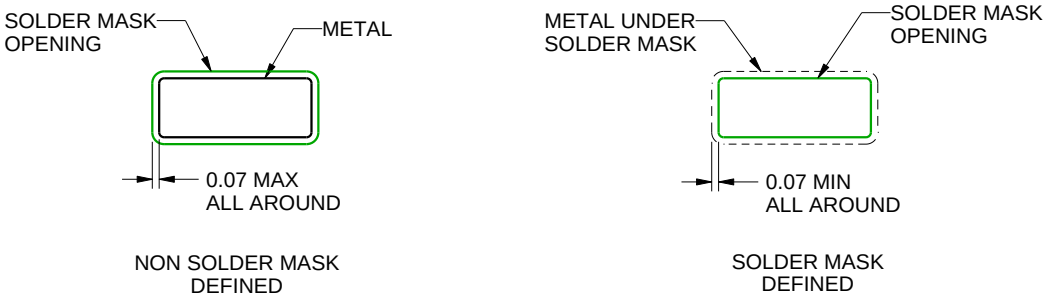



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

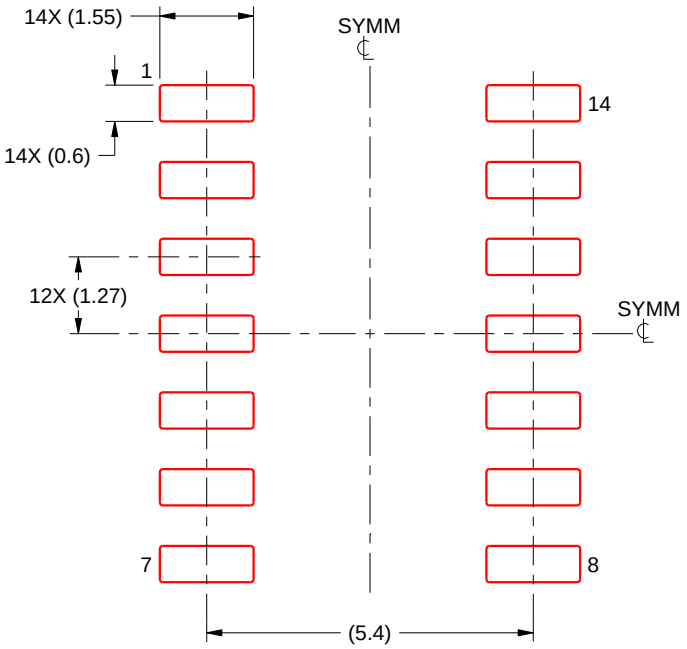
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

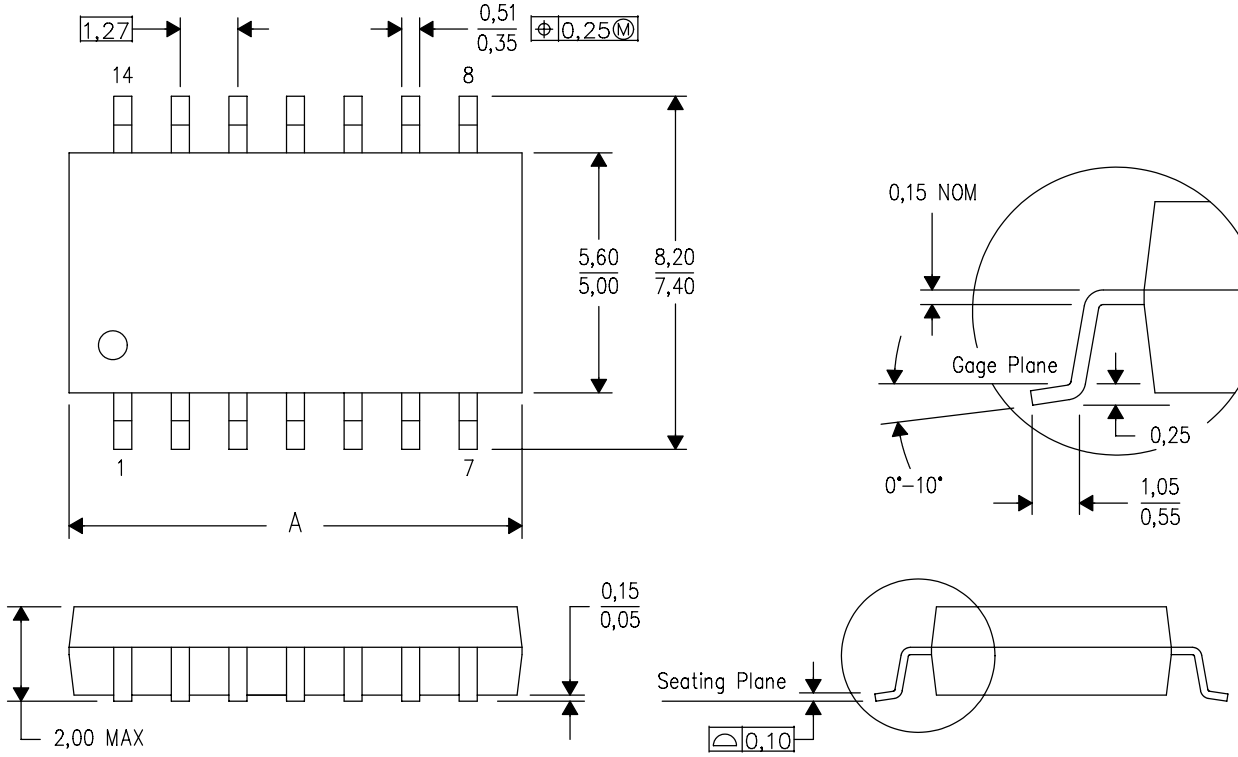
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

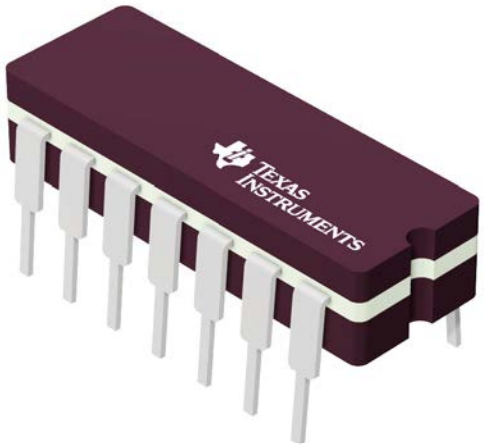
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

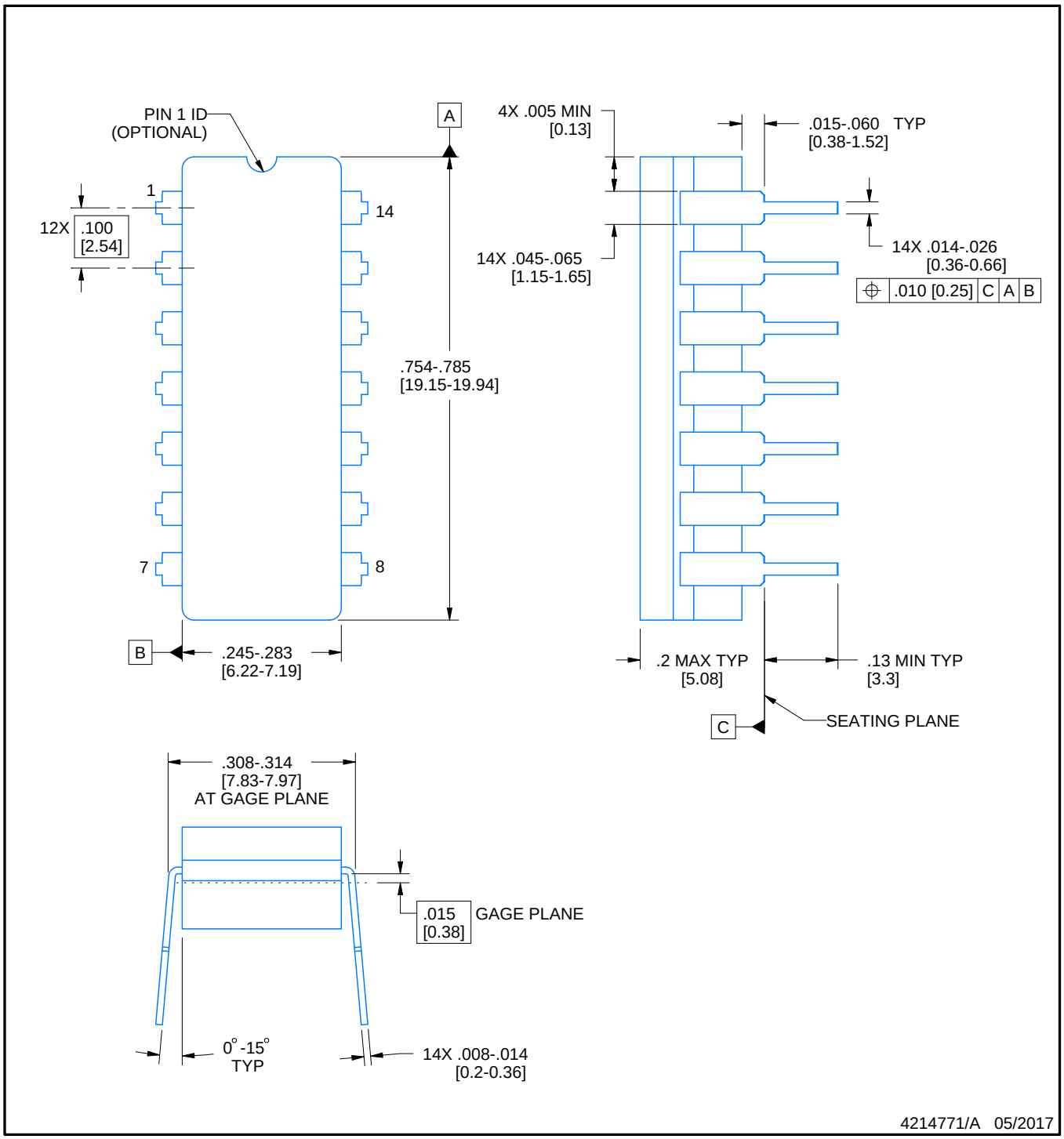
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

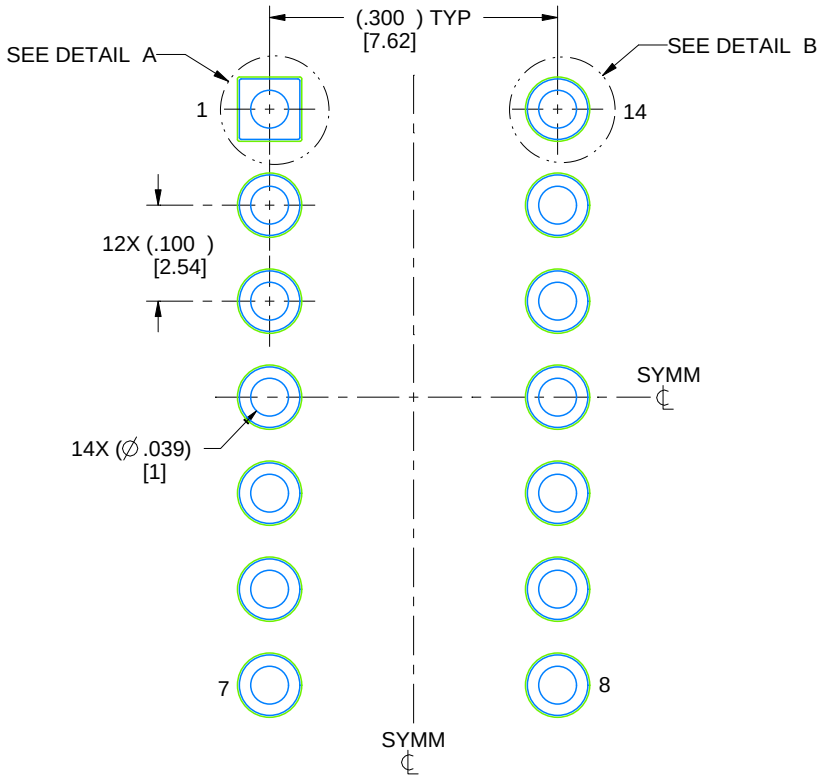
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

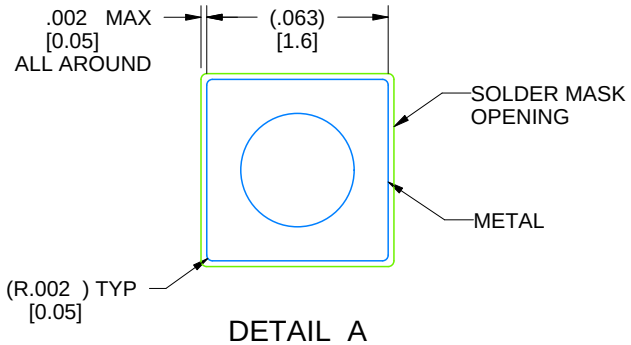
## J0014A

## CDIP - 5.08 mm max height

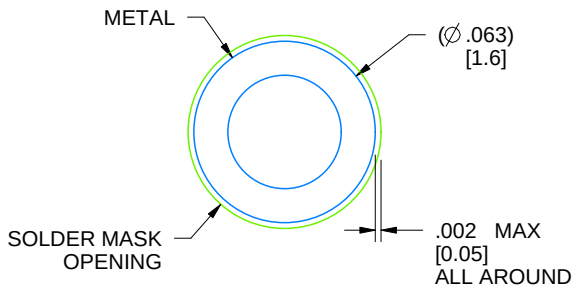
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



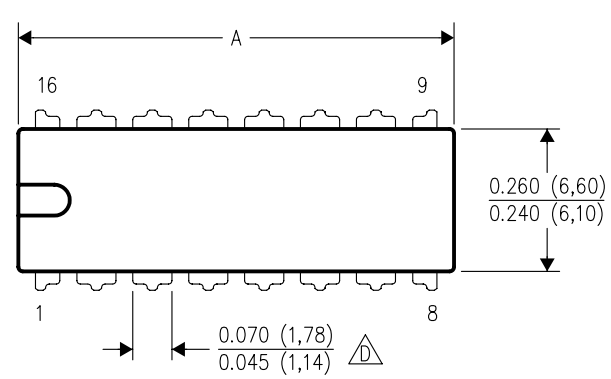

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

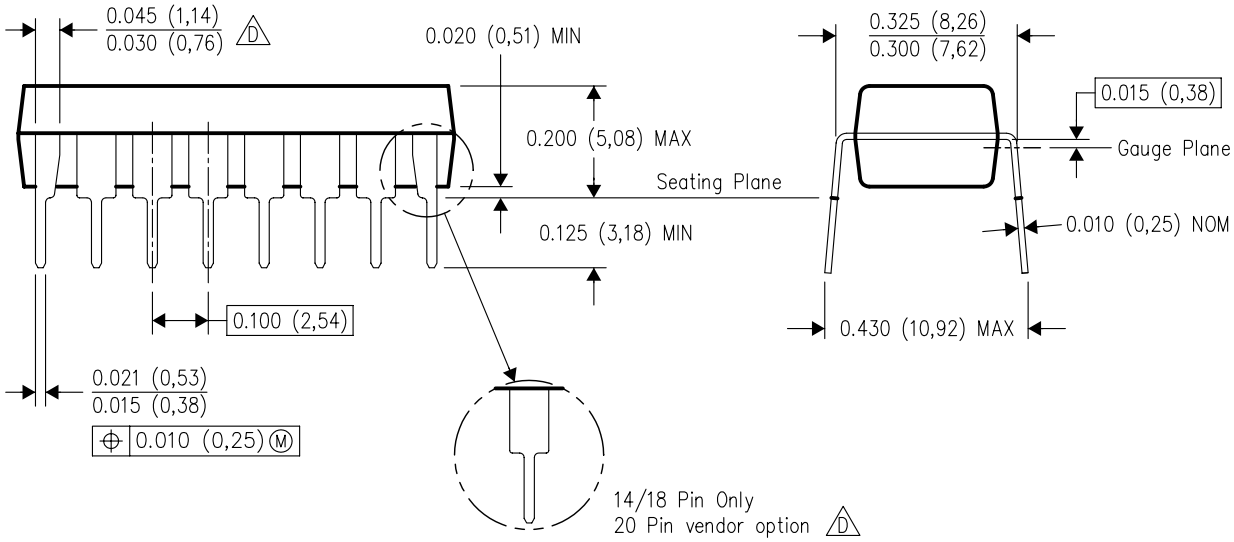
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

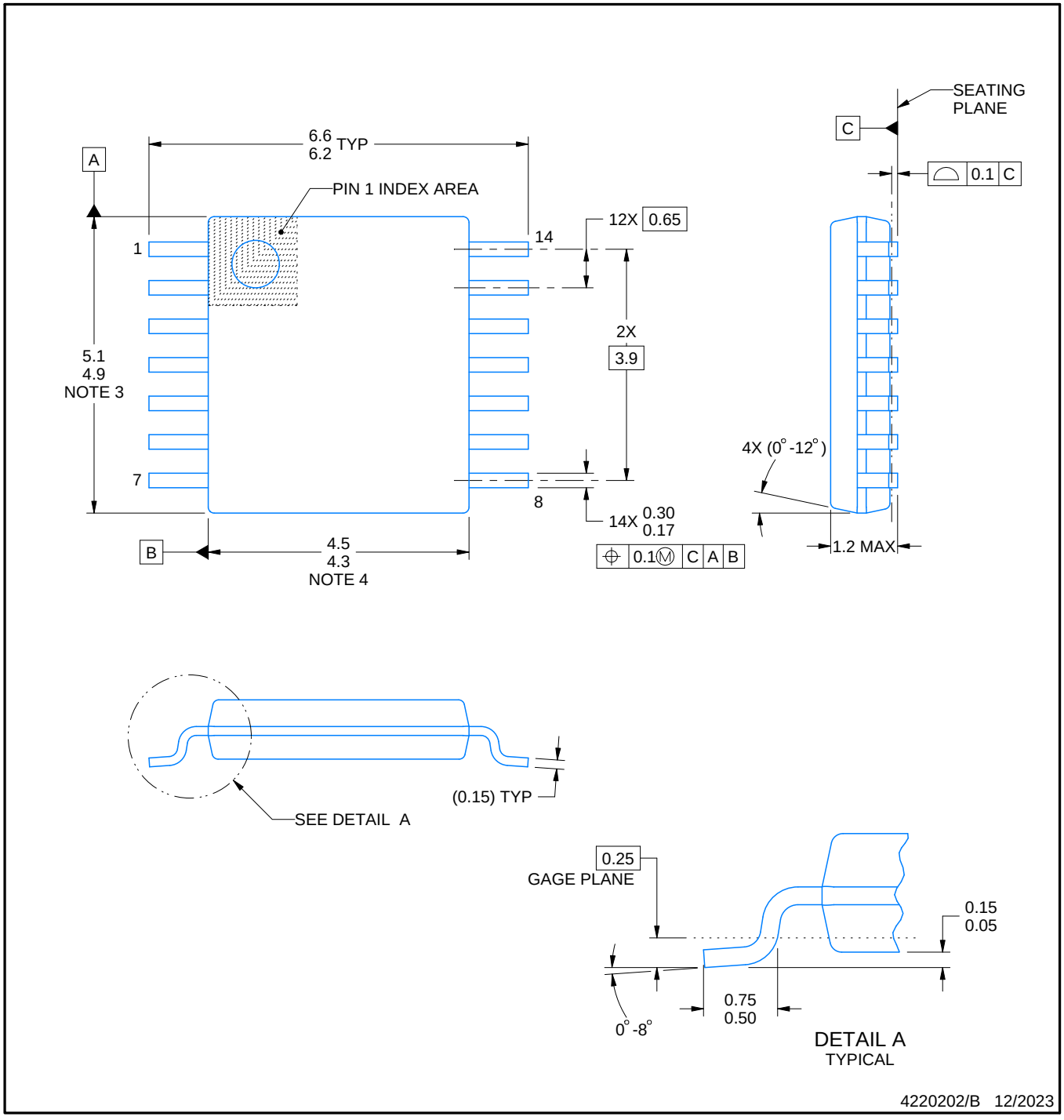
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

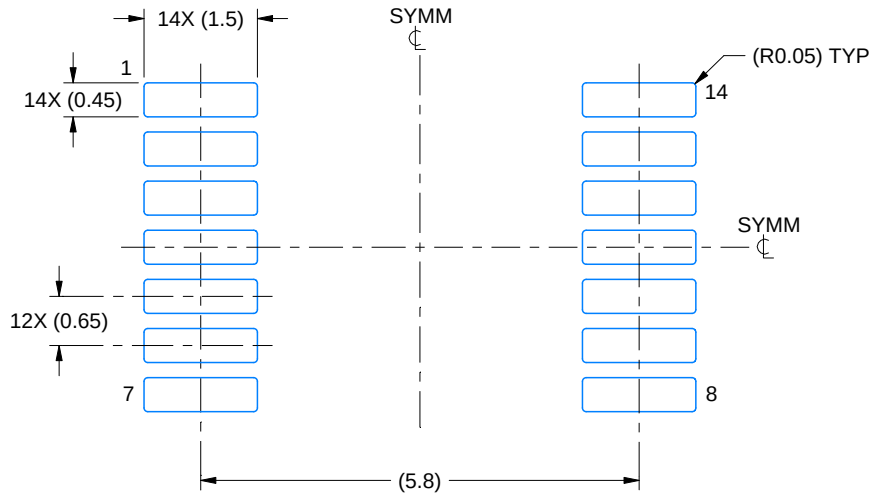
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

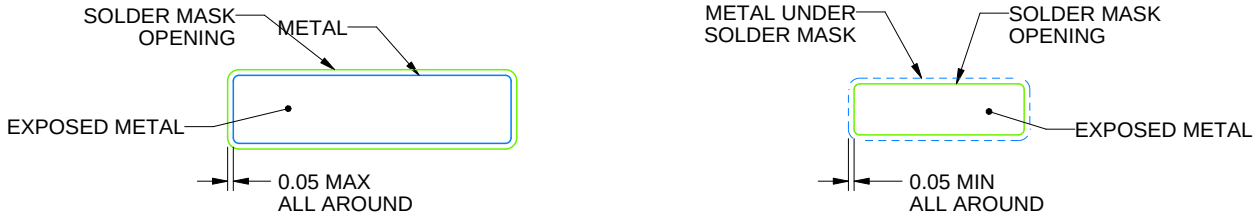



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

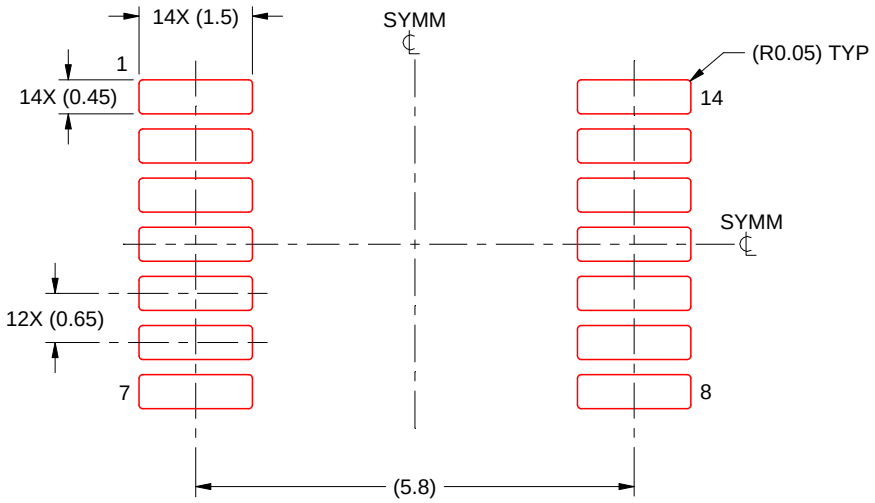



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



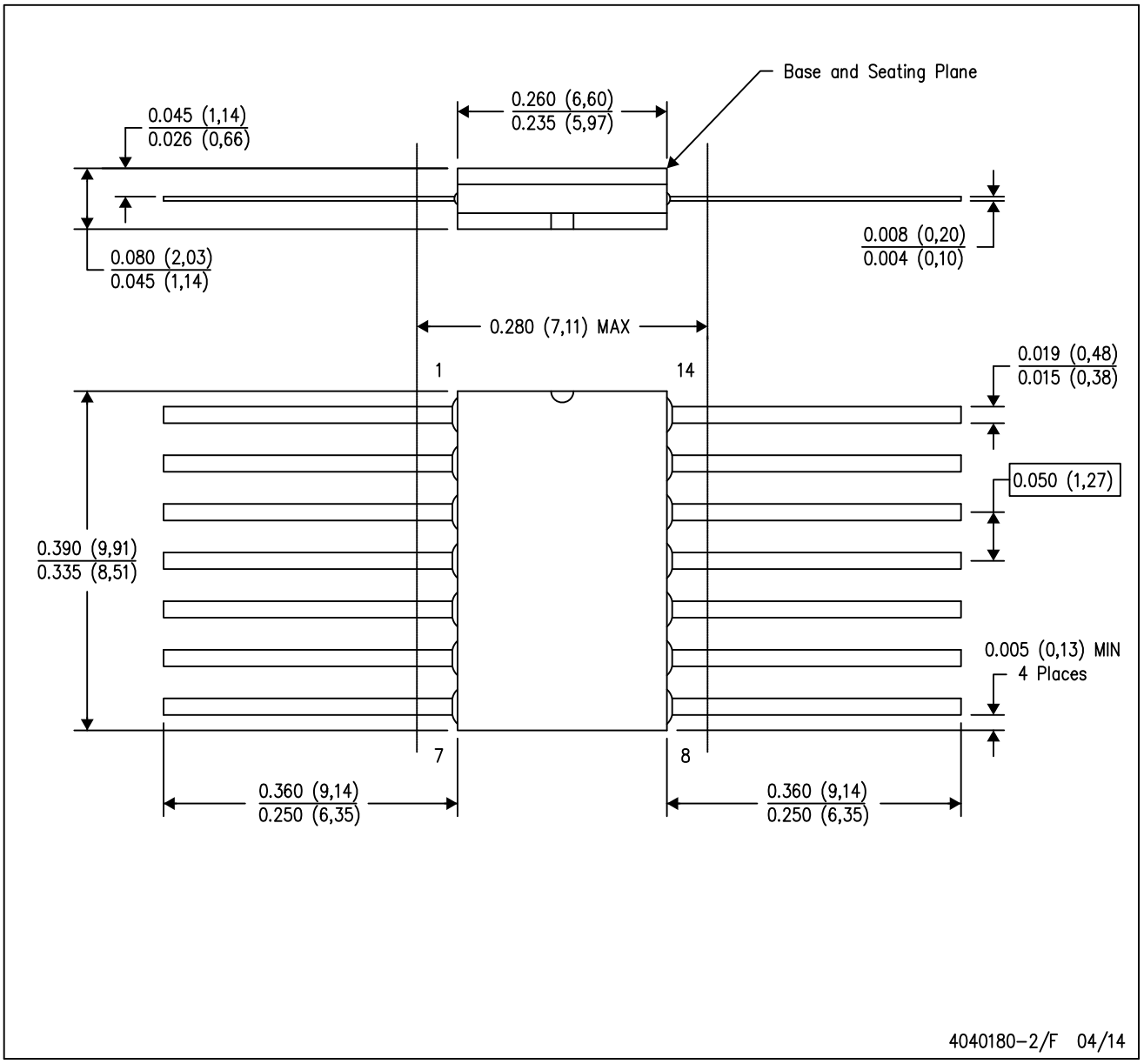

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



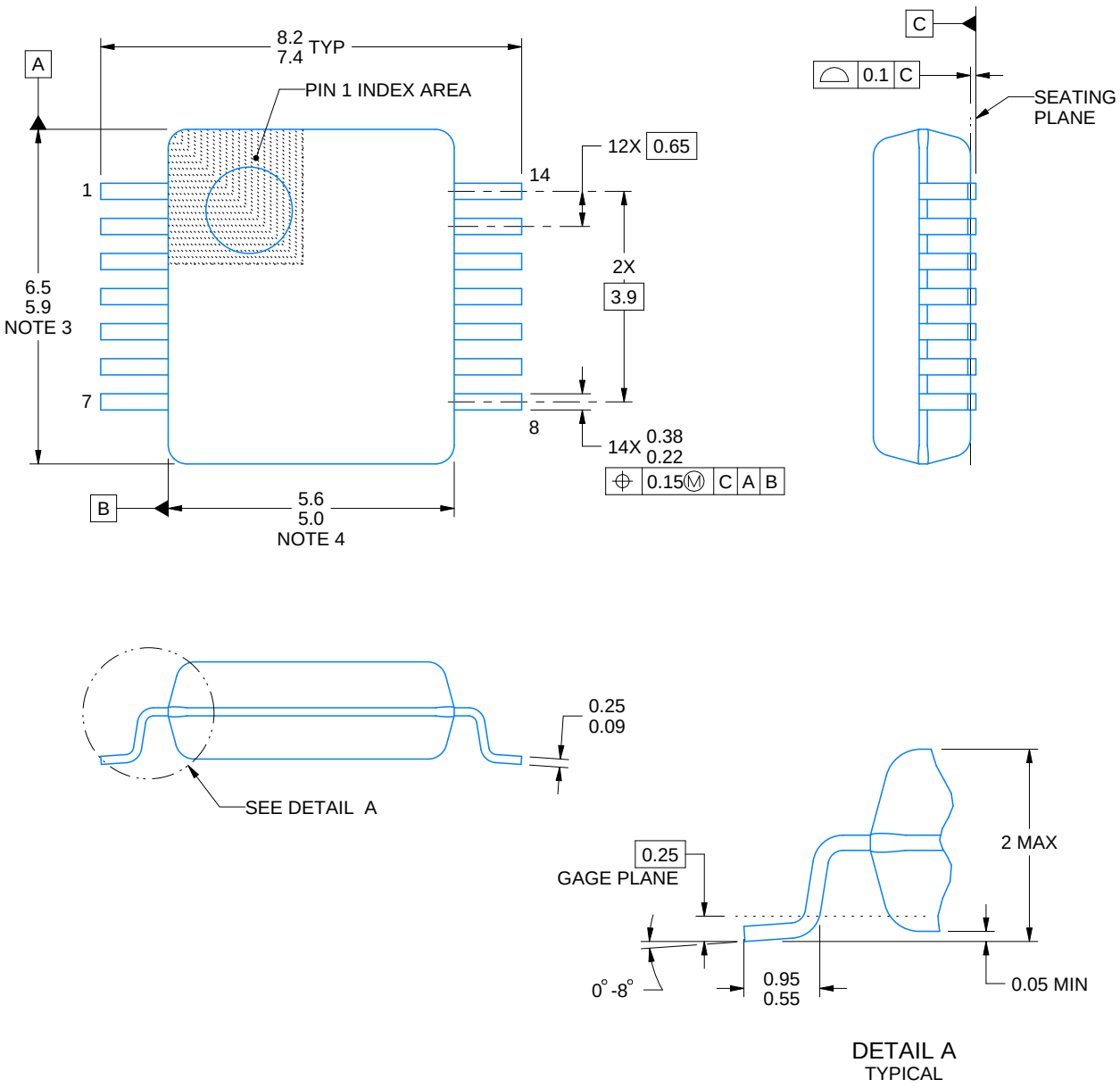

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

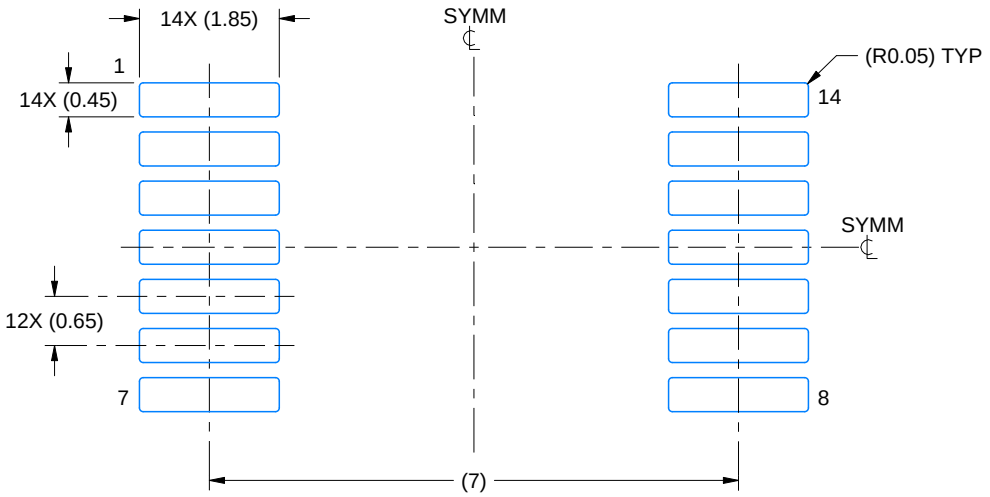
SMALL OUTLINE PACKAGE



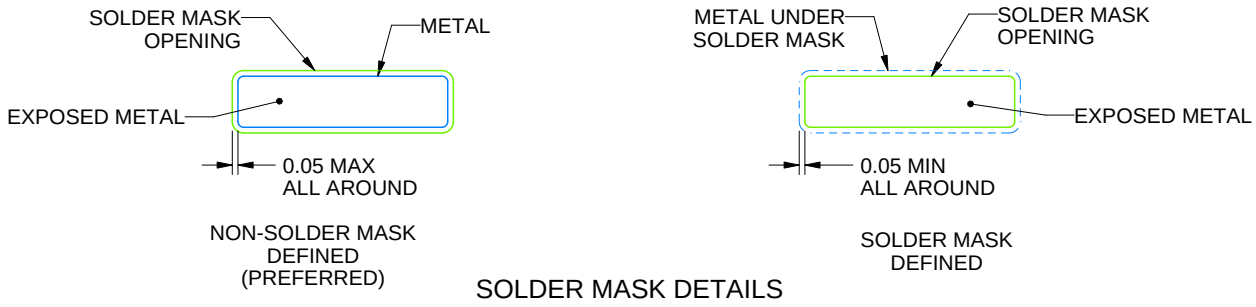

4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

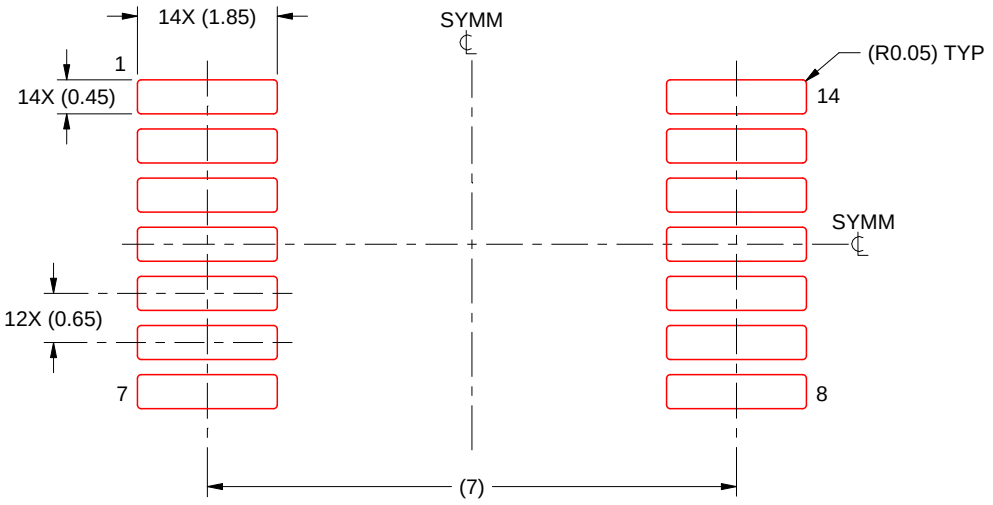



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月