TEXAS INSTRUMENTS
LM74700D-Q1
JAJSRB9 – SEPTEMBER 2023

LM74700D-Q1 車載用、低 I_Q、バッテリ逆接続保護向け、理想的ダイオード・コントローラ

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:
    -40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 3.2V～65V の入力範囲 (スタートアップ時 3.9V)
- 逆電圧定格:-65V
- 外部の N チャネル MOSFET 用のチャージ・ポンプ
- アノードからカソードへの順方向電圧降下レギュレーション:20mV
- イネーブル・ピン機能
- シャットダウン時電流 (EN=LOW):1µA
- 動作時静止電流 (EN = HIGH):80µA
- ピーク・ゲート・ターンオフ電流:2.3A
- 逆電流遮断に対する高速応答:0.75µs 未満
- 適切な TVS ダイオードにより車載用 ISO7637 過渡要件に適合
- 8 ピン SOIC パッケージで供給

2 アプリケーション

- 車載用 ADAS システム - カメラ
- 車載用インフォテインメント・システム - ヘッド・ユニット
- 産業用ファクトリ・オートメーション - PLC
- エンタープライズ向け電源
- アクティブ OR 接続による冗長化電源の実現

3 概要

LM74700D-Q1 は、外部の N チャネル MOSFET と組み合わせて理想ダイオード整流器として動作することにより 20mV の順方向電圧降下で低損失逆極性保護を実現する、車載用 AEC Q100 認定済み理想的ダイオード・コントローラです。入力電源電圧範囲が 3.2V～65V と広いため、12V、24V、48V の車載用バッテリ・システムも含め、多くの一般的な DC バス電圧を制御できます。3.2V の入力電圧をサポートしているため、車載用システムの厳しいコールド・クランク要件に向けた、特に優れた設計になっています。このデバイスは、最低 -65V の負の電源電圧に耐えられ、負荷を保護できます。

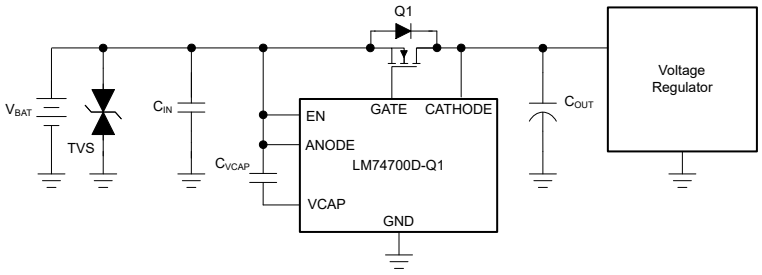
このデバイスは、MOSFET のゲートを制御し、順方向電圧降下を 20mV にレギュレートします。このレギュレーション方式により、逆電流イベント発生時に MOSFET の正常なターンオフが可能になり、DC 逆電流が確実にゼロになります。このデバイスは、逆電流遮断に対する高速応答 (0.75µs 未満) が可能なため、ISO7637 パルス・テスト中、電源障害時、ならびに入力のマイクロ短絡時における出力電圧のホールドアップ要件を持つシステムに適しています。

LM74700D-Q1 コントローラは、外部の N チャネル MOSFET 用にチャージ・ポンプ・ゲート駆動を提供します。LM74700D-Q1 は、電圧定格が高いため、車載用 ISO7637 保護のシステム設計の簡素化に利用できます。イネーブル・ピンが LOW のとき、コントローラはオフで、消費電流は約 1µA です。

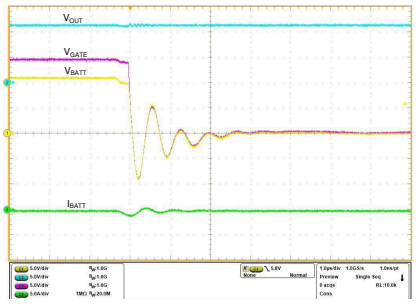
パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
LM74700D-Q1	D (SOIC、8)	5mm × 3.9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路図



入力短絡時の逆電流阻止

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2023	*	Initial release

5 Pin Configuration and Functions

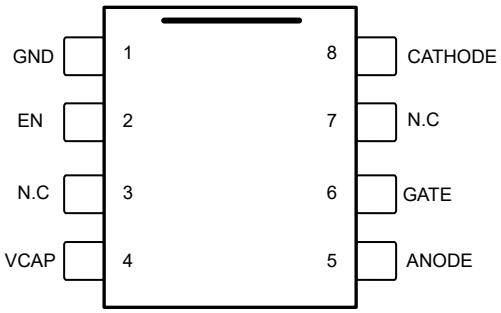


図 5-1. D Package, 8-Pin SOIC Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	G	Ground pin.
2	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
3	N.C	—	No connection
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	N.C	—	No connection
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	ANODE to GND	–65	70	V
	EN to GND, $V_{(ANODE)}$ > 0 V	–0.3	70	V
	EN to GND, $V_{(ANODE)}$ ≤ 0 V	$V_{(ANODE)}$	(70 + $V_{(ANODE)}$)	V
Output Pins	GATE to ANODE	–0.3	15	V
	VCAP to ANODE	–0.3	15	V
Output to Input Pins	CATHODE to ANODE	–5	75	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (GND, VCAP, ANODE, CATHODE)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	–60		65	V
	CATHODE to GND			65	
	EN to GND	–60		65	
Input to Output pins	ANODE to CATHODE	–70			V
External capacitance	ANODE	22			nF
	CATHODE, VCAP to ANODE	0.1			µF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM74700D-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4		65	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
$V_{(ANODE\ POR(Hys))}$	VANODE POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		0.9	1.5	µA
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V, $V_{(ANODE)}$ = 48 V		4.2		µA
$I_{(Q)}$	Operating Quiescent Current			80	130	µA
$I_{(Q)}$	Operating Quiescent Current	$V_{(ANODE)}$ = 48 V		110		µA
ENABLE INPUT						
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN\_IH)}$	Enable input high threshold		1.06	2	2.6	
$V_{(EN\_Hys)}$	Enable Hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3	5	µA
V_{ANODE} to $V_{CATHODE}$						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AK)}$ Threshold		13	20	29	mV
$V_{(AK)}$	$V_{(AK)}$ threshold for full conduction mode		34	50	57	mV
$V_{(AK\ REV)}$	$V_{(AK)}$ threshold for reverse current blocking		–17	–11	–2	mV
Gm	Regulation Error AMP Transconductance[1]		1200	1800	3100	µA/V
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} - V_{(CATHODE)}$ = 100 mV, $V_{(GATE)} - V_{(ANODE)}$ = 5 V	3	11		mA
	Peak sink current	$V_{(ANODE)} - V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} - V_{(ANODE)}$ = 5 V		2370		mA
	Regulation max sink current	$V_{(ANODE)} - V_{(CATHODE)}$ = 0 V, $V_{(GATE)} - V_{(ANODE)}$ = 5 V	6	26		µA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(ANODE)} - V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} - V_{(ANODE)}$ = 100 mV	0.4		2	Ω
CHARGE PUMP						

6.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} – V_{(ANODE)}$ = 7 V	162	300	600	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} – V_{(ANODE)}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(ANODE)}$	Charge pump voltage at $V_{(ANODE)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA	8			V
	Charge pump turn on voltage		10.8	12.1	12.9	V
	Charge pump turn off voltage		11.6	13	13.9	V
	Charge Pump Enable comparator Hysteresis		0.54	0.9	1.36	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(ANODE)}$ UV release at rising edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.8	6.6	7.7	V
	$V_{(VCAP)} – V_{(ANODE)}$ UV threshold at falling edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.11	5.68	6	V
CATHODE						
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = 12 V, $V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV		1.7	2	µA
		$V_{(ANODE)}$ = 48 V, $V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV		1.7		µA
		$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV		1.2	2.2	µA
		$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV, $V_{(ANODE)}$ = 48 V		3.5		µA
		$V_{(ANODE)}$ = –12 V, $V_{(CATHODE)}$ = 12 V		1.25	2.06	µA

(1) Parameter specified by design and characterization

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(VCAP)} > V_{(VCAP\ UVLOR)}$		75	110	µs
$t_{Reverse\ delay}$	Reverse voltage detection to Gate Turn Off delay	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV to –100 mV		0.45	0.75	µs
$t_{Reverse\ delay}$	Reverse voltage detection to Gate Turn Off delay	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV to –100 mV, $V_{(ANODE)}$ = 48 V		0.45		µs
$t_{Forward\ recovery}$	Forward voltage detection to Gate Turn On delay	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV to 700 mV		1.4	2.6	µs
$t_{Forward\ recovery}$	Forward voltage detection to Gate Turn On delay	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV to 700 mV, $V_{(ANODE)}$ = 48 V		1.4		µs

7 Typical Characteristics

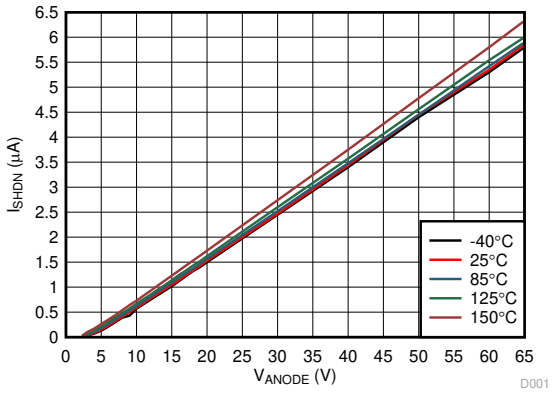


図 7-1. Shutdown Supply Current vs Supply Voltage

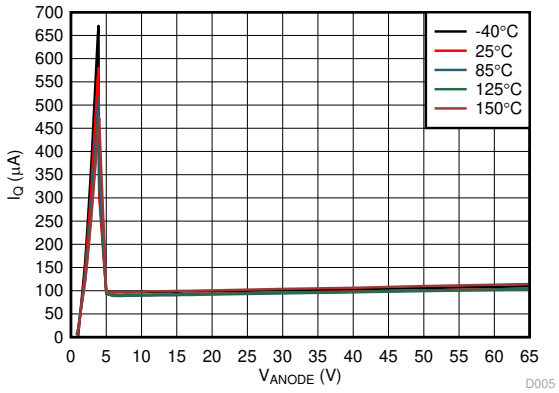


図 7-2. Operating Quiescent Current vs Supply Voltage

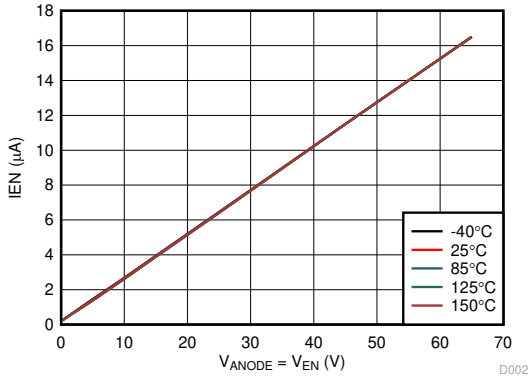


図 7-3. Enable Sink Current vs Supply Voltage

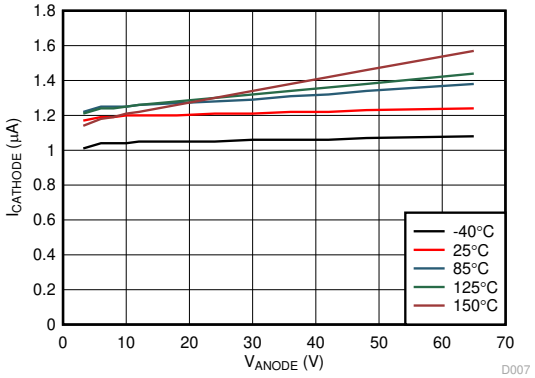


図 7-4. CATHODE Sink Current vs Supply Voltage

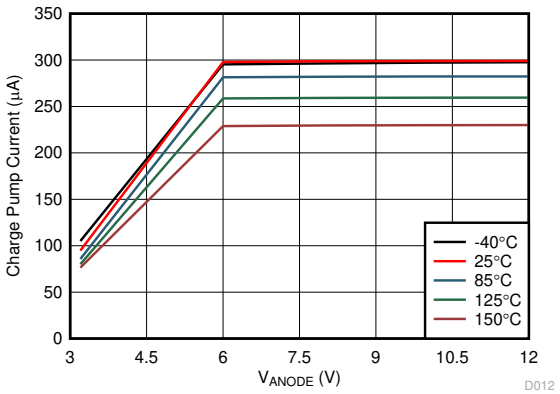


図 7-5. Charge Pump Current vs Supply Voltage at VCAP = 6 V

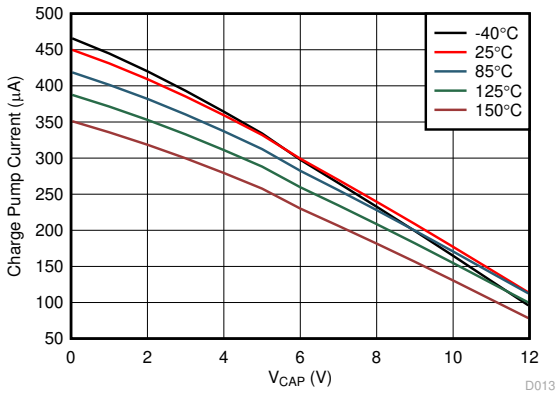


図 7-6. Charge Pump V-I Characteristics at ANODE > = 12 V

7 Typical Characteristics (continued)

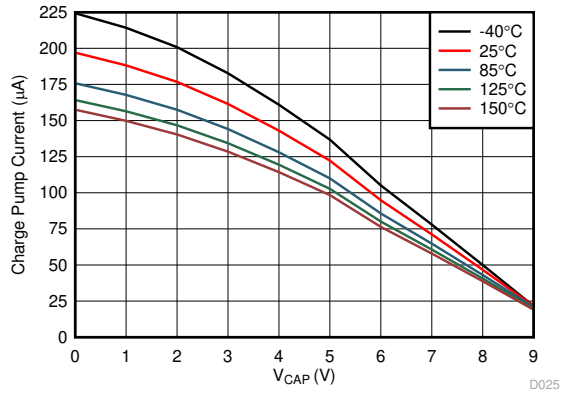


図 7-7. Charge Pump V-I Characteristics at ANODE = 3.2 V

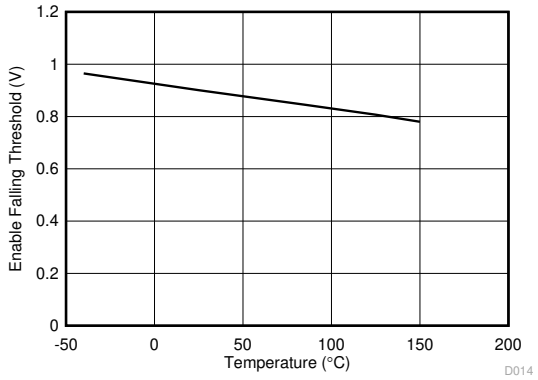


図 7-8. Enable Falling Threshold vs Temperature

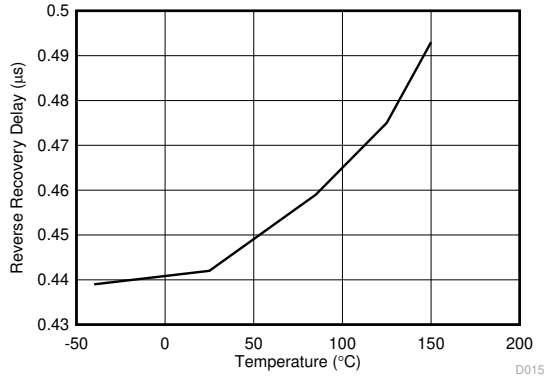


図 7-9. Reverse Current Blocking Delay vs Temperature

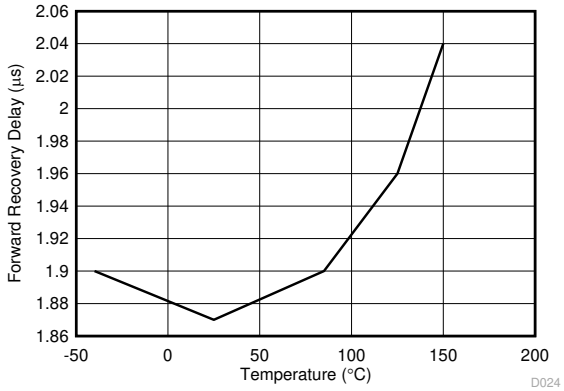


図 7-10. Forward Recovery Delay vs Temperature

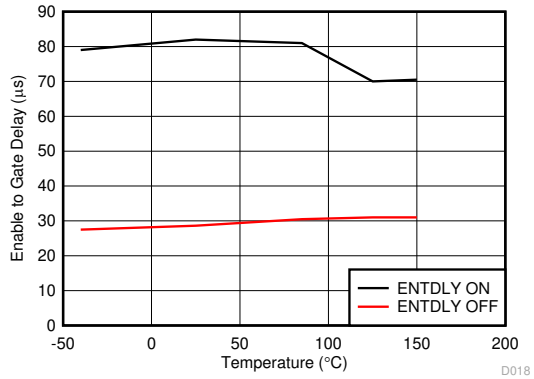


図 7-11. Enable to Gate Delay vs Temperature

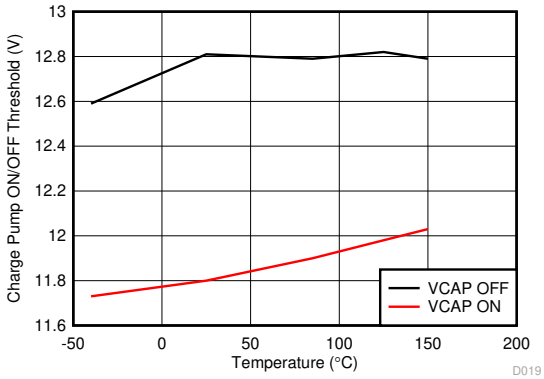


図 7-12. Charge Pump ON/OFF Threshold vs Temperature

7 Typical Characteristics (continued)

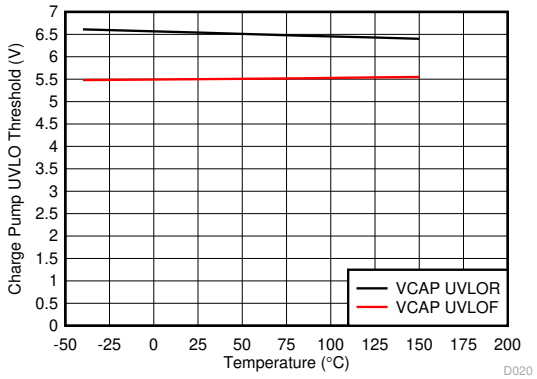


図 7-13. Charge Pump UVLO Threshold vs Temperature

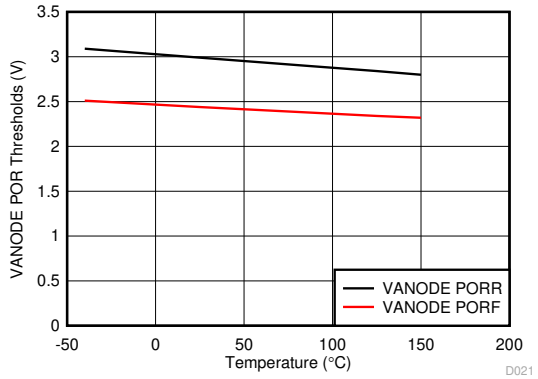


図 7-14. ANODE POR Threshold vs Temperature

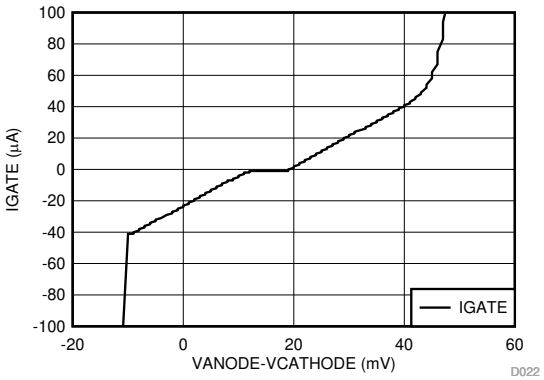


図 7-15. Gate Current vs Forward Voltage Drop

8 Parameter Measurement Information

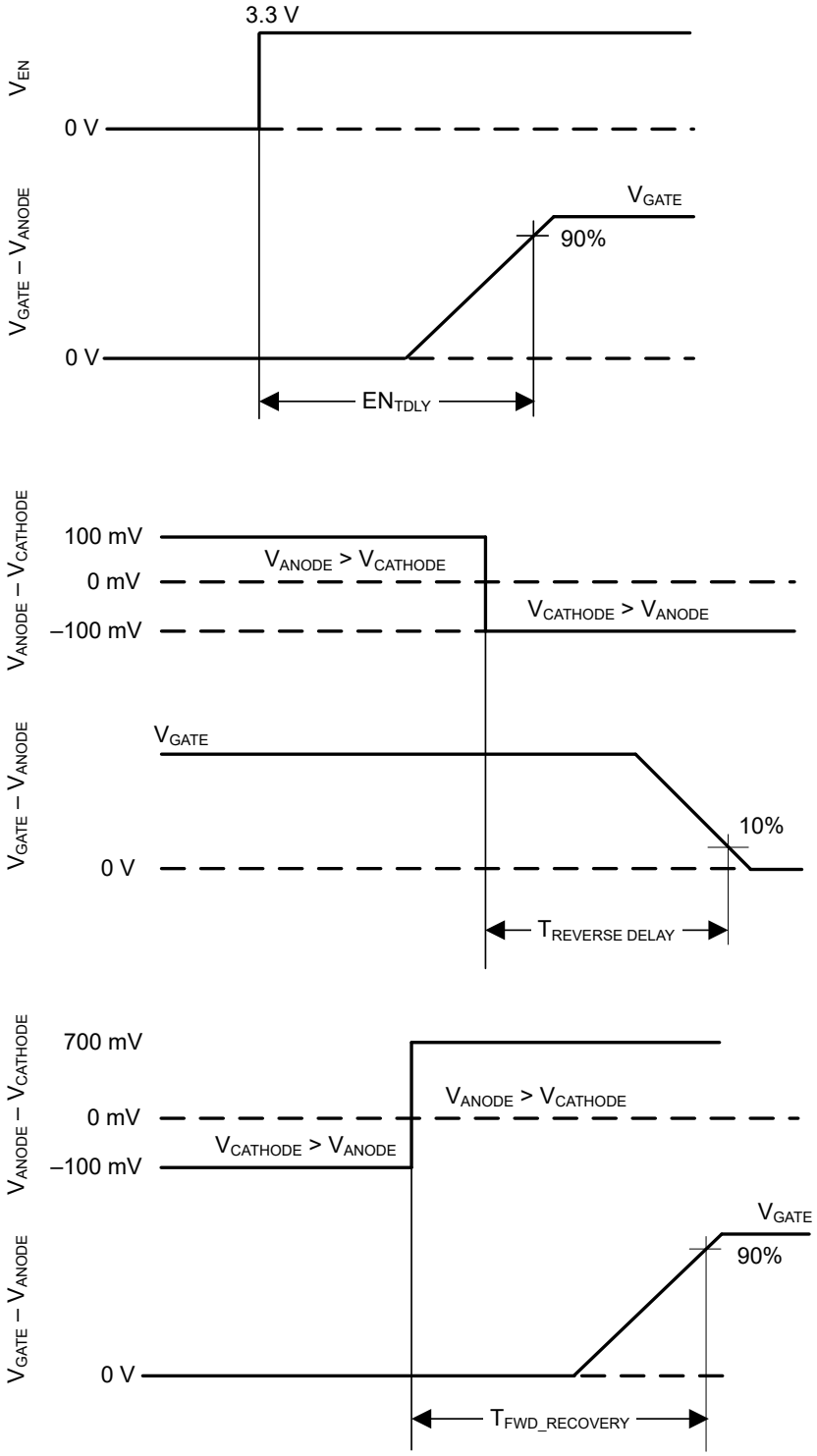


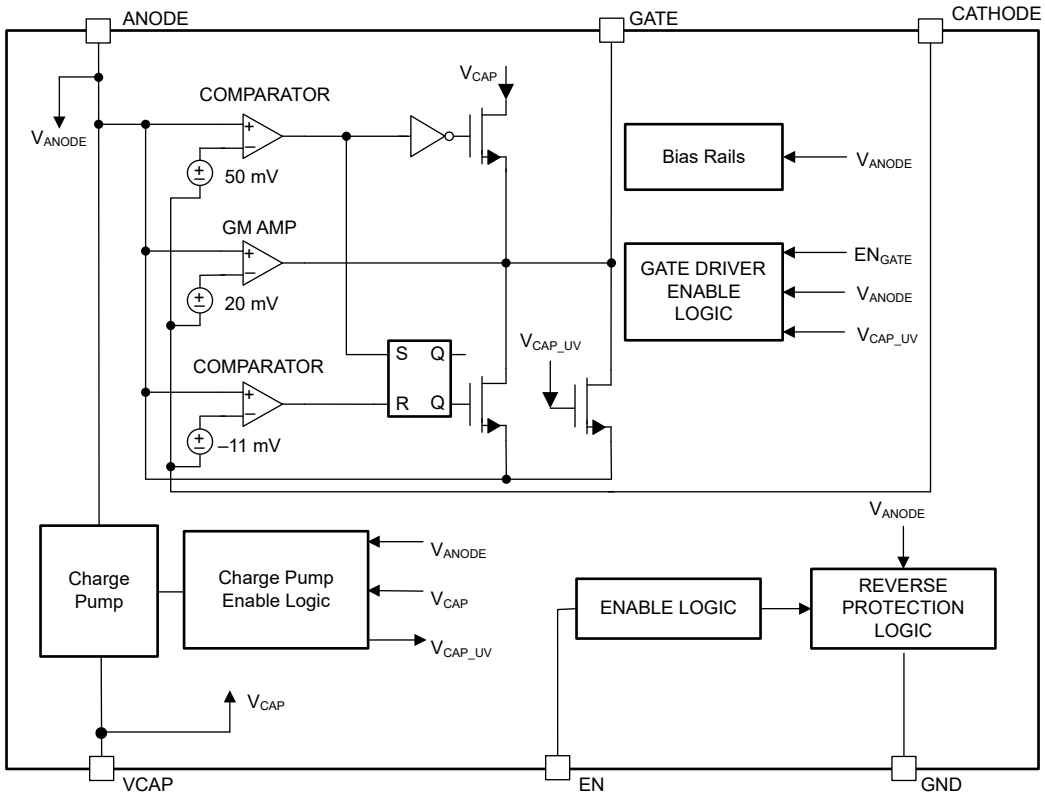
図 8-1. Timing Waveforms

9 Detailed Description

9.1 Overview

The LM74700D-Q1 ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an OR-ing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn-off of the MOSFET during a reverse current event and make sure of zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below –11 mV , resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the LM74700D-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current.

9.2 機能ブロック図



9.3 Feature Description

9.3.1 Input Voltage

The ANODE pin is used to power the LM74700D-Q1 internal circuitry, typically drawing 80 µA when enabled and 1 µA when disabled. If the ANODE pin voltage is greater than the POR Rising threshold, then LM74700D-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –65 V, allowing the LM74700D-Q1 to withstand negative voltage transients.

9.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN pin, voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled the charge pump sources a charging current of 300-µA typical. If EN pins is pulled low, then the charge pump remains disabled. To make sure that the external MOSFET can be driven above the specified threshold voltage, the VCAP to ANODE voltage must be above the under voltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled.

$$T_{DRV\_EN} = 75\mu s + C_{VCAP} \times \frac{V_{VCAP\_UVLOR}}{300\ \mu A} \quad (1)$$

where

- C_{VCAP} is the charge pump capacitance connected across ANODE and VCAP pins
- V_{VCAP_UVLOR} = 6.6 V (typical)

To remove any chatter on the gate drive, approximately 900 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 13 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 12.1 V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 12.1 V and 13 V as shown in 図 9-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74700D-Q1 is reduced. When the charge pump is disabled, it sinks 5-µA typical.

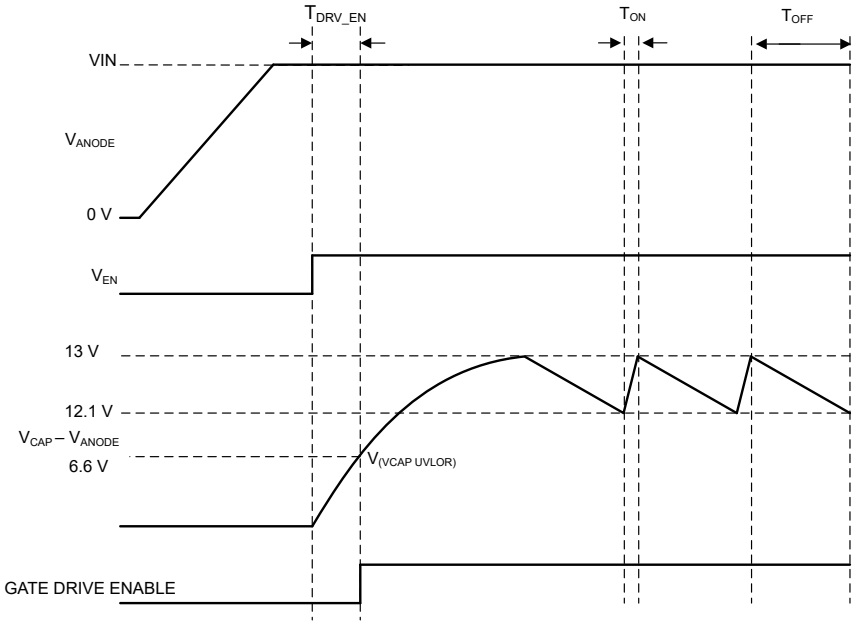


図 9-1. Charge Pump Operation

9.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the *Regulated conduction Mode*, *Full Conduction Mode* and *Reverse Current Production Mode* sections. 図 9-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74700D-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is –11 mV.

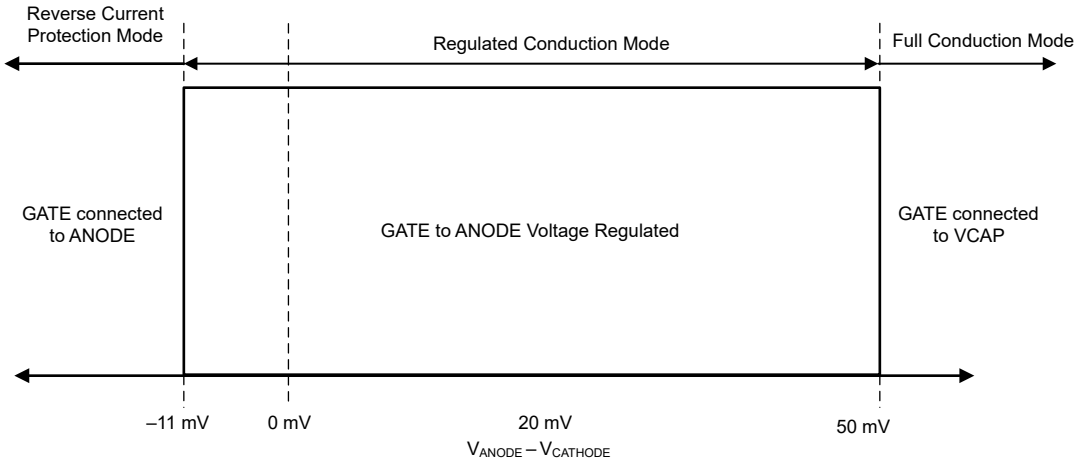


図 9-2. Gate Driver Mode Transitions

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than ANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

9.3.4 Enable

The LM74700D-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74700D-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –65 V. This ability allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 µA pulls the EN pin low and disables the device.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The LM74700D-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN\_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74700D-Q1 enters low I_Q operation with the ANODE pin only sinking 1 µA. When the LM74700D-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET body diode.

9.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74700D-Q1. Each of the three modes is described in the *Regulated Conduction Mode*, *Full Conduction Mode*, and *Reverse Current Protection Mode* sections.

9.4.2.1 Regulated Conduction Mode

For the LM74700D-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the *Gate Driver* section, and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of –11 mV to 50 mV. During forward regulation mode, the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn-off of the MOSFET at very light loads and makes sure of zero DC reverse current flow.

9.4.2.2 Full Conduction Mode

For the LM74700D-Q1 to operate in full conduction mode, the gate driver must be enabled as described in the *Gate Driver* section, and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

9.4.2.3 Reverse Current Protection Mode

For the LM74700D-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the *Gate Driver* section, and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than –11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

10 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LM74700D-Q1 is used with an N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in 図 10-1 where the LM74700D-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74700D-Q1 to operate, but is used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

10.2 Typical Application

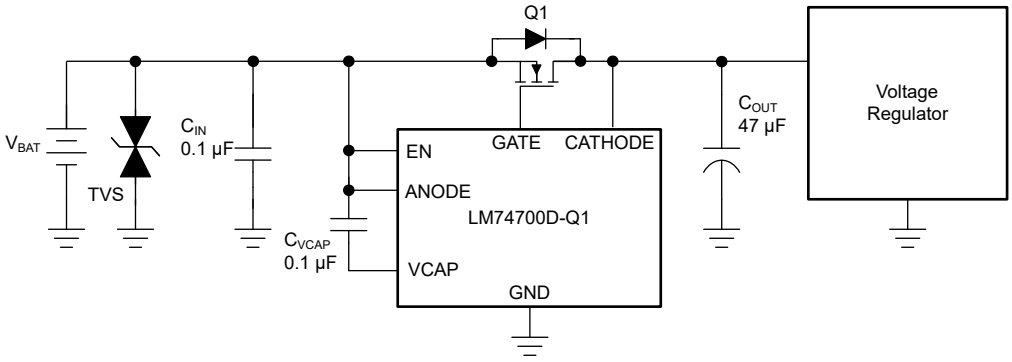


図 10-1. Typical Application Circuit

10.2.1 Design Requirements

A design example, with system design parameters listed in 表 10-1 is presented.

表 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 12-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A Nominal, 5-A Maximum
Output capacitance	1-µF Minimum, 47-µF Typical Holdup Capacitance
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2

10.2.2 Detailed Design Procedure

10.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

10.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum source current through body diode and the drain-to-source On resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This includes any anticipated fault conditions. TI recommends to use MOSFETs with voltage rating up to 60-V maximum with the LM74700D-Q1 because anode-cathode maximum voltage is 65 V. The maximum V_{GS} LM74700D-Q1 can drive is 13 V, so select s MOSFET with 15-V minimum V_{GS}. If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level. During start-up, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ cam not be beneficial always. Higher $R_{DS(ON)}$ provides increased voltage information to the LM74700D-Q1 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. TI recommends to operate the MOSFET in regulated conduction mode during nominal load conditions and select $R_{DS(ON)}$ such that at nominal operating current, forward voltage drop V_{DS} is close to 20-mV regulation point and not more than 50 mV.

As a guideline, TI suggests to choose $(20\ mV / I_{Load(Nominal)}) \leq R_{DS(ON)} \leq (50\ mV / I_{Load(Nominal)})$.

MOSFET manufacturers usually specify $R_{DS(ON)}$ at 4.5-V V_{GS} and 10-V V_{GS}. $R_{DS(ON)}$ increases drastically below 4.5-V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th}. For stable regulation at light load conditions, TI recommends to operate the MOSFET close to 4.5-V V_{GS}, that is, much higher than MOSFET gate threshold voltage. TI recommends to choose MOSFET gate threshold voltage V_{th} of 2-V to 2.5-V maximum. Choosing a lower V_{th} MOSFET also reduces the turn-ON time.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 3-A nominal current: $(20\ mV / 3A) \leq R_{DS(ON)} \leq (50\ mV / 3A) = 6.67\ m\Omega \leq R_{DS(ON)} \leq 16.67\ m\Omega$
- MOSFET gate threshold voltage V_{th}: 2-V maximum

DMT6007LFG MOSFET from Diodes Inc. is selected to meet this 12-V reverse battery protection design requirements and is rated at:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 6.5-mΩ typical and 8.5-mΩ maximum rated at 4.5-V V_{GS}
- MOSFET V_{th}: 2-V maximum

Consider thermal resistance of the MOSFET against the expected maximum power dissipation in the MOSFET to make sure that the junction temperature (T_J) is well controlled.

10.2.2.3 Charge Pump VCAP, Input and Output Capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 × $C_{ISS(MOSFET)}$(µF)
- C_{IN}: minimum 22 nF of input capacitance
- C_{OUT}: minimum 100 nF of output capacitance

10.2.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in 図 10-2, a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

There are two important specifications are breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a Zener diode and is specified at a low current value typical 1 mA and the breakdown voltage must be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74700D-Q1 (65 V). The breakdown voltage of TVS– must be beyond than maximum reverse battery voltage –16 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and must not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS– and the voltage across the TVS is close to the clamping voltage.

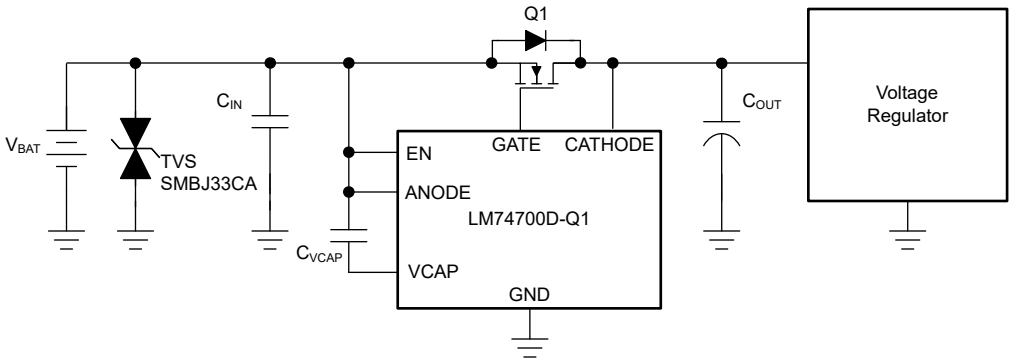


図 10-2. Typical 12-V Battery Protection With Single Bi-Directional TVS

The next criterion is that the absolute maximum rating of Anode to Cathode reverse voltage of the LM74700D-Q1 (–75 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, a 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

In case of ISO 7637-2 pulse 1, the anode of LM74700D-Q1 is pulled down by the ISO pulse and clamped by TVS–. The MOSFET is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS– must not exceed (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 15 A of peak surge current as shown in 図 10-5 and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS are rated up to 600-W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

10.2.4 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

The typical 24-V battery protection application circuit shown in 図 10-3 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.

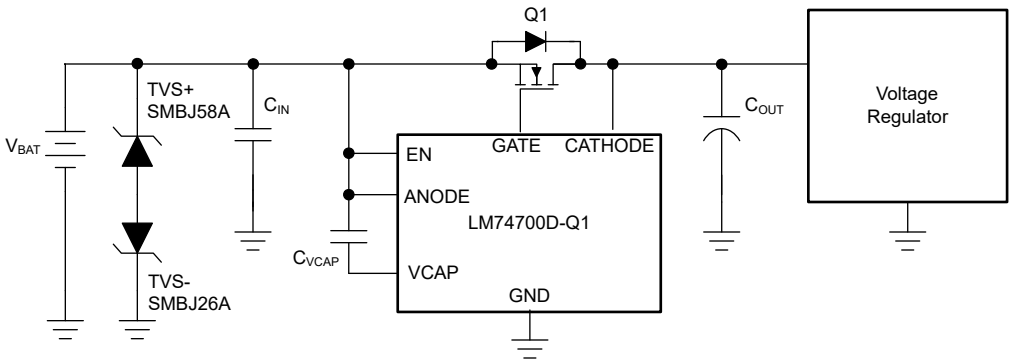


図 10-3. Typical 24-V Battery Protection with Two Uni-Directional TVS

The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74700D-Q1 (65 V), and must withstand 65-V suppressed load dump. The breakdown voltage of TVS– must be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This action translates to 12 A flowing through the TVS–. The clamping voltage of the TVS– cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (–TVS Clamping voltage + Output capacitor voltage). For a 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS– must not exceed, 75 V – 32 V = 43 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65 V, maximum clamping voltage is ≤ 43 V and the clamping voltage cannot be less than the breakdown voltage. Two uni-directional TVS connected back-back must be used at the input. For positive side TVS+, TI recommends SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical). For the negative side TVS–, TI recommends SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V.

For 24-V battery protection, TI recommends a 75-V rated MOSFET to be used along with SMBJ26A and SMBJ58A connected back-to-back at the input.

10.2.5 Application Curves

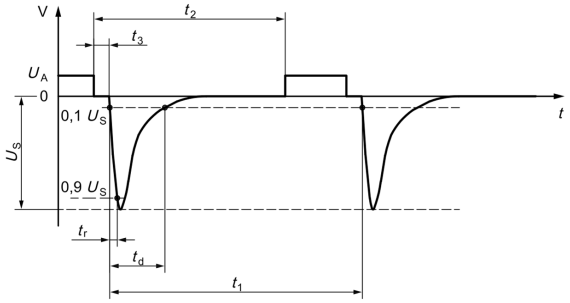
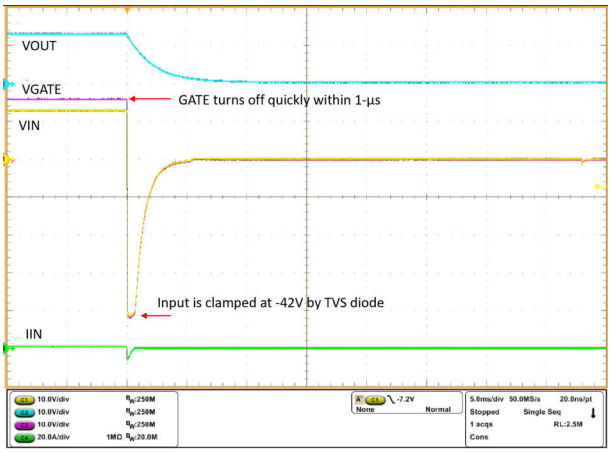
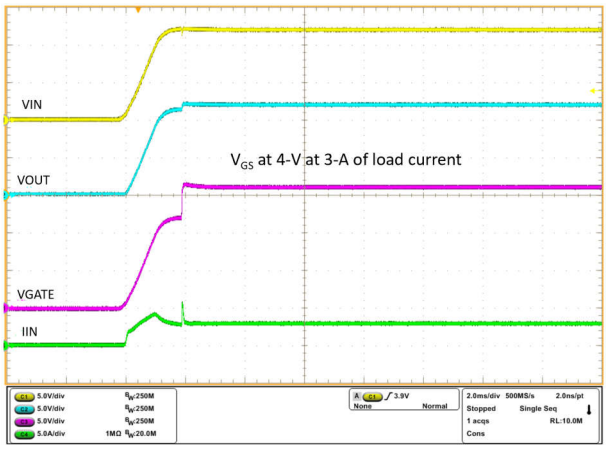


図 10-4. ISO 7637-2 Pulse 1



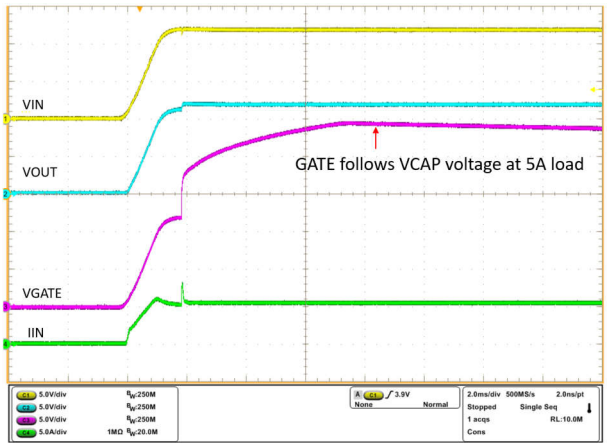
Time (5 ms/DIV)

図 10-5. Response to ISO 7637-2 Pulse 1



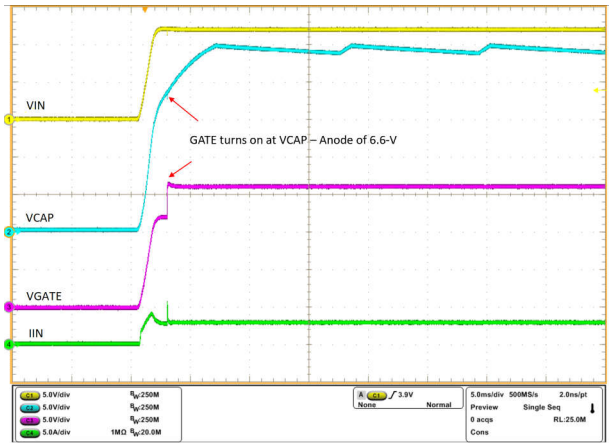
Time (2 ms/DIV)

図 10-6. Start-Up With 3-A Load



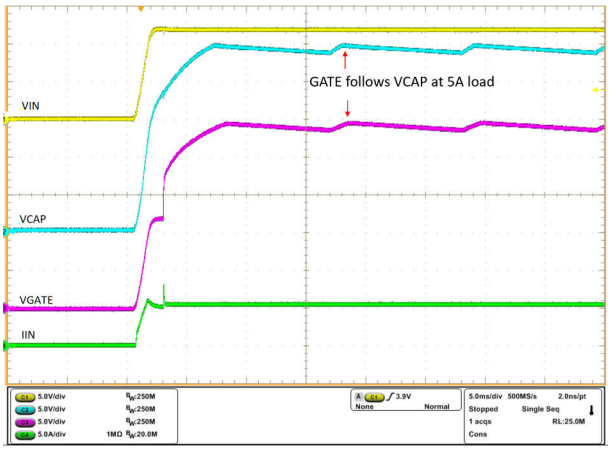
Time (2 ms/DIV)

図 10-7. Start-Up With 5-A Load



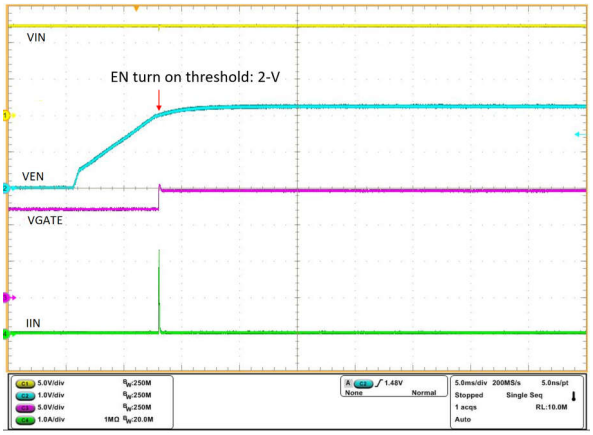
Time (5 ms/DIV)

図 10-8. VCAP During Start-Up at 3-A Load



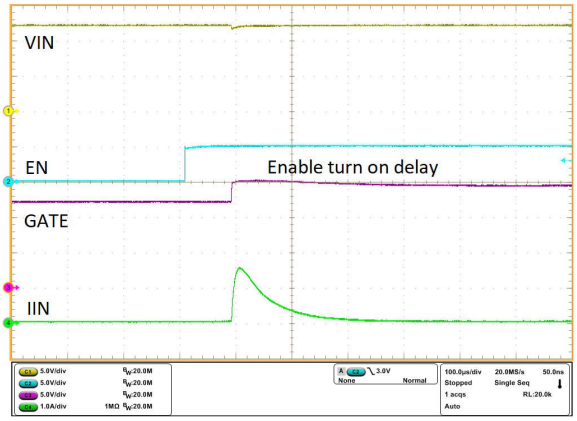
Time (5 ms/DIV)

図 10-9. VCAP During Start-Up at 5.8-A Load



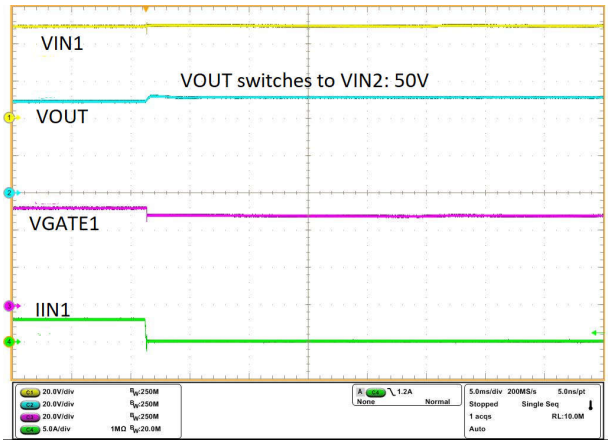
Time (5 ms/DIV)

図 10-10. Enable Threshold



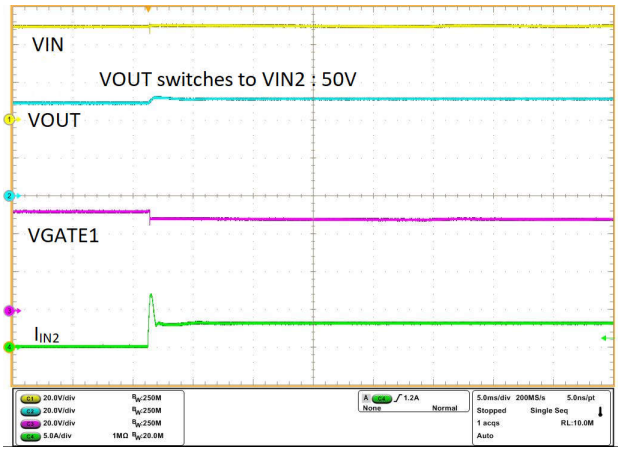
Time (100 µs/DIV)

図 10-11. Enable Turn-ON Delay



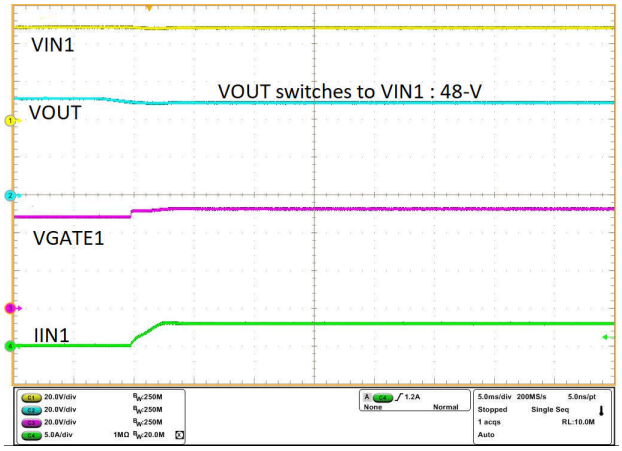
Time (5 ms/DIV)

図 10-12. OR-ing V_{IN1} to V_{IN2} Switch Over



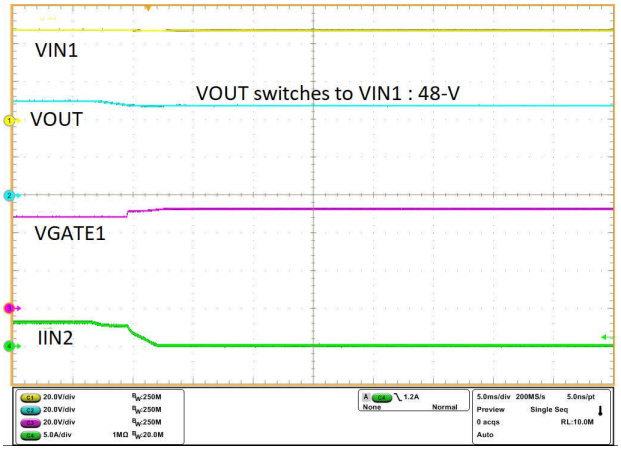
Time (5 ms/DIV)

図 10-13. OR-ing V_{IN1} to V_{IN2} Switch Over



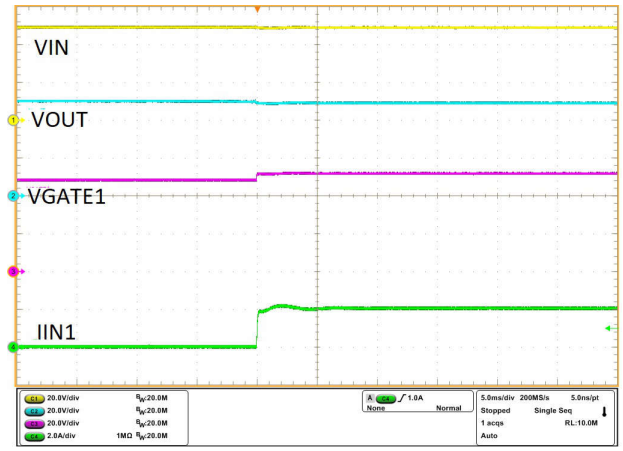
Time (5 ms/DIV)

図 10-14. OR-ing V_{IN2} to V_{IN1} Switch Over



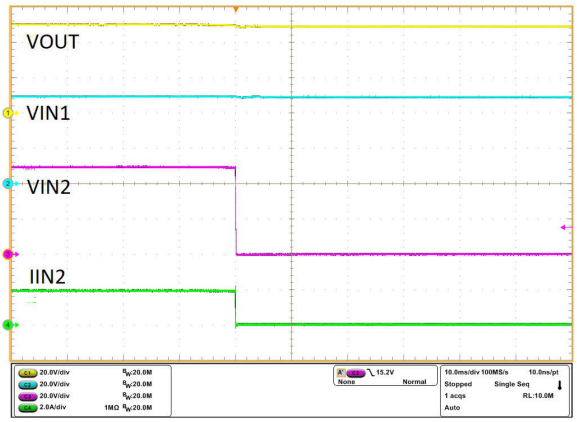
Time (5 ms/DIV)

図 10-15. OR-ing V_{IN2} to V_{IN1} Switch Over



Time (5 ms/DIV)

図 10-16. OR-ing - V_{IN2} Failure and Switch Over to V_{IN1}



Time (10 ms/DIV)

図 10-17. OR-ing - V_{IN2} Failure and Switch Over to V_{IN1}

10.2.6 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, because each diode in an OR-ing application spends most of the time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74700D-Q1 ICs combined with external N-Channel MOSFETs can be used in OR-ing Solution as shown in 図 10-18. The forward diode drop is reduced as the external N-Channel MOSFET is turned ON during normal operation. LM74700D-Q1 quickly detects the reverse current, pulls down the MOSFET gate fast, leaving the body diode of the MOSFET to block the reverse current flow. An effective OR-ing solution must be extremely fast to limit the reverse current amount and duration. The LM74700D-Q1 devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (V_{IN1}, V_{IN2}) and the common load point respectively. The source to drain voltage VDS for each MOSFET is monitored by the Anode and Cathode pins of the LM74700D-Q1. A fast comparator shuts down the Gate Drive through a fast Pull-Down within 0.45 µs (typical) as soon as $V_{(IN)} – V_{(OUT)}$ falls below –11 mV. A fast comparator turns on the Gate with 11-mA gate charge current once the differential forward voltage $V_{(IN)} – V_{(OUT)}$ exceeds 50 mV.

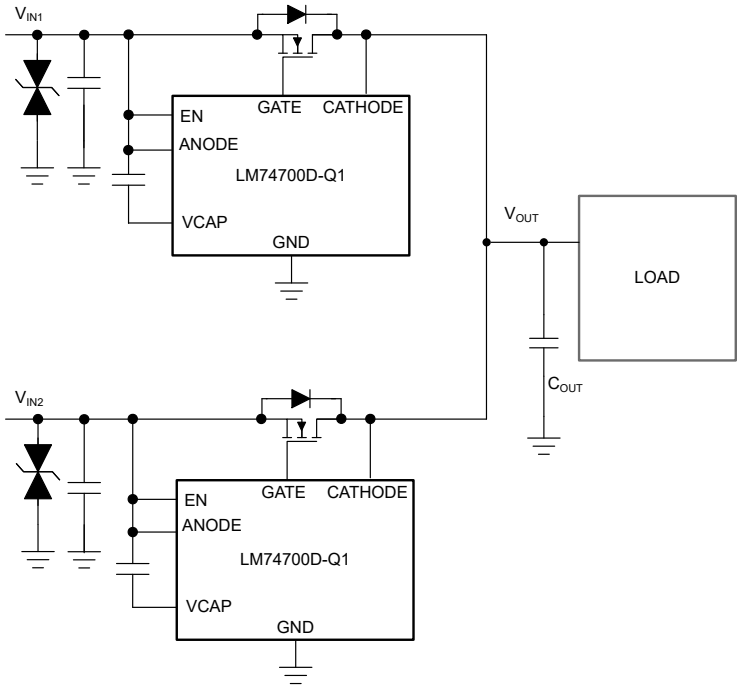


図 10-18. Typical OR-ing Application

図 10-12 to 図 10-15 show the smooth switch over between two power supply rails V_{IN1} at 48 V and V_{IN2} at 50 V. 図 10-16 and 図 10-17 illustrate the performance when V_{IN2} fails. LM74700D-Q1 controlling V_{IN2} power rail turns off quickly, so that the output remains uninterrupted and V_{IN1} is protected from V_{IN2} failure.

10.3 Power Supply Recommendations

The LM74700D-Q1 ideal diode controller is designed for the supply voltage range of 3.2 V ≤ V_{ANODE} ≤ 65 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 22 nF. To prevent LM74700D-Q1 and surrounding components from damage under the conditions of a direct output short circuit, make sure to use a power supply having over load and short-circuit protection.

10.4 Layout

10.4.1 Layout Guidelines

- Connect ANODE, GATE, and CATHODE pins of LM74700D-Q1 close to the MOSFET SOURCE, GATE, and DRAIN pins.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this design is through the MOSFET
- Keep the charge pump capacitor across VCAP and ANODE pins away from the MOSFET to lower the thermal effects on the capacitance value.
- Place input capacitor close to the device ANODE and GND pins.
- Connect the Gate pin of the LM74700D-Q1 to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and to produce good results.

10.4.2 Layout Example

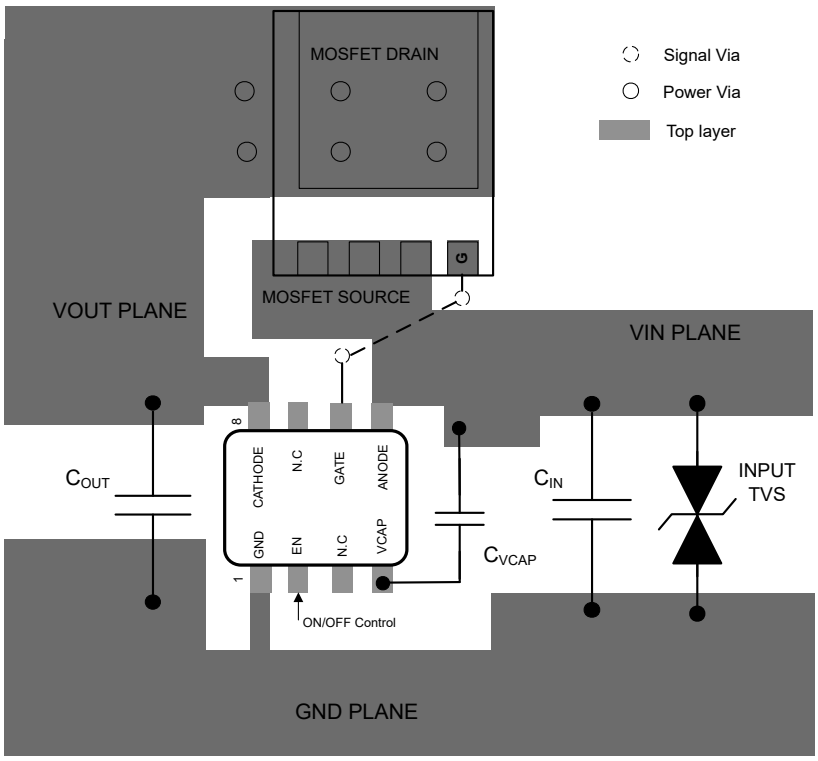


図 10-19. LM74700D-Q1 Example Layout

11 Device and Documentation Support

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 サポート・リソース

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11.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM74700QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74700Q
LM74700QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74700Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

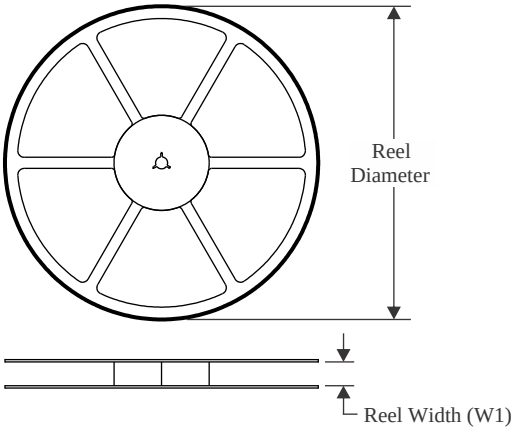
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

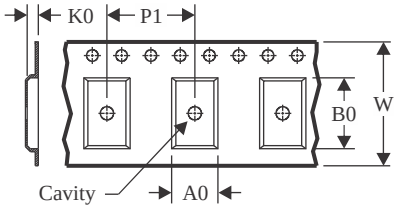
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

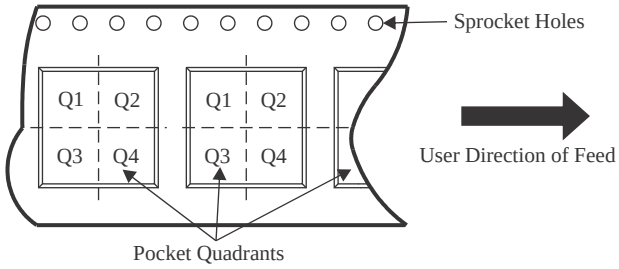


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

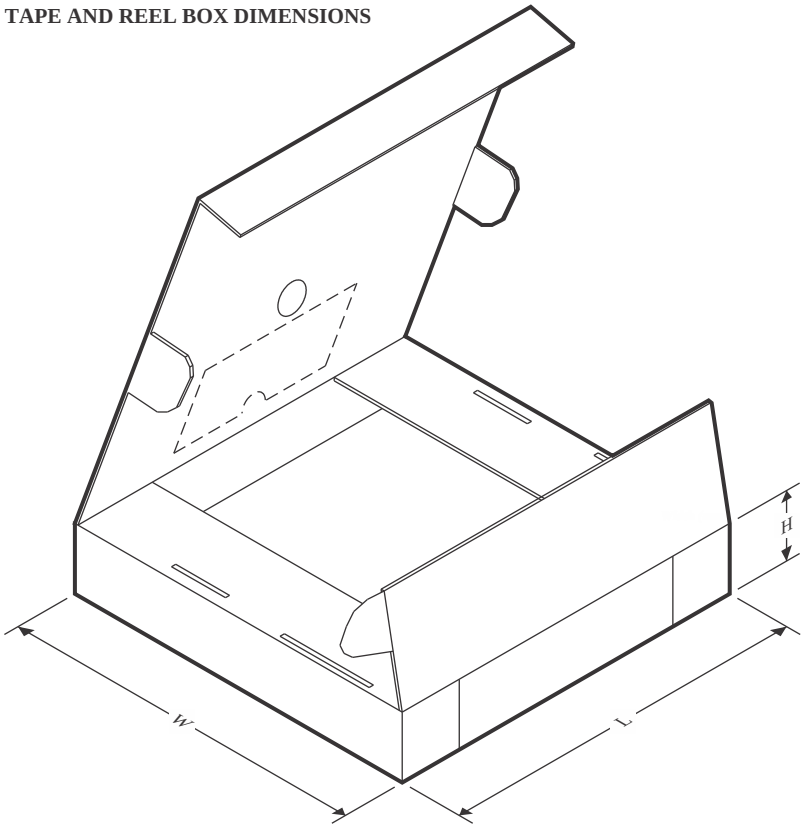
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

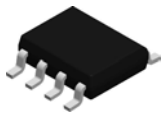
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74700QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74700QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

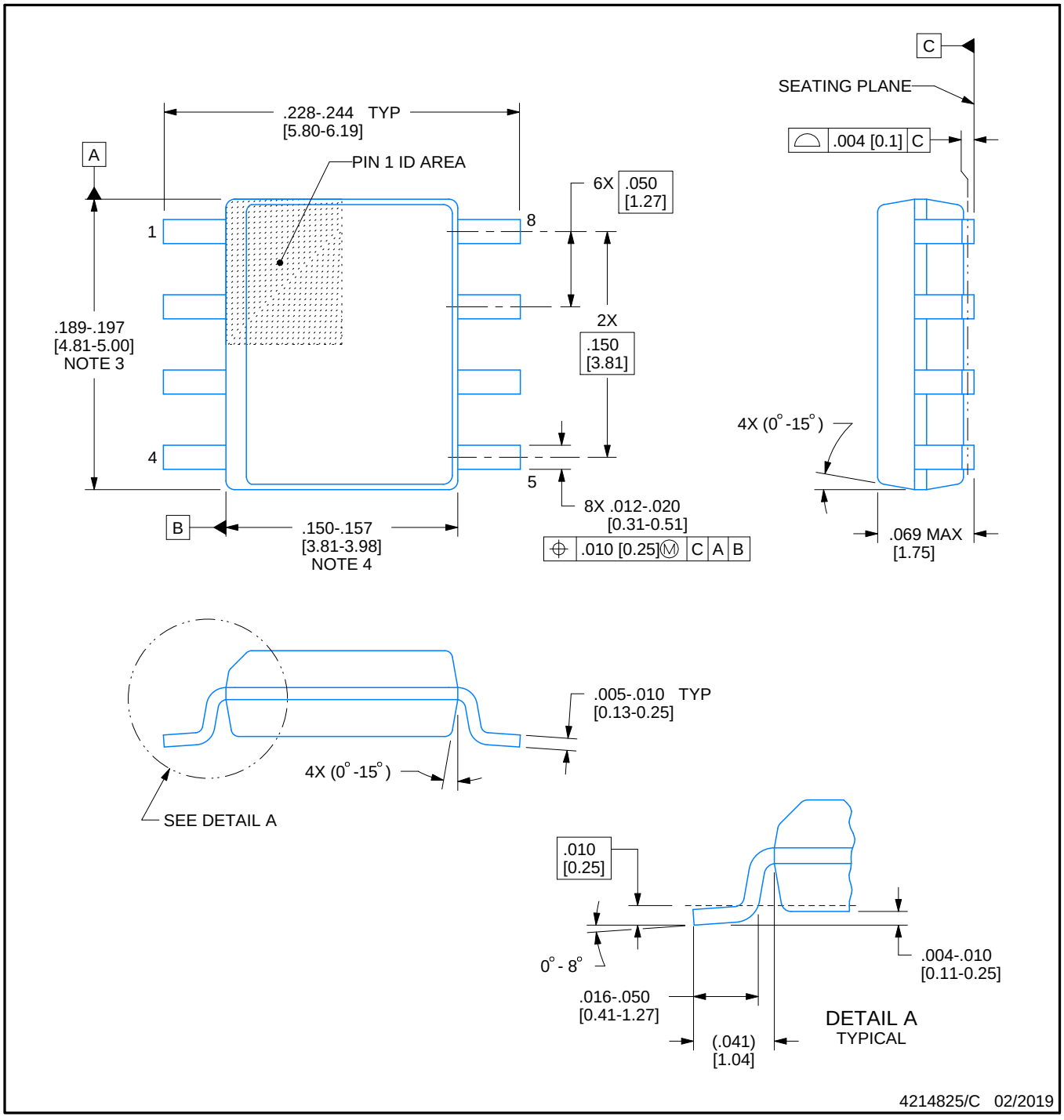


PACKAGE OUTLINE

D0008A

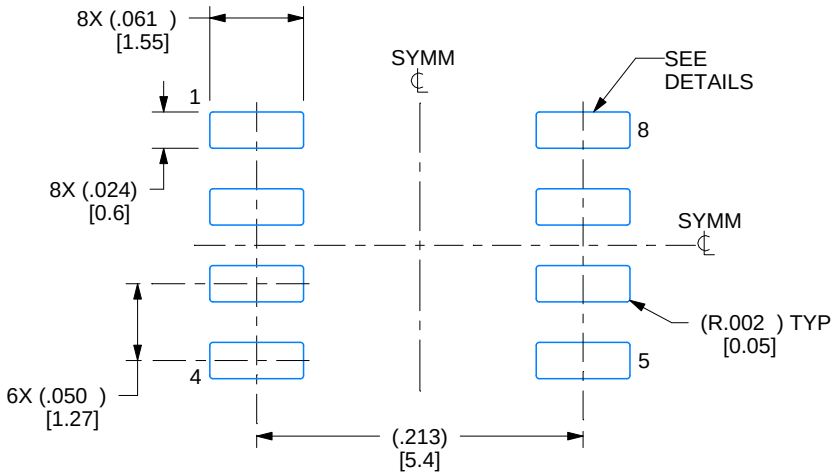
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

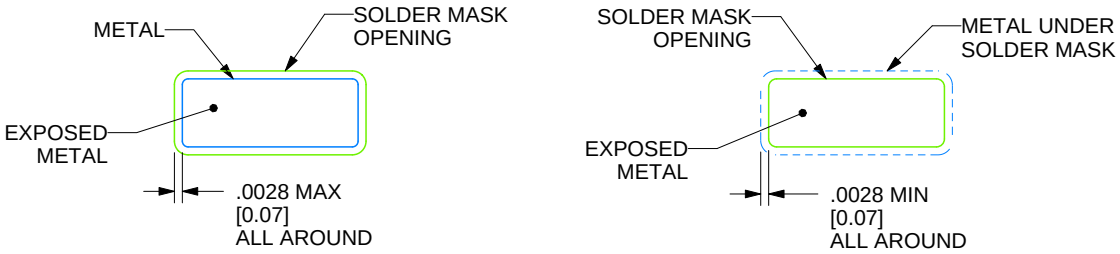


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

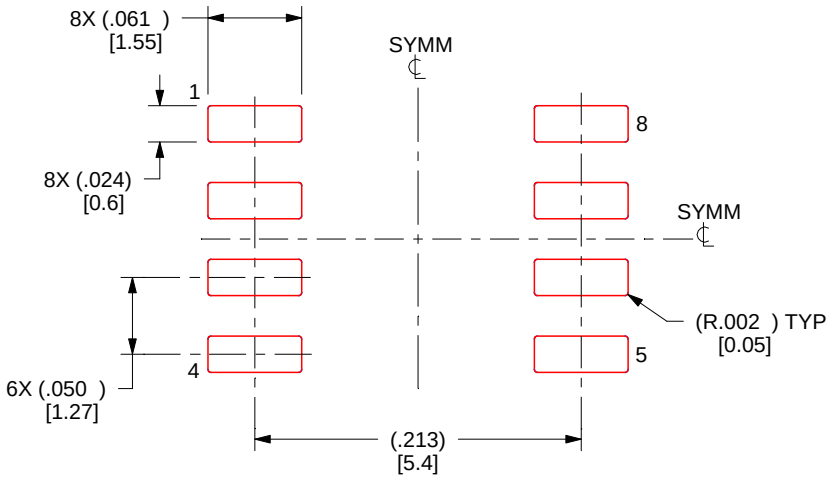
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月