TEXAS INSTRUMENTS
LM74722-Q1
JAJSJ94B – SEPTEMBER 2021 – REVISED AUGUST 2022

LM74722-Q1 車載用低 IQ 理想ダイオード・コントローラ、200kHz アクティブ整流およびロード・ダンプ保護機能搭載

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:
    –40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 3V～65V の入力範囲
- 最低 –65V までの逆入力保護
- 動作時の低い静止電流:35µA (最大値)
- 低いシャットダウン電流 (EN = LOW):3.3µA
- アノードからカソードへ 13mV の順方向電圧降下レギュレーションを行う理想ダイオード動作
- 外部のバック・ツー・バック N チャネル MOSFET を駆動
- 30mA の昇圧レギュレータを内蔵
- 最大 200 kHz のアクティブ整流
- 逆電流阻止の高速応答:0.5µs
- 高速な順方向 GATE ターンオン遅延:0.72µs
- 調整可能な過電圧保護機能
- 適切な TVS ダイオードにより車載用 ISO7637 過渡要件に適合
- 省スペースの 12 ピン WSON パッケージで供給

2 アプリケーション

- 車載用バッテリ保護
  - ADAS ドメイン・コントローラ
  - プレミアム・オーディオ・アンプ
  - ヘッド・ユニット

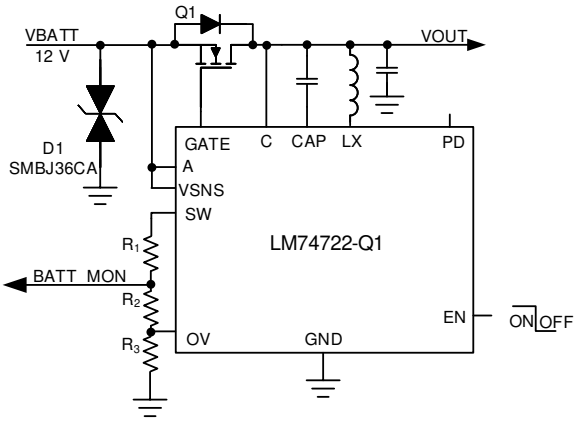
3 概要

LM74722-Q1 理想ダイオード・コントローラは外付けのバック・ツー・バック N チャネル MOSFET を駆動および制御して、電力パスの ON / OFF 制御と過電圧保護を備えた理想ダイオード整流器をエミュレートします。入力電源電圧範囲が 3V～65V と広いため、12V および 24V 車載用バッテリ駆動 ECU を保護および制御できます。このデバイスは最低 –65V の負の電源電圧に耐え、この電圧から負荷を保護できます。内蔵の理想ダイオード・コントローラ (GATE) は第 1 の MOSFET を駆動し、逆入力保護および出力電圧保持用のショットキー・ダイオードを置き換えることができます。高速ターンオン / オフ・コンパレータを搭載した強力な昇圧レギュレータは、たとえば、ECU が入力の瞬断にさらされたり、入力信号に最大 200kHz の周波数で AC が重畳されたりする、ISO16750 または LV124 などの車載テスト時に、堅牢で効率的な MOSFET スイッチング性能を確実に発揮します。動作中の静止電流が 35µA (最大値) と低いので、常時オンのシステム設計が可能になります。電力パスに第 2 の MOSFET を使えば、EN ピンを使用した負荷切断制御が可能になります。EN が LOW のとき、静止電流は 3.3µA (最大値) まで減少します。このデバイスは、OV ピンを使用して調整可能な過電圧カットオフまたは過電圧クランプ保護機能を備えています。

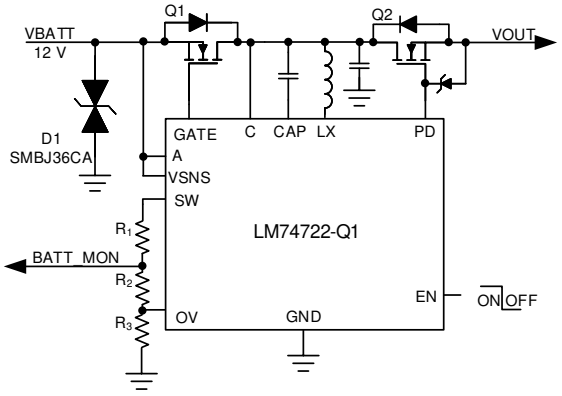
製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM74722-Q1	WSON (12)	3.00mm × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



低 IQ の理想ダイオード



スイッチ出力を備えた低 IQ の理想ダイオード

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (February 2022) to Revision B (August 2022)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

Changes from Revision * (September 2021) to Revision A (February 2022)	Page
• データシートのタイトルを更新	1
• Updated the *Load Disconnect Switch Control (PD)* description	11

5 Pin Configuration and Functions

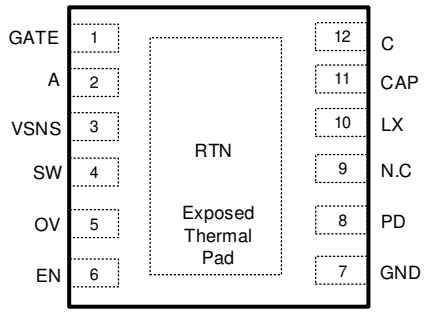


図 5-1. WSON 12-Pin DRR Transparent Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	LM74722-Q1 DRR-12 (WSON)		
GATE	1	O	Diode controller gate drive output. Connect to the GATE of the external MOSFET.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET.
VSNS	3	I	Voltage sensing input
SW	4	I	Voltage sensing disconnect switch terminal. VSNS and SW connect internally through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line, thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used, then short them together and connect to C pin.
OV	5	I	Adjustable overvoltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OV exceeds the over voltage cut-off threshold, then the PD is pulled low turning OFF the HSFET. PD is driven high when the sense voltage goes below the OV falling threshold.
EN	6	I	EN input. Connect to A or C pin for always ON operation. In this mode, the device consumes an IQ of 35 µA (maximum) that can be driven externally from a micro controller I/O. Pulling this pin low below 0.3 V enters the device in low Iq shutdown mode.
GND	7	G	Connect to the system ground plane.
PD	8	O	Pull down connection for the external HSFET. Connect to the GATE of the external FET. Keep PD pin floating when not used.
N.C	9	I	No connect
LX	10	I	Switch node of the internal boost regulator. This node must be kept small on the PCB for good performance and low EMI. Connect the boost inductor between this pin and the DRAIN connection of the external FET.
CAP	11	O	Boost regulator output. This pin is used to provide a drive voltage to the gate driver of the ideal diode stage as well as drive supply for the HSFET. Connect a 1-µF capacitor between this pin and the DRAIN connection of the external FET.
C	12	I	Cathode of the ideal diode and supply voltage pin. Connect to the DRAIN of the external MOSFET. The voltage sensed at this pin is used to control the external MOSFET GATE. This pin must be locally bypassed with at least 1 µF.
RTN	Thermal Pad	—	Leave exposed pad floating. Do not connect to GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	–65	70	V
Input Pins	C to GND	–0.3	70	V
Input Pins	VSNS, SW, EN, OV to GND, $V_{(A)} > 0$ V	–0.3	70	V
Input Pins	VSNS, SW, EN, OV to GND, $V_{(A)} \leq 0$ V	$V_{(A)}$	(70 + $V_{(A)}$)	V
Input Pins	RTN to GND	–65	0.3	V
Input Pins	I_{VSNS}, I_{SW}	–1	10	mA
Input Pins	I_{EN}, I_{OV}, $V_{(A)} > 0$ V	–1		mA
Input Pins	I_{EN}, I_{OV}, $V_{(A)} \leq 0$ V	Internally limited		
Output Pins	CAP to C	–0.3	15.9	V
Output Pins	CAP to A	–0.3	85	V
Output Pins	GATE to A	–0.3	15	V
Output Pins	LX, CAP, PD to GND	–0.3	85	V
Output to Input Pins	C to A	–5	85	V
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GATE, EN, GND, C)	±750	
			Other pins	±500	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
	C to GND			65	
	EN to GND	–60		65	
External capacitance	A	0.1			µF
	VS, C, CAP to C	1			µF
External Inductor	LX	100			µH
External MOSFET max V_{GS} rating	GATE to A	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM74722-Q1 DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.7	°C/W
$R_{\theta JC}$	Junction-to-case (botton) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)} = V_{(C)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_A SUPPLY VOLTAGE						
$V_{(A\ POR)}$	VA POR Rising threshold		3.1	3.4	3.85	V
	VA POR Falling threshold		2.2	2.6	2.9	
$V_{(C)}$	Minimum voltage at C				3	
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		1.5	3.3	µA
$I_{(Q)}$	Total System Quiescent Current	$V_{(EN)}$ = 2 V, Active Rectifier Controller In Regulation, –40°C ≤ T_J ≤ +85°C		27	32	
		$V_{(EN)}$ = 2 V, Active Rectifier Controller In Regulation, –40°C ≤ T_J ≤ +125°C		27	35	
ENABLE INPUT						
$V_{(EN\_IH)}$	Enable input high threshold				2	V
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.85	1.2	
$V_{(EN\_Hys)}$	Enable Hysteresis			485		mV
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		55	155	nA
V_{ANODE} to $V_{CATHODE}$						
$V_{(AC\ REG)}$	Regulated Forward $V_{(AC)}$ Threshold		7.5	12.8	18.7	mV
$V_{(AC\_FWD)}$	$V_{(AC)}$ threshold from RCB to oFCB		75	105	140	
$V_{(AC\_REV)}$	$V_{(AC)}$ threshold for reverse current blocking		–12	–5.6	–1.3	
GATE DRIVE						
$V_{(GATE)}$ - $V_{(A)}$		3 V < $V_{(C)}$ < 65 V	9.5		13	V
$I_{(GATE)}$	Regulation max sink current	$V_{(A)} – V_{(C)}$ = 0 V, $V_{(GATE)} – V_{(A)}$ = 5 V	8.5	22	39	µA
	Peak Pull down current	$V_{(A)} – V_{(C)}$ = –20 mV		2.5		A
R_{GATE}	GATE pull down resistance	$V_{(A)} – V_{(C)}$ = –20 mV, $V_{(GATE)} – V_{(A)}$ = 100 mV		1.2		Ω
BOOST REGULATOR CHARGE PUMP						
$V_{(CAP)} – V_{(C)}$	Boost output rising threshold			13	15.5	V
	Hysteresis			1.1		

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CAP)}$	Boost load capacity	$V_{(CAP)} – V_{(C)}$ = 7.5 V		29		mA
$I_{(LX)}$	Peak Inductor current limit	$V_{(C)}$ = 12 V	110	140	175	
		$V_{(C)}$ = 3 V			210	
$R_{(LX)}$	Low side switch on-resistance		1.3	2.7	5.1	Ω
BATTERY SENSING (VSNS, SW) AND OVER VOLTAGE DETECTION (OVP, PD)						
$R_{(SW)}$	Battery sensing disconnect switch resistance		104	226	430	Ω
$V_{(OVR)}$	Overvoltage threshold input, risIng		1.13	1.231	1.33	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.03	1.125	1.215	V
$V_{(OV\_Hys)}$	OV Hysteresis			110		mV
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 5 V		50	110	nA
$I_{(PD\_SRC)}$	Pull up current	3 V < $V_{(C)}$ < 65 V	43	50	60	µA
$I_{(PD\_SINK,Pk)}$	Peak Pull down current	$V_{(OV)}$ > $V_{(OVR)}$	55	88	117	mA
$I_{(PD\_SINK,DC)}$	DC Pull down current		7	10	14	mA
CATHODE						
$V_{(C)}$	C POR Rising		2.58	2.8	2.95	V
	C POR Falling		2.35	2.6	2.85	
$I_{(C)}$	C sink current	$V_{(A)}$ = 12 V, $V_{(A)} – V_{(C)}$ = –100 mV		8.5	15	µA
		$V_{(A)}$ = –14 V, $V_{(C)}$ = 14 V		12.8	18	

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(C)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{A\_POR(DLY)}$	A (low to high) to GATE turn-on delay	$V_{(A)}$ ↑ V(A POR) to $V_{(GATE – A)}$ > 5 V, $C_{((GATE – A)}$ = 10 nF			200	µs
$t_{GATE\_ON(DLY)}$	Forward voltage detection to GATE turn-on delay	$V_{(A)} – V_{(C)}$ = –100 mV to 700 mV, $V_{(GATE – A)}$ > 5 V, $C_{((GATE – A)}$ = 10 nF		0.72	1.25	µs
		$V_{(A)} – V_{(C)}$ = –100 mV to 700 mV, $V_{(GATE – A)}$ > 5 V, $C_{((GATE – A)}$ = 30 nF		1.02	1.9	µs
$t_{GATE\_OFF(DLY)}$	Reverse voltage detection to GATE turn-off delay	$V_{(A)} – V_{(C)}$ = +30 mV to –100 mV, $V_{(GATE – A)}$ < 1 V, $C_{((GATE – A)}$ = 10 nF		0.46	0.65	µs
$t_{EN\_OFF(DLY)PD}$	EN to PD Delay	EN ↓ to PD ↓		6.5	12	µs
$t_{OV\_OFF(DLY)PD}$	OV to PD Deglitch	OV ↑ to PD ↓		0.9	1.5	µs
t_{PD_Pk}	Peak Pull Down duration	$I_{(PD\_SINK,Pk)}$ ↑ to $I_{(PD\_SINK,DC)}$ ↓	11	38	65	µs

6.7 Typical Characteristics

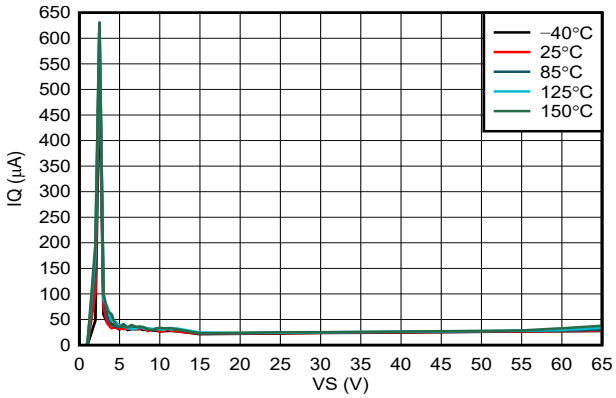


図 6-1. Operating Quiescent Current vs Supply Voltage

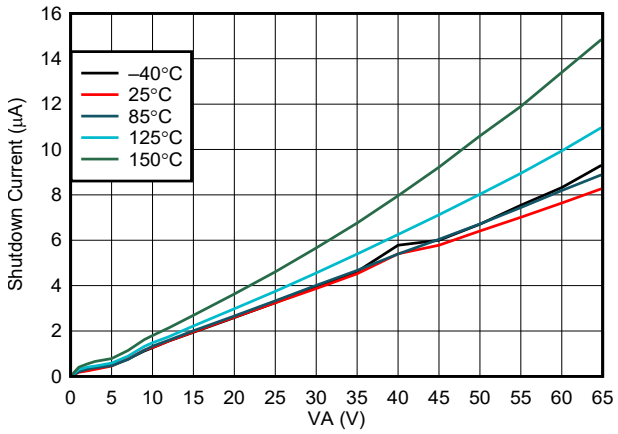


図 6-2. Shutdown Supply Current vs Supply Voltage

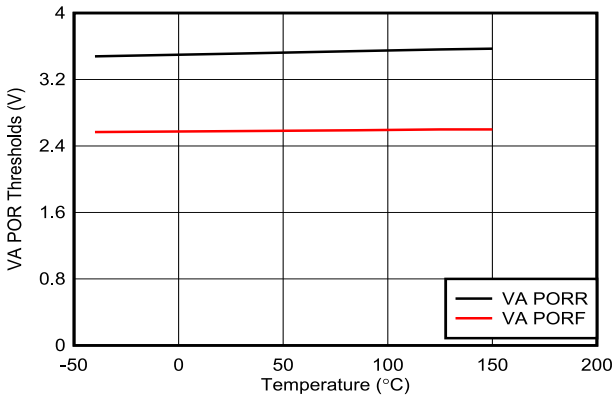


図 6-3. VA POR Threshold vs Temperature

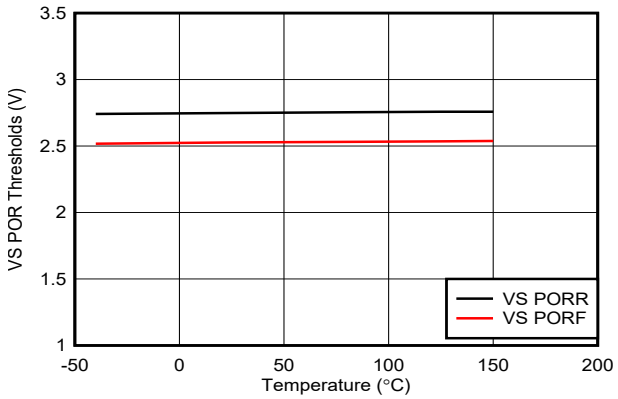


図 6-4. VS POR Threshold vs Temperature

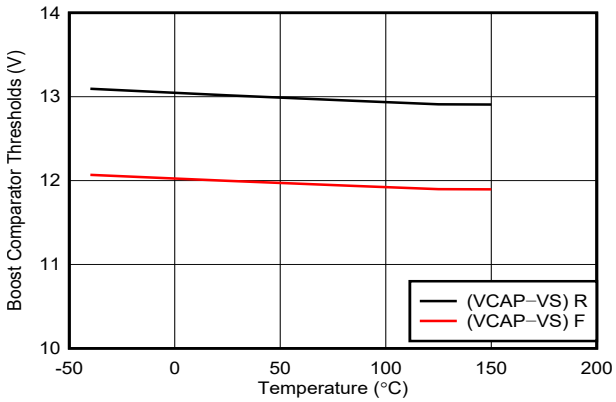


図 6-5. Boost Comparator Threshold vs Temperature

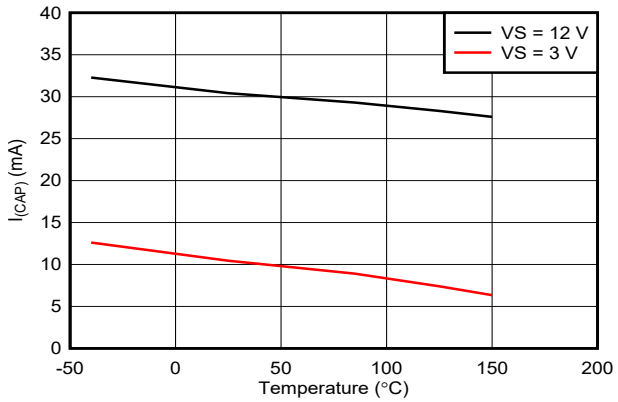


図 6-6. Boost Loading Capacity vs Temperature

6.7 Typical Characteristics (continued)

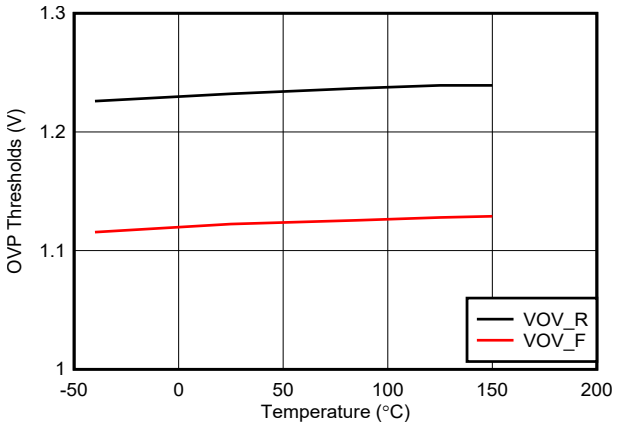


図 6-7. OV Threshold vs Temperature

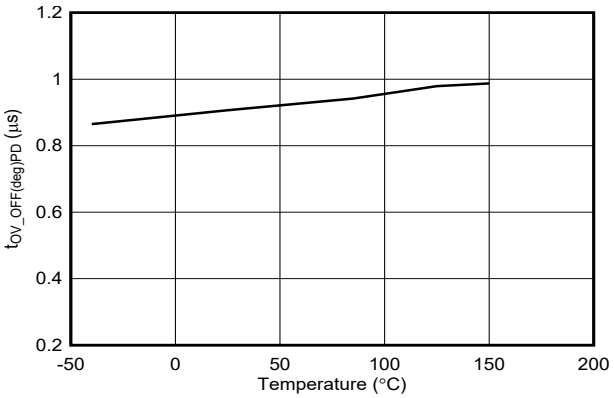


図 6-8. PD Turn-Off Delay During OV

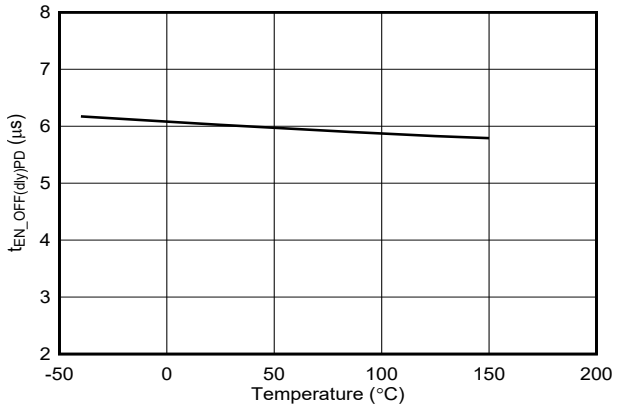


図 6-9. PD Turn-Off Delay During EN

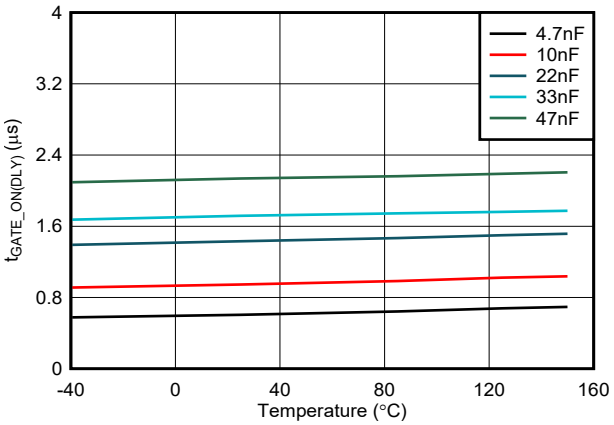


図 6-10. Forward Turn-On Delay vs Temperature

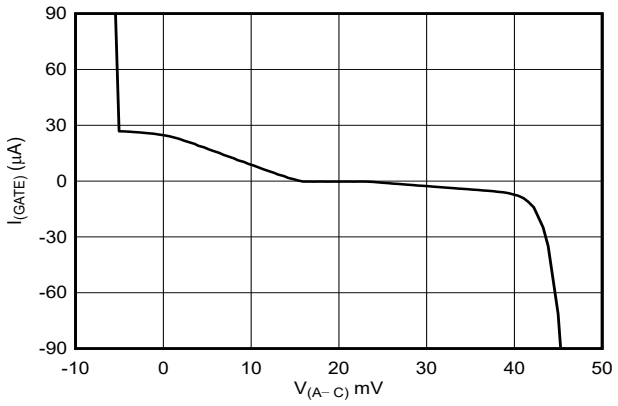


図 6-11. Gate Current vs Forward Voltage Drop

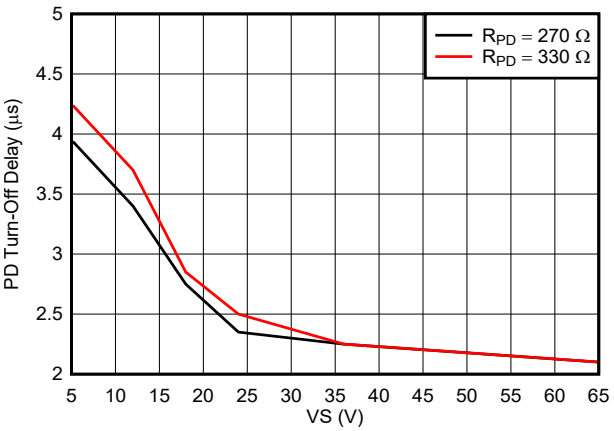


図 6-12. PD Turn-Off Delay vs Supply Voltage

7 Parameter Measurement Information

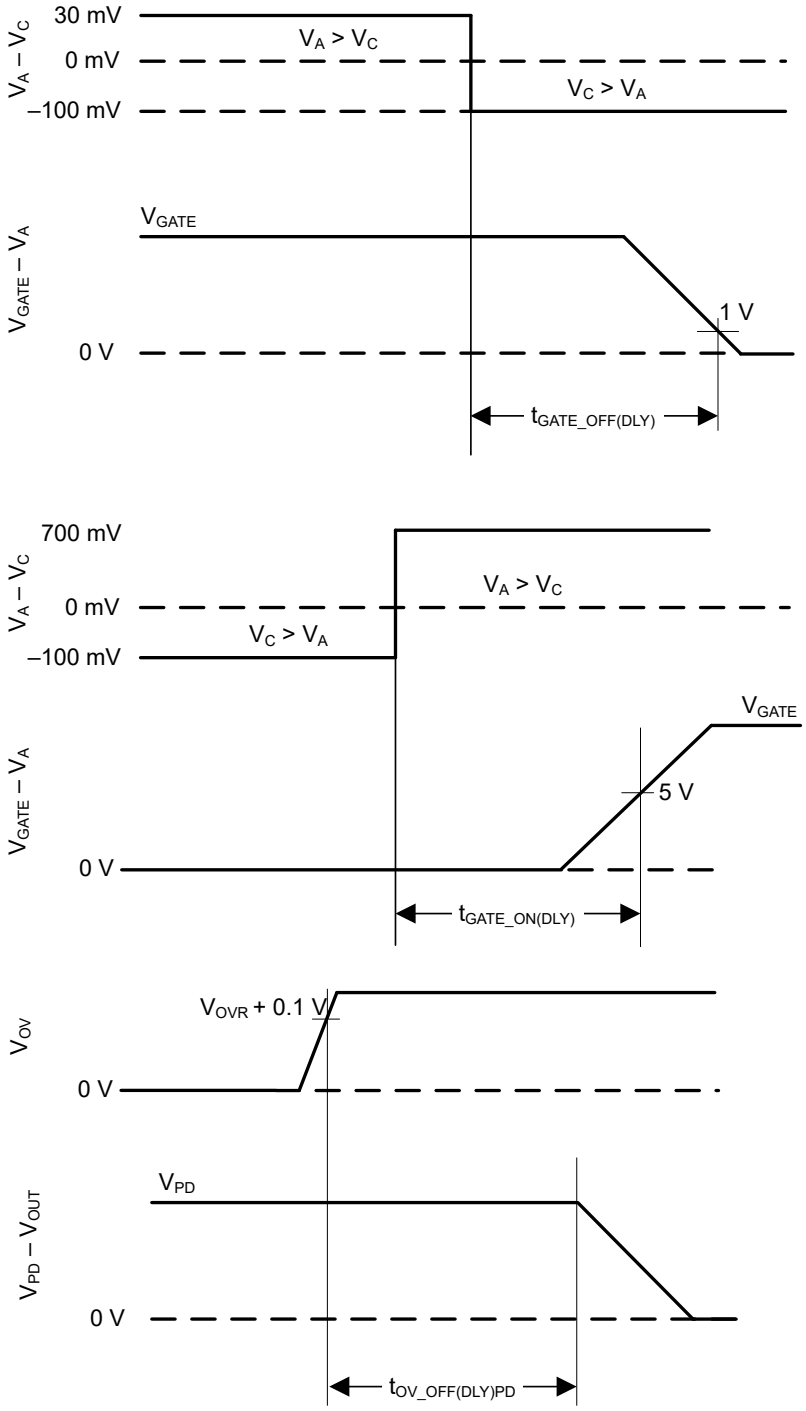


図 7-1. Timing Waveforms

8 Detailed Description

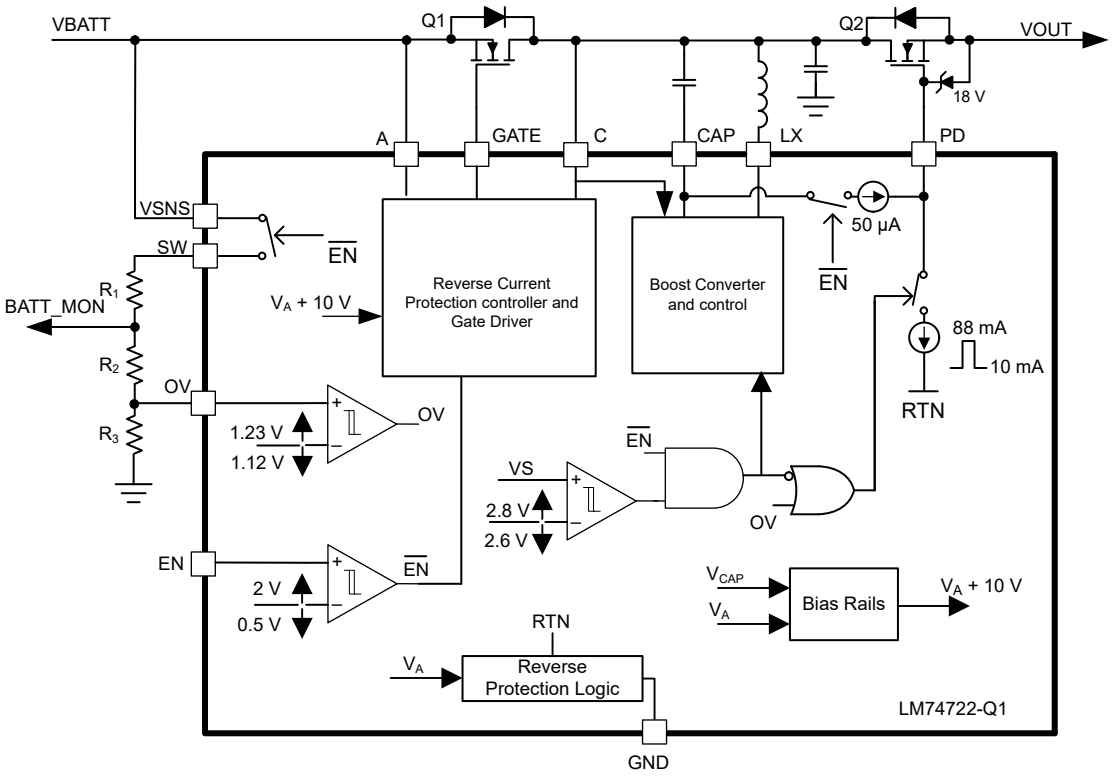
8.1 Overview

The LM74722-Q1 ideal diode controller drives and controls external back-to-back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON and OFF control and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery powered ECUs. IQ during operation (EN = High) is < 35 µA and < 3.3 µA during shutdown mode (EN = Low). The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (GATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong 30-mA boost regulator and short turn-ON and turn-OFF delay times of comparators ensures fast transient response ensuring robust and efficient MOSFET switching performance during automotive testing, such as ISO16750 or LV124, where an ECU is subjected to input short interruptions and AC superimpose input signals up to 200-kHz frequency. The device features an adjustable overvoltage cutoff protection feature for load dump protection.

The LM74722-Q1 controls the GATE of the MOSFET Q1 to regulate the forward voltage drop at 13 mV. The linear regulation scheme in these devices enables graceful control of the GATE voltage and turns off of the MOSFET during a reverse current event and ensures zero DC reverse current flow.

LM74722-Q1 PD gate drive can be used to drive load disconnect MOSFET (Q2). The back to back connected MOSFET configuration can be used when system requires overvoltage protection, inrush current protection or output load disconnect function.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Dual Gate Control (GATE, PD)

The LM74722-Q1 features two separate gate control and driver outputs. That is, GATE and PD to drive back-to-back N-channel MOSFETs.

8.3.1.1 Reverse Battery Protection (A, C, GATE)

A, C, GATE comprises of the ideal diode stage. Connect the source of the external MOSFET to A, drain to C and gate to GATE pin. The LM74722-Q1 has integrated reverse input protection down to –65 V.

In LM74722-Q1, the voltage drop across the MOSFET is continuously monitored between the A and C pins. The GATE to A voltage is adjusted as needed to regulate the forward voltage drop at 13 mV (typical). This closed loop regulation scheme enables graceful turn-off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74722-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{(AC\_REV)}$ threshold, then the GATE goes low within 0.5 µs (typical). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits the $V_{(AC\_FWD)}$ threshold within 0.72 µs (typical). As shown in 図 8-1, for ideal diode only designs, connect LM74722-Q1.

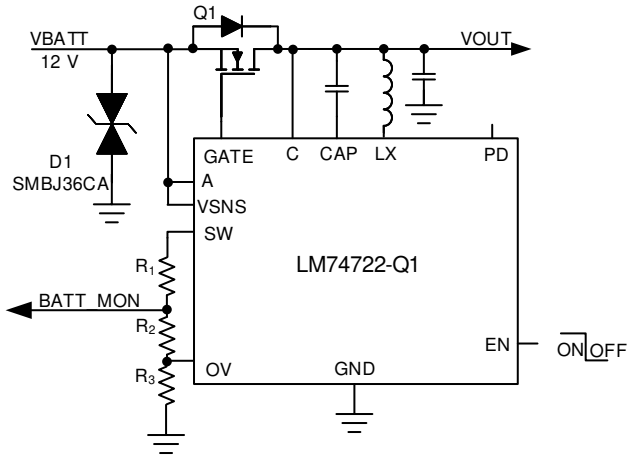


図 8-1. Configuring LM74722-Q1 for Ideal Diode Only

8.3.1.2 Load Disconnect Switch Control (PD)

The PD pin provides a 50-µA drive and 88-mA peak pulldown strength for the load disconnect switch stage. Connect the Gate of the FET to PD pin. Place a 18-V Zener (Dz) across the FET gate and source.

For inrush current limiting, connect C_{dVdT} capacitor and R_1 as shown in 図 8-2.

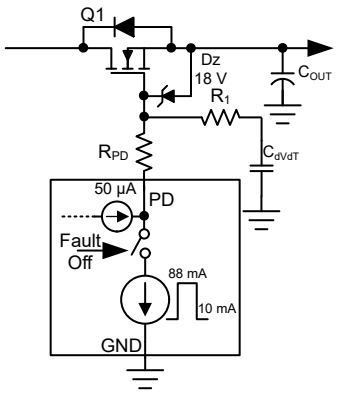


図 8-2. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the PD voltage ramp during power up for inrush current limiting. Use 式 1 to calculate C_{dVdT} capacitance value.

$$C_{dVdT} = \frac{I_{PD\_DRV} \times C_{OUT}}{I_{INRUSH}} \quad (1)$$

where I_{PD_DRV} is 50 µA (typical), I_{INRUSH} is the inrush current, and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn-off time.

PD is pulled low during the following conditions:

- During an OV event with the OV pin voltage rising above the $V_{(OVR)}$ threshold
- When the EN pin is pulled low with $V_{(EN)}$ driven lower than $V_{(EN\_IL)}$ level
- When the voltage at VS pin drops below the $V_{(VS\ POR)}$ falling threshold

During these conditions, the FET Q1 turns OFF with its GATE connected to its SOURCE terminal through the external Zener (Dz).

Use 式 2 to the peak power dissipated in the LM74722-Q1 at the instance of PD pulldown.

$$P_{PD\_peak} = V_{OUT} \times I_{PD\_SINK} \quad (2)$$

where

- I_{PDSINK_peak} is the peak sink current of 88 mA (typical)

In the system designs with input voltage above 48 V, TI recommends to place a resistor, R_{PD}, in series with the PD pin as shown in 図 8-2. The peak power dissipation during the pulldown events gets distributed in R_{PD} and the internal PD switch. A resistor value in the range of 270 Ω to 330 Ω can be selected to limit the device power dissipation within the safe limits.

8.3.1.3 Overvoltage Protection and Battery Voltage Sensing (VSNS, SW, OV)

A disconnect switch is integrated between VSNS and SW pins. When the device is enabled, this internal switch allows input voltage monitoring by connecting a resistor divider from SW pin to GND. This switch is turned OFF when EN pin is pulled low. This action helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

LM74722-Q1 has an OV pin which can be used to design overvoltage cutoff (OV setpoint referred to input side, VIN) or overvoltage clamp functionality (OV setpoint referred to output side, VOUT).

図 8-3 shows a typical resistor ladder connection for battery voltage sensing and overvoltage threshold programming.

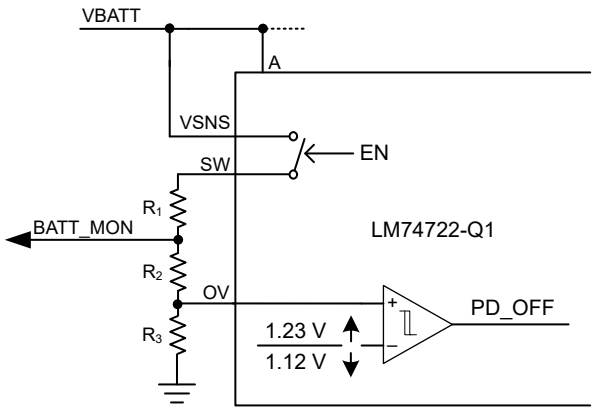


図 8-3. Programming Overvoltage Threshold and Battery Voltage Sensing

8.3.2 Boost Regulator

The LM74722-Q1 integrates a boost converter to provide voltage necessary to drive the external N-channel MOSFETs for the ideal diode and the load disconnect stages. Place a 1-µF capacitor across drain of the FET to GND and across the CAP pin to drain of the FET. Use a 100-µH inductor with saturation current rating > 175 mA. For the boost converter to be enabled, the EN pin voltage must be above the specified input high threshold, $V_{(ENR)}$. The boost converter has a maximum output load capacity of 30-mA typical. If EN pin is pulled low, then the boost converter remains disabled.

8.4 Device Functional Modes

Shutdown Mode

The LM74722-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold, $V_{(EN\_IL)}$. Both the gate drivers (GATE and PD) and the boost regulator are disabled in shutdown mode. During shutdown mode, the LM74722-Q1 enters low IQ operation with a total input quiescent consumption of 1.5 µA (typical).

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

LM74722-Q1 controls two N-channel power MOSFETs with GATE used to control diode MOSFET to emulate an ideal diode and PD controlling second MOSFET for power path cutoff when disabled or during an overvoltage protection and provide inrush current limiting. IQ during operation (EN = High) is < 38 µA and < 3.5 µA during shutdown mode (EN = Low). LM74722-Q1 can be placed into low quiescent current mode using EN = low, where both GATE and PD are turned OFF.

9.2 Typical 12-V Reverse Battery Protection Application

図 9-1 shows a typical application circuit of LM74722-Q1 configured to provide reverse battery protection with overvoltage protection and inrush current limiting.

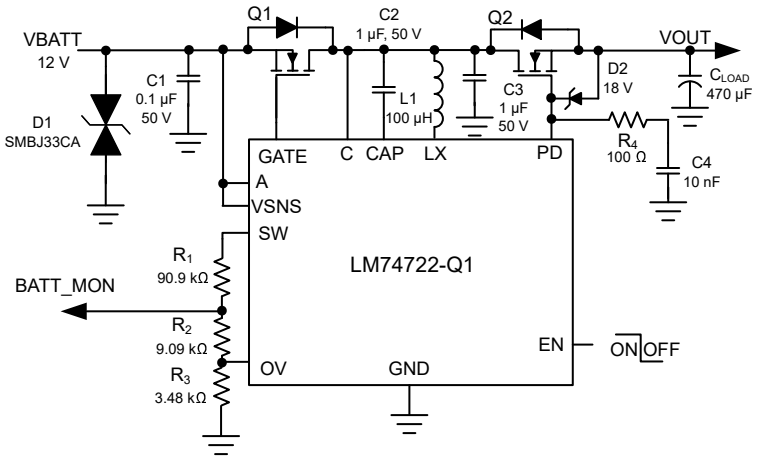


図 9-1. Typical Application Circuit – 12-V Reverse Battery Protection and Overvoltage Protection

9.2.1 Design Requirements for 12-V Battery Protection

表 9-1 lists the system design requirements.

表 9-1. Design Parameters - 12-V Reverse Battery Protection and Overvoltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output power	50 W
Output current range	4-A nominal, 5-A maximum
Input capacitance	0.1-µF minimum
Output capacitance	0.1-µF minimum, (optional 220 µF for E-10 functional class A performance)
Overvoltage cutoff	37 V, output cutoff > 37 V
AC super imposed test	2-V peak-peak 100 kHz
Automotive transient immunity compliance	ISO 7637-2, ISO 16750-2 and LV124
Battery monitor ratio	8:1

9.2.1.1 Automotive Reverse Battery Protection

9.2.1.1.1 Input Transient Protection: ISO 7637-2 Pulse 1

ISO 7637-2 pulse 1 specifies negative transient immunity of electronic modules connected in parallel with an inductive load when the battery is disconnected. A typical pulse 1 specified in ISO 7637-2 starts with battery disconnection where supply voltage collapses to 0 V followed by –150 V 2 ms applied with a source impedance of 10 Ω at a slew rate of 1 µs on the supply input. LM74722-Q1 blocks reverse current and prevents the output voltage from swinging negative, protecting the rest of the electronic circuits from damage due to negative transient voltage. MOSFET Q1 is quickly turned off within 0.5 µs by fast reverse comparator of LM74722-Q1. A single bidirectional TVS is required at the input to clamp the negative transient pulse within the operating maximum voltage across cathode to anode of 85 V and does not violate the MOSFET Q1 drain-source breakdown voltage rating.

図 9-2 shows ISO 7637-2 pulse 1 performance of LM74722-Q1.

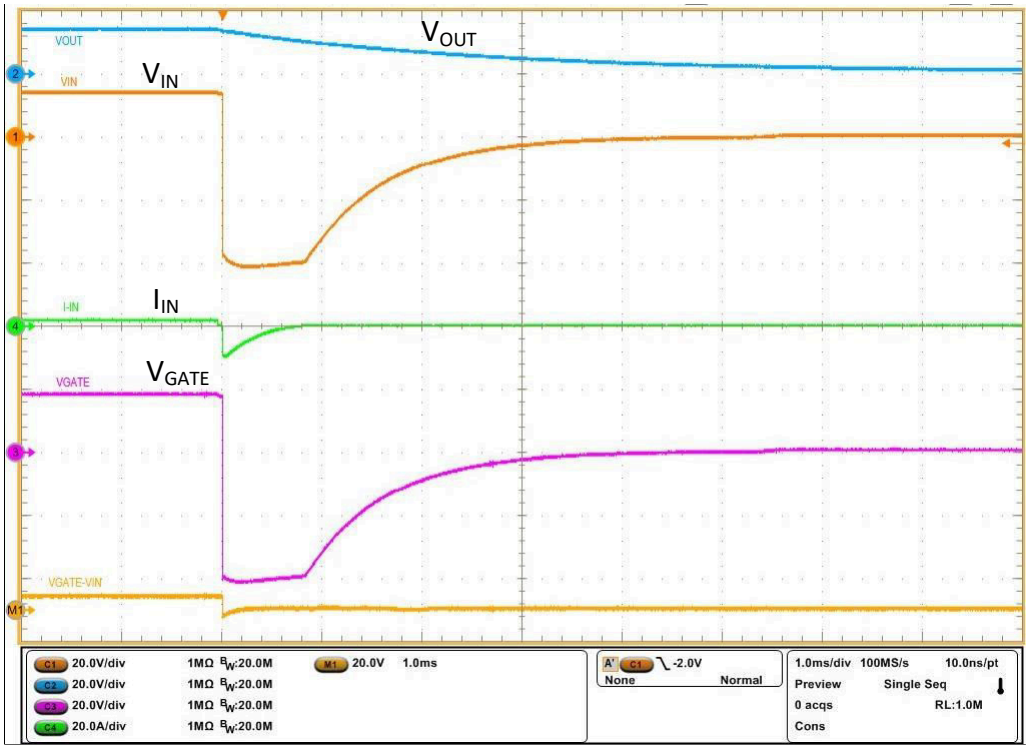


図 9-2. Performance During ISO 7637-2 Pulse 1 Test

9.2.1.1.2 AC Super Imposed Input Rectification: ISO 16750-2 and LV124 E-06

Alternators are used to power the automotive electrical system and charge the battery during normal run time of the vehicle. Rectified alternator output contains residual AC ripple voltage superimposed on the DC battery voltage due to various reasons. These reasons include engine speed variation, regulator duty cycle with field switching ON and OFF, and electrical load variations. On a 12-V battery supply, alternator output voltage is regulated by a voltage regulator between 14.5 V to 12.5 V by controlling the field current of alternator rotor. All electronic modules are tested for proper operation with superimposed AC ripple on the DC battery voltage. AC super imposed test specified in ISO 16750-2 and LV124 E-06 requires AC ripple of 2-V peak-peak on a 13.5-V DC battery voltage, swept from 15 Hz to 30 kHz. LM74722-Q1 rectifies the AC superimposed voltage by turning the MOSFET Q1 OFF quickly to cut off reverse current and turning the MOSFET Q1 ON quickly during forward conduction. 図 9-3 shows active rectification of 6-V peak-peak 100-kHz AC input by LM74722-Q1. Fast turn-off and quick turn-on of the MOSFET reduces power dissipation in the MOSFET Q1, and active rectification reduces power dissipation in the output hold-up capacitor ESR by half. 図 9-4 shows active rectification of 2-V peak-peak 200-kHz AC input.

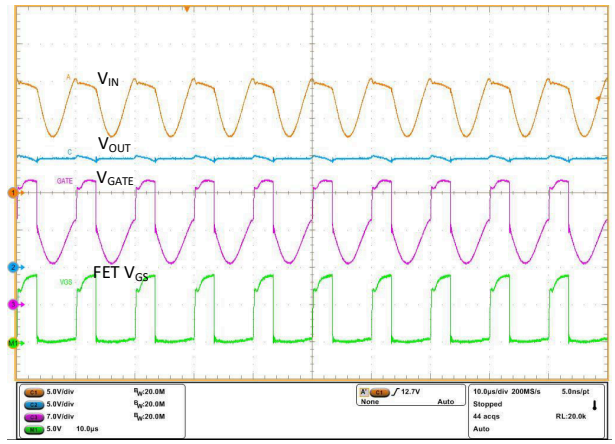


図 9-3. AC Super Imposed Test - 6-V Peak-Peak 100 kHz

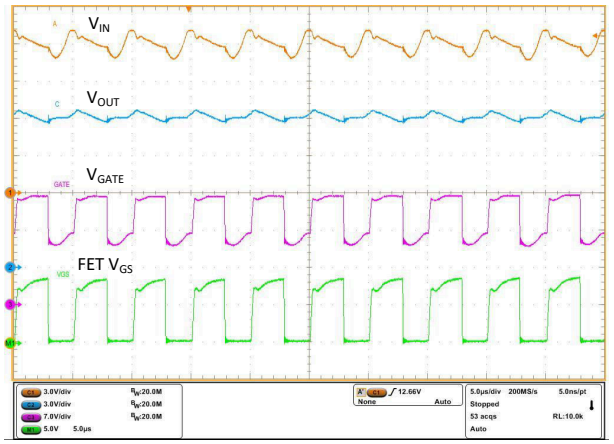


図 9-4. AC Super Imposed Test - 2-V Peak-Peak 200 kHz

9.2.1.1.3 Input Micro-Short Protection: LV124 E-10

E-10 test specified in LV124 standard checks for immunity of electronic modules to short interruptions in power supply input due to contact issues or relay bounce. During this test (case 2), micro-short is applied on the input for a duration as low as 10 µs to several ms. For a functional pass status A, electronic modules are required to run uninterrupted during the E-10 test (case 2) with 100-µs duration. When input micro-short is applied for 100 µs, LM74722-Q1 quickly turns off MOSFET Q1 by shorting GATE to ANODE (source of MOSFET) within 0.5 µs to prevent the output from discharging and the PD remains ON keeping MOSFET Q2 ON, enabling fast recovery after the input short is removed.

図 9-5 shows performance of LM74722-Q1 during E10 input power supply interruption test case 2. After the input short is removed, input voltage recovers and MOSFET Q1 is turned back ON within 200 µs. Note that dual-gate drive topology allows MOSFET Q2 to remain ON during the test and helps in restoring the input power faster. Output voltage remains unperturbed during the entire duration, achieving functional status A.

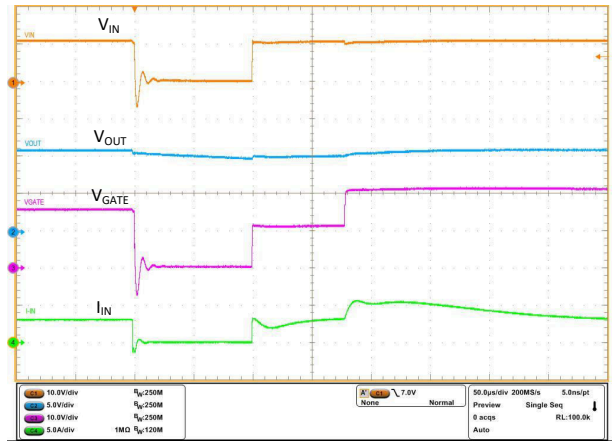


図 9-5. Input Micro-Short – LV124 E10 TC 2 100 µs

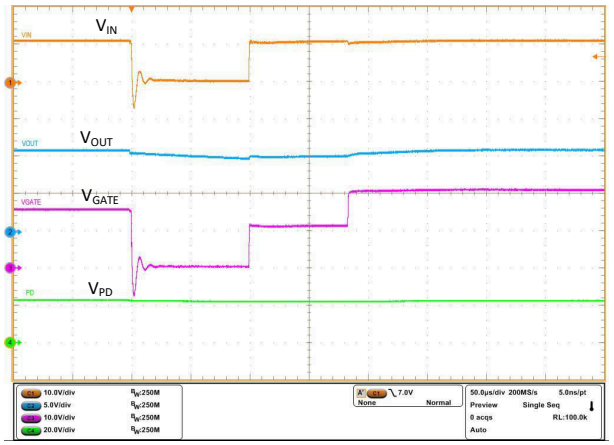


図 9-6. Input Micro-Short – LV124 E10 TC 2 100 µs With PD

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

表 9-1 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with overvoltage cutoff. During power up, inrush current through MOSFET Q2 must be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature, and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2, and maximum operating voltage determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q2 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple, and ISO 7637-2 pulse 1 requirements. Overvoltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-to-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2, and LM74722-Q1.

9.2.2.2 Boost Converter Components (C2, C3, L1)

Place a minimum of a 1-µF capacitor across CAP pin to C pin (C2) and across C pin to GND (C3) of LM74722-Q1. Use a 100-µH inductor (L1) with saturation current rating > 175 mA. Example: XPL2010-104ML from coil craft.

9.2.2.3 Input and Output Capacitance

TI recommends a minimum input capacitance C1 of 0.1 µF and output capacitance C_{OUT} of 0.1 µF.

9.2.2.4 Hold-Up Capacitance

Usually, bulk capacitors are placed on the output due to various reasons, such as uninterrupted operation during power interruption or micro-short at the input, holdup requirements for doing a memory dump before turning of the module, and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status *A* during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage drop in the output of LM74722-Q1 is based on the UVLO settings of downstream DC/DC converters. For this design, 2.5-V drop in output voltage for 100 µs is considered and the minimum holdup capacitance required is calculated by

$$C_{(HOLD\_UP\_MIN)} = \frac{I_{LOAD\_MAX} \times 100\ \mu s}{\Delta V_{OUT}} \tag{3}$$

Minimum holdup capacitance required for 1-V drop in 100 µs is 470 µF.

9.2.2.5 Overvoltage Protection and Battery Monitor

Resistors R_1, R_2 and R_3 connected in series are used to program the overvoltage threshold and battery monitor ratio. The resistor values required for setting the overvoltage threshold, V_{OV}, to 37 V and battery monitor ratio V_{BATT_MON}:V_{BATT} to 1:8 are calculated by solving 式 4 and 式 5.

$$V_{OVR} = \frac{R_3 \times V_{OV}}{R_1+R_2+R_3} \tag{4}$$

$$V_{BAT\_MON} = \frac{(R_2 + R_3) \times V_{OV}}{R_1+R_2+R_3} \tag{5}$$

For minimizing the input current drawn from the battery through resistors R_1, R_2 and R_3, TI recommends to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_1 + R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{OVR} is 1.23 V and battery monitor ratio (V_{BATT_MON} / V_{BATT}) is designed for a ratio of 1:8. To limit (R_1 + R_2 + R_3) < 120 kΩ, select (R_1 + R_2) = 100 kΩ. Solving Equation 4 gives R_3 = 3.45 kΩ. Solving Equation 5 for R2 using (R_1 + R_2) = 100 kΩ and R_3 = 3.45 kΩ, gives R_2 = 9.48 kΩ and R_1 = 90.52 kΩ.

Standard 1% resistor values closest to the calculated resistor values are R1 = 90.9 kΩ, R2 = 9.09 kΩ, and R3 = 3.48 kΩ.

9.2.2.6 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This includes all the automotive transient events and any anticipated fault conditions. TI recommends to use MOSFETs with V_{DS} voltage rating of 60 V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back-to-back at the input.

The maximum V_{GS} LM74722-Q1 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a Zener diode can be used to clamp V_{GS} to safe level, but this results in increased I_Q current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ cannot always be beneficial. Higher $R_{DS(ON)}$ provides increased voltage information to the LM74722-Q1 reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with < 50-mV forward voltage drop at maximum current is a good starting point. Based on the design requirements, BUK7Y4R8-60E MOSFET is selected

9.2.2.7 MOSFET Selection: Load Disconnect MOSFET Q2

The V_{DS} rating of the MOSFET Q2 must be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12-V design, transient overvoltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2 A 50 V for 50 µs. Further, ISO 7637-2 pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors. The maximum voltage on the 12-V battery can be limited to < 40 V the minimum recommended input capacitance of 0.1 µF. The 50-V SO 7637-2 pulse 2 A can also be absorbed by input and output capacitors and its amplitude can be reduced to 40-V peak by placing sufficient amount of capacitance at input and output. Choose a MOSFET with ≥ 40-V V_{DS} rating .

The VGS rating of the MOSFET Q2 must be higher than that maximum boost drive output of 15.5 V. FET with VGS absolute maximum rating of +/– 20 VGS is selected.

Inrush current through the MOSFET during input hot-plug into the 12-V battery is determined by output capacitance. External capacitor on HGATE, C_{DVDT}, is used to limit the inrush current during input hot-plug or start-up. The value of inrush current determined by 式 1 must be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA). To limit inrush current to 250 mA, value of C_{DVDT} is 10.43 nF. The closest standard value of 10.0 nF is chosen.

Duration of inrush current is calculated by 式 6

$$T_{INRUSH} = \frac{12 \times C_{OUT}}{I_{INRUSH}} \tag{6}$$

Calculated inrush current duration is 2.36 ms with 250-mA inrush current.

MOSFET BUK7Y4R8-60E having 60-V V_{DS} and ±20-V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET safe operating area (SOA).

9.2.2.8 TVS Selection

TI recommends a 600-W SMBJ TVS such as SMBJ33CA for input transient clamping and protection. For detailed explanation on TVS selection for 12-V battery systems, refer to *TVS Selection for 12-V Battery Systems*.

9.2.3 Application Curves

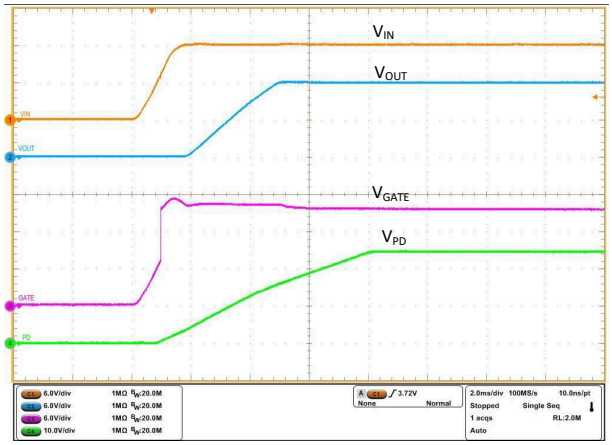


図 9-7. Start-Up 12 V with EN Pulled to VIN

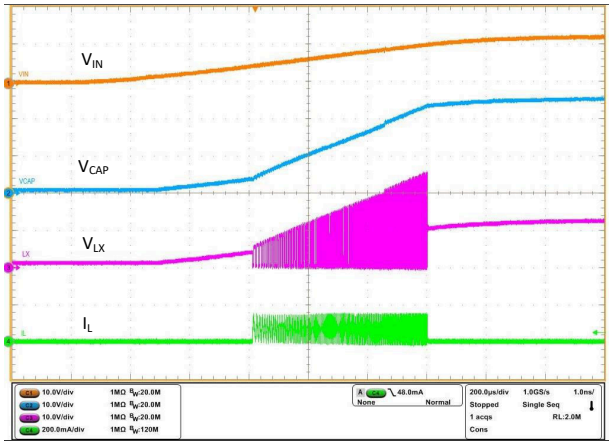


図 9-8. Start-Up 12 V Showing Boost Output (V_{CAP}) and Switching (V_{LX})

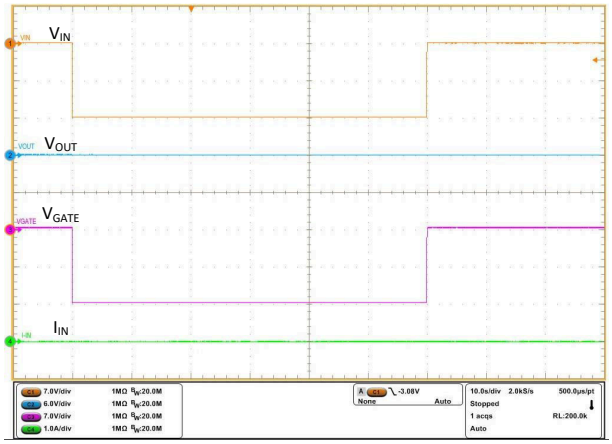


図 9-9. Reverse Input Voltage –14 V for 60 s

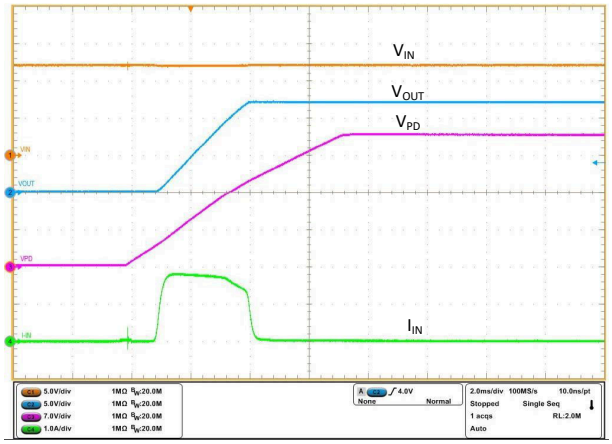


図 9-10. Inrush Current with No Load at Output

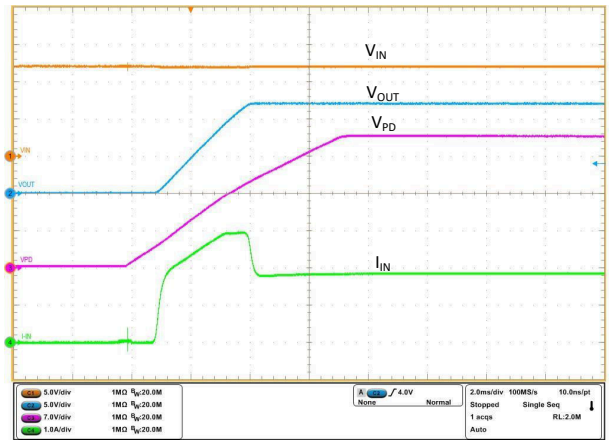


図 9-11. Inrush Current with 60-Ω Load

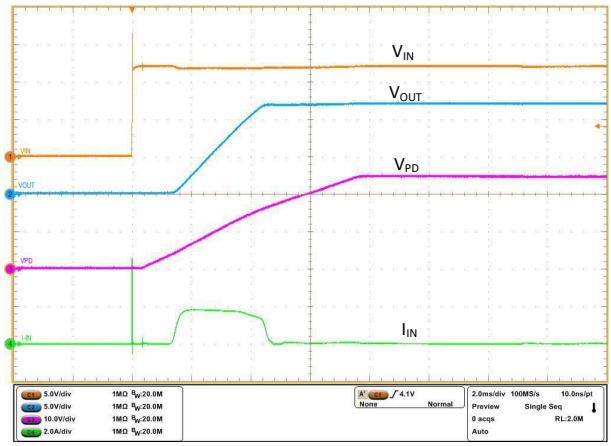


図 9-12. Hot-Plug into 12 V

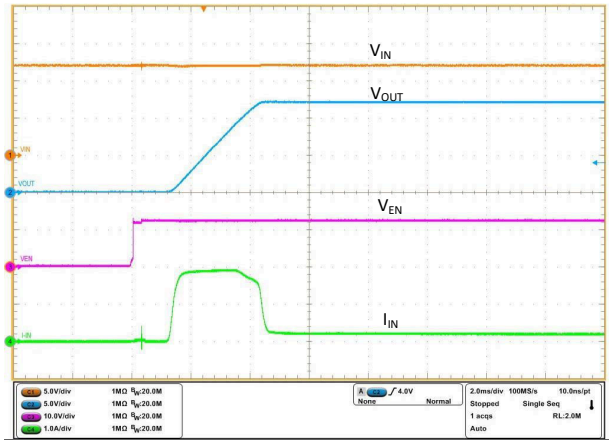


図 9-13. Output Turn-On with Enable

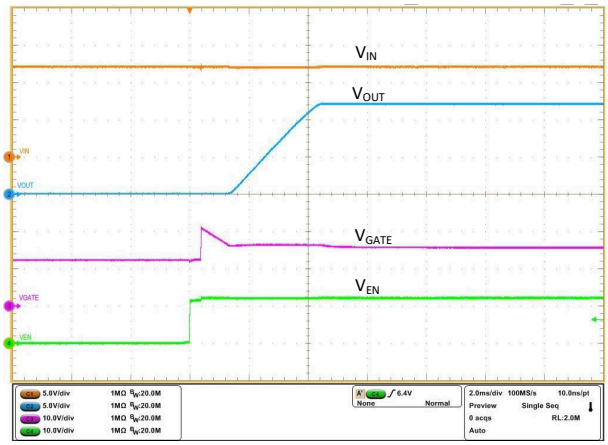


図 9-14. GATE Turn-On with Enable

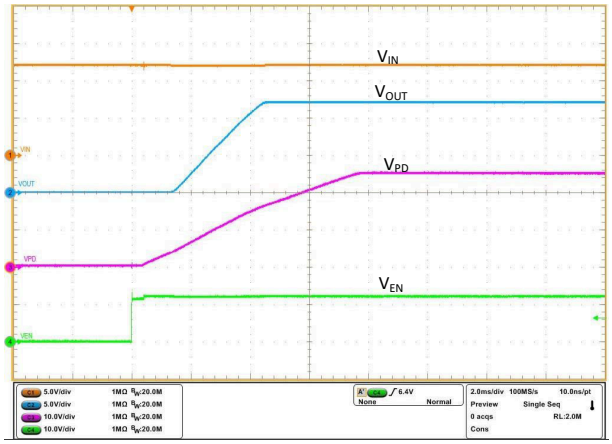


図 9-15. PD Turn-On with Enable

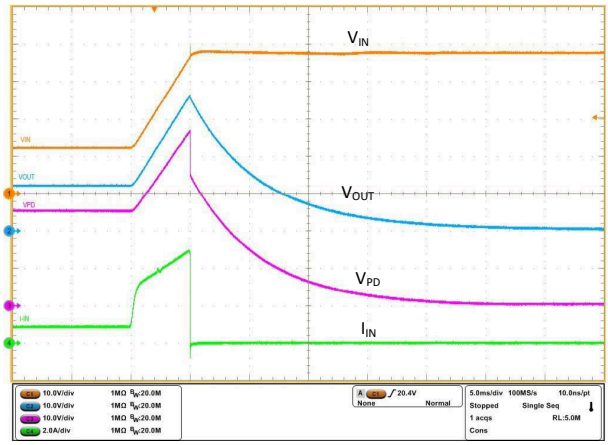


図 9-16. Overvoltage Protection

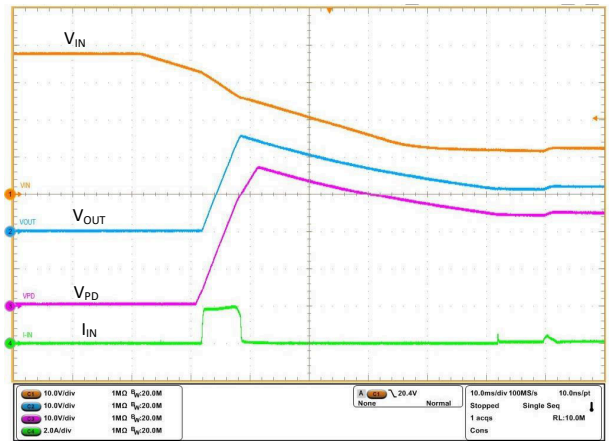


図 9-17. Overvoltage Recovery

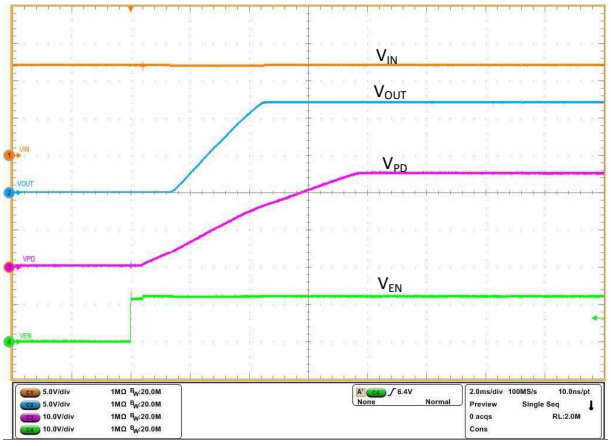


図 9-18. Turn-On Delay – PD

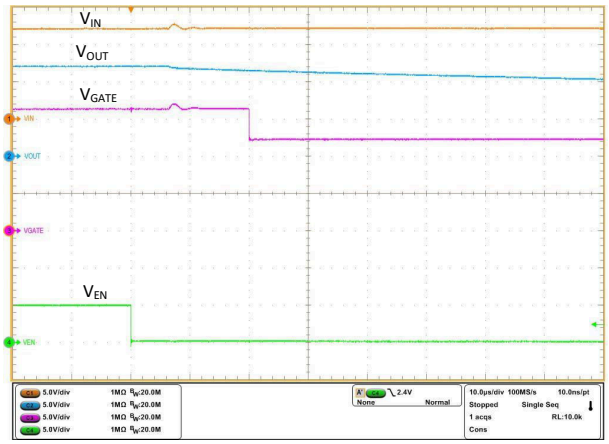


図 9-19. Turn-Off Delay – GATE

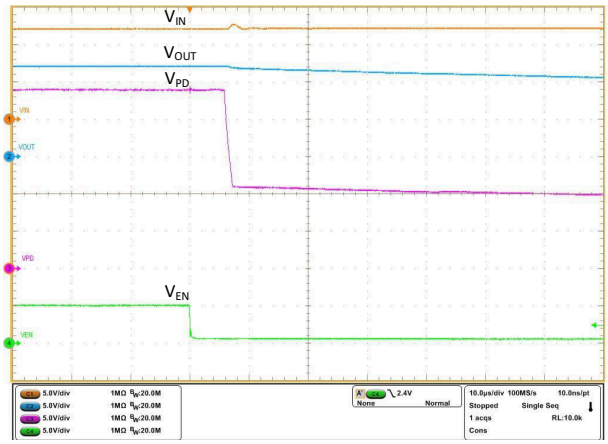


図 9-20. Turn-Off Delay – PD

9.3 What to Do and What Not to Do

Leave the exposed pad (RTN) of the IC floating. Do not connect the exposed pad (RTN) to the GND plane. Connecting the RTN to the GND disables the reverse polarity protection feature.

10 Power Supply Recommendations

10.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as overvoltage cutoff, reverse current blocking, and EN causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients

Equation 8 can estimate the approximate value of input capacitance.

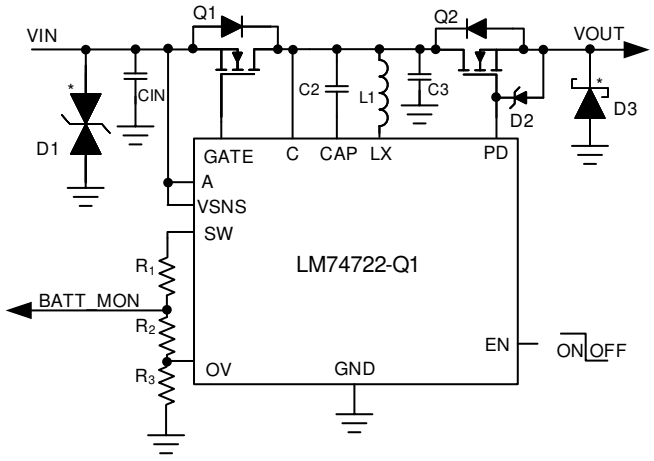
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (7)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications can require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing, such as automotive ISO7637 pulses.

図 10-1 shows the circuit implementation with optional protection components (a ceramic capacitor, TVS, and Schottky diode).



* Optional components needed for suppression of transients.

図 10-1. Circuit Implementation With Optional Protection Components for LM74722-Q1

10.2 TVS Selection for 12-V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74722-Q1 (65 V). The breakdown voltage of TVS– must be beyond the maximum reverse battery voltage –16 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS– and the voltage across the TVS is close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM74722-Q1 (85 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM74722-Q1 is pulled down by the ISO pulse, clamped by TVS–, and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS clamping voltage + output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS– must not exceed (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS are rated up to 600-W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

If 40-V rated MOSFET is choosen then maximum voltage across C (Drain of the MOSFET) and A (Source of the MOSFET) must not exceed 40-V. For 40-V MOSFET selection, two back-to-back connected uni-directional TVS diodes are required to protect against input transient events. On the positive side, the SMBJ33A TVS diode can be used for 12-V battery protection application. However on the negative side, TVS has to withstand 16-V reverse battery connection and clamping voltage has to be –(40 V - 16 V) = –24 V. SMBJ16A can be used.

10.3 TVS Selection for 24-V Battery Systems

For 24-V battery protection application, the TVS and MOSFET in 図 9-1 must be changed to suit 24-V battery requirements.

The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74722-Q1 (70 V), and must withstand 65-V suppressed load dump. The breakdown voltage of TVS– must be lower than maximum reverse battery voltage –32 V, so that the TVS– does not damage due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12 A flowing through the TVS–. The clamping voltage of the TVS– cannot be the same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the anode to cathode voltage seen is equal to (-– TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS– must not exceed, 85 V – 32 V = 53 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65 V, maximum clamping voltage is ≤ 53 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-to-back must be used at the input. For positive side TVS+, TI recommends SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical). For the negative side TVS–, TI recommends SMBJ28A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V.

For 24-V battery protection, TI recommends that a 75-V rated MOSFET be used along with SMBJ28A and SMBJ58A connected back-to-back at the input.

11 Layout

11.1 Layout Guidelines

- Connect A, GATE, and C pins of LM74722-Q1 close to the MOSFET SOURCE, GATE and DRAIN pins for the ideal diode stage.
- Use thick and short traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- Connect the GATE pin of the LM74722-Q1 to the MOSFET GATE with short trace.
- Minimize the loops formed by capacitor across CAP pin and DRAIN of the FET and C3 to GND by placing these capacitors as close as possible. Keep the GND side of the C3 capacitor close to GND pin of LM74722-Q1. Boost converter switching currents flow into LX, CAP, GND pins and C3 (across DRAIN of the FET to GND).
- Place transient suppression components, like input TVS and output Schottky, close to LM74722-Q1.

11.2 Layout Example

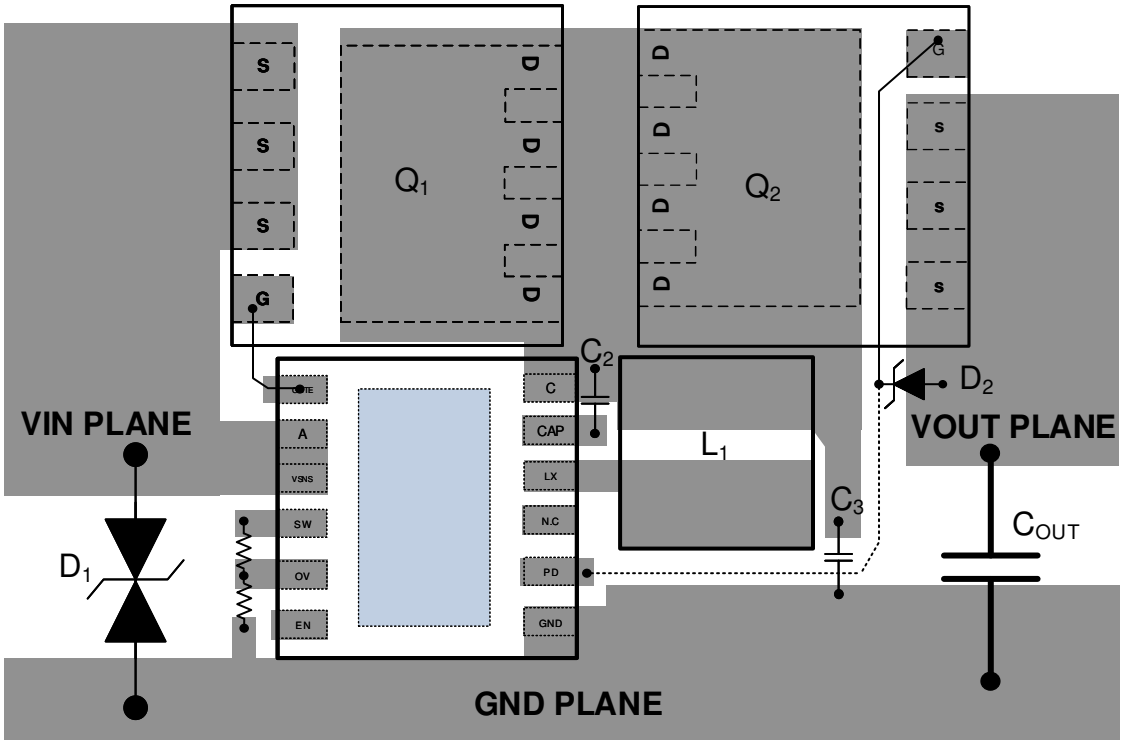


図 11-1. LM74722-Q1 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM74722QDRRRQ1	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L74722
LM74722QDRRRQ1.A	Active	Production	WSON (DRR) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L74722

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

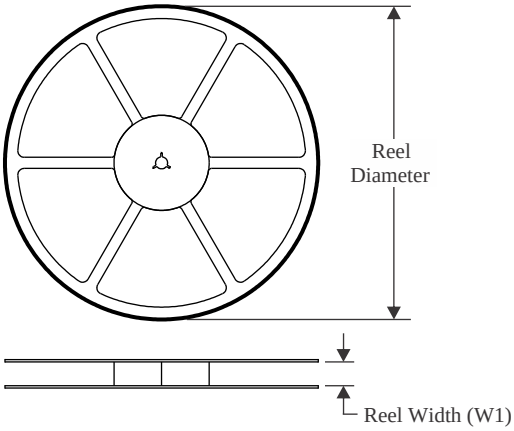
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

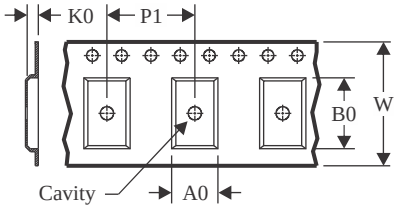
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

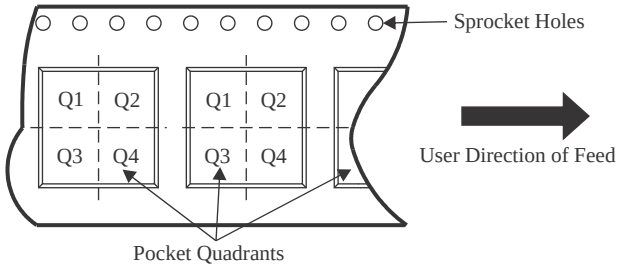


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

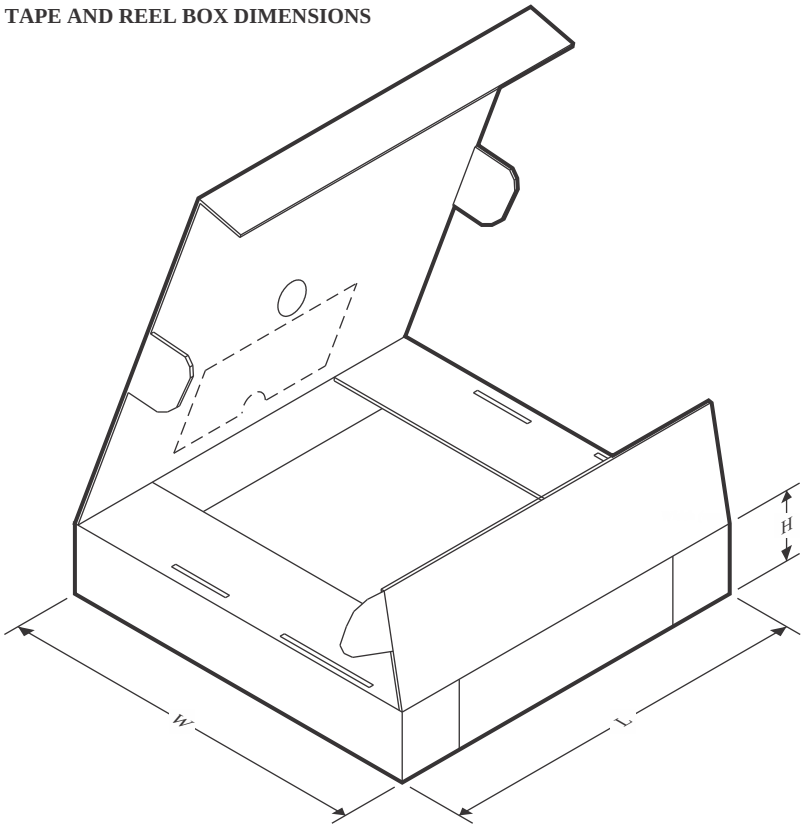
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74722QDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74722QDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

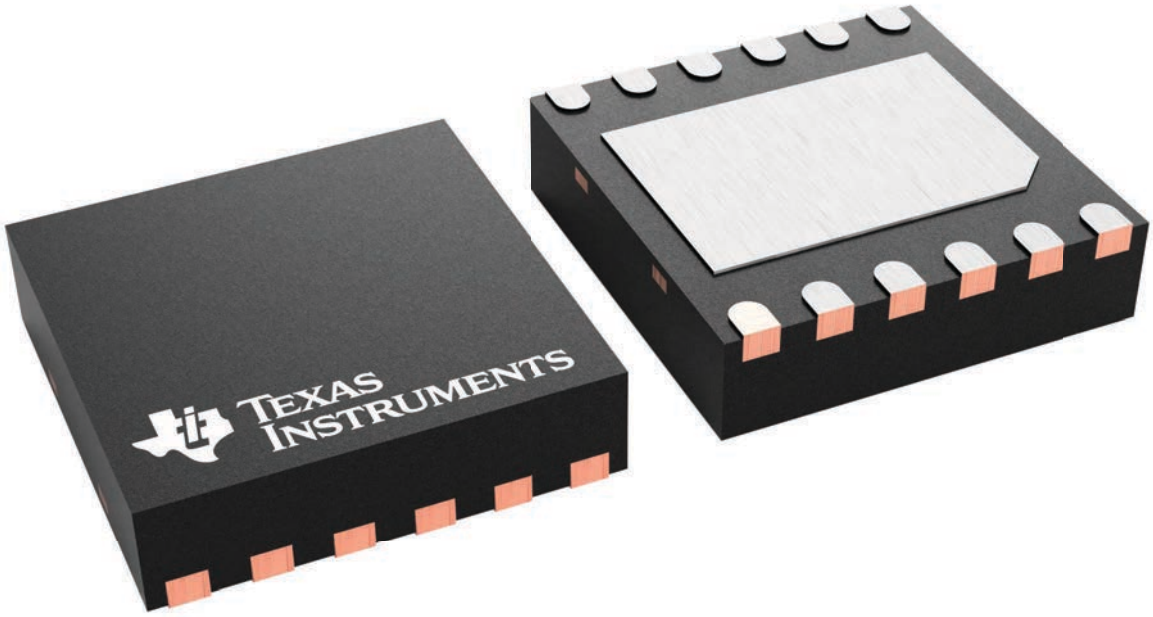
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



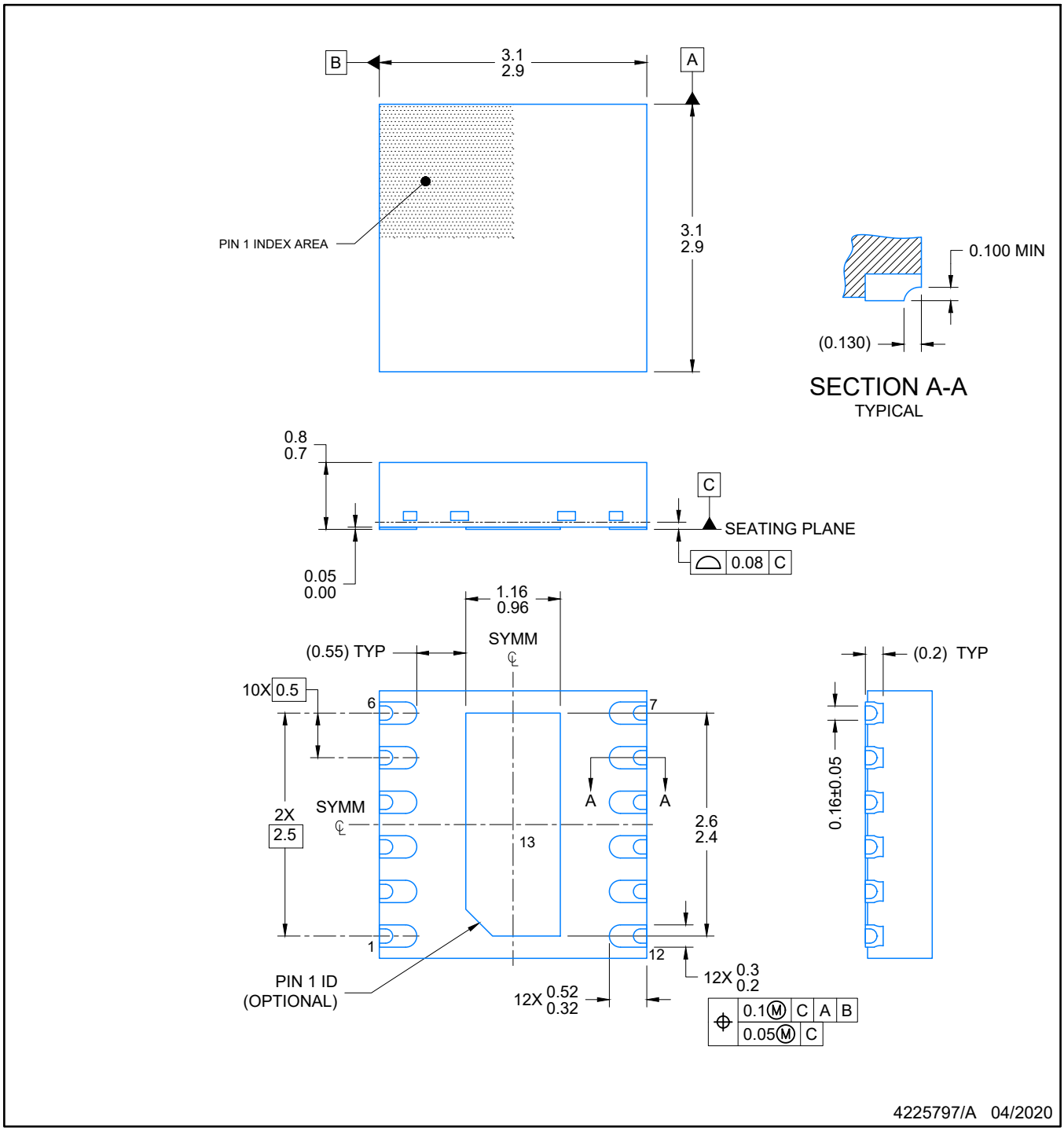
4223490/B

PACKAGE OUTLINE

DRR0012F

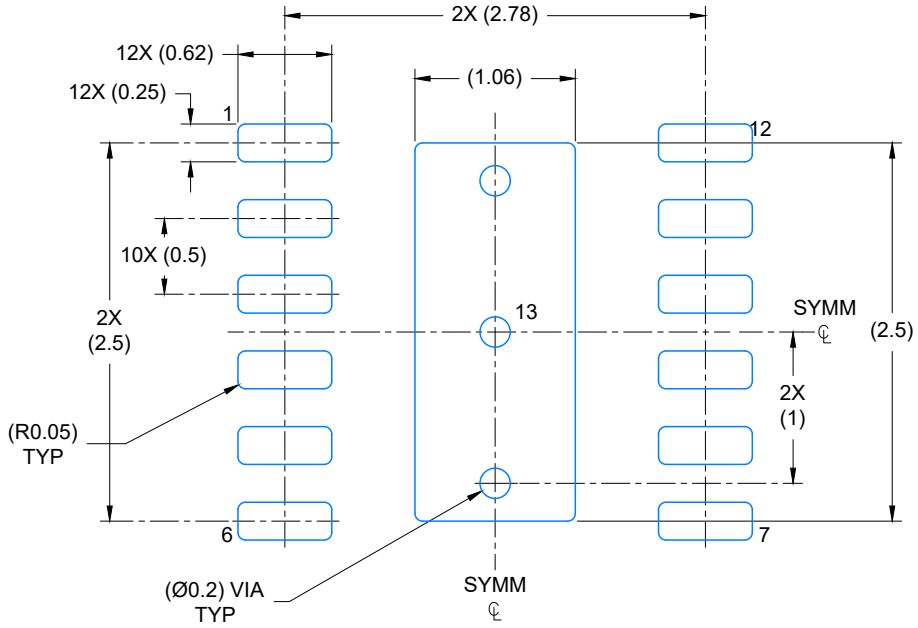
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

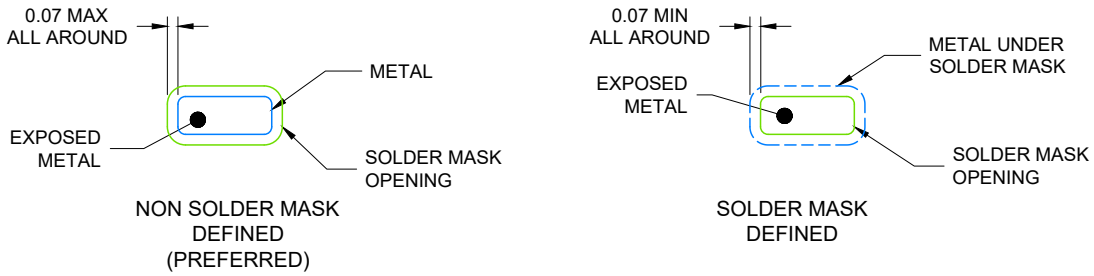


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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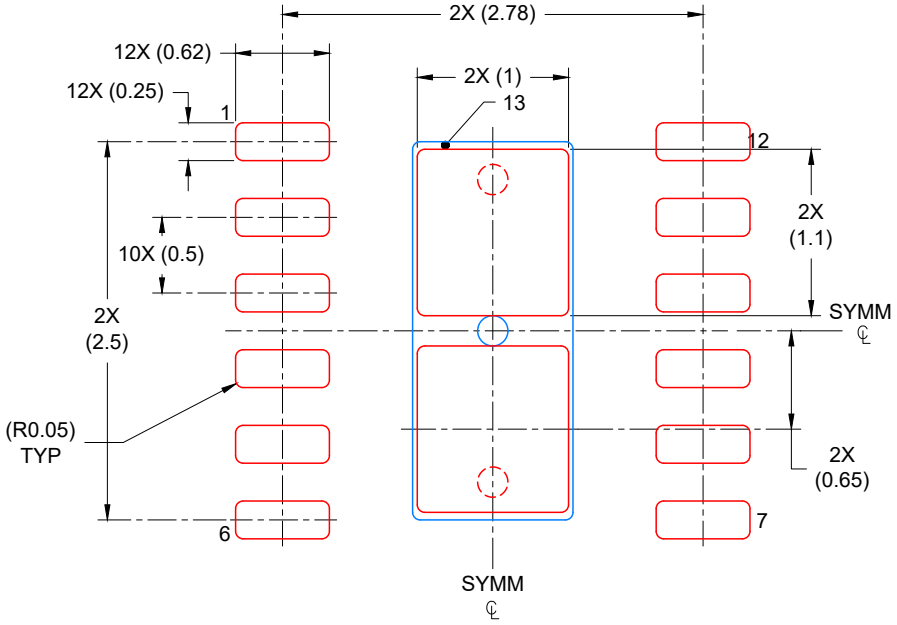
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED COVERAGE BY AREA
SCALE: 20X

4225797/A 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月