LM833 Dual High-Speed Audio Operational Amplifier

1 Features

- Dual-Supply Operation: ±5 V to ±18 V
- Low Noise Voltage: 4.5 nV/√Hz
- Low Input Offset Voltage: 0.15 mV
- Low Total Harmonic Distortion: 0.002%
- High Slew Rate: 7 V/μs
- High-Gain Bandwidth Product: 16 MHz
- High Open-Loop AC Gain: 800 at 20 kHz
- Large Output-Voltage Swing: –14.6 V to 14.1 V
- Excellent Gain and Phase Margins
- Available in 8-Terminal MSOP Package (3.0 mm x 4.9 mm x 0.65 mm)

2 Applications

- HiFi Audio System Equipment
- Preamplification and Filtering
- Set-Top Box
- Microphone Preamplifier Circuit
- General-Purpose Amplifier Applications

3 Description

The LM833 device is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. Dual amplifiers are utilized widely in audio circuits optimized for all preamp and high level stages in PCM and HiFi systems. The LM833 device is pin-for-pin compatible with industry-standard dual operation amplifiers. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM833	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

4 Typical Design Example Audio Pre-Amplifier

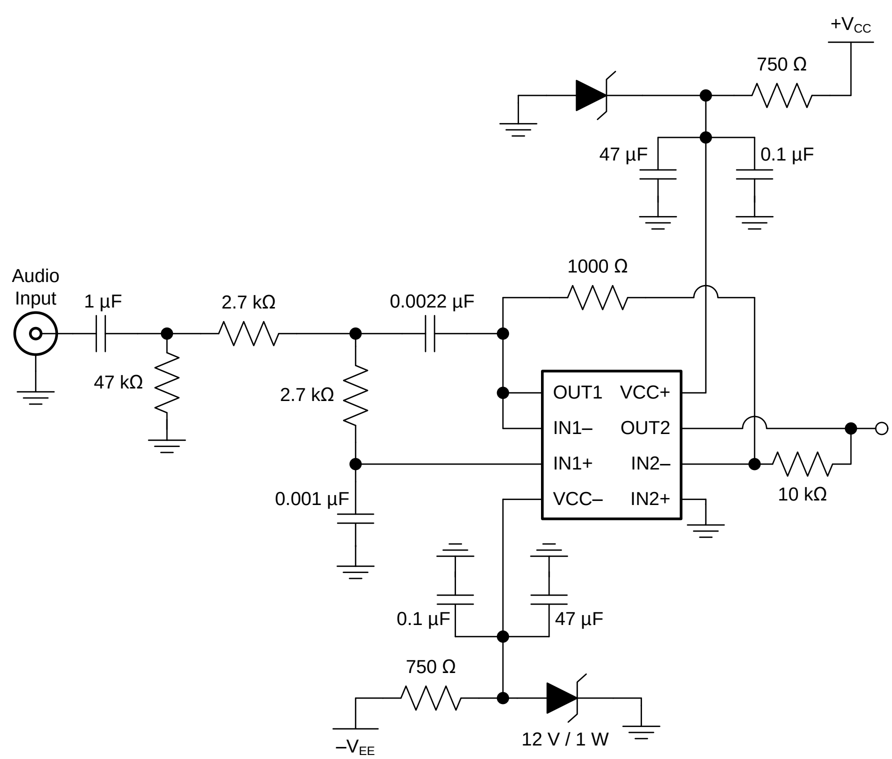


Table of Contents

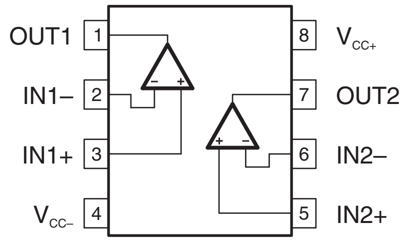
5 Revision History

Changes from Revision A (August 2010) to Revision B	Page
• Updated document to new TI data sheet format.	1
• Deleted *Ordering Information* table.	1
• Added *Device Information* table.	1
• Added *Pin Functions* table.	3
• Added *Handling Ratings* table.	4
• Added *Thermal Information* table.	4
• Added *Power Supply Recommendations, Layout, Device and Documentation Support,* and *Mechanical, Packaging, and Orderable Information* sections	20

Changes from Original (July 2010) to Revision A	Page
• Changed data sheet status from Product Preview to Production Data.	1

6 Pin Configuration and Functions

**D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE
(TOP VIEW)**



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1+	3	Input	Noninverting input
IN1–	2	Input	Inverting Input
IN2+	5	Input	Noninverting input
IN2-	6	Input	Inverting Input
OUT1	1	Output	Output 1
OUT2	7	Output	Output 2
V_{CC+}	8	—	Positive Supply
$V_{CC–}$	4	—	Negative Supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)		18	V
V_{CC-}	Supply voltage(2)		–18	V
$V_{CC+} – V_{CC-}$	Supply voltage		36	V
	Input voltage, either input(2)(3)	V_{CC-}	V_{CC+}	V
	Input current(4)		±10	mA
	Duration of output short circuit(5)	Unlimited		
T_J	Operating virtual junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
$V_{(ESD)}$	Human-Body Model (HBM)(1)	0	2.5	kV
	Charged-Device Model (CDM)(2)	0	1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC-}	Supply voltage	–5	–18	V
V_{CC+}		5	18	
T_A	Operating free-air temperature range	–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		LM833			UNIT
		D	DGK	P	
		8 PINS			
$R\theta_{JA}$	Junction-to-ambient thermal resistance(2)(3)	97	172	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).
(2) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = 25°C		0.15	2	mV
				T_A = –40°C to 85°C			3	
αV_{IO}	Input offset voltage temperature coefficient	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = –40°C to 85°C		2		μV/°C
I_{IB}	Input bias current	V_O = 0, V_{CM} = 0		T_A = 25°C		300	750	nA
				T_A = –40°C to 85°C			800	
I_{IO}	Input offset current	V_O = 0, V_{CM} = 0		T_A = 25°C		25	150	nA
				T_A = –40°C to 85°C			175	
V_{ICR}	Common-mode input voltage range	ΔV_{IO} = 5 mV, V_O = 0			±13	±14		V
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V		T_A = 25°C	90	110		dB
				T_A = –40°C to 85°C	85			
V_{OM}	Maximum output voltage swing	V_{ID} = ±1 V	R_L = 600 Ω	V_{OM+}		10.7		V
				V_{OM-}		–11.9		
			R_L = 2000 Ω	V_{OM+}	13.2	13.8		
				V_{OM-}	–13.2	–13.7		
			R_L = 10,000 Ω	V_{OM+}	13.5	14.1		
				V_{OM-}	–14	–14.6		
CMMR	Common-mode rejection ratio	V_{IN} = ±13 V			80	100		dB
k_{SVR} (1)	Supply-voltage rejection ratio	V_{CC+} = 5 V to 15 V, V_{CC-} = –5 V to –15 V			80	105		dB
I_{OS}	Output short-circuit current	$\lvert V_{ID}\rvert$ = 1 V, Output to GND		Source current	15	29		mA
				Sink current	–20	–37		
I_{CC}	Supply current (per channel)	V_O = 0		T_A = 25°C		2.05	2.5	mA
				T_A = –40°C to 85°C			2.75	

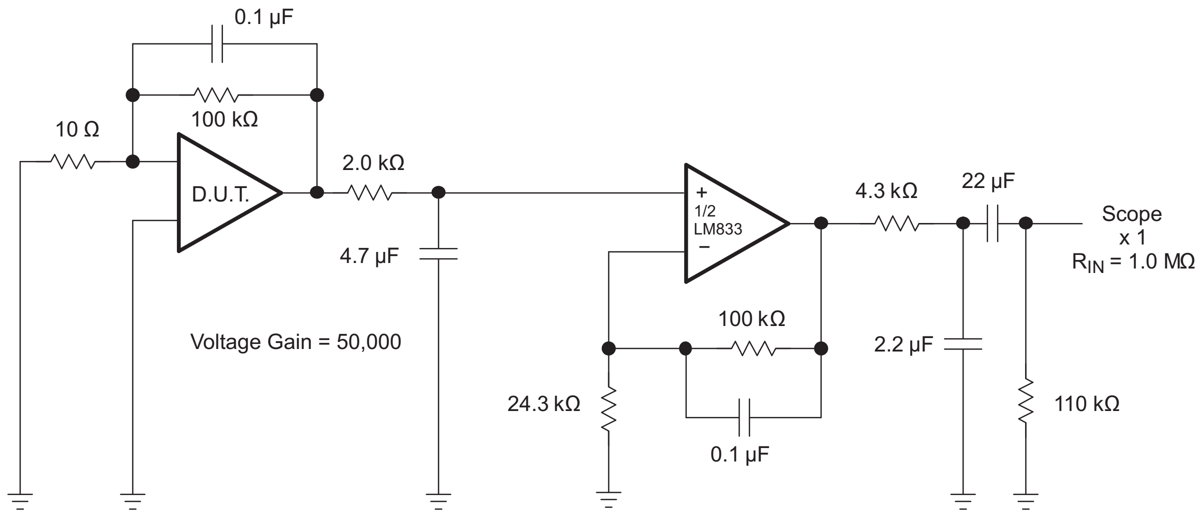
(1) Measured with $V_{CC\pm}$ differentially varied at the same time

7.6 Operating Characteristics

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	A_{VD} = 1, V_{IN} = –10 V to 10 V, R_L = 2 kΩ, C_L = 100 pF		5	7		V/μs
GBW	Gain bandwidth product	f = 100 kHz		10	16		MHz
B_1	Unity gain frequency	Open loop			9		MHz
G_m	Gain margin	R_L = 2 kΩ	C_L = 0 pF		–11		dB
			C_L = 100 pF		–6		
Φ_m	Phase margin	R_L = 2 kΩ	C_L = 0 pF		55		degrees
			C_L = 100 pF		40		
	Amp-to-amp isolation	f = 20 Hz to 20 kHz			–120		dB
	Power bandwidth	V_O = 27 $V_{(PP)}$, R_L = 2 kΩ, THD ≤ 1%			120		kHz
THD	Total harmonic distortion	V_O = 3 V_{rms}, A_{VD} = 1, R_L = 2 kΩ, f = 20 Hz to 20 kHz			0.002%		
z_o	Open-loop output impedance	V_O = 0, f = 9 MHz			37		Ω
r_{id}	Differential input resistance	V_{CM} = 0			175		kΩ
C_{id}	Differential input capacitance	V_{CM} = 0			12		pF
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω			4.5		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.5		pA/√Hz

7.7 Typical Characteristics



NOTE: All capacitors are non-polarized.

Figure 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

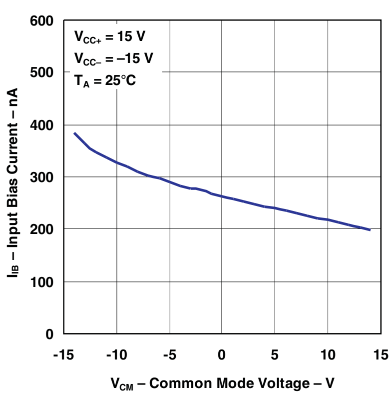


Figure 2. Input Bias Current vs Common-Mode Voltage

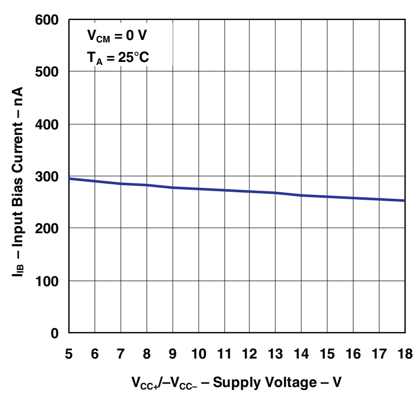


Figure 3. Input Bias Current vs Supply Voltage

Typical Characteristics (continued)

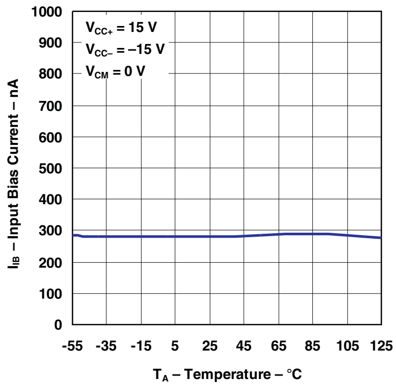


Figure 4. Input Bias Current vs Temperature

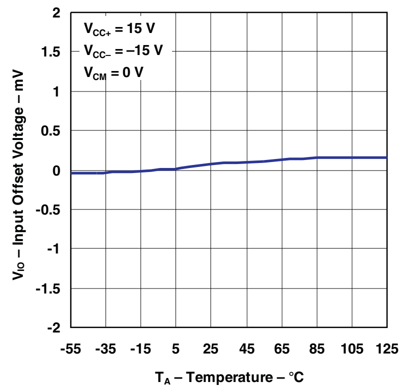


Figure 5. Input Offset Voltage vs Temperature

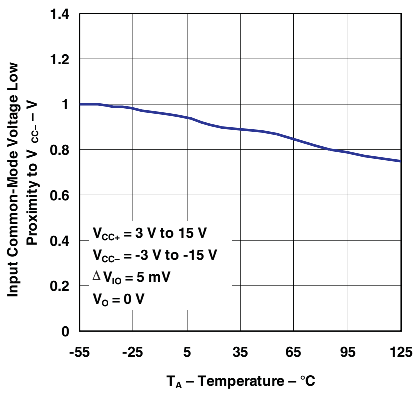


Figure 6. Input Common-Mode Voltage Low Proximity to V_{CC-} vs Temperature

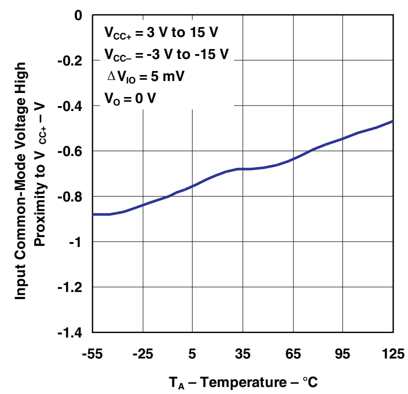


Figure 7. Input Common-Mode Voltage High Proximity to V_{CC+} vs Temperature

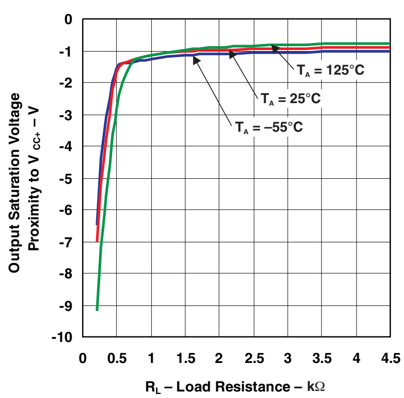


Figure 8. Output Saturation Voltage Proximity to V_{CC+} vs Load Resistance

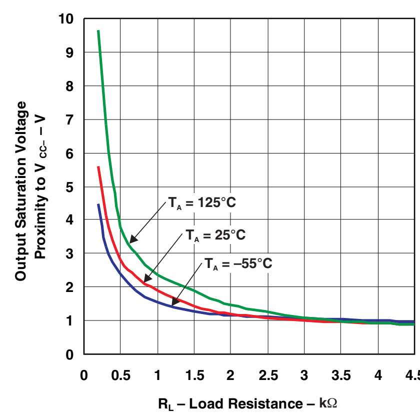


Figure 9. Output Saturation Voltage Proximity to V_{CC-} vs Load Resistance

Typical Characteristics (continued)

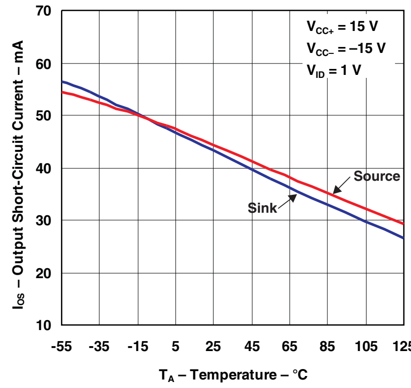


Figure 10. Output Short-Circuit Current vs Temperature

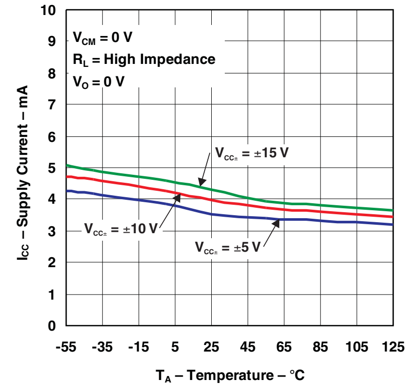


Figure 11. Supply Current vs Temperature

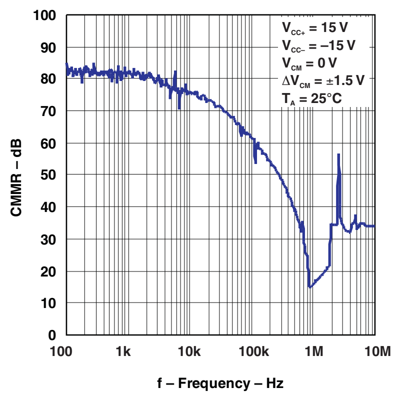


Figure 12. CMRR vs Frequency

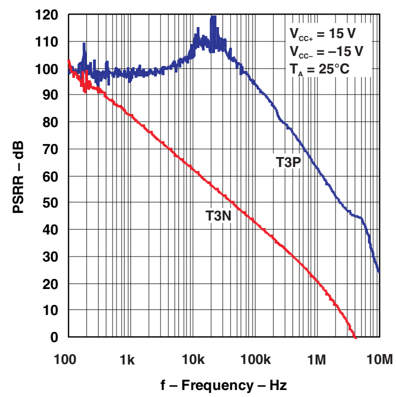


Figure 13. PSSR vs Frequency

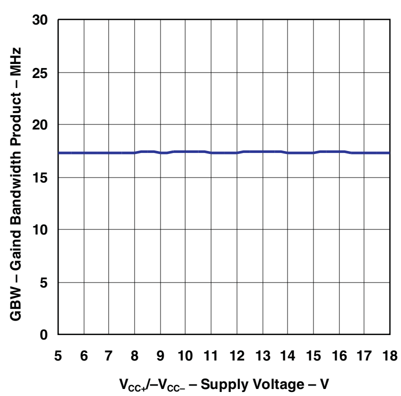


Figure 14. Gain Bandwidth Product vs Supply Voltage

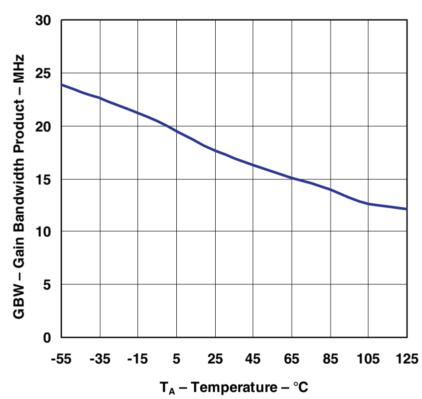


Figure 15. Gain Bandwidth Product vs Temperature

Typical Characteristics (continued)

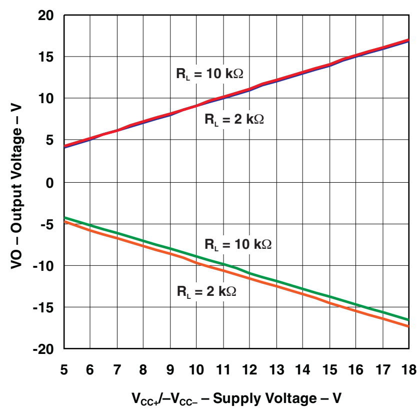


Figure 16. Output Voltage vs Supply Voltage

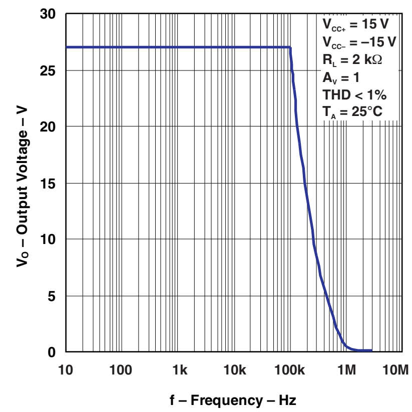


Figure 17. Output Voltage vs Frequency

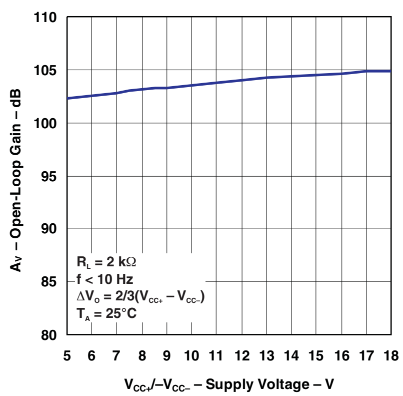


Figure 18. Open-Loop Gain vs Supply Voltage

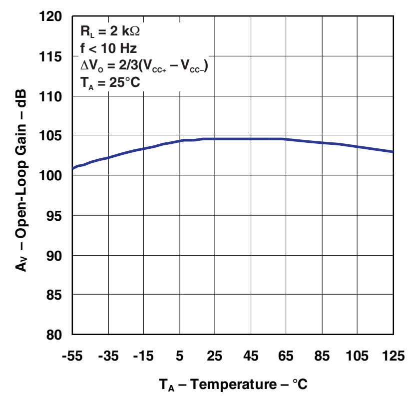


Figure 19. Open-Loop Gain vs Temperature

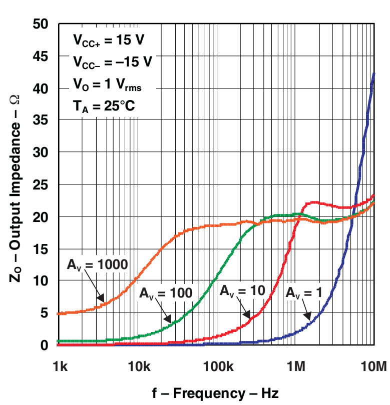


Figure 20. Output Impedance vs Frequency

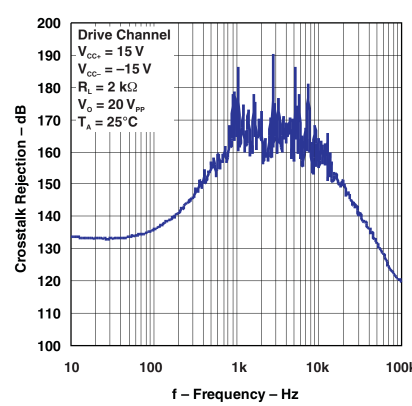


Figure 21. Crosstalk Rejection vs Frequency

Typical Characteristics (continued)

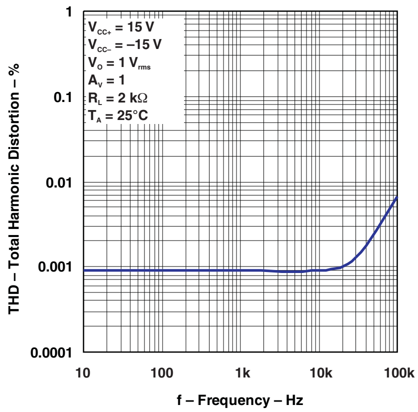


Figure 22. Total Harmonic Distortion vs Frequency

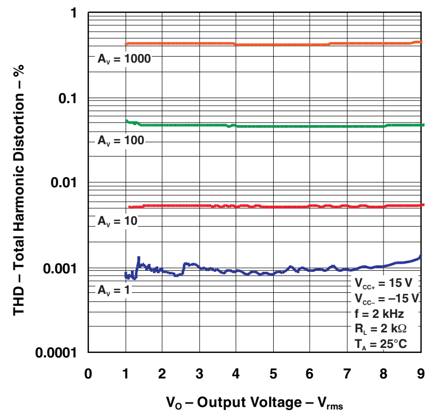


Figure 23. Total Harmonic Distortion vs Output Voltage

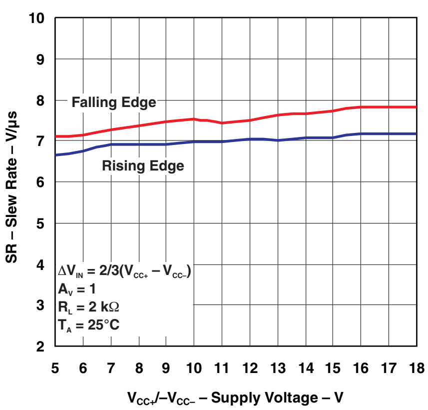


Figure 24. Slew Rate vs Supply Voltage

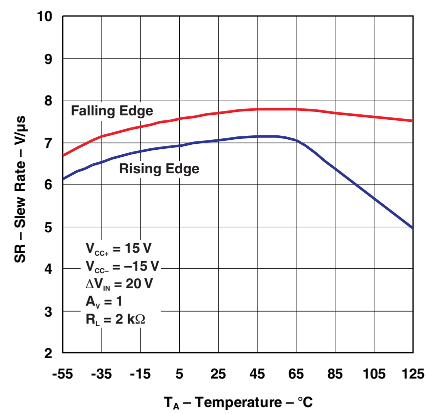


Figure 25. Slew Rate vs Temperature

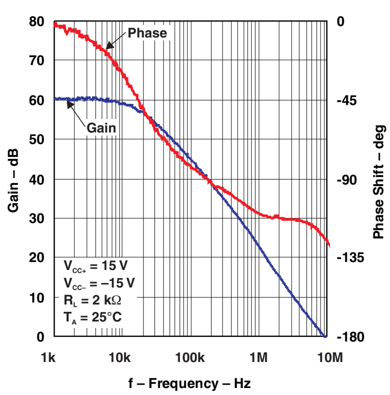


Figure 26. Gain and Phase vs Frequency

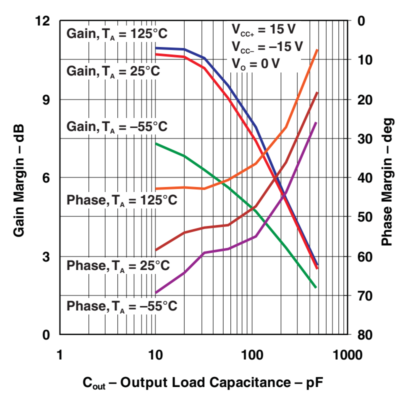


Figure 27. Gain and Phase Margin vs Output Load Capacitance

Typical Characteristics (continued)

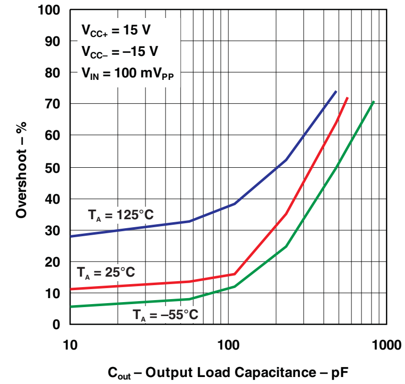


Figure 28. Overshoot vs Output Load Capacitance

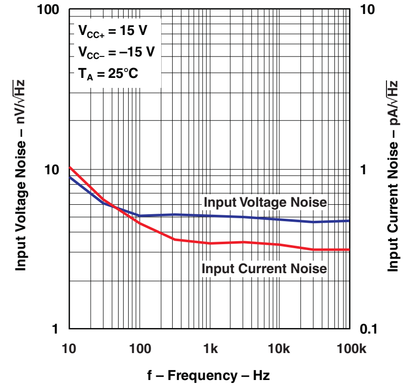


Figure 29. Input Voltage and Current Noise vs Frequency

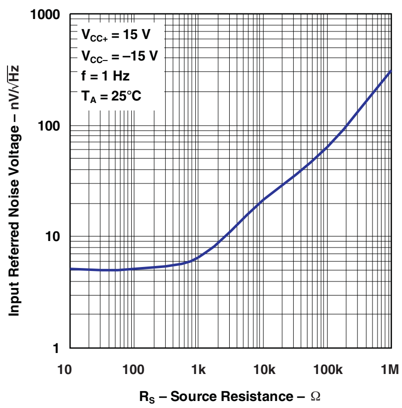


Figure 30. Input Referred Noise Voltage vs Source Resistance

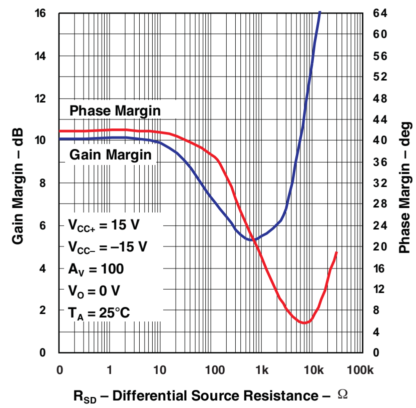


Figure 31. Gain and Phase Margin vs Differential Source Resistance

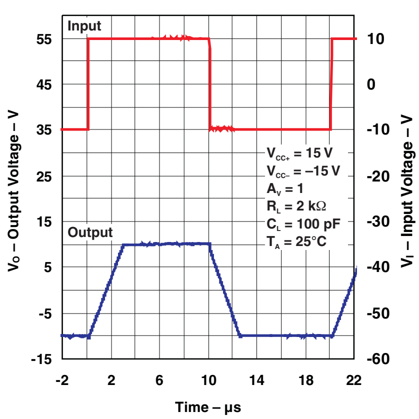


Figure 32. Large Signal Transient Response (A_V = 1)

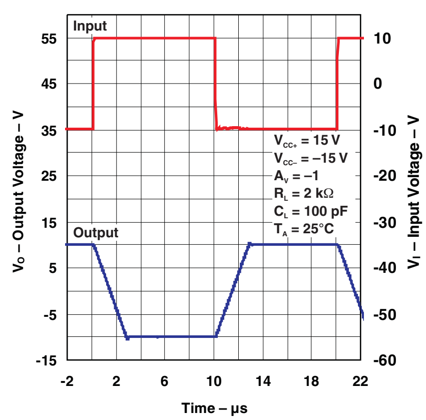


Figure 33. Large Signal Transient Response (A_V = –1)

Typical Characteristics (continued)

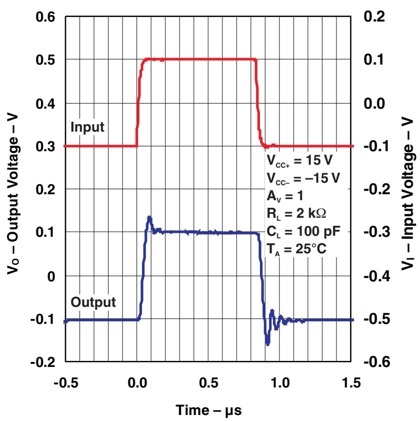


Figure 34. Small Signal Transient Response

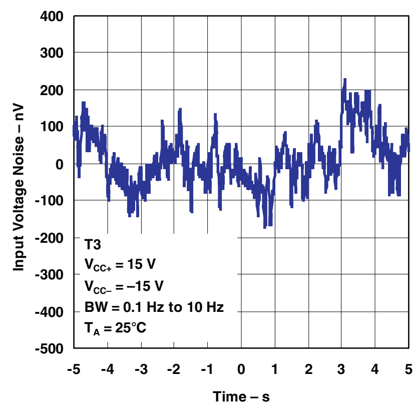


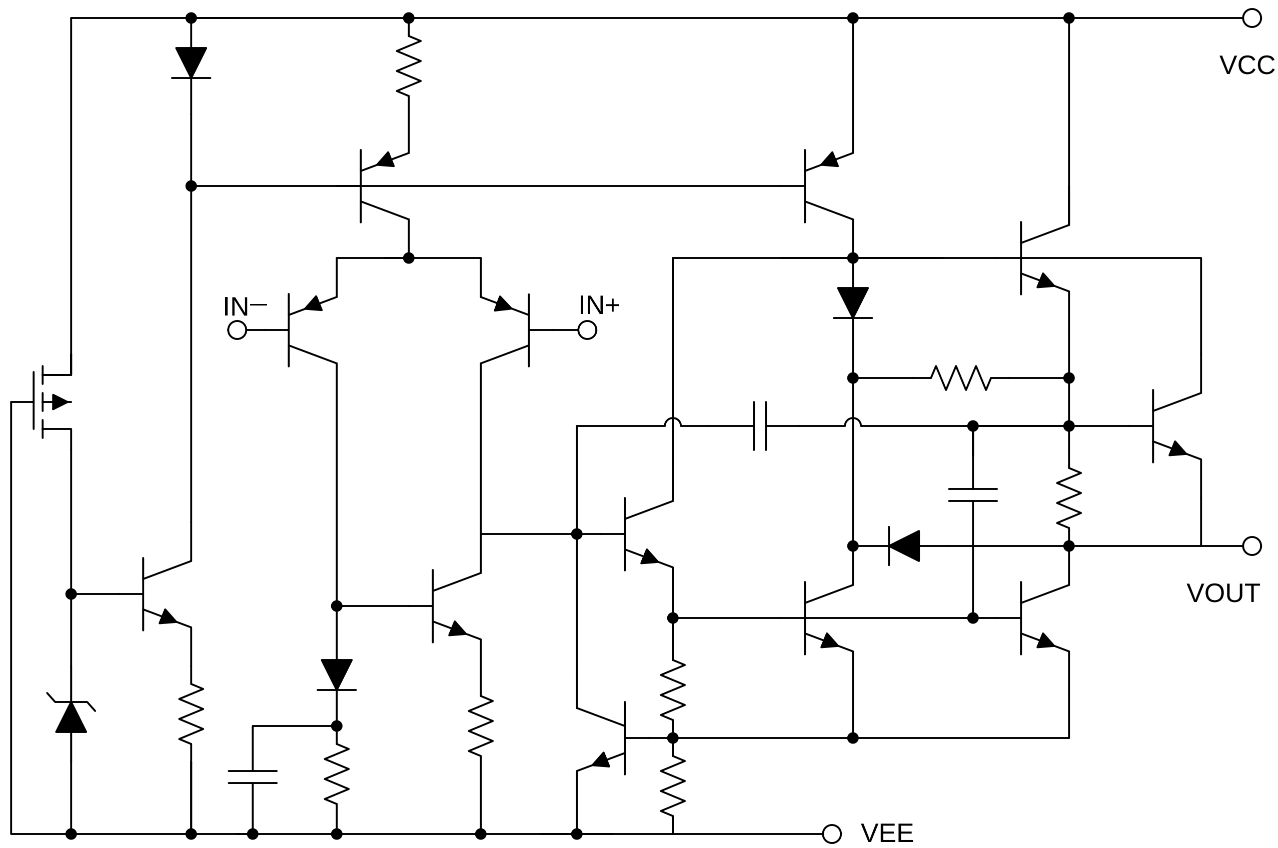
Figure 35. Low-Frequency Noise

8 Detailed Description

8.1 Overview

The LM833 device is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltage with low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortions, and symmetrical sink/source performance. The dual amplifiers are utilized widely in circuit of audio optimized for all preamp and high-level stages in PCM and HiFi systems. The LM833 device is pin-for-pin compatible with industry-standard dual operation amplifiers' pin assignments. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The LM833 operational amplifier is fully specified and ensured for operation from ±5 V to ±18 V. In addition, many specifications apply from –40°C to 85°C. Parameters that vary significantly with operating voltages or temperature are shown in *Absolute Maximum Ratings* .

8.3.2 High Gain Bandwidth Product

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. The LM833 has a high gain bandwidth of 16 MHz which stays relatively stable over a wide range of supply voltages. Parameters that vary significantly with temperature are shown in Figure 14.

8.3.3 Low Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. The LM833 has a very low THD of 0.002% meaning that the LM833 will add little harmonic distortion when used in audio signal applications. More specific characteristics are shown in Figure 22.

8.4 Device Functional Modes

The LM833 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

An application of the LM833 is the two stage RIAA Phono Preamplifier. A primary task of the phono preamplifier is to provide gain (usually 30 to 40 dB at 1 kHz) and accurate amplitude and phase equalization to the signal from a moving magnet or a moving coil cartridge. In addition to the amplification and equalization functions, the phono preamp must not add significant noise or distortion to the signal from the cartridge. The circuit shown in Figure 36 uses two amplifiers, fulfills these qualifications, and has greatly improved performance over a single-amplifier design.

9.2 Typical Application

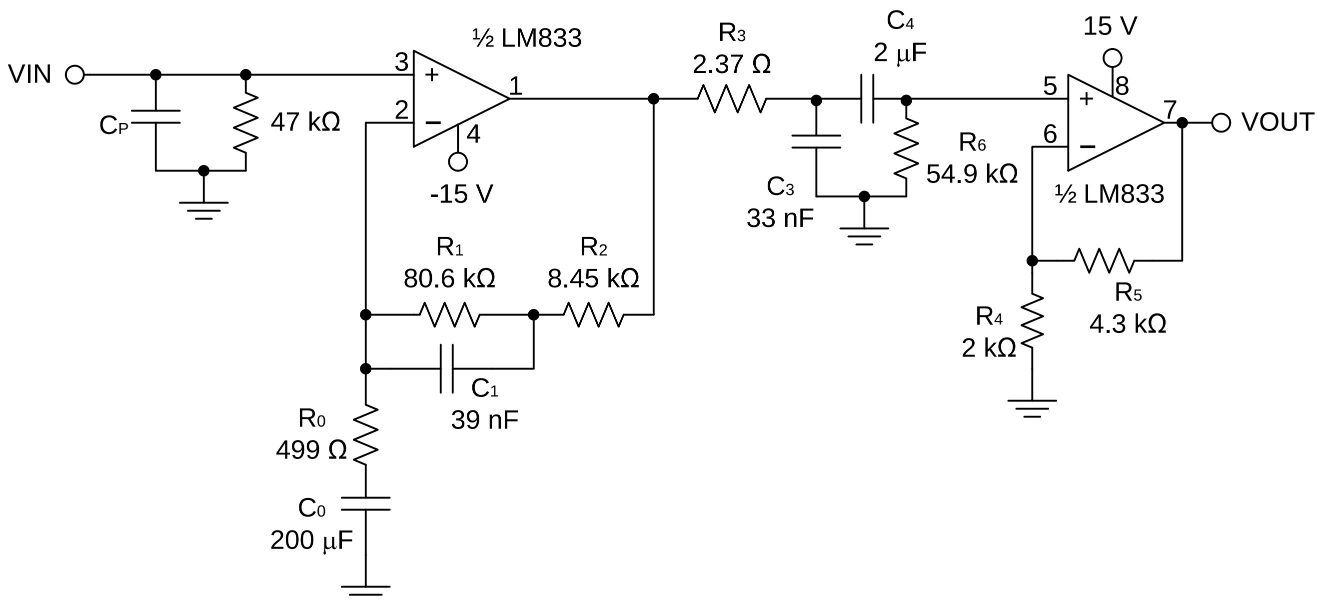


Figure 36. RIAA Phono Preamplifier

9.2.1 Design Requirements

- Supply Voltage = ±15 V
- Low-Frequency −3 dB corner of the first amplifier (f_0) > 20 Hz (below audible range)
- Low-Frequency −3 dB corner of the second stage (f_L) = 20.2 Hz

9.2.2 Detailed Design Procedure

9.2.2.1 Introduction to Design Method

Equation 1 through Equation 5 show the design equations for the preamplifier.

$$R_1 = 8.058\ R_0 A_1$$

where

- A_1 is the 1 kHz voltage gain of the first amplifier (1)

Typical Application (continued)

$$C_1 = \frac{3.18 \times 10^{-3}}{R_1} \quad (2)$$

$$R_2 = \frac{R_1}{9} - R_0 \quad (3)$$

$$C_3 = 7.5 \times 10^{-5} \frac{(R_3 + R_6)}{R_3 R_6} = \frac{7.5 \times 10^{-5}}{R_P} \quad (4)$$

$$C_4 = \frac{1}{2 \pi f_L (R3 + R6)}$$

where

- f_L is the low-frequency −3 dB corner of the second stage (5)

For standard RIAA preamplifiers, f_L should be kept well below the audible frequency range. If the preamplifier is to follow the IEC recommendation (IEC Publication 98, Amendment #4), f_L should equal 20.2 Hz.

$$A_{V2} = 1 + \frac{R_5}{R_4}$$

where

- A_{V2} is the voltage gain of the second amplifier (6)

$$C_0 \approx \frac{1}{2 \pi f_0 R_0}$$

where

- f_0 is the low-frequency −3 dB corner of the first amplifier (7)

This should be kept well below the audible frequency range.

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Because 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

9.2.2.2 RIAA Phono Preamplifier Design Procedure

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Since 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

Choose R_0. R_0 should be small for minimum noise contribution, but not so small that the feedback network excessively loads the amplifier.

Example: Choose R_0 = 500

Choose 1 kHz gain, A_{V1} of first amplifier. This will typically be around 20 dB to 30 dB.

Example: Choose A_{V1} = 26 dB = 20

Calculate $R_1 = 8.058\ R_0 A_{V1}$

Example: $R_1 = 8.058 \times 500 \times 20 = 80.58$ k

$$\text{Calculate } C_1 = \frac{3.18 \times 10^{-3}}{R_1} \quad (8)$$

$$\text{Example: } C_1 = \frac{3.18 \times 10^{-3}}{8.058 \times 10^4} = 0.03946\,\mu F \quad (9)$$

If C_1 is not a convenient value, choose the nearest convenient value and calculate a new R_1 from Equation 10.

Typical Application (continued)

$$R_1 = \frac{3.18 \times 10^{-3}}{C_1} \tag{10}$$

Example: New C_1 = 0.039 µF.

$$\text{New } R_1 = \frac{3.18 \times 10^{-3}}{3.9 \times 10^{-8}} = 81.54\,k$$

$$\text{Use } R_1 = 80.6\,k \tag{11}$$

Calculate a new value for R_0 from Equation 12.

$$R_0 = \frac{R_1}{8.058\,A_{V1}} \tag{12}$$

$$\text{Example: New } R_0 = \frac{8.06 \times 10^4}{8.058 \times 20} = 498.8 \tag{13}$$

Use R_0 = 499.

$$\text{Calculate } R_2 = \frac{R_1}{9} - R_0$$

$$\text{Example: } R_2 = \frac{8.06 \times 10^4}{9} - 499 = 8456.56 \tag{14}$$

Use R_2 = 8.45 K.

Choose a convenient value for C_3 in the range from 0.01 µF to 0.05 µF.

Example: C_3 = 0.033 µF

$$\text{Calculate } R_P = \frac{7.5 \times 10^{-5}}{C_3}$$

$$\text{Example: } R_P = \frac{7.5 \times 10^{-5}}{3.3 \times 10^{-8}} = 2.273\,k \tag{15}$$

Choose a standard value for R_3 that is slightly larger than R_P.

Example: R_3 = 2.37 k

Calculate R_6 from $1 / R_6 = 1 / R_P - 1 / R_3$

Example: R_6 = 55.36 k

Use 54.9 k

Calculate C_4 for low-frequency rolloff below 1 Hz from design Equation 5.

Example: C_4 = 2 µF. Use a good quality mylar, polystyrene, or polypropylene.

Choose gain of second amplifier.

Example: The 1 kHz gain up to the input of the second amplifier is about 26 dB for this example. For an overall 1 kHz gain equal to about 36 dB we choose:

A_{V2} = 10 dB = 3.16

Choose value for R4.

Example: R_4 = 2 k

Calculate $R_5 = (A_{V2} - 1)\,R_4$

Typical Application (continued)

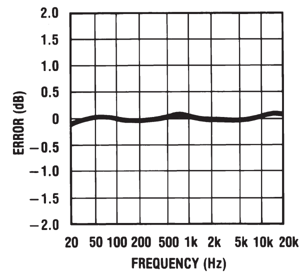
Example: R_5 = 4.32 k

Use R_5 = 4.3 k

Calculate C_0 for low-frequency rolloff below 1 Hz from design Equation 7.

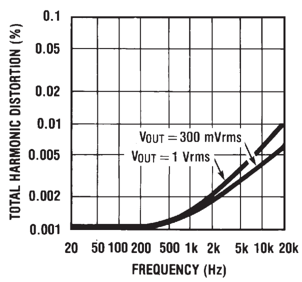
Example: C_0 = 200 µF

9.2.3 Application Curves for Output Characteristics



The maximum observed error for the prototype was 0.1 dB.

Figure 37. Deviation from Ideal RIAA Response for Circuit of Figure 36 Using 1% Resistors



The lower curve is for an output level of 300 mV_{rms} and the upper curve is for an output level of 1 V_{rms}.

Figure 38. THD of Circuit in Figure 36 as a Function of Frequency

9.3 Typical Application — Reducing Oscillation from High-Capacitive Loads

While all the previously stated operating characteristics are specified with 100-pF load capacitance, the LM833 device can drive higher-capacitance loads. However, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or oscillation. The value of the load capacitance at which oscillation occurs varies from lot-to-lot. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 39).

9.3.1 Test Schematic

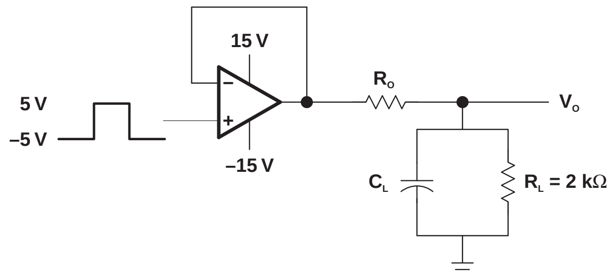


Figure 39. Capacitive Load Testing Circuit

Typical Application — Reducing Oscillation from High-Capacitive Loads (continued)

9.3.2 Output Characteristics

Figure 40 through Figure 45 demonstrate the effect adding this small resistance has on the ringing in the output signal.

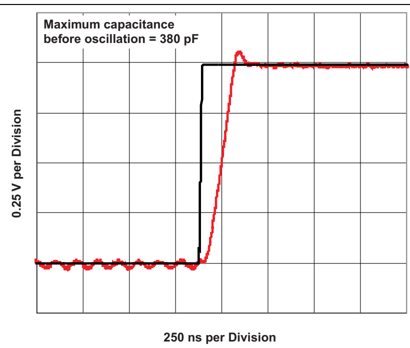


Figure 40. Pulse Response
(R_L = 600 Ω, C_L = 380 pF)

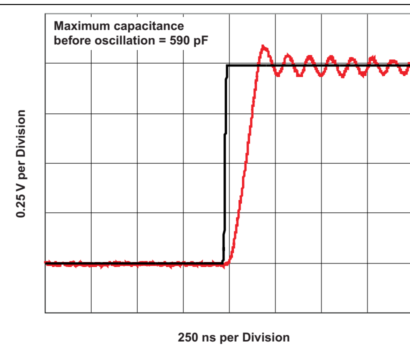


Figure 41. Pulse Response
(R_L = 2 kΩ, C_L = 560 pF)

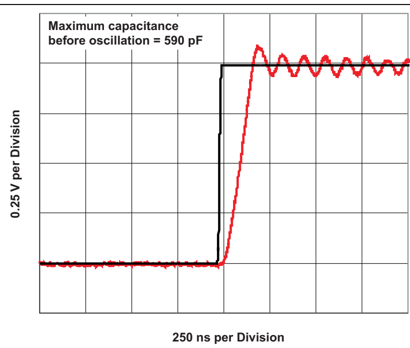


Figure 42. Pulse Response
(R_L = 10 kΩ, C_L = 590 pF)

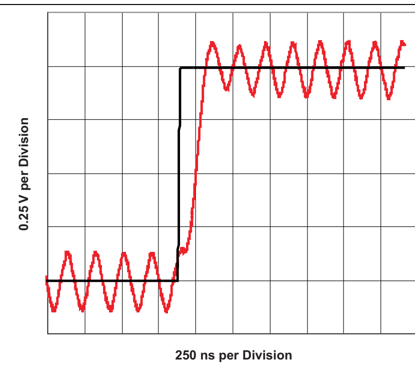


Figure 43. Pulse Response
(R_O = 0 Ω, C_O = 1000 pF,
R_L = 2 kΩ)

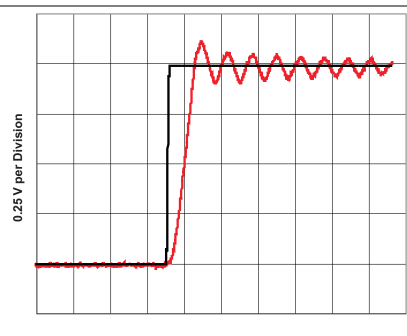


Figure 44. Pulse Response
(R_O = 4 Ω, C_O = 1000 pF,
R_L = 2 kΩ)

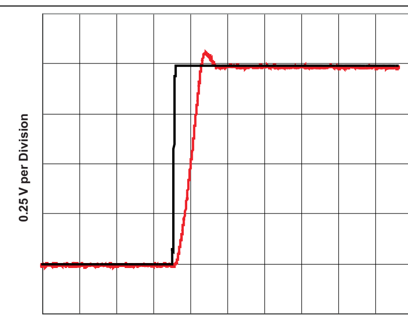


Figure 45. Pulse Response
(R_O = 35 Ω, C_O = 1000 pF,
R_L = 2 kΩ)

10 Power Supply Recommendations

The LM833 is specified for operation from 10 to 36 V (±5 to ±18 V); many specifications apply from –40°C to 85°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 36 V can permanently damage the device (see *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

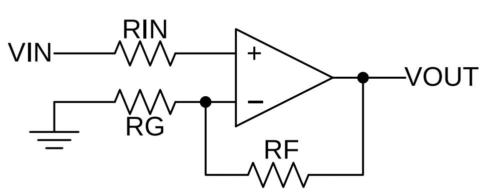


Figure 46. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

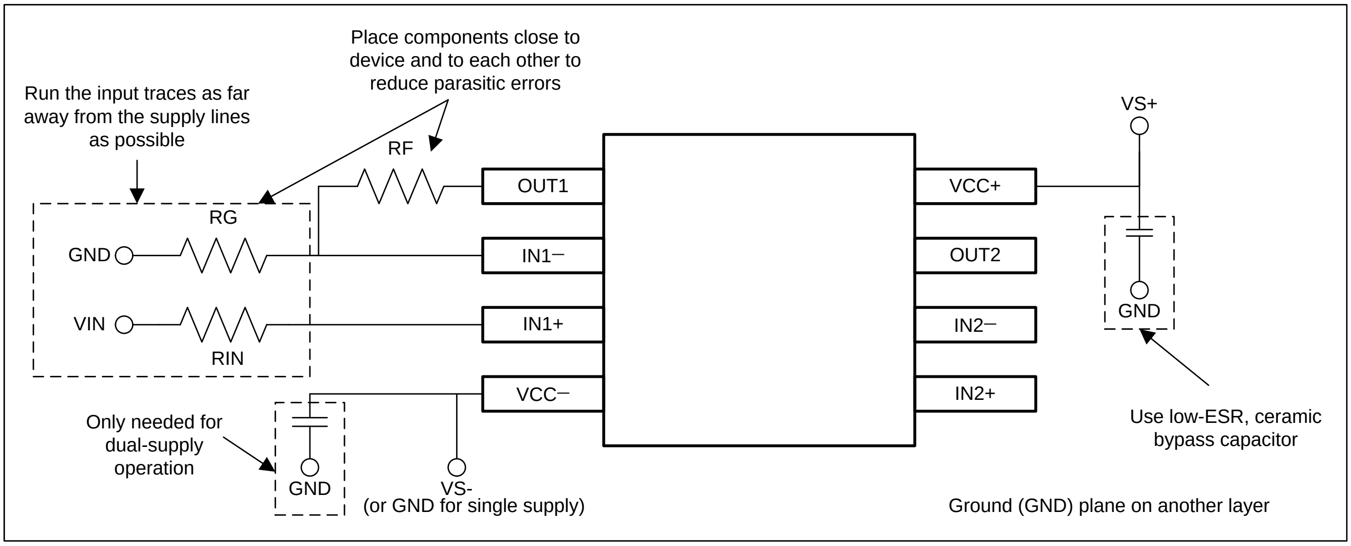


Figure 47. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM833D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	LM833
LM833DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RSU
LM833DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RSU
LM833DGKT	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 85	RSU
LM833DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM833
LM833DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM833
LM833P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LM833P
LM833P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LM833P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

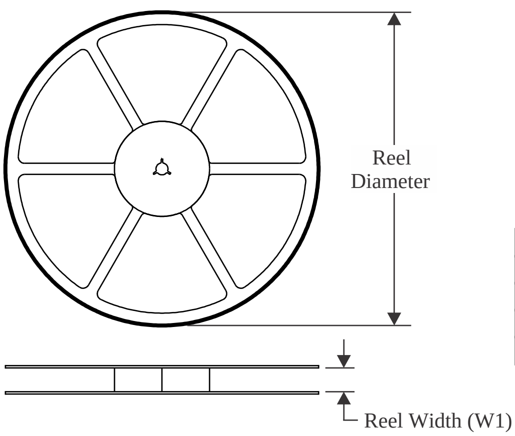
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

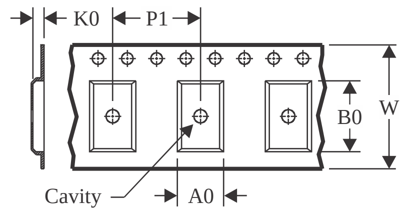
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

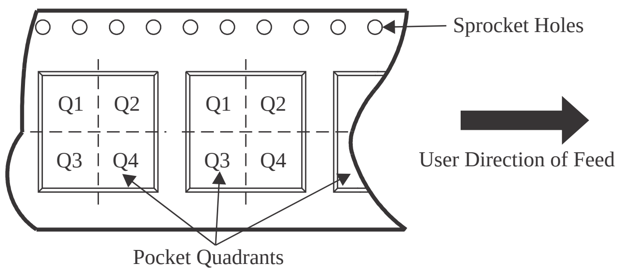


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

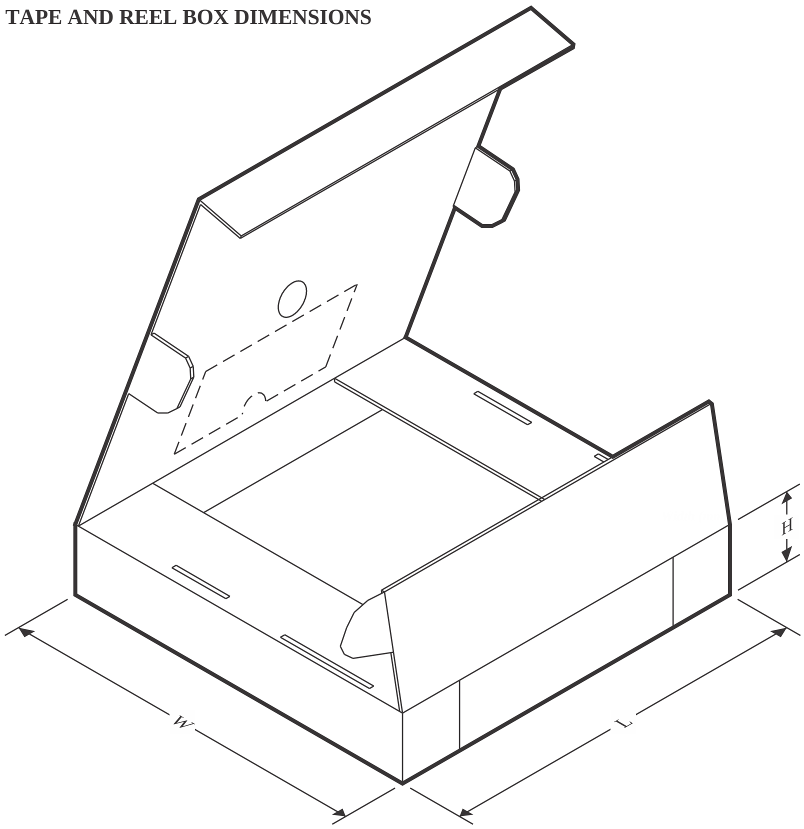
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

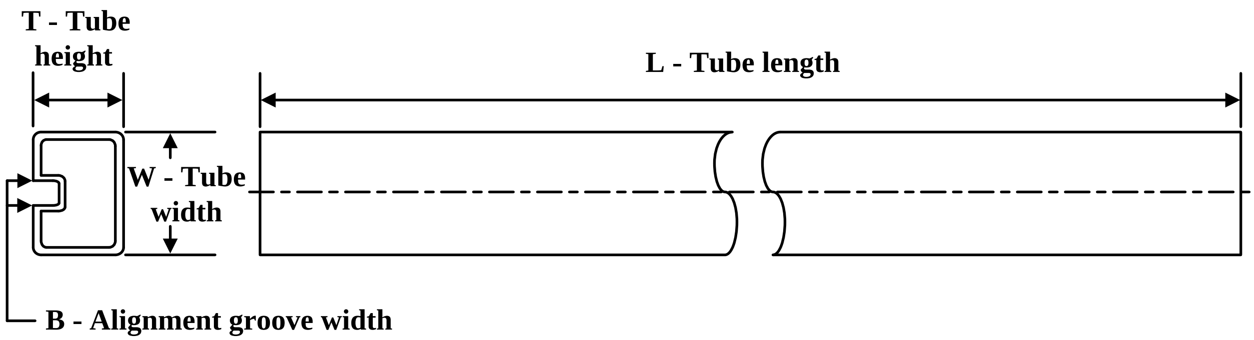
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

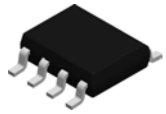
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
LM833DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM833P	P	PDIP	8	50	506	13.97	11230	4.32
LM833P.A	P	PDIP	8	50	506	13.97	11230	4.32

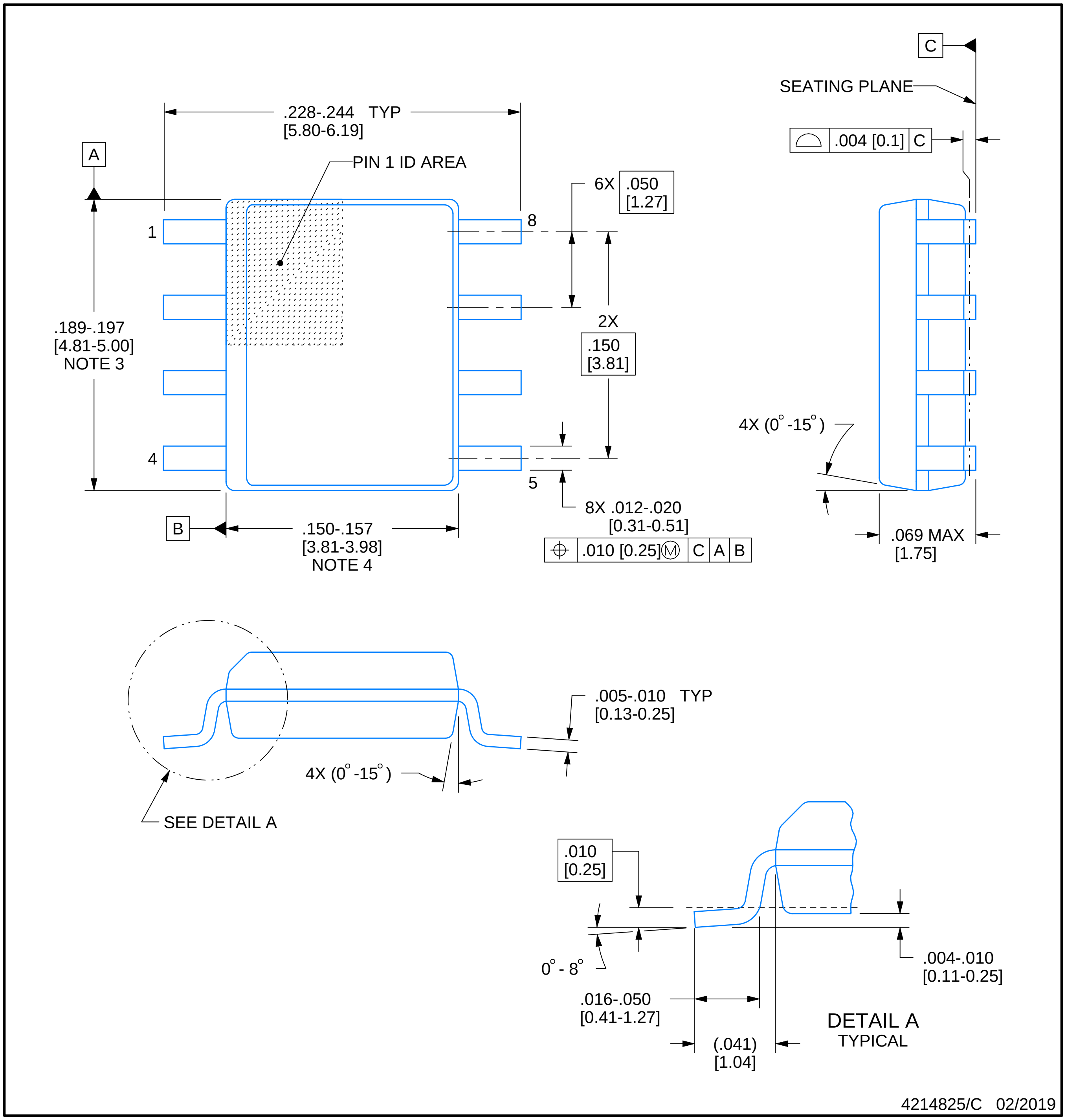


PACKAGE OUTLINE

D0008A

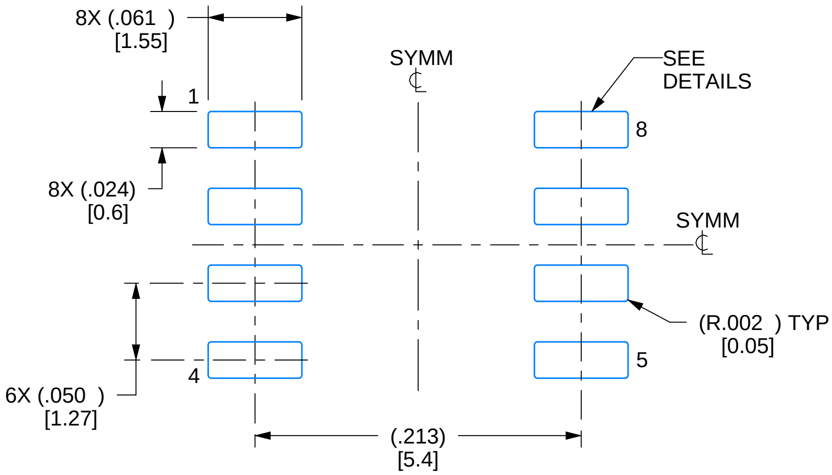
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

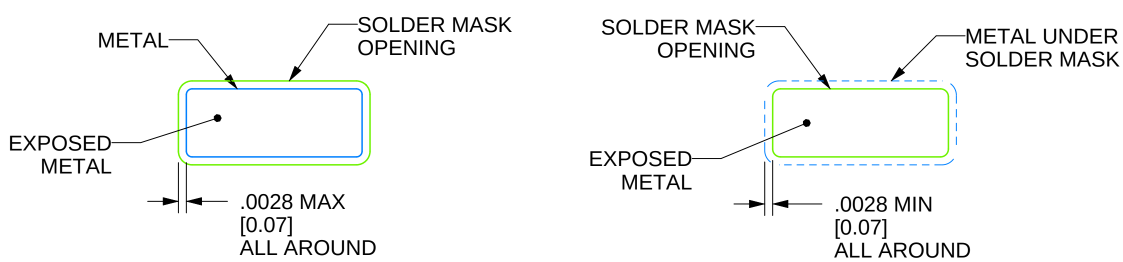


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

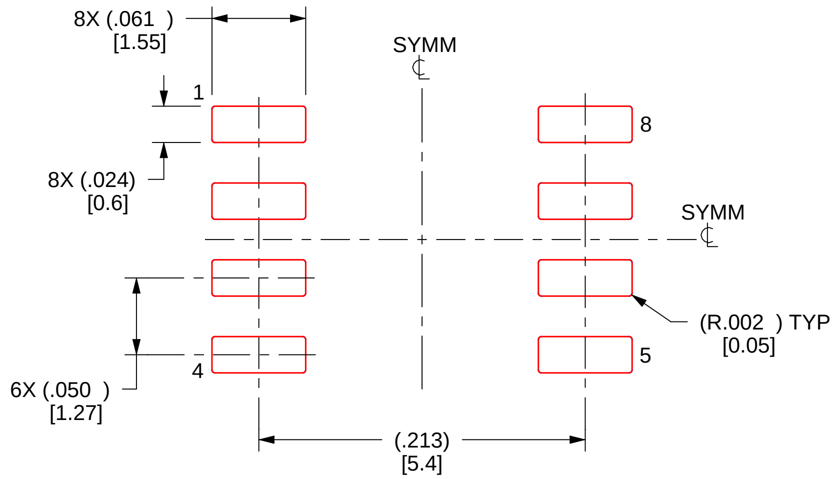
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



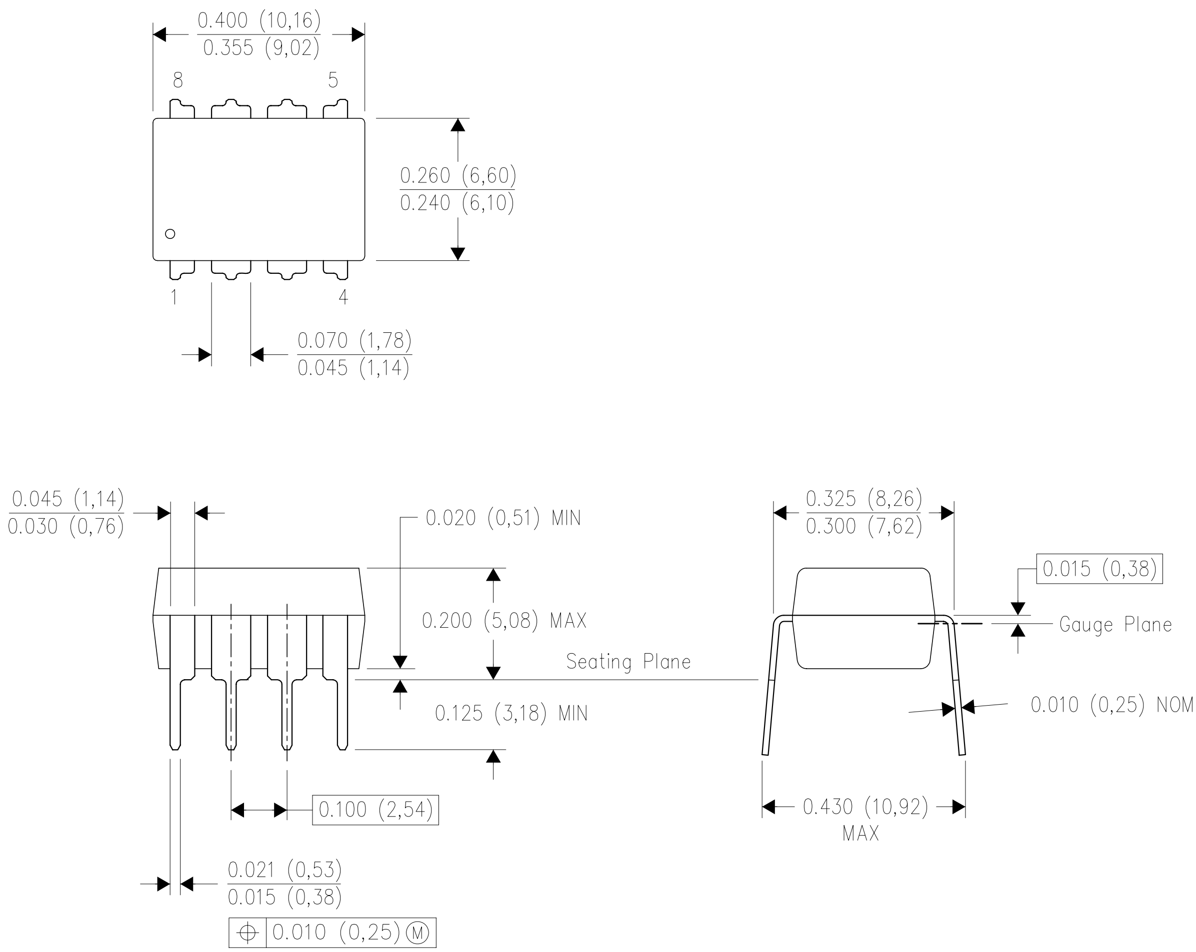
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

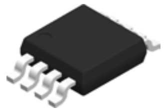
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

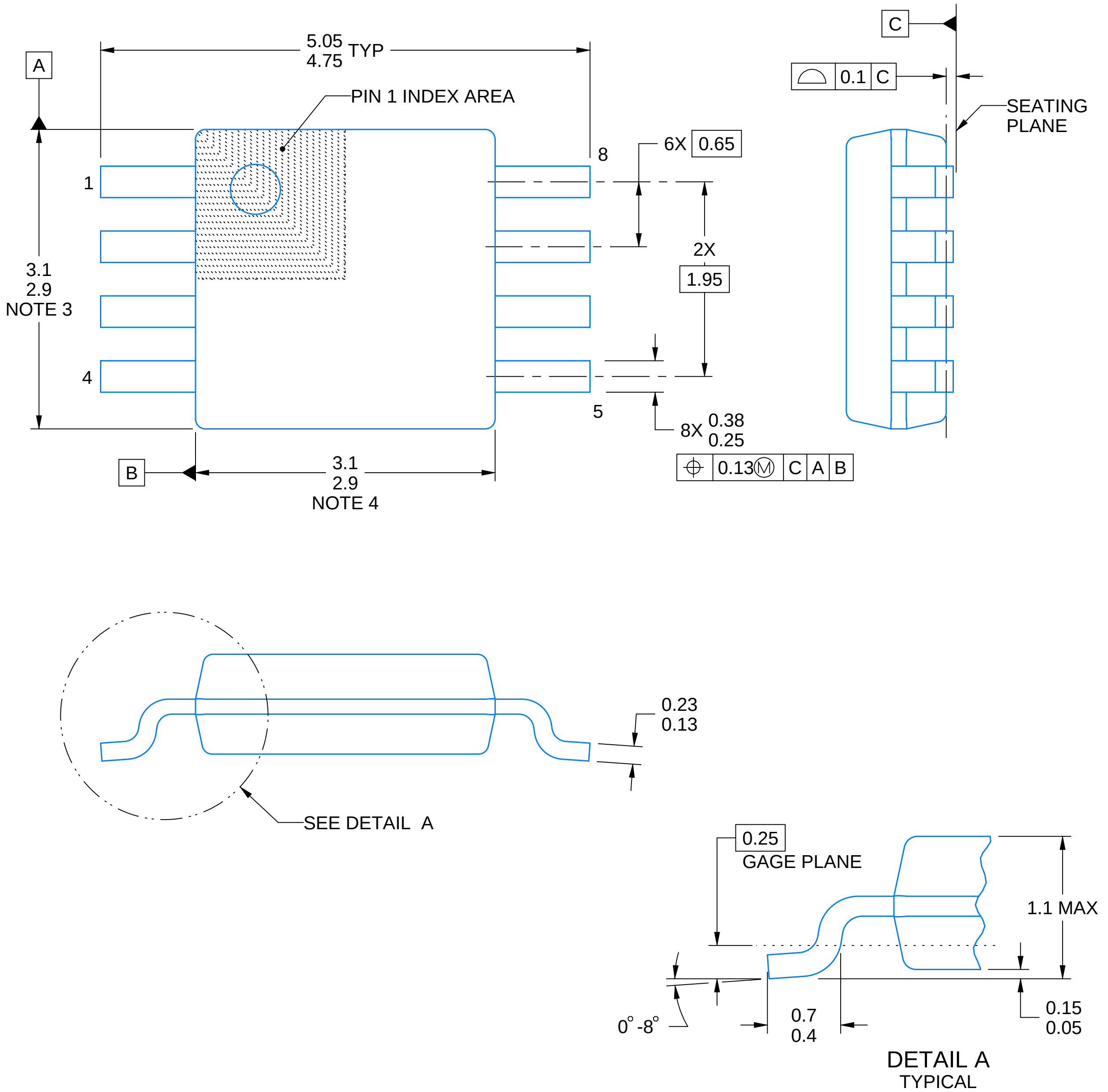
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.



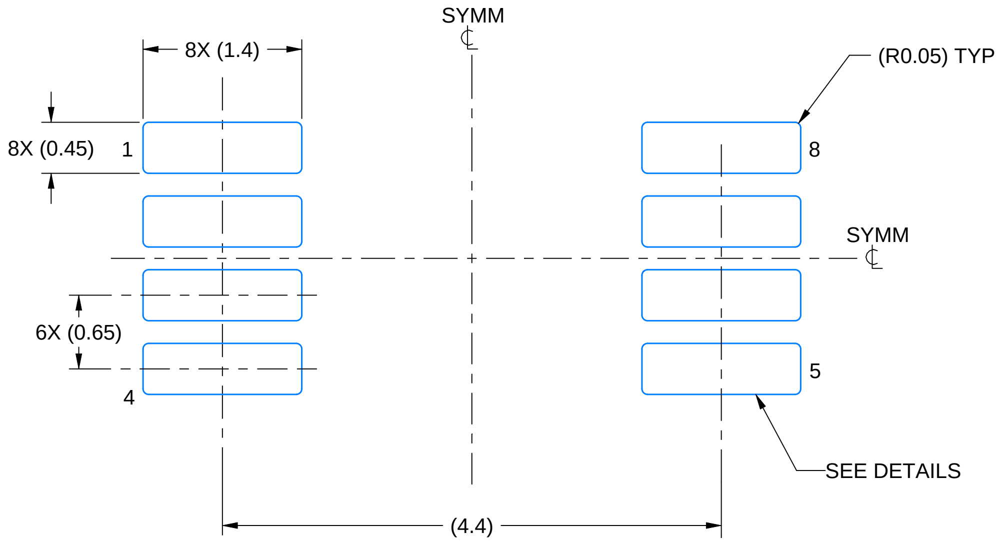


4214862/A 04/2023

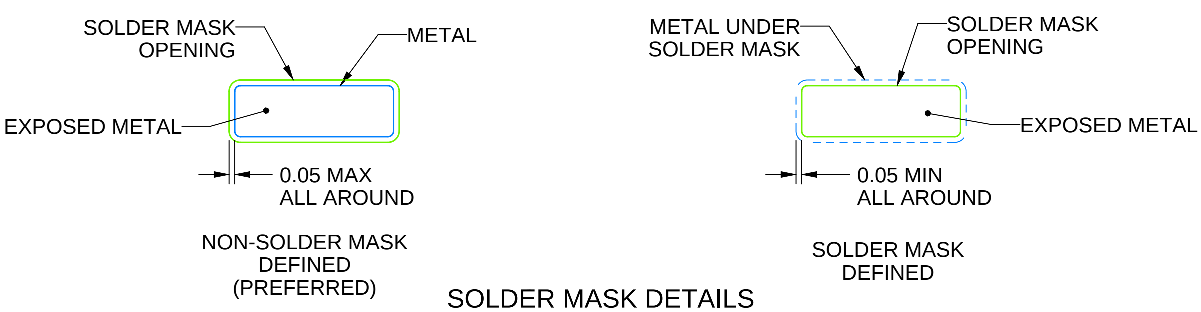
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

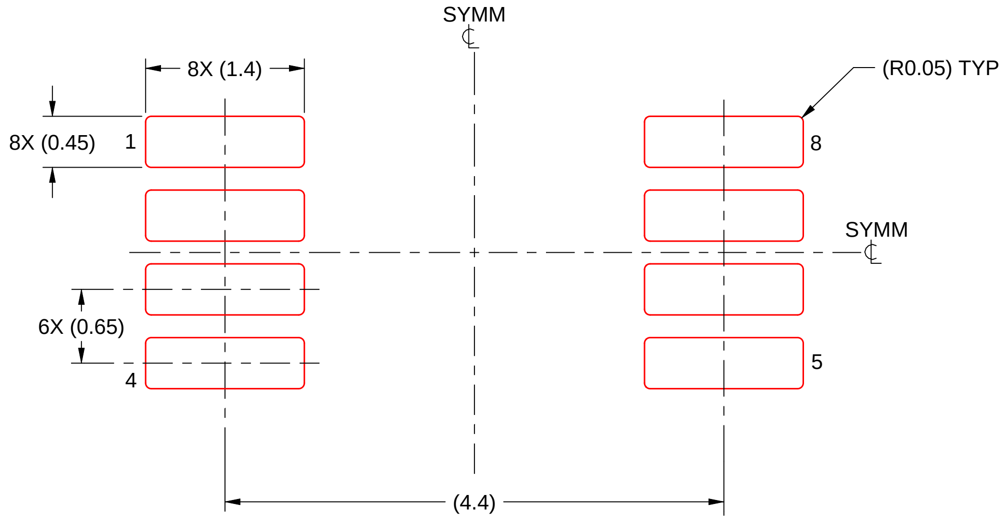


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER