LMC6001-MIL 超低入力電流アンプ

1 特長

- (特に記述のない限り最大制限値、25℃)
- 入力電流(100%テスト済み): 25fA
- 入力電流(全温度範囲): 2pA
- 低消費電力: 750µA
- 低いV_{OS}: 350µV
- 低ノイズ: 1kHz時の標準値22nV/√Hz

2 アプリケーション

- 電位計アンプ
- フォトダイオードのプリアンプ
- イオン検出器
- A.T.E.リーク試験

3 概要

LMC6001-MILデバイスは、100%テスト済みの最大25fAの入力電流、低い動作電力、2000VのESD保護を特長とし、低入力電流のオペアンプについて新たな業界のベンチマークを達成した製品です。テキサス・インスツルメンツは、モールド・コンパウンドの緻密な管理技術により、この超低入力電流を、低コストのモールド・パッケージで実現しています。

他の低入力電流オペアンプで一般的な、電源オン時の長いセトリング時間を回避するため、LMC6001-MILは動作の最初の1分間で3回テストされます。25fAの制限を満たしているユニットでも、ドリフトが発生するなら不合格になります。

入力電流ノイズが0.13fA/√Hzと非常に低いため、LMC6001-MILは高抵抗値信号源をほぼノイズなしに増幅できます。100kΩで1dB、1MΩで0.1dB、10MΩ～2,000MΩでは0.01dB以下しか加算されないため、LMC6001-MILはほぼノイズのないアンプと呼べます。

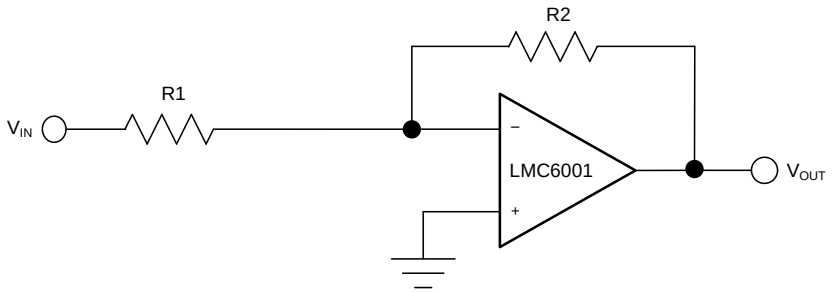
LMC6001-MILは、感受性の高い光検出トランスインピーダンス・アンプやセンサ・アンプなど、超低入力リーク電流が要求される電位計アプリケーションに理想的です。入力換算ノイズがわずか22nV/√Hzであるため、LMC6001-MILはJFET入力タイプの電位計アンプよりも高い信号/ノイズ比を実現できます。LMC6001-MILの他の用途として、長間隔の積分器、非常に高い入力インピーダンスの計測アンプ、高感度の電界測定回路が挙げられます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMC6001-MIL	PDIP (8)	9.81mm×6.35mm
	TO-99 (8)	9.08mm×9.08mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



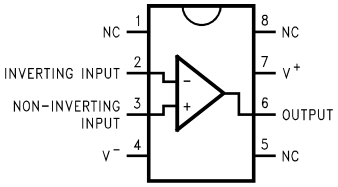
目次

4 改訂履歴

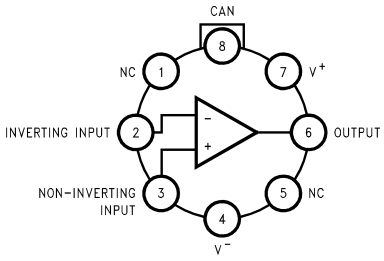
日付	改訂内容	注
	*	初版

5 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View



LMC Package
8-Pin TO-99
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP NO.	TO-99 NO.		
CAN	—	8	—	No internal connection; connected to the external casing.
+IN	3	3	I	Noninverting Input
–IN	2	2	I	Inverting Input
NC	1, 5, 8	1, 5	—	No connection
OUTPUT	6	6	O	Output
V+	7	7	—	Positive (higher) power supply
V–	4	4	—	Negative (lower) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	Unit
Differential Input Voltage	±Supply Voltage		
Voltage at Input/Output Pin	(V^+) + 0.3	(V^-) − 0.3	V
Supply Voltage $(V^+ - V^-)$	−0.3	+16	V
Output Short Circuit to V^+	See (3)(4)		
Output Short Circuit to V^-	See (3)		
Lead Temperature (Soldering, 10 Sec.)	260		°C
Junction Temperature	150		°C
Current at Input Pin	±10		mA
Current at Output Pin	±30		mA
Current at Power Supply Pin	40		mA
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not connect the output to V^+, when V^+ is greater than 13 V or reliability will be adversely affected.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{SS}	Supply input voltage	4.5	15.5	V
T_J	Operating junction temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		LMC6001-MIL		UNIT
		P (PDIP)	LMC (TO-99)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100	145	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	45	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics for LMC6001AI

Limits are ensured for T_J = 25°C unless otherwise specified. Unless otherwise specified, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, and R_L > 1 M.

PARAMETER		TEST CONDITIONS		LMC6001AI			UNIT
				MIN (1)	TYP (2)	MAX (1)	
I_B	Input Current	Either Input, V_{CM} = 0 V, V_S = ±5 V			10	25	fA
			At the temperature extremes			2000	
I_{OS}	Input Offset Current				5		
		At the temperature extremes				1000	
V_{OS}	Input Offset Voltage					0.7	mV
		At the temperature extremes				1	
		V_S = ±5 V, V_{CM} = 0 V				10	
			At the temperature extremes			1.35	
TCV_{OS}	Input Offset Voltage Drift				2.5		µV/°C
R_{IN}	Input Resistance				>1		TΩ
CMRR	Common Mode	0 V ≤ V_{CM} ≤ 7.5 V		75	83		dB
	Rejection Ratio	V^+ = 10 V	At the temperature extremes	72			
+PSRR	Positive Power Supply Rejection Ratio	5 V ≤ V^+ ≤ 15 V		73	83		
			At the temperature extremes	70			
−PSRR	Negative Power Supply Rejection Ratio	0 V ≥ V^- ≥ −10 V		80	94		
			At the temperature extremes	77			
A_V	Large Signal Voltage Gain	Sourcing, R_L = 2 kΩ (3)		400	1400		V/mV
				300			
		Sinking, R_L = 2 kΩ (3)		180	350		
			At the temperature extremes	100			

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) V^+ = 15 V, V_{CM} = 7.5 V and R_L connected to 7.5 V. For Sourcing tests, 7.5 V ≤ V_O ≤ 11.5 V. For Sinking tests, 2.5 V ≤ V_O ≤ 7.5 V.

DC Electrical Characteristics for LMC6001AI (continued)

Limits are ensured for T_J = 25°C unless otherwise specified. Unless otherwise specified, V^+ = 5 V, V^- = 0 V, V_{CM} = 1.5 V, and R_L > 1 M.

PARAMETER		TEST CONDITIONS			LMC6001AI			UNIT
					MIN(1)	TYP(2)	MAX(1)	
V_{CM}	Input Common-Mode Voltage	V^+ = 5 V and 15 V For CMRR ≥ 60 dB	V_{CM} Low			–0.4	–0.1	V
				At the temperature extremes			0	
			V_{CM} High		V^+ − 2.3	V^+ − 1.9		
				At the temperature extremes	V^+ − 2.5			
V_O	Output Swing	V^+ = 15 V, R_L = 2 kΩ to 2.5 V	V_O Low			0.1	0.14	V
				At the temperature extremes			0.17	
			V_O High		4.8	4.87		
				At the temperature extremes	4.73			
		V^+ = 15 V, R_L = 2 kΩ to 7.5 V	V_O Low			0.26	0.35	
				At the temperature extremes			0.45	
			V_O High		14.5	14.63		
				At the temperature extremes	14.34			
I_O	Output Current	Sourcing, V^+ = 5 V, V_O = 0 V			16	22		mA
			At the temperature extremes		10			
		Sinking, V^+ = 5 V, V_O = 5 V			16	21		
			At the temperature extremes		13			
		Sourcing, V^+ = 15 V, V_O = 0 V			28	30		
			At the temperature extremes		22			
		Sinking, V^+ = 15 V, V_O = 13 V(4)			28	34		
			At the temperature extremes		22			
I_S	Supply Current	V^+ = 5 V, V_O = 1.5 V				450	750	µA
			At the temperature extremes				900	
		V^+ = 15 V, V_O = 7.5 V				550	850	
			At the temperature extremes				950	

(4) Do not connect the output to V + , when V + is greater than 13 V or reliability will be adversely affected.

6.6 Dissipation Ratings

	MIN	MAX	UNIT
Power Dissipation	See (1)		

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

6.7 Typical Characteristics

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

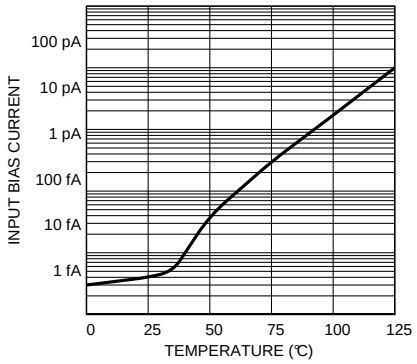
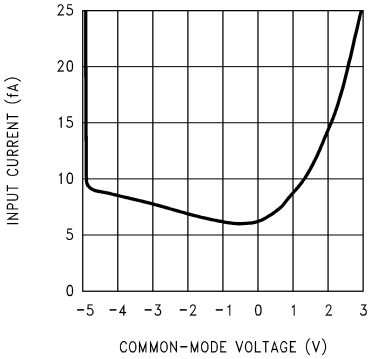


Figure 1. Input Current vs. Temperature



V_S = ±5 V

Figure 2. Input Current vs. V_{CM}

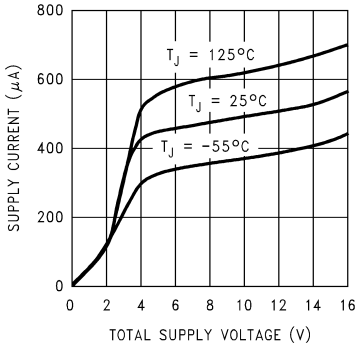


Figure 3. Supply Current vs. Supply Voltage

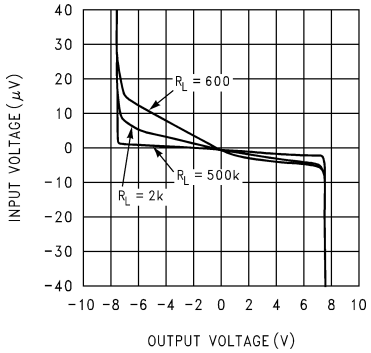


Figure 4. Input Voltage vs. Output Voltage

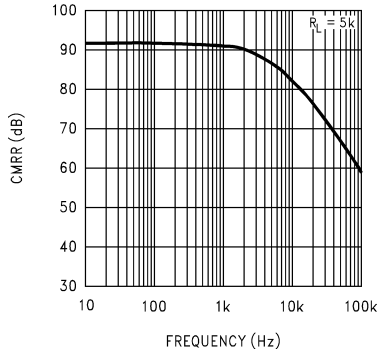


Figure 5. Common-Mode Rejection Ratio vs. Frequency

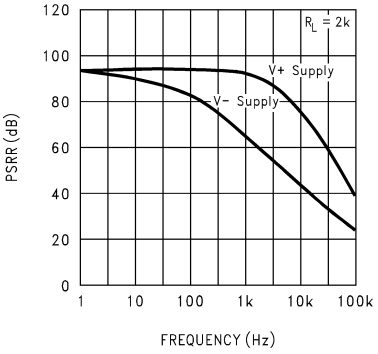


Figure 6. Power Supply Rejection Ratio vs. Frequency

Typical Characteristics (continued)

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

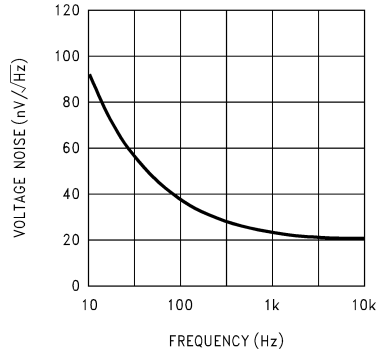


Figure 7. Input Voltage Noise vs. Frequency

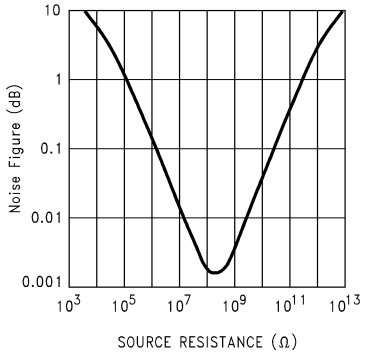


Figure 8. Noise Figure vs. Source Resistance

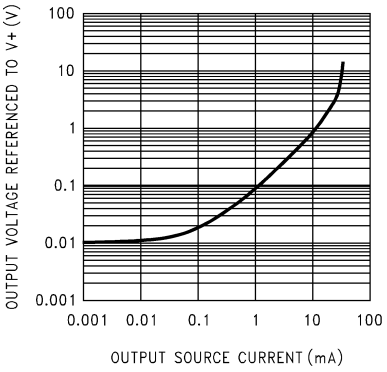


Figure 9. Output Characteristics Sourcing Current

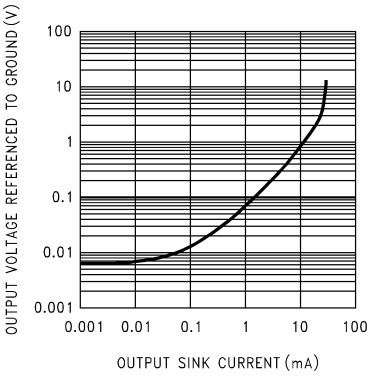


Figure 10. Output Characteristics Sinking Current

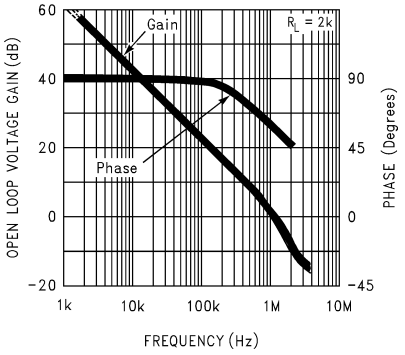
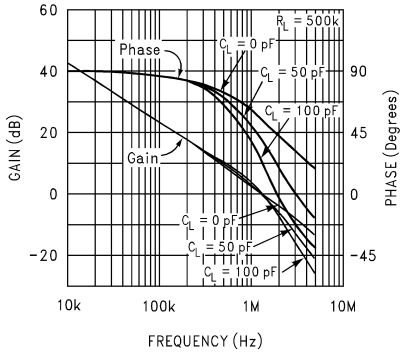


Figure 11. Gain and Phase Response vs. Temperature (−55°C to +125°C)



R_L = 500 kω

Figure 12. Gain and Phase Response vs. Capacitive Load

Typical Characteristics (continued)

V_S = ±7.5 V, T_A = 25°C, unless otherwise specified

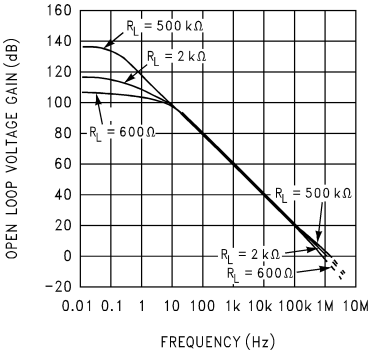


Figure 13. Open-Loop Frequency Response

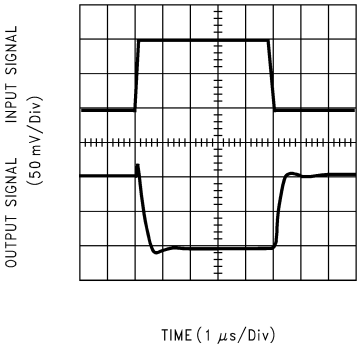


Figure 14. Inverting Small Signal Pulse Response

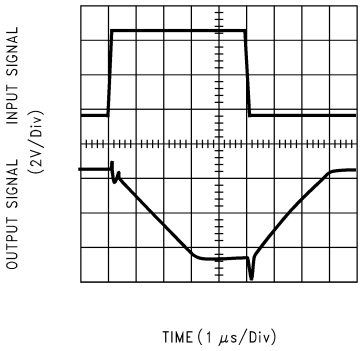


Figure 15. Inverting Large Signal Pulse Response

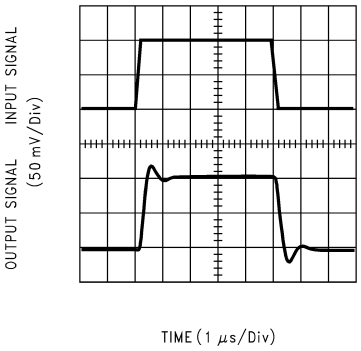


Figure 16. Noninverting Small Signal Pulse Response

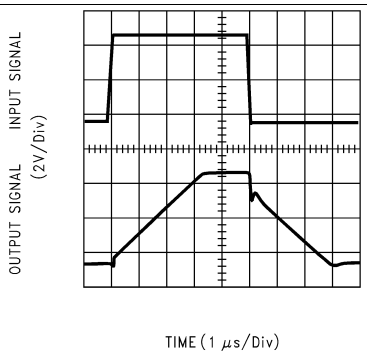


Figure 17. Noninverting Large Signal Pulse Response

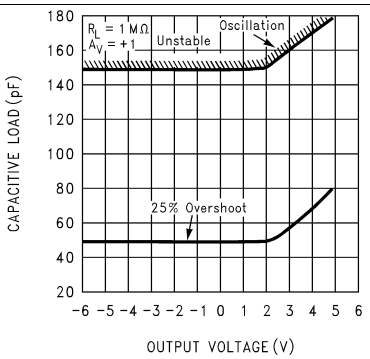


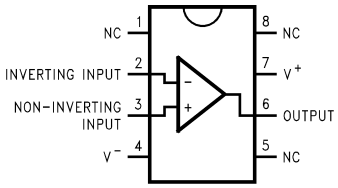
Figure 18. Stability vs. Capacitive Load

7 Detailed Description

7.1 Overview

LMC6001-MIL has an extremely low input current of 25 fA. In addition, its ultra-low input current noise of 0.13 fA/√Hz allows almost noiseless amplification of high-resistance signal sources. LMC6001-MIL is ideally suited for electrometer applications requiring ultra-low input leakage current such as sensitive photodetection transimpedance amplifiers and sensor amplifiers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Amplifier Topology

The LMC6001-MIL incorporates a novel op amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional op amps. These features make the LMC6001-MIL both easier to design with, and provide higher speed than products typically found in this low-power class.

7.3.2 Latch-up Prevention

CMOS devices tend to be susceptible to latch-up due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6001-MIL is designed to withstand 100-mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latch-up mode. Limiting current to the supply pins will also inhibit latch-up susceptibility.

7.4 Device Functional Modes

The LMC6001-MIL has a single functional mode and operates according to the conditions listed in *Recommended Operating Conditions*.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6001.

Although the LMC6001 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and printed-circuit-board parasitics, reduce phase margins.

When high input impedances are demanded, TI suggests guarding the LMC6001. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. See *Printed-Circuit-Board Layout For High-Impedance Work*.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 19) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

Because it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 (SNOSBZ3) and LMC662 (SNOSC51) for a more detailed discussion on compensating for input capacitance.

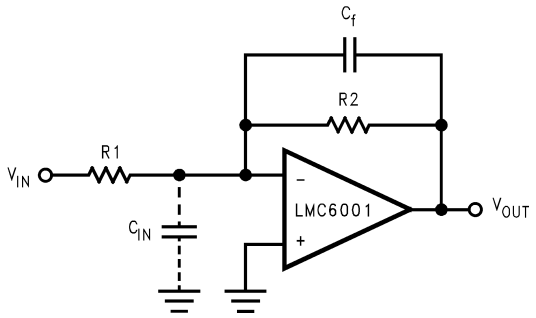


Figure 19. Cancelling the Effect of Input Capacitance

8.1.2 Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load. See *Typical Characteristics*.

Direct capacitive loading will reduce the phase margin of many op amps. A pole in the feedback loop is created by the combination of the output impedance of the op amp and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 20.

Application Information (continued)

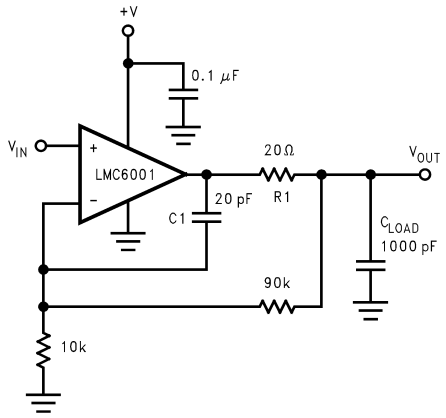


Figure 20. LMC6001 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 20, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the inverting input of the amplifier, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (Figure 21). Typically a pullup resistor conducting 500 µA or more will significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open-loop gain of the amplifier can also be affected by the pullup resistor. See *DC Electrical Characteristics for LMC6001AI*.

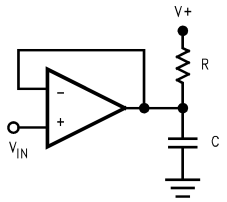


Figure 21. Compensating for Large Capacitive Loads with a Pullup Resistor

8.2 Typical Application

The extremely high input resistance, and low power consumption, of the LMC6001 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, electrostatic field detectors and gas chromotographs.

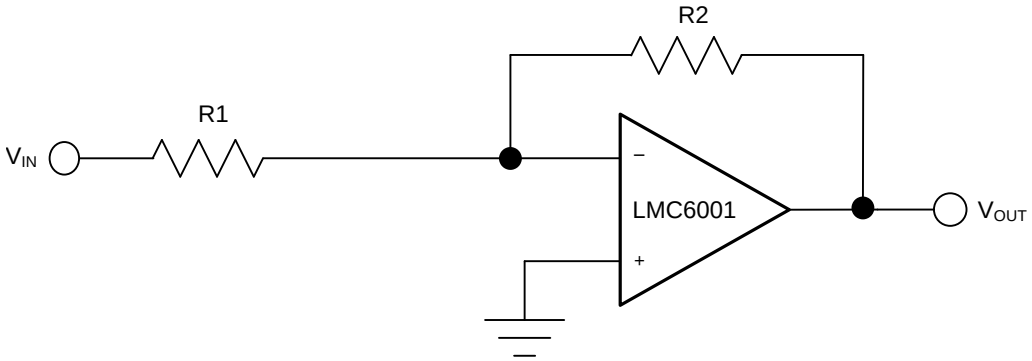


Figure 22. Typical Application Schematic, LMC6001

Typical Application (continued)

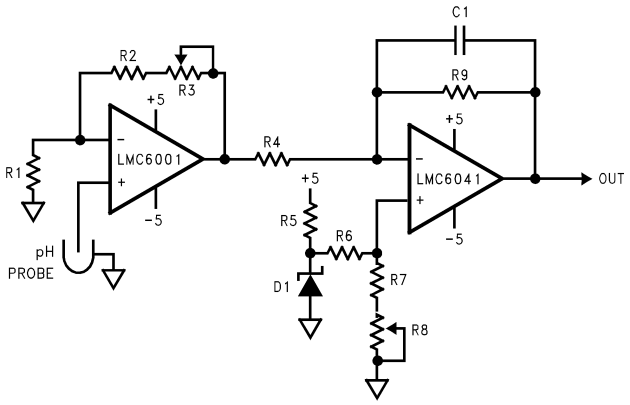
8.2.1 Two Op Amp, Temperature Compensated Ph Probe Amplifier

The signal from a pH probe has a typical resistance between 10 MΩ and 1000 MΩ. Because of this high value, it is very important that the amplifier input currents be as small as possible. The LMC6001 with less than 25-fA input current is an ideal choice for this application.

The LMC6001 amplifies the probe output providing a scaled voltage of ±100 mV/pH from a pH of 7. The second op amp, a micropower LMC6041 provides phase inversion and offset so that the output is directly proportional to pH, over the full range of the probe. The pH reading can now be directly displayed on a low-cost, low-power digital panel meter. Total current consumption will be about 1 mA for the whole system.

The micropower dual-operational amplifier, LMC6042, would optimize power consumption but not offer these advantages:

1. The LMC6001A ensures a 25-fA limit on input current at 25°C.
2. The input ESD protection diodes in the LMC6042 are only rated at 500 V while the LMC6001 has much more robust protection that is rated at 2000 V.



(1)

R1 100 k + 3500 ppm/°C

R2 68.1 k

R3, 8 5 k

R4, 9 100 k

R5 36.5 k

R6 619 k

R7 97.6 k

D1 LM4040D1Z-2.5

C1 2.2 µF

(2) µΩ style 137 or similar

Figure 23. Ph Probe Amplifier

8.2.1.1 Design Requirements

The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with 0 V out at a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature-compensating resistor, R1, is placed in the feedback loop. This cancels the temperature dependence of the probe. This resistor must be mounted where it will be at the same temperature as the liquid being measured.

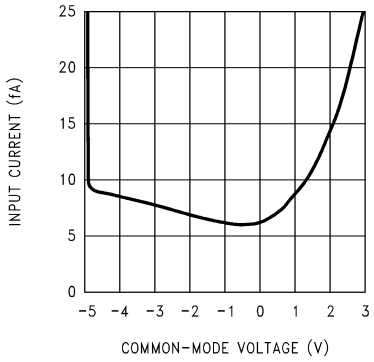
8.2.1.2 Detailed Design Procedure

The set-up and calibration is simple with no interactions to cause problems.

Typical Application (continued)

1. Disconnect the pH probe and with R3 set to about mid-range and the noninverting input of the LMC6001 grounded, adjust R8 until the output is 700 mV.
2. Apply −414.1 mV to the noninverting input of the LMC6001. Adjust R3 for and output of 1400 mV. This completes the calibration. As real pH probes may not perform exactly to theory, minor gain and offset adjustments should be made by trimming while measuring a precision buffer solution.

8.2.1.3 Application Curve



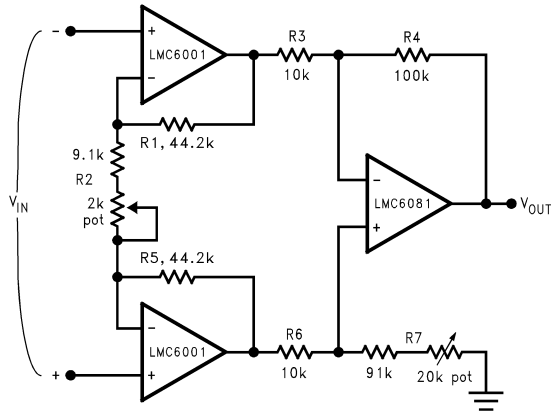
V_S = ±5 V

Figure 24. Input Current vs. V_{CM}

8.3 System Example

8.3.1 Ultra-Low Input Current Instrumentation Amplifier

Figure 25 shows an instrumentation amplifier that features high-differential and common-mode input resistance (>10^{14}Ω), 0.01% gain accuracy at A_V = 1000, excellent CMRR with 1-MΩ imbalance in source resistance. Input current is less than 20 fA and offset drift is less than 2.5 µV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low-drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.85k).

Figure 25. Instrumentation Amplifier

9 Power Supply Recommendations

See the *Recommended Operating Conditions* for the minimum and maximum values for the supply input voltage and operating junction temperature.

10 Layout

10.1 Layout Guidelines

10.1.1 Printed-Circuit-Board Layout For High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PCB. When one wishes to take advantage of the ultra-low bias current of the LMC6001, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PCB, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the inputs of the LMC6001 and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth, connected to the inputs of the op amp, as in Figure 30. To have a significant effect, guard rings must be placed on both the top and bottom of the PCB. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10 TΩ, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input.

This would cause a 500 times degradation from the LMC6001's actual performance. If a guard ring is used and held within 1 mV of the inputs, then the same resistance of 10 TΩ will only cause 10 fA of leakage current. Even this small amount of leakage will degrade the extremely low input current performance of the LMC6001. See Figure 28 for typical connections of guard rings for standard op amp configurations.

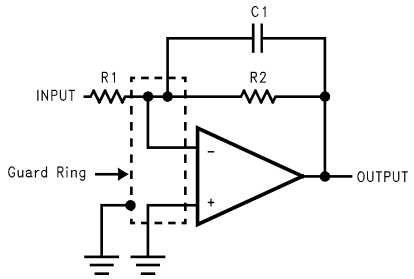


Figure 26. Inverting Amplifier

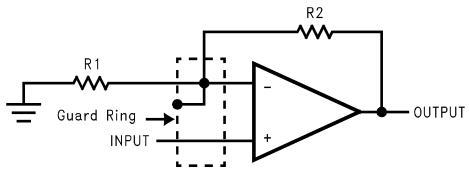


Figure 27. Noninverting Amplifier

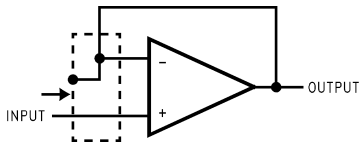
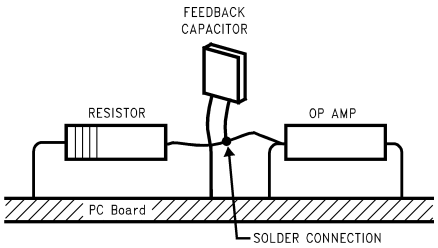


Figure 28. Typical Connections of Guard Rings

Layout Guidelines (continued)

The designer should be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 29.



(Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB).

Figure 29. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LMC6001 is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

10.2 Layout Example

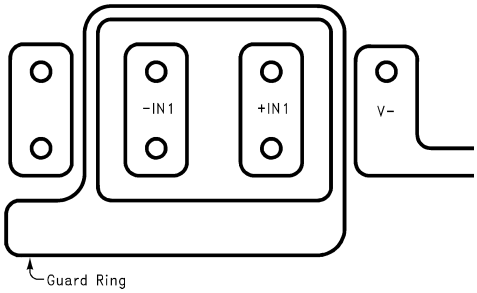


Figure 30. Examples of Guard Ring in PCB Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『*LMC660 CMOSクワッド・オペアンプ*』、SNOSBZ3
- 『*LMC662 CMOSクワッド・オペアンプ*』、SNOSC51

11.2 関連リンク

表 1 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMC6001-MIL	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6001A MDC	Active	Production	DIESALE (Y) | 0	270 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	
LMC6001A-MDC.A	Active	Production	DIESALE (Y) | 0	270 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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最終更新日：2025 年 10 月