LMG1020 5V、7A、5AのローサイドGaNおよびMOSFETドライバ、1nsパルス幅のアプリケーション用

1 特長

- GaNおよびシリコンFET用の超高速ローサイド・ゲート・ドライバ
- 最小入力パルス幅: 1ns
- 最高60MHzでの動作
- 標準2.5ns、最大4.5nsの伝搬遅延
- 400psの標準立ち上がりおよび立ち下がり時間
- 7Aピーク・ソース電流および5Aピーク・シンク電流
- 5Vの電源電圧
- UVLOおよび過熱保護
- 0.8mm×1.2mmのWCSPパッケージ

2 アプリケーション

- LiDAR
- タイム・オブ・フライト(ToF)レーザー・ドライバ
- 顔認識
- クラスEワイヤレス充電器
- VHF共振電力コンバータ
- GaNベースの同期整流器
- 拡張現実

3 概要

LMG1020デバイスはシングル、ローサイドのドライバで、LiDAR、タイム・オブ・フライト、顔認識などの高速アプリケーションや、ローサイド・ドライバを使用するあらゆる電力コンバータで、GaN FETおよびロジック・レベルMOSFETを駆動するよう設計されています。LMG1020は設計が単純なため、伝播遅延が2.5ナノ秒と非常に短く、最小で1ナノ秒のパルス幅に対応できます。ゲートと、OUTHおよびOUTLとの間に外付けの抵抗を接続することで、それぞれプルアップ・エッジとプルダウン・エッジの駆動強度を独立に設定できます。

ドライバには、過負荷またはフォルト状況に対応するため、低電圧誤動作防止(UVLO)および過熱保護(OTP)機能があります。

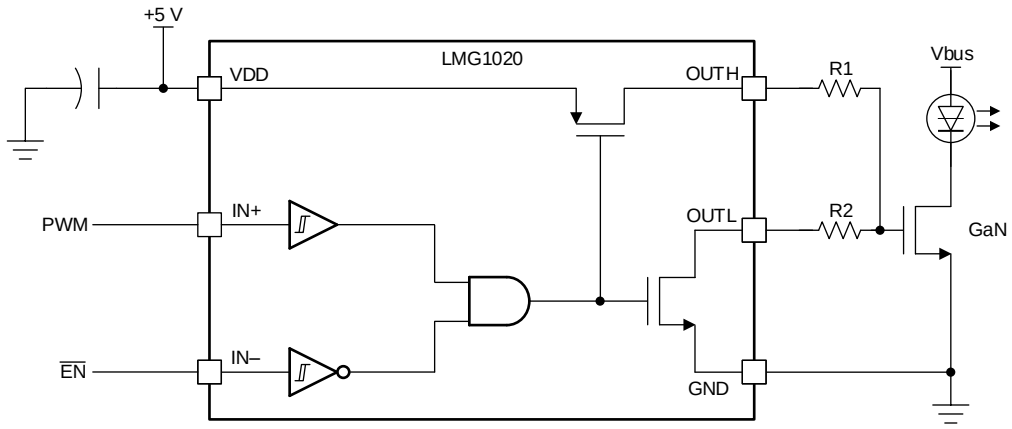
LMG1020は0.8mm×1.2mmのWCSPパッケージを使用しており、ゲート・ループのインダクタンスが最小化され、高周波数のアプリケーションで電力密度を最大化できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMG1020	WCSP (6)	0.80mm×1.20mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

LiDARドライバ段の概略図



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4 改訂履歴

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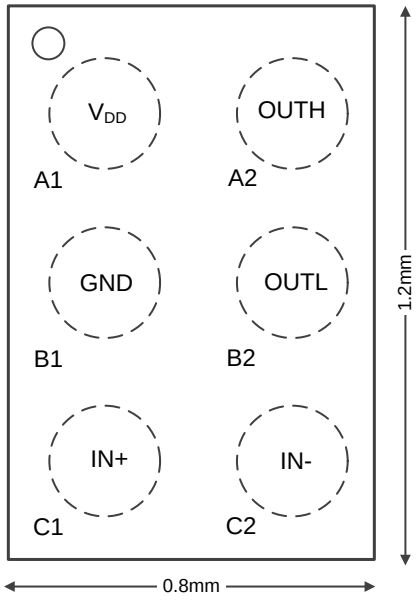
5 Pin Configuration and Functions

YFF Package
6-Ball WCSP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	B1	—	Ground
IN+	C1	I	Positive logic-level input
IN–	C2	I	Negative logic-level input
OUTL	B2	O	Pulldown gate drive output. Connect through an optional resistor to the target transistor's gate
OUTH	A2	O	Pullup gate drive output. Connect through a resistor to the target transistor's gate
VDD	A1	I	Input voltage supply. Decouple through a small size, low inductance capacitor to GND

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		5.75	V
V_{IN}	IN+, IN- pin voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	OUTH, OUTL pin voltage	-0.3	5.75	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Operating Temperature	-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.4	V
V_{INx}	IN+ or IN- input voltage	0		V_{DD}	V
T_J	Operating Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN1020 YFF (WCSP) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	38.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (VDD=5V unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
$I_{VDD, Q}$	VDD Quiescent Current	IN_+ = IN_- = 0 V			75	µA
$I_{VDD, op}$	VDD Operating Current(1)	fsw = 30 MHz, 2 Ω, 0.1 pF load		40		mA
		fsw = 30 MHz, 2 Ω, 100 pF load		51		mA
$V_{DD, UVLO}$	Under-voltage Lockout	V_{DD} rising	4.06	4.19	4.33	V
$\Delta V_{DD, UVLO}$	UVLO Hysteresis			85		mV
T_{OTP}	Over temperature shutdown, rising edge threshold			170		°C
ΔT_{OTP}	Over temperature hysteresis			18		°C
Input DC Characteristics						
V_{IH}	IN+, IN- high threshold		1.7		2.6	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.5		1	V
R_{IN+}	Positive input pull-down resistance	To GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to V_{DD}	100	150	250	kΩ
C_{IN}	Input pin capacitance(1)	To GND		1.3		pF
Output DC Characteristics						
V_{OL}	OUTL voltage	I_{OUTL} = 100 mA, IN+= IN- = 0 V			36	mV
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH} = 100 mA, IN+= 5 V, IN- = 0 V			50	mV
I_{OH}	Peak source current(1)	V_{OUTH} = 0 V, IN+= 5 V, IN- = 0 V		7		A
I_{OL}	Peak sink current(1)	V_{OUTL} = 5 V, IN+= IN- = 0 V		5		A

(1) Insured by design

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6.6 Switching Characteristics

over operating free-air temperature range (VDD=5V unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{start}	Startup Time, V_{DD} rising above UVLO	IN- = GND, IN+ = V_{DD} , V_{DD} rising to 4.2V to OUTH rising		40	70	µs
$t_{shut-off}$	ULVO falling	IN- = GND, IN+ = VDD , VDD falling below 4.1V to OUTH falling	1	1.9	3.1	µs
$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100 pF load	1.5	2.5	4.1	ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100 pF load	1.8	2.6	4.3	ns
Δt_{pd}	Pulse positive distrortion ($t_{pd, f}$ - $t_{pd, r}$)			230	603	ps
t_{rise}	Output rise time	0Ω series 100 pF load(1)		375		ps
t_{fall}	Output fall time	0Ω series 100 pF load(1)		350		ps
t_{min}	Minimum input pulse width	0Ω series 100 pF load(1)		1		ns

(1) rise and fall calulated as a 20% to 80%

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6.7 Typical Characteristics

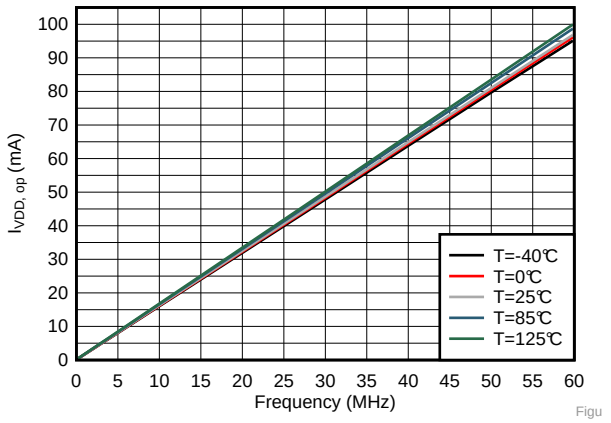


図 1. $I_{VDD, op}$ vs Frequency With 2 Ω Series 100 pF Load

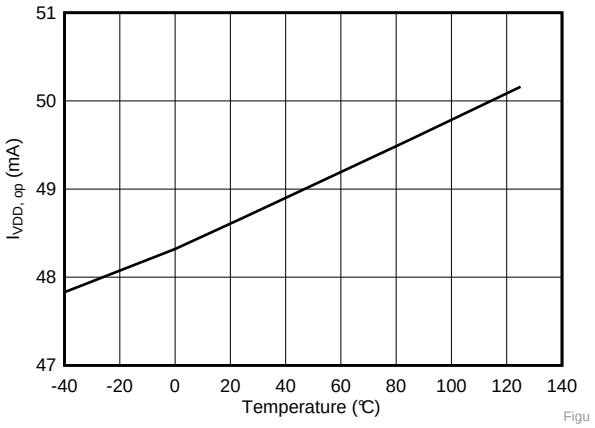


図 2. $I_{VDD, op}$ vs Temperature At 30MHz With 2 Ω series 100 pF Load

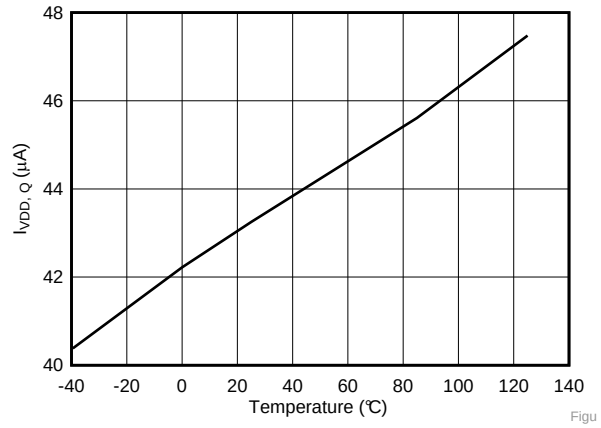


図 3. Quiescent Current vs Temperature

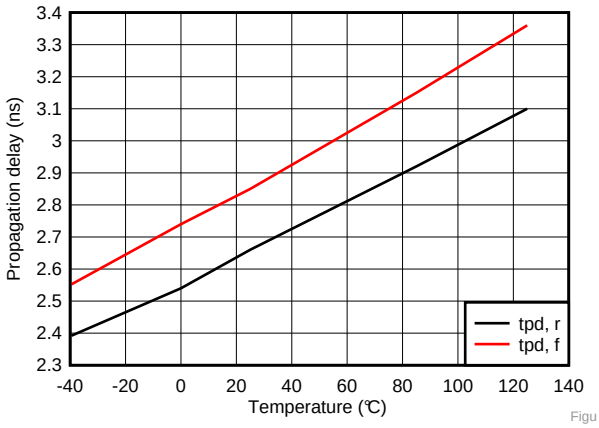


図 4. Propagation Delay vs Temperature

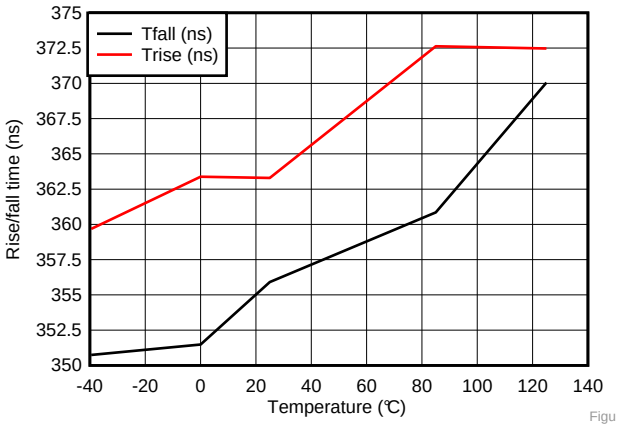


図 5. Rise And Fall Time vs Temperature With 0 Ω Series 100 pF Load

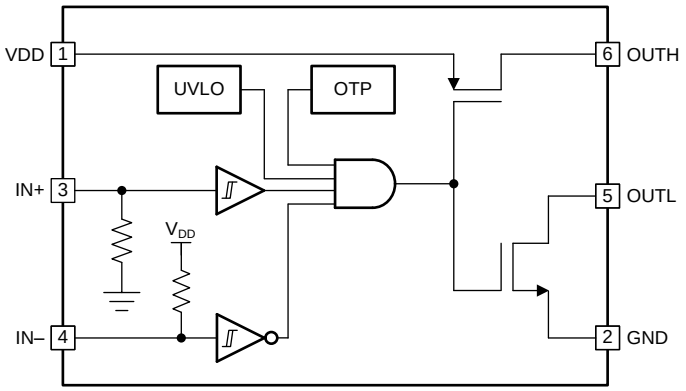
7 Detailed Description

7.1 Overview

LMG1020 is a high-performance low-side 5-V gate driver for GaN and logic-level silicon power transistors. While the LMG1020 is designed for high-speed applications, such as wireless power transmission and LiDAR applications, it is a high-performance solution for any other low-side driving applications.

The LMG1020 is optimized to provide the lowest propagation delay through the driver to the power transistor. LMG1020 is in a small 0.8×1.2mm WCSP ball-grid array package in order to minimize its parasitic inductance. This low inductance design helps achieve high current, low ringing performance in very high frequency operation when driving power FETs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Stage

The input stage features two Schmitt-triggers at the pins IN+ and IN– to reduce sensitivity to noise on the inputs. IN+ signal and the inverted IN– signal are both sent to an AND gate. IN+ is connected with a pull-down resistor while IN– is connected with a pull-up resistor to prevent unintended turnon. The output signal will follow the difference between IN+ and IN–. Both IN+ and IN– are single ended inputs, and these two pins cannot be used as a differential input pair.

7.3.2 Output Stage

LMG1020 provides 7-A source, 5-A sink (asymmetrical drive) peak-drive current capability, and features a split output configuration. The OUTH and OUTL outputs of the LMG1020 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently adjust the turnon and turnoff drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver. The output stage OUTL is also pulled down in undervoltage condition, which prevents the unintended charge accumulation of device C_{iss}.

7.3.3 V_{DD} and undervoltage lockout

LMG1020 features nominal 5V and maximum 5.25V of supply voltage, and its absolute maximum supply voltage is 5.75 V. In the design, it is recommended to limit the variability of the power supply to be within 5% (0.25V), and the overshoot voltage during switching transient not to exceed the absolute maximum voltage. Refer to Section VDD and Overshoot for more the detailed design guide.

LMG1020 also features internal undervoltage lockout (UVLO) to protect the driver and circuit in case of fault conditions. The UVLO point is setup between 4.1V and 4.2V with a hysteresis of 85mV. This UVLO level is specifically designed to guarantee that GaN power devices can be switched at a low $R_{DS(ON)}$ region. During UVLO condition, the OUTL is pulled down to ground.

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Feature Description (continued)

7.3.4 Overtemperature Protection (OTP)

LMG1020 features overtemperature protection (OTP) function by having a rising edge trigger point at around 170°C. With a hysteresis of 20°C, the device can restart to operate when junction temperature is below 150°C.

7.4 Device Functional Modes

表 1. Truth Table

IN–	IN+	OUTH	OUTL
L	L	OPEN	L
L	H	H	OPEN
H	L	OPEN	L
H	H	OPEN	L

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 5 V) in order to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1020 is a 60-MHz low-side gate driver for enhancement mode GaN FETs and Si FETs in a single-ended configuration. The split-gate outputs with strong source and sink capability provides flexibility to adjust the turnon and turnoff strength independently. As a low side driver, LMG1020 can be used in a variety of applications, including different power converters, LiDAR, time-of-flight laser drivers, class-E wireless chargers, synchronous rectifiers, and augmented reality. LMG1020 can also be used as a high frequency low current laser diode driver, or as a signal buffer with very fast rise/fall time.

8.2 Typical Application

The LMG1020 is designed to be used with a single low-side, ground-referenced GaN or logic-level Si FET, as shown in 図 6. Independent gate drive resistors, R1 and R2, are used to independently control the turnon and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor.

TI recommends using at least a 2 Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing overshoot must not exceed the maximum absolute supply voltage.

For applications requiring smaller resistance values, contact TI E2E for guidance.

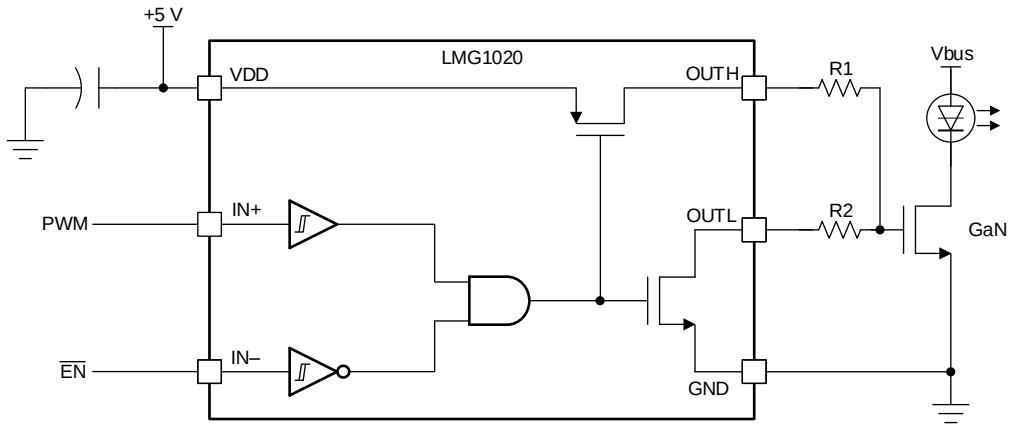

図 6. Typical Implementation of a Circuit

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Typical Application (continued)

8.2.1 Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates the LMG1020 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

8.2.2 Detailed Design Procedure

8.2.2.1 Handling Ground Bounce

For the best switching performance and gate loop with lowest parasitics, it is recommended to connect the ground return pin of LMG1020 as close as possible to the source of the low-side FET in a low inductance manner. However, doing so can cause the ground of LMG1020 to bounce relative to the system or controller ground and lead to erroneous switching logic on the input so as mis-turn on/off on the output.

First of all, LMG1020 has input hysteresis built into the input buffers to help counteract this effect. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by 式 1

$$\frac{di_S}{dt} = \frac{V_{HYST}}{L_{RS}}$$

where

- L_{RS} is the inductance between FET source and ground,
- V_{HYST} is the hysteresis of the input pin,
- and $di_s/\Delta t$ is the maximum allowed current slew rate. (1)

For an assumed parasitic inductance of 0.5 nH and a minimum hysteresis of 0.5 V, the maximum slew rate is 1 A/ns. Many applications would exhibit higher current slew rates, up to the 10 A/ns range, which would make this approach impractical. The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to the LMG1020. A current-limiting, 100 Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

Secondly, for moderate ground-bounce cases, a simple R-C filter can be built with a simple resistor in series with the inputs. By utilizing the input capacitance of LMG1020, the resistor could be close to its input pin. The addition of a small capacitor on the input as supplement can also be helpful. A small time constant of the R-C filter can can enough to filter out high frequency noises. This solution is acceptable for moderate cases in applications where extra delay is acceptable and the pulse width is not extremely short such as 1ns range.

For more extreme cases, or where no delay is tolerable while pulse width is extremely short, using a common-mode choke provides the best results.

One example application where ground-bounce is particularly challenging is when using a current sense resistor. In configuration A LMG1020 ground is connected to the source of GaN FET, while the controller ground is connected to the other side of the current sense resistor as shown in 図 7. Due to the fast switching and very fast current slew rates, the high ground potential bounce induced by inductance of the sense resistor can disrupt the operation of the circuit or even damage the part. To prevent this, a common-mode choke can be used for IN+ and IN–, respectively. Resistors can also added to the signal output line before LMG1020 depending on the input signal pulse width to provide additional RC filtering. 図 9 presents the schematic using approach A with the preferred filtering method. Approach B as 図 8 places the current sense resistor within the gate drive loop path. In this case, the LMG1020 GND pin is connected to the signal ground, and with good ground plane connection, the ground bounce issue can be less severe than approach A. However, the inductance of the current sense resistor adds common-source inductance to the gate drive loop. The voltage generated across this parasitic inductance will subtract from the gate-drive voltage of the FET, slowing down the turnon and turnoff di/dt of the FET, or even cause mis-turn on and off. Additional gate resistance will have to be added to ensure the loop is stable and ring-free. The slower rise may negate the advantage of the fast switching of the GaN FET and may cause additional losses in the circuit. Therefore, this approach is not recommended.

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Typical Application (continued)

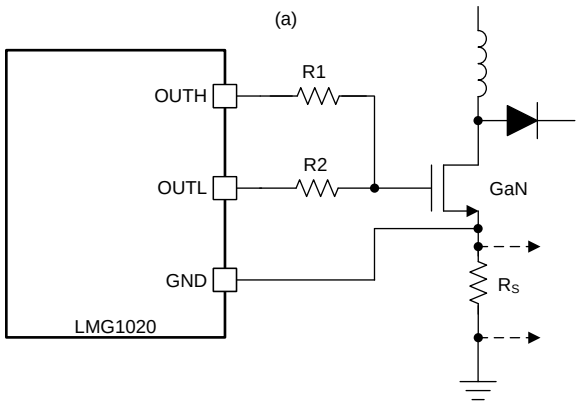

図 7. Source Resistor Current Sense A Configuration

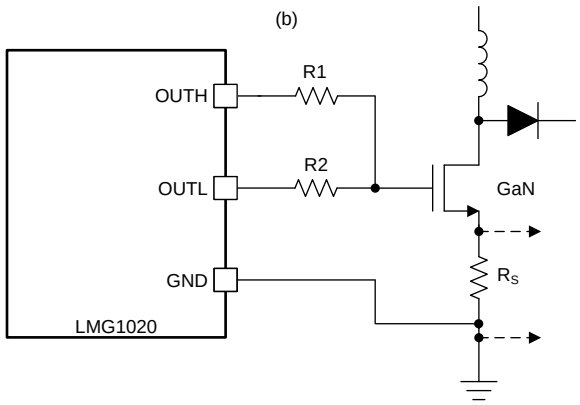

図 8. Source Resistor Current Sense B Configuration

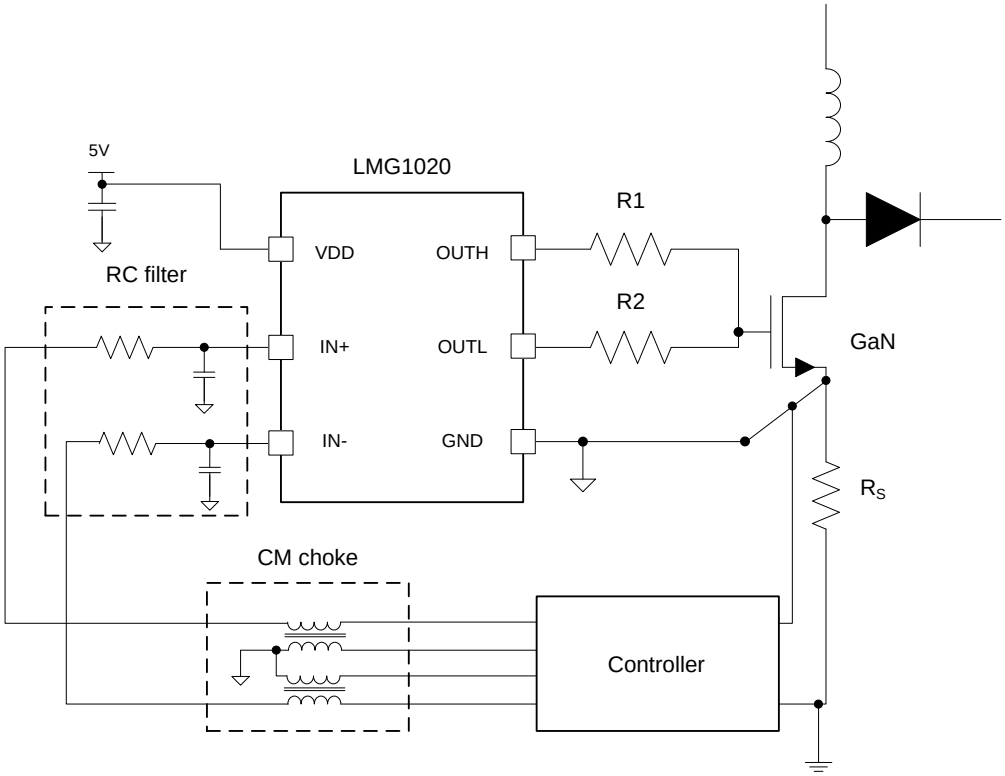

図 9. Filtering For Ground Bounce Noise Handling When Using LMG1020

8.2.2.2 Creating Nanosecond Pulse With LMG1020

LMG1020 can be used to drive pulses of nano seconds duration on to a capacitive load. LMG1020 can be driven with a equivalently short pulse on one input pin. However, this takes a sufficiently strong digital driver and careful consideration of the routing parasitics from digital output to input of LMG1020. Two inputs and included AND gate in LMG1020 provide an alternate method to create a short pulse at the LMG1020 output. Starting with both IN+ and IN– at low, taking IN+ high will cause the output to go high. Now if IN– is taken high as well, output will be pulled low. So a digital signal and its delayed version can be applied to IN+ and IN– respectively to create a

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Typical Application (continued)

pulse at the output with width corresponding to the delay between the signals, as shown in 図 10. The delay can be digitally controlled in the nanosecond range. This method alleviates the requirements for driving the input of LMG1020. If a separate delayed version of the digital signal is not available, a RC delay followed by a buffer can be used to derive the second signal. Optionally, if LMG1020 must be driven with a single short duration pulse, that pulse can itself be generated using another LMG1020 by the above method to meet drive requirements.

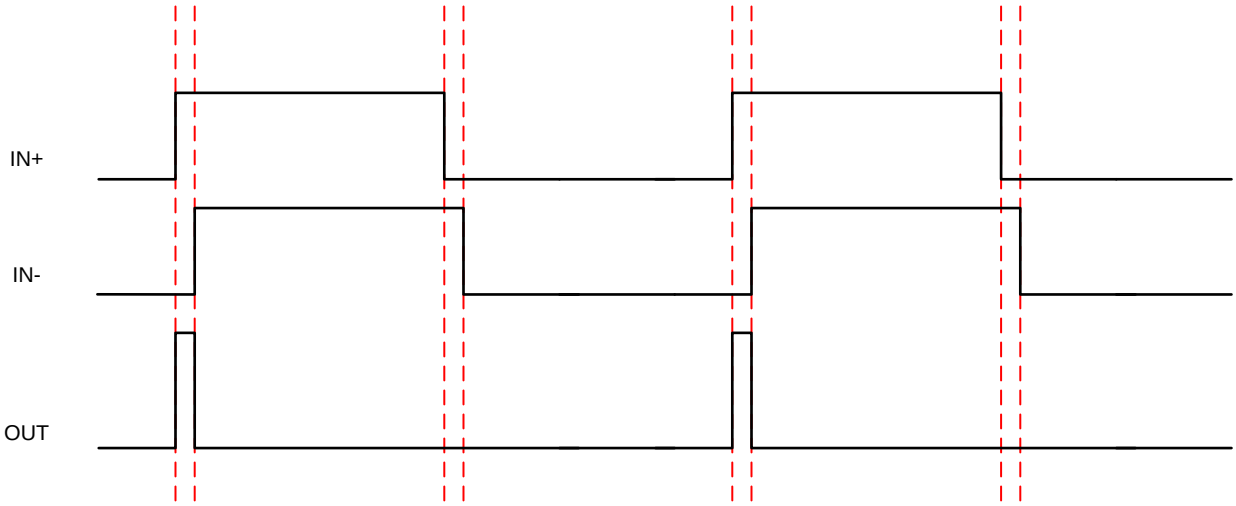

図 10. Timing Diagram To Create Short Pulses

8.2.3 VDD and Overshoot

Fast switching with high current is prone to ringing with parasitic inductances, including those on PCB traces. Overshoot associated with such ringing transients need to be evaluated and controlled as a part of the PCB design process to limit device stress. The parameters affecting stress are how high the overshoot is above the absolute maximum specification and the ratio of overshoot duration to the switching time period. Recommended design practice is to limit the overshoots to the absolute maximum pin voltages. This is accomplished with carful PCB layout to minimize parasitic inductances, choice of components with low ESL and addition of series resistance to limit rise times. For large overshoots, limiting the variability of the power supply may be required. For example, 0.5V of overshoot will be permissible with a maximum recommended supply of 5.25 V (5% variability); however, for larger overshoots, a supply with lower variability will be preferred.

8.2.4 Operating at Higher Frequency

With fast rise/fall time, and capability of achieving 1 ns pulse width, depending on the capacitive load condition, the operating frequency of LMG1020 can be increased in a burst manner. In conditions which requires very high frequency pulsing, a pulse train with certain period of pause between each burst can be adopted to avoid overheat of the device. This will help maintain the RMS output current similar as lower frequency operation but boost the transient frequency to very high. In addition, higher decoupling capacitance will be needed to supply high frequency charging of the capacitive load.

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Typical Application (continued)

8.2.5 Application Curves

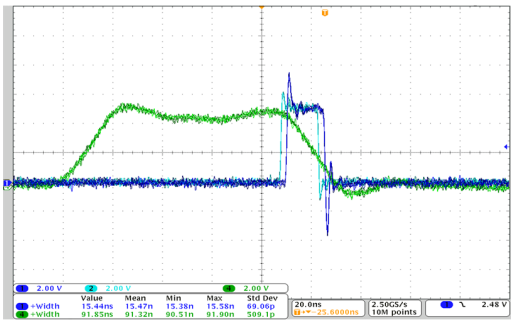

図 11. 90 ns Pulse from Function Generator Yielding 15 ns Pulse On The Input (Cyan) And Gate (Blue) After Pulse Shortening

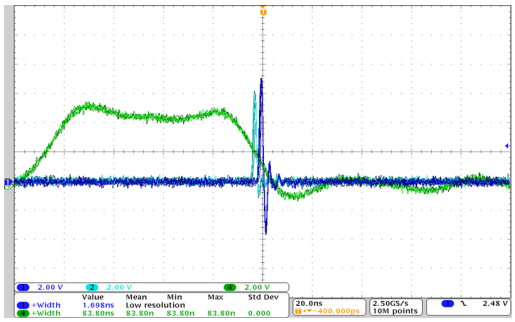

図 12. 90 ns Pulse from Function Generator Yielding 1.5 ns Pulse On The Input (Cyan) And Gate (Blue) After Pulse Shortening

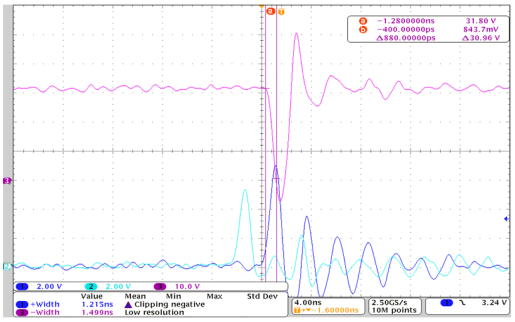

図 13. 1.2 ns Gate Pulse Yielding 1.5 ns 30V Into 1 Ω Pulse (500MHz Scope)

図 14. V_{DS} for 1.5 ns Pulse With 40V of Bus Voltage

図 11 and 図 12 are the waveforms showing the pulse short pulse generation and input/output pulses. The 90ns long pulse (in green color) and its delayed signal are sent through an AND gate, which outputs a short pulse signal as the input of LMG1020. The output signal (in blue color) follows the input (in cyan color) with certain propagation delay. An output pulse short as 1.5 ns can be obtained as 図 12.

図 13 is taken with a 500MHz oscilloscope and shows typical operation waveforms, including the input logic gating signal (cyan), gate signal (blue), and drain to source signal (pink) of the switching GaN FET. On the drain waveform of the FET, it is possible to see a 20V overshoot. This is due to the inductance in the power loop. Vg seems to be oscillating, but this is caused by pickup noise, which is inevitable even when using a spring ground connection.

図 14 shows the waveform of drain to source voltage of a FET driven by LMG1020 with 1.5ns pulse width and 300ps fall time, which drives maximum 60A current at 40V bus voltage.

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9 Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between V_{DD} and GND pins to support the high peak current being drawn from V_{DD} during turnon of the FETs. It is most desirable to place the V_{DD} decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

TI recommends the use of a three-terminal capacitor connecting in shunt-through manner to achieve the lowest ESL and best transient performance. This capacitor can be placed as close as possible to the IC, while another capacitor in larger capacitance can be placed closely to the three-terminal cap to supply enough charge but with slightly lower bandwidth. As a general practice, the combination of a 0.1 µF of 0402 or feed-through capacitor (closest to LMG1020) and a 1 µF 0603 capacitor is recommended.

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10 Layout

10.1 Layout Guidelines

The layout of the LMG1020 is critical to its performance and functionality. The LMG1020 is available in a WCSP ball-grid array package, which enables low-inductance connection to a BGA-type GaN FET. 図 15 shows the recommended layout of the LMG1020 with a ball-grid array GaN FET. 図 16 presents a layout of LMG1020 with a 0.1 µF feed-through capacitor and a larger 1uF capacitor.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

10.1.1 Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the LMG1020. The LMG1020 should be placed as close to the GaN FET as possible, with gate drive resistors R1 and R2 immediately connecting OUTH and OUTL to the FET gate. Large traces must be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the LMG1020 GND pin connect to this plane with minimal impedance. Finally, take care to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

10.1.2 Bypass Capacitor

The VDD power terminal of the LMG1020 must by bypassed to ground immediately adjacent to the IC. Because of the fast gate drive of the IC, the placement and value of the bypass capacitor is critical. The bypass capacitor must be place on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF, up to 1 µF, with temperature coefficient X7R or better. Recommended body types are Low Inductance Chip Capacitor (LICC), Inter-Digitated Capacitor (IDC), Feed-through, and LGA. Finally, an additional 1 µF capacitor (not shown in 図 15) must be placed as close to the IC as practical.

10.2 Layout Example

図 15 presents a typical layout of LMG1020 with a 0402 decoupling capacitor C1, which is placed as close as possible to LMG1020. The ground return at GaN FET Kelvin source immediately flows through a via to the closest inner layer, and overlaps with the top layer traces.

図 16 presents a layout of LMG1020 with a 0.1 µF feed-through capacitor (C1) and a larger 1uF capacitor (C3) for decoupling. In this design, the feed-through capacitor C1 is placed in a shunt-through manner for lower noise decoupling, and C3 is placed next to C1. 0201 resistors are used at the output of LMG1020, which brings lower parasitic inductance than 0402 package.

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Layout Example (continued)

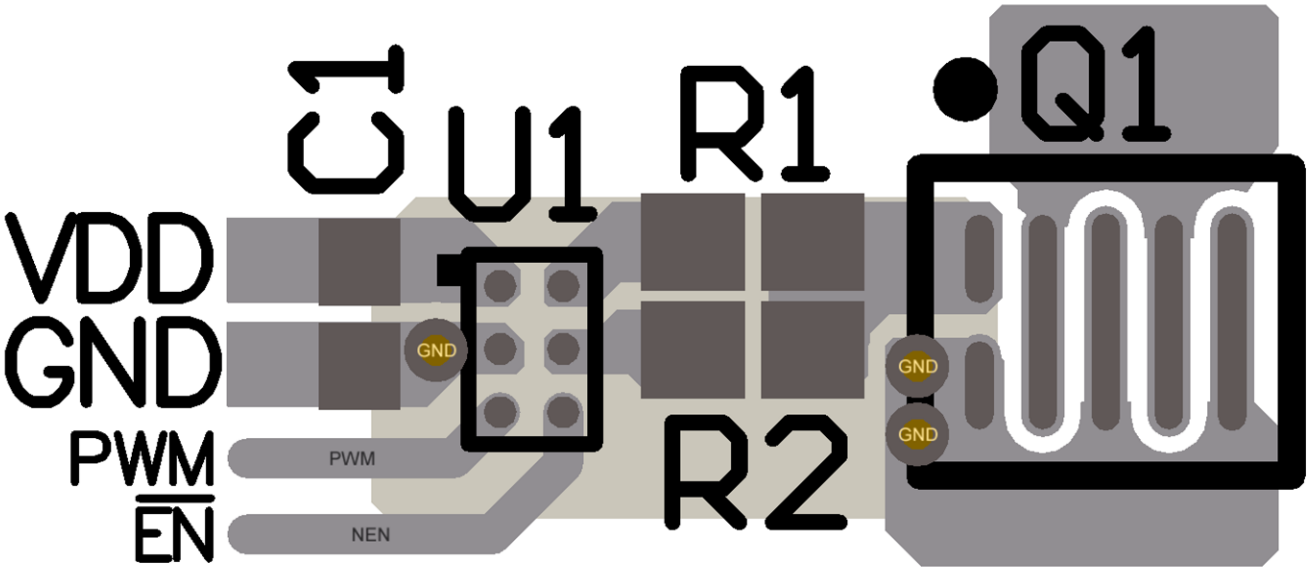

図 15. Typical LMG1020 Layout With Ball-Grid GaN FET And 0402 Decoupling Capacitor

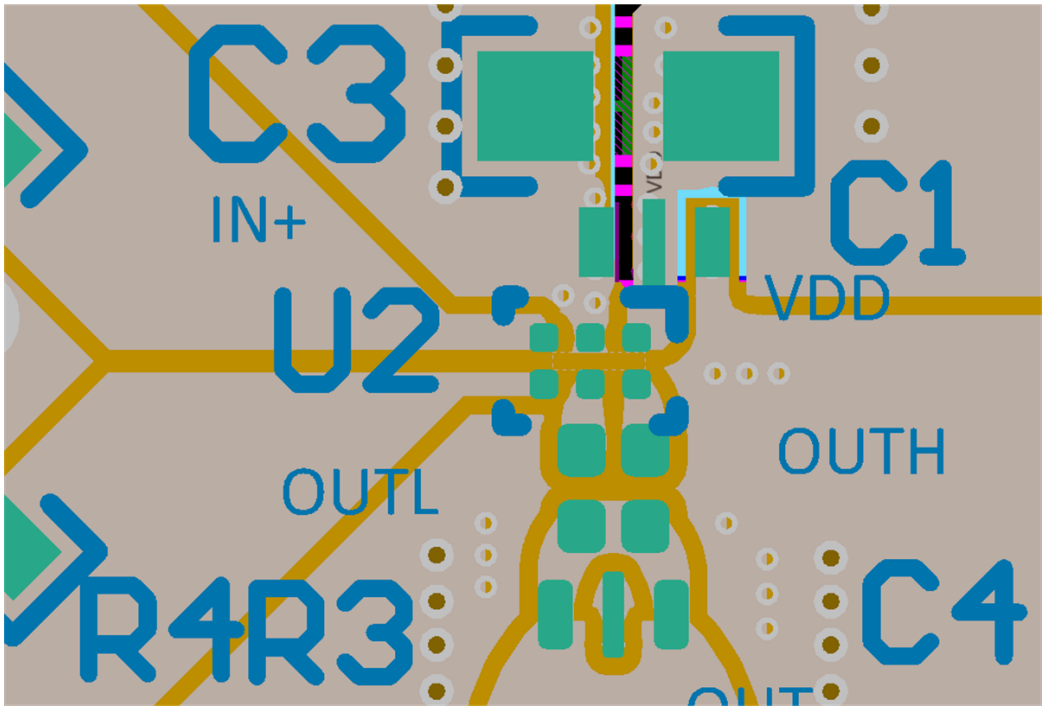

図 16. Typical Layout Of LMG1020 And A Feed-Through Decoupling Capacitor With A Capacitor Load

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『LMG1020-EVMナノ秒LiDAR EVMの使用法』(SNOU150)
- 『LMG1020 PSpiceトランジェント・モデル』(SNOM618)
- 『LMG1020 TINA-TIリファレンス・デザイン』(SNOM619)
- 『LMG1020 TINA-TIトランジェントSpiceモデル』(SNOM620)
- 『LMG1020EVM Altiumデザイン・ファイル』(SNOR025)

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMG1020YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT
LMG1020YFFR.A	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT
LMG1020YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT
LMG1020YFFT.A	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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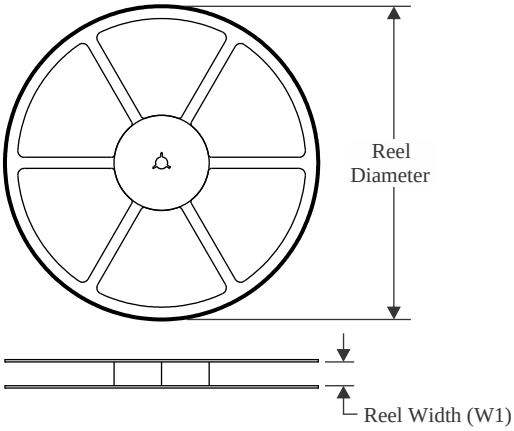
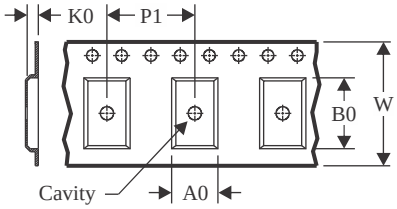
TAPE AND REEL INFORMATION

REEL DIMENSIONS

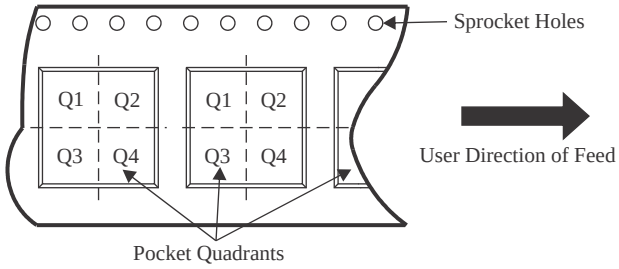


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

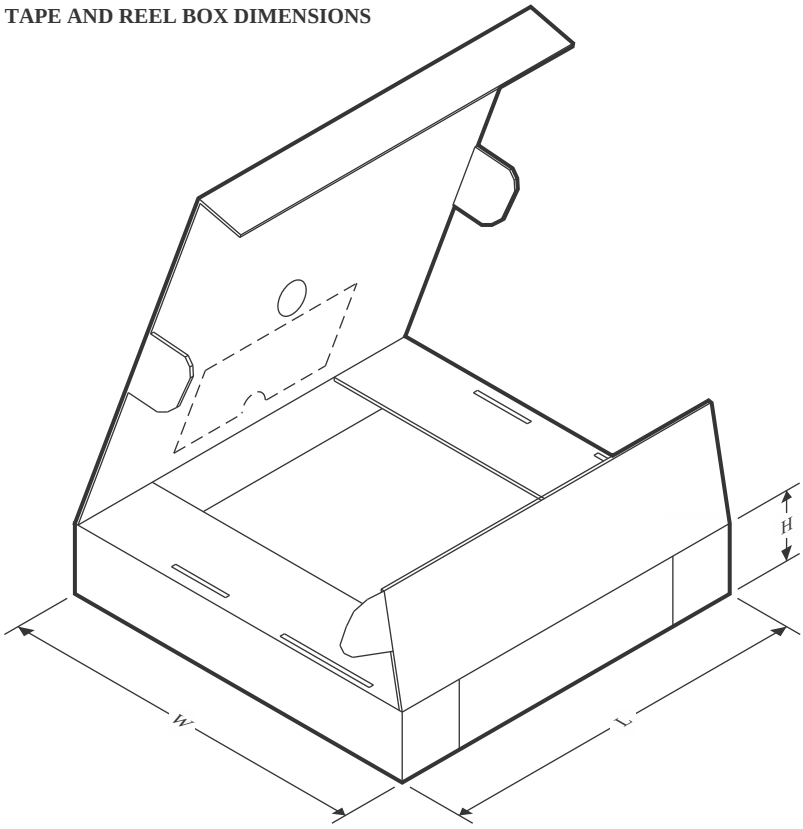
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG1020YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
LMG1020YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

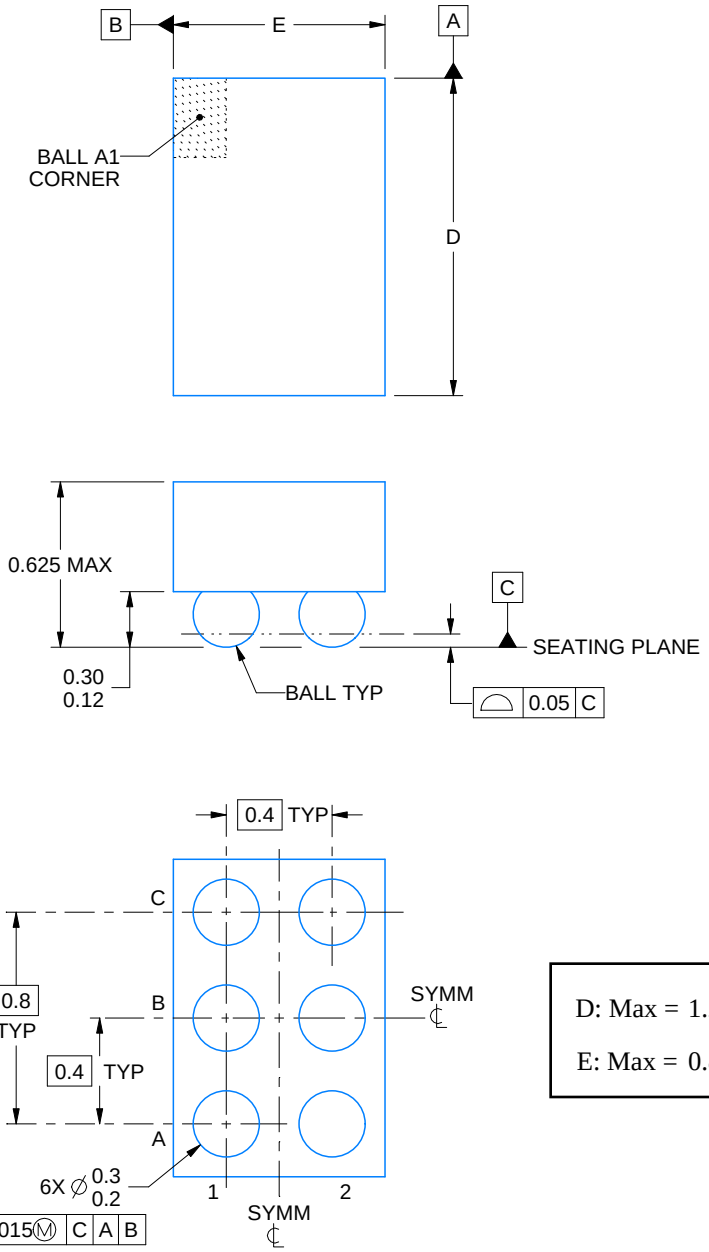
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG1020YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
LMG1020YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



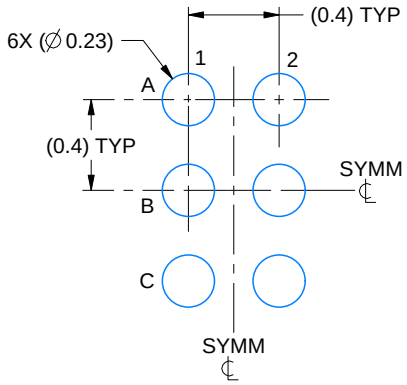
D: Max = 1.285 mm, Min =1.225 mm

E: Max = 0.885 mm, Min =0.825 mm

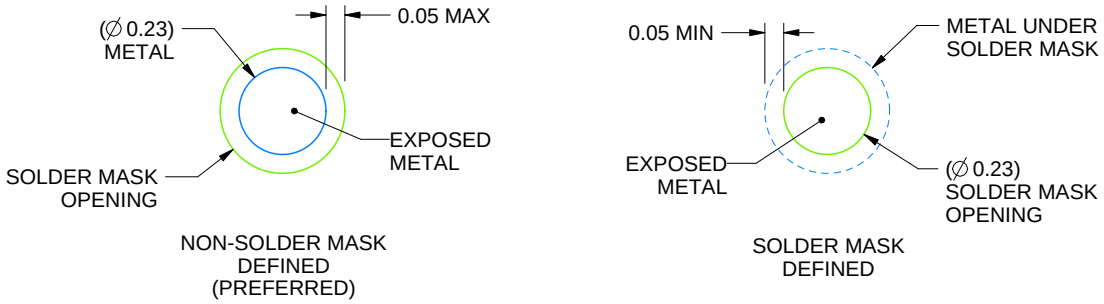
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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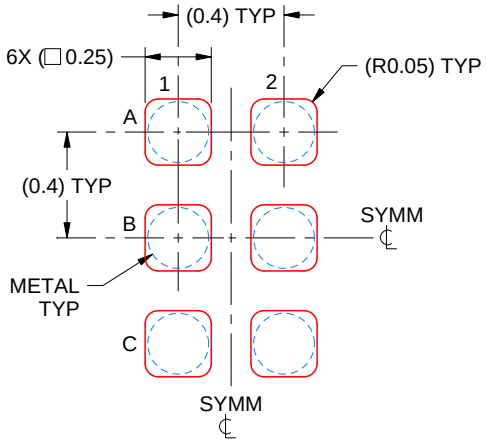
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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