LMH6518 900MHz、デジタル制御、可変ゲイン アンプ

1 特長

- ゲイン範囲:40dB
- ゲイン ステップ サイズ:2dB
- 総合ゲイン分解能 (GSPS ADC 使用時):8.5mdB
- 最小ゲイン:-1.16dB
- 最大ゲイン:38.8dB
- -3dB 帯域幅 (BW):900MHz
- 立ち上がりおよび立ち下がり時間:< 500ps
- 復帰時間:5ns 未満
- 伝搬遅延のばらつき:100ps
- HD2 (100MHz):−50dBc
- HD3 (100MHz):−53dBc
- 入力換算ノイズ (最大ゲイン):0.98nV/√Hz
- 過電圧クランプによる高速復帰
- 消費電力:1.1W (補助出力を無効化することで 0.75W に低減可能)

2 アプリケーション

- オシロスコープのプログラマブル ゲイン アンプ
- 差動 ADC ドライバ
- 高周波数のシングルエンド入力から差動への変換
- 高精度ゲイン制御アプリケーション
- 医療用アプリケーション
- RF/IF アプリケーション

3 概要

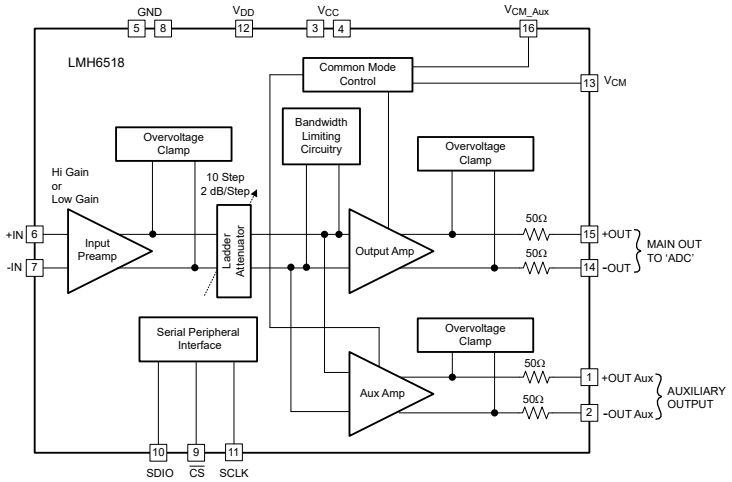
LMH6518 は、総合ゲインを -1.16dB から 38.8dB まで 40dB の範囲にわたって 2dB 刻みで変化させることができるデジタル制御可変ゲイン アンプです。すべてのゲインにおいて、-3dB 帯域幅は 900MHz です。各設定でのゲイン精度は 0.1dB (標準値) です。フルスケール レンジを調整可能な、テキサス・インスツルメンツの GSPS (ギガサンプル毎秒) ADC と組み合わせて使用すると、LMH6518 はゲインを調整することで 6.8mV_{PP} から 920mV_{PP} のフルスケール入力信号に対応でき、700mV_{PP} (公称値) の ADC 入力を得ることができます。補助出力 (+OUT AUX、−OUT AUX) はメイン出力に追従します。補助出力は、オシロスコープのトリガ機能回路で使うことを想定していますが、その他の用途にも使用できます。

LMH6518 のゲインは、SPI 互換シリアル バスを介して設定します。本デバイスのゲインと GSPS ADC FS 入力の両方を操作した場合、8.5mdB の信号経路総合ゲイン分解能を達成できます。入力と出力は DC 結合されています。出力は差動であり、個別の同相モード電圧制御機能 (メインおよび補助出力用) を備えています。また、選択可能な (20MHz、100MHz、200MHz、350MHz、650MHz、750MHz、全 BW) 帯域幅制限回路 (メイン出力と補助出力の両方に共通) を備えています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LMH6518	RGH (WQFN、16)	4mm × 4 mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



機能ブロック図

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4 Pin Configuration and Functions

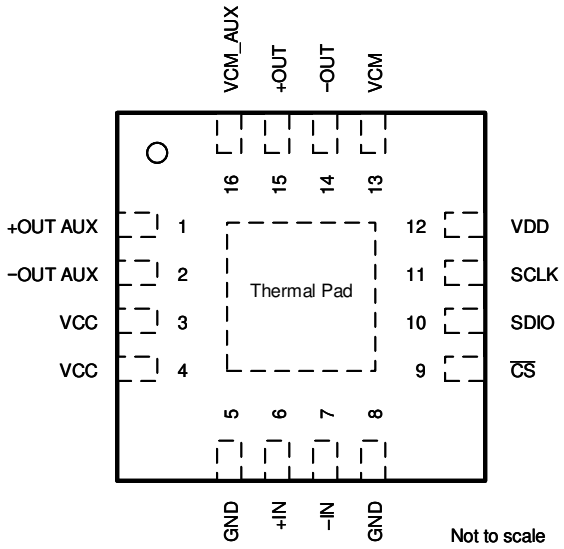


図 4-1. RGH Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	+OUT AUX	O	Auxiliary positive output
2	−OUT AUX	O	Auxiliary negative output
3	VCC	P	Analog power supply
4	VCC	P	Analog power supply
5	GND	G	Ground, electrically connected to the WQFN heat sink
6	+IN	I	Positive input
7	–IN	I	Negative input
8	GND	G	Ground, electrically connected to the WQFN heat sink
9	$\overline{CS}$	I	Serial chip select (SPI, active low): While this signal is asserted, SCLK is used to accept serial data present on SDIO and to source serial data on SDIO. When this signal is deasserted, SDIO is ignored and SDIO is in a high-impedance state.
10	SDIO	I/O	Serial data-in or data-out (SPI). During a write operation, serial data are shifted into the device (8-bit command and 16-bit data) on this pin while $\overline{CS}$ signal is asserted. During a read operation, serial data are shifted out of the device on this pin while $\overline{CS}$ signal is asserted. At other times, and after one complete access cycle (24 bits; see 図 6-1 and 図 6-2), this input is ignored. This output is in a high-impedance state when $\overline{CS}$ is deasserted. This pin is bidirectional.
11	SCLK	I	Serial clock (SPI): Serial data are shifted into and out of the device synchronous with this clock signal. SCLK transitions with $\overline{CS}$ deasserted are ignored. To minimize digital crosstalk, stop SCLK when not used.
12	VDD	P	Digital power supply
13	VCM	I	Input from ADC to control main output common mode (CM) voltage
14	−OUT	O	Main negative output
15	+OUT	O	Main positive output
16	VCM_AUX	I	Input to control auxiliary output CM voltage
Pad	Thermal Pad	—	Thermal pad (WQFN heat sink), electrically connected to pins 5 and 8 (GND)

(1) G = ground, I = input, O = output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Analog supply voltage (5 V nominal)			5.5	V
V_{DD}	Digital supply voltage (3.3 V nominal)			3.6	
	Differential input signal voltage			±1	V
	Maximum dc output value(2)			1700	mV_{PP}
	Input common mode voltage		1	4	V
	V_{CM} and V_{CM_Aux}			2	V
	SPI inputs			3.6	V
	Soldering temperature	Infrared or convention (20 s)		235	°C
		Wave (10 s)		260	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When the LMH6518 output is held at saturation conditions for long time periods the part can develop a permanent output offset voltage. To manage this output offset condition the device attenuation must be set properly to avoid long periods of output saturation.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		5 ±5%		V
V_{DD}	Digital supply voltage		3.3 ±5%		V
T_A	Ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		LMH6518 RGH (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Unless otherwise noted, all limits are specified at T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100-Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
DYNAMIC PERFORMANCE						
LSBW	–3-dB bandwidth	All gains		900		MHz
	Peaking	All gains		1		dB
GF_0.1 dB	±0.1-dB gain flatness	All gains		150		MHz
GF_1 dB	±1-dB gain flatness	All gains		400		MHz
TRS	Rise time			460		ps
TRL	Fall time			450		
OS	Overshoot	Main output		9%		
t_{s_1}	Settling time	Main output, ±0.5%		10		ns
t_{s_2}	Settling time	Main output, ±0.05%		14		
t_recover	Recovery time(4)	All gains		<5		ns
P_D	Propagation delay	V_{OUT} = 0.7 V_{PP}, all gains		1.2		ns
P_{D_VAR}	Propagation delay variation	Gain varied		100		ps
NOISE, DISTORTION, AND RF SPECIFICATIONS						
e_{n_1}	Input noise spectral density	Max gain, 10 MHz		0.98		nV/√Hz
e_{n_2}	Input noise spectral density	Preamp LG and 0-dB ladder, 10 MHz		4.1		nV/√Hz
e_{no_1}	RMS output noise	Max gain, 100 Hz to 400 MHz		1.7		mV
e_{no_2}	RMS output noise	Preamp LG, 0-dB ladder, 100 Hz to 400 MHz		940		µV
NF_1	Noise figure	Max gain, R_S = 50 Ω each input, 10 MHz		3.8		dB
NF_2	Noise figure	Preamp LG, 0-dB ladder, R_S = 50 Ω each input, 10 MHz		13.5		dB
HD2_1	2nd harmonic distortion(5)	Main output, 100 MHz, all gains		–50		dBc
HD3_1	3rd harmonic distortion(5)	Main output, 100 MHz, all gains		–53		dBc
HD2_2	2nd harmonic distortion(5)	Auxiliary output, 100 MHz, all gains		–48		dBc
HD3_2	3rd harmonic distortion(5)	Auxiliary output, 100 MHz, all gains		–50		dBc
HD2_3	2nd harmonic distortion(5)	Main output, 250 MHz, all gains		–44		dBc
HD3_3	3rd harmonic distortion(5)	Main output, 250 MHz, all gains		–50		dBc
HD2/HD3_4	2nd and 3rd harmonic distortion(5)	Auxiliary output, 250 MHz, all gains		–42		dBc
IMD3	Intermodulation distortion(5)	f = 250 MHz, main output		–65		dBc
OIP3_1	Intermodulation intercept(5)	Main output, 250 MHz		26		dBm
P_1dB_main	–1-dB compression	Main output, 250 MHz, 0-dB ladder		1.8		V_{PP}
		Main output, 250 MHz, 20-dB ladder		1		
P_1dB_aux	–1-dB compression	Auxiliary output, 250 MHz, 0-dB ladder		1.65		V_{PP}
		Auxiliary output, 250 MHz, 20-dB ladder		1		

5.5 Electrical Characteristics (続き)

Unless otherwise noted, all limits are specified at T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100-Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
GAIN PARAMETERS						
$A_{V\_DIFF\_MAX}$	Maximum gain		38.1	38.8	39.5	dB
$A_{V\_DIFF\_MIN}$	Minimum gain		–1.91	–1.16	–0.4	dB
Gain_Step	Gain step size	All gains including preamp step	1.8	2	2.2	dB
	Gain step size with ADC (see セクション 7)	ADC FS adjusted		8.5		mdB
Gain_Range	Gain range		39	40	41	dB
$TC\_A_{V\_DIFF}$	Gain temp coefficient(6)	All gains		–0.8		mdB/°C
$Gain\_A_{CC}$	Absolute gain accuracy	Compared to theoretical from max gain in 2-dB steps	0.75		0.75	dB
MATCHING						
Gain_match	Gain matching, main and auxiliary	All gains		±0.1	±0.2	dB
BW_match	–3-dB bandwidth matching, main and auxiliary	All gains		5%		
RT_match	Rise time matching, main and auxiliary	All gains		5%		
PD_match	Propagation delay matching, main and auxiliary	All gains		100		ps
ANALOG I/O						
CMRR_1	CM rejection ratio (see 表 8-1)	Preamp HG, 0-dB ladder, 1.9 V < CMVR < 3.1 V	45	86		dB
CMRR_2	CM rejection ratio (see 表 8-1)	Preamp LG, 0-dB ladder, 1.9 V < CMVR < 3.1 V	40	55		dB
CMVR_1	Input common-mode voltage	Preamp HG, all ladder steps, CMRR ≥ 45 dB	1.9		3.1	V
CMVR_2	Input common-mode voltage	Preamp LG, all ladder steps, CMRR ≥ 40 dB	1.9		3.1	V
$\lvert\Delta V_{O\_CM}\rvert$ $\Delta_{I\_CM}\rvert$		All gains, 2 V < CMVR < 3 V	–60	–100		dB
CMRR_CM	CM rejection ratio relative to VCM (see 表 8-1)	Preamp LG, 0 dB		101		dB
Z_{in_diff}	Differential input impedance	All gains		150 || 1.5		kΩ || pF
Z_{in_CM}	CM input impedance	Preamp HG		420 || 1.7		kΩ || pF
		Preamp LG		900 || 1.7		
FS_{OUT1}	Full scale voltage swing	Main output, all gains, THD at 100 MHz ≤ –40 dBc	770(7)	800		mV_{PP}
FS_{OUT2}	Full scale voltage swing	Main output, clamped, 0-dB ladder		1800	1960	mV_{PP}
FS_{OUT3}	Full scale voltage swing	Auxiliary output, all gains THD at 100 MHz ≤ –40 dBc	770(7)	800		mV_{PP}
FS_{OUT4}	Full scale voltage swing	Auxiliary output, clamped, 0-dB ladder		1600	1760	mV_{PP}
V_{OUT_MAX1}	Voltage at each output pin (clamped)	Main output, all gains, V_{CM} = 1.2 V	0.5		1.8	V
V_{OUT_MAX2}	Voltage at each output pin (clamped)	Auxiliary output, all gains, V_{CM} = 1.2 V	0.8		2.2	V

5.5 Electrical Characteristics (続き)

Unless otherwise noted, all limits are specified at T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100-Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OUT_MAX3}	Voltage at each output pin (clamped)	Main output, all gains, V_{CM} = 1.45 V				2.05	V
V_{OUT_MAX4}	Voltage at each output pin (clamped)	Auxiliary output, all gains, V_{CM} = 1.45 V				2.45	V
Z_{OUT_DIFF}	Differential output impedance	All gains		92	100	108	Ω
V_{OOS}	Output offset voltage	All gains			±15	±40	mV
V_{OOS_shift1}	Output offset voltage shift	Preamp LG to preamp HG			13.7		mV
V_{OOS_shift2}	Output offset voltage shift	All gains, excluding preamp step			12.7		mV
TCV_{OOS}	Output offset voltage drift(6)	Preamp HG, 0-dB ladder			–24		µV/°C
		Preamp LG, 0-dB ladder			–7		
I_B	Input bias current(8)	T_A = –40°C to +85°C			40	100	µA
		T_A = –65°C to +150°C				140	
V_{OCM}	Output CM voltage	All gains	T_A = –40°C to +85°C		1.2		V
			T_A = –65°C to +150°C	0.95		1.45	
V_{OS_CM}	Output CM offset	All gains			±15	±30	mV
$TC\_V_{OS\_CM}$	CM offset voltage temperature coefficient	All gains			+55		µV/°C
BAL_Error_DC	Output gain balance error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$			–78		dB
BAL_Error_AC	Output gain balance error	250 MHz, $\frac{v_{O\_CM}}{v_{OUT}}$			–45		dB
PB	Phase balance error (see 表 8-1)	250 MHz			±0.8		deg
PSRR	Differential power-supply rejection (see 表 8-1)	Preamp HG, 0-dB ladder		–60	–87		dB
		Preamp LG, 0-dB ladder		–50	–70		
PSRR_CM	CM power-supply rejection (see 表 8-1)	Preamp LG, 0-dB ladder		–55	–71		dB
V_{CM_I}	V_{CM} input bias current(8)	All gains	T_A = –40°C to +85°C		±1	±10	nA
			T_A = –65°C to +150°C			±20	
$V_{CM\_AUX\_I}$	V_{CM_AUX} input bias current(8)	All gains	T_A = –40°C to +85°C		±1	±10	nA
			T_A = –65°C to +150°C			±20	
DIGITAL I/O							
V_{IH}	Input logic high	T_A = –65°C to +150°C		V_{DD} – 0.6			V
V_{IL}	Input logic low	T_A = –65°C to +150°C				0.5	V
V_{OH}	Output logic high				V_{DD}		V
V_{OL}	Output logic low				0		V
R_{Hi_Z}	Output resistance	High-impedance mode			5		MΩ
I_in	Input bias current				<1		µA
F_{SCLK}	SCLK rate					10	MHz
F_{SCLK_DT}	SCLK duty cycle			45%	50%	55%	

5.5 Electrical Characteristics (続き)

Unless otherwise noted, all limits are specified at T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100-Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (see 表 8-1 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER REQUIREMENTS							
I_{S1}	Supply current, V_{CC}	T_A = –40°C to +85°C		195	210	225	mA
		T_A = –65°C to +150°C				230	
I_{S1_off}	Supply current, V_{CC} aux off	T_A = –40°C to +85°C			150	165	mA
		T_A = –65°C to +150°C				170	
I_{DD}	Supply current, V_{DD}	T_A = –40°C to +85°C			180	350	µA
		T_A = –65°C to 150°C				400	
BANDWIDTH LIMITING FILTER SPECIFICATIONS							
	Pass band tolerance, –3 dB bandwidth	All gains	20 MHz	0%	20%		
			100 MHz	0%	20%		
			200 MHz	0%	20%		
			350 MHz		±25%		
			650 MHz		±25%		
			750 MHz		±25%		
		Preamp LG, 0-dB ladder	350 MHz		±10%		
			650 MHz		±10%		
			750 MHz		±10%		

(1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C unless otherwise specified. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depends on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Recovery time is the slower of the main and auxiliary outputs. Output swing of 700 mV_{PP} shifted up or down by 50% (0.35 V) by introducing an offset. Measured values correspond to the time required to return to within ±1% of 0.7 V_{PP} (±7 mV).
(5) Distortion data taken under single ended input condition.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Specified by design.
(8) Positive current is current flowing into the device.

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_S	SDIO setup time	25			ns
t_H	SDIO hold time	25			ns
t_{CES}	$\overline{CS}$ enable setup time (from $\overline{CS}$ asserted to rising edge of SCLK)	25			ns
t_{CDS}	$\overline{CS}$ disable setup time (from $\overline{CS}$ deasserted to rising edge of SCLK)	25			ns
t_{IAG}	Inter-access gap	3			SCLK cycles

5.7 Typical Characteristics

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

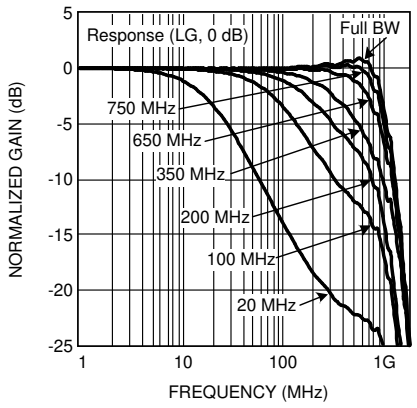


図 5-1. Response (LG, 0-dB)

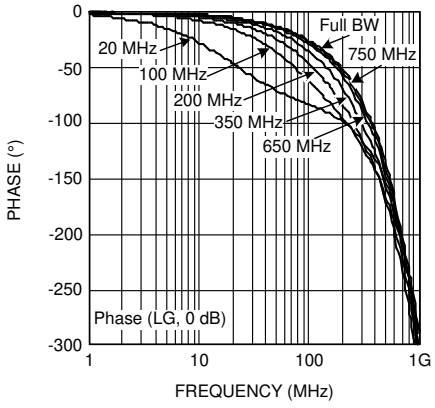


図 5-2. Phase (LG, 0-dB)

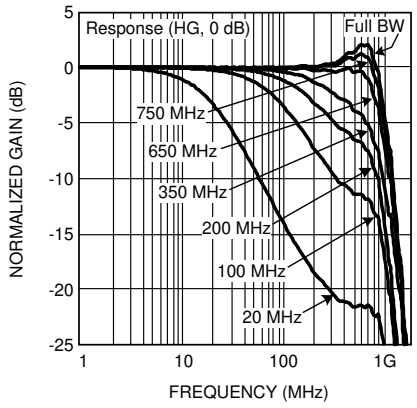


図 5-3. Response (HG, 0-dB)

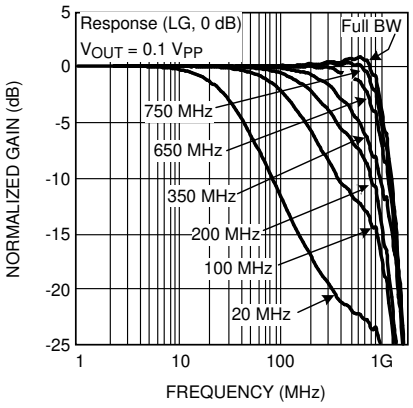


図 5-4. Small Signal Response (LG, 0-dB)

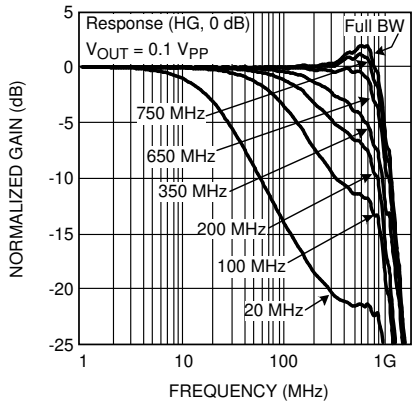


図 5-5. Small Signal Response (HG, 0-dB)

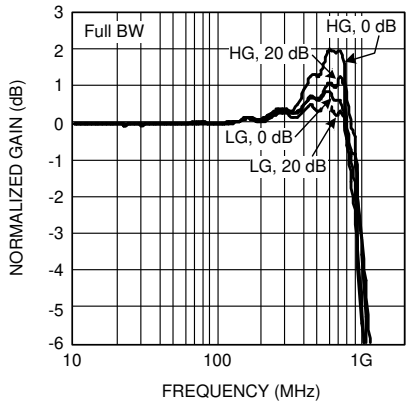


図 5-6. Response vs Gain

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

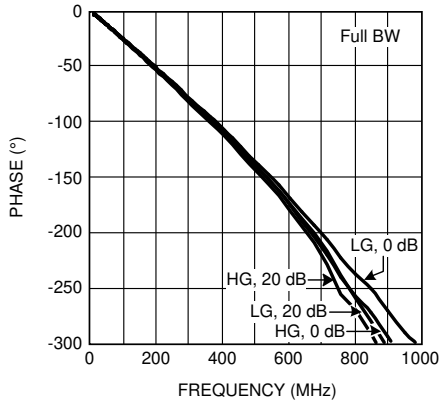


図 5-7. Phase vs Gain

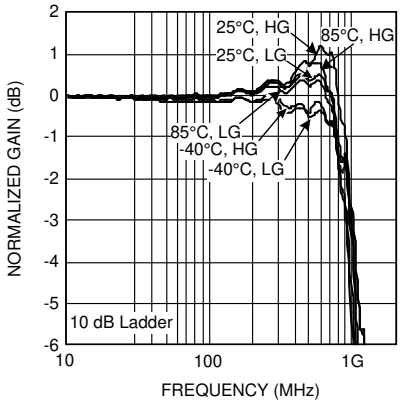


図 5-8. Response Over Temperature

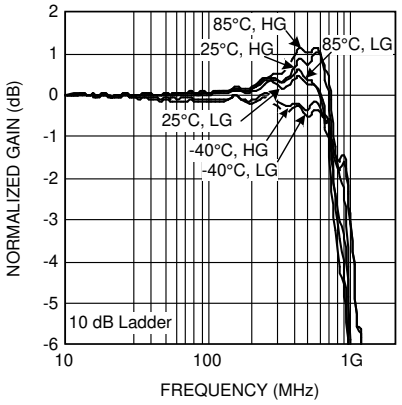


図 5-9. Auxiliary Response Over Temperature

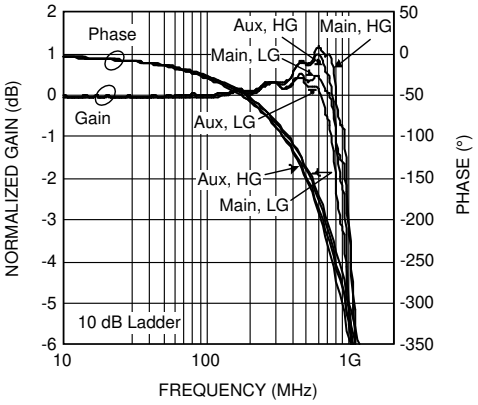


図 5-10. Main vs Auxiliary Response

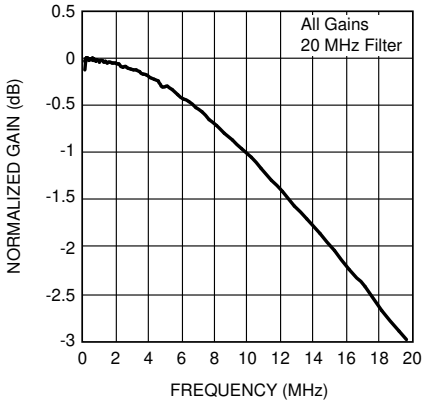


図 5-11. Response vs Gain

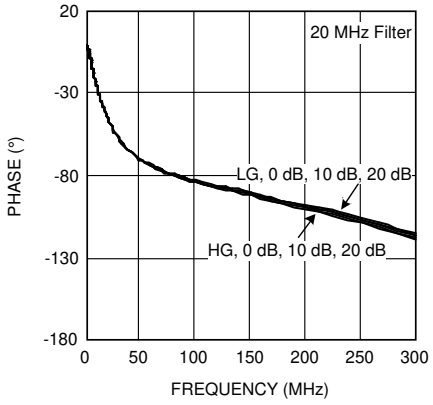


図 5-12. Phase vs Gain

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

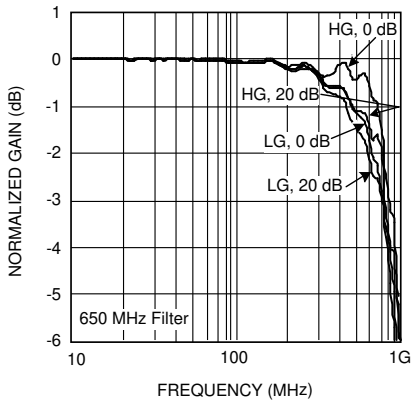


図 5-13. Response vs Gain

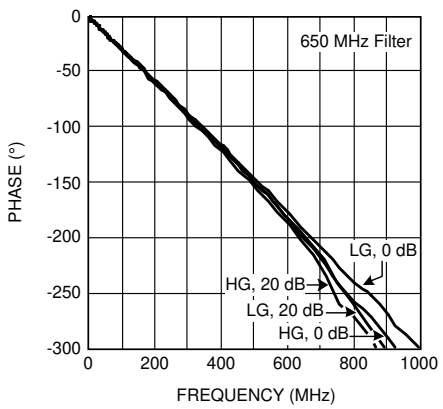


図 5-14. Phase vs Gain

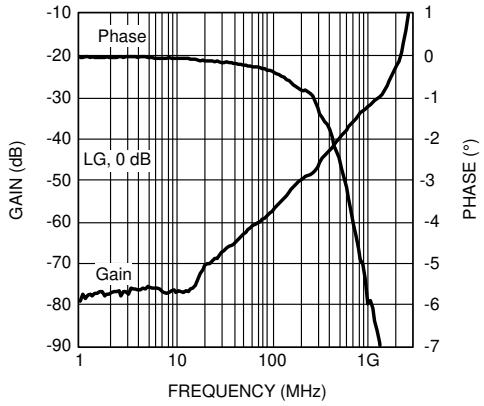


図 5-15. Balance Error

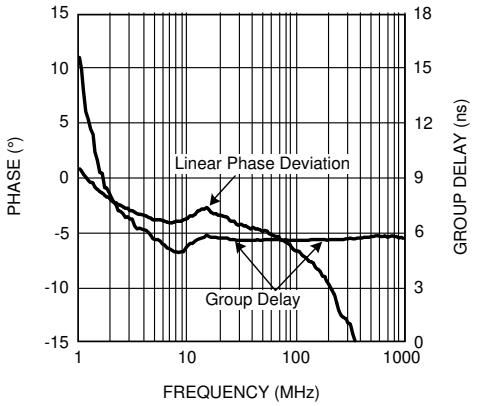


図 5-16. Linear Phase Deviation and Group Delay

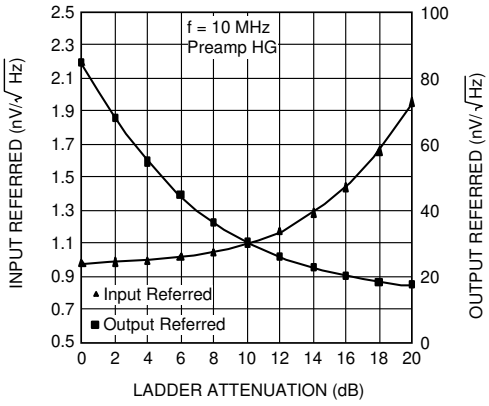


図 5-17. Noise vs Ladder Attenuation

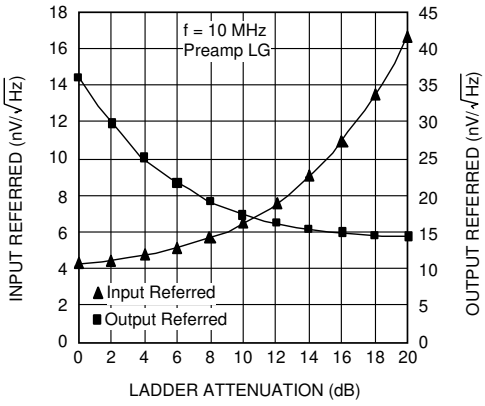


図 5-18. Noise vs Ladder Attenuation

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

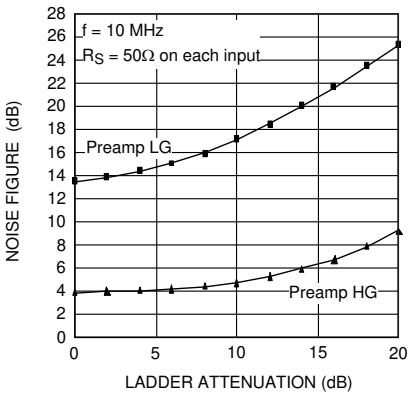


図 5-19. Noise Figure vs Gain

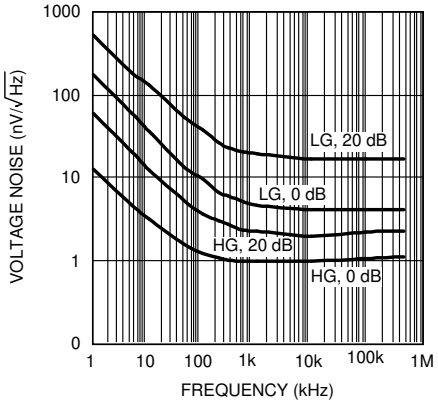


図 5-20. Input Voltage Noise vs Frequency

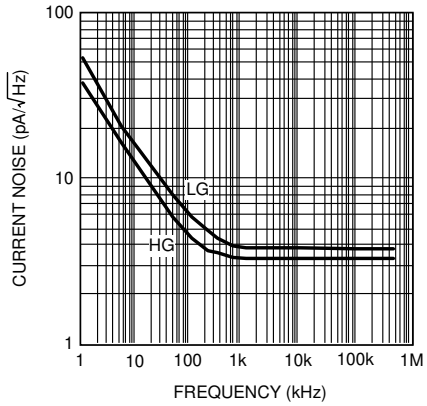


図 5-21. Input Current Noise vs Frequency

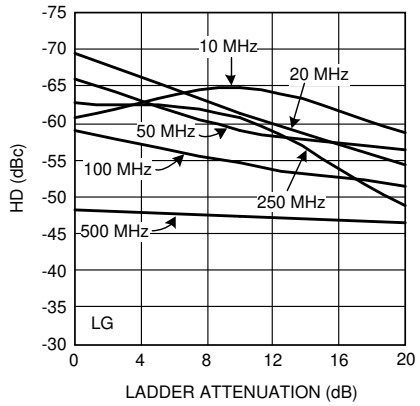


図 5-22. HD2 vs Ladder Attenuation

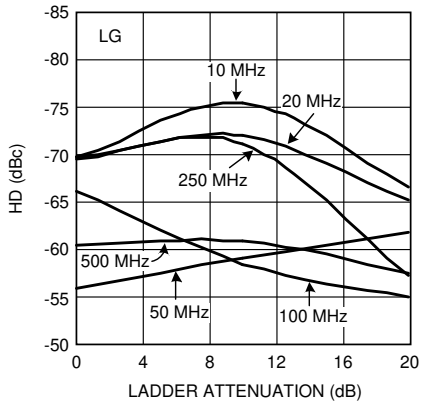


図 5-23. HD3 vs Ladder Attenuation

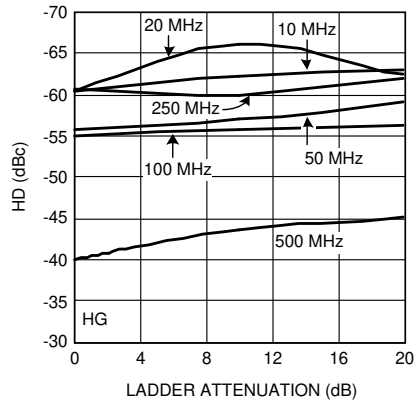


図 5-24. HD2 vs Ladder Attenuation

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

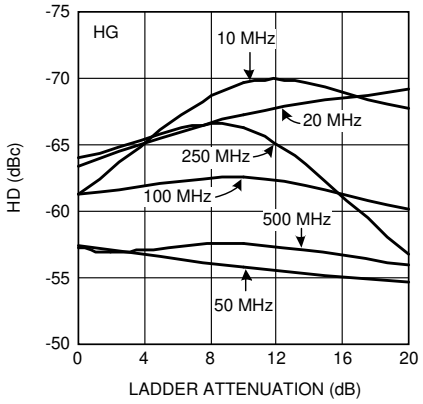


図 5-25. HD3 vs Ladder Attenuation

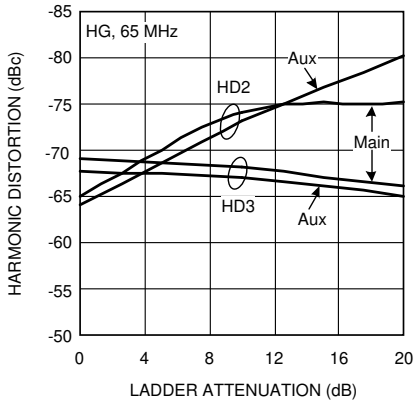


図 5-26. Main and Auxiliary Distortion Comparison

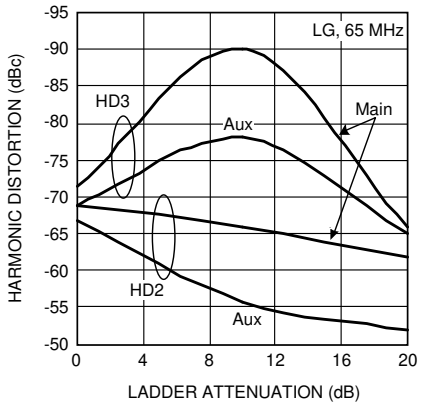


図 5-27. Main and Auxiliary Distortion Comparison

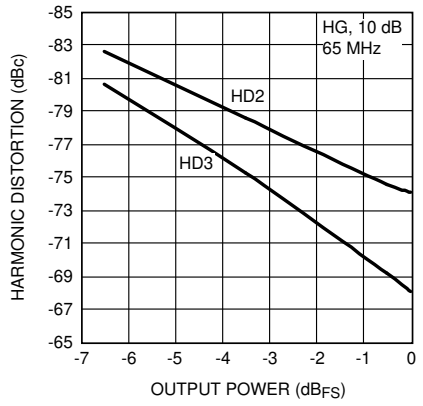


図 5-28. Distortion vs Output Power

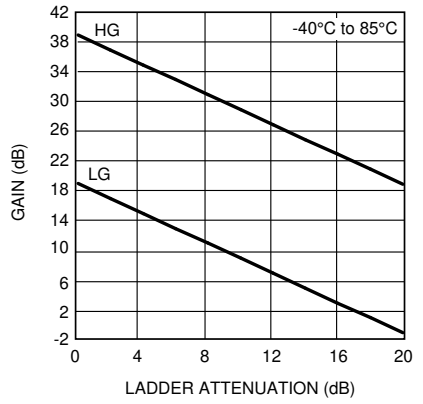


図 5-29. Gain vs Ladder Attenuation

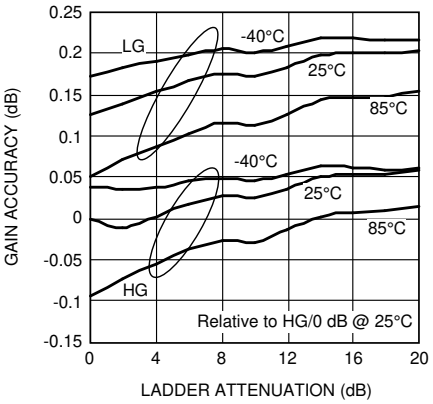


図 5-30. Gain Accuracy vs Ladder Attenuation

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

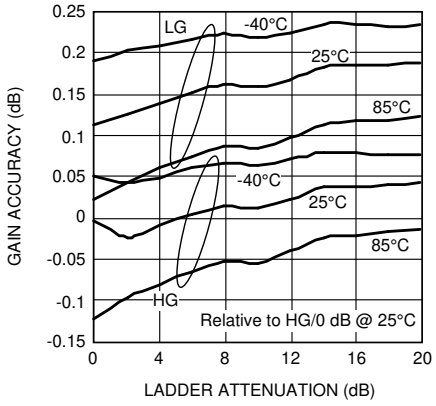


図 5-31. Auxiliary Gain Accuracy vs Ladder Attenuation

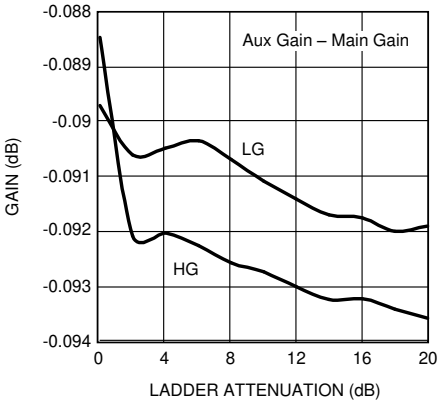


図 5-32. Gain Matching vs Ladder Attenuation

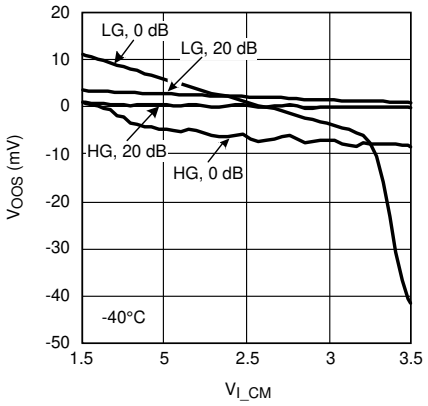


図 5-33. A_{V_CM}

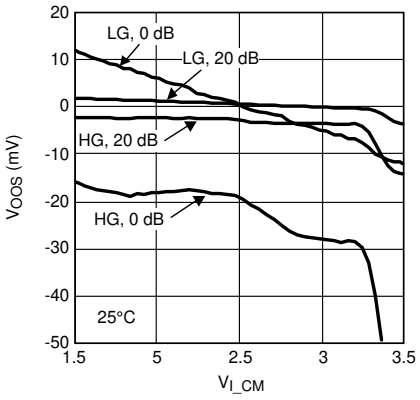


図 5-34. A_{V_CM}

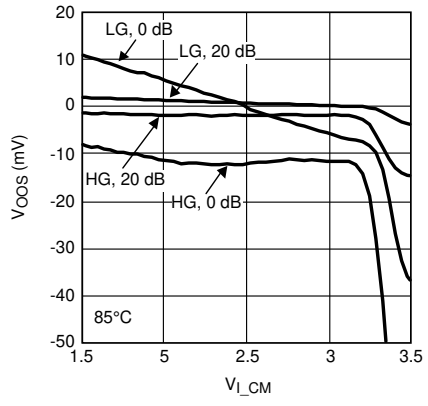


図 5-35. A_{V_CM}

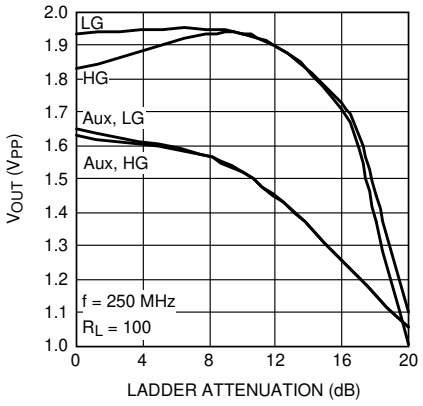


図 5-36. –1-dB Compression vs Ladder Attenuation

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

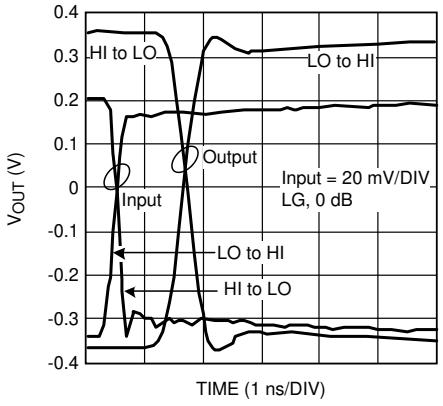


図 5-37. Step Response

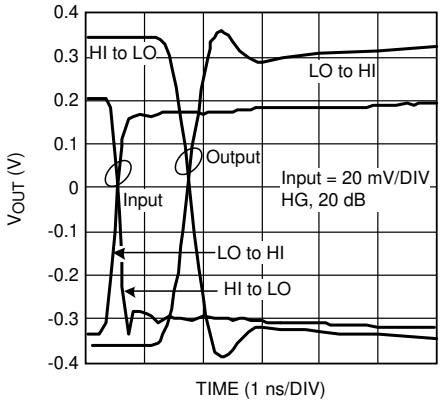


図 5-38. Step Response

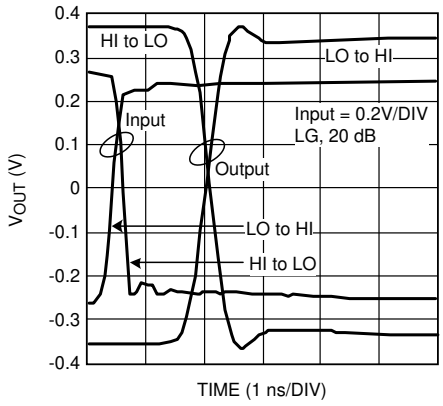


図 5-39. Step Response

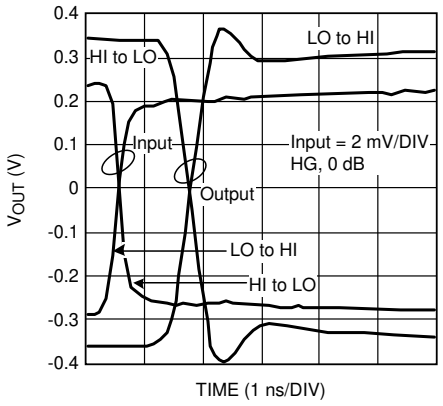


図 5-40. Step Response

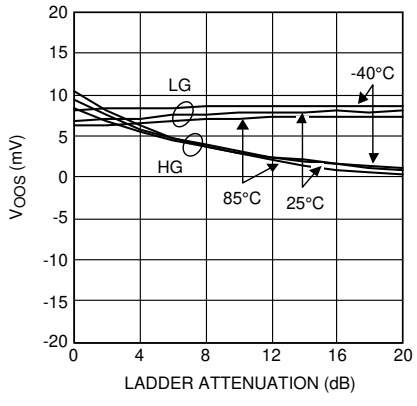


図 5-41. Output Offset Voltage (Typical Unit 1)

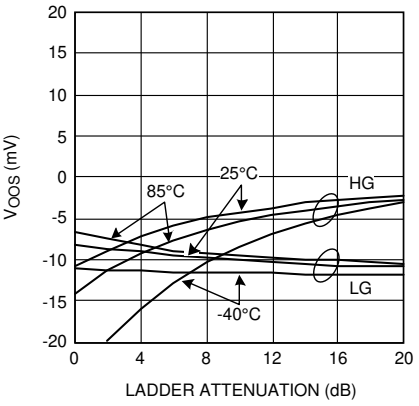


図 5-42. Output Offset Voltage (Typical Unit 2)

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

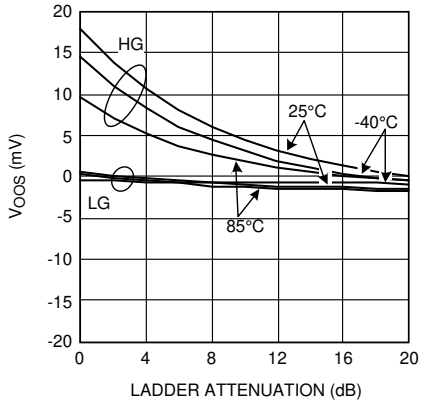


図 5-43. Output Offset Voltage (Typical Unit 3)

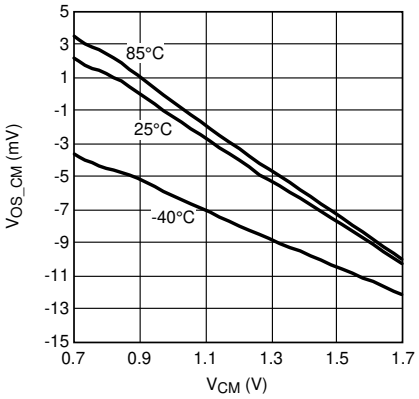


図 5-44. V_{OS_CM} vs V_{CM}

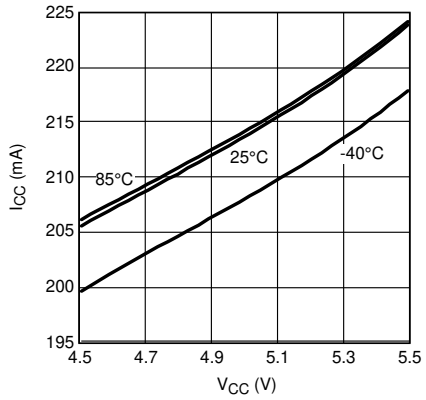


図 5-45. Supply Current vs Supply Voltage

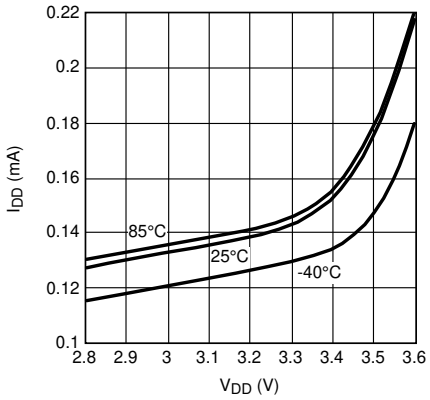


図 5-46. Supply Current vs Supply Voltage

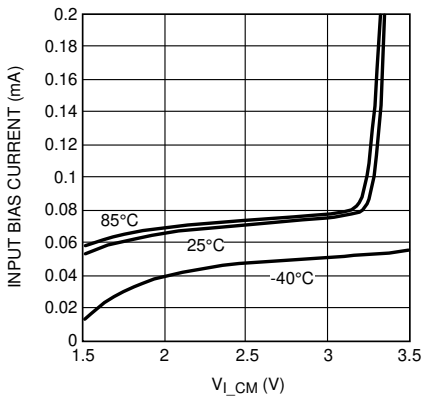


図 5-47. Input Bias Current vs Input CM

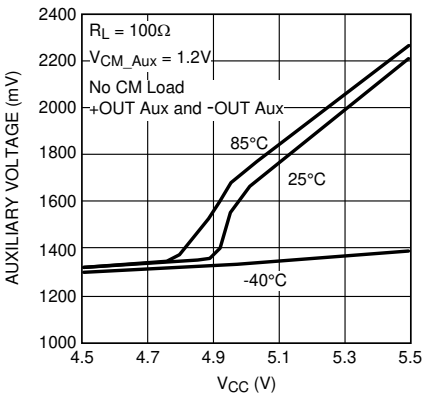


図 5-48. Auxiliary Output Voltage (Hi-Z Mode)

5.7 Typical Characteristics (continued)

at input CM = 2.5-V, V_{CM} = 1.2-V, $V_{CM\ AUX}$ = 1.2-V, single-ended input drive, V_{CC} = 5-V, V_{DD} = 3.3-V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8-dB (preamp LG, 0-dB ladder attenuation), and full power setting (with auxiliary output turned on) (unless otherwise noted)

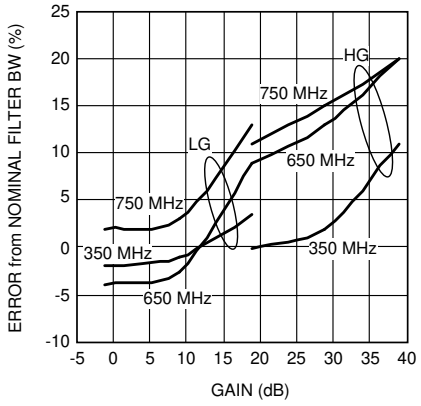


図 5-49. Filter BW vs Gain

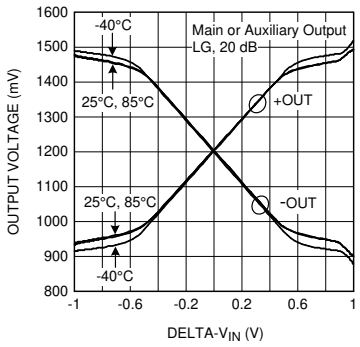


図 5-50. Output vs Input

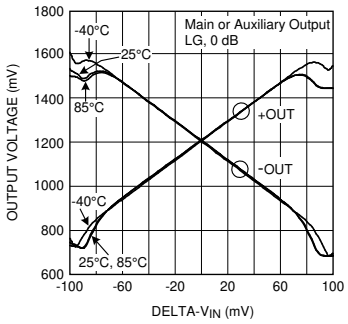


図 5-51. Output vs Input

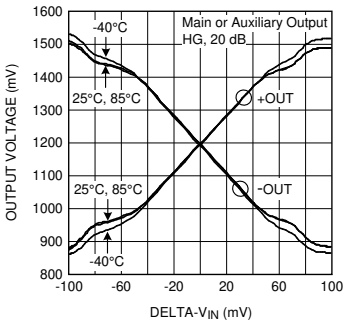


図 5-52. Output vs Input

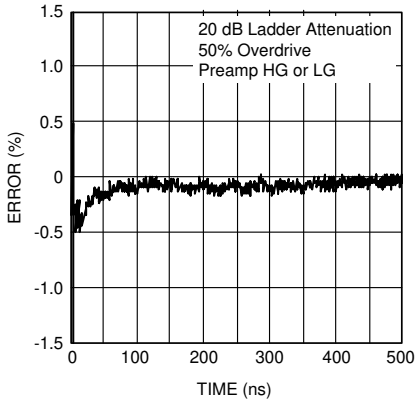


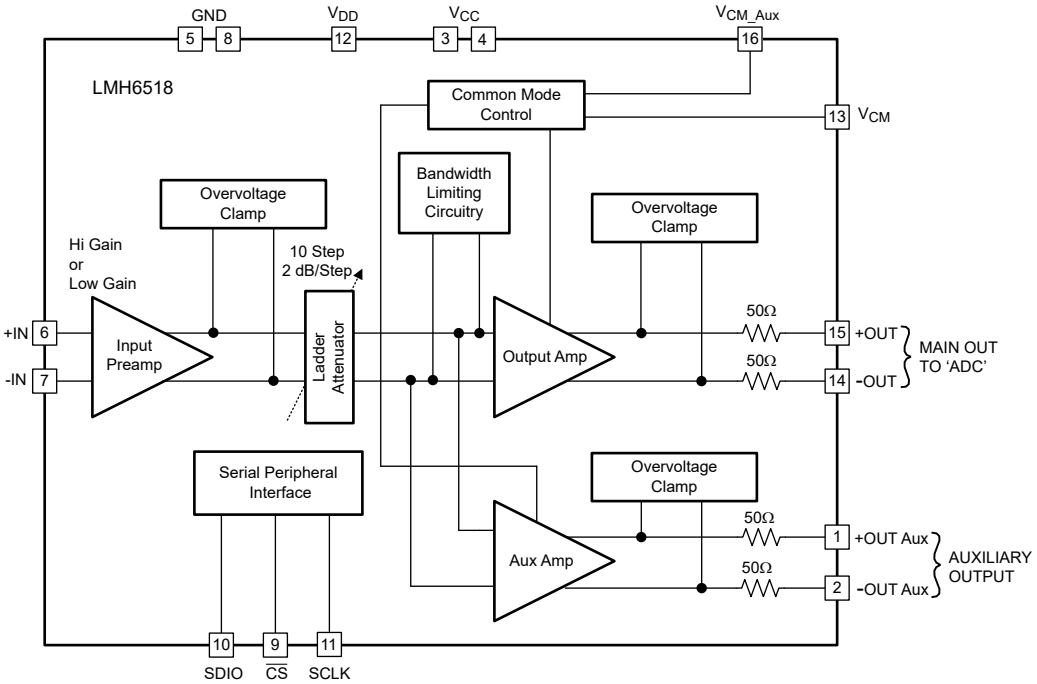
図 5-53. Overdrive Recovery Time (Return to Zero)

6 Detailed Description

6.1 Overview

The LMH6518 is a digitally-controlled variable gain amplifier (DVGA) that is designed specifically as an oscilloscope analog front end (AFE). This device samples an analog voltage and conditions the voltage for the analog to digital converter (ADC) input. This device is specifically designed to drive TI's giga sample ADCs that have a 100-Ω input impedance and 800 mV_{PP} full-scale input voltage.

6.2 Functional Block Diagram



6.3 Feature Description

The LMH6518 offers several unique features in addition to being a general purpose digital variable gain amplifier (DVGA).

6.3.1 Input Preamplifier

The LMH6518 has a fully differential preamplifier which has a consistent 150-kΩ impedance across all gain settings. The LMH6518 is also driven with a single-ended signal source. The preamplifier has two gain settings. See *セクション 7.2.1.2.2* for details.

6.3.1.1 Primary Output Amplifier

The LMH6518 has two nearly identical amplifiers. The output amplifier was designed as the primary output amplifier. The output amplifier features an internal 100-Ω termination that interfaces with 100-Ω input impedance ADCs. The output amplifier has a common-mode voltage control pin that sets the output common-mode voltage of the amplifier.

6.3.1.2 Auxiliary Amplifier

The LMH6518 has a second output amplifier that was designed to provide a trigger signal when used as an oscilloscope AFE. The auxiliary amplifier has all of the features of the output amplifier and provides a duplicate signal for use in trigger circuits. The auxiliary amplifier has a common mode voltage control pin which sets the output common mode of the amplifier.

6.3.2 Overvoltage Clamp

The LMH6518 features two levels of clamps used to protect the amplifier and the ADC from voltage transients. These clamps are placed after the input preamplifier and also after the final output amplifier. The clamp voltages are set by the preamp and ladder attenuator logic functions. The SPI bus is used to set and control the preamp (HG or LG) and ladder attenuator (0-dB to 20-dB, 10 states) logic functions.

6.3.3 Attenuator

The primary gain control feature of the LMH65418 is the digital attenuator. The attenuator controls the overall gain of the amplifier. The attenuator has a range of 0-dB to 20-dB of attenuation.

6.3.4 Digital Control Block

The LMH6518 has digitally controlled gain, as well as digitally controlled voltage clamps and digitally controlled bandwidth. If the block is not used, this block can also disable the auxiliary amplifier. セクション 6.5.1 has details on the digital control registers and programming.

6.4 Device Functional Modes

6.4.1 Primary Amplifier

The main functional mode of the LMH6518 is as an AFE providing gain, voltage clamping, and frequency limiting. In this mode, the gain, bandwidth, and voltage swing are all programmable using the SPI control block.

6.4.2 Auxiliary Output

The secondary functional mode of the LMH6518 is the auxiliary output. This output is nearly identical to the primary amplifier. The only difference is that the auxiliary output has slightly lower distortion performance. The auxiliary output was designed to provide a trigger signal when used as an oscilloscope AFE.

6.5 Programming

6.5.1 Logic Functions

The following LMH6518 functions are controlled using the SPI-compatible bus:

- Filters (20 MHz, 100 MHz, 200 MHz, 350 MHz, 650 MHz, 750 MHz, or full bandwidth)
- Power mode (full power or auxiliary high impedance, Hi-Z)
- Preamp (HG or LG)
- Attenuation ladder (0 dB to 20 dB, 10 states)
- LMH6518 state *write* or *read* back

The SPI bus uses 3.3-V logic. *SDIO* is the serial digital input-output that writes to or reads back from the LMH6518. *SCLK* is the bus clock with chip-select function controlled by $\overline{CS}$.

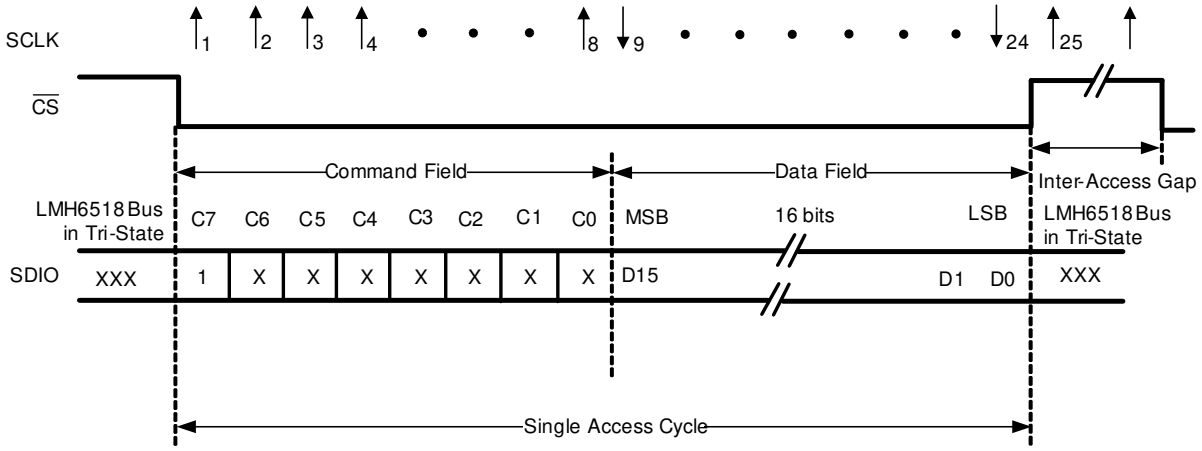


図 6-1. Serial Interface Protocol, Read Operation

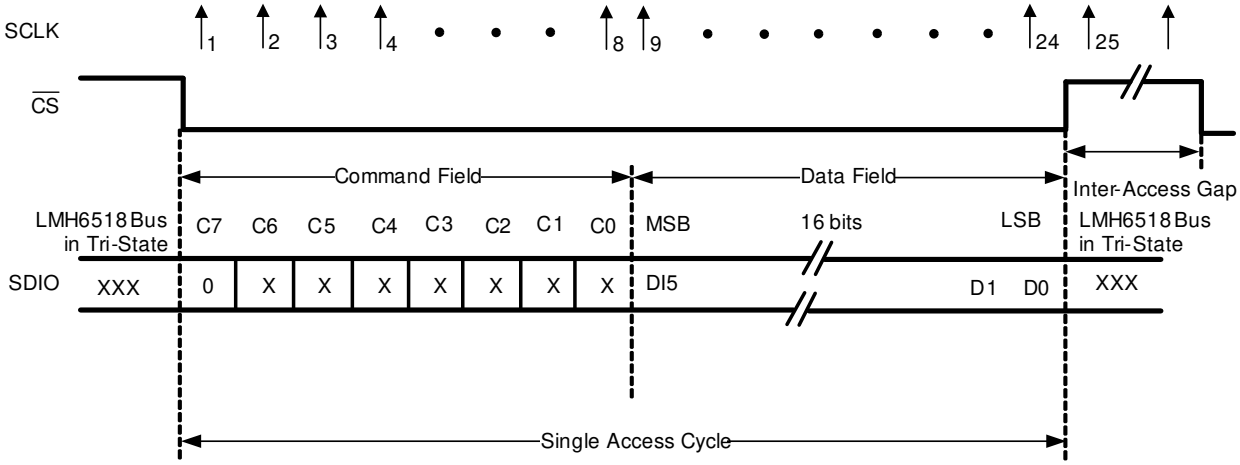


図 6-2. Serial Interface Protocol, Write Operation

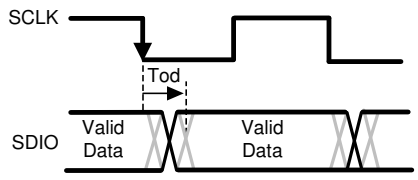


図 6-3. Read Timing

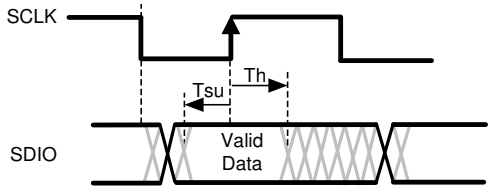


図 6-4. Write Timing

表 6-1. Data Field

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
X	0	0	0	0	0 = Full power 1 = Aux Hi-Z	0	See 表 6-3			0	0 = LG 1 = HG	See 表 6-4			

注

Bits D5, D9, and D11 to D14 must be 0. Otherwise, device operation is undefined and specifications are not valid.

表 6-2. Default Power-On Reset Condition

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

表 6-3. Filter Selection Data Field

FILTER			BANDWIDTH (MHz)
D8	D7	D6	
0	0	0	Full
0	0	1	20
0	1	0	100
0	1	1	200
1	0	0	350
1	0	1	650
1	1	0	750
1	1	1	Unallowed

注

All filters are low-pass, single pole roll-off and operate on both main and auxiliary outputs. These filters are intended as signal path bandwidth and noise limiting.

表 6-4. Ladder Attenuation Data Field

LADDER ATTENUATION				BANDWIDTH (dB)
D3	D2	D1	D0	
0	0	0	0	0
0	0	0	1	−2
0	0	1	0	−4
0	0	1	1	−6
0	1	0	0	−8
0	1	0	1	−10
0	1	1	0	−12
0	1	1	1	−14
1	0	0	0	−16
1	0	0	1	−18
1	0	1	0	−20
1	0	1	1	Unallowed
1	1	0	0	Unallowed
1	1	0	1	Unallowed
1	1	1	0	Unallowed
1	1	1	1	Unallowed

注

An *unallowed* SPI state can result in undefined operation where device behavior is not valid.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The LMH6518 device is an excellent choice for applications that require a differential signal path and drive a differential, high-bandwidth analog-to-digital converter. The LMH6581 has 900 MHz of bandwidth and drives signals up to 1.8 V_{PP}.

Typical applications for the LMH6518 include an oscilloscope AFE, gain control in a radio receiver, and a data-acquisition system.

7.2 Typical Application

7.2.1 Oscilloscope Front End

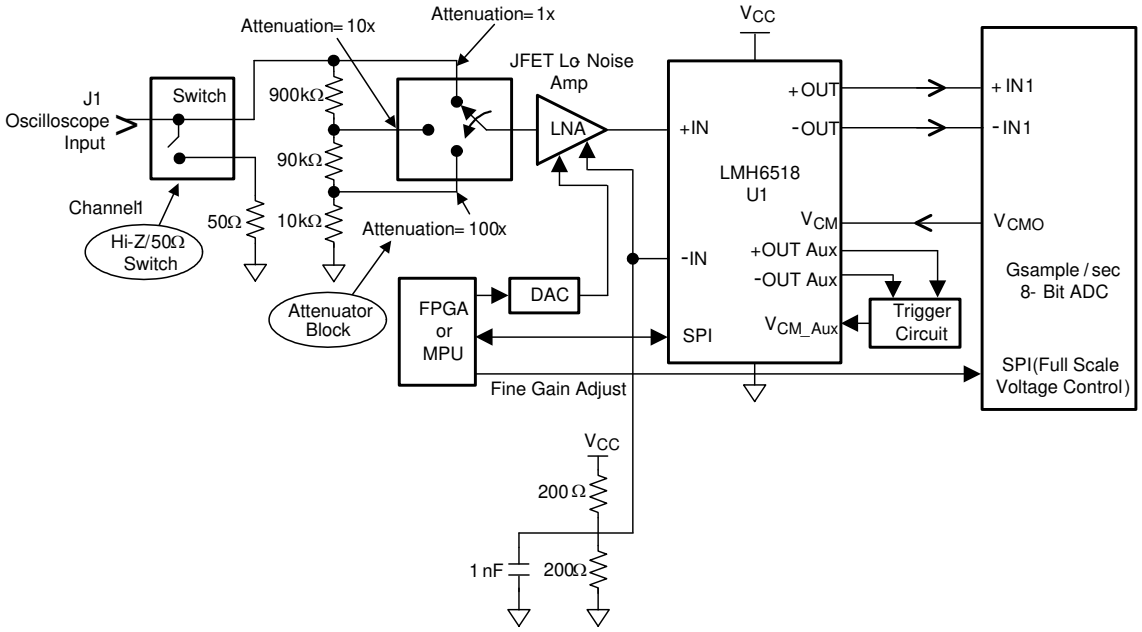


図 7-1. Digital Oscilloscope Front-End

7.2.1.1 Design Requirements

An oscilloscope is used to sample signals from millivolts to volts. To make the best use of the limited ADC input range, the oscilloscope input circuitry must have a wide gain range.

In this design example, the LMH6518 is driving an ADC12J2700 and has the following requirements:

- Common mode voltage = 1.225-V
- Full scale voltage = 650 mV_{PP} to 800 mV_{PP}
- Bandwidth = 900-MHz
- Trigger channel
- Spurious free dynamic range = 50-dB

7.2.1.2 Detailed Design Procedure

図 7-2 shows a block diagram of the LMH6518 main output signal path.

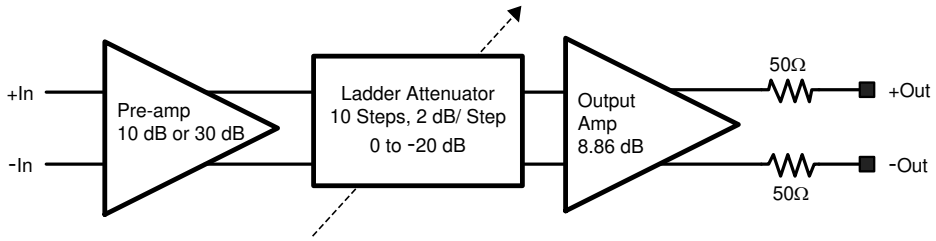


図 7-2. LMH6518 Signal Path Block Diagram

The auxiliary output (not shown) uses another but similar output amplifier that taps into the ladder attenuator output. In this data sheet, preamp gain of 30 dB is referred to as high gain (HG), and preamp gain of 10 dB as low gain (LG).

The LMH6518 2-dB/step gain resolution and 40-dB adjustment range (from −1.16 dB to 38.8 dB). These specifications allow this device to be used with the TI GSPS ADCs, which have full scale (FS) adjustment through the extended control mode (ECM) to provide near-continuous variability (8.5-mdB resolution) that covers 42.6-dB FS input range using 式 1.

$$\left(20 \times \log \frac{920\ mV_{PP}}{6.8\ mV_{PP}} = 42.6\ dB\right) \tag{1}$$

TI's GSPS ECM control allows the ADC FS to be set using the ADC SPI bus. The ADC FS voltage range is from 560 mV to 840 mV with 9 bits of FS voltage control.

The ADC ECM gain resolution is calculated with 式 2.

$$\text{Gain Resolution} = 20 \log \frac{0.56 + \left(\frac{0.84 - 0.56}{2 \times 512}\right)}{0.56 - \left(\frac{0.84 - 0.56}{2 \times 512}\right)} = 8.5\ mdB \tag{2}$$

However, the *recommended* ADC FS operating range is narrower: from 595 mV to 805 mV with 700 mV_{PP} as the midpoint. Raising the value of ADC FS voltage is tantamount to reducing the signal path gain to accommodate a larger input and vice versa, thus providing a method of gain fine-adjust. The ADC ECM gain adjustment is −1.21-dB, as in 式 3.

$$\left(= 20 \times \log \frac{700\ mV}{805\ mV}\right) \text{ to } +1.41\ dB$$

$$\left(= 20 \times \log \frac{700\ mV}{595\ mV}\right) \tag{3}$$

The ADC FS fine-adjust range of 2.62 dB (= 1.41 dB + 1.21 dB) is larger than the LMH6518 2-dB/step resolution; therefore, there is always at least one LMH6518 gain setting to accommodate any FS signal from 6.8 mV_{PP} to 920 mV_{PP} at the LMH6518 input, with 0.62-dB (= 2.62-2) overlap.

Assuming a nominal 0.7-V_{PP} output, the LMH6518 minimum FS input swing is limited by the maximum signal path gain possible and vice versa with 式 4.

$$\text{Maximum LMH6518 FS Input} \frac{0.7\ V_{PP}}{10\left(\frac{(38.8+1.41)\ dB}{20}\right)} = 6.8\ mV_{PP} \tag{4}$$

(or 8 mV_{PP} with no ADC fine adjust in 式 5)

$$\text{Maximum LMH6518 FS Input} \frac{0.7\ V_{PP}}{10\left(\frac{(-1.16-1.21)\ dB}{20}\right)} = 920\ mV_{PP} \tag{5}$$

(or 800 mV_{PP} with no ADC FS adjust)

To accommodate a higher FS input, an additional attenuator is required before the LMH6518. This front-end attenuator is shown in the 図 7-1 with details shown in 図 7-12. The highest minimum attenuation level is determined by the largest FS input signal (FS_{max}) in 式 6.

$$\text{Attenuation (dB)} = 20 \times \log \frac{FS_{MAX}\ (V_{PP})}{800\ mV_{PP}} \tag{6}$$

Therefore, to accommodate 80 V_{PP}, a 40-dB minimum attenuation is required before the LMH6518.

In a typical oscilloscope application, the voltage range encountered is from 1 mV/DIV to 10 V/DIV with eight vertical divisions visible on the screen. One of the primary concerns in a digital oscilloscope is SNR that translates to display trace width to thickness. Typically, oscilloscope manufacturers require the noise level to be low enough so that the *no-input* visible trace width is less than 1% of FS. Experience shows that this corresponds to a minimum SNR of 52 dB.

The factors that influence SNR are:

- Scope front-end noise (Front-end attenuator + scope probe Hi-Z buffer which is discussed later in this data sheet and shown in 図 7-1)
- LMH6518
- ADC

The LMH6518 related SNR factors are:

- Bandwidth
- Preamp used (Preamp HG or LG)
- Ladder attenuation
- Signal level

SNR increases with the inverse square root of the bandwidth. Therefore, reducing bandwidth from 450 MHz to 200 MHz for example, improves SNR by 3.5-dB, as seen in 式 7.

$$\left(20 \times \log \frac{\sqrt{450\ MHz}}{\sqrt{200\ MHz}} = 3.5\ dB\right) \tag{7}$$

The other factors listed previously, preamp and ladder attenuation, depend on the signal level and also impact SNR. The combined effect of these factors is summarized in 図 7-3, where SNR is plotted as a function of the LMH6518 FS input voltage (assuming scope bandwidth of 200-MHz) and not including the ADC and the front-end noise.

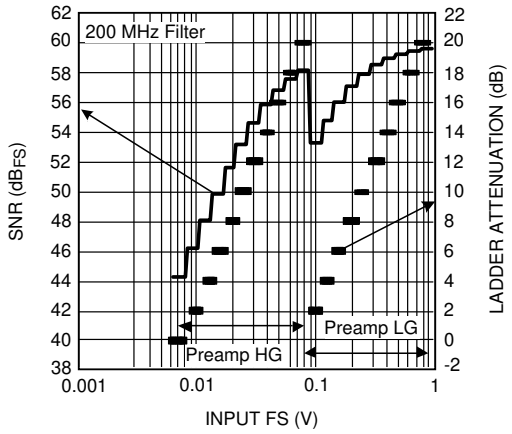


図 7-3. LMH6518 SNR and Ladder Attenuation Used vs Input

As 図 7-3 shows, SNR of at least 52 dB is maintained for FS inputs greater than 24 mV_{PP} (3 mV/DIV on a scope) assuming the LMH6518 internal 200-MHz filter is enabled. Most oscilloscope manufacturers relax the SNR specifications to 40 dB for the highest gain (lowest scope voltage setting). From 図 7-3, the LMH6518 minimum SNR is 43.5 dB, thereby meeting the relaxed SNR specification for the lower range of scope front panel voltages.

In 図 7-3, the step change in SNR near Input FS of 90 mV_{PP} is the transition point from preamp LG to preamp HG with a subsequent 3-dB difference due to the preamp HG to 20-dB ladder attenuation lower output noise compared to preamp LG to 2-dB ladder attenuation noise. Judicious choice of front-end attenuators maintains the 52-dB SNR specification for scope FS inputs ≥ 24 mV_{PP} by confining the LMH6518 gain range to the lower 30.5-dB using 式 8 from the total range of 40-dB (= 38.8 – (−1.16)) is possible.

$$(= 20 \times \log \frac{0.8\ V_{PP}}{24\ mV_{PP}}) \tag{8}$$

For example, to cover the range of 1 mV/DIV to 10 V/DIV (80-dB range), 表 7-1 lists a configuration that affords good SNR.

表 7-1. Oscilloscope Example Including Front-End Attenuators

ROW	SCOPE FS INPUT (V_{PP})	*S*, SCOPE VERTICAL SCALE (V/DIV)	PREAMP	LADDER ATTENUATION RANGE (dB)	*A*, FRONT-END ATTENUATION (V/V)	MINIMUM SNR (dB) WITH 200 MHz FILTER
1	8 m to 24 m	1 m to 3 m	HG	0 to 10	1	44
2	24 m to 80 m	3 m to 10 m	HG	10 to 20	1	52
3	80 m to 0.8	10 m to 0.1	LG	0 to 20	1	53.4
4	0.8 to 8	0.1 to 1	LG	0 to 20	10	53.4
5	8 to 80	1 to 10	LG	0 to 20	100	53.4

In 表 7-1, the highest FS input in row 5, column 2 (80 V_{PP}), *and* the LMH6518 highest FS input allowed (0.8 V_{PP}) set the front-end attenuator value with 式 9.

$$100x\ (= \frac{80\ V_{PP}}{0.8\ V_{PP}}) \tag{9}$$

The 100 × attenuator allows high-SNR operation down to 30.5-dB, as explained earlier, or 2.4 V_{PP} at scope input. In that same table, rows 1 to 3 with no front-end attenuation (1 ×) cover the scope FS input range from 8 mV_{PP} to 800 mV_{PP}. That leaves the scope FS input range of 0.8 V_{PP} to 2.4 V_{PP}. If the 100 × attenuator is used for the entire scope FS range of 0.8 V_{PP} to 80 V_{PP}, SNR dips below 52-dB for a portion of that range. Another attenuation level is thus required to maintain the SNR specification requirement of 52 dB.

One possible attenuation partitioning is to select the additional attenuator value to cover a 20 dB range above 0.8 V_{PP} FS (to 8 V_{PP}) with the 100 × attenuator covering the remaining 20-dB range from 8 V_{PP} to 80 V_{PP}. Mapping 8 V_{PP} FS scope input to 0.8 V_{PP} at LMH6518 input means the additional attenuator is 10 ×, as shown in 表 7-1, row 4. The remaining scope input range of 8 V_{PP} to 80 V_{PP} is then covered by the 100 × front-end attenuator derived earlier. The entire scope input range is now covered with SNR maintained approximately 52 dB for a scope FS input ≥ 24 mV_{PP}, as shown in 表 7-1.

7.2.1.2.1 Settings and ADC SPI Code (ECM)

Covering the range from 1 mV/div to 10 V/div requires the following adjustment within the digital oscilloscope:

- Front-end attenuator
- LMH6518 preamp
- LMH6518 ladder attenuation
- ADC FS value (ECM)

The LMH6518 product folder contains a spreadsheet that helps calculate the front-end attenuator, LMH6518 preamp gain (HG or LG), ladder attenuation, and ADC FS setting based on the scope vertical scale (S in V/div).

The following step-by-step procedure explains the operations performed by the spreadsheet based on the scope vertical scale setting (S in V/div) and front-end attenuation *A* (from 表 7-1). A numerical example is also worked out for more clarification:

1. Determine the required signal path gain, K, with 式 10:

$$K = 20 \times \log \frac{0.95 \times 700\ mV_{PP}}{\frac{8 \times S(V/div)}{A}} = -21.6 + 20 \times \log \frac{A}{S(V/div)} \quad (10)$$

   Assuming the full-scale signal occupies 95% of the 0.7 V_{PP} FS for 5% overhead that occupies eight vertical scope divisions.
   Required condition: −2.37 dB ≤ K ≤ 40.3 dB
   Example: With S = 110 mV/div, 表 7-1 shows that A = 10 V/V in 式 11.

$$\rightarrow K = -21.6 + 20 \times \log \frac{10}{110\ mV} = 17.57\ dB \quad (11)$$

2. Determine the LMH6518 gain, G:
   G is the closest LMH6518 gain to the value of K where
   - G = (38.8 – 2n)dB; n = 0, 1, 2, …, 20

   For this example, the closest G to K = 17.57 dB is 16.8 dB (with n = 11). The next LMH6518 gain, 18.8 dB (with n = 10) is incorrect as 16.8 is closer. If 18.8 dB were mistakenly selected, the ADC FS setting is out of range. Therefore, G = 16.8 dB
3. Determine preamp (HG or LG) and ladder attenuation:
   - If G ≥ 18.8 dB → Preamp is HG and ladder attenuation = 38.8 – G
   - If G < 18.8 dB → Preamp is LG and ladder attenuation = 18.8 – G

   For this example, with G = 16.8 → *Preamp LG* and *Ladder Attenuation = 2 dB* (= 18.8 to 16.8).

4. Determine the required ADC FS voltage, FS_E, with 式 12:

$$FS_E = \frac{S \times 8}{A} \times 1.05 \times 10^{\frac{G}{20}} \quad (12)$$

The *1.05* factor is to add 5% FS overhead margin to avoid ADC overdrive with 式 13.

$$FS_E = \frac{S \times 8}{10} \times 1.05 \times 10^{\frac{16.8}{20}} = 639.3 \text{ mV} \quad (13)$$

Required condition: 0.56 V ≤ FS_E ≤ 0.84 V
Recommend condition: 0.595 V ≤ FS_E ≤ 0.805 V for optimum ADC FS

5. Determine the ADC ECM code ratio with 式 14:

$$\text{ECM (ratio)} = \frac{FS_E - 0.56}{0.28} \quad (14)$$

where

- 0.28 V = (0.84 – 0.56) V
- 0.56 V is the lower end of the ADC FS adjustability

For this example:

$$\text{ECM (ratio)} = \frac{0.6393 - 0.56}{0.28} = 0.283$$

Required condition: 0 ≤ ECM (ratio) ≤ 1

6. Determine the ECM binary code sent on ADC SPI bus:
   - Convert the ECM value represented by the ratio calculated previously, to binary:
   - ECM (binary) = DEC2BIN{ECM(ratio) × 511, 9}
     where *DEC2BIN* is a spreadsheet function that converts the decimal ECM ratio, from step 5, multiplied by 511 distinct levels, into binary 9 bits.

注

The web-based spreadsheet computes ECM without the use of *DEC2BIN* function to ease use by all spreadsheet users who do not have this function installed.

For this example: ECM (binary) = DEC2BIN(0.283 × 511, 9) = 010010000. This number is sent to the ADC on the SPI bus to program the ADC to proper FS voltage.

7.2.1.2.2 Input and Output Considerations

The LMH6518 ideal input and output conditions, considered individually, are listed in 表 7-2.

表 7-2. LMH6518 Ideal Input and Output Conditions

IMPEDANCE FROM EACH INPUT TO GROUND (Ω)	COMMON MODE INPUT (V)	DIFFERENTIAL INPUT (V_{PP})	LOAD IMPEDANCE (Ω)	DIFFERENTIAL OUTPUT (V)	COMMON MODE OUTPUT (V)
≤50	1.5 to 3.1	< 0.8	100 (differential) and 50 (single-ended)	< 0.77	0.95 to 1.45

In addition to the individual conditions listed in 表 7-2, the input and output terminal conditions must match differentially (that is, +IN to −IN and +OUT to −OUT), as well, for best performance.

The input is differential but is driven single-ended as long as the conditions of 表 7-2 are met, and there is good matching between the driven and undriven inputs from DC to the highest frequency of interest. If not, there is a settling time impact among other possible performance degradations. The data-sheet specifications are with

single-ended input, unless specified. 図 7-4 is the recommended bench-test schematic to drive one input and to bias the other input with good matching in mind.

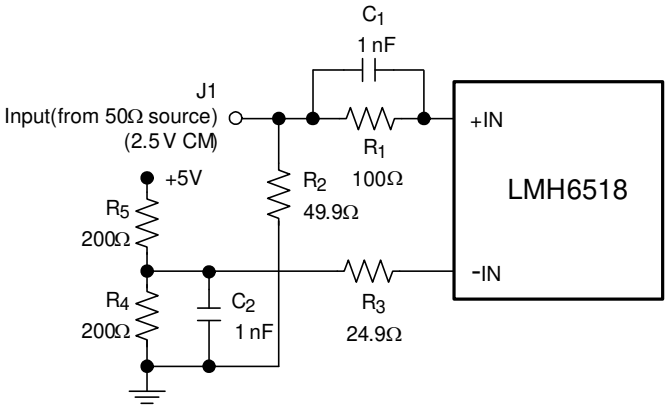


図 7-4. Recommended Single-Ended Bench-Test Input Drive from 50-Ω Source

With 図 7-4, each LMH6518 input sees 25-Ω to ground at higher frequencies when the capacitors look like shorts. This impedance increases to 125-Ω at DC for both inputs, thereby preserving the required matching at any frequency. This configuration, using properly selected R's and C's, allows four times less biasing power dissipation than when undriven inputs are biased with an effective 25-Ω from the LMH6518 input to ground.

Driving the LMH6518 input from a ground-referenced, 50-Ω source is possible by providing level shift circuitry on the driven input. 図 7-5 shows a circuit where half the input signal reaches the LMH6518 input, while the negative supply voltage (V_{EE}) prevents biasing current on the 50-Ω source at J1 while providing 50-Ω termination to the source. The driven input (+IN) is biased to 2.5-V (V_{CC}/2) in 図 7-5.

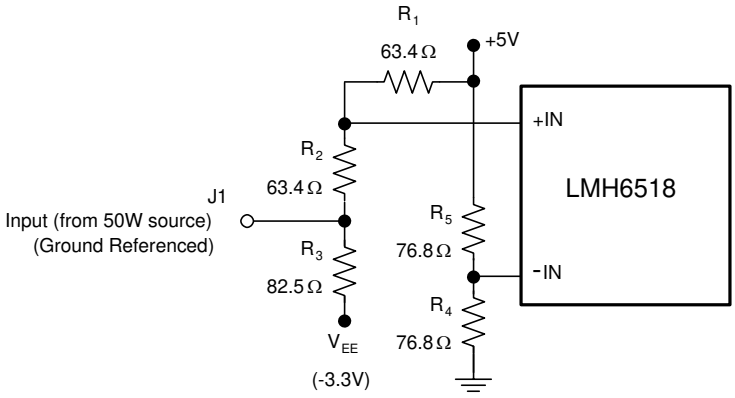


図 7-5. LMH6518 Driven by a Ground-Referenced Source

In 図 7-5, the equivalent impedance from each LMH6518 input to ground is around 38-Ω. The power consumption of this configuration is approximately 0.5 W (in R_1 – R_5) which is higher than that of 図 7-4 because of additional power dissipated to perform the level shifting. Additional 50-Ω attenuators is placed between J1 and R_2/R_3 junction in 図 7-5 to accommodate higher input voltages.

Shifting the LMH6518 *output* common mode level is also possible by using a level shift approach similar to that of 図 7-5. The circuit in 図 7-6 shows an implementation where the LMH6518 nominal 1.2-V CM output, set by a

1.2-V on V_{CM} input from the GSPS ADC, is shifted lower for proper interface to different ADCs (which require V_{CM} = 0-V and have high input impedance).

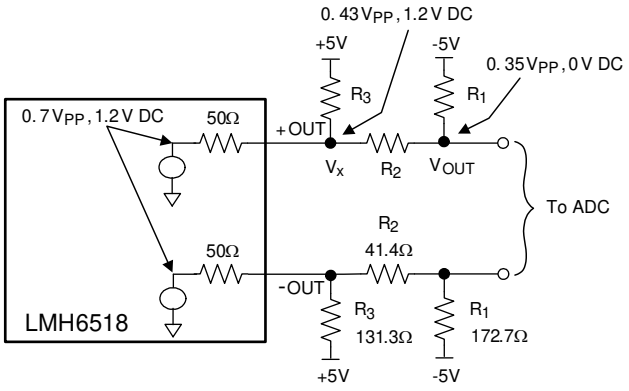


図 7-6. Output CM Shift Scheme

In 図 7-6, Vx is kept at 1.2-V by proper selection of external resistor values, so that the LMH6518 outputs are not CM-loaded. As was the case with input level shifting, this output-level shifting also consumes additional power (0.58 W).

7.2.1.2.2.1 Output Swing, Clamping, and Operation Beyond Full Scale

One of the major concerns when interfacing to low-voltage ADCs (such as the GSPS ADC that the LMH6518 is intended to drive) is to ensure that the ADC input is not violated with excessive drive. For this reason, plus the important requirement that an oscilloscope recovers quickly and gracefully from an overdrive condition, the LMH6518 is fitted with three overvoltage clamps: one at the preamp output, and one each at the main and auxiliary outputs. The preamp clamp is responsible for preventing the preamp from saturation (to minimize recovery time) with large ladder attenuation when preamp output swing is highest. Alternatively, the output clamps perform this function when ladder attenuation is lower. Therefore, the output amplifier is closer to saturation and prolonged recovery (if not properly clamped). The combination of these clamps results in 図 5-50, 図 5-51, 図 5-52, and 図 7-9. With these four graphs, observe where output limiting starts due to the clamp action. LMH6518 owes the fast recovery time (< 5 ns) from 50% overdrive to these clamps.

図 5-50, 図 5-51, 図 5-52, and 図 7-9 in *セクション 5.7* are used to determine the LMH6518 linear swing beyond full scale. This information sets the overdrive limit for both oscilloscope waveform capture and signal triggering. The preamp clamp is set tighter than the output clamp, evidenced by lower output swing with 20-dB ladder attenuation than with 0 dB. With high ladder attenuation (20 dB) defining the limit, the graphs show that the +OUT and −OUT difference of 0.4-V is well inside the clamp range, thereby providing 0.8 V_{PP} of unhindered output swing. This corresponds to an overdrive capability of approximately ±7% beyond full scale.

From 図 7-1, the signal path consists of the input impedance switch, the attenuator switch, low-noise amplifier (LNA, JFET amplifier) to drive the LMH6518 input (+IN), and the DAC to provide offset adjust. The LNA must have the following characteristics:

- Set the U1 common-mode level to V_{CC} / 2 (approximately 2.5 V)
- Low drift (1-mV shift at LNA output can translate into 88-mV shift at the LMH6518 output at maximum gain, or approximately 13% of FS)
- Low output impedance (≤ 50 Ω) to drive U1 for good settling behavior
- Low noise (< 0.98 nV/$\sqrt{\text{Hz}}$) to reduce the impact on the LMH6518 noise figure. Be aware that 図 7-1 does not show the necessary capacitors across the resistors in the front-end attenuators (see 図 7-12). These capacitors provide frequency response compensation and limit the noise contribution from the resistors so that the resistors do not impact the signal path noise. For more information about front-end attenuator design, including frequency compensation, see *セクション 8.2.1* for additional resources.

- Gain of 1 V/V (or close to 1 V/V)
- Excellent frequency response flatness from dc to > 500 MHz to 800 MHz to not impact the time domain performance

The undriven input (−IN) is biased to V_{CC} / 2 using a voltage driver. The impedance driving the LMH6518 −IN pin must be closely matched to the LNA output impedance for good settling-time performance.

セクション 7.2.2 shows one possible implementation of the LNA buffer along with performance data.

When the LMH6518 auxiliary output is not used, this output can be disabled using the SPI (see *セクション 6.5.1* for the SPI register map). *セクション 5.5* shows that by disabling this output, device power dissipation decreases by the reduction in supply current of approximately 60 mA. 図 7-7 shows that in the absence of heavy common loading, the auxiliary output is at a voltage close to 1.7 V (V_{CC} = 5 V). With higher supply voltages, the auxiliary voltage also increases. Ensure that any circuitry tied to this output is capable of handling the 2.3 V possible under V_{CC} worst-case condition of 5.5 V.

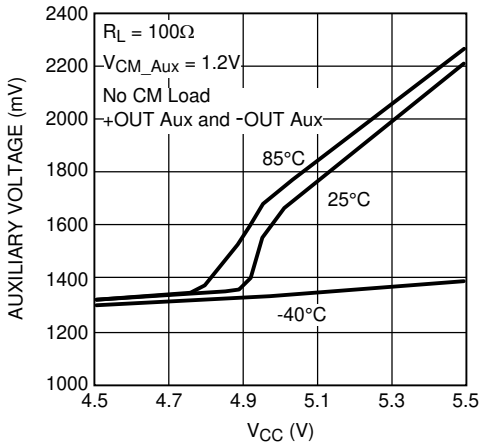


図 7-7. Auxiliary Output Voltage as a Function of V_{CC}

7.2.1.2.3 Oscilloscope Trigger Applications

With the auxiliary output of the LMH6518 offering a second output that follows the main one (except for a slightly reduced distortion performance), the oscilloscope trigger function is implemented by tapping this output. The auxiliary common mode is set with the V_{CM_Aux} input of the LMH6518. If required, the trigger function is placed at a distance from the main signal path by taking advantage of the differential auxiliary output and rejecting any board-related common-mode interference pick-up at the receive end.

If trigger circuitry is physically close to the LMH6518, the circuit diagram shown in 図 7-8 allows operation using only one of two auxiliary outputs. Unused outputs require proper termination using R_1, R_{11} combination. U3 (DAC101C085) generates a 0-V to 2.5-V trigger level, with 2.4-mV resolution as in 式 15 or 0.7% (= 2.4-mV × 100/0.35 V_{PP}) of FS, which is compared to the LMH6518 +OUT AUX by using an ultra-fast comparator, U2 (LMH7220). The U2 complimentary LVDS output is terminated in the required 100-Ω load (R_{10}), for best performance, where the LVDS trigger output is available.

$$\left(=\frac{2.5V}{2^{10}}\right) \tag{15}$$

The LMH7220 offset voltage (±9.5 mV) and offset voltage drift (±50-µV/°C) error is 5.9 LSB of the trigger DAC (U3) as in 式 16.

$$(9.5\ \text{mV} + 50\ \frac{\mu\text{V}}{^\circ\text{C}} \times 100^\circ\text{C} = 1.45\ \text{mV} \equiv 5.9\ \text{LSB}) \tag{16}$$

The offset voltage related portion of this error is nulled, if necessary, during the oscilloscope initial calibration. To do so, the LMH6518 input is terminated properly with no input applied and U3 output is adjusted around V_{CM_Aux} voltage (1.2 V ±10 mV) while looking for the U2 output transition. The U3 output, relative to V_{CM_Aux} at transition corresponds to the U2 offset error, which is factored into the trigger readings and thus eliminated, leaving only the offset voltage temperature drift component (= 2 LSB).

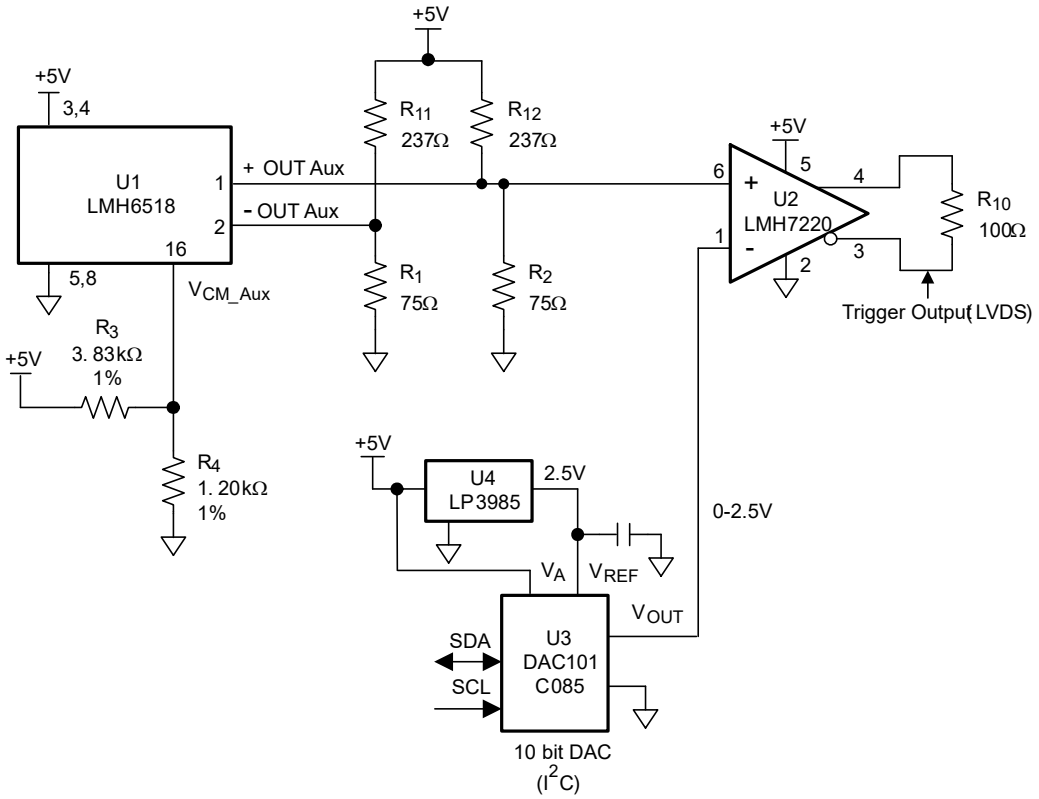


図 7-8. Single-Ended Trigger From the LMH6518 Auxiliary Output

The U2 minimum toggle rate specification of 750Mbps with ±50-mV overdrive allows the oscilloscope to trigger on repetitive waveforms much greater than the 500-MHz oscilloscope bandwidth applications, when the input signal is at least 14.3% of FS swing with 式 17.

$$\left(= \frac{50\ \text{mV}}{\frac{0.7\text{V}}{2}} \times 100\right) \tag{17}$$

The worst-case, single-event, minimum-discernible pulse duration is set by the LMH7220 propagation delay specification of 3.63 ns (20-mV overdrive).

Both the main and the auxiliary outputs recover gracefully and quickly from a 50% overdrive condition, as tabulated in *セクション 5.5* under overdrive recovery time. However, overdrive conditions beyond 50% can result in longer recovery times due to the interaction between an internal clamp and the common-mode feedback loop that sets the output common-mode voltage. This long recovery time can have an impact on both the displayed waveform and the oscilloscope trigger. The result is a loss of trigger pulse or visual distortion of the displayed

waveform. To avoid this scenario, the oscilloscope must detect an excessive overdrive and go into trigger-loss mode. Done in this way, the oscilloscope display shows the last waveform that did not violate the overdrive condition. Preferably, there is a visual indicator on the screen that alerts the user of the excessive condition, and returns the display to normal after the condition is corrected.

7.2.1.3 Application Curves

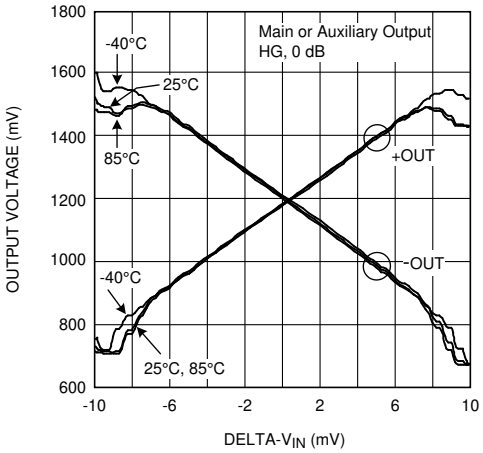


図 7-9. V_{OUT} vs V_{IN}

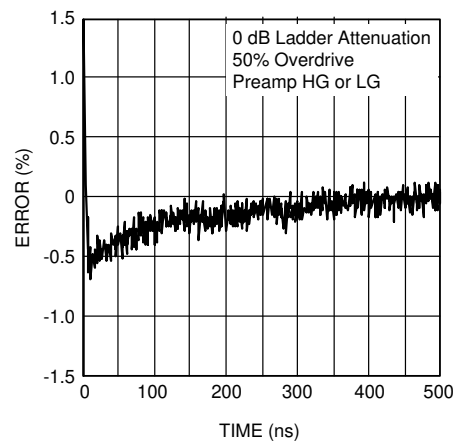


図 7-10. Overdrive Recovery

7.2.2 JFET LNA Implementation

図 7-11 shows the schematic drawing for a possible implementation of the LNA buffer.

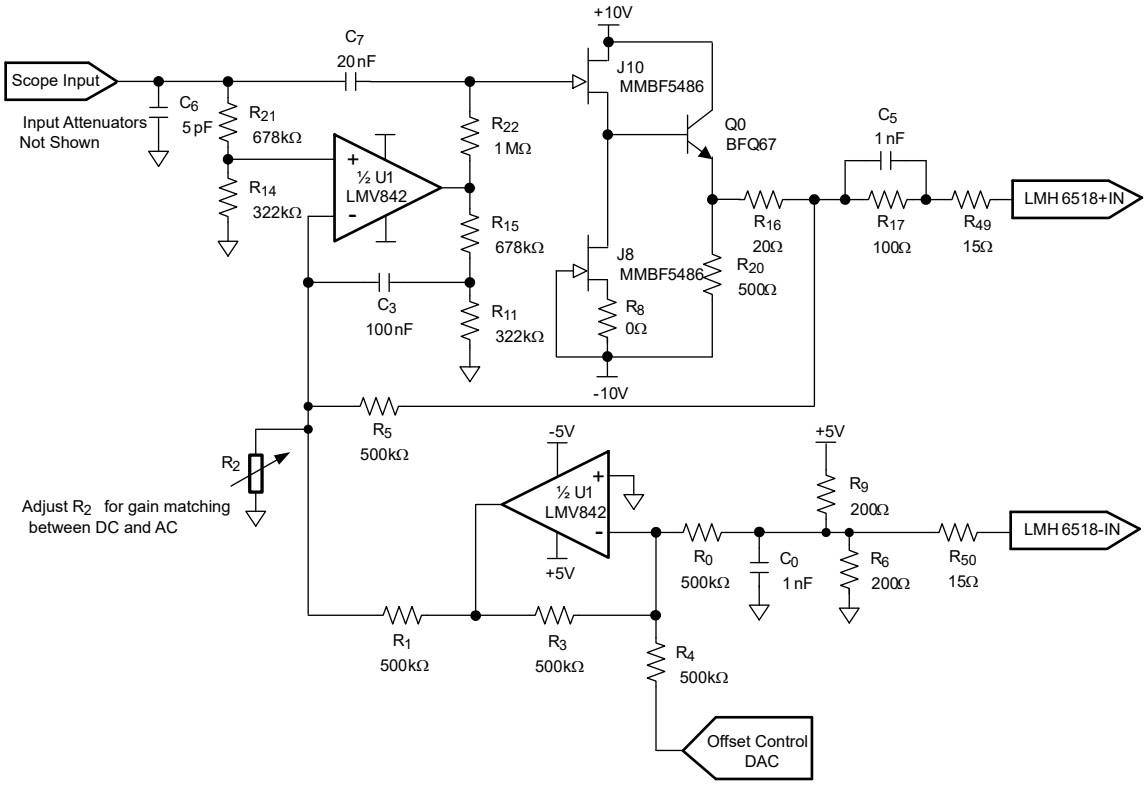


図 7-11. JFET LNA Implementation

7.2.2.1 Design Requirements

This circuit uses an N-Channel JFET (J10) in source-follower configuration to buffer the input signal with J8 acting as a constant current source. This buffer presents a fixed input impedance (1 MΩ || 10 pF) with a gain close to 1-V/V.

The signal path is ac-coupled through C_7 with dc (and low frequency) at LMH6518 +IN maintained through the action of U1. NPN transistor Q0 is an emitter follower which isolates the buffer from the load (LMH6518 input and board traces).

The undriven input of the LMH6518 (−IN) is biased to 2.5-V by R_6, R_9 voltage divider. The lower half of U1 inverts this voltage and the upper half of U1 compares this voltage to the combination of the driven output level at LMH6518 +IN and the scaled version of scope input at R_{14}, R_{21} junction, and adjusts J10 Gate accordingly to set the LMH6518 +IN. This control loop has a frequency response that covers dc to a few Hz, limited by roll-off capacitor C_3 and R_{15} combination (first order approximation). DC and low-frequency gain is given by 式 18.

$$\text{Gain (DC)} = \frac{R_{14}}{R_{14} + R_{21}} \left(1 + \frac{R_5}{R_1 \parallel R_2}\right) \cong 1 \text{ V/V} \tag{18}$$

With the values in 図 7-11 → R_2 approximately 452 kΩ.

For a flat frequency response, the dc (low frequency) gain requires lowering to match the less-than-1 V/V ac (high frequency) path gain through the JFETs. This is done by increasing the value of R_2.

Choose values of R_{15} and R_{11} so that the frequency response at J10 Gate (and consequently the output) remain flat when C_7 starts to conduct as in 式 19.

$$\frac{R_{21}}{R_{14}} = \frac{R_{15}}{R_{11}} \tag{19}$$

Offset correction is done by varying the voltage at R_4, using a DAC or equivalent as shown, to shift the LMH6518 +IN voltage relative to −IN. The result is a circuit which shifts the ground referenced scope input to 2.5-V (V_{CC} / 2) CM with adjustable offset and without any JFET or BJT related offsets.

The front-end attenuator (not shown) lower leg resistance is increased for proper divider-ratio to account for the 1-MΩ shunt due to the series combination of R_{21} and R_{14}. For example, a 10:1 front-end attenuator is formed by a series 900 kΩ and a shunt 111 kΩ for a scope BNC input impedance of 1 MΩ (= 900 K + (111 K || 1 M)).

表 7-3 lists other possible JFET candidates that fall in the range of speed (f_t) and low-noise requirement.

表 7-3. Selected JFET Candidates Specifications

COMPANY	PART NUMBER	V_P (V)	I_{dss} (mA)	gm (mS)	INPUT C (pF)	NOISE(1) (nV/RtHz)	BREAK DOWN (V)	CALCULATED f_t (MHz)
Interfet	IF140	–2.2	10	5.5	2.3	4	–20	380
Interfet	IF142	–2.2	10	5.5	2.3	4	–25	380
Interfet	2N5397/8	–2.5	13	8	5	2.5	–25	254
Interfet	2N5911/2	–2.5	13	8	5	2.5	—	254
Interfet	J308/9/10	–2.3	21	17	5.8	—	–25	466
Philips	BF513	–3	15	10	5	—	—	318
Fairchild	MMBF5486	–4	14	7	4	2.5	–25	278
Vishay Siliconix	SST441	–3.5	13	6	3.5	4	–35	272

(1) Noise data at approximately I_{dss} / 2.

The LNA noise can degrade the scope SNR if comparable to the input-referred noise of the LMH6518. LNA noise is influenced by the following operating conditions:

1. JFET equivalent input noise
2. BJT base current

Reducing either *a* or *b* above, or both, reduces noise. One way to reduce *a* is to increase R_8 (currently set to 0 Ω). This reduces the noise impact of J8 but requires a JFET which has a higher I_{dss} rating to maintain the operating current of J10, so that the J10 noise contribution is minimized. Reducing the BJT base current is accomplished with increasing R_{20} at the expenses of higher rise and fall times. A higher β also reduces the base current (keep in mind that β and f_t at the operating collector current is what matters).

図 7-13 shows the impact of the JFET buffer noise on SNR, compared to SNR in 図 7-3, assuming either 3-nV/√Hz or 1.5-nV/√Hz buffer noise for comparison.

7.2.2.2 Detailed Design Procedure

7.2.2.2.1 Attenuator Design

図 7-12 shows a front-end attenuator designed to work with 図 7-11.

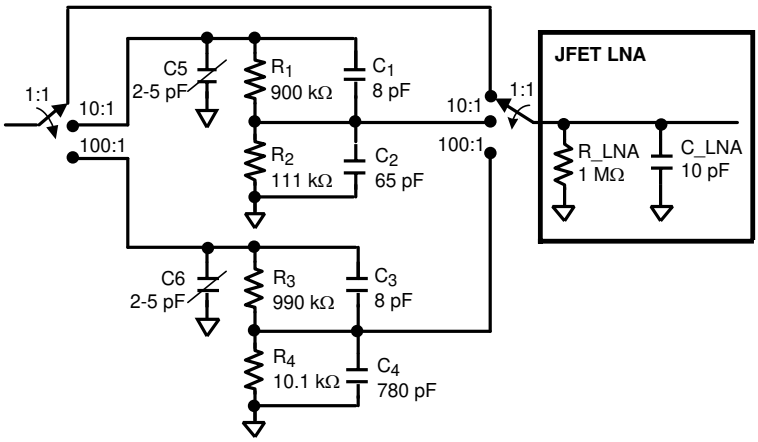


図 7-12. Front-End Attenuator for JFET LNA Implementation

R_LNA and C_LNA are the input impedance components of the JFET LNA. The 10:1 and 100:1 attenuators bottom resistors (R_2 and R_4) are adjusted higher to compensate for the LNA 1-MΩ input impedance, compared to the case where a high-input-impedance LNA is used. The two switches used on the input and output of the attenuator block are low-capacitance, high-isolation switches to reduce any speed or crosstalk impact. Capacitors C_1 to C_4 provide the proper frequency response (and step response) by creating zeros that flatten the response for wide-band operation. For the 10:1 attenuator, $R_1C_1 = R_2C_2$. The same applies to the 100:1 attenuator. The shunt capacitors, C_1 to C_4, have a important other benefit in that these capacitors roll off the resistor thermal noise at a low frequency (low-pass response, −3-dB down at approximately 20-kHz), thereby eliminating any significant noise contribution from the attenuation resistors. Otherwise, the channel noise is dominated by the attenuator resistor thermal noise. Adjust trimmer capacitors C_5 and C_6 to match the input capacitance regardless of attenuator used.

7.2.2.3 Application Curve

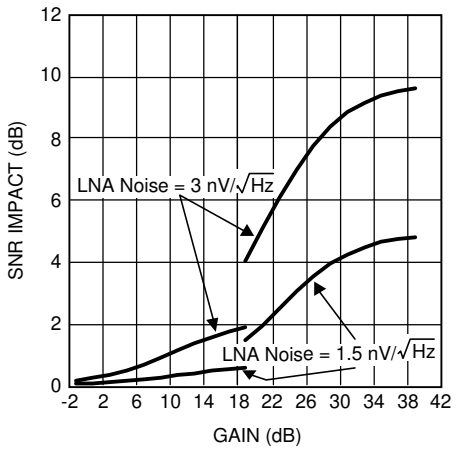


図 7-13. LNA Buffer SNR Impact

7.3 Power Supply Recommendations

The LMH6581 requires two power supplies. The analog signal path is powered by a single 5-V (±5%) supply and the digital control is powered by a single 3.3-V (±5%) supply. The 5-V supply must be capable of providing the 230-mA of quiescent current plus any load current. Make sure that the loads of both amplifiers are included.

The 3.3-V digital supply requires only a small, 400-µA current.

Place supply bypass capacitors at pins 3, 4, and 12. Low-ESR, ceramic capacitors of 0.01-µF are recommended.

7.4 Layout

7.4.1 Layout Guidelines

Layout is critical to achieve specified performance. Circuit symmetry is necessary for good HD2 performance. Input traces must have impedance-controlled transmission lines. To reduce output to input coupling, use ground plane to fill between the amplifier input and output traces. Output termination resistors are provided on chip internally to the LMH6518. When driving an ADC, the ADC must be placed physically close to the LMH6518 output pins. Use controlled impedance transmission lines if the ADC must be placed farther than 10 mm from the amplifier output pins.

7.4.2 Layout Example

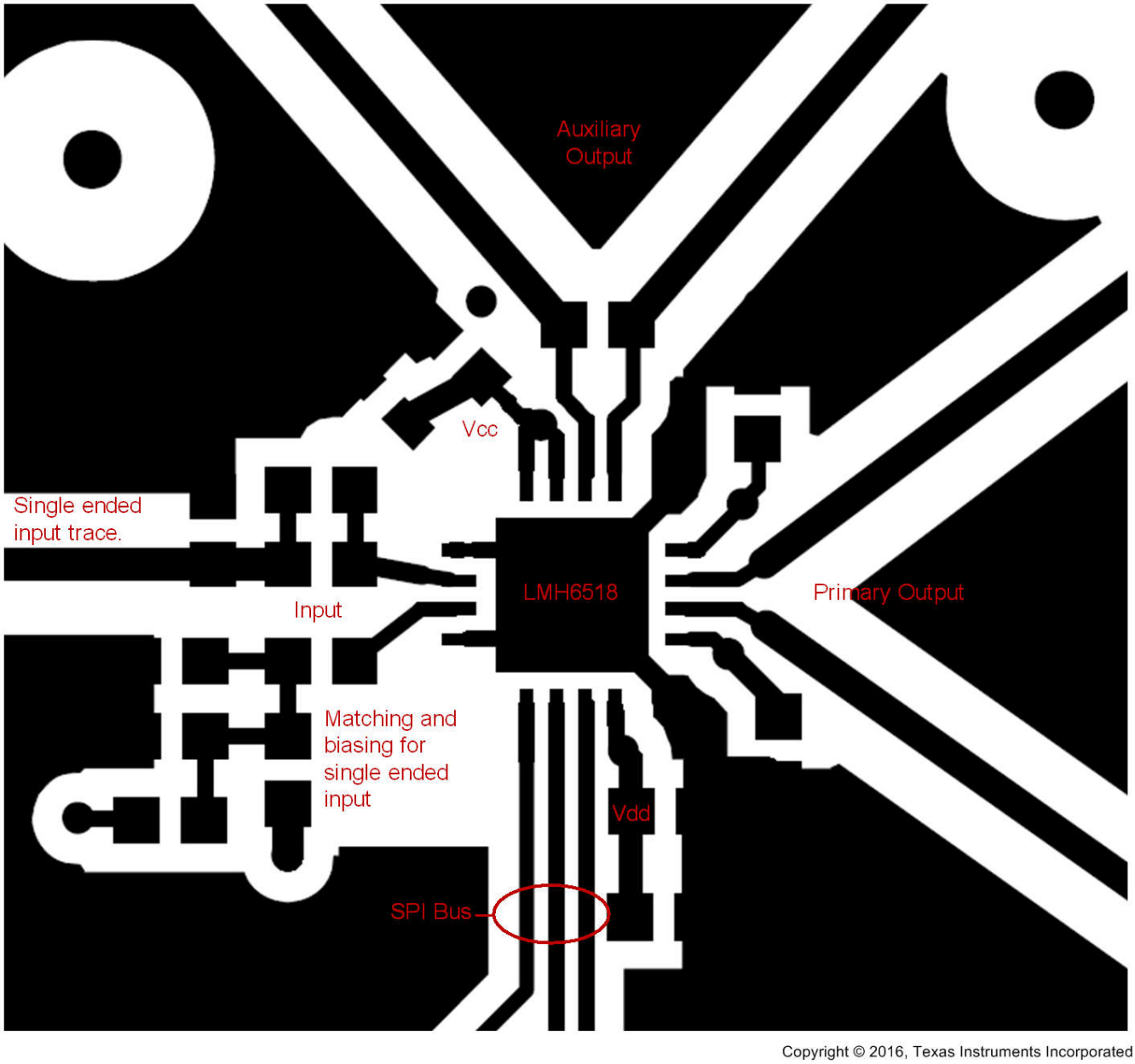


図 7-14. LMH6518 Layout Schematic

8 Device and Documentation Support

8.1 Device Support

8.1.1 サード・パーティ製品に関する免責事項

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8.1.2 Device Nomenclature

表 8-1. Definition of Terms and Specifications

TERM	DEFINITION
A_{V_CM} (dB)	Change in output offset voltage (ΔV_{OOS}) with respect to the change in input common-mode voltage (ΔV_{I_CM})
A_{V_DIFF} (dB)	Gain with 100-Ω differential load
CM	Common mode
CMRR (dB)	Common-mode rejection defined as: A_{V_DIFF} (dB) – A_{V_CM} (dB)
CMRR_CM	Common-mode rejection relative to V_{CM} defined as: ΔV_{OOS} /ΔV_{CM}
HG	Preamp high gain
Ladder	Ladder attenuator setting (0 dB to 20 dB)
LG	Preamp low gain
Max Gain	Gain = 38.8 dB
Min Gain	Gain = −1.16 dB
+OUT	Positive main output
−OUT	Negative main output
+OUT AUX	Positive auxiliary output
−OUT AUX	Negative auxiliary output
PB	Phase balance defined as the phase difference between the complimentary outputs relative to 180°
PSRR	Input-referred V_{OOS} shift divided by change in V_{CC}
PSRR_CM	Output common-mode voltage change (ΔV_{O_CM}) with respect to V_{CC} voltage change (ΔV_{CC})
V_{CM}	Input pin voltage that sets main output CM
V_{CM_Aux}	Input pin voltage that sets auxiliary output CM
V_{I_CM}	Input CM voltage (average of +IN and −IN)
ΔV_{IN} (V)	Differential voltage across device inputs
V_{OOS}	DC offset voltage. Differential output voltage measured with inputs shorted together to V_{CC} / 2
V_{O_CM}	Output common-mode voltage (dc average of V_{+OUT} and $V_{–OUT}$)
V_{OS_CM}	CM offset voltage: $V_{O\_CM} – V_{CM}$
ΔV_{O_CM}	Variation in output common-mode voltage (V_{O_CM})
$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$	Balance error. Measure of the output swing balance of +OUT and −OUT, as reflected on the output common-mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common-mode voltage change (ΔV_{O_CM}) divided by the output differential voltage change (ΔV_{OUT}, which is nominally around 700 mV_{PP})
ΔV_{OUT}	Change in differential output voltage (corrected for dc offset, V_{OOS})

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

Wideband Amplifiers by Peter Staric and Erik Margan, published by Springer (2006). (Section 5.2)

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2016) to Revision E (July 2024) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Updated text for clarity in *Pin Configurations and Functions* ... 3
- Updated note 1 text for clarity in the *Absolute Maximum Ratings* ... 4
- Added note 2 in the *Absolute Maximum Ratings* ... 4
- Added new row for maximum dc output *Absolute Maximum Ratings* ... 4
- Updated last sentence in paragraph for clarity in *Layout Guidelines* ... 37

Changes from Revision C (July 2013) to Revision D (September 2016) — **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 ... 1
- Added *Thermal Information* table ... 4
- Changed Y-axis unit on Output vs Input *Typical Characteristics* graphs From: (V) To: (mV) ... 9
- Changed Y-axis unit on V_{OUT} vs V_{IN} *Application Curves* graph From: (V) To: (mV) ... 33

Changes from Revision A (March 2013) to Revision B (March 2013) — **Page**

- ナショナル セミコンダクターのデータシートのレイアウトを テキサス・インスツルメンツ形式に変更 ... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6518SQ/NOPB	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ
LMH6518SQ/NOPB.A	Active	Production	WQFN (RGH) | 16	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ
LMH6518SQE/NOPB	Active	Production	WQFN (RGH) | 16	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ
LMH6518SQE/NOPB.A	Active	Production	WQFN (RGH) | 16	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ
LMH6518SQX/NOPB	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ
LMH6518SQX/NOPB.A	Active	Production	WQFN (RGH) | 16	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

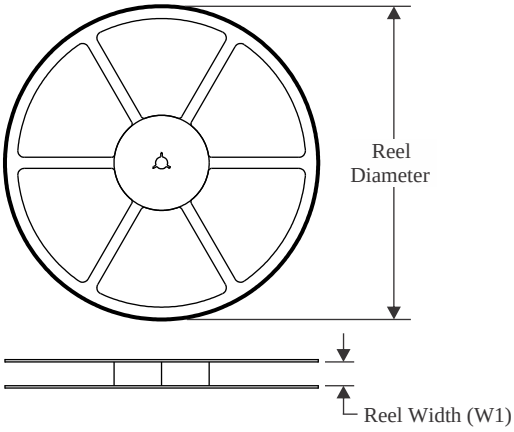
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

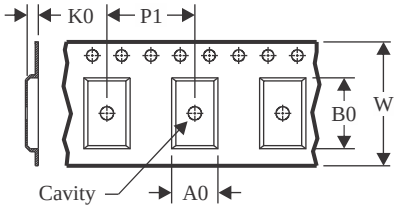
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

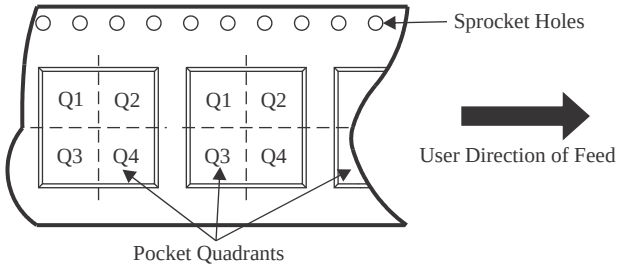


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

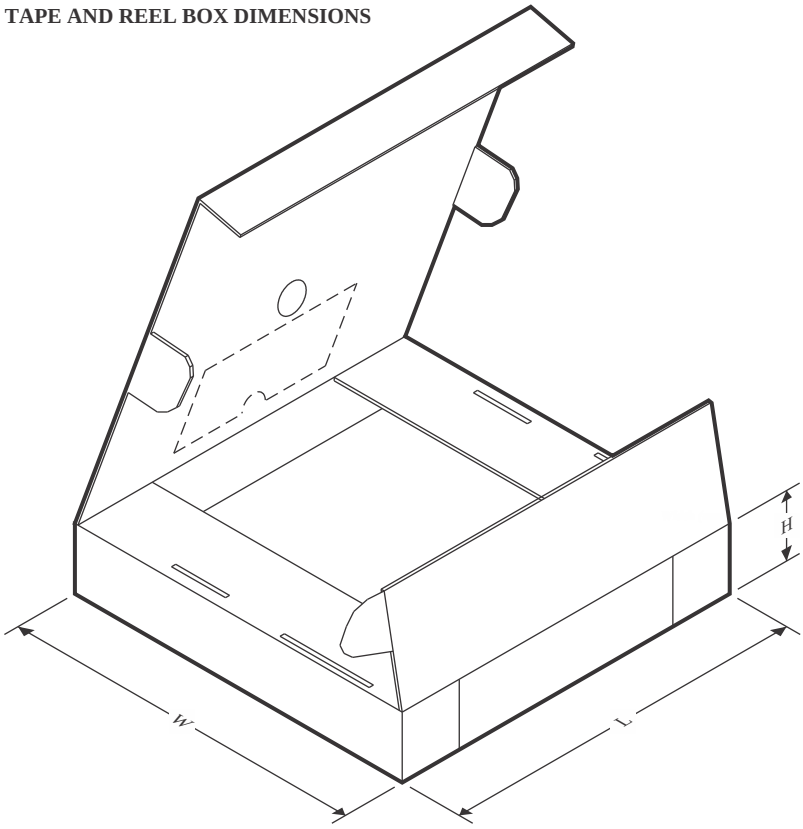
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6518SQ/NOPB	WQFN	RGH	16	1000	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQE/NOPB	WQFN	RGH	16	250	177.8	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQX/NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

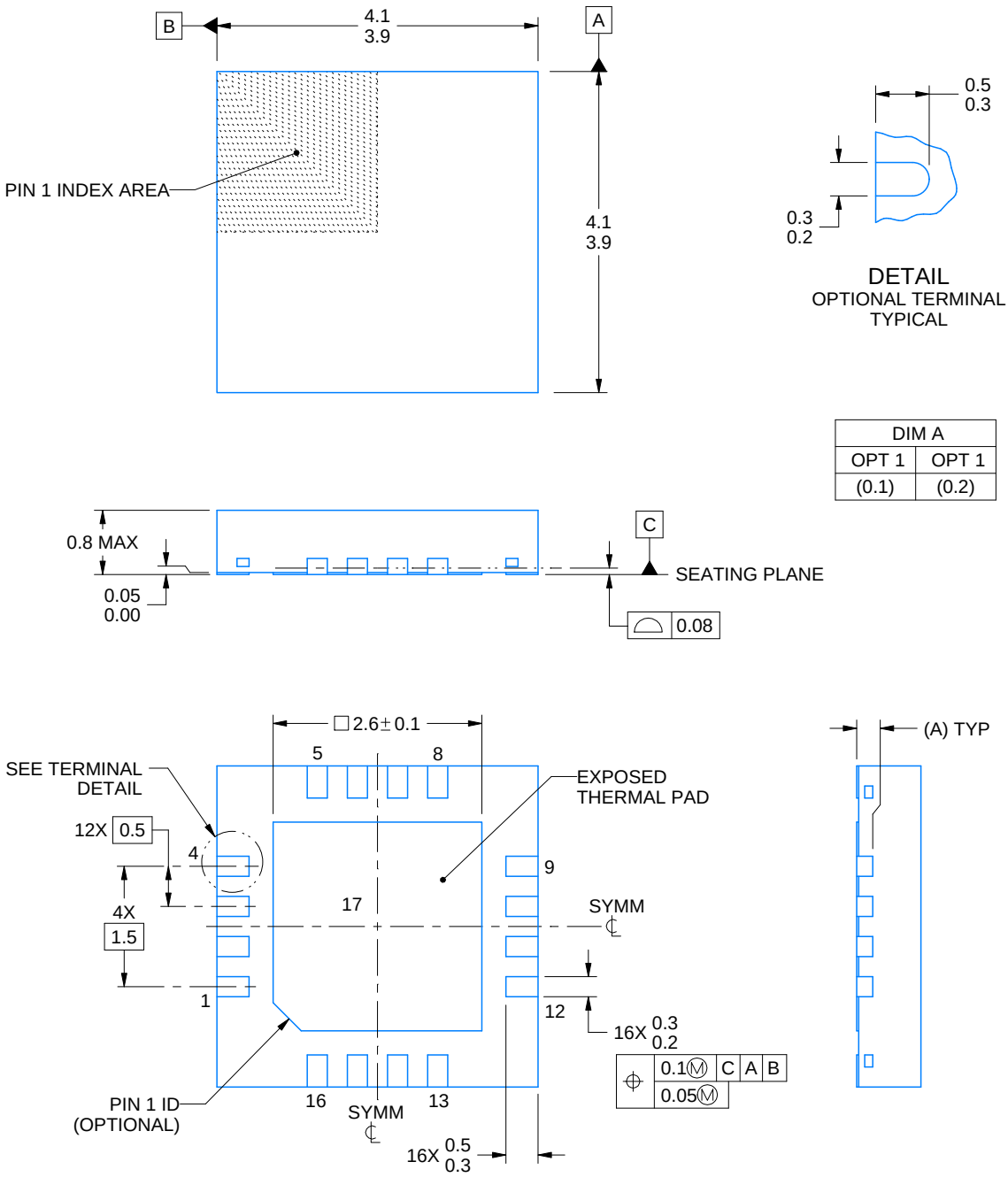
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6518SQ/NOPB	WQFN	RGH	16	1000	208.0	191.0	35.0
LMH6518SQE/NOPB	WQFN	RGH	16	250	208.0	191.0	35.0
LMH6518SQX/NOPB	WQFN	RGH	16	4500	356.0	356.0	36.0

PACKAGE OUTLINE

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

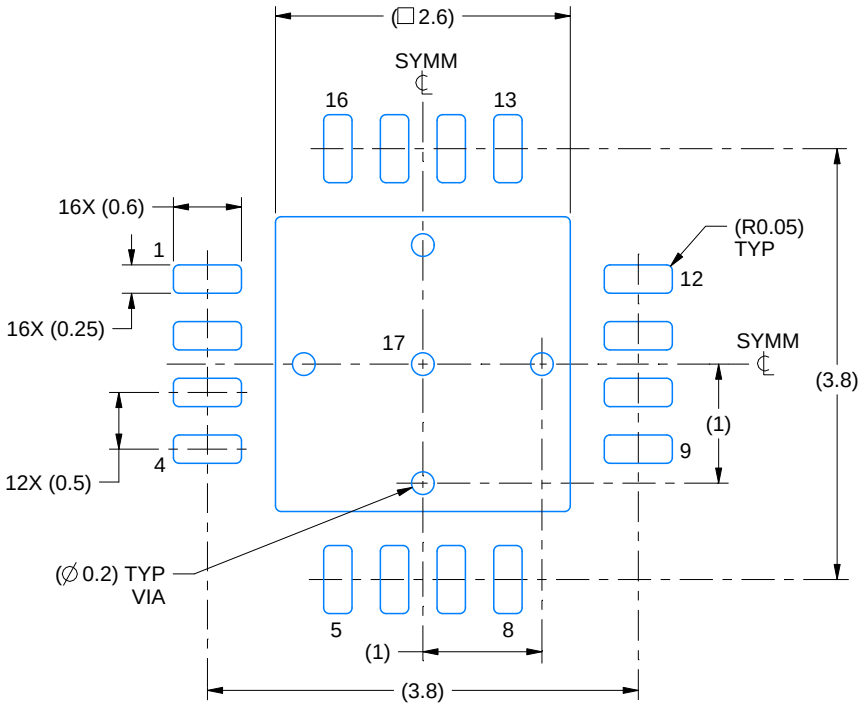
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

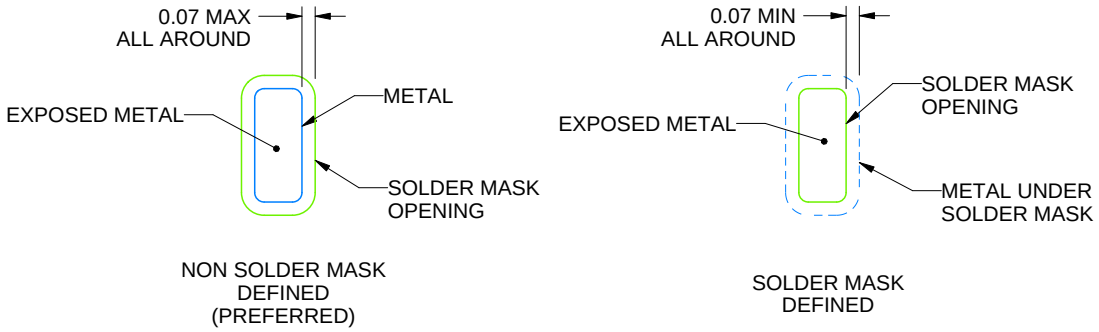
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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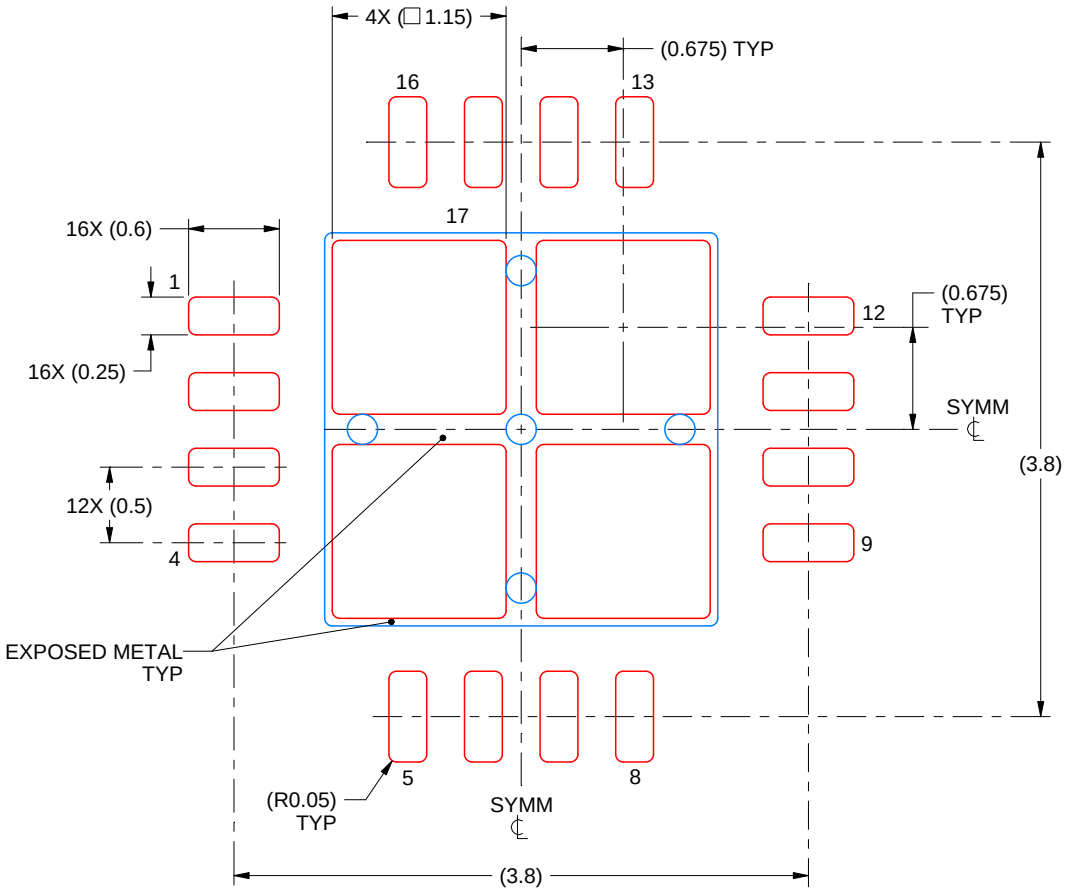
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月