TEXAS INSTRUMENTS
LMH6644-MIL
JAJSDE7 – JUNE 2017

LMH6644-MIL 低消費電力、130MHz、75mA、レール・ツー・レール出力アンプ

1 特長

(V_S = ±5V、T_A = 25℃、R_L = 2kΩ、A_V = +1: 特記ない限り標準値)

- -3dB BW (A_V = +1) 130 MHz
- 電源電圧範囲: 2.7V～12.8V
- スルー・レート (A_V = -1) 130V/μs(1)
- 消費電流(無負荷) 2.7mA/アンプ
- 出力短絡電流: +115mA～145mA
- リニア出力電流: ±75mA
- 入力同相電圧がV^-よりも0.5V、V^+よりも1V拡張
- 出力電圧スイングがレールから40mV
- 入力電圧ノイズ(100kHz): 17nV/√Hz
- 入力電流ノイズ(100kHz): 0.9pA/√Hz
- THD (5MHz、R_L = 2kΩ、V_O = $2V_{PP}$、A_V = +2): –62dBc
- セトリング・タイム: 68ns
- 3V、5V、±5Vで完全に特性を規定
- オーバードライブ回復100ns
- 出力短絡保護(2)
- CMVR超過時に出力位相の反転なし

(1) スルー・レートは立ち上がりと立ち下がりのスルー・レートの平均値です。

(2) 出力短絡期間は、V_S < 6Vで、室温またはそれ以下の気温の場合には無制限です。V_S > 6Vの場合、許容される短絡期間は1.5msです。

2 アプリケーション

- アクティブ・フィルタ
- CD/DVD ROM
- ADCバッファ・アンプ
- ポータブル・ビデオ
- 電流センス・バッファ

3 概要

LMH6644-MILは真の単一電源電圧帰還アンプで、高速(130MHz)、低歪み(-62dBc)、非常に高い出力電流(約75mA)を低コストで実現し、同程度の性能を持つ既存のデバイスと比較して消費電力が低減されています。

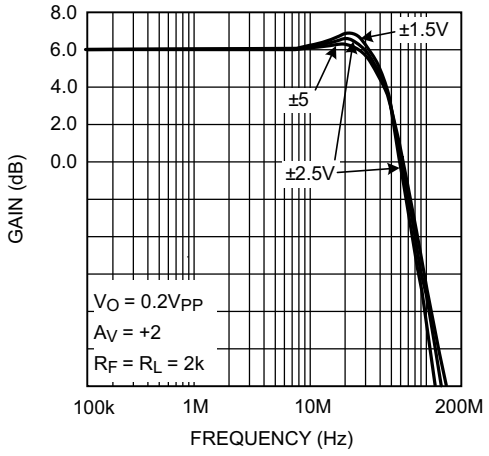
入力同相電圧範囲は、V^-よりも0.5V下、V^+から1Vまで拡張されています。出力電圧範囲は双方の電源レールの40mV以内まで拡張されているため、低電圧アプリケーションで特に望ましい、広いダイナミック・レンジが得られます。出力段は約75mAの能力を持ち、重負荷を駆動可能です。出力スルー・レートが高い(130V/μs)ため、速度が高い場合も大きなピーク・ツー・ピーク出力スイングを維持でき、3V電源から40MHzという非常に優れたフルパワー帯域幅を実現できます。これらの特性と低コストから、多くの産業用および商業用アプリケーションに理想的です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMH6644-MIL	SOIC (14)	8.64mm×3.91mm
	TSSOP (14)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

各種の電源における閉ループ・ゲインと周波数との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	改訂内容	注
2017年6月	*	初版

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5 概要（続き）

あらゆる動作電圧とモードにおいてデバイスの安定性を保証するため、十分な注意が払われています。その結果、あらゆるゲイン設定で、重負荷と軽負荷の両方において、周波数応答特性が非常に優れ(150Ω負荷およびA_V = +2において、12MHzまで0.1dBのゲイン平坦性)、ピーキングが最小限(一般に最大値2dB)です。これらの特性と、短いセトリング・タイム(68ns)、低い歪みから、このデバイスはADCバッファでも、高周波数のフィルタ・アプリケーションでも適切に動作します。

このデバイスは、低い差動ゲイン(0.01%)と差動位相(0.01°)の特性から、プロフェッショナル品質のビデオ性能を実現しています。差動ゲインおよび差動位相の特性は、重負荷時(150Ω)でも、出力電圧範囲の全体にわたって適切に維持されます。

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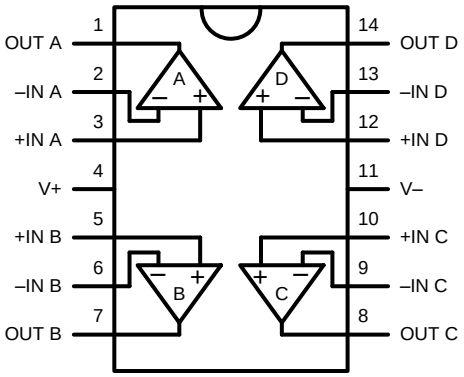
6 Pin Configuration and Functions

Package D14A, PW14A
14-Pin SOIC and 14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	ChA inverting input
+IN A	3	I	ChA non-inverting input
–IN B	6	I	ChB inverting input
+IN B	5	I	ChB non-inverting input
–IN C	9	I	ChC inverting input
+IN C	10	I	ChC non-inverting input
–IN D	13	I	ChD inverting input
+IN D	12	I	ChD non-inverting input
OUT A	1	O	ChA output
OUT B	7	O	ChB output
OUT C	8	O	ChC output
OUT D	14	O	ChD output
V^-	11	I	Negative supply
V^+	4	I	Positive supply

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7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN} differential			±2.5	V
Output short circuit duration		See (3) and (4)		
Supply voltage ($V^+ – V^–$)			13.5	V
Voltage at input/output pins			V^+ +0.8 $V^–$ –0.8	V
Input current			±10	mA
Junction temperature(5)			+150	°C
Soldering information	Infrared or convection reflow (20 s)		235	°C
	Wave soldering lead temperature (10 s)		260	°C
Storage temperature range, T_{stg}		–65	+150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	2000	V
		Machine model (MM)(3)	200	
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(4)	1000	

(1) Human body model, 1.5 kΩ in series with 100 pF. Machine Model, 0 Ω in series with 200 pF.
(2) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.
(4) JEDEC document JEP157 states that 1000-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^–$)	2.7	12.8	V
Operating temperature range(2)	–40	+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

7.4 Thermal Information

THERMAL METRIC(1)		LMH6644-MIL		UNIT
		D14A	PW14A	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	145	155	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

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7.5 3-V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to V^+/2

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, V_{ID} R_L = 2 kΩ to V^+/2			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
BW	–3-dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				80	115		MHz
		A_V = +2, –1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1-dB gain flatness	A_V = +2, R_L = 150Ω to V+/2, Rf = 402Ω, V_{OUT} = 200mV$_{PP}$					19		MHz
PBW	Full power bandwidth	A_V = +1, –1dB, V_{OUT} = 1V$_{PP}$					40		MHz
e_n	Input-referred voltage noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-referred current noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total harmonic distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = –1, R_L = 100Ω to V^+/2					–48		dBc
DG	Differential gain	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to V^+/2					0.17%		
		R_L =1kΩ to V^+/2					0.03%		
DP	Differential phase	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to V^+/2					0.05		deg
		R_L =1kΩ to V^+/2					0.03		
CT Rej.	Cross-talk rejection	f = 5MHz, receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V					68		ns
SR	Slew rate (3)	A_V = –1, V_I = 2V$_{PP}$				90	120		V/µs
V_{OS}	Input offset voltage				±7		±1	±5	mV
TC V_{OS}	Input offset average drift	See (4)					±5		µV/°C
I_B	Input bias current	See (5)			–3.25		–1.50	–2.60	µA
I_{OS}	Input offset current				1000		20	800	nA
R_{IN}	Common-mode input resistance						3		MΩ

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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3-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 3 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to $V^+/2$

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 3 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$, V_{ID} R_L = 2 kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
C_{IN}	Common-mode input capacitance						2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			–0.1		–0.5	–0.2	V
			1.6			1.8	2.0		
CMRR	Common-mode rejection ratio	V_{CM} Stepped from 0V to 1.5V				72	95		dB
A_{VOL}	Large signal voltage gain	V_O = 0.5V to 2.5V R_L = 2kΩ to $V^+/2$	75			80	96		dB
		V_O = 0.5V to 2.5V R_L = 150Ω to $V^+/2$	70			74	82		
V_O	Output swing high	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV				2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV				2.80	2.93		
	Output swing low	R_L = 2kΩ to $V^+/2$, V_{ID} = –200mV					25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = –200mV					75	150	
I_{SC}	Output short circuit current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)	35			50	95		mA
		Sinking to $V^+/2$ V_{ID} = –200mV (6)	40			55	110		
I_{OUT}	Output current	V_{OUT} = 0.5V from either supply					±65		mA
+PSRR	Positive power supply rejection ratio	V^+ = 3.0V to 3.5V, V_{CM} = 1.5V				75	85		dB
I_S	Supply current (per channel)	No load			4.50		2.70	4.00	mA

(6) Short circuit test is a momentary test. See Note 7 under 5-V Electrical Characteristics.

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7.6 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to V^+/2

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, V_{ID} R_L = 2 kΩ to V^+/2			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
BW	–3-dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				90	120		MHz
		A_V = +2, –1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1-dB gain flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 402Ω, V_{OUT} = 200mV$_{PP}$					15		MHz
PBW	Full power bandwidth	A_V = +1, –1dB, V_{OUT} = 2V$_{PP}$					22		MHz
e_n	Input-referred voltage noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-referred current noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total harmonic distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2					–60		dBc
DG	Differential gain	NTSC, A_V = +2 R_L =150Ω to V^+/2					0.16%		
		R_L = 1kΩ to V^+/2					0.05%		
DP	Differential phase	NTSC, A_V = +2 R_L = 150Ω to V^+/2					0.05		deg
		R_L = 1kΩ to V^+/2					0.01		
CT Rej.	Cross-talk rejection	f = 5MHz, receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load					68		ns
SR	Slew rate (3)	A_V = –1, V_I = 2V$_{PP}$				95	125		V/µs
V_{OS}	Input offset voltage				±7		±1	±5	mV
TC V_{OS}	Input offset average drift	See (4)					±5		µV/°C
I_B	Input bias current	See (5)			–3.25		–1.70	–2.60	µA
I_{OS}	Input offset current				1000		20	800	nA
R_{IN}	Common-mode input resistance						3		MΩ
C_{IN}	Common-mode input capacitance						2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			–0.1		–0.5	–0.2	V
			3.6			3.8	4.0		
CMRR	Common-mode rejection ratio	V_{CM} Stepped from 0V to 3.5V				72	95		dB
A_{VOL}	Large signal voltage gain	V_O = 0.5V to 4.50V R_L = 2kΩ to V^+/2	82			86	98		dB
		V_O = 0.5V to 4.25V R_L = 150Ω to V^+/2	72			76	82		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to $V^+/2$

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$, V_{ID} R_L = 2 kΩ to $V^+/2$			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
V_O	Output swing high	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV				4.90	4.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV				4.65	4.90		
	Output swing low	R_L = 2kΩ to $V^+/2$, V_{ID} = –200mV					25	100	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = –200mV					100	150	
I_{SC}	Output short circuit current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)(7)	40			55	115		mA
		Sinking to $V^+/2$ V_{ID} = –200mV (6)(7)	55			70	140		
I_{OUT}	Output current	V_O = 0.5V from either supply					±70		mA
+PSRR	Positive power supply rejection ratio	V^+ = 4.0V to 6V				79	90		dB
I_S	Supply current (per channel)	No load			5.00		2.70	4.25	mA

(6) Short circuit test is a momentary test. See Note 7.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

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7.7 ±5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for V^+ = 5 V, $V^–$ = –5 V, V_{CM} = V_O = 0 V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to ground

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5 V, $V^–$ = –5 V, V_{CM} = V_O = 0 V, V_{ID}			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
BW	–3-dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$				95	130		MHz
		A_V = +2, –1, V_{OUT} = 200mV$_{PP}$					46		
$BW_{0.1dB}$	0.1-dB gain flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 806Ω, V_{OUT} = 200mV$_{PP}$					12		MHz
PBW	Full power bandwidth	A_V = +1, –1dB, V_{OUT} = 2V$_{PP}$					24		MHz
e_n	Input-referred voltage noise	f = 100kHz					17		nV/√Hz
		f = 1kHz					48		
i_n	Input-referred current noise	f = 100kHz					0.90		pA/√Hz
		f = 1kHz					3.3		
THD	Total harmonic distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2					–62		dBc
DG	Differential gain	NTSC, A_V = +2 R_L = 150Ω to V^+/2					0.15%		
		R_L = 1kΩ to V^+/2					0.01%		
DP	Differential phase	NTSC, A_V = +2 R_L = 150Ω to V^+/2					0.04		deg
		R_L = 1kΩ to V^+/2					0.01		
CT Rej.	Cross-talk rejection	f = 5MHz, receiver: R_f = R_g = 510Ω, A_V = +2					47		dB
T_S	Settling time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V					68		ns
SR	Slew rate (3)	A_V = –1, V_I = 2V$_{PP}$				100	135		V/µs
V_{OS}	Input offset voltage				±7		±1	±5	mV
TC V_{OS}	Input offset average drift	See (4)					±5		µV/°C
I_B	Input bias current	See (5)			–3.25		–1.60	–2.60	µA
I_{OS}	Input offset current				1000		20	800	nA
R_{IN}	Common-mode input resistance						3		MΩ
C_{IN}	Common-mode input capacitance						2		pF
CMVR	Input common-mode voltage range	CMRR ≥ 50dB			–5.1		–5.5	–5.2	V
			3.6			3.8	4.0		
CMRR	Common-mode rejection ratio	V_{CM} Stepped from –5V to 3.5V				74	95		dB

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

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±5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for V^+ = 5 V, $V^–$ = –5 V, V_{CM} = V_O = 0 V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2 kΩ to ground

PARAMETER		TEST CONDITIONS	AT TEMPERATURE EXTREMES			V^+ = 5 V, $V^–$ = –5 V, V_{CM} = V_O = 0 V, V_{ID}			UNIT
			MIN	TYP	MAX	MIN(1)	TYP(2)	MAX(1)	
A_{VOL}	Large signal voltage gain	V_O = –4.5V to 4.5V, R_L = 2kΩ	84			88	96		dB
		V_O = –4.0V to 4.0V, R_L = 150Ω	74			78	82		
V_O	Output swing high	R_L = 2kΩ, V_{ID} = 200mV				4.90	4.96		V
		R_L = 150Ω, V_{ID} = 200mV				4.65	4.80		
	Output swing low	R_L = 2kΩ, V_{ID} = –200mV					–4.96	–4.90	V
		R_L = 150Ω, V_{ID} = –200mV					–4.80	–4.65	
I_{SC}	Output short circuit current	Sourcing to ground V_{ID} = 200mV (6)(7)	35			60	115		mA
		Sinking to ground V_{ID} = –200mV (6)(7)	65			85	145		
I_{OUT}	Output current	V_O = 0.5V from either supply				±75			mA
PSRR	Power supply rejection ratio	(V^+, $V^–$) = (4.5V, –4.5V) to (5.5V, –5.5V)				78	90		dB
I_S	Supply current (per channel)	No load			5.50		2.70	4.50	mA

(6) Short circuit test is a momentary test. See (7).
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

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7.8 Typical Performance Characteristics

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

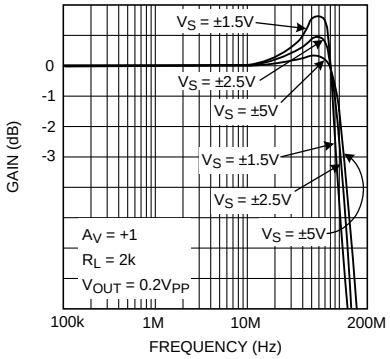

Figure 1. Closed Loop Frequency Response for Various Supplies

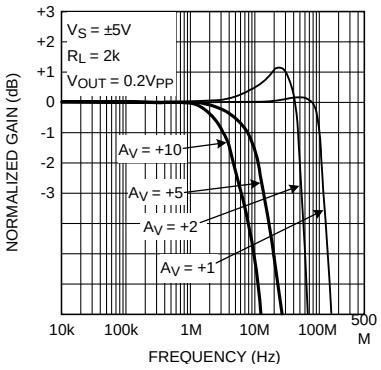

Figure 2. Closed Loop Gain vs Frequency for Various Gain

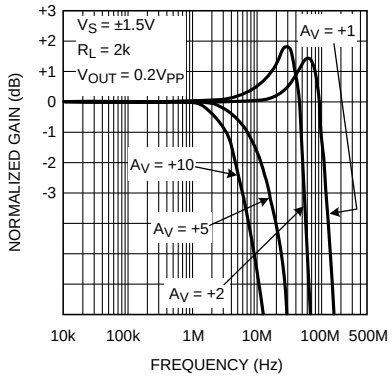

Figure 3. Closed Loop Gain vs Frequency for Various Gain

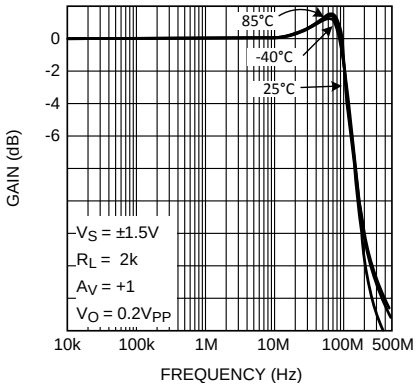

Figure 4. Closed Loop Frequency Response for Various Temperature

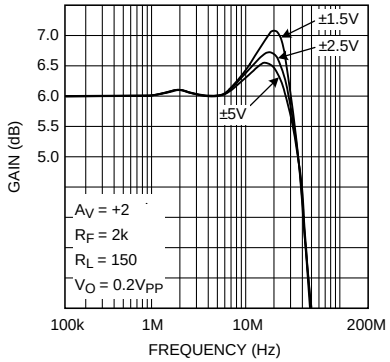

Figure 5. Closed Loop Gain vs Frequency for Various Supplies

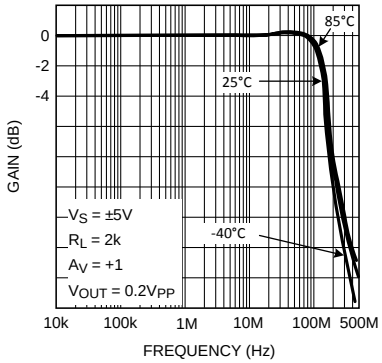

Figure 6. Closed Loop Frequency Response for Various Temperature

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

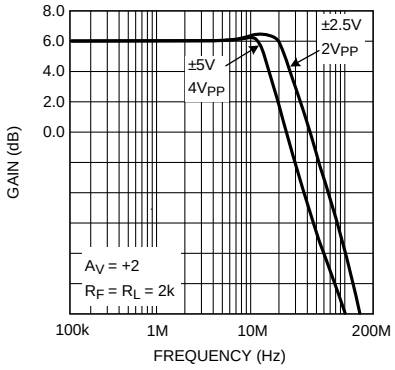

Figure 7. Large Signal Frequency Response

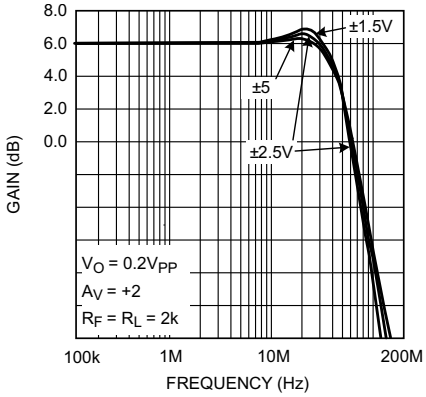

Figure 8. Closed Loop Small Signal Frequency Response for Various Supplies

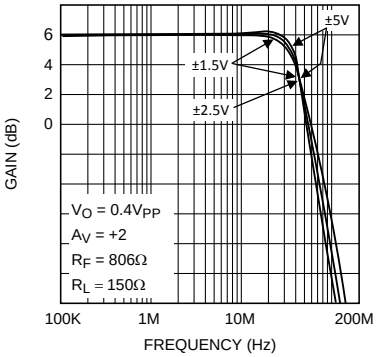

Figure 9. Closed Loop Frequency Response for Various Supplies

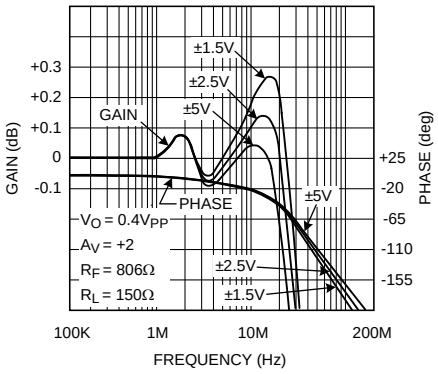

Figure 10. ±0.1dB Gain Flatness for Various Supplies

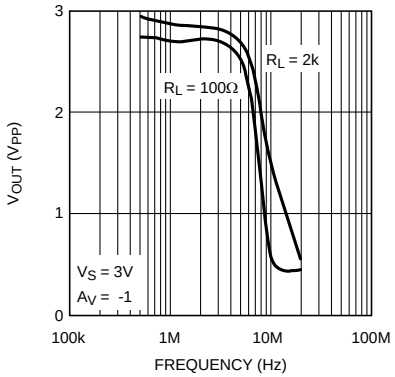

Figure 11. V_{OUT} (V_{PP}) for THD < 0.5%

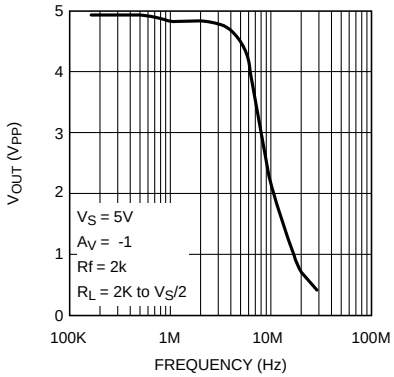

Figure 12. V_{OUT} (V_{PP}) for THD < 0.5%

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

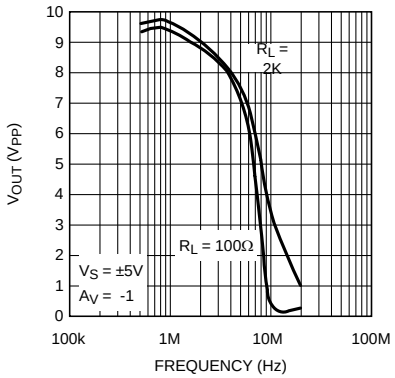

Figure 13. V_{OUT} (V_{PP}) for THD < 0.5%

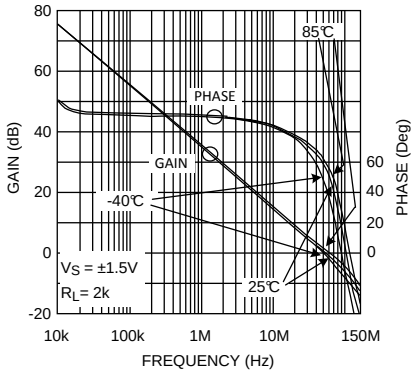

Figure 14. Open Loop Gain/Phase for Various Temperature

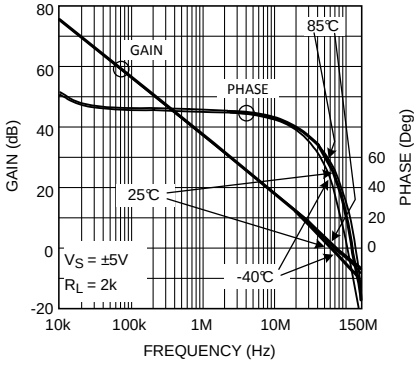

Figure 15. Open Loop Gain/Phase for Various Temperature

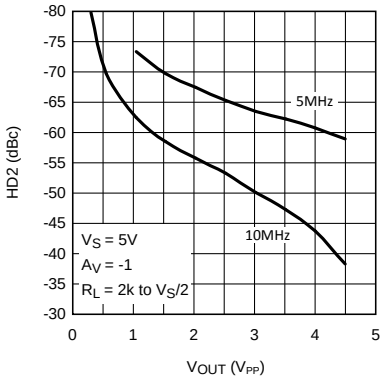

Figure 16. HD2 (dBc) vs Output Swing

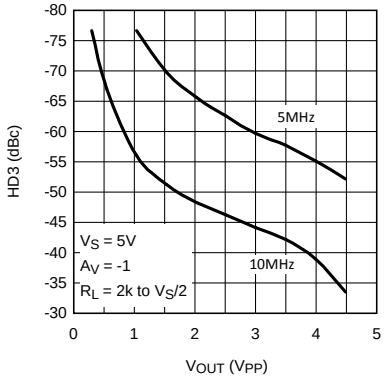

Figure 17. HD3 (dBc) vs Output Swing

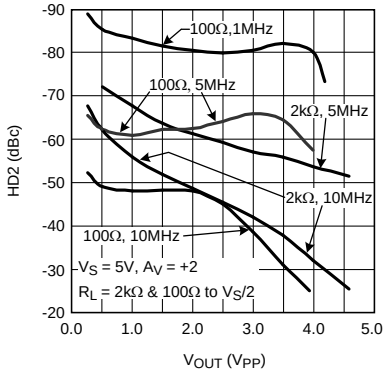

Figure 18. HD2 vs Output Swing

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

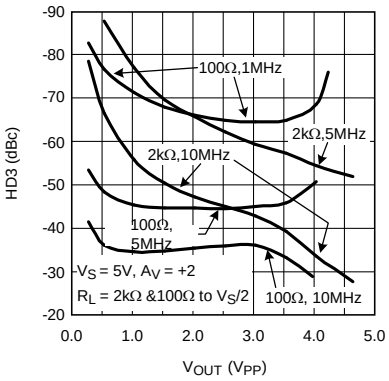

Figure 19. HD3 vs Output Swing

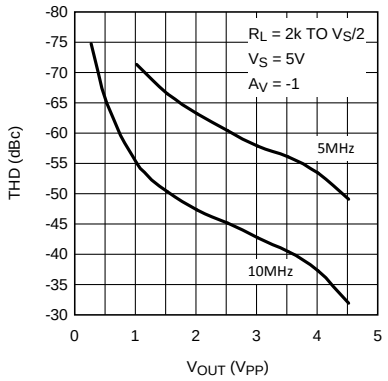

Figure 20. THD (dBc) vs Output Swing

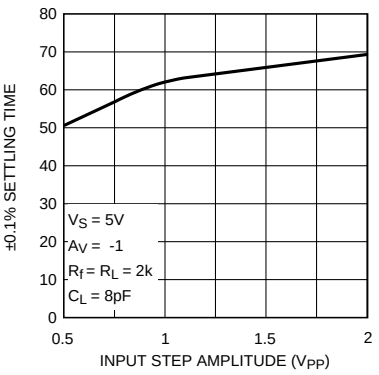

Figure 21. Settling Time vs Input Step Amplitude (Output Slew and Settle Time)

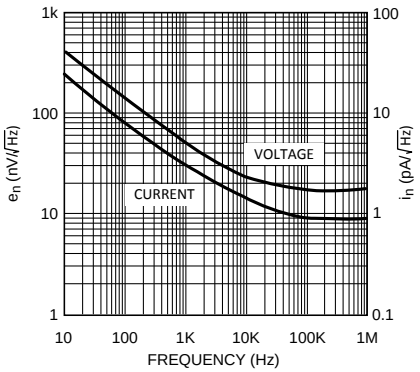

Figure 22. Input Noise vs Frequency

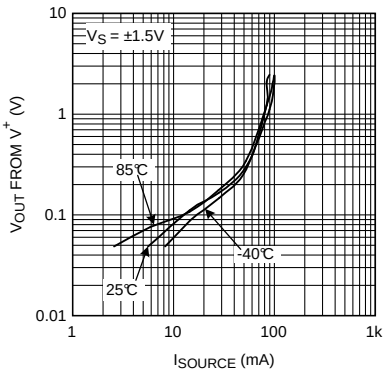

Figure 23. V_{OUT} from V^+ vs I_{SOURCE}

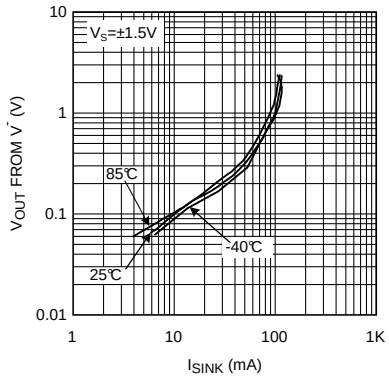

Figure 24. V_{OUT} from V^- vs I_{SINK}

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

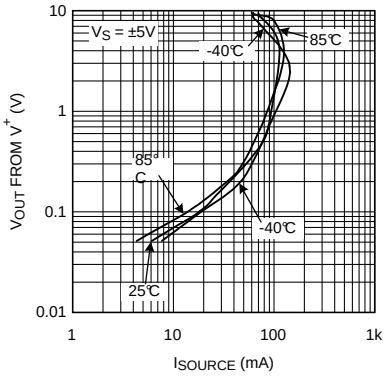

Figure 25. V_{OUT} from V^+ vs I_{SOURCE}

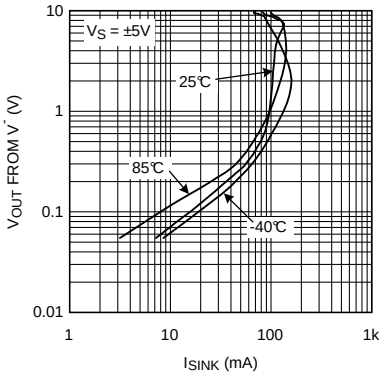

Figure 26. V_{OUT} from V^- vs I_{SINK}

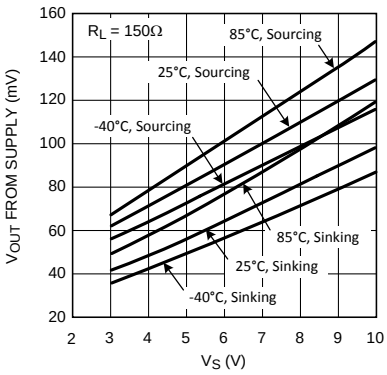

Figure 27. Swing vs V_S

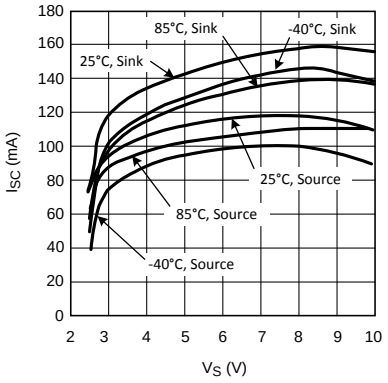

Figure 28. Short Circuit Current (to V_S/2) vs V_S

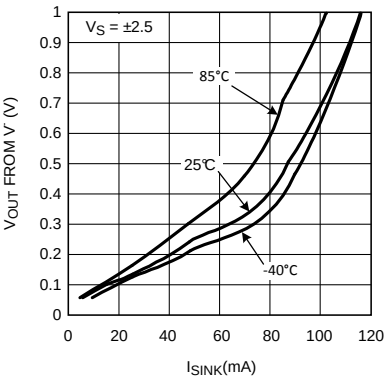

Figure 29. Output Sinking Saturation Voltage vs I_{OUT}

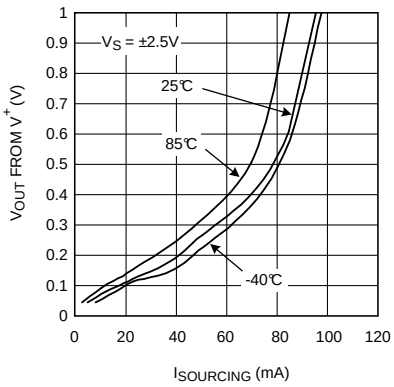

Figure 30. Output Sourcing Saturation Voltage vs I_{OUT}

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

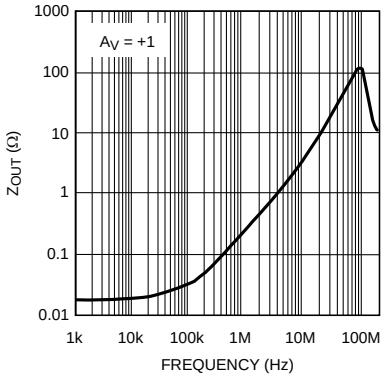

Figure 31. Closed Loop Output Impedance vs Frequency A_V = +1

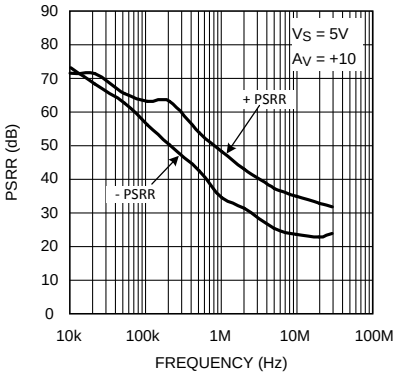

Figure 32. PSRR vs Frequency

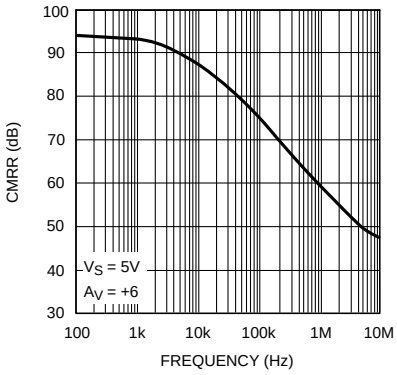

Figure 33. CMRR vs Frequency

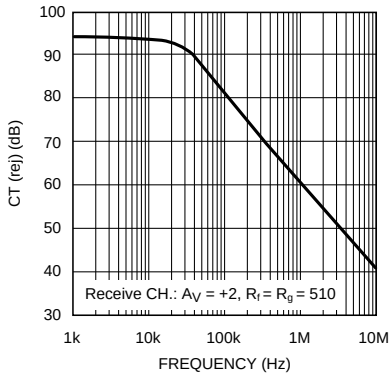

Figure 34. Crosstalk Rejection vs Frequency (Output to Output)

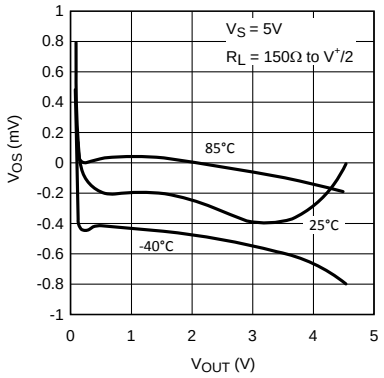

Figure 35. V_{OS} vs V_{OUT} (Typical Unit)

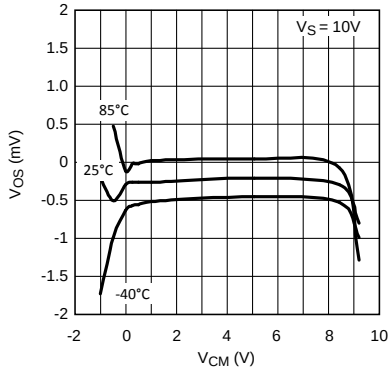

Figure 36. V_{OS} vs V_{CM} (Typical Unit)

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

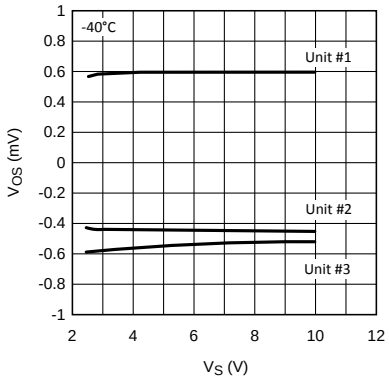

Figure 37. V_{OS} vs V_S (for 3 Representative Units)

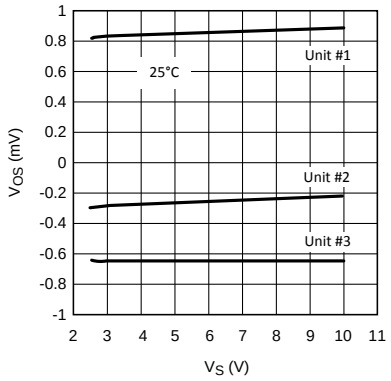

Figure 38. V_{OS} vs V_S (for 3 Representative Units)

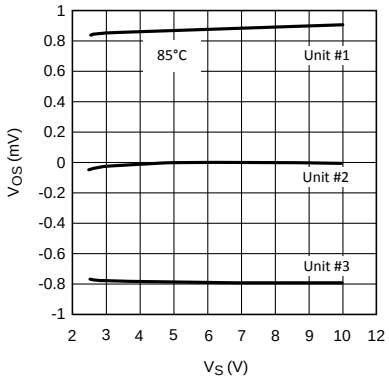

Figure 39. V_{OS} vs V_S (for 3 Representative Units)

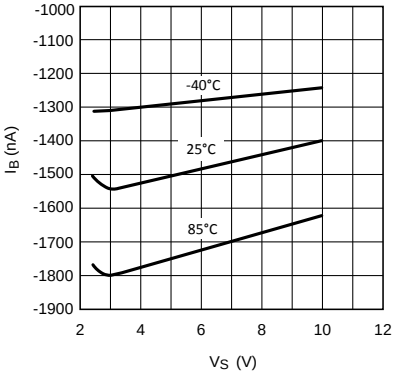

Figure 40. I_B vs V_S

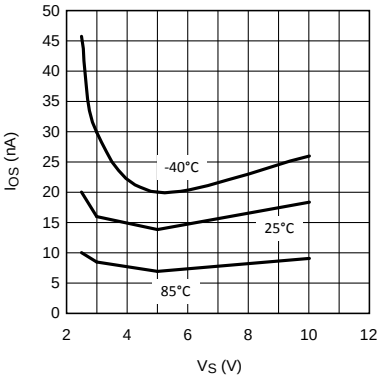

Figure 41. I_{OS} vs V_S

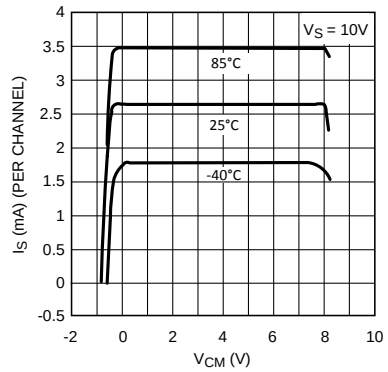

Figure 42. I_S vs V_{CM}

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

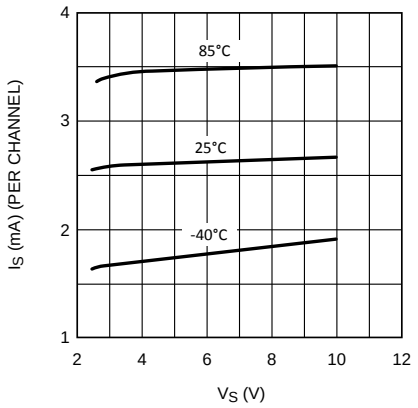

Figure 43. I_S vs V_S

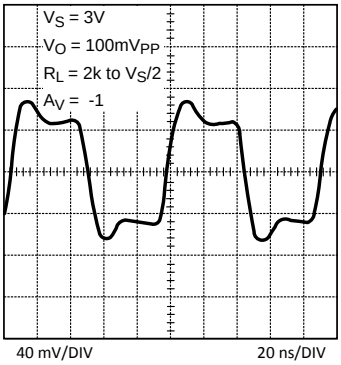

Figure 44. Small Signal Step Response

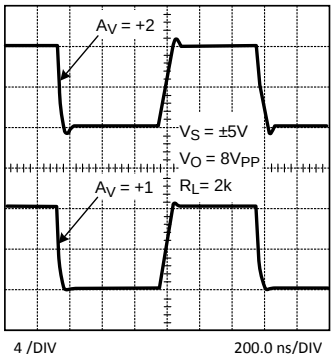

Figure 45. Large Signal Step Response

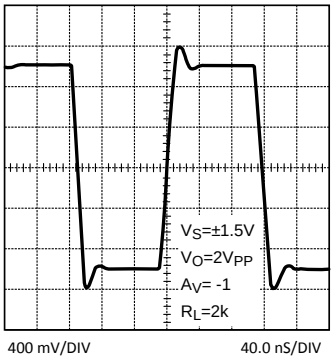

Figure 46. Large Signal Step Response

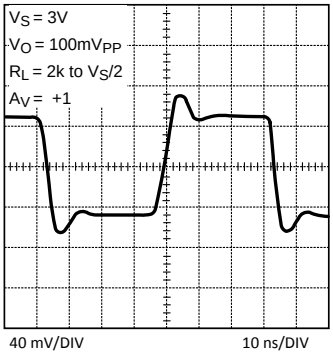

Figure 47. Small Signal Step Response

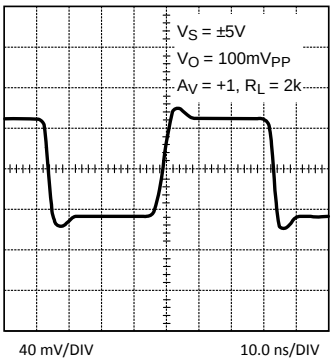

Figure 48. Small Signal Step Response

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Typical Performance Characteristics (continued)

V^+ = +5 V, V^- = –5 V, R_F = R_L = 2 kΩ, unless specified otherwise.

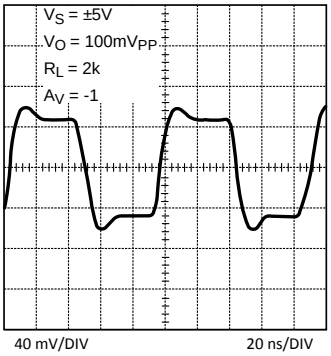

Figure 49. Small Signal Step Response

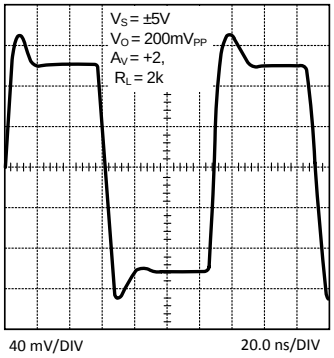

Figure 50. Small Signal Step Response

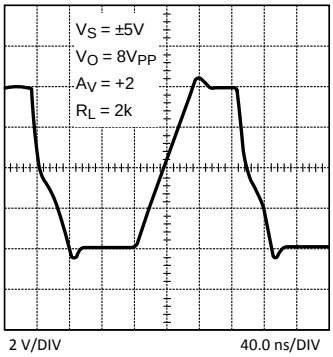

Figure 51. Large Signal Step Response

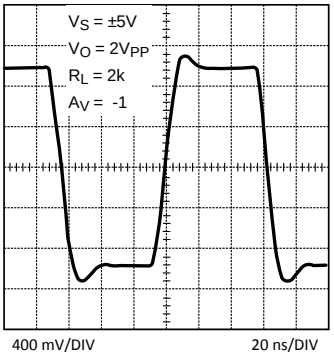

Figure 52. Large Signal Step Response

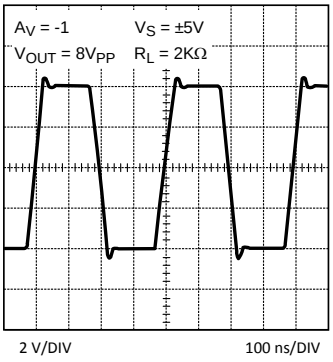

Figure 53. Large Signal Step Response

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8 Detailed Description

8.1 Overview

The LMH6644-MIL is based on proprietary VIP10 dielectrically isolated bipolar process. This device architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low-supply voltage (2.7 V) and low-bias current.
- A class A-B *turn-around* stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75-mA output current (at 0.5 V from the supply rails) while consuming only 2.7 mA of total supply current per channel. This architecture allows output to reach within mV of either supply rail.
- Consistent performance over the entire operating supply voltage range with little variation for the most important specifications (for example, BW, SR, I_{OUT}, and so forth)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

8.2 Functional Block Diagram

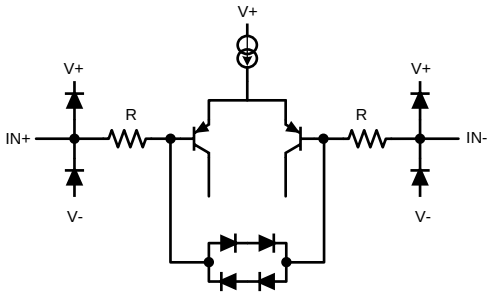

Figure 54. Input Equivalent Circuit

8.3 Feature Description

The LMH6644-MIL is a drop-in replacement for the AD805X family of high-speed op amps in most applications. In addition, the LMH6644-MIL will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's specified parameters are included in the list of LMH6644-MIL ensured specifications in order to ensure equal or better level of performance. However, as in most high-performance parts and due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

8.4 Device Functional Modes

With 3-V supplies and a common-mode input voltage range that extends 0.5 V below V^-, the LMH6644-MIL find applications in low voltage/low power applications. Even with 3-V supplies, the –3dB BW (@ A_V = +1) is typically 115 MHz with a tested limit of 80 MHz. Production testing guarantees that process variations will not compromise speed. High-frequency response is exceptionally stable, confining the typical –3dB BW over the industrial temperature range to ±2.5%.

As seen in *Typical Performance Characteristics*, the LMH6644-MIL output current capability (~75 mA) is enhanced compared to AD805X. This enhancement increases the output load range, adding to the LMH6644-MIL's versatility. Since LMH6644-MIL is capable of high-output current, device junction temperature should not to exceed the Absolute Maximum Ratings.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See Figure 56.

However, if the input voltage range of –0.5 V to 1 V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10 mA.

Output overdrive recovery time is less than 100 ns as can be seen in Figure 57.

9.2 Typical Application

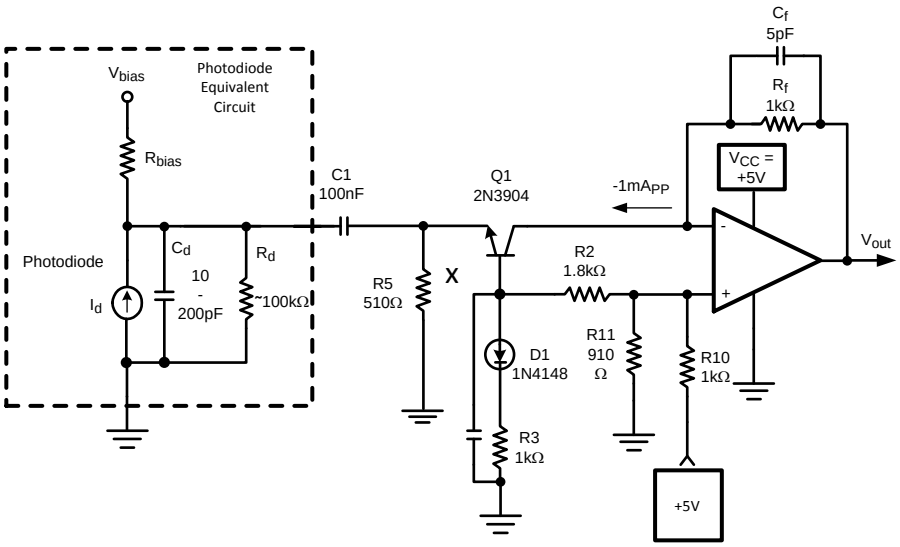

Figure 55. Single-Supply Photodiode I-V Converter

9.2.1 Design Requirements

The circuit shown in Figure 55 is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high-slew-rate limit and high speed, the LMH6644-MIL lends itself well to such an application. This circuit achieves approximately 1 V/mA of transimpedance gain and capable of handling up to 1 mApp from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (Cd) from the op amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5-V single supply, the device input/output is shifted to near half supply using a voltage divider from VCC. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

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Typical Application (continued)

9.2.1.1 Input and Output Topology

All input / output pins are protected against excessive voltages by ESD diodes connected to V^+ and V^- rails (see Figure 54). These diodes start conducting when the input / output pin voltage approaches 1 V_{be} beyond V^+ or V^- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in Figure 54), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching 2 V_{be}. This occurs most commonly when the device is used as a comparator (or with little or no feedback) and the device inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases and the differential input voltage is clamped. It is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through this protection circuit, extra series resistors can be placed. Together with the built-in series resistors of several hundred ohms, these external resistors can limit the input current to a safe number (that is, less than 10 mA). Be aware that these input series resistors may impact the switching speed of the device and could slow down the device.

9.2.1.2 Single-Supply, Low-Power Photodiode Amplifier

The circuit shown in Figure 55 is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH6644-MIL lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single-supply operation. With 5-V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counter-acting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT}\left[(C_{IN})/(2\pi \cdot \text{GBWP} \cdot R_F)\right] \quad (1)$$

where

- GBWP is the Gain Bandwidth Product of the Op Amp

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_P = \text{SQRT}\left[\text{GBWP}/(2\pi R_F \cdot C_{IN})\right] \quad (2)$$

With op amp input capacitance of 3 pF and an estimate for Q1 output capacitance of about 3 pF as well, C_{IN} = 6 pF. From the typical performance plots, GBWP is approximately 57 MHz. Therefore, with R_f = 1k, from Equation 1 and Equation 2:

$$C_f = \sim 4.1 \text{ pF and } f_p = 39 \text{ MHz} \quad (3)$$

For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in Figure 58 below showing about 9-ns rise/fall times, corresponding to about 39 MHz for f_p. The overall supply current from the +5 V supply is around 5 mA with no load.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

No matter how low an Rf is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the op amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin where GBWP is the Gain Bandwidth Product of the Op Amp, optimized as such, the I-V converter will have a theoretical pole, fp, at: (2) With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3 pF as well, C_{IN} = 6 pF. From the typical performance plots, GBWP is approximately 57 MHz. Therefore, with Rf = 1k, from Equation 2 and Equation 3 : C_f = ~4.1 pF and fp = 39 MHz.

For this example, optimum C_f was empirically determined to be around 5 pF. This time domain response is shown in Figure 58 showing about 9 ns rise/fall times, corresponding to about 39 MHz for fp. The overall supply current from the +5-V supply is around 5 mA with no load.

9.2.3 Application Curves

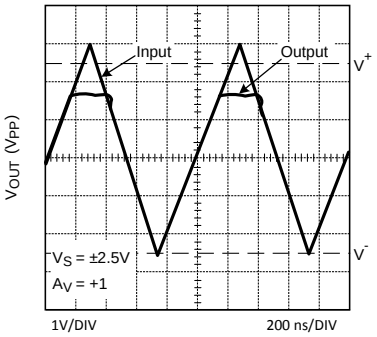

Figure 56. Input and Output Shown with CMVR Exceeded

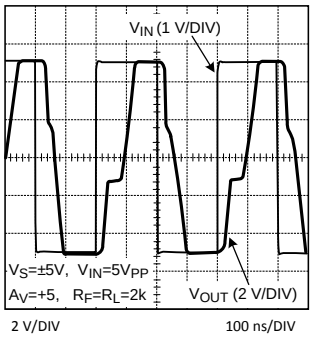

Figure 57. Overload Recovery Waveform

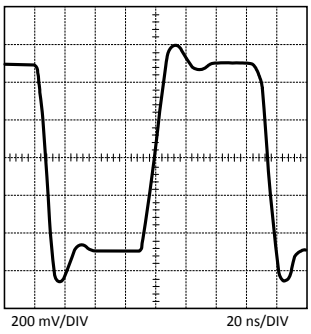

Figure 58. Converter Step Response (1 V_{PP}, 20 ns/DIV)

10 Power Supply Recommendations

The LMH6644-MIL device can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends all the way down to the V– rail to simplify single supply applications. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

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11 Layout

11.1 Layout Guidelines

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers", SNOA367, for more information). Texas Instruments suggests the following evaluation boards as a guide for high-frequency layout and as an aid in device testing and characterization:

Table 1. Printed Circuit Board Layout And Component Values

DEVICE	PACKAGE	EVALUATION BOARD PN
LMH6644MA	14-Pin SOIC	LMH730231
LMH6644MT	14-Pin TSSOP	LMH730131

Another important parameter in working with high-speed and high-performance amplifiers is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

11.2 Layout Example

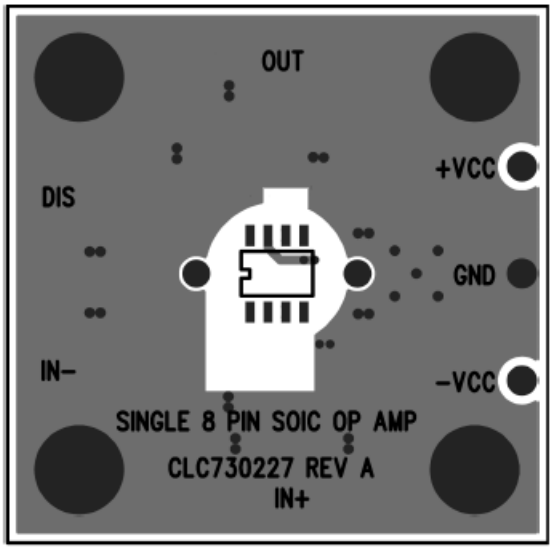

Figure 59. LMH6644-MIL Layer 1

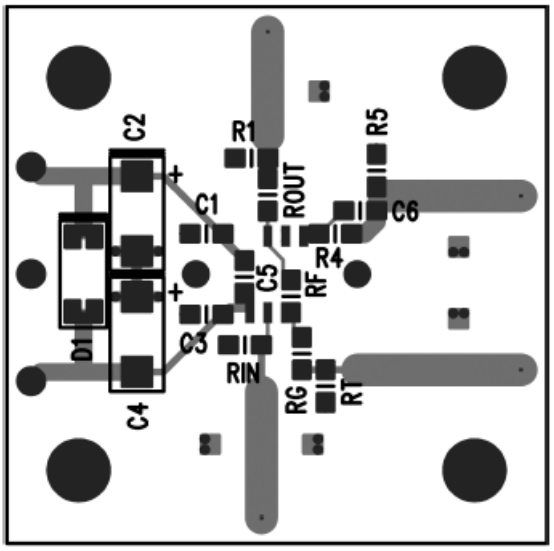

Figure 60. LMH6644-MIL Layer 2

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6644 MDC	Active	Production	DIESALE (Y) | 0	100 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	
LMH6644-MDC.A	Active	Production	DIESALE (Y) | 0	100 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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