

LMK04100 Family Clock Jitter Cleaner with Cascaded PLLs

 Check for Samples: [LMK04100](#), [LMK04101](#), [LMK04102](#), [LMK04110](#), [LMK04111](#), [LMK04131](#), [LMK04133](#)

FEATURES

- **Cascaded PLLatinum™ PLL Architecture**
 - PLL1
 - Redundant Reference Inputs
 - Loss of Signal Detection
 - Automatic and Manual Selection of Reference Clock Input
 - PLL2
 - Phase Detector Rate up to 100 MHz
 - Input Frequency-Doubler
 - Integrated VCO
- **Outputs**
 - LVPECL/2VPECL, LVDS, and LVC MOS Formats
 - Support Clock Rates up to 1080 MHz
 - Five Dedicated Channel Divider Blocks
 - Common Output Frequencies Supported:
 - 30.72 MHz, 61.44 MHz, 62.5 MHz, 74.25 MHz, 75 MHz, 77.76 MHz, 100 MHz, 106.25 MHz, 125 MHz, 122.88 MHz, 150 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 187.5 MHz, 200 MHz, 212.5 MHz, 245.76 MHz, 250 MHz, 311.04 MHz, 312.5 MHz, 368.64 MHz, 491.52 MHz, 622.08 MHz, 625 MHz, 983.04 MHz
- **MICROWIRE (SPI) Programming Interface**

- **Industrial Temperature Range: -40 to 85 °C**
- **3.15 V to 3.45 V Operation**
- **Package: 48 Pin WQFN (7.0 x 7.0 x 0.8 mm)**

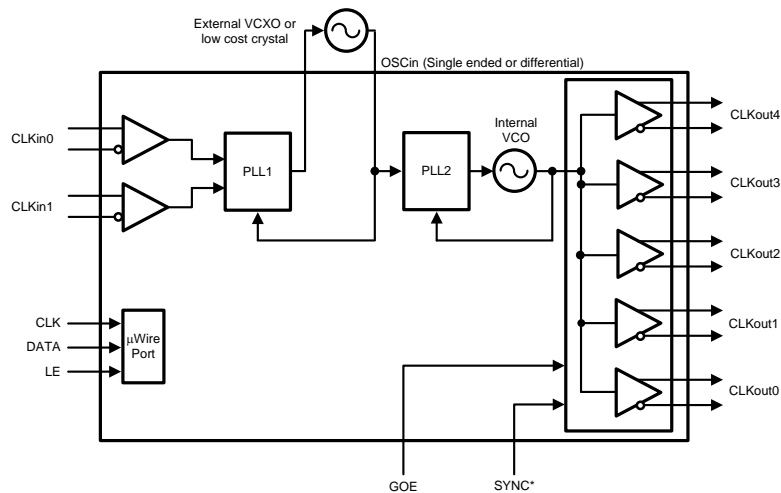
APPLICATIONS

- **Multi-Carrier/Multi-Mode/Multi-Band 2G/3G/4G Basestations**
- **Cellular Repeaters**
- **High Speed A/D clocking**
- **SONET/SDH OC-48/OC-192/OC-768 Line Cards**
- **GbE/10GbE, 1/2/4/8/10G Fibre Channel Line Cards**
- **Optical Transport Networks**
- **Broadcast Video, HDTV**
- **Serial ATA**

DESCRIPTION

The LMK04100 family of precision clock conditioners provides jitter cleaning, clock multiplication and distribution without the need for high-performance VCXO modules.

When connected to a recovered system reference clock and a VCXO, the device generates 5 low jitter clocks in LVC MOS, LVDS, or LVPECL formats.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PLLatinum is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

Table 1. Device Configuration Information

| NSID | 2VPECL / LVPECL OUTPUTS | LVDS OUTPUTS | LVC MOS OUTPUTS | VCO |
|------------|-------------------------|--------------|-----------------|------------------|
| LMK04100SQ | 3 | | 4 | 1185 to 1296 MHz |
| LMK04101SQ | 3 | | 4 | 1430 to 1570 MHz |
| LMK04102SQ | 3 | | 4 | 1600 to 1750 MHz |
| LMK04110SQ | 5 | | | 1185 to 1296 MHz |
| LMK04111SQ | 5 | | | 1430 to 1570 MHz |
| LMK04131SQ | 2 | 2 | 2 | 1430 to 1570 MHz |
| LMK04133SQ | 2 | 2 | 2 | 1840 to 2160 MHz |

Table 2. Device Output Format Information

| NSID | CLKout0 | CLKout1 | CLKout2 | CLKout3 | CLKout4 |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| LMK04100SQ | 2VPECL / LVPECL | LVC MOS x 2 | LVC MOS x 2 | 2VPECL / LVPECL | 2VPECL / LVPECL |
| LMK04101SQ | 2VPECL / LVPECL | LVC MOS x 2 | LVC MOS x 2 | 2VPECL / LVPECL | 2VPECL / LVPECL |
| LMK04102SQ | 2VPECL / LVPECL | LVC MOS x 2 | LVC MOS x 2 | 2VPECL / LVPECL | 2VPECL / LVPECL |
| LMK04110SQ | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL |
| LMK04111SQ | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL | 2VPECL / LVPECL |
| LMK04131SQ | LVDS | 2VPECL / LVPECL | LVC MOS x 2 | 2VPECL / LVPECL | LVDS |
| LMK04133SQ | LVDS | 2VPECL / LVPECL | LVC MOS x 2 | 2VPECL / LVPECL | LVDS |

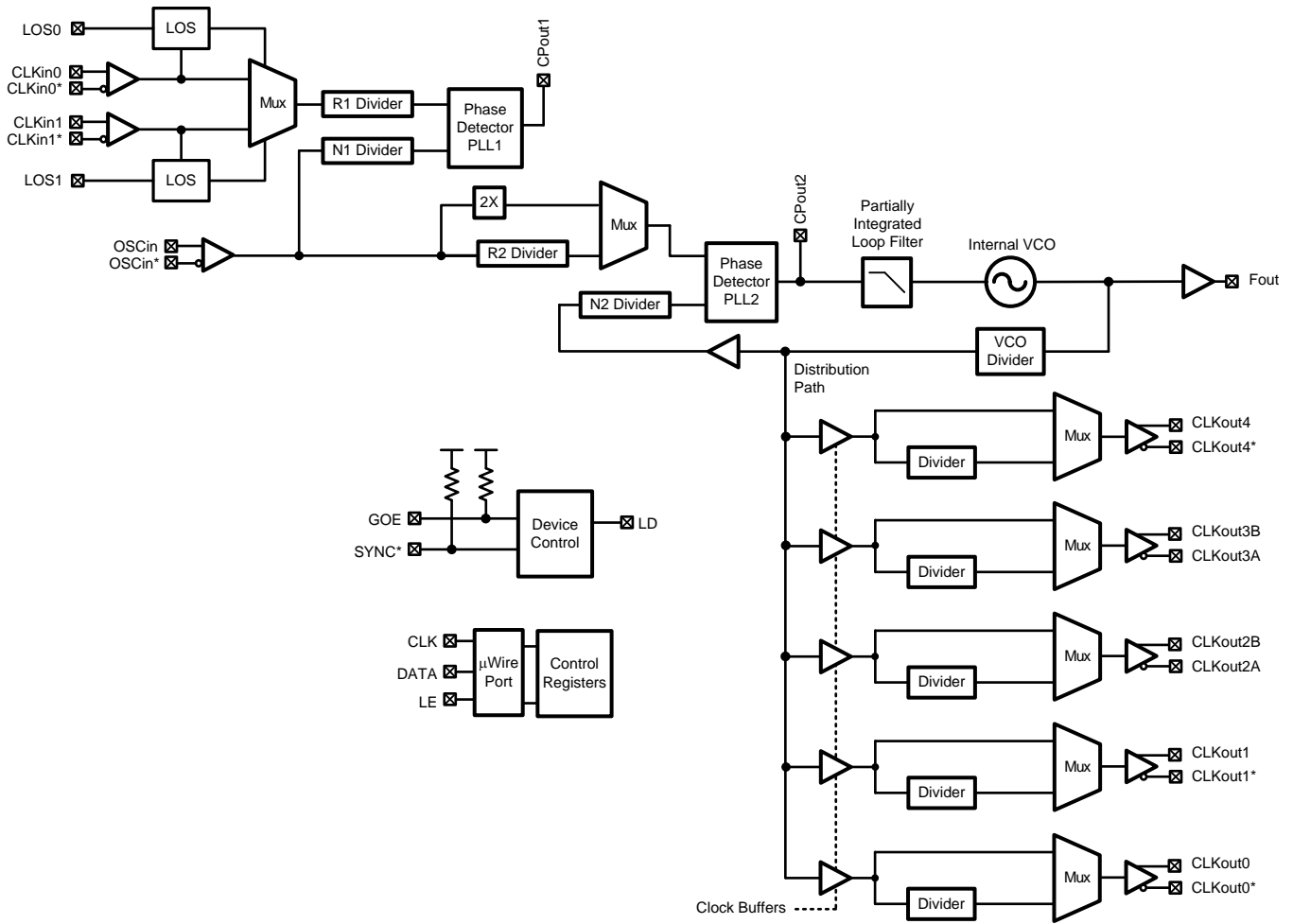
Table 3 shows a limited list of example frequencies. Multiple output frequencies can be programmed on a single device provided that the VCO frequency and VCO divider values are the same.

Table 3. Example Configurations for Common Frequencies

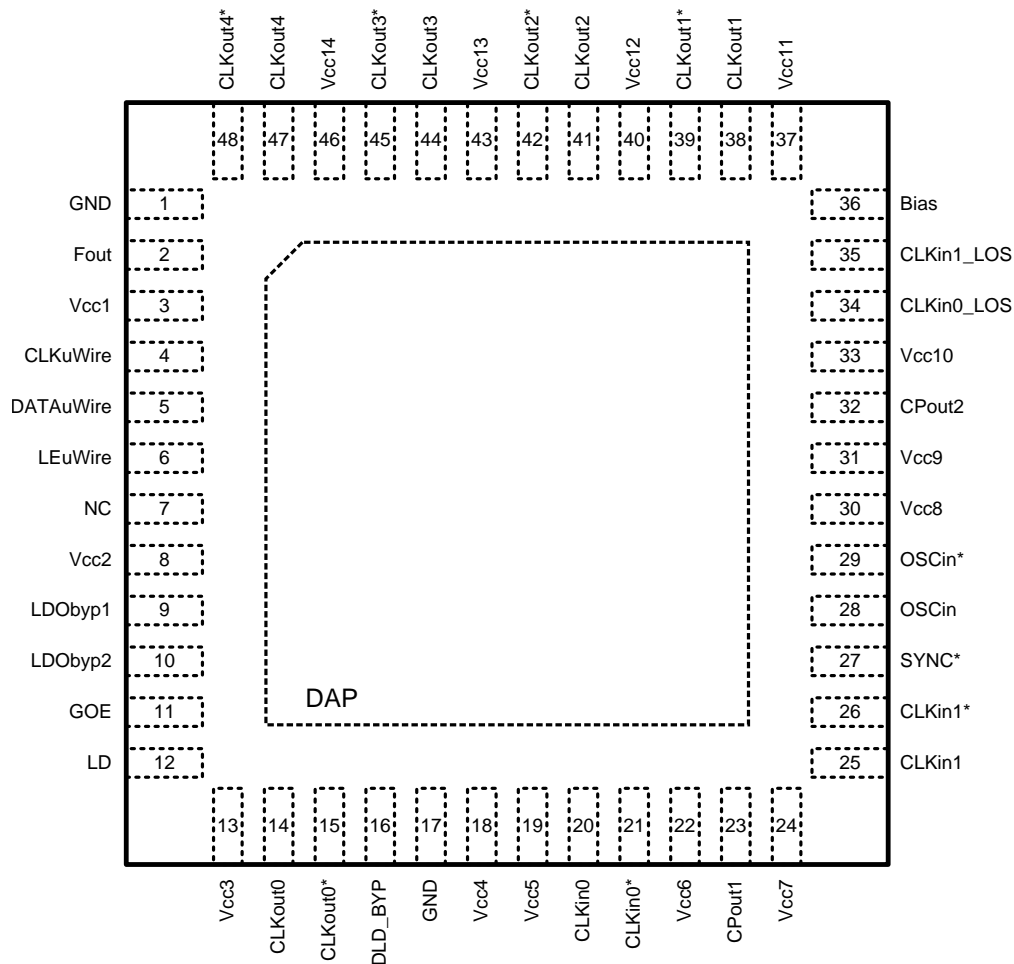
| OSCI _n (MHz) | VCO Divider | PLL2 N | VCO Frequency ⁽¹⁾ | Output Divider | Output Frequency | Application |
|-------------------------|-------------|--------|------------------------------|----------------|------------------|--------------------|
| 25 | 2 | 30 | 1500 | 12 | 62.5 | GigE |
| 25 | 2 | 30 | 1500 | 10 | 75 | SATA |
| 24.8832 | 2 | 25 | 1244.16 | 8 | 77.76 | SONET |
| 25 | 2 | 24 | 1200 | 6 | 100 | PCI Express |
| 26.5625 | 7 | 8 | 1487.5 | 2 | 106.25 | Fibre Channel |
| 25 | 2 | 30 | 1500 | 6 | 125 | GigE |
| 25 | 5 | 12 | 1500 | 2 | 150 | SATA |
| 24.8832 | 2 | 25 | 1244.16 | 4 | 155.52 | SONET |
| 25 | 2 | 25 | 1250 | 4 | 156.25 | 10 GigE |
| 26.5625 | 2 | 25 | 1275 | 4 | 159.375 | 10-G Fibre Channel |
| 25 | 2 | 25 | 1500 | 4 | 187.5 | 12 GigE |
| 25 | 3 | 16 | 1200 | 2 | 200 | PCI Express |
| 26.5625 | 3 | 16 | 1275 | 2 | 212.5 | 4-G Fibre Channel |
| 25 | 3 | 20 | 1500 | 2 | 250 | GigE |
| 24.8832 | 2 | 25 | 1244.16 | 2 | 311.04 | SONET |
| 25 | 2 | 25 | 1250 | 2 | 312.5 | XGMII |
| 24.8832 | 2 | 25 | 1244.16 | 1 | 622.08 | SONET |
| 25 | 2 | 25 | 1200 | 1 | 625 | 10 GigE |

(1) Use VCO Frequency to select proper device option

Functional Block Diagram



Connection Diagram



**Figure 1. 48-Pin WQFN Package
Top Down View**

PIN DESCRIPTIONS

| Pin Number | Name(s) | I/O | Type | Description |
|------------|------------------|-----|-------------|---|
| 1 | GND | | GND | Ground (For Fout Buffer) |
| 2 | Fout | O | ANLG | VCO Frequency Output Port |
| 3 | V _{CC1} | | PWR | Power Supply for VCO Output Buffer |
| 4 | CLKuWire | I | CMOS | Microwire Clock Input |
| 5 | DATAuWire | I | CMOS | Microwire Data Input |
| 6 | LEuWire | I | CMOS | Microwire Latch Enable Input |
| 7 | NC | | | No Connection |
| 8 | V _{CC2} | | PWR | Power Supply for VCO |
| 9 | LDObyp1 | | ANLG | LDO Bypass, bypassed to ground with a 10 μ F capacitor |
| 10 | LDObyp2 | | ANLG | LDO Bypass, bypassed to ground with a 0.1 μ F capacitor |
| 11 | GOE | I | CMOS | Global Output Enable |
| 12 | LD | O | CMOS | Lock Detect and PLL multiplexer Output |
| 13 | V _{CC3} | | PWR | Power Supply for CLKout0 |
| 14 | CLKout0 | O | LVDS/LVPECL | Clock Channel 0 Output |

PIN DESCRIPTIONS (continued)

| Pin Number | Name(s) | I/O | Type | Description |
|------------|-------------------|-----|----------------|---|
| 15 | CLKout0* | O | LVDS/LVPECL | Clock Channel 0* Output |
| 16 | DLD_BYP | | ANLG | DLD Bypass, bypassed to ground with a 0.47 μ F capacitor |
| 17 | GND | | GND | Ground (Digital) |
| 18 | V _{CC4} | | PWR | Power Supply for Digital |
| 19 | V _{CC5} | | PWR | Power Supply for CLKin buffers and PLL1 R-divider |
| 20 | CLKin0 | I | ANLG | Reference Clock Input Port for PLL1 - AC or DC Coupled ⁽¹⁾ |
| 21 | CLKin0* | I | ANLG | Reference Clock Input Port for PLL1 (complimentary) - AC or DC Coupled ⁽¹⁾ |
| 22 | V _{CC6} | | PWR | Power Supply for PLL1 Phase Detector and Charge Pump |
| 23 | CPout1 | O | ANLG | Charge Pump1 Output |
| 24 | V _{CC7} | | PWR | Power Supply for PLL1 N-Divider |
| 25 | CLKin1 | I | ANLG | Reference Clock Input Port for PLL1 - AC or DC Coupled ⁽¹⁾ |
| 26 | CLKin1* | I | ANLG | Reference Clock Input Port for PLL1 (complimentary) - AC or DC Coupled ⁽²⁾ |
| 27 | SYNC* | I | CMOS | Global Clock Output Synchronization |
| 28 | OSCIin | I | ANLG | Reference oscillator Input for PLL2 - AC Coupled |
| 29 | OSCIin* | I | ANLG | Reference oscillator Input for PLL2 - AC Coupled |
| 30 | V _{CC8} | | PWR | Power Supply for OSCIin Buffer and PLL2 R-Divider |
| 31 | V _{CC9} | | PWR | Power Supply for PLL2 Phase Detector and Charge Pump |
| 32 | CPout2 | O | ANLG | Charge Pump2 Output |
| 33 | V _{CC10} | | PWR | Power Supply for VCO Divider and PLL2 N-Divider |
| 34 | CLKin0_LOS | O | LVC MOS | Status of CLKin0 reference clock input |
| 35 | CLKin1_LOS | O | LVC MOS | Status of CLKin1 reference clock input |
| 36 | Bias | I | ANLG | Bias Bypass. AC coupled with 1 μ F capacitor to Vcc1 |
| 37 | V _{CC11} | | PWR | Power Supply for CLKout1 |
| 38 | CLKout1 | O | LVPECL/LVC MOS | Clock Channel 1 Output |
| 39 | CLKout1* | O | LVPECL/LVC MOS | Clock Channel 1* Output |
| 40 | V _{CC12} | | PWR | Power Supply for CLKout2 |
| 41 | CLKout2 | O | LVPECL/LVC MOS | Clock Channel 2 Output |
| 42 | CLKout2* | O | LVPECL/LVC MOS | Clock Channel 2* Output |
| 43 | V _{CC13} | | PWR | Power Supply for CLKout3 |
| 44 | CLKout3 | O | LVPECL | Clock Channel 3 Output |
| 45 | CLKout3* | O | LVPECL | Clock Channel 3* Output |
| 46 | V _{CC14} | | PWR | Power Supply for CLKout4 |
| 47 | CLKout4 | O | LVDS/LVPECL | Clock Channel 4 Output |
| 48 | CLKout4* | O | LVDS/LVPECL | Clock Channel 4* Output |
| DAP | DAP | | | DIE ATTACH PAD, connect to GND |

(1) The reference clock inputs may be either AC or DC coupled.

(2) The reference clock inputs may be either AC or DC coupled.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| Parameter | Symbol | Ratings | Units |
|--|-----------|----------------------------|-------|
| Supply Voltage ⁽⁵⁾ | V_{CC} | -0.3 to 3.6 | V |
| Input Voltage | V_{IN} | -0.3 to ($V_{CC} + 0.3$) | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |
| Lead Temperature (solder 4 sec) | T_L | +260 | °C |
| Junction Temperature | T_J | 125 | °C |
| Differential Input Current (CLKinX/X*, OSCin/OSCin*) | I_{IN} | ± 5 | mA |

- "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.
- This device is a high performance RF integrated circuit with an ESD rating up to 8 KV Human Body Model, up to 300 V Machine Model and up to 1,250 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.
- Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.
- If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- Never to exceed 3.6 V.

Package Thermal Resistance

| Package | θ_{JA} | θ_{J-PAD} (Thermal Pad) |
|-----------------------------|---------------|--------------------------------|
| 48-Lead WQFN ⁽¹⁾ | 27.4° C/W | 5.8° C/W |

- Specification assumes 16 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the WQFN. It is recommended that the maximum number of vias be used in the board layout.

Recommended Operating Conditions

| Parameter | Symbol | Condition | Min | Typical | Max | Unit |
|---------------------|----------|------------------|------|---------|------|------|
| Ambient Temperature | T_A | $V_{CC} = 3.3$ V | -40 | 25 | 85 | °C |
| Supply Voltage | V_{CC} | | 3.15 | 3.3 | 3.45 | V |

Electrical Characteristics

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at $V_{CC} = 3.3$ V, $T_A = 25$ °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------|---|---|-----|-----|-----|-------|
| Current Consumption | | | | | | |
| I_{CC_PD} | Power Down Supply Current | | | 0.7 | | mA |
| I_{CC_CLKS} | Supply Current with all clocks enabled, Fout disabled. ⁽¹⁾ | LMK04100, LMK04101, LMK04102 ⁽²⁾ | | 380 | 435 | mA |
| | | LMK04110, LMK04111 ⁽²⁾ | | 378 | 435 | |
| | | LMK04131, LMK04133 ⁽²⁾ | | 335 | 385 | |

- Load conditions for output clocks: LVPECL: 50 Ω to $V_{CC}-2$ V. 2VPECL: 50 Ω to $V_{CC}-2.36$ V. LVDS: 100 Ω differential. LVCMOS: 10 pF.
- Additional test conditions for I_{CC} limits: CLKoutX_DIV = 510, PLL1 and PLL2 locked. (See [Table 34](#) for more information)

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|--|------|-----------------|-----------------|
| CLKin0/0* and CLKin1/1* Input Clock Specifications | | | | | | |
| f _{CLKin} | Clock Input Frequency (3) | Manual Select mode | 0.001 | | 400 | MHz |
| | | Auto-Switching mode | 1 | | 400 | |
| SLEW _{CLKin} | Slew Rate on CLKin (4) | 20% to 80% | 0.15 | 0.5 | | V/ns |
| V _{ID} CLKin | Clock Input Differential Input Voltage (5) | Each pin AC coupled CLKinX_TYPE=0 (Bipolar) | 0.25 | | 1.55 | V |
| V _{SS} CLKin | | CLKinX and CLKinX* are both driven, AC coupled. CLKinX_TYPE=0 (Bipolar) | 0.5 | | 3.1 | V _{pp} |
| V _{ID} CLKin | | CLKinX and CLKinX* are both driven, AC coupled. CLKinX_TYPE=1 (MOS) | 0.25 | | 1.55 | V |
| V _{SS} CLKin | | | 0.5 | | 3.1 | V _{pp} |
| V _{CLKin} | | Input Voltage Swing, single-ended | AC coupled to CLKinX; CLKinX* AC coupled to Ground CLKinX_TYPE=0 (Bipolar) | 0.25 | | 2.0 |
| | AC coupled to CLKinX; CLKinX* AC coupled to Ground CLKinX_TYPE=1 (MOS) | | 0.25 | | 2.0 | V _{pp} |
| V _{CLKin-offset} | DC offset voltage between CLKinX/CLKinX* CLKinX-CLKinX* | Each pin AC coupled CLKinX_TYPE=0 (Bipolar) | | 44 | | mV |
| | | Each pin AC coupled CLKinX_TYPE=1 (MOS) | | 294 | | mV |
| V _{CLKin-VIH} | High Input Voltage | DC coupled to CLKinX; CLKinX* AC coupled to Ground CLKinX_TYPE=1 (MOS) | 2.0 | | V _{CC} | V |
| V _{CLKin-VIL} | Low Input Voltage | DC coupled to CLKinX; CLKinX* AC coupled to Ground CLKinX_TYPE=1 (MOS) | 0.0 | | 0.4 | V |

(3) CLKin0 and CLKin1 maximum of 400 MHz is guaranteed by characterization, production tested at 200 MHz.

(4) In order to meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.

(5) See [Differential Voltage Measurement Terminology](#) for definition of V_{ID} and V_{OD} voltages.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|--|---|------|------|------|-----------------|
| PLL1 Specifications | | | | | | |
| f _{PD} | PLL1 Phase Detector Frequency | | | | 40 | MHz |
| I _{CPout1} SOURCE | PLL1 Charge Pump Source Current ⁽⁶⁾ | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 100b | | 25 | | μA |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 101b | | 50 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 110b | | 100 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 111b | | 400 | | |
| | | PLL1_CP_GAIN = 000b | | NA | | |
| | | PLL1_CP_GAIN = 001b | | NA | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 010b | | 20 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 011b | | 80 | | |
| I _{CPout1} SINK | PLL1 Charge Pump Sink Current ⁽⁶⁾ | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 100b | | -25 | | μA |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 101b | | -50 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 110b | | -100 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 111b | | -400 | | |
| | | PLL1_CP_GAIN = 000b | | NA | | |
| | | PLL1_CP_GAIN = 001b | | NA | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 010b | | -20 | | |
| | | V _{CPout1} = V _{CC} /2, PLL1_CP_GAIN = 011b | | -80 | | |
| I _{CPout1} %MIS | Charge Pump Sink / Source Mismatch | V _{CPout1} = V _{CC} /2, T = 25 °C | | 3 | 10 | % |
| I _{CPout1} V _{TUNE} | Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation | 0.5 V < V _{CPout1} < V _{CC} - 0.5 V T _A = 25 °C | | 4 | | % |
| I _{CPout1} %TEMP | Charge Pump Current vs. Temperature Variation | | | 4 | | % |
| PLL1 I _{CPout1} TRI | Charge Pump TRI-STATE Leakage Current | 0.5 V < V _{CPout} < V _{CC} - 0.5 V | | | 5 | nA |
| PLL2 Reference Input (OSCin) Specifications | | | | | | |
| f _{OSCin} | PLL2 Reference Input ⁽⁷⁾ | EN_PLL2_REF 2X = 0 ⁽⁸⁾ | | | 250 | MHz |
| | | EN_PLL2_REF 2X = 1 | | | 50 | |
| SLEW _{OSCin} | PLL2 Reference Clock minimum slew rate on OSCin | 20% to 80% | 0.15 | 0.5 | | V/ns |
| V _{ID} OSCin | Differential voltage swing ⁽⁹⁾ | AC coupled | 0.2 | | 1.55 | V |
| V _{SS} OSCin | | | 0.4 | | 3.1 | V _{pp} |
| V _{OSCin} | Single-ended Input Voltage for OSCin or OSCin* | AC coupled; Unused pin AC coupled to GND | 0.2 | | 2.0 | V _{pp} |

(6) This parameter is programmable

(7) f_{OSCin} maximum frequency guaranteed by characterization. Production tested at 200 MHz.

(8) The EN_PLL2_REF2X bit (Register 13) enables/disables a frequency doubler mode for the PLL2 OSCin path.

(9) See [Differential Voltage Measurement Terminology](#) for definition of V_{ID} and V_{OD} voltages.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|------|-------|------|-------|
| Crystal Oscillator Mode Specifications | | | | | | |
| f _{XTAL} | Crystal Frequency Range | | 6 | | 20 | MHz |
| ESR | Crystal Effective Series Resistance | 6 MHz < F _{XTAL} < 20 MHz | | | 100 | Ohms |
| P _{XTAL} | Crystal Power Dissipation ⁽¹⁰⁾ | Vectron VXB1 crystal, 12.288 MHz, R _{ESR} < 40 Ω | | 200 | | μW |
| C _{IN} | Input Capacitance of LMK041xx OSCin port | -40 to +85 °C | | 6 | | pF |
| PLL2 Phase Detector and Charge Pump Specifications | | | | | | |
| f _{PD} | Phase Detector Frequency | | | | 100 | MHz |
| I _{CPout} SOURCE | PLL2 Charge Pump Source Current ⁽⁶⁾ | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 00b | | 100 | | μA |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 01b | | 400 | | |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 10b | | 1600 | | |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 11b | | 3200 | | |
| I _{CPout} SINK | PLL2 Charge Pump Sink Current ⁽⁶⁾ | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 00b | | -100 | | μA |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 01b | | -400 | | |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 10b | | -1600 | | |
| | | V _{CPout2} =V _{CC} /2, PLL2_CP_GAIN = 11b | | -3200 | | |
| I _{CPout2} %MIS | Charge Pump Sink/Source Mismatch | V _{CPout2} =V _{CC} /2, T _A = 25 °C | | 3 | 10 | % |
| I _{CPout2} V _{TUNE} | Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation | 0.5 V < V _{CPout2} < V _{CC} - 0.5 V T _A = 25 °C | | 4 | | % |
| I _{CPout2} %TEMP | Charge Pump Current vs. Temperature Variation | | | 4 | | % |
| I _{CPout2} TRI | Charge Pump Leakage | 0.5 V < V _{CPout2} < V _{CC} - 0.5 V | | | 10 | nA |
| Internal VCO Specifications | | | | | | |
| f _{VCO} | VCO Tuning Range | LMK041x0 | 1185 | | 1296 | MHz |
| | | LMK041x1 | 1430 | | 1570 | |
| | | LMK041x2 | 1600 | | 1750 | |
| | | LMK041x3 | 1840 | | 2160 | |
| P _{VCO} | VCO Output power to a 50 Ω load driven by Fout | LMK041x0, T _A = 25 °C, single-ended | | 3 | | dBm |
| | | LMK041x1, T _A = 25 °C, single-ended | | 3 | | |
| | | LMK041x2, T _A = 25 °C, single-ended | | 2 | | |
| | | LMK041x3, T _A = 25 °C, single-ended 1840 MHz | | 0 | | |
| | | LMK041x3, T _A = 25 °C, single-ended 2160 MHz | | -5 | | |

(10) See Application Section discussion of Crystal Power Dissipation.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|---|-----------------------|----------|-----------------|-------|
| K _{VCO} | Fine Tuning Sensitivity (The range displayed in the typical column indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range). | LMK041x0 | | 7 to 9 | | MHz/V |
| | | LMK041x1 | | 8 to 11 | | |
| | | LMK041x2 | | 9 to 14 | | |
| | | LMK041x3 | | 14 to 26 | | |
| ΔT _{CL} | Allowable Temperature Drift for Continuous Lock (11) | After programming R15 for lock, no changes to output configuration are permitted to guarantee continuous lock | | | 125 | °C |
| CLKout's Internal VCO Closed Loop Jitter Specifications using a Commercial Quality VCXO | | | | | | |
| J _{CLKout} 12 kHz–20MHz | LMK041x0/ LMK041x1/ LMK041x2/ f _{CLKout} = 122.88 MHz Integrated RMS Jitter | LVDS | | 160 | | fs |
| | | LVPECL 1600 mVpp | | 150 | | |
| | | LVC MOS | | 140 | | |
| | LMK041x3 f _{CLKout} = 122.88 MHz Integrated RMS Jitter | LVDS | | 170 | | fs |
| | | LVPECL 1600 mVpp | | 160 | | |
| | | LVC MOS | | 150 | | |
| J _{CLKout} 1.875–20MHz | LMK041x0/ LMK041x1/ LMK041x3/ f _{CLKout} = 153.6 MHz Integrated RMS Jitter | LVDS | | 90 | | fs |
| | | LVPECL 1600 mVpp | | 80 | | |
| | | LVC MOS | | 75 | | |
| | | | | | | |
| Digital Inputs (CLKuWire, DATAuWire, LEuWire) | | | | | | |
| V _{IH} | High-Level Input Voltage | | 1.6 | | V _{CC} | V |
| V _{IL} | Low-Level Input Voltage | | | | 0.4 | V |
| I _{IH} | High-Level Input Current | V _{IH} = V _{CC} | -5 | | 25 | μA |
| I _{IL} | Low-Level Input Current | V _{IL} = 0 | -5.0 | | 5.0 | μA |
| Digital Inputs (GOE, SYNC*) | | | | | | |
| V _{IH} | High-Level Input Voltage | | 1.6 | | V _{CC} | V |
| V _{IL} | Low-Level Input Voltage | | | | 0.4 | V |
| I _{IH} | High-Level Input Current | V _{IH} = V _{CC} | -5.0 | | 5.0 | μA |
| I _{IL} | Low-Level Input Current | V _{IL} = 0 | -40.0 | | 5.0 | μA |
| Digital Outputs (CLKinX_LOS, LD) | | | | | | |
| V _{OH} | High-Level Output Voltage | I _{OH} = -500 μA | V _{CC} - 0.4 | | | V |
| V _{OL} | Low-Level Output Voltage | I _{OL} = 500 μA | | | 0.4 | V |
| Default Power On Reset Clock Output Frequency | | | | | | |
| f _{CLKout-startup} | Default output clock frequency at device power on | CLKout2, LM041x0 | | 50 | | MHz |
| | | CLKout2, LM041x1 | | 62 | | |
| | | CLKout2, LM041x2 | | 68 | | |
| | | CLKout2, LM041x3 | | 81 | | |

(11) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R0 register was last programmed, and still have the part stay in lock. The action of programming the R0 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R0 register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of -40 °C to 85 °C without violating specifications.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|--|--|---------------------------|-------|-------|
| LVDS Clock Outputs (CLKoutX) | | | | | | |
| f _{CLKout} | Maximum Frequency | R _L = 100 Ω | 1080 | | | MHz |
| T _{SKEW} | CLKoutX to CLKoutY (12) | LVDS-LVDS, T = 25 °C, F _{CLK} = 800 MHz, R _L = 100 Ω | | | 30 | ps |
| V _{OD} | Differential Output Voltage (13) | R = 100 Ω differential termination, AC coupled to receiver input, F _{CLK} = 800 MHz, T = 25 °C | 250 | 350 | 450 | mV |
| V _{SS} | | | 500 | 700 | 900 | mVpp |
| ΔV _{OD} | Change in Magnitude of V _{OD} for complementary output states | | -50 | | 50 | mV |
| V _{OS} | Output Offset Voltage | | 1.125 | 1.25 | 1.375 | V |
| ΔV _{OS} | Change in V _{OS} for complementary output states | | | | 35 | mV |
| I _{SA} I _{SB} | Output short circuit current - single ended | | Single-ended output shorted to GND, T = 25 °C | -24 | | 24 |
| I _{SAB} | Output short circuit current - differential | Complimentary outputs tied together | -12 | | 12 | mA |
| LVPECL Clock Outputs (CLKoutX) (14) | | | | | | |
| f _{CLKout} | Maximum Frequency | | 1080 | | | MHz |
| T _{SKEW} | CLKoutX to CLKoutY (12) | LVPECL-to-LVPECL, T = 25 °C, F _{CLK} = 800 MHz, each output terminated with 120 Ω to GND. | | | 40 | ps |
| V _{OH} | Output High Voltage | F _{CLK} = 100 MHz, T = 25 °C Termination = 50 Ω to V _{CC} - 2 V | | V _{CC} - 0.93 | | V |
| V _{OL} | Output Low Voltage | | | V _{CC} - 1.82 | | V |
| V _{OD} | Output Voltage (13) | | 660 | 890 | 965 | mV |
| V _{SS} | | | 1320 | 1780 | 1930 | mVpp |

(12) Equal loading and identical channel configuration on each channel is required for specification to be valid.

(13) See [Differential Voltage Measurement Terminology](#) for definition of V_{ID} and V_{OD} voltages.

(14) LVPECL/2VPECL is programmable for all NSIDs.

Electrical Characteristics (continued)

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40 °C ≤ T_A ≤ 85 °C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, at the [Recommended Operating Conditions](#) at the time of product characterization and are not guaranteed.)

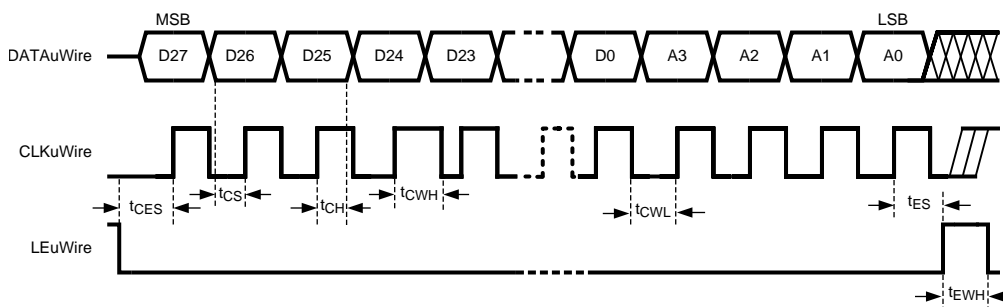
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|---|-----------------------|------------------------|------|-------|
| 2VPECL Clock Outputs (CLKoutX) | | | | | | |
| f _{CLKout} | Maximum Frequency | | 1080 | | | MHz |
| T _{SKEW} | CLKoutX to CLKoutY ⁽¹⁵⁾ | 2VPECL-2VPECL, T=25 °C, F _{CLK} = 800 MHz, each output terminated with 120 Ω to GND. | | | 40 | ps |
| V _{OH} | Output High Voltage | F _{CLK} = 100 MHz, T = 25 °C Termination = 50 Ω to V _{CC} - 2 V | | V _{CC} - 0.95 | | V |
| V _{OL} | Output Low Voltage | | | V _{CC} - 1.98 | | V |
| V _{OD} | Output Voltage ⁽¹⁶⁾ | | 800 | 1030 | 1200 | mV |
| V _{SS} | | | 1600 | 2060 | 2400 | mVpp |
| LVC MOS Clock Outputs (CLKoutX) | | | | | | |
| f _{CLKout} | Maximum Frequency | 5 pF Load | 250 | | | MHz |
| V _{OH} | Output High Voltage | 1 mA Load | V _{CC} - 0.1 | | | V |
| V _{OL} | Output Low Voltage | 1 mA Load | | | 0.1 | V |
| I _{OH} | Output High Current (Source) | V _{CC} = 3.3 V, V _O = 1.65 V | | 28 | | mA |
| I _{OL} | Output Low Current (Sink) | V _{CC} = 3.3 V, V _O = 1.65 V | | 28 | | mA |
| T _{SKEW} | Skew between any two LVC MOS outputs, same channel or different channel | R _L = 50 Ω, C _L = 10 pF, T = 25 °C, F _{CLK} = 100 MHz. ⁽¹⁵⁾ | | | 100 | ps |
| DUTY _{CLK} | Output Duty Cycle | V _{CC} /2 to V _{CC} /2, F _{CLK} = 100 MHz, T = 25 °C ⁽¹⁷⁾ | 45 | 50 | 55 | % |
| T _R | Output Rise Time | 20% to 80%, R _L = 50 Ω, C _L = 5 pF | | 400 | | ps |
| T _F | Output Fall Time | 80% to 20%, R _L = 50 Ω, C _L = 5 pF | | 400 | | ps |
| Mixed Clock Skew | | | | | | |
| T _{SKEW ChanX - ChanY} | LVPECL to LVDS skew | Same device, T = 25 °C, 250 MHz | | -230 | | ps |
| | LVDS to LVC MOS skew | Same device, T = 25 °C, 250 MHz | | 770 | | ps |
| | LVC MOS to LVPECL skew | Same device, T = 25 °C, 250 MHz | | -540 | | ps |
| Microwire Interface Timing | | | | | | |
| T _{CS} | Data to Clock Setup Time | See MICROWIRE Input Timing | 25 | | | ns |
| T _{CH} | Data to Clock Hold Time | See MICROWIRE Input Timing | 8 | | | ns |
| T _{CWH} | Clock Pulse Width High | See MICROWIRE Input Timing | 25 | | | ns |
| T _{CWL} | Clock Pulse Width Low | See MICROWIRE Input Timing | 25 | | | ns |
| T _{ES} | Clock to Latch Enable Setup Time | See MICROWIRE Input Timing | 25 | | | ns |
| T _{CES} | Enable to Clock Setup | See MICROWIRE Input Timing | 25 | | | ns |
| T _{EW} | Load Enable Pulse Width | See MICROWIRE Input Timing | 25 | | | ns |

(15) Equal loading and identical channel configuration on each channel is required for specification to be valid.

(16) See [Differential Voltage Measurement Terminology](#) for definition of V_{ID} and V_{OD} voltages.

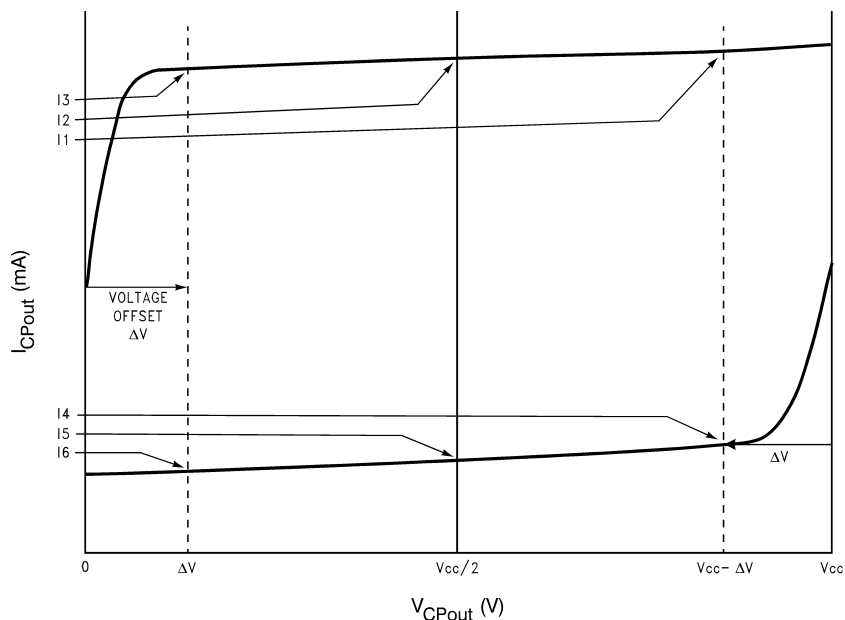
(17) Guaranteed by characterization.

Serial Data Timing Diagram



Register programming information on the DATAuWire pin is clocked into a shift register on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/ μ s is recommended for these signals. After programming is complete the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state. If the CLKuWire or DATAuWire lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

Figure 2. Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $V_{CPout} = V_{CC} - \Delta V$

I2 = Charge Pump Sink Current at $V_{CPout} = V_{CC}/2$

I3 = Charge Pump Sink Current at $V_{CPout} = \Delta V$

I4 = Charge Pump Source Current at $V_{CPout} = V_{CC} - \Delta V$

I5 = Charge Pump Source Current at $V_{CPout} = V_{CC}/2$

I6 = Charge Pump Source Current at $V_{CPout} = \Delta V$

ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

CHARGE PUMP OUTPUT CURRENT MAGNITUDE VARIATION VS. CHARGE PUMP OUTPUT VOLTAGE

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

CHARGE PUMP SINK CURRENT VS. CHARGE PUMP OUTPUT SOURCE CURRENT MISMATCH

$$I_{CPout \text{ Sink}} \text{ Vs } I_{CPout \text{ Source}} = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

CHARGE PUMP OUTPUT CURRENT MAGNITUDE VARIATION VS. TEMPERATURE

$$I_{CPout} \text{ Vs } T_A = \frac{|I2|_{T_A} - |I2|_{T_A=25^\circ C}}{|I2|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I5|_{T_A} - |I5|_{T_A=25^\circ C}}{|I5|_{T_A=25^\circ C}} \times 100\%$$

Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 11 illustrates the two different definitions side-by-side for inputs and Figure 12 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

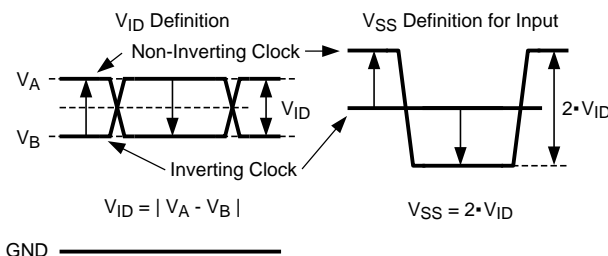
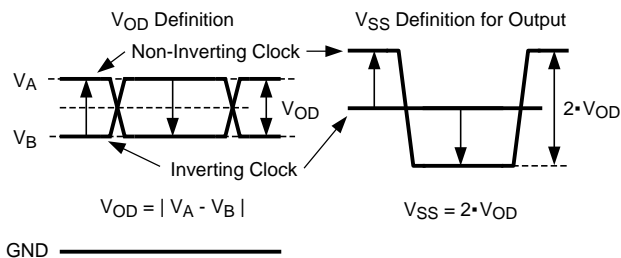


Figure 3. Two Different Definitions for Differential Input Signals



Refer to application note AN-912 Common Data Transmission Parameters and their Definitions ([SNLA036](#)) for more information.

Figure 4. Two Different Definitions for Differential Output Signals

Typical Performance Characteristics

CLOCK OUTPUT AC CHARACTERISTICS

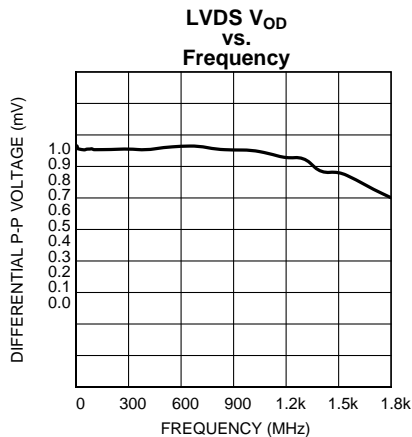


Figure 5.

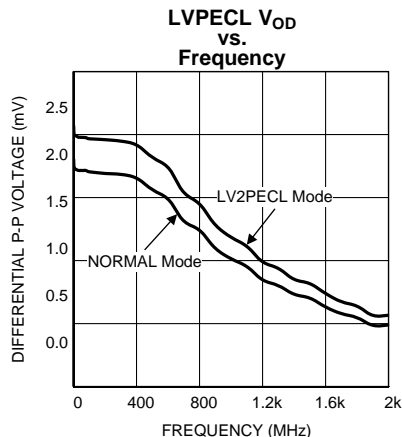


Figure 6.

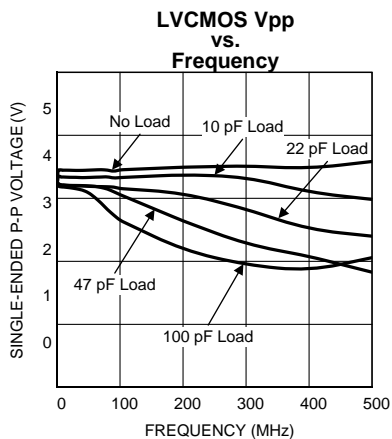


Figure 7.

Typical Dynamic I_{CC} , LVCMOS Driver, $V_{CC} = 3.3 V$,
Temp = 25 °C, $C_L = 5 pF$

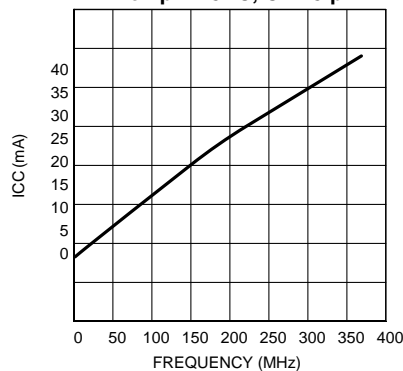
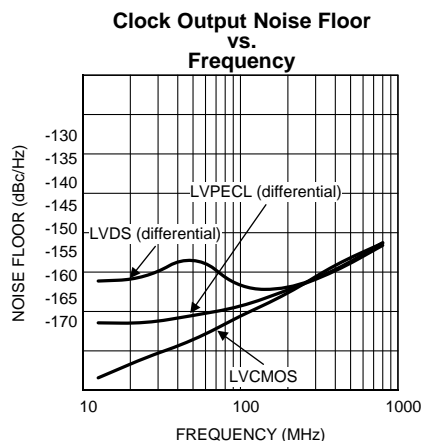


Figure 8.



To estimate this noise, only the output frequency is required. Divide value and input frequency are not relevant.
Figure 9.

FEATURES

SYSTEM ARCHITECTURE

The cascaded PLL architecture of the LMK041xx was chosen to provide the lowest jitter performance over the widest range of output frequencies and phase noise offset frequencies. The first stage PLL (PLL1) is used in conjunction with an external reference clock and an external VCXO to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2). PLL1 typically uses a narrow loop bandwidth (10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. The “cleaned” reference clock frequency accuracy is combined with the low phase noise of an external VCXO to provide the reference input to PLL2. The low phase noise reference provided to PLL2 allows it to use wider loop bandwidths (50 kHz to 200 kHz). The chosen loop bandwidth for PLL2 should take best advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO for PLL2. Low jitter is achieved by allowing the external VCXO’s phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO’s phase noise to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

REDUNDANT REFERENCE INPUTS (CLKin0/CLKin0*, CLKin1/CLKin1*)

The LMK041xx has two LVDS/LVPECL/LVCMOS compatible reference clock inputs for PLL1, CLKin0 and CLKin1. The selection of the preferred input may be fixed to either CLKin0 or CLKin1, or may be configured to employ one of two automatic switching modes when redundant clock signals are present. The PLL1 reference clock input buffers may also be individually configured as either a CMOS buffered input or a bipolar buffered input.

PLL1 CLKinX (X=0,1) LOSS OF SIGNAL (LOS)

When either of the two auto-switching modes is selected for the reference clock input mode, the signal status of the selected reference clock input is indicated by the state of the CLKinX_LOS (loss-of-signal) output. These outputs may be configured as either CMOS (active HIGH on loss-of-signal), NMOS open-drain or PMOS open-drain. If PLL1 was originally locked and then both reference clocks go away, then the frequency accuracy of the LMK04100 device will be set by the absolute tuning range of the VCXO used on PLL1. The absolute tuning range of the VCXO can be determined by multiplying its’ tuning constant by the charge pump voltage.

INTEGRATED LOOP FILTER POLES

The LMK041xx features programmable 3rd and 4th order loop filter poles for PLL2. When enabled, internal resistors and capacitor values may be selected from a fixed range of values to achieve either 3rd or 4th order loop filter response. These programmable components compliment external components mounted near the chip.

CLOCK DISTRIBUTION

The LMK041xx features a clock distribution block with a minimum of five outputs that are a mixture of LVPECL, 2VPECL, LVDS, and LVCMOS. The exact combination is determined by the part number. The 2VPECL is a Texas Instruments proprietary configuration that produces a 2 Vpp differential swing for compatibility with many data converters. More than five outputs may be available for device versions that offer dual LVCMOS outputs.

CLKout DIVIDE (CLKoutX_DIV, X = 0 to 4)

Each individual clock distribution channel includes a channel divider. The range of divide values is 2 to 510, in steps of 2. “Bypass” mode operates as a divide-by-1.

GLOBAL CLOCK OUTPUT SYNCHRONIZATION (SYNC*)

The SYNC* input is used to synchronize the active clock outputs. When SYNC* is held in a logic low state, the outputs are also held in a logic low state. When SYNC* goes high, the clock outputs are activated and will transition to a high state simultaneously with one another.

SYNC* must be held low for greater than one clock cycle of the Clock Distribution Path. After this low event has been registered, the outputs will not reflect the low state for four more cycles. Similarly after SYNC* becomes high, the outputs will simultaneously transition high after four Clock Distribution Path cycles have passed. See [Figure 10](#) for further detail.

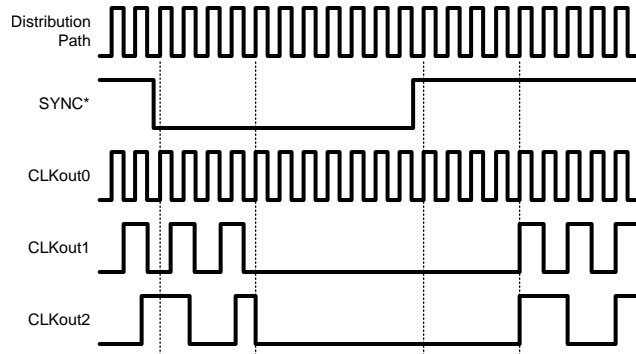


Figure 10. Clock Output synchronization using the SYNC* pin

GLOBAL OUTPUT ENABLE AND LOCK DETECT

Each Clock Output Channel may be either enabled or put into a high impedance state via the Clock Output Enable control bit (one for each channel). Each output enable control bit is gated with the Global Output Enable input pin (GOE). The GOE pin provides an internal pull-up so that if it is un-terminated externally, then the clock output states are determined by the Clock Channel Output Enable Register bits. All clock outputs can be disabled simultaneously if the GOE pin is pulled low by an external signal.

Table 4. Clock Output Control

| CLKoutX _EN bit | EN_CLKout _Global bit | GOE pin | CLKoutX Output State |
|--------------------|--------------------------|-------------------|----------------------|
| 1 | 1 | Low | Low |
| Don't care | 0 | Don't care | Off |
| 0 | Don't care | Don't care | Off |
| 1 | 1 | High / No Connect | Enabled |

The Lock Detect (LD) signal can be connected to the GOE pin in which case all outputs are disabled automatically if the synthesizer is not locked. See [EN_CLKoutX: Clock Channel Output Enable](#) and also [SYSTEM LEVEL DIAGRAM](#) for actual implementation details.

The Lock Detect (LD) pin can be programmed to output a 'High' when both PLL1 and PLL2 are locked, or only when PLL1 is locked or only when PLL2 is locked.

Functional Description

ARCHITECTURAL OVERVIEW

The LMK041xx chip consists of two high performance synthesizer blocks (Phase Locked Loop, internal VCO/VCO Divider, and loop filter), source selection, distribution system, and independent clock output channels.

The Phase Frequency Detector in PLL1 compares the divided (R Divider 1) system clock signal from the selected CLKinX and CLKinX* input with the divided (N Divider 1) output of the external VCXO attached to the PLL2 OSCin port. The external loop filter for PLL1 should be narrow to provide a clean reference clock from the external VCXO to the OSCin/OSCin* pins for PLL2.

The Phase Frequency Detector in PLL2 then compares the divided (R Divider 2) reference signal from the PLL2 OSCin port with the divided (N Divider 2 and VCO Divider) output of the internal VCO. The bandwidth of the external loop filter for PLL2 should be designed to be wide enough to take advantage of the low in-band phase noise of PLL2 and the low high offset phase noise of the internal VCO. The VCO output is passed through a common VCO divider block and placed on a distribution path for the clock distribution section. It is also routed to the PLL2_N counter. Each clock output channel allows the user to select a path with a programmable divider block, a phase synchronization circuit, and LVDS/LVPECL/2VPECL/LVCMOS compatible output buffers.

PHASE DETECTOR 1 (PD1)

Phase Detector 1 in PLL1 (PD1) can operate up to 40 MHz. Since a narrow loop bandwidth should be used for PLL1, the need to operate at high phase detector rate to lower the in-band phase noise becomes unnecessary.

PHASE DETECTOR 2 (PD2)

Phase Detector 2 in PLL2 (PD2) supports a maximum comparison rate of 100 MHz, though the actual maximum frequency at the input port (PLL2 OSCin/OSCin*) is 250 MHz. Operating at highest possible phase detector rate will ensure low in-band phase noise for PLL2 which in turn produces lower total jitter, as the in-band phase noise from the reference input and PLL are proportional to N^2 .

PLL2 FREQUENCY DOUBLER

The PLL2 reference input at the OSCin port may be optionally routed through a frequency doubler function rather than through the PLL2_R counter. The maximum phase comparison frequency of the PLL2 phase detector is 100 MHz, so the input to the frequency doubler is limited to a maximum of 50 MHz. The frequency doubler feature allows the phase comparison frequency to be increased when a relative low frequency oscillator is driving the OSCin port. By doubling the PLL2 phase comparison frequency, the in-band PLL2 noise is reduced by about 3 dB.

INPUTS / OUTPUTS

PLL1 Reference Inputs (CLKin0 / CLKin0*, CLKin1 / CLKin1*)

The reference clock inputs for PLL1 may be selected from either CLKin0 and CLKin1. The user has the capability to manually select one of the two inputs or to configure an automatic switching mode operation. A detailed description of this function is described in the uWire programming section of this data sheet.

PLL2 OSCin / OSCin* Port

The feedback from the external oscillator being locked with PLL1 is injected to the PLL2 OSCin/OSCin* pins. This input may be driven with either an AC coupled single-ended or AC coupled differential signal. If operated in single ended mode, the unused input should be tied to GND with a 0.1 μ F capacitor. Internal to the chip, this signal is routed to the PLL1_N Counter and to the reference input for PLL2. The internal circuitry of the OSCin port also supports the optional implementation of a crystal based oscillator circuit. A crystal, varactor diode and a small number of other external components may be used to implement the oscillator. The internal oscillator circuit is enabled by setting the EN_PLL2_XTAL bit.

CPout1 / CPout2

The CPout1 pin provides the charge pump current output to drive the loop filter for PLL1. This loop filter should be configured so that the total loop bandwidth for PLL1 is less than 200 Hz. When combined with an external oscillator that has low phase noise at offsets close to the carrier, PLL1 generates a reference for PLL2 that is frequency locked to the PLL1 reference clock but has the phase noise performance of the oscillator. The CPout2 pin provides the charge pump current output to drive the loop filter for PLL2. This loop filter should be configured so that the total loop bandwidth for PLL2 is in the range of 50 kHz to 200 kHz. See the section on uWire device control for a description of the charge pump current gain control.

Fout

The buffered output of the internal VCO is available at the Fout pin. This is a single-ended output (sinusoid). Each time the PLL2_N counter value is updated via the uWire interface, an internal algorithm is triggered that optimizes the VCO performance.

Digital Lock Detect 1 Bypass

The VCO coarse tuning algorithm requires a stable OSCin clock (reference clock to PLL2) to frequency calibrate the internal VCO correctly. In order to ensure a stable OSCin clock, the first PLL must achieve lock status. A digital lock detect is used in PLL1 to monitor its lock status. After lock is achieved by PLL1, the coarse tuning circuitry is enabled and frequency calibration for the internal VCO begins.

The (DLD_BYP) pin is provided to allow an external bypass cap to be connected to the digital lock detect 1. This capacitor will eliminate potential glitches at initial startup of PLL1 due to unknown phase relationships between the Ncntr1 and Rcntr1.

Bias

Proper bypassing of this pin by a 1 μ F capacitor connected to V_{CC} is important for low noise performance.

General Programming Information

LMK041xx devices are programmed using several 32-bit registers. Each register consists of a 4-bit address field and 28-bit data field. The address field is formed by bits 0 through 3 (LSBs) and the data field is formed by bits 4 through 31 (MSBs). The contents of each register are clocked in MSB first (bit 31), and the LSB (bit 0) last. During programming, the LE signal should be held LOW. The serial data is clocked in on the rising edge of the CLK signal. After the LSB (bit 0) is clocked in the LE signal should be toggled LOW-to-HIGH-to-LOW to latch the contents into the register selected in the address field. Registers R0-R4, R7, and R8-R15 must be programmed in order to achieve proper device operation. [Figure 11](#) illustrates the serial data timing sequence.

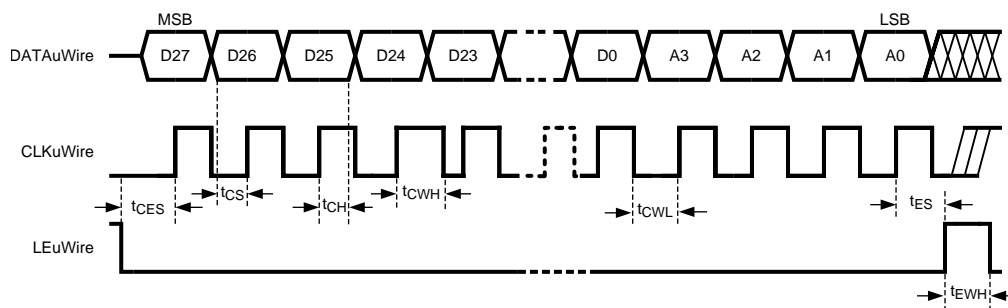


Figure 11. uWire Timing Diagram

To achieve proper frequency calibration, the OSCin port must be driven with a valid signal before programming Register 15. Changes to PLL2_R Counter or the OSCin port signal require Register 15 to be reloaded in order to activate the frequency calibration process.

RECOMMENDED PROGRAMMING SEQUENCE

The recommended programming sequence involves programming R7 with the reset bit set to 1 (Reg. 7, bit 4) to ensure the device is in a default state. If R7 is programmed again, the reset bit should be set to 0. Registers are programmed in order with R15 being the last register programmed. An example programming sequence is shown below:

- Program R7 with the RESET bit = 1 (b4 = 1). This ensures that the device is configured with default settings. When RESET = 1, all other R7 bits are ignored.
 - If R7 is programmed again during the initial configuration of the device, the RESET bit should be cleared (b4 = 0)
- Program R0 through R4 as necessary to configure the clock outputs as desired. These registers configure clock channel functions such as the channel multiplexer output selection, divide value, and enable/disable bit.
- Program R5 and R6 with the default values shown in the register map on the following pages.
- Program R7 with RESET = 0.
- Program R8 through R10 with the default values shown in the register map on the following pages.
- Program R11 to configure the reference clock inputs (CLKin0 and CLKin1).
 - type, LOS timeout, LOS type, and mode (manual or auto-switching)
- Program R12 to configure PLL1.

- Charge pump gain, polarity, R counter and N counter
- Program R13 through R15 to configure PLL2 parameters, crystal mode options, and certain globally asserted functions.

The following table provides the register map for device programming:

Table 5. Register Map

| Register | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
|----------|-------------|----|----|----|----|----|----|----|-----------------|----------------------|----|----------------------|-------------------|-------------------|-------------------|-------------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Data [31:4] | | | | | | | | | | | | | | | | | | | | | | | | | | A | A | A | A | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | 3 | 2 | 1 | 0 | | | | | |
| R0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLKout0_PEC_LVL | 0 | 0 | 0 | 0 | CLKout0_MUX | EN_CLKout0 | CLKout0_DIV [7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLKout1_PEC_LVL | CLKout1B_STATE [1:0] | | CLKout1A_STATE [1:0] | CLKout1_MUX [1:0] | EN_CLKout1 | CLKout1_DIV [7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| R2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLKout2_PEC_LVL | CLKout2B_STATE [1:0] | | CLKout2A_STATE [1:0] | CLKout2_MUX [1:0] | EN_CLKout2 | CLKout2_DIV [7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | |
| R3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLKout3_PEC_LVL | CLKout3B_STATE [1:0] | | CLKout3A_STATE [1:0] | CLKout3_MUX [1:0] | EN_CLKout3 | CLKout3_DIV [7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | |
| R4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | CLKout4_PEC_LVL | 0 | 0 | 0 | 0 | CLKout4_MUX [1:0] | EN_CLKout4 | CLKout4_DIV [7:0] | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | | | |
| R5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | | | | |
| R6 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | | | |

Table 5. Register Map (continued)

| Register | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|--------------------|---------------|-----------------------|--------------------|---------------|----|----|----|----|-----------------------|---------|----|-----------------------------|-------------------------|---------------|-------------------|-------------------|------------------|------------------|---------------------|----------------|----------------|-------------------|----------------|-----------------|---|-------|---|---|---|---|
| R7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESET | 0 | 1 | 1 | 1 |
| R8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| R9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| R10 | 0 | 0 | RC_DLD1_Start | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| R11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | CLKin1_BUFTYPE | CLKin0_BUFTYPE | LOS_TIMEOUT [1:0] | LOS_TYPE [1:0] | CLKin_SEL [1:0] | | | 1 | 0 | 1 | 1 |
| R12 | PLL1_CP_POL | PLL1_CP_GAIN [2:0] | | PLL1_R Counter [11:0] | | | | | | | | | | | PLL1_N Counter [11:0] | | | | | | | | | | | 1 | 1 | 0 | 0 | | | |
| R13 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | EN_PLL2_XTAL | EN_Fout | 0 | EN_CLKout_Global, default=1 | POWER DOWN, default = 0 | EN_PLL2_REF2X | PLL2 CP TRI-STATE | PLL1 CP TRI-STATE | PLL2_R4_LF [2:0] | PLL2_R3_LF [2:0] | PLL2_C3_C4_LF [3:0] | | | 1 | 1 | 0 | 1 | | | | | |
| R14 | 0 | 0 | 0 | OSCin_FREQ [7:0] | | | | | | | PLL_MUX [4:0] | | | | PLL2_R Counter [11:0] | | | | | | | | | | | 1 | 1 | 1 | 0 | | | |
| R15 | 0 | 0 | 0 | 1 | PLL2_CP_GAIN [1:0] | VCO_DIV [3:0] | | | | | PLL2_N Counter [17:0] | | | | | | | | | | | | | | | | | 1 | 1 | 1 | 1 | |

DEFAULT DEVICE REGISTER SETTINGS AFTER POWER ON/RESET

Table 6 illustrates the default register settings programmed in silicon for the LMK041xx after power on or asserting the reset bit.

Table 6. Default Device Register Settings after Power On/Reset

| Field Name | Default Value (decimal) | Default State | Field Description | Register | Bit Location (MSB:LSB) |
|--------------------|-------------------------|-----------------------------|---|--------------------|------------------------|
| CLKoutX_PECL_LVL | 0 | 2VPECL disabled | This bit sets LVPECL clock level. Valid when the clock channel is configured as LVPECL/2VPECL; otherwise, not relevant. | R0 to R4 | 23 |
| CLKoutXB_STATE | 0 | Inverted | This field sets the state of output B of an LVCMOS Clock channel. | R1 to R3 | 22:21 |
| CLKoutXA_STATE | 1 | Non-Inverted | This field sets the state of output A of an LVCMOS Clock channel. | R1 to R3 | 20:19 |
| EN_CLKoutX | 0 | OFF | Clock Channel enable bit. Note: The state of CLKout2 is ON by default. | R0 to R4 | 16 |
| Reserved Registers | | (1) | (1) | R5,R6,R8 R9,R10 | NA |
| RC_DLD1_Start | 1 | Enabled | Forces the VCO tuning algorithm state machine to wait until PLL1 is locked. | R10 | 29 |
| CLKin1_BUFTYPE | 1 | MOS mode | CLKin1 Input Buffer Type | R11 | 11 |
| CLKin0_BUFTYPE | 1 | MOS mode | CLKin0 Input Buffer Type | R11 | 10 |
| LOS_TIMEOUT | 1 | 3 MHz (min.) | Selects Lower Reference Clock input frequency for LOS Detection. | R11 | 9:8 |
| LOS_TYPE | 3 | CMOS | Selects LOS output type ⁽²⁾ | R11 | 7:6 |
| CLKin_SEL | 0 | CLKin0 | Selects Reference Clock source | R11 | 5:4 |
| PLL1 CP Polarity | 1 | Positive polarity | Selects the charge pump output polarity, i.e., the tuning slope of the external VCXO | R12 | 31 |
| PLL1_CP_GAIN | 6 | 100 μ A | Sets the PLL1 Charge Pump Gain | R12 | 30:28 |
| PLL1_R Counter | 1 | Divide = 1 | Sets divide value for PLL1_R Counter | R12 | 27:16 |
| PLL1_N Counter | 1 | Divide = 1 | Sets divide value for PLL1_N Counter | R12 | 15:4 |
| EN_PLL2_REF2X | 0 | Disabled | Enables or disables the OSCin frequency doubler path for the PLL2 reference input | R13 | 16 |
| EN_PLL2_XTAL | 0 | OFF | Enables or Disables internal circuits that support an external crystal driving the OSCin pins | R13 | 21 |
| EN_Fout | 0 | OFF | Enables or disables the VCO output buffer | R13 | 20 |
| CLK Global Enable | 1 | Enabled | Global enable or disable for output clocks | R13 | 18 |
| POWER DOWN | 0 | Disabled (device is active) | Device power down control | R13 | 17 |
| PLL2 CP TRI-STATE | 0 | TRI-STATE disabled | Enables or disables TRI-STATE for PLL2 Charge Pump | R13 | 15 |
| PLL1 CP TRI-STATE | 0 | TRI-STATE disabled | Enables or disables TRI-STATE for PLL1 Charge Pump | R13 | 14 |
| OSCin_FREQ | 200 | 200 MHz | Source frequency driving OSCin port | R14 | 28:21 |
| PLL_MUX | 31 | Reserved | Selects output routed to LD pin | R14 | 20:16 |
| PLL2_R Counter | 1 | Divide = 1 | Sets Divide value for PLL2_R Counter | R14 | 15:4 |
| PLL2_CP_GAIN | 2 | 1600 μ A | Sets PLL2 Charge Pump Gain | R15 | 27:26 |
| VCO_DIV | 2 | Divide = 2 | Sets divide value for VCO output divider | R15 | 25:22 |
| PLL2_N Counter | 1 | Divide = 1 | Sets PLL2_N Counter value | R15 | 21:4 |

(1) These registers are reserved. The Power On/Reset values for these registers are shown in the register map and should not be changed during programming.

(2) If the CLKin_SEL value is set to either [0,0] or [0,1], the LOS_TYPE field should be set to [0,0].

REGISTER R0 TO R4

Registers R0 through R4 control the five clock outputs. Register R0 controls CLKout0, Register R1 controls CLKout1, and so on. Aside from this, the functions of the bits in these registers are identical. The X in CLKoutX_MUX, CLKoutX_DIV, and CLKoutX_EN denote the actual clock output which may be from 0 to 4.

CLKoutX_DIV: Clock Channel Divide Registers

Each of the five clock output channels (0 through 4) has a dedicated 8-bit divider followed by a fixed divide by 2 that is used to generate even integer related versions of the distribution path clock frequency (VCO Divider output). If the VCO Divider value is even then the Channel Divider may be bypassed (See CLK Output Mux), giving an effective divisor of 1 while preserving a 50% duty cycle output waveform.

Table 7. CLKoutX_DIV: Clock Channel Divide Values

| CLKoutX_DIV [7:0] | | | | | | | | Total Divide Value |
|---------------------|----|----|----|----|----|----|----|--------------------|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | invalid |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 6 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10 |
| - | - | - | - | -- | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 510 |

EN_CLKoutX: Clock Channel Output Enable

Each Clock Output Channel may be either enabled or disabled via the Clock Output Enable control bits. Each output enable control bit is gated with the Global Output Enable input pin (GOE) and Global Output Enable bit (EN_CLKout_Global). The GOE pin provides an internal pull-up so that if it is unterminated externally, the clock output states are determined by the Clock Output Enable Register bits. All clock outputs can be set to the low state simultaneously if the GOE pin is pulled low by an external signal. If EN_CLKout_Global is programmed to 0 all outputs are turned off. If both GOE and EN_CLKout_Global are low the clock outputs are turned off.

Table 8. EN_CLKoutX: Clock Channel Output Enable Control Bits

| BIT NAME | BIT = 1 | BIT = 0 | DEFAULT |
|------------------|--|-----------------------|---------|
| EN_CLKout0 | ON | OFF | OFF |
| EN_CLKout1 | ON | OFF | OFF |
| EN_CLKout2 | ON | OFF | ON |
| EN_CLKout3 | ON | OFF | OFF |
| EN_CLKout4 | ON | OFF | OFF |
| EN_CLKout_Global | According to individual channel settings | All EN_CLKout X = OFF | - |

Note the default state of CLKout2 is ON after power on or RESET assertion. The nominal frequency is 62 MHz (LMK041x1) or 81 MHz (LMK041x3). This is based on a channel divide value of 12 and default VCO_DIV value of 2. If an active CLKout2 at power on is inappropriate for the user's application, the following method can be employed to shut off CLKout2 during system initialization:

When the device is powered on, holding the GOE pin LOW will disable all clock outputs. The device can be programmed while the GOE is held LOW. The state of CLKout2 can be altered during device programming according to the user's specific application needs. After device configuration is complete, the GOE pin should be set HIGH to enable the active clock channels.

CLKoutX/CLKoutX* LVCMOS Mode Control

For clock outputs that are configured as LVCMOS, the LVCMOS CLKoutX/CLKoutX* outputs can be independently configured by uWire CLKoutXA_STATE and CLKoutXB_STATE bits. The following choices are available for LVCMOS outputs:

Table 9. CLKoutXA_STATE, CLKoutXB_STATE Control Bits for LVCMOS Modes

| CLKoutXA_STATE | | CLKoutXB_STATE | | LVCMOS Modes |
|----------------|----|----------------|----|--------------|
| b1 | b0 | b1 | b0 | |
| 0 | 0 | 0 | 0 | Inverted |
| 0 | 1 | 0 | 1 | Normal |
| 1 | 0 | 1 | 0 | Low |
| 1 | 1 | 1 | 1 | TRI-STATE |

CLKoutX/CLKoutX* LVPECL Mode Control

Clock outputs designated as LVPECL can be configured in one of two possible output levels. The default mode is the common LVPECL swing of 800 mVp-p single-ended (1.6 Vp-p differential). A second mode, 2VPECL, can be enabled in which the swing is increased to 1000 mVp-p single-ended (2 Vp-p differential).

Table 10. LVPECL Output Format Control

| CLKoutX_PECL_LVL | Output Format |
|------------------|--------------------|
| 0 | LVPECL (800 mVpp) |
| 1 | 2VPECL (1000 mVpp) |

CLKoutX_MUX: Clock Output Mux

The output of each CLKoutX channel pair is controlled by its' channel multiplexer (mux). The mux can select between several signals: bypassed, divided only.

Table 11. CLKoutX_MUX: Clock Channel Multiplexer Control Bits

| CLKout_MUX | Clock Mode |
|------------|------------|
| 0 | Bypassed |
| 1 | Divided |

REGISTERS 5, 6

These registers are reserved. These register values should not be modified from the values shown in the register map.

REGISTER 7

RESET bit

This bit is only in register R7. The use of this bit is optional and it should be set to '0' if not used. Setting this bit to a '1' forces all registers to their power on reset condition and therefore automatically clears this bit.

REGISTERS 8, 9

These registers are reserved. These register values should not be modified from the values shown in the register map.

REGISTER 10

RC_DLD1_Start: PLL1 Digital Lock Detect Run Control bit

This bit is used to control the state machine for the PLL2 VCO tuning algorithm. The following table describes the function of this bit.

Table 12. RC_DLD1_Start bit states

| RC_DLD1_Start | Description |
|---------------|--|
| 1 | The PLL2 VCO tuning algorithm trigger is delayed until PLL1 Digital Lock Detect is valid. |
| 0 | The PLL2 VCO tuning algorithm runs immediately after any PLL2_N counter update, despite the state of PLL1 Digital Lock Detect. |

If the user is unsure of the state of the reference clock input at startup of the LMK041xx device, setting RC_DLD1_Start = 0 will allow PLL2 to tune and lock the internal VCO to the oscillator attached to the OSCin port. This ensures that the active clock outputs will start up at frequencies close to their desired values. The error in clock output frequency will depend on the open loop accuracy of the oscillator driving the OSCin port. The frequency of an active clock output is normally given by:

$$F_{CLK} = \frac{N}{R} \cdot \frac{F_{OSCin}}{(VCO_DIV \cdot CLK_DIV)}$$

If the open loop frequency accuracy of the external oscillator (either a VCXO or crystal based oscillator) is "X" ppm, then the error in the output clock frequency (F_{CLK} error) will be:

$$F_{CLK \text{ error}} = \frac{N}{R} \cdot \frac{X \cdot F_{OSCin}}{(VCO_DIV \cdot CLK_DIV)}$$

Setting this bit to 0 does not prevent PLL1 from locking the external oscillator to the reference clock input after the latter input becomes valid.

REGISTER 11

CLKinX_BUFTYPE: PLL1 CLKinX/CLKinX* Buffer Mode Control

The user may choose between one of two input buffer modes for the PLL1 reference clock inputs: either bipolar junction differential or MOS. Both CLKinX and CLKinX* input pins must be AC coupled when driven differentially. In single ended mode, the CLKinX* pin must be coupled to ground through a capacitor. The active CLKinX buffer mode is selected by the CLKinX_TYPE bits programmed via the uWire interface.

Table 13. PLL1 CLKinX_BUFTYPE Mode Control Bits

| b1 | b0 | CLKin1_TYPE | CLKin0_TYPE |
|----|----|------------------|------------------|
| 0 | 0 | BJT Differential | BJT Differential |
| 0 | 1 | BJT Differential | MOS |
| 1 | 0 | MOS | BJT Differential |
| 1 | 1 | MOS | MOS |

CLKin_SEL: PLL1 Reference Clock Selection and Revertive Mode Control Bits

This register allows the user to set the reference clock input that is used to lock PLL1, or to select an auto-switching mode. The automatic switching modes are revertive or non-revertive. In either revertive or non-revertive mode, CLKin0 is the initial default reference source for the auto-switching mode. When revertive mode is active, the switching control logic will always select CLKin0 as the reference if it is active, otherwise it selects CLKin1. When non-revertive mode is active, the switching logic will only switch the reference input if the currently selected input fails.

Table 14 illustrates the control modes. Modes [1,0] and [1,1] are the auto-switching modes. The behavior of both modes is tied to the state of the LOS signals for the respective reference clock inputs.

If the reference clock inputs are active prior to configuration of the device, then the normal programming sequence described under [General Programming Information](#) can be used without modification. If it cannot be guaranteed that the reference clocks are active prior to device programming, then the device programming sequence should be modified in order to ensure that CLKin0 is selected as the default. Under this scenario, the device should be programmed as described in "General Programming Information", with CLKin_SEL bits programmed to [0,0] in register R11. The other R11 fields for clock type and LOS timeout should be programmed with the appropriate values for the given application. After the reference clock inputs have started, register R11 should be programmed a second time with the CLKin_SEL field modified to the set the desired mode. The clock type field and LOS field values should remain the same.

Table 14. CLKin_SEL: Reference Clock Selection Bits

| CLKin_SEL [1:0] | | Function |
|-----------------|----|--|
| b1 | b0 | |
| 0 | 0 | Force CLKin0 / CLKin0* as PLL1 reference |
| 0 | 1 | Force CLKin1 / CLKin1* as PLL1 reference |
| 1 | 0 | Non-revertive. Auto-switching. CLKin0 is the default reference clock. If CLKin0 fails, CLKin1 is automatically selected if active. If CLKin0 restarts, CLKin1 remains as the selected reference clock unless it fails, then CLKin0 is re-selected. |
| 1 | 1 | Revertive. Auto-switching. CLKin0 is the preferred reference clock and is selected when active. |

CLKinX_LOS

The CLKin0_LOS and CLKin1_LOS pins indicate the state of the respective PLL1 CLKinX reference input when the CLKin_SEL bits are set to either [1,0] or [1,1]. The detection logic that determines the state of the reference inputs is sensitive to the frequency of the reference inputs and must be configured to operate with the appropriate frequency range of the reference inputs, as described in the next section.

PLL1 Reference Clock LOS Timeout Control

This register is used to tune the LOS timeout based upon the frequency of the reference clock input(s). The register value controls the timeout setting for both CLKin0 and CLKin1. The value programmed in the LOS_TIMEOUT register represents the minimum input frequency for which loss of signal can be detected. For example, if the reference input frequency is 12.288 MHz, then either register values (0,0) or (0,1) will result in valid loss of signal detection. If the reference input frequency is 1 MHz, then only the register value (0,0) will result in valid detection of signal loss.

Table 15. Reference Clock LOS Timeout Control Bits

| b1 | b0 | Corresponding Minimum Input Frequency |
|----|----|---------------------------------------|
| 0 | 0 | 1 MHz |
| 0 | 1 | 3.0 MHz |
| 1 | 0 | 13 MHz |
| 1 | 1 | 32 MHz |

LOS Output Type Control

The output format of the LOS pins may be selected as active CMOS, open drain NMOS and open drain PMOS, as shown in the following table.

Table 16. Loss of Signal (LOS) Output Pin Format Type

| LOS_TYPE [1:0] | | Functional Description |
|----------------|----|------------------------|
| b1 | b0 | |
| 0 | 0 | Reserved |
| 0 | 1 | NMOS open drain |
| 1 | 0 | PMOS open drain |
| 1 | 1 | Active CMOS |

The LOS output signal is valid only when CLKIn_SEL bits are set to either [1,0] or [1,1]. If the CLKIn_SEL field is programmed to either of the fixed inputs, [0,0] or [0,1], the LOS_TYPE bits should be set to [0,0].

REGISTER 12

PLL1_N: PLL1_N Counter

The size of the PLL1_N counter is 12 bits. This counter will support a maximum divide ratio of 4095 and minimum divide ratio of 1. The 12 bit resolution is sufficient to support minimum phase detector frequency resolution of approximately 50 kHz when the VCXO frequency is 200 MHz.

For a 200 MHz external VCXO, the minimum phase detector rate will be $PD_{min} = 200 \text{ MHz}/4095 = 48.84 \text{ kHz}$

Table 17. PLL1_N Counter Values

| N [17:0] | | | | | | | | | | VALUE |
|----------|-----|-----|----|----|----|----|----|----|----|-----------|
| b11 | b10 | ... | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Valid |
| 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| | | | . | . | . | . | . | . | . | ... |
| 1 | 1 | | 1 | | | | | | | 4095 |

PLL1_R: PLL1_R Counter

The size of the PLL1_R counter is 12 bits. This counter will support a maximum divide ratio of 4095 and minimum divide ratio of 1.

Table 18. PLL1_R Counter Values

| R [11:0] | | | | | | | | | | | | VALUE |
|----------|-----|----|----|----|----|----|----|----|----|----|----|-----------|
| b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Valid |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | ... |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4095 |

PLL1 Charge Pump Current Gain (PLL1_CP_GAIN) and Polarity Control (PLL1_CP_POL)

The Loop Band Width (LBW) on PLL1 should be narrow to suppress the noise from the system or input clocks at CLKInX/CLKInX* port. This configuration allows the noise of the external VCXO to dominate at low offset frequencies. Given that the noise of the external VCXO is far superior than the noise of PLL1, this setting produces a very clean reference clock to PLL2 at the OSCin port.

In order to achieve a LBW as low as 10 Hz at the supported VCXO frequency (1 MHz to 200 MHz), a range of charge pump currents in PLL1 is provided. The table below shows the available current gains. A small charge pump current is required to obtain a narrow LBW at high phase detector rate (small N value).

Table 19. PLL1 Charge Pump Current Selections (PLL1_CP_GAIN)

| PLL1_CP_GAIN [2:0] | | | PLL1 Charge Pump Current Magnitude (µA) |
|--------------------|----|----|---|
| b2 | b1 | b0 | |
| 0 | 0 | 0 | RESERVED |
| 0 | 0 | 1 | RESERVED |
| 0 | 1 | 0 | 20 |
| 0 | 1 | 1 | 80 |
| 1 | 0 | 0 | 25 |
| 1 | 0 | 1 | 50 |
| 1 | 1 | 0 | 100 |
| 1 | 1 | 1 | 400 |

The PLL1_CP_POL bit sets the PLL1 charge pump for operation with a positive or negative slope VCO/VCXO. A positive slope VCO/VCXO increases frequency with increased tuning voltage. A negative slope VCO/VCXO increases frequency with decreased tuning voltage.

Table 20. PLL1 Charge Pump Polarity Control Bits (PLL1_CP_POL)

| PLL1_CP_POL | DESCRIPTION |
|-------------|-------------------------|
| 0 | Negative Slope VCO/VCXO |
| 1 | Positive Slope VCO/VCXO |

REGISTER 13

EN_PLL2_XTAL: Crystal Oscillator Option Enable

If an external crystal is being used to implement a discrete VCXO, the internal feedback amplifier must be enabled in order to complete the oscillator circuit.

Table 21. EN_PLL2_XTAL: External Crystal Option

| EN_PLL2_XTAL | Oscillator Amplifier State |
|--------------|----------------------------|
| 0 | OFF |
| 1 | ON |

EN_Fout: Fout Power Down Bit

The EN_Fout bit allows the Fout port to be enabled or disabled. By default EN_Fout = 0.

CLK Global Enable: Clock Global enable bit

In addition to the external GOE pin, an internal Register 13 bit (b18) can be used to globally enable/disable the clock outputs via the uWire programming interface. The default value is 1. When CLK Global Enable = 1, the active output clocks are enabled. The active output clocks are disabled if this bit is 0.

POWERDOWN Bit -- Device Power Down

This bit can power down the entire device. Enabling this bit powers down the entire device and all functional blocks, regardless of the state of any of the other bits or pins.

Table 22. Power Down Bit Values

| POWERDOWN Bit | Mode |
|---------------|----------------------------|
| 0 | Normal Operation |
| 1 | Entire device powered down |

EN_PLL2_REF2X: PLL2 Frequency Doubler control bit

When F_{OSCin} is below 50 MHz, the PLL2 frequency doubler can be enabled by setting $\text{EN_PLL2_REF2X} = 1$. The default value is 0. When $\text{EN_PLL2_REF2X} = 1$, the signal at the OSCin port bypasses the PLL2_R counter and is passed through a frequency doubler circuit. The output of this circuit is then input to the PLL2 phase comparator block. This feature allows the phase comparison frequency to be increased for lower frequency OSCin sources (< 50 MHz), and can be used with either VXCOs or crystals. For instance, when using a pullable crystal of 12.288 MHz to drive the OSCin port, the PLL2 phase comparison frequency is 24.576 MHz when $\text{EN_PLL2_REF2X} = 1$. A higher PLL phase comparison frequency reduces PLL2 in-band phase noise and RMS jitter. The PLL in-band phase noise can be reduced by approximately 2 to 3 dB. The on-chip loop filter typically is enabled to reduce PLL2 reference spurs when EN_PLL2_REF2X is enabled. Suggested values in this case are: $R3 = 600 \Omega$, $C3 = 50 \text{ pF}$, $R4 = 10 \text{ k}\Omega$, $C4 = 60 \text{ pF}$.

PLL2 Internal Loop Filter Component Values

Internal loop filter components are available for PLL2, enabling the user to implement either 3rd or 4th order loop filters without requiring external components. The user may select from a fixed set of values for both the resistors and capacitors. Internal loop filter resistance values for R3 and R4 can be set individually according to *Table 20* and *Table 21*.

Table 23. PLL2 Internal Loop Filter Resistor Values, PLL2_R3_LF

| PLL2_R3_LF [2:0] | | | RESISTANCE |
|------------------|----|----|------------|
| b2 | b1 | b0 | |
| 0 | 0 | 0 | < 600 Ω |
| 0 | 0 | 1 | 10 kΩ |
| 0 | 1 | 0 | 20 kΩ |
| 0 | 1 | 1 | 30 kΩ |
| 1 | 0 | 0 | 40 kΩ |
| 1 | 0 | 1 | Invalid |
| 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | Invalid |

Table 24. PLL2 Internal Loop Filter Resistor Values, PLL2_R4_LF

| PLL2_R4_LF [2:0] | | | RESISTANCE |
|------------------|----|----|------------|
| b2 | b1 | b0 | |
| 0 | 0 | 0 | < 200 Ω |
| 0 | 0 | 1 | 10 kΩ |
| 0 | 1 | 0 | 20 kΩ |
| 0 | 1 | 1 | 30 kΩ |
| 1 | 0 | 0 | 40 kΩ |
| 1 | 0 | 1 | Invalid |
| 1 | 1 | 0 | Invalid |
| 1 | 1 | 1 | Invalid |

Internal loop filter capacitors for C3 and C4 can be set individually according to the following table.

Table 25. PLL2 Internal Loop Filter Capacitor Values

| PLL2_C3_C4_LF [3:0] | | | | Loop Filter Capacitance(pF) |
|---------------------|----|----|----|-----------------------------|
| b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | C3 = 0, C4 = 10 |
| 0 | 0 | 0 | 1 | C3 = 0, C4 = 60 |
| 0 | 0 | 1 | 0 | C3 = 50, C4 = 10 |
| 0 | 0 | 1 | 1 | C3 = 0, C4 = 110 |
| 0 | 1 | 0 | 0 | C3 = 50, C4 = 110 |
| 0 | 1 | 0 | 1 | C3 = 100, C4 = 110 |
| 0 | 1 | 1 | 0 | C3 = 0, C4 = 160 |
| 0 | 1 | 1 | 1 | C3 = 50, C4 = 160 |
| 1 | 0 | 0 | 0 | C3 = 100, C4 = 10 |
| 1 | 0 | 0 | 1 | C3 = 100, C4 = 60 |
| 1 | 0 | 1 | 0 | C3 = 150, C4 = 110 |
| 1 | 0 | 1 | 1 | C3 = 150, C4 = 60 |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

PLL1 CP TRI-STATE and PLL2 CP TRI-STATE

The charge pump output of either CPout1 or CPout2 may be placed in a TRI-STATE mode by setting the appropriate PLLx CP TRI-STATE bit.

Table 26. PLL1 Charge Pump TRI-STATE bit values

| PLL1 CP TRI-STATE | Description |
|-------------------|-----------------------------|
| 1 | PLL1 CPout1 is at TRI-STATE |
| 0 | PLL1 CPout1 is active |

Table 27. PLL2 Charge Pump TRI-STATE bit values

| PLL2 CP TRI-STATE | Description |
|-------------------|-----------------------------|
| 1 | PLL2 CPout2 is at TRI-STATE |
| 0 | PLL2 CPout2 is active |

REGISTER 14

OSCin_FREQ: PLL2 Oscillator Input Frequency Register

The frequency of the PLL2 reference input to the PLL2 Phase Detector (OSCin/OSCin* port) must be programmed in order to support proper operation of the internal VCO tuning algorithm. This is an 8-bit register that sets the frequency to the nearest 1-MHz increment.

Table 28. OSCin_FREQ Register Values

| OSCin_FREQ [7:0] | | | | | | | | VALUE |
|------------------|----|----|----|----|----|----|----|-----------|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Valid |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 MHz |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 MHz |
| . | . | . | . | . | . | . | . | ... |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 250 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Not Valid |
| . | . | . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Not Valid |

PLL2_R: PLL2_R Counter

The PLL2 R Counter is 12 bits wide. It divides the PLL2 OSCin/OSCin* clock and is connected to the PLL2 Phase Detector.

Table 29. PLL2_R: PLL2_R Counter Values

| R [11:0] | | | | | | | | | | | VALUE | |
|----------|-----|----|----|----|----|----|----|----|----|----|-------|-----------|
| b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Valid |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| . | . | . | . | . | . | . | . | . | . | . | . | ... |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4095 |

PLL_MUX: LD Pin Selectable Output

The signal appearing on the LD pin is programmable via the uWire interface and provides access to several internal signals which may be valuable for either status monitoring during normal operation or for debugging during the hardware development phase. This pin may be forced to either a HIGH or LOW state, and may also be configured as specified in *Table 27*.

Table 30. PLL_MUX: LD Pin Selectable Outputs

| PLL_MUX [4:0] | | | | | LD Output |
|---------------|----|----|----|----|--|
| b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | 0 | HiZ |
| 0 | 0 | 0 | 0 | 1 | Logic High |
| 0 | 0 | 0 | 1 | 0 | Logic Low |
| 0 | 0 | 0 | 1 | 1 | PLL2 Digital Lock Detect Active High |
| 0 | 0 | 1 | 0 | 0 | PLL2 Digital Lock Detect Active Low |
| 0 | 0 | 1 | 0 | 1 | PLL2 Analog Lock Detect Push Pull |
| 0 | 0 | 1 | 1 | 0 | PLL2 Analog Lock Detect Open Drain NMOS |
| 0 | 0 | 1 | 1 | 1 | PLL2 Analog Lock Detect Open Drain PMOS |
| 0 | 1 | 0 | 0 | 0 | Reserved |
| 0 | 1 | 0 | 0 | 1 | PLL2_N Divider Output / 2 |
| 0 | 1 | 0 | 1 | 0 | Reserved |
| 0 | 1 | 0 | 1 | 1 | PLL2_R Divider Output / 2 |
| 0 | 1 | 1 | 0 | 0 | Reserved |
| 0 | 1 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 1 | 0 | PLL1 Digital Lock Detect Active HIGH |
| 0 | 1 | 1 | 1 | 1 | PLL1 Digital Lock Detect Active LOW |
| 1 | 0 | 0 | 0 | 0 | Reserved |
| 1 | 0 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 0 | 1 | 1 | Reserved |
| 1 | 0 | 1 | 0 | 0 | PLL1_N Divider Output / 2 |
| 1 | 0 | 1 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 1 | 0 | PLL1_R Divider Output / 2 |
| 1 | 0 | 1 | 1 | 1 | PLL1 and PLL2 Digital Lock Detect |
| 1 | 1 | 0 | 0 | 0 | Inverted PLL1 and PLL2 Digital Lock Detect |
| 1 | 1 | 0 | 0 | 1 | Reserved |
| 1 | 1 | 0 | 1 | 0 | Reserved |
| 1 | 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | 1 | Reserved |

REGISTER 15

PLL2_N: PLL2_N Counter

The PLL2_N Counter is 18 bits wide. It divides the output of the VCO Divider and is connected to the PLL2 Phase Detector. Each time the PLL2_N Counter value is updated via the uWire interface, an internal algorithm is triggered that optimizes the VCO performance.

Table 31. PLL2_N: PLL2_N Counter Values

| N [17:0] | | | | | | | | | | VALUE |
|----------|-----|-----|----|----|----|----|----|----|----|-----------|
| b17 | b16 | ... | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0 | 0 | ... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Not Valid |
| 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| | | | . | . | . | . | . | . | . | ... |
| 1 | 1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 262143 |

PLL2_CP_GAIN: PLL2 Charge Pump Current and Output Control

The PLL2 charge pump output current level is controlled with the PLL2_CP_GAIN register. The following table presents the charge pump current control values.

Table 32. PLL2_CP_GAIN: PLL2 Charge Pump Current Selections

| PLL2_CP_GAIN [1:0] | | CP_TRI | Charge Pump Current (µA) |
|--------------------|----|--------|--------------------------|
| b1 | b0 | | |
| X | X | 1 | Hi-Z |
| 0 | 0 | 0 | 100 |
| 0 | 1 | 0 | 400 |
| 1 | 0 | 0 | 1600 |
| 1 | 1 | 0 | 3200 |

VCO_DIV: PLL2 VCO Divide Register

A divider is provided on the output of the PLL2 VCO to enable a wide range of output clock frequencies. The output of this divider is placed on the input path for the clock distribution section, which feeds each of the individual clock channels. The divider provides integer divide ratios from 2 to 8.

Table 33. VCO_DIV: PLL2 VCO Divider Values

| VCO_DIV [3:0] | | | | Divide Value |
|---------------|----|----|----|--------------|
| b3 | b2 | b1 | b0 | |
| 0 | 0 | 0 | 0 | Invalid |
| 0 | 0 | 0 | 1 | Invalid |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |

APPLICATION INFORMATION

SYSTEM LEVEL DIAGRAM

The following diagram illustrates the typical interconnection of the LMK041xx in a clocking application.

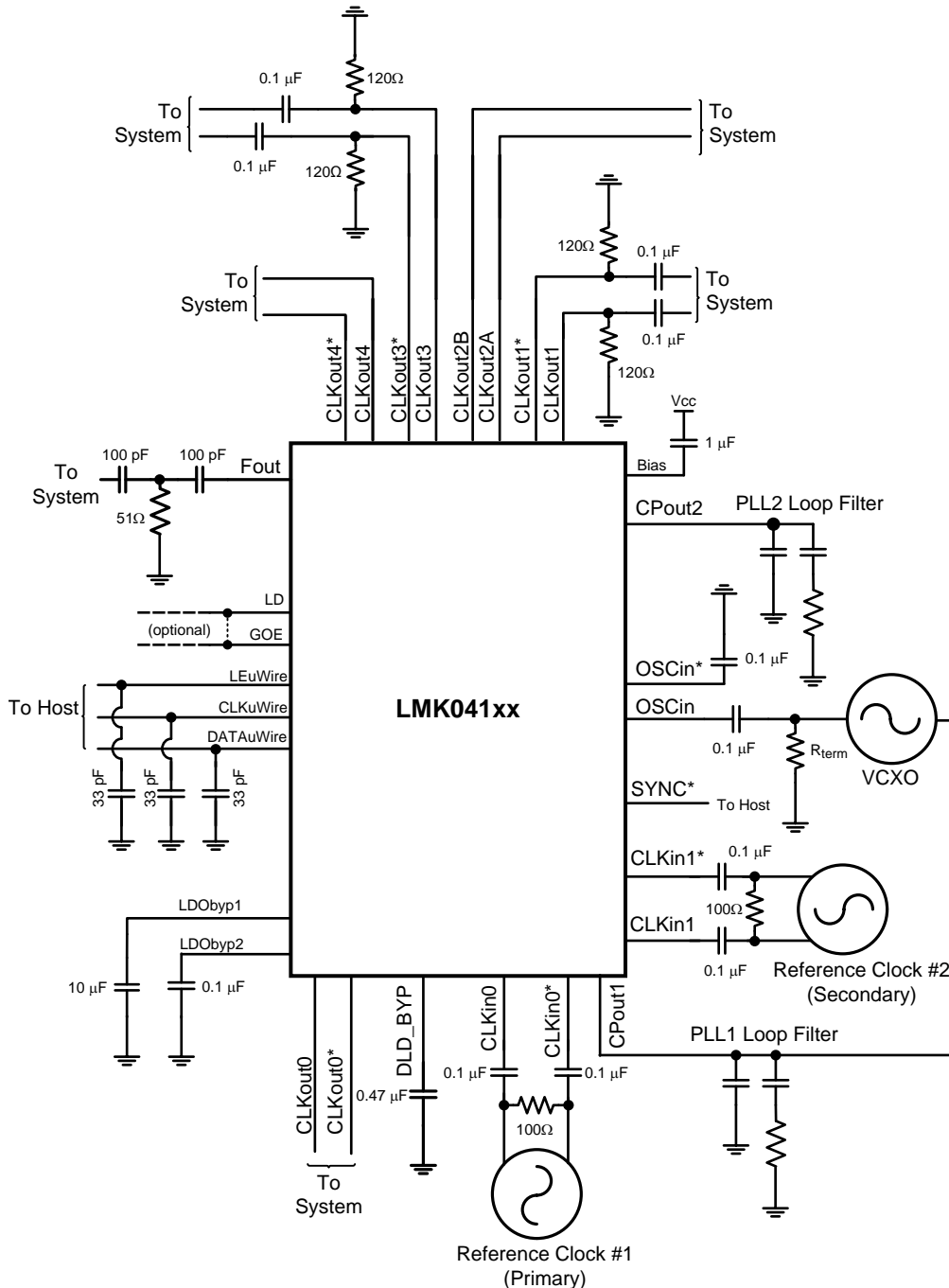


Figure 12. Typical Application

Figure 12 shows an LMK04100 family device with external circuitry. The primary reference clock input is at CLKin0/0*. A secondary reference clock is driving CLKin1/1*. Both clocks are depicted as AC coupled differential drivers. The VCXO attached to the OSCin/OSCin* port is configured as an AC coupled single-ended driver. Any of the input ports (CLKin0/0*, CLKin1/1*, or OSCin/OSCin*) may be configured as either differential or single-ended. These options are discussed later in the data sheet.

The diagram shows an optional connection between the LD pin and GOE. With this arrangement, the LD pin can be programmed to output a lock detect signal that is active HIGH (see Table 27 for optional LD pin outputs). If lock is lost, the LD pin will transition to a LOW, pulling GOE low and causing all clock outputs to be disabled. This scheme should be used only if disabling the clock outputs is desirable when lock is lost.

The loop filter for PLL2 consists of three external components that implement two lower order poles, plus optional internal integrated components if 3rd or 4th order poles are needed. The loop filter components for PLL1 must be external components.

The VCO output buffer signal that appears at the Fout pin when enabled (EN_Fout = 1) should be AC coupled using a 100 pF capacitor. This output is a single-ended signal by default. If a differential signal is required, a 50 Ω balun may be connected to this pin to convert it to differential.

The clock outputs are all AC coupled with 0.1 μ F capacitors. CLKout1 and CLKout3 are depicted as LVPECL, with 120 Ω emitter resistors as source termination. However, the output format of the clock channels will vary by device part number, so the designer should use the appropriate source termination for each channel. Later sections of this data sheet illustrate alternative methods for AC coupling, DC coupling and terminating the clock outputs.

LDO BYPASS AND BIAS PIN

The LDObyp1 and LDObyp2 pins should be connected to GND through external capacitors, as shown in the diagram. Furthermore, the Bias pin should be connected to V_{CC} through a 1 μ F capacitor in series.

LOOP FILTER

Each PLL of the LMK04100 family requires a dedicated loop filter. The loop filter for PLL1 must be connected to the CPout1 pin. [Figure 13](#) shows a simple 2-pole loop filter. The output of the filter drives an external VCXO module or discrete implementation of a VCXO using a crystal resonator. Higher order loop filters may be implemented using additional external R and C components. It is recommended the loop filter for PLL1 result in a total closed loop bandwidth in the range of 10 Hz to 200 Hz. The design of the loop filter is application specific and highly dependent on parameters such as the phase noise of the reference clock, VCXO phase noise, and phase detector frequency for PLL1. TI's Clock Conditioner Owner's Manual covers this topic in detail and TI's Clock Design Tool can be used to simulate loop filter designs for both PLLs. These resources may be found: http://www.ti.com/lscds/ti/analog/clocksandtimers/clocks_and_timers.page.

As shown in the diagram, the charge pump for PLL2 is directly connected to the optional internal loop filter components, which are normally used only if either a third or fourth pole is needed. The first and second poles are implemented with external components. The loop must be designed to be stable over the entire application-specific tuning range of the VCO. The designer should note the range of K_{VCO} listed in the table of Electrical Characteristics and how this value can change over the expected range of VCO tuning frequencies. Because loop bandwidth is directly proportional to K_{VCO} , the designer should model and simulate the loop at the expected extremes of the desired tuning range, using the appropriate values for K_{VCO} .

When designing with the integrated loop filter of the LMK04100 family, considerations for minimum resistor thermal noise often lead one to the decision to design for the minimum value for integrated resistors, R3 and R4. Both the integrated loop filter resistors and capacitors (C3 and C4) also restrict the maximum loop bandwidth. However, these integrated components do have the advantage that they are closer to the VCO and can therefore filter out some noise and spurs better than external components. For this reason, a common strategy is to minimize the internal loop filter resistors and then design for the largest internal capacitor values that permit a wide enough loop bandwidth. In situations where spurs requirements are very stringent and there is margin on phase noise, it might make sense to design for a loop filter with integrated resistor values larger than their minimum value.

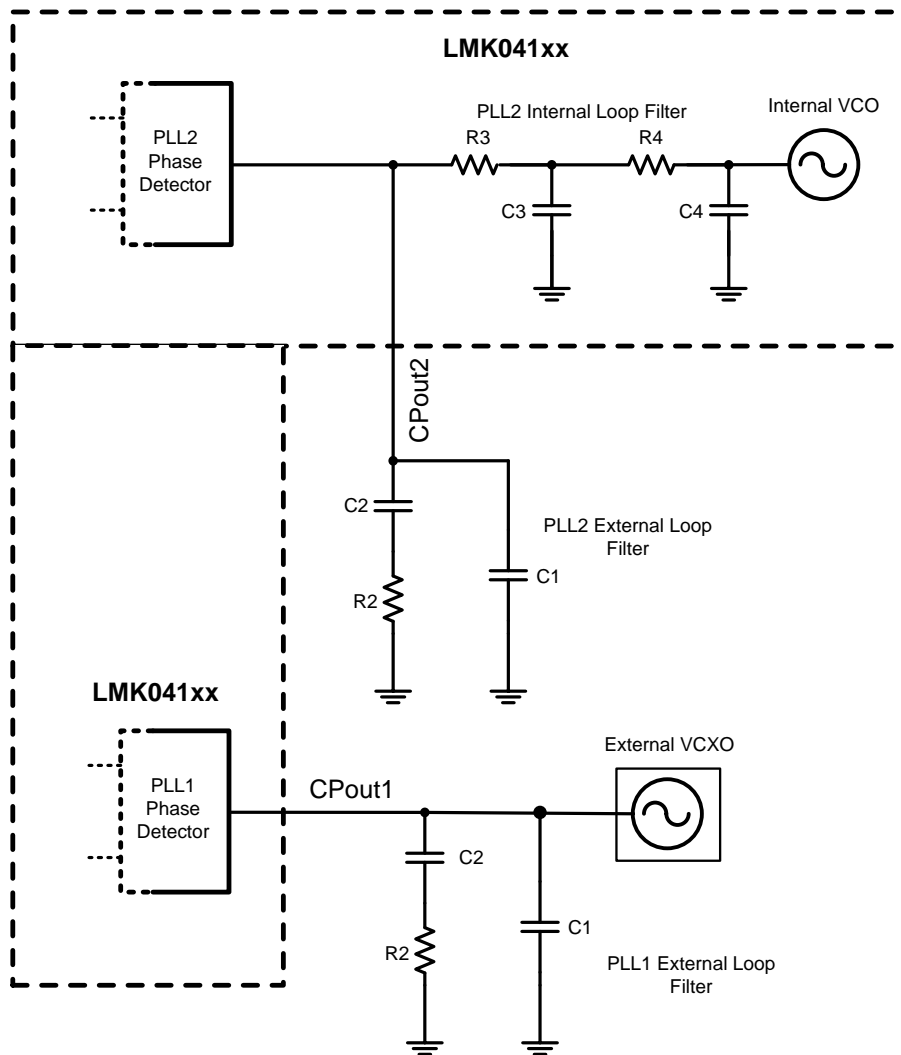


Figure 13. Loop Filter

Table 34. Typical Current Consumption for Selected Functional Blocks

| Block | Condition | Typical I_{CC} (Temp = 25 °C, $V_{CC} = 3.3$ V) (mA) | Power Dissipated in device (mW) | Power Dissipated in LVPECL/2VPECL Emitter Resistors (mW) |
|------------------------------|---|---|--|---|
| Entire device, core current | Single input clock (CLKIN_SEL = 0 or 1); LOS disabled; PLL1 and PLL2 locked; All CLKouts are off; No LVPECL emitter resistors connected | 115 | 380 | - |
| REFMUX | Enable auto-switch mode (CLKIN_SEL = 2 or 3) | 4.3 | 14 | - |
| LOS | Enable LOS (LOS_TYPE = 1, or 2, or 3) | 3.6 | 12 | - |
| Low Channel Internal Buffer | The low channel internal buffer is enabled when CLKout0 is enabled | 10 | 33 | - |
| High Channel Internal Buffer | The high channel internal buffer is enabled when one of CLKout1 through CLKout4 is enabled | 10 | 33 | - |
| Divide circuitry per output | Divider bypassed (CLKout_MUX = 0, 2) | 0 | 0 | - |
| | Divider enabled, divide = 2 (CLKout_MUX = 1, 3) | 5.3 | 17 | - |
| | Divider enabled, divide > 2 (CLKout_MUX = 1, 3) | 8.5 | 28 | - |

Table 34. Typical Current Consumption for Selected Functional Blocks (continued)

| Block | Condition | Typical I _{CC} (Temp = 25 °C, V _{CC} = 3.3 V) (mA) | Power Dissipated in device (mW) | Power Dissipated in LVPECL/2VPECL Emitter Resistors (mW) |
|--|---|---|--|---|
| Fout Buffer | EN_Fout = 1 | 14.5 | 48 | - |
| LVDS Buffer | LVDS buffer, enabled | 19.3 | 64 | - |
| LVPECL/2VPECL Buffer | LVPECL/2VPECL buffer (enabled and with 120 Ω emitter resistors) | 40 | 82 | 50 |
| | LVPECL/2VPECL buffer (disabled and with 120 Ω emitter resistors) | 21.7 | 47 | 25 |
| | LVPECL/2VPECL (disabled and with no emitter resistors) | 0 | 0 | - |
| LVCMOS Buffer (1) | LVCMOS buffer static I _{CC} , C _L = 5 pF | 4.5 | 15 | - |
| | LVCMOS buffer dynamic I _{CC} , C _L = 5 pF, CLKout = 100 MHz | 16 | 53 | - |
| Entire device (Single input clock (CLKIN_SEL = 0 or 1); LOS disabled; PLL1 and PLL2 locked; Fout disabled; All CLKouts are on); Divide > 2 on each output. | LMK0410x (2) (3) | 379.5 | 1102 | 150 |
| | LMK0411x (2) (3) | 377.5 | 996 | 250 |
| | LMK0413x (2) (3) | 337.1 | 1012 | 100 |

- (1) Dynamic power dissipation of LVCMOS buffer varies with output frequency and can be found in the LVCMOS dynamic I_{CC} vs frequency plot, as shown in [CLOCK OUTPUT AC CHARACTERISTICS](#). Total power dissipation of the LVCMOS buffer is the sum of static and dynamic power dissipation. CLKoutXa and CLKoutXb are each considered an LVCMOS buffer.
- (2) Assuming Theta_J = 27.4 °C/W, the total power dissipated on chip must be less than 40/27.4 = 1450 mW to guarantee a junction temperature is less than 125 °C.
- (3) Worst case power dissipation can be estimated by multiplying typical power dissipation with a factor of 1.2.

CURRENT CONSUMPTION / POWER DISSIPATION CALCULATIONS

Due to the myriad of possible configurations the following table serves to provide enough information to allow the user to calculate estimated current consumption of the device. Unless otherwise noted V_{CC} = 3.3 V, T_A = 25 °C.

From [Table 34](#) the current consumption can be calculated in any configuration. For example, the current for the entire device with 1 LVDS (CLKout0) & 1 LVPECL (CLKout1) output in bypassed mode can be calculated by adding up the following blocks: core current, clock buffer, one LVDS output buffer current, and one LVPECL output buffer current. There will also be one LVPECL output drawing emitter current, but some of the power from the current draw is dissipated in the external 120 Ω resistors which doesn't add to the power dissipation budget for the device. If dividers are switched in, then the additional current for these stages needs to be added as well.

For power dissipated by the device, the total current entering the device is multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs. If no emitter resistors are connected to the LVPECL outputs, this power will be 0 watts. For example, in the case of 1 LVDS (CLKout0) & 1 LVPECL (CLKout1) operating at 3.3 V, we calculate 3.3 V × (115 + 10 + 10 + 19.3 + 40) mA = 3.3 V × 194.3 mA = 641.2 mW. Because the LVPECL output (CLKout1) has the emitter resistors hooked up and the power dissipated by these resistors is 50 mW, the total device power dissipation is 641.2 mW - 50 mW = 591.2 mW.

When the LVPECL output is active, ~1.7 V is the average voltage on each output as calculated from the LVPECL V_{OH} & V_{OL} typical specification. Therefore the power dissipated in each emitter resistor is approximately (1.7 V)² / 120 Ω = 25 mW. When the LVPECL output is disabled, the emitter resistor voltage is ~1.07 V. Therefore the power dissipated in each emitter resistor is approximately (1.07 V)² / 120 Ω = 9.5 mW.

POWER SUPPLY CONDITIONING

The recommended technique for power supply management is to connect the power pins for the clock outputs (pins 13, 37, 40, 43, and 46) to a dedicated power plane and connect all other power pins on the device (pins 3, 8, 18, 19, 22, 24, 30, 31, and 33) to a second power plane. Note: the LMK04100 family has internal voltage regulators for the PLL and VCO blocks to provide noise immunity.

THERMAL MANAGEMENT

Power consumption of the LMK04100 family of devices can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in Figure 14. More information on soldering WQFN packages can be obtained: <http://www.ti.com/packaging>.

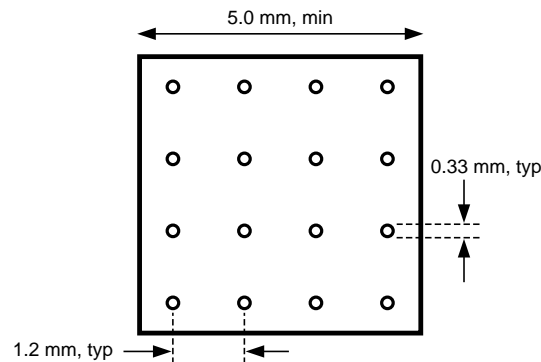


Figure 14. Recommended Land and Via Pattern

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in Figure 14 should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

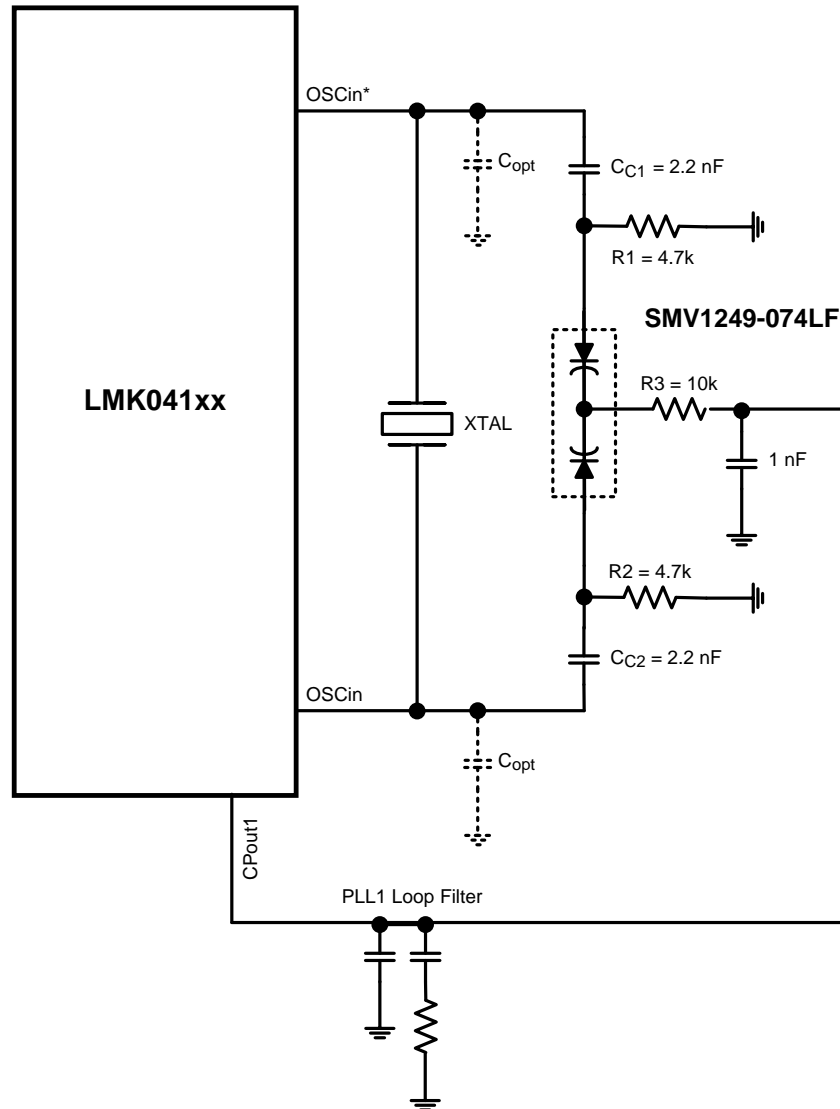


Figure 15. Reference Design Circuit for Crystal Oscillator Option

OPTIONAL CRYSTAL OSCILLATOR IMPLEMENTATION (OSCin/OSCin*)

The LMK04100 family features supporting circuitry for a discretely implemented oscillator driving the OSCin port pins. Figure 15 illustrates a reference design circuit for a crystal oscillator:

This circuit topology represents a parallel resonant mode oscillator design. When selecting a crystal for parallel resonance, the total load capacitance, C_L , must be specified. The load capacitance is the sum of the tuning capacitance (C_{TUNE}), the capacitance seen looking into the OSCin port (C_{IN}), and stray capacitance due to PCB parasitics (C_{STRAY}), and is given by:

$$C_L = C_{TUNE} + C_{IN} + \frac{C_{STRAY}}{2} \quad (1)$$

C_{TUNE} is provided by the varactor diode shown in Figure 15, Skyworks model SMV1249-074. A dual diode package with common cathode provides the variable capacitance for tuning. The single diode capacitance ranges from approximately 31 pF at 0.3 V to 3.4 pF at 3 V. The capacitance range of the dual package (anode to anode) is approximately 15.5 pF at 3 V to 1.7 pF at 0.3 V. The desired value of V_{TUNE} applied to the diode should be $V_{CC}/2$, or 1.65 V for $V_{CC} = 3.3$ V. The typical performance curve from the data sheet for the SMV1249-074 indicates that the capacitance at this voltage is approximately 6 pF (12 pF/2).

The nominal input capacitance (C_{IN}) of the LMK04100 family OSCin pins is 6 pF. The stray capacitance (C_{STRAY}) of the PCB should be minimized by arranging the oscillator circuit layout to achieve trace lengths as short as possible and as narrow as possible trace width (50 Ω characteristic impedance is not required). As an example, assume that C_{STRAY} is 4 pF. The total load capacitance is nominally:

$$C_L = 6 + 6 + \frac{4}{2} = 14 \text{ pF} \quad (2)$$

Consequently the load capacitance specification for the crystal in this case should be nominally 14 pF.

The 2.2 nF capacitors shown in the circuit are coupling capacitors that block the DC tuning voltage applied by the 4.7 k and 10 k resistors. The value of these coupling capacitors should be large, relative to the value of C_{TUNE} ($C_{C1} = C_{C2} \gg C_{TUNE}$), so that C_{TUNE} becomes the dominant capacitance.

For a specific value of C_L , the corresponding resonant frequency (F_L) of the parallel resonant mode circuit is:

$$F_L = F_S \cdot \left\{ \frac{C_1}{2(C_0 + C_{L1})} + 1 \right\} = F_S \cdot \left\{ \frac{1}{2 \left(\frac{C_0}{C_1} + \frac{C_L}{C_1} \right)} + 1 \right\} \quad (3)$$

F_S = Series resonant frequency

C_1 = Motional capacitance of the crystal

C_L = Load capacitance

C_0 = Shunt capacitance of the crystal, specified on the crystal datasheet

The normalized tuning range of the circuit is closely approximated by:

$$\frac{\Delta F}{F} = \frac{F_{CL1} - F_{CL2}}{F_{CL1}} = \frac{C_1}{2} \cdot \left\{ \frac{1}{(C_0 + C_{L1})} - \frac{1}{(C_0 + C_{L2})} \right\} = \frac{1}{2} \cdot \left\{ \frac{1}{\left(\frac{C_0}{C_1} + \frac{C_{L1}}{C_1} \right)} - \frac{1}{\left(\frac{C_0}{C_1} + \frac{C_{L2}}{C_1} \right)} \right\} \quad (4)$$

C_{L1} , C_{L2} = The endpoints of the circuit's load capacitance range, assuming a variable capacitance element is one component of the load. F_{CL1} , F_{CL2} = parallel resonant frequencies at the extremes of the circuit's load capacitance range.

A common range for the pullability ratio, C_0/C_1 , is 250 to 280. The ratio of the load capacitance to the shunt capacitance is $\sim(n * 1000)$, $n < 10$. Hence, picking a crystal with a smaller pullability ratio supports a wider tuning range because this allows the scale factors related to the load capacitance to dominate.

Example crystal specifications are presented in [Table 35](#).

Table 35. Example Crystal Specifications

| Parameter | Value |
|---------------------------------------|--------------------------|
| Nominal Frequency (MHz) | 12.288 |
| Frequency Stability, T = 25 °C | ± 10 ppm |
| Operating temperature range | -40 °C to +85 °C |
| Frequency Stability, -40 °C to +85 °C | ± 15 ppm |
| Load Capacitance | 14 pF |
| Shunt Capacitance (C_0) | 5 pF Maximum |
| Motional Capacitance (C_1) | 20 fF ± 30% |
| Equivalent Series Resistance | 25 Ω Maximum |
| Drive level | 2 mWatts Maximum |
| C_0/C_1 ratio | 225 typical, 250 Maximum |

See [Figure 16](#) for a representative tuning curve.

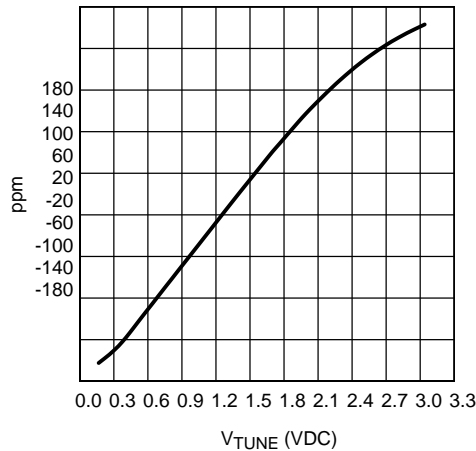


Figure 16. Example Tuning Curve, 12.288 MHz Crystal

The tuning curve achieved in the user's application may differ from the curve shown above due to differences in PCB layout and component selection.

This data is measured on the bench with the crystal integrated with the LMK04100 family. Using a voltmeter to monitor the V_{TUNE} node for the crystal, the PLL1 reference clock input frequency is swept in frequency and the resulting tuning voltage generated by PLL1 is measured at each frequency. At each value of the reference clock frequency, the lock state of PLL1 should be monitored to ensure that the tuning voltage applied to the crystal is valid.

The curve shows over the tuning voltage range of 0.17 VDC to 3.0 VDC, the frequency range is ± 163 ppm; or equivalently, a tuning range of ± 2000 Hz. The measured tuning voltage at the nominal crystal frequency (12.288 MHz) is 1.4 V. Using the diode data sheet tuning characteristics, this voltage results in a tuning capacitance of approximately 6.5 pF.

The tuning curve data can be used to calculate the gain of the oscillator (K_{VCO}). The data used in the calculations is taken from the most linear portion of the curve, a region centered on the crossover point at the nominal frequency (12.288 MHz). For a well designed circuit, this is the most likely operating range. In this case, the tuning range used for the calculations is ± 1000 Hz (± 0.001 MHz), or ± 81.4 ppm. The simplest method is to calculate the ratio:

$$K_{VCO} = \frac{\Delta F}{\Delta V} = \left(\frac{\Delta F_2 - \Delta F_1}{V_{TUNE2} - V_{TUNE1}} \right), \frac{\text{MHz}}{\text{V}} \quad (5)$$

ΔF₂ and ΔF₁ are in units of MHz. Using data from the curve this becomes:

$$\frac{0.001 - (-0.001)}{2.03 - 0.814} = 0.00164 \frac{\text{MHz}}{\text{V}} \quad (6)$$

A second method uses the tuning data in units of ppm:

$$K_{VCO} = \frac{F_{NOM} \cdot (\Delta \text{ppm}_2 - \Delta \text{ppm}_1)}{\Delta V \cdot 10^6} \quad (7)$$

F_{NOM} is the nominal frequency of the crystal and is in units of MHz. Using the data, this becomes:

$$\frac{12.288 \cdot (81.4 - (-81.4))}{(2.03 - 0.814) \cdot 10^6} = 0.00164, \frac{\text{MHz}}{\text{V}} \quad (8)$$

In order to ensure startup of the oscillator circuit, the equivalent series resistance (ESR) of the selected crystal should conform to the specifications listed in the table of Electrical Characteristics. It is also important to select a crystal with adequate power dissipation capability, or *drive level*. If the drive level supplied by the oscillator exceeds the maximum specified by the crystal manufacturer, the crystal will undergo excessive aging and possibly become damaged. Drive level is directly proportional to resonant frequency, capacitive load seen by the crystal, voltage and equivalent series resistance (ESR).

For more complete coverage of crystal oscillator design, see Application Note AN-1939: [SNAA065](#).

ADDITIONAL OUTPUTS WITH AN LMK04100 FAMILY DEVICE

The number of outputs on a LMK04100 family device can be expanded in many ways. The first method is to use the differential outputs as two single-ended outputs. For CMOS outputs, both the positive and negative outputs can be programmed to be in phase, or 180 degrees out of phase. LVDS/LVPECL positive and negative outputs are always 180 degrees out of phase. LVDS single-ended is not recommended.

In addition to this technique, the number of outputs can be expanded with a LMK01000 family device. To do this, one of the clock outputs of a LMK04100 can drive the LMK01000 device.

For more information on phase synchronization with multiple devices, please refer to application note AN-1864: [SNAA060](#).

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LMK04100SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04100 |
| LMK04100SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04100 |
| LMK04100SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04100 |
| LMK04101SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04101 |
| LMK04101SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04101 |
| LMK04101SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04101 |
| LMK04102SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04102 |
| LMK04102SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04102 |
| LMK04102SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04102 |
| LMK04110SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04110 |
| LMK04110SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04110 |
| LMK04110SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04110 |
| LMK04111SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04111 |
| LMK04111SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04111 |
| LMK04111SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04111 |
| LMK04131SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04131 |
| LMK04131SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04131 |
| LMK04131SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04131 |
| LMK04133SQ/NOPB | Active | Production | WQFN (RHS) 48 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04133 |
| LMK04133SQE/NOPB | Active | Production | WQFN (RHS) 48 | 250 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04133 |
| LMK04133SQX/NOPB | Active | Production | WQFN (RHS) 48 | 2500 LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 85 | LMK04133 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

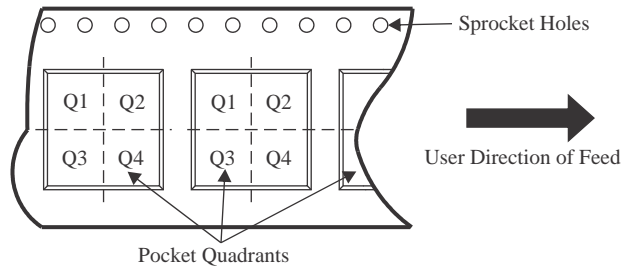
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK04100SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04100SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04100SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04101SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04101SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04101SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04102SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04102SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04102SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04110SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04110SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04110SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04111SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04111SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04111SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04131SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

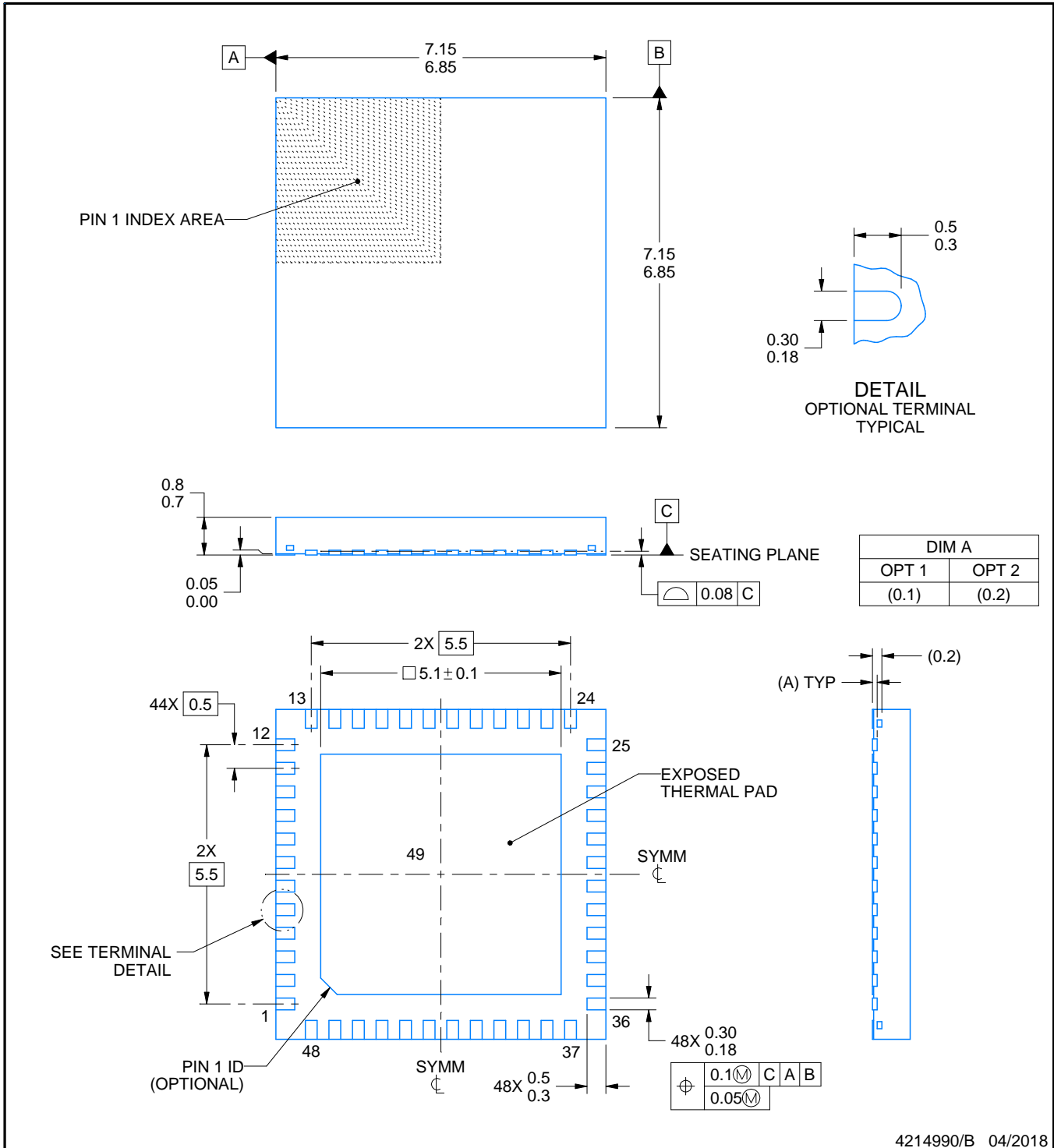
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMK04131SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04131SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04133SQ/NOPB | WQFN | RHS | 48 | 1000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04133SQE/NOPB | WQFN | RHS | 48 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| LMK04133SQX/NOPB | WQFN | RHS | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK04100SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04100SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04100SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |
| LMK04101SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04101SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04101SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |
| LMK04102SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04102SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04102SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |
| LMK04110SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04110SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04110SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |
| LMK04111SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04111SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04111SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |
| LMK04131SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04131SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04131SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMK04133SQ/NOPB | WQFN | RHS | 48 | 1000 | 356.0 | 356.0 | 36.0 |
| LMK04133SQE/NOPB | WQFN | RHS | 48 | 250 | 208.0 | 191.0 | 35.0 |
| LMK04133SQX/NOPB | WQFN | RHS | 48 | 2500 | 356.0 | 356.0 | 36.0 |



4214990/B 04/2018

NOTES:

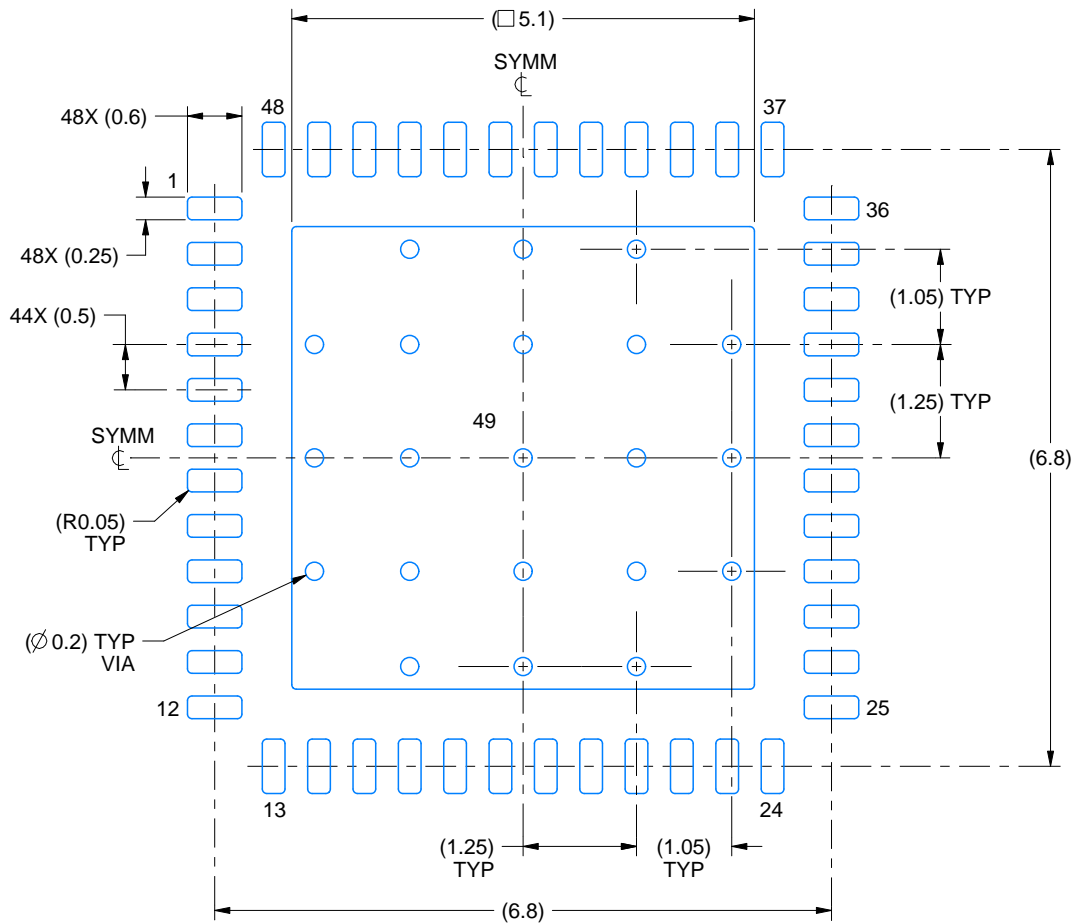
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

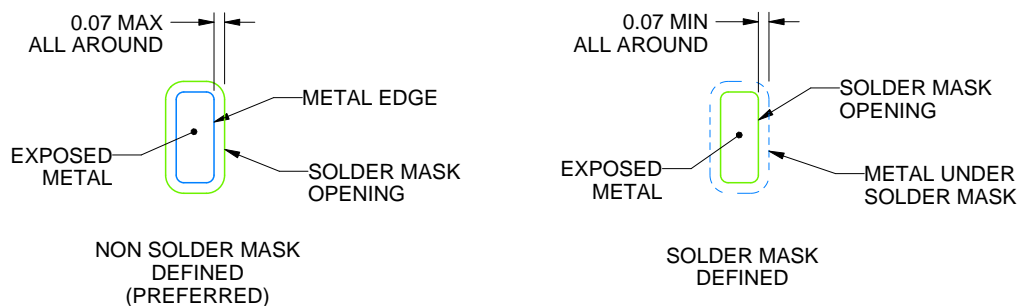
RHS0048A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4214990/B 04/2018

NOTES: (continued)

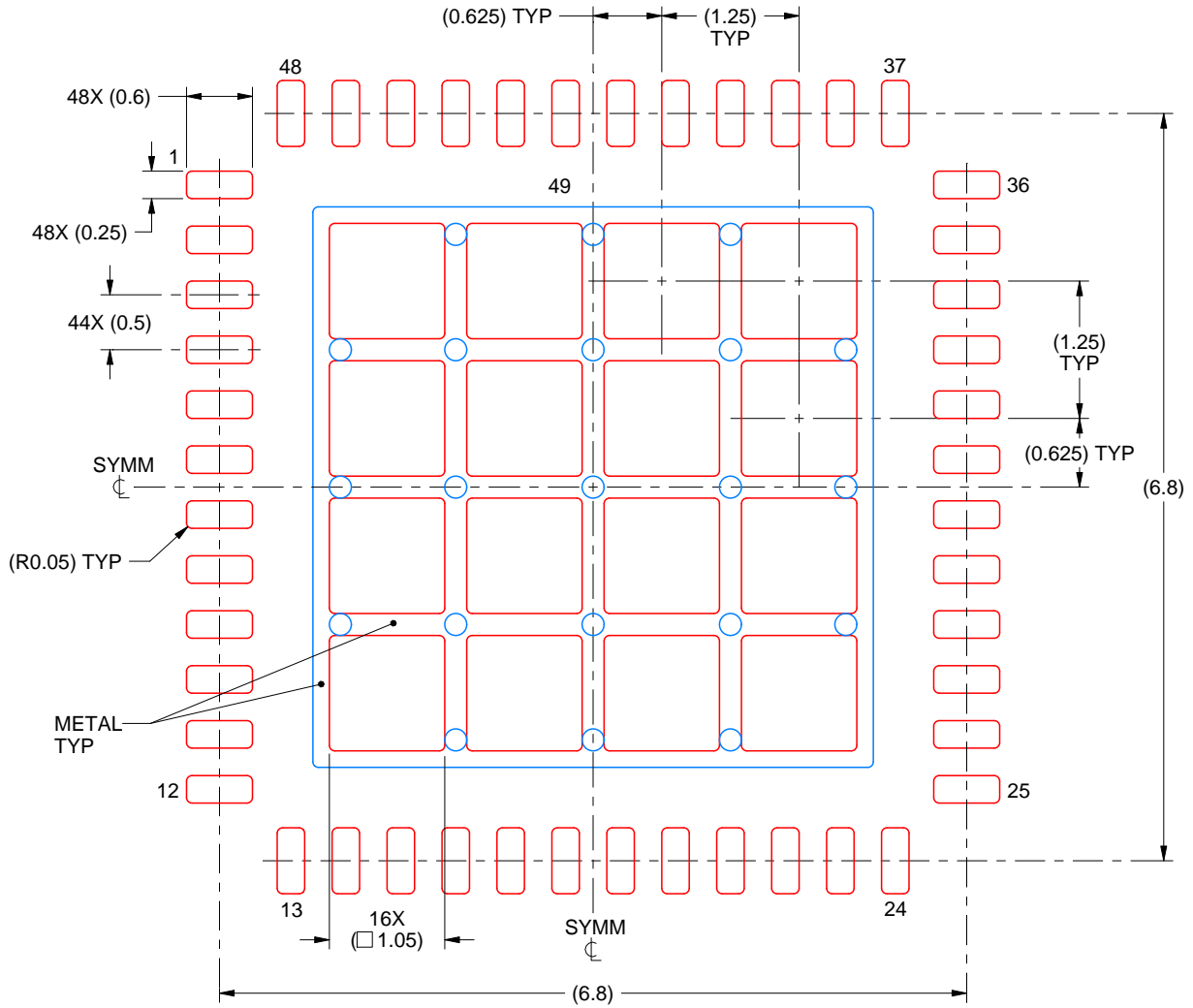
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHS0048A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated