

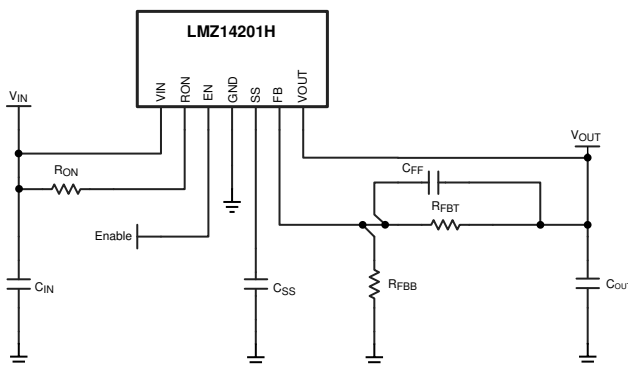
LMZ14201H SIMPLE SWITCHER® 6V~42V、1A 高出力電圧パワー・モジュール

1 特長

- シールド付きインダクタを内蔵
- シンプルな PCB レイアウト
- 外部のソフトスタートと高精度イネーブルによる柔軟なスタートアップ・シーケンシング
- 突入電流からの保護
- 入力 UVLO および出力短絡保護
- 40°C~125°Cの接合部温度範囲
- 単一の露出パッドと標準ピン配置により取り付けと製造が容易
- 低出力電圧リップル
- ピン単位で互換性のあるファミリ:
 - LMZ14203H/2H/1H (最大 42V、3A、2A、1A)
 - LMZ14203/2/1 (最大 42V、3A、2A、1A)
 - LMZ12003/2/1 (最大 20V、3A、2A、1A)
- WEBENCH® Power Designer に完全に対応しています
- 電気的特性
 - 最大 1A の出力電流
 - 入力電圧範囲: 6V~42V
 - 出力電圧を最小 5V まで調整可能
 - 最大効率 97%
- 性能上の利点
 - 高い効率によりシステムの発熱が減少
 - 補償不要
 - 低いパッケージ熱抵抗
 - 低放射 EMI (EN 55022 クラス B テスト済み)¹

2 アプリケーション

- 12V と 24V の各レールへの中間バス変換
- 時間に制約のあるプロジェクト
- スペースに制限があり、熱の要件が厳しいアプリケーション
- 負出力電圧アプリケーション



アプリケーション概略回路図

3 概要

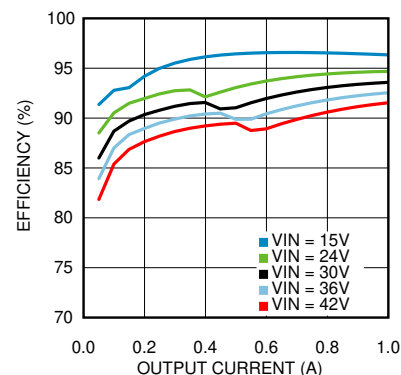
LMZ14201H SIMPLE SWITCHER® パワー・モジュールは使いやすい降圧型 DC/DC ソリューションで、非常に優れた電力変換効率、ラインおよび負荷レギュレーション、出力精度で、最大 1A の負荷を駆動できます。LMZ14201H の革新的なパッケージは、熱特性を強化するとともに、人手でも機械でもハンダ付けできます。

LMZ14201H は 6V~42V の入力電圧レールを受け付け、最低 5V の高精度かつ可変の出力電圧を供給します。LMZ14201H は、わずか 3 つの外付け抵抗と 4 つの外付けコンデンサだけで、完全な電源ソリューションを構築できます。LMZ14201H は信頼性が高く堅牢な設計で、サーマル・シャットダウン、入力低電圧誤動作防止、出力過電圧保護、短絡保護、出力電流制限の保護機能が搭載されており、プリバイアス出力へのスタートアップが可能です。スイッチング周波数は、1 つの抵抗により最大 1MHz に調整できます。

製品情報

部品番号 ⁽²⁾	パッケージ ⁽¹⁾	本体サイズ (公称)
LMZ14201H	TO-PMOD (7)	10.16mm × 9.85mm

- 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- ピーク・リフロー温度は 245°C です。詳細については、[SNAA214](#) を参照してください。



効率 V_{OUT} = 12V, T_A = 25°C

¹ EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007.



Table of Contents

1 特長	1	8 Application and Implementation	17
2 アプリケーション	1	8.1 Application Information.....	17
3 概要	1	8.2 Typical Application.....	17
4 Revision History	2	9 Power Supply Recommendations	22
5 Pin Configuration and Functions	3	10 Layout	23
6 Specifications	4	10.1 Layout Guidelines.....	23
6.1 Absolute Maximum Ratings.....	4	10.2 Layout Example.....	24
6.2 ESD Ratings.....	4	11 Device and Documentation Support	27
6.3 Recommended Operating Conditions.....	4	11.1 Documentation Support.....	27
6.4 Thermal Information.....	4	11.2 Receiving Notification of Documentation Updates..	27
6.5 Electrical Characteristics.....	5	11.3 サポート・リソース.....	27
6.6 Typical Characteristics.....	7	11.4 Trademarks.....	27
7 Detailed Description	15	11.5 Electrostatic Discharge Caution.....	27
7.1 Overview.....	15	11.6 Glossary.....	27
7.2 Functional Block Diagram.....	15	12 Mechanical, Packaging, and Orderable	
7.3 Feature Description.....	15	Information	27
7.4 Device Functional Modes.....	16		

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (October 2015) to Revision I (August 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新.....	1
• Updated 式 17	21

Changes from Revision G (August 2015) to Revision H (October 2015)	Page
• Added this new bullet in the Power Module SMT Guidelines section.....	23

5 Pin Configuration and Functions

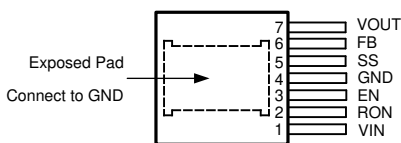


图 5-1. NDW Package 7-Pin TO-PMD (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	Power	Supply input — Additional external input capacitance is required between this pin and the exposed pad (EP).
2	RON	Analog	ON-time resistor — An external resistor from V_{IN} to this pin sets the ON-time and frequency of the application. Typical values range from 100 k Ω to 700 k Ω .
3	EN	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.18 V.
4	GND	Ground	Ground — Reference point for all stated voltages. Must be externally connected to EP.
5	SS	Analog	Soft-Start — An internal 8 μ A current source charges an external capacitor to produce the soft-start function.
6	FB	Analog	Feedback — Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connect the feedback resistor divider between the output and ground to set the output voltage.
7	VOUT	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and the EP.
—	EP	Ground	Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

	MIN	MAX	UNIT
V _{IN} , RON to GND	−0.3	43.5	V
EN, FB, SS to GND	−0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 sec)		245	°C
Storage Temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) For soldering specifications, refer to the following document: [SNOA549](#)

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V _{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMZ14201H	UNIT
		NDW (TO-PMD)	
		7 PINS	
R _{θJA} Junction-to-ambient thermal resistance	4 layer printed-circuit-board, 7.62 cm x 7.62 cm (3 in x 3 in) area, 1 oz copper, no air flow	16	°C/W
	4 layer printed-circuit-board, 6.35 cm x 6.35 cm (2.5 in x 2.5 in) area, 1 oz copper, no air flow	18.4	
R _{θJC(top)} Junction-to-case (top) thermal resistance		1.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$, $R_{ON} = 249\text{ k}\Omega$

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
SYSTEM PARAMETERS						
ENABLE CONTROL						
V_{EN}	EN threshold trip point	V_{EN} rising, $T_J = -40^\circ\text{C}$ to 125°C	1.10	1.18	1.25	V
V_{EN-HYS}	EN threshold hysteresis			90		mV
SOFT-START						
I_{SS}	SS source current	$V_{SS} = 0\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C	8	10	15	μA
I_{SS-DIS}	SS discharge current			-200		μA
CURRENT LIMIT						
I_{CL}	Current limit threshold	DC average, $T_J = -40^\circ\text{C}$ to 125°C	1.5	1.95	2.7	A
VIN UVLO						
V_{INUVLO}	Input UVLO	EN pin floating V_{IN} rising		3.75		V
$V_{INUVLO-HYST}$	Hysteresis	EN pin floating V_{IN} falling		130		mV
ON/OFF TIMER						
t_{ON-MIN}	ON timer minimum pulse width			150		ns
t_{OFF}	OFF timer pulse width			260		ns
REGULATION AND OVERVOLTAGE COMPARATOR						
V_{FB}	In-regulation feedback voltage	$V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$ $V_{SS} > +0.8\text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C $I_{OUT} = 10\text{ mA}$ to 1 A	0.782	0.803	0.822	V
		$V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$ $V_{SS} > +0.8\text{ V}$ $T_J = 25^\circ\text{C}$ $I_{OUT} = 10\text{ mA}$ to 1 A	0.786	0.803	0.818	
V_{FB}	In-regulation feedback voltage	$V_{IN} = 36\text{ V}$, $V_{OUT} = 24\text{ V}$ $V_{SS} > +0.8\text{ V}$ $T_J = -40^\circ\text{C}$ to 125°C $I_{OUT} = 10\text{ mA}$ to 1 A	0.780	0.803	0.823	V
		$V_{IN} = 36\text{ V}$, $V_{OUT} = 24\text{ V}$ $V_{SS} > +0.8\text{ V}$ $T_J = 25^\circ\text{C}$ $I_{OUT} = 10\text{ mA}$ to 1 A	0.787	0.803	0.819	
V_{FB-OVP}	Feedback overvoltage protection threshold			0.92		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non-Switching Input Current	$V_{FB} = 0.86\text{ V}$		1		mA
I_{SD}	Shut Down Quiescent Current	$V_{EN} = 0\text{ V}$		25		μA
THERMAL CHARACTERISTICS						
T_{SD}	Thermal shutdown (rising)				165	$^\circ\text{C}$
$T_{SD-HYST}$	Thermal shutdown hysteresis				15	$^\circ\text{C}$
PERFORMANCE PARAMETERS						
ΔV_{OUT}	Output Voltage Ripple	$V_{OUT} = 5\text{ V}$, $C_{OUT} = 100\text{ }\mu\text{F}$ 6.3 V X7R		8		mV _{PP}
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{IN} = 16\text{ V}$ to 42 V , $I_{OUT} = 1\text{ A}$		0.01%		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$V_{IN} = 24\text{ V}$, $I_{OUT} = 0\text{ A}$ to 1 A		1.5		mV/A
η	Efficiency	$V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$, $I_{OUT} = 0.5\text{ A}$		94%		

Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$, $R_{ON} = 249\text{ k}\Omega$

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX ⁽¹⁾	UNIT
η	Efficiency	$V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$, $I_{OUT} = 1\text{ A}$		92%		

- (1) Minimum and Maximum limits are 100% production tested at 25°C . Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at 25°C and represent the most likely parametric norm.

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.

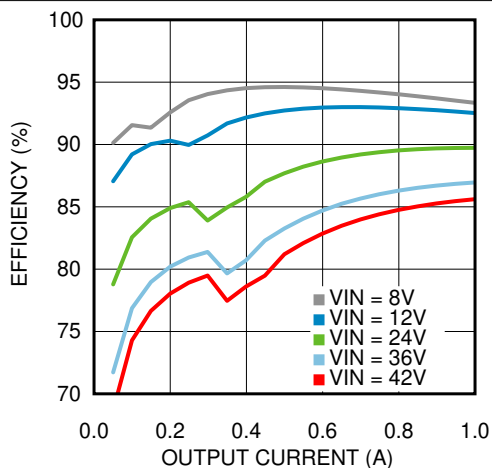


FIG 6-1. Efficiency $V_{OUT} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

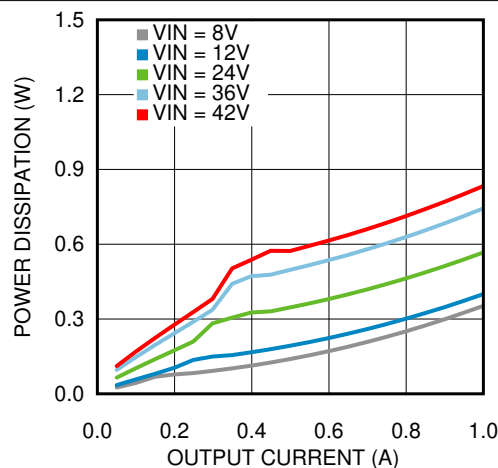


FIG 6-2. Power Dissipation $V_{OUT} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

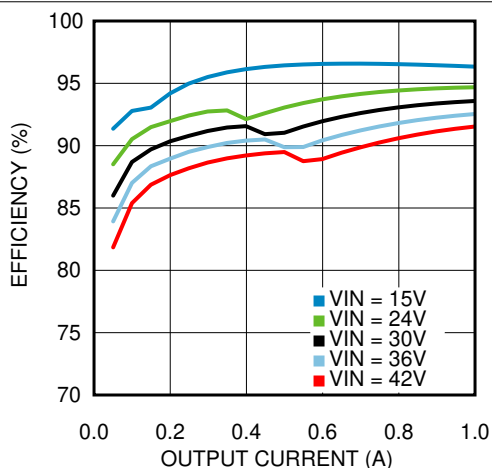


FIG 6-3. Efficiency $V_{OUT} = 12\text{ V}$, $T_A = 25^\circ\text{C}$

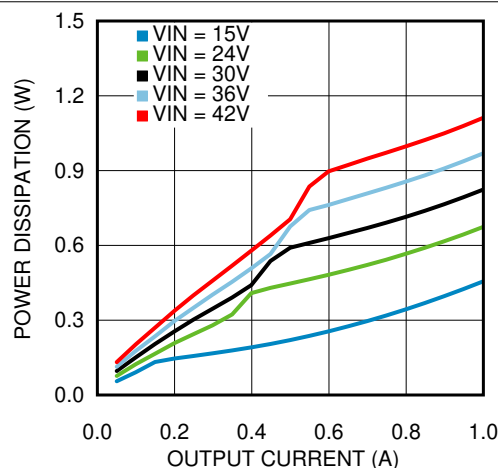


FIG 6-4. Power Dissipation $V_{OUT} = 12\text{ V}$, $T_A = 25^\circ\text{C}$

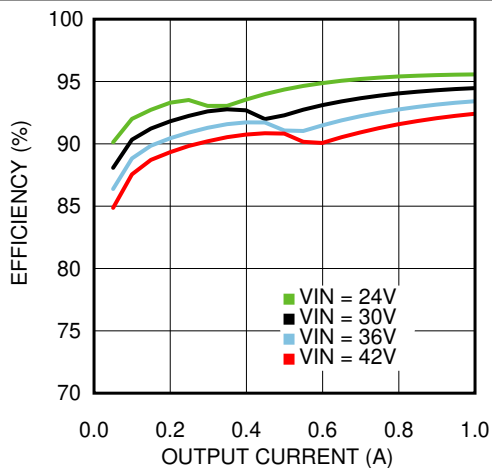


FIG 6-5. Efficiency $V_{OUT} = 15\text{ V}$, $T_A = 25^\circ\text{C}$

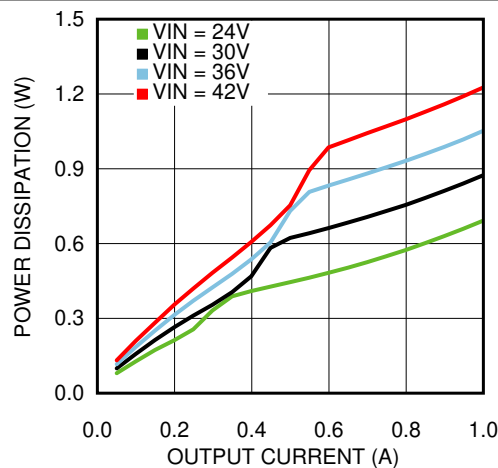


FIG 6-6. Power Dissipation $V_{OUT} = 15\text{ V}$, $T_A = 25^\circ\text{C}$

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.

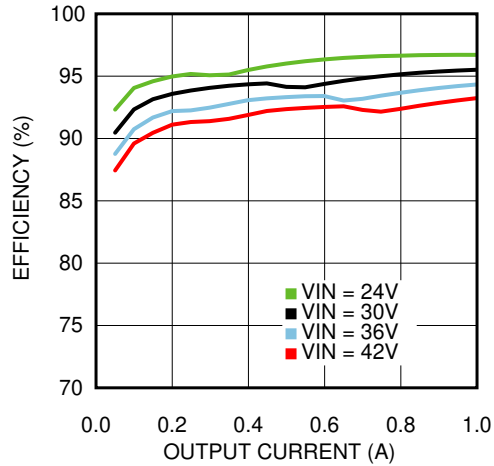


FIG 6-7. Efficiency $V_{OUT} = 18\text{ V}$, $T_A = 25^\circ\text{C}$

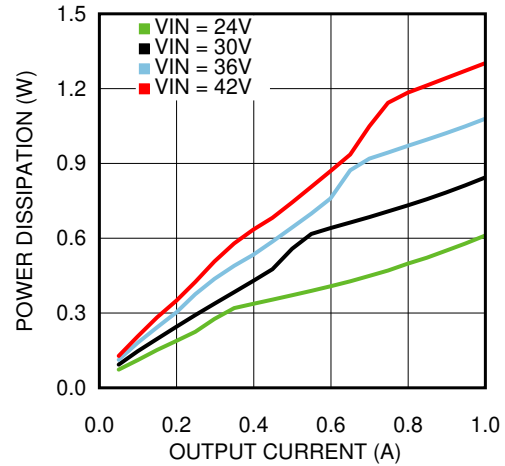


FIG 6-8. Power Dissipation $V_{OUT} = 18\text{ V}$, $T_A = 25^\circ\text{C}$

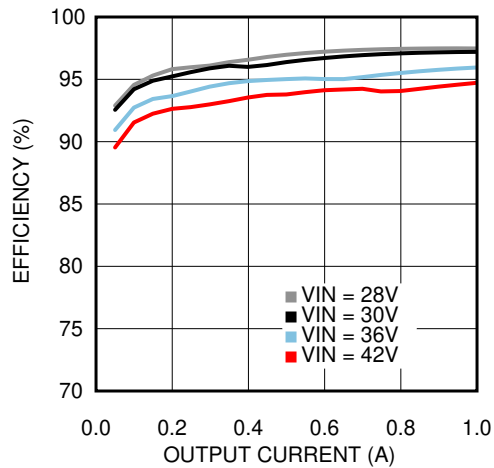


FIG 6-9. Efficiency $V_{OUT} = 24\text{ V}$, $T_A = 25^\circ\text{C}$

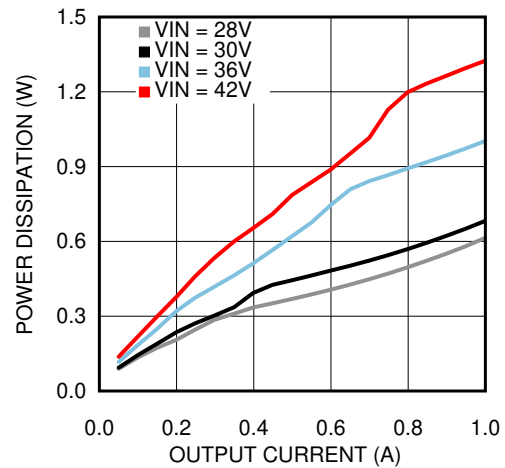


FIG 6-10. Power Dissipation $V_{OUT} = 24\text{ V}$, $T_A = 25^\circ\text{C}$

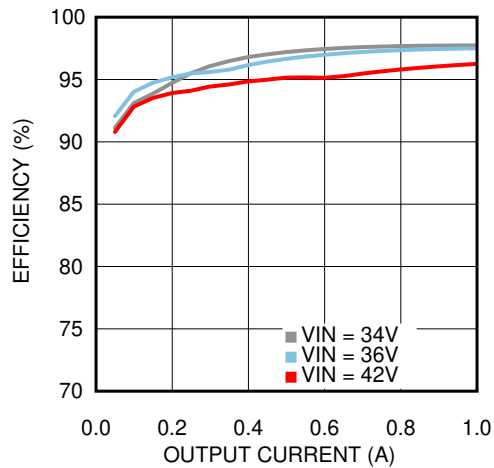


FIG 6-11. Efficiency $V_{OUT} = 30\text{ V}$, $T_A = 25^\circ\text{C}$

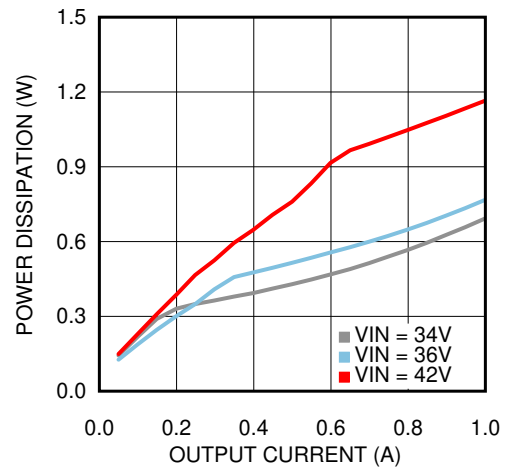


FIG 6-12. Power Dissipation $V_{OUT} = 30\text{ V}$, $T_A = 25^\circ\text{C}$

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.

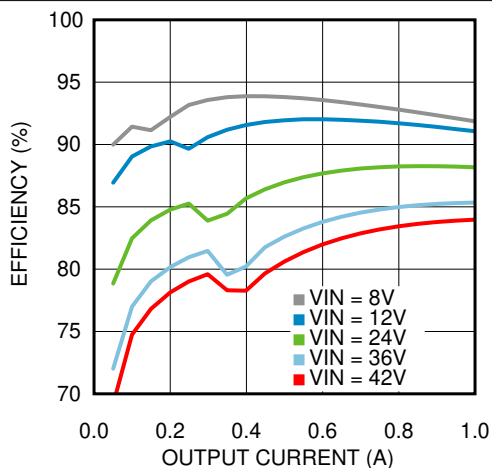


FIG 6-13. Efficiency $V_{OUT} = 5\text{ V}$, $T_A = 85^\circ\text{C}$

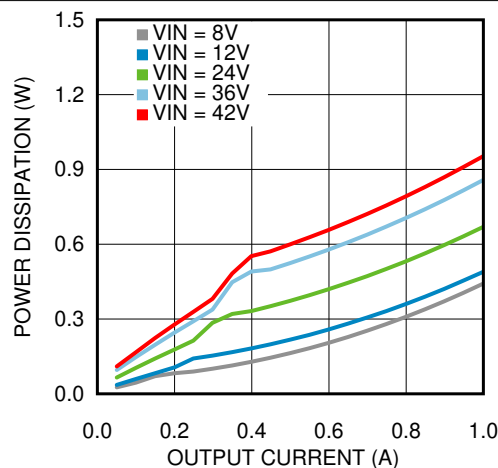


FIG 6-14. Power Dissipation $V_{OUT} = 5\text{ V}$, $T_A = 85^\circ\text{C}$

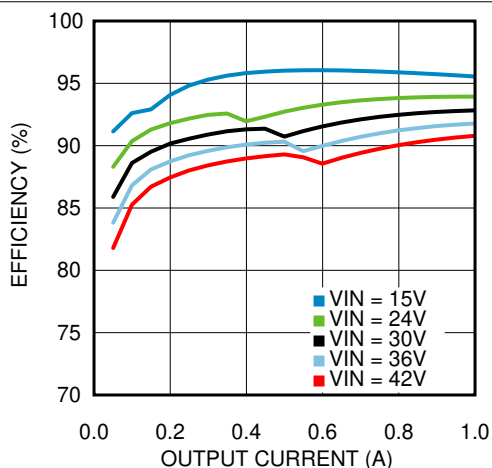


FIG 6-15. Efficiency $V_{OUT} = 12\text{ V}$, $T_A = 85^\circ\text{C}$

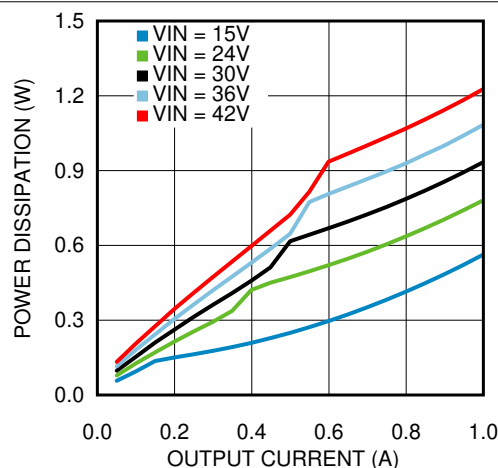


FIG 6-16. Power Dissipation $V_{OUT} = 12\text{ V}$, $T_A = 85^\circ\text{C}$

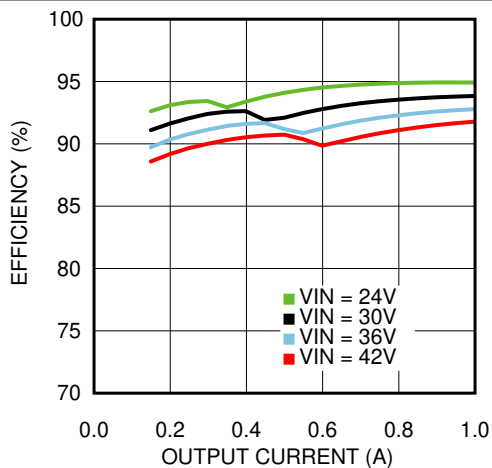


FIG 6-17. Efficiency $V_{OUT} = 15\text{ V}$, $T_A = 85^\circ\text{C}$

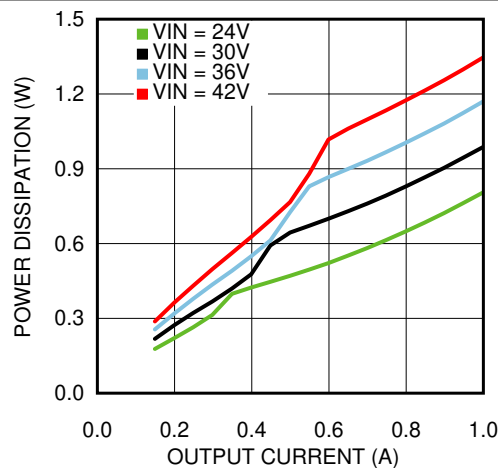
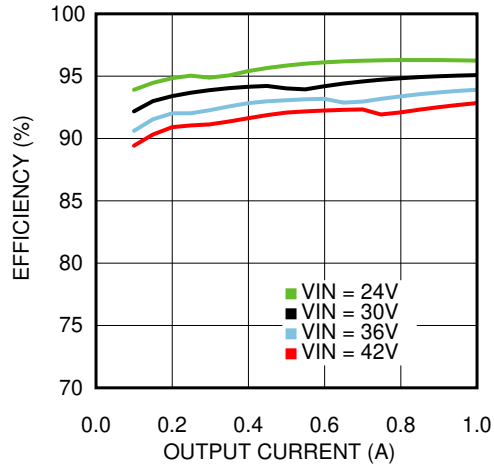


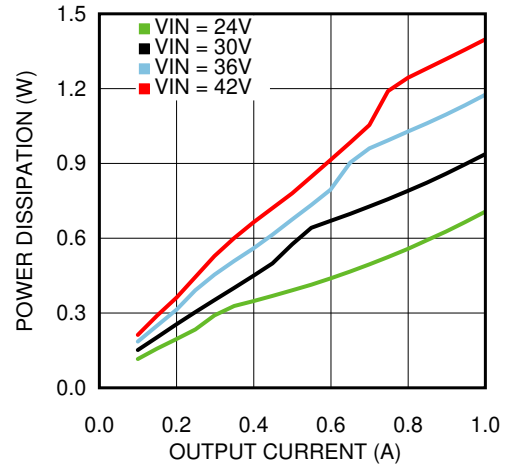
FIG 6-18. Power Dissipation $V_{OUT} = 15\text{ V}$, $T_A = 85^\circ\text{C}$

6.6 Typical Characteristics (continued)

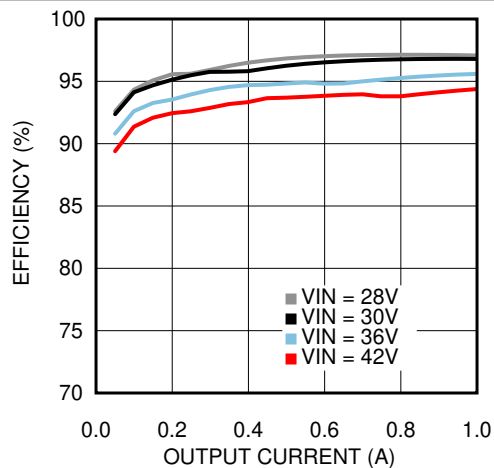
Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.



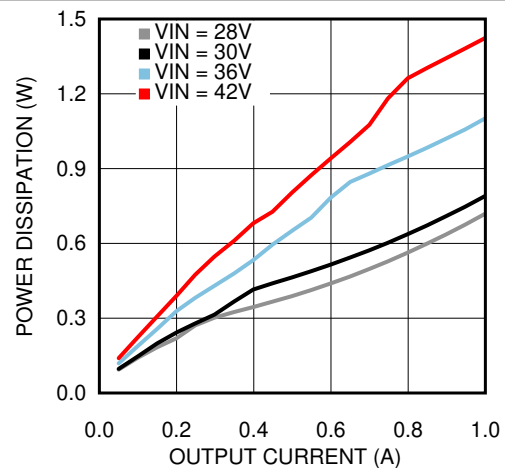
6-19. Efficiency $V_{OUT} = 18\text{ V}$, $T_A = 85^\circ\text{C}$



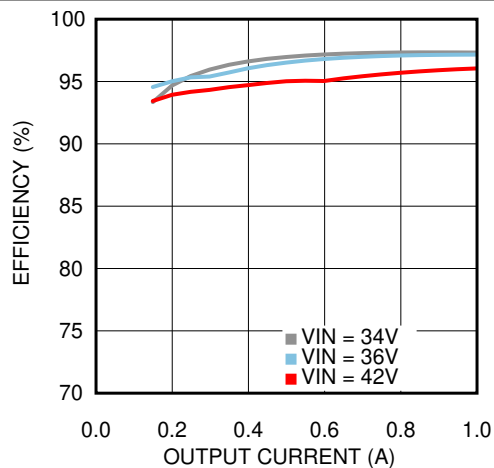
6-20. Power Dissipation $V_{OUT} = 18\text{ V}$, $T_A = 85^\circ\text{C}$



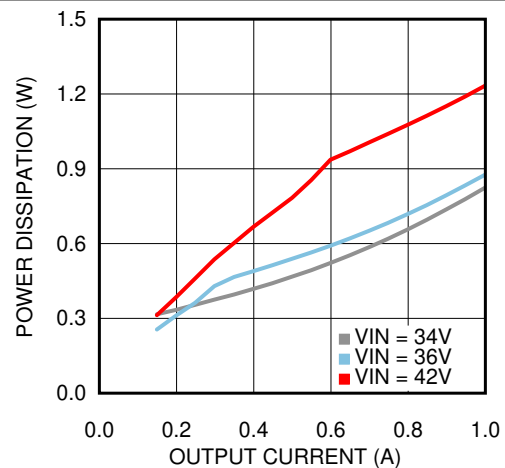
6-21. Efficiency $V_{OUT} = 24\text{ V}$, $T_A = 85^\circ\text{C}$



6-22. Power Dissipation $V_{OUT} = 24\text{ V}$, $T_A = 85^\circ\text{C}$



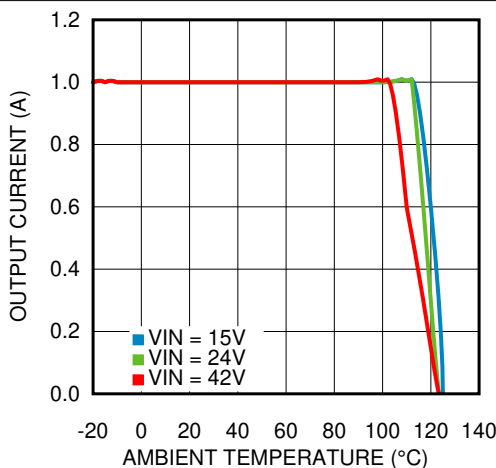
6-23. Efficiency $V_{OUT} = 30\text{ V}$, $T_A = 85^\circ\text{C}$



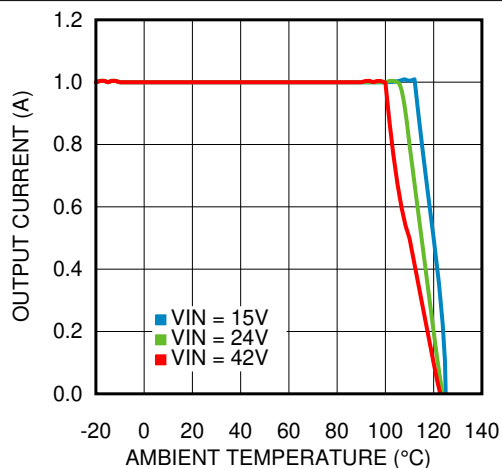
6-24. Power Dissipation $V_{OUT} = 30\text{ V}$, $T_A = 85^\circ\text{C}$

6.6 Typical Characteristics (continued)

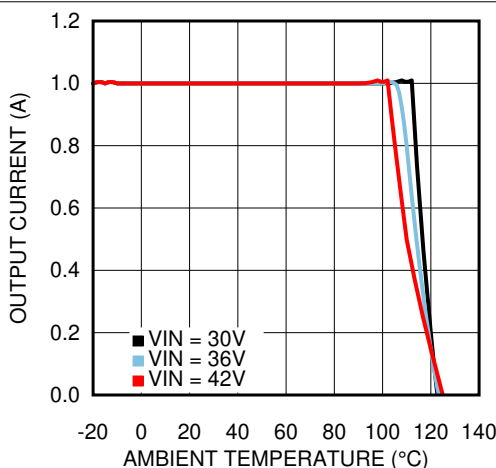
Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.



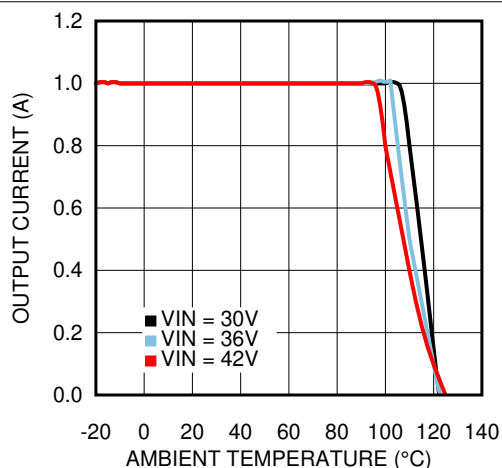
6-25. Thermal Derating $V_{OUT} = 12\text{ V}$, $R_{\theta JA} = 16^\circ\text{C/W}$



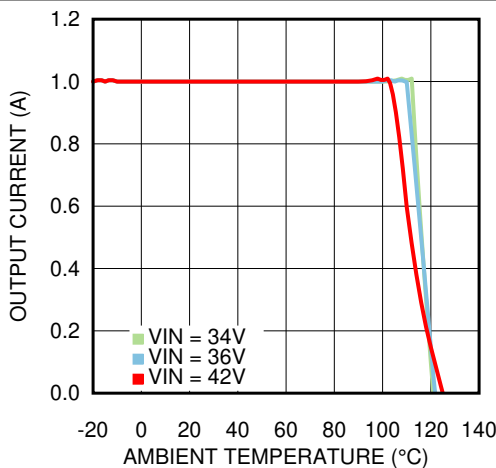
6-26. Thermal Derating $V_{OUT} = 12\text{ V}$, $R_{\theta JA} = 20^\circ\text{C/W}$



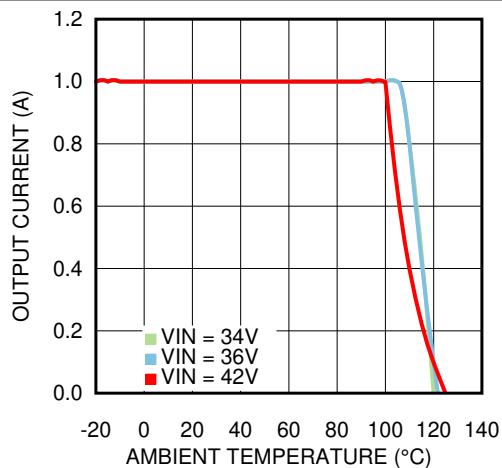
6-27. Thermal Derating $V_{OUT} = 24\text{ V}$, $R_{\theta JA} = 16^\circ\text{C/W}$



6-28. Thermal Derating $V_{OUT} = 24\text{ V}$, $R_{\theta JA} = 20^\circ\text{C/W}$



6-29. Thermal Derating $V_{OUT} = 30\text{ V}$, $R_{\theta JA} = 16^\circ\text{C/W}$



6-30. Thermal Derating $V_{OUT} = 30\text{ V}$, $R_{\theta JA} = 20^\circ\text{C/W}$

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.

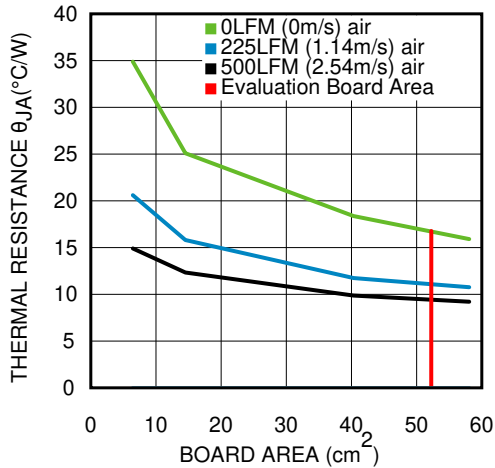


FIG 6-31. Package Thermal Resistance $R_{\theta JA}$ 4 Layer PCB With 1-oz Copper

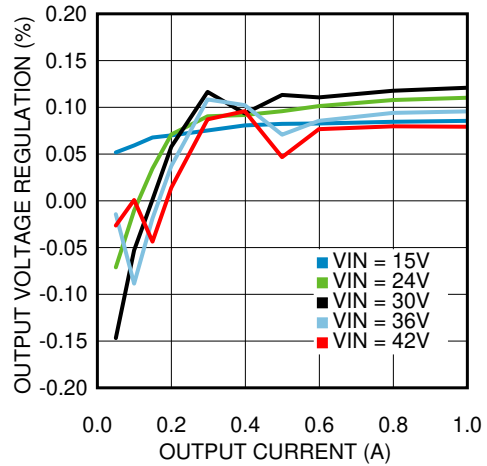


FIG 6-32. Line and Load Regulation $T_A = 25^\circ\text{C}$

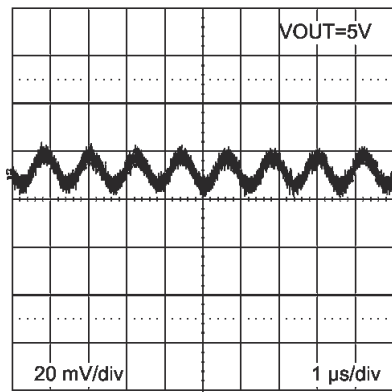


FIG 6-33. Output Ripple $V_{IN} = 12\text{ V}$, $I_{OUT} = 1\text{ A}$, Ceramic C_{OUT} , BW = 200 MHz

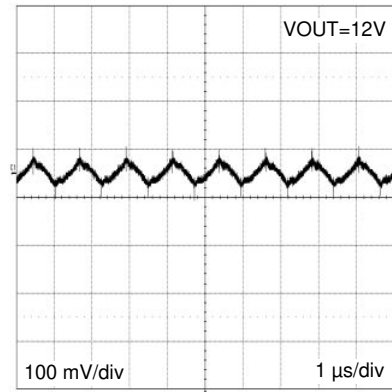


FIG 6-34. Output Ripple $V_{IN} = 24\text{ V}$, $I_{OUT} = 1\text{ A}$, Polymer Electrolytic C_{OUT} , BW = 200 MHz

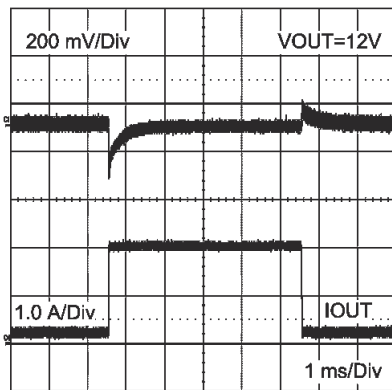


FIG 6-35. Load Transient Response $V_{IN} = 24\text{ V}$ $V_{OUT} = 12\text{ V}$ Load Step from 10% to 100%

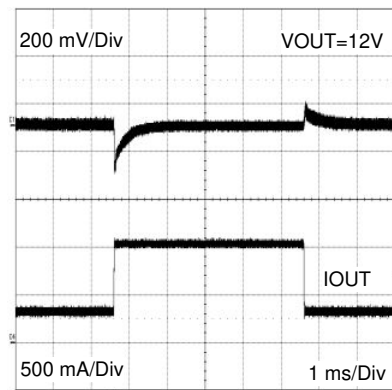


FIG 6-36. Load Transient Response $V_{IN} = 24\text{ V}$ $V_{OUT} = 12\text{ V}$ Load Step From 30% to 100%

6.6 Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F X7R Ceramic}$; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.

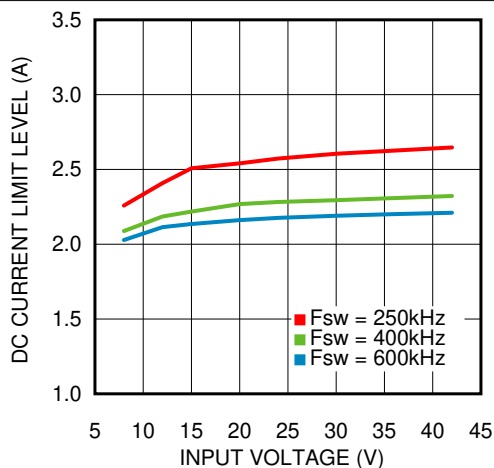


FIG 6-37. Current Limit vs. Input Voltage $V_{OUT} = 5\text{ V}$

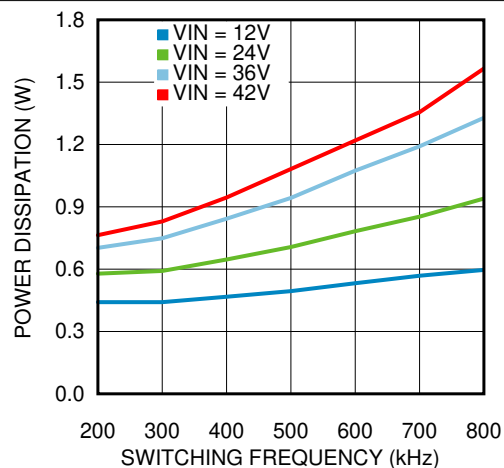


FIG 6-38. Switching Frequency vs. Power Dissipation $V_{OUT} = 5\text{ V}$

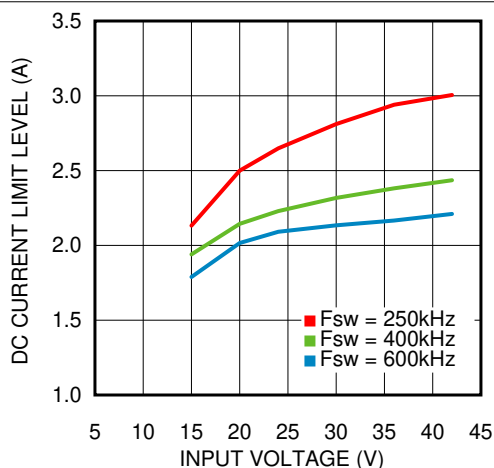


FIG 6-39. Current Limit vs. Input Voltage $V_{OUT} = 12\text{ V}$

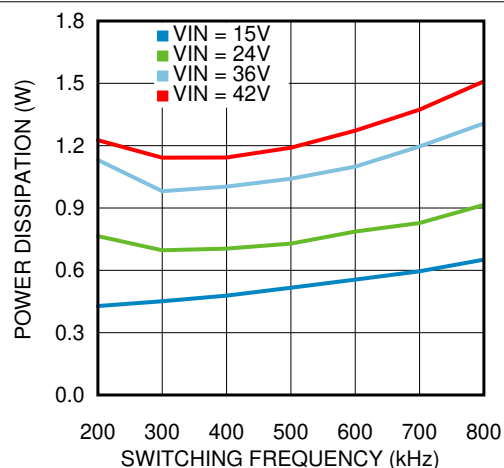


FIG 6-40. Switching Frequency vs. Power Dissipation $V_{OUT} = 12\text{ V}$

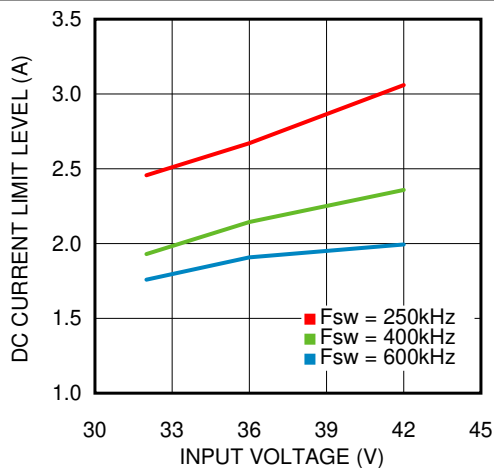


FIG 6-41. Current Limit vs. Input Voltage $V_{OUT} = 24\text{ V}$

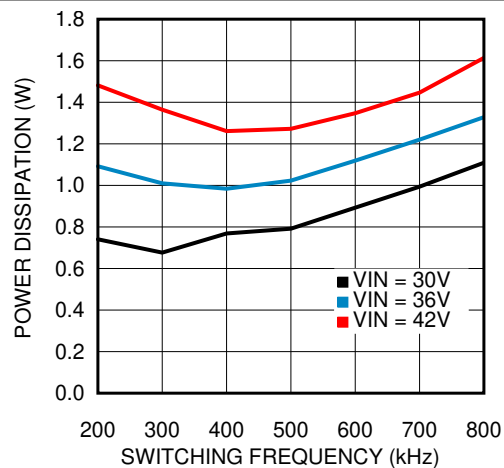
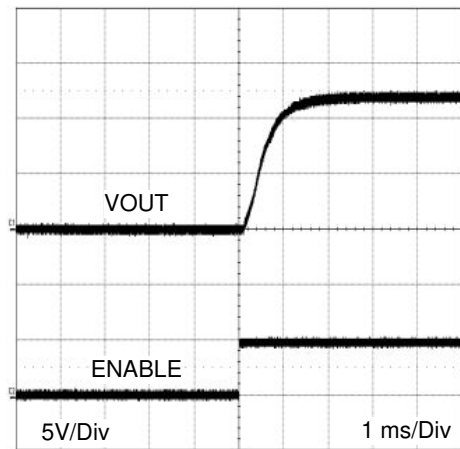


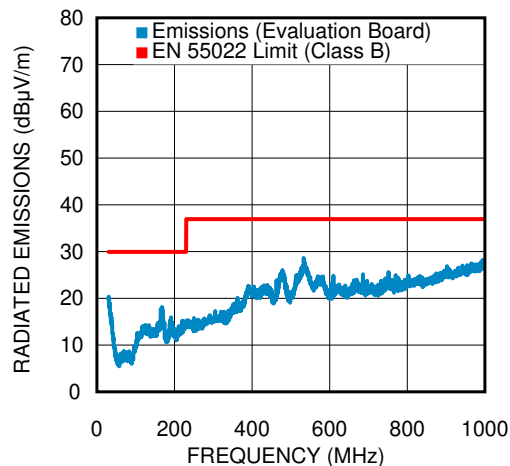
FIG 6-42. Switching Frequency vs. Power Dissipation $V_{OUT} = 24\text{ V}$

6.6 Typical Characteristics (continued)

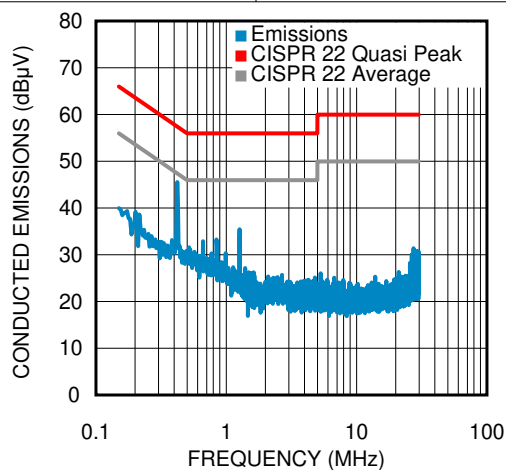
Unless otherwise specified, the following conditions apply: $V_{IN} = 24\text{ V}$; $C_{in} = 10\text{-}\mu\text{F}$ X7R Ceramic; $C_O = 47\text{ }\mu\text{F}$; $T_A = 25^\circ\text{C}$.



6-43. Start-Up $V_{IN} = 24\text{ V}$, $I_{OUT} = 1\text{ A}$



6-44. Radiated EMI of Evaluation Board, $V_{OUT} = 12\text{ V}$



6-45. Conducted EMI, $V_{OUT} = 12\text{ V}$ Evaluation Board BOM and 3.3- μH , 1- μF LC Line Filter

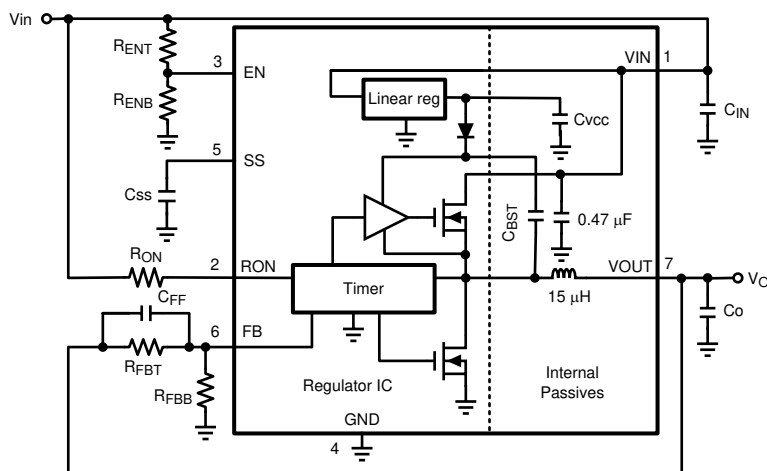
7 Detailed Description

7.1 Overview

7.1.1 COT Control Circuit Overview

Constant ON-Time control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared to an internal 0.8V reference. If the feedback voltage is below the reference, the high-side MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON} . R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the high-side MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.2 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the [セクション 7.2](#), when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds the I_{CL} value, the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below I_{CL} . Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds I_{CL} , further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

Note

The DC current limit varies with duty cycle, switching frequency, and temperature.

7.3.3 Thermal Protection

The junction temperature of the LMZ14201H should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and

additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145 °C (typical Hyst = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

7.3.4 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.5 Prebiased Start-Up

The LMZ14201H will properly start up into a prebiased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the startup sequence. The prebias level of the output voltage must be less than the input UVLO set point. This will prevent the output prebias from enabling the regulator through the high-side MOSFET body diode.

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

8 Application and Implementation

Note

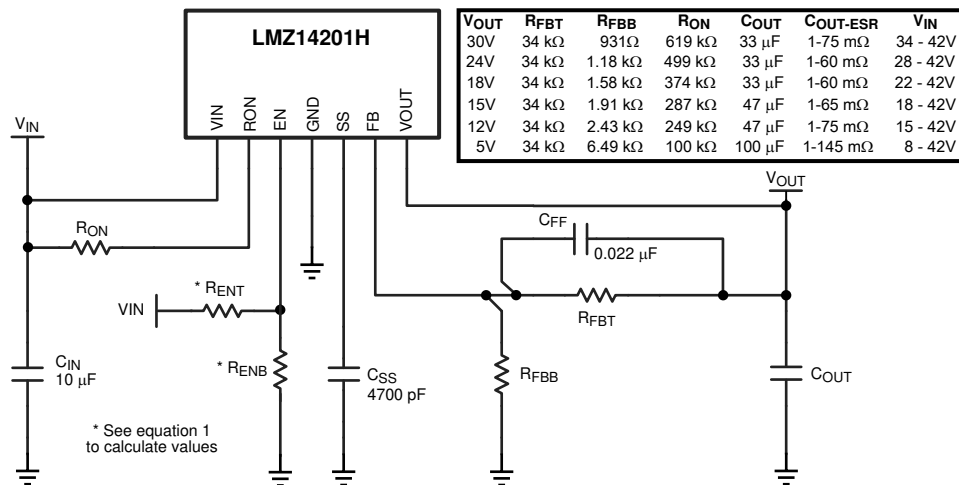
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMZ14201H is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LMZ14201H. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software utilizes iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application



8-1. Simplified Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 5 V to 30 V
- I_{OUT} = 1 A

Refer to the table in 8-1 for more information.

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps for the LMZ14201H Application

The LMZ14201H is fully supported by WEBENCH which offers the following: component selection, electrical simulation, thermal simulation, as well as a build-it prototype board for a reduction in design time. The following list of steps can be used to manually design the LMZ14201H application.

1. Select minimum operating V_{IN} with enable divider resistors.
2. Program V_O with divider resistor selection.
3. Program turnon time with soft-start capacitor selection.
4. Select C_O .

5. Select C_{IN} .
6. Set operating frequency with R_{ON} .
7. Determine module dissipation.
8. Lay out PCB for required thermal performance.

8.2.2.1.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V reference threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN} . The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of the R_{ENT} and R_{ENB} divider shown in the [セクション 7.2](#) is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable undervoltage lockout. This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14201H output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN-ENABLE} / 1.18 \text{ V}) - 1 \quad (1)$$

The EN pin is internally pulled up to V_{IN} and can be left floating for always-on operation. However, it is good practice to use the enable divider and turn on the regulator when V_{IN} is close to reaching its nominal value. This will ensure smooth start-up and will prevent overloading the input supply.

8.2.2.1.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The high-side MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8 \text{ V} \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8 \text{ V}) - 1 \quad (3)$$

These resistors should be chosen from values in the range of 1 k Ω to 50 k Ω .

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , and R_{ON} is included in the simplified applications schematic.

8.2.2.1.3 Soft-Start Capacitor, C_{SS} , Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8 μ A current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / I_{SS} = 0.8 \text{ V} \times C_{SS} / 8 \text{ } \mu\text{A} \quad (4)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8 \text{ } \mu\text{A} / 0.8 \text{ V} \quad (5)$$

Use of a 4700-pF capacitor results in 0.5-ms soft-start duration. This is a recommended value. Note that high values of C_{SS} capacitance will cause more output voltage droop when a load transient goes across the DCM-CCM boundary. Use 式 18 below to find the DCM-CCM boundary load current for the specific operating condition. If a fast load transient response is desired for steps between DCM and CCM mode the soft-start capacitor value should be less than 0.018 μF .

Note that the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200- μA current sink:

- The enable input being “pulled low”
- Thermal shutdown condition
- Overcurrent fault
- Internal V_{IN} UVLO

8.2.2.1.4 Output Capacitor, C_O , Selection

None of the required output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst-case RMS current rating of $0.5 \times I_{LR \text{ P-P}}$, as calculated in 式 19. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 μF is generally required. Experimentation will be required if attempting to operate with a minimum value. Low-ESR capacitors, such as ceramic and polymer electrolytic capacitors are recommended.

8.2.2.1.4.1 Capacitance

式 6 provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT-TRAN}) \quad (6)$$

As an example, for 1A load step, $V_{IN} = 24 \text{ V}$, $V_{OUT} = 12 \text{ V}$, $V_{OUT-TRAN} = 50 \text{ mV}$:

$$C_O \geq 1 \text{ A} \times 0.8 \text{ V} \times 15 \text{ } \mu\text{H} \times 24 \text{ V} / (4 \times 12 \text{ V} \times (24 \text{ V} - 12 \text{ V}) \times 50 \text{ mV})$$

$$C_O \geq 10.05 \text{ } \mu\text{F}$$

8.2.2.1.4.2 ESR

The ESR of the output capacitor affects the output voltage ripple. High ESR will result in larger V_{OUT} peak-to-peak ripple voltage. Furthermore, high output voltage ripple caused by excessive ESR can trigger the overvoltage protection monitored at the FB pin. The ESR should be chosen to satisfy the maximum desired V_{OUT} peak-to-peak ripple voltage and to avoid overvoltage protection during normal operation. The following equations can be used:

$$ESR_{MAX-RIPPLE} \leq V_{OUT-RIPPLE} / I_{LR \text{ P-P}} \quad (7)$$

where

- $I_{LR \text{ P-P}}$ is calculated using 式 19 below.

$$ESR_{MAX-OVP} < (V_{FB-OVP} - V_{FB}) / (I_{LR \text{ P-P}} \times A_{FB}) \quad (8)$$

where

- A_{FB} is the gain of the feedback network from V_{OUT} to V_{FB} at the switching frequency.

As worst-case, assume the gain of A_{FB} with the C_{FF} capacitor at the switching frequency is 1.

The selected capacitor should have sufficient voltage and RMS current rating. The RMS current through the output capacitor is:

$$I(C_{OUT(RMS)}) = I_{LR P-P} / \sqrt{12} \quad (9)$$

8.2.2.1.5 Input Capacitor, C_{IN} , Selection

The LMZ14201H module contains an internal 0.47 μ F input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be as close as possible to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value.

Worst-case input ripple current rating is dictated by 式 10:

$$I(C_{IN(RMS)}) \approx 1/2 \times I_O \times \sqrt{D/1-D} \quad (10)$$

where

- $D \approx V_O / V_{IN}$

(As a point of reference, the worst-case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10- μ F X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected. Also note ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain maximum value of input ripple voltage ΔV_{IN} to be maintained then 式 11 may be used.

$$C_{IN} \geq I_O \times D \times (1-D) / f_{SW-CCM} \times \Delta V_{IN} \quad (11)$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 12-V output application this equals 240 mV and $f_{SW} = 400$ kHz.

$$C_{IN} \geq 1 \text{ A} \times 12 \text{ V} / 24 \text{ V} \times (1 - 12 \text{ V} / 24 \text{ V}) / (400000 \times 0.240 \text{ V})$$

$$C_{IN} \geq 2.6 \mu\text{F}$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.1.6 ON-Time, R_{ON} , Resistor Selection

Many designs will begin with a desired switching frequency in mind. As seen in the [Typical Characteristics](#) section, the best efficiency is achieved in the 300 kHz to 400 kHz switching frequency range. 式 12 can be used to calculate the R_{ON} value.

$$f_{SW(CCM)} \approx V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (12)$$

This can be rearranged as

$$R_{ON} \approx V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (13)$$

The selection of R_{ON} and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the [COT Control Circuit Overview](#) section.

The ON-time of the LMZ14201H timer is determined by the resistor R_{ON} and the input voltage V_{IN} . It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (14)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON} . This limits the maximum operating frequency, which is governed by 式 15:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ nsec}) \quad (15)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150 \text{ nsec} / (1.3 \times 10^{-10}) \quad (16)$$

If R_{ON} calculated in 式 13 is less than the minimum value determined in 式 16 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited in order to keep the frequency unchanged.

Additionally, the minimum OFF-time of 260 ns (typical) limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

8.2.2.1.6.1 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}-1) \times 15 \mu\text{H} \times 1.18 \times 10^{20} \times I_O / ((V_{IN}-V_O) \times R_{ON}^2) \quad (17)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using 式 12 above.

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN}-V_O) / (2 \times 15 \mu\text{H} \times f_{SW(CCM)} \times V_{IN}) \quad (18)$$

The inductor internal to the module is 15 μH . This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR P-P} = V_O \times (V_{IN} - V_O) / (15 \mu\text{H} \times f_{SW} \times V_{IN}) \quad (19)$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from 式 12.

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.3 Application Curve

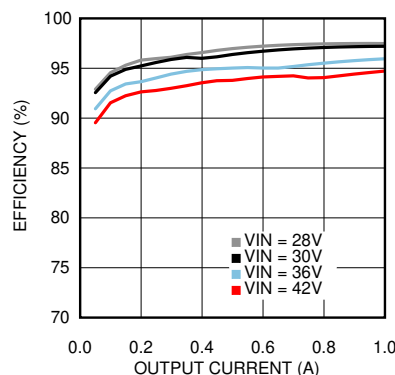


图 8-2. Efficiency $V_{OUT} = 24 \text{ V}$, $T_A = 25^\circ\text{C}$

9 Power Supply Recommendations

The LMZ14201H device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14201H supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ14201H, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47- μ F or 100- μ F electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops.

From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{IN1}) is placed at a distance away from the LMZ14203. Therefore place C_{IN1} as close as possible to the LMZ14203 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

Both feedback resistors, R_{FBT} and R_{FBB} , and the feed forward capacitor C_{FF} , should be close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT} , R_{FBB} , and C_{FF} should be routed away from the body of the LMZ14203 to minimize noise.

4. Make input and output bus connections as wide as possible.

This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.1.1 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
 - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
 - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to AN *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* ([SNAA214](#)) for Reflow information
- Maximum number of reflows allowed is one

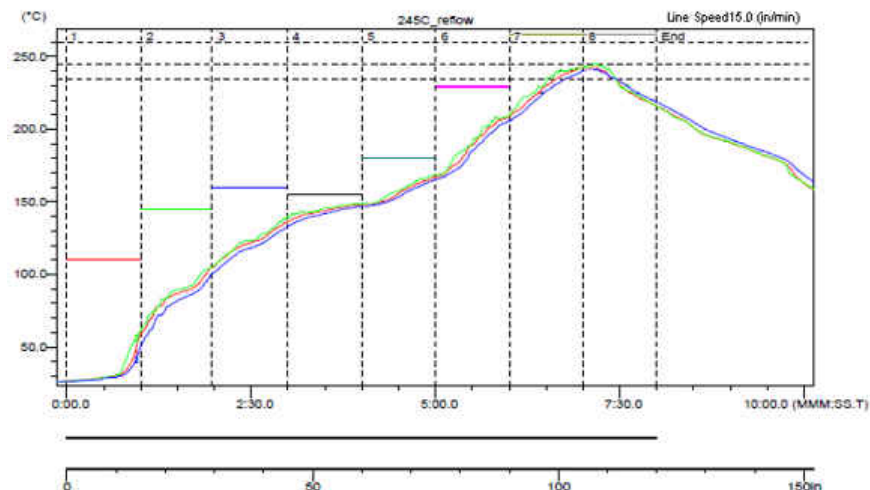


图 10-1. Sample Reflow Profile

表 10-1. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0	—	0	—
2	242.5	7.1	0.55	6.31	0	7.1	0	—
3	241	7.09	0.42	6.44	0	—	0	—

10.2 Layout Example

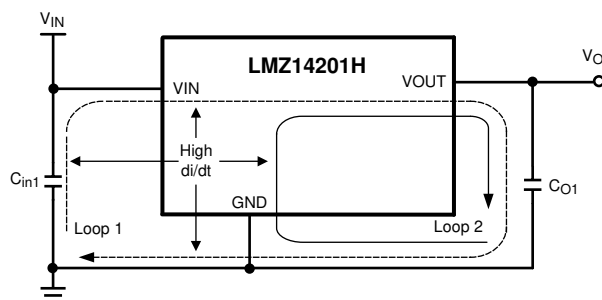


图 10-2. Critical Current Loops to Minimize

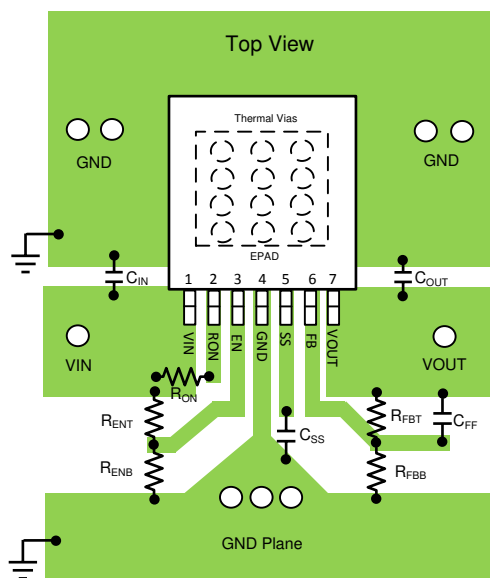


Figure 10-3. PCB Layout Guide

10.2.1 Power Dissipation and Board Thermal Requirements

For a design case of $V_{IN} = 24\text{ V}$, $V_{OUT} = 12\text{ V}$, $I_{OUT} = 1\text{ A}$, $T_A (\text{MAX}) = 85^\circ\text{C}$, and $T_{\text{JUNCTION}} = 125^\circ\text{C}$, the device must see a maximum junction-to-ambient thermal resistance of:

$$R_{\theta\text{JA-MAX}} < (T_{\text{J-MAX}} - T_{\text{A(MAX)}}) / P_D \quad (20)$$

This $R_{\theta\text{JA-MAX}}$ will ensure that the junction temperature of the regulator does not exceed $T_{\text{J-MAX}}$ in the particular application ambient temperature.

To calculate the required $R_{\theta\text{JA-MAX}}$ we need to get an estimate for the power losses in the IC. Figure 10-4 is taken from the *Typical Characteristics* section and shows the power dissipation of the LMZ14201H for $V_{OUT} = 12\text{ V}$ at $85^\circ\text{C } T_A$.

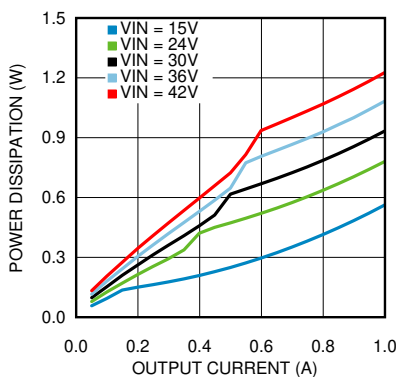


Figure 10-4. Power Dissipation $V_{OUT} = 12\text{ V}$, $T_A = 85^\circ\text{C}$

Using the $85^\circ\text{C } T_A$ power dissipation data as a conservative starting point, the power dissipation P_D for $V_{IN} = 24\text{ V}$ and $V_{OUT} = 12\text{ V}$ is estimated to be 0.75 W . The necessary $R_{\theta\text{JA-MAX}}$ can now be calculated.

$$R_{\theta\text{JA-MAX}} < (125^\circ\text{C} - 85^\circ\text{C}) / 0.75\text{ W} \quad (21)$$

$$R_{\theta\text{JA-MAX}} < 53.3^\circ\text{C/W} \quad (22)$$

To achieve this thermal resistance the PCB is required to dissipate the heat effectively. The area of the PCB will have a direct effect on the overall junction-to-ambient thermal resistance. In order to estimate the necessary copper area we can refer to [Figure 10-5](#). This graph is taken from the *Typical Characteristics* section and shows how the $R_{\theta JA}$ varies with the PCB area.

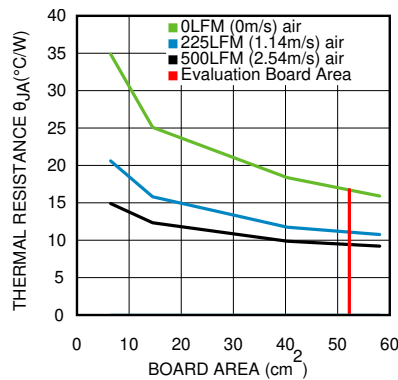


Figure 10-5. Package Thermal Resistance $R_{\theta JA}$ 4-Layer PCB With 1-oz Copper

For $R_{\theta JA-MAX} < 53.3^{\circ}\text{C/W}$ and only natural convection (that is, no air flow), the PCB area can be smaller than 9 cm². This corresponds to a square board with 3 cm × 3 cm (1.18 in × 1.18 in) copper area, 4 layers, and 1 oz copper thickness. Higher copper thickness will further improve the overall thermal performance. Note that thermal vias should be placed under the IC package to easily transfer heat from the top layer of the PCB to the inner layers and the bottom layer.

For more guidelines and insight on PCB copper area, thermal vias placement, and general thermal design practices, refer to Application Note AN-2020 ([SNVA419](#)).

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, [SNVA425](#)
- *Evaluation Board Application Note AN-2024*, [SNVA422](#)
- *AN-2026 Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules*, [SNVA424](#)
- *AN-2020 Thermal Design By Insight, Not Hindsight*, [SNVA419](#)
- *AN Design Summary LMZ1xxx and LMZ2xxx Power Modules Family*, [SNAA214](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

WEBENCH® and SIMPLE SWITCHER® are registered trademarks of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMZ14201HTZ/NOPB	Active	Production	TO-PMOD (NDW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZ/NOPB.A	Active	Production	TO-PMOD (NDW) 7	250 SMALL T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZ/NOPB.B	Active	Production	TO-PMOD (NDW) 7	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
LMZ14201HTZE/NOPB	Active	Production	TO-PMOD (NDW) 7	45 TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZE/NOPB.A	Active	Production	TO-PMOD (NDW) 7	45 TUBE	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZE/NOPB.B	Active	Production	TO-PMOD (NDW) 7	45 TUBE	-	Call TI	Call TI	-40 to 125	
LMZ14201HTZX/NOPB	Active	Production	TO-PMOD (NDW) 7	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZX/NOPB.A	Active	Production	TO-PMOD (NDW) 7	500 LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	LMZ14201 HTZ
LMZ14201HTZX/NOPB.B	Active	Production	TO-PMOD (NDW) 7	500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

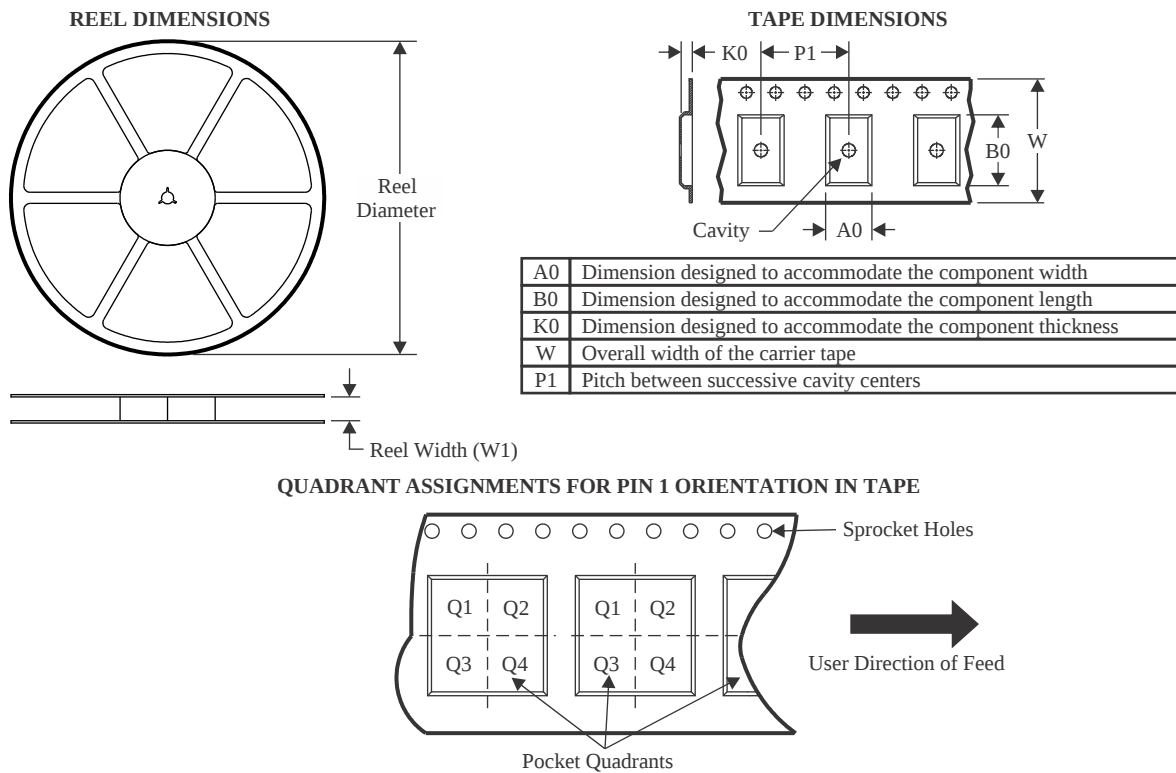
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

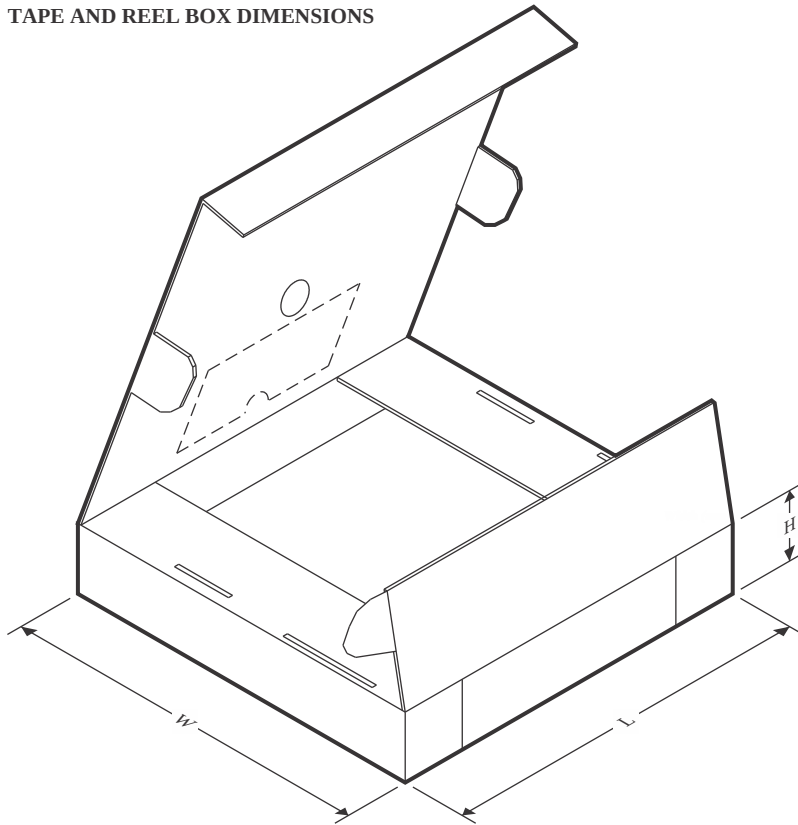
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14201HTZ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14201HTZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14201HTZ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ14201HTZX/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMZ14201HTZE/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4
LMZ14201HTZE/NOPB.A	NDW	TO-PMOD	7	45	502	17	6700	8.4



重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](#) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2025, Texas Instruments Incorporated

最終更新日：2025 年 10 月