LP3470A プログラマブルな遅延と精度 1% のリセット・スレッショルドを備えた超低消費電力電圧スーパーバイザ

1 特長

- LP3470 とピン互換
- 5 ピンの SOT-23 パッケージ
- オープン・ドレインの $\overline{\text{RESET}}$ 出力
- 外付けコンデンサを使用してリセットのタイムアウト時間をプログラム可能
- 短時間の VCC 過渡への耐性
- ±1% (標準値) のリセット・スレッショルド精度
- 非常に小さい静止電流 (標準値 0.3µA)
- $\overline{\text{RESET}}$ は VCC を 0.95V まで下げても有効

2 アプリケーション

- 重要な µP と µC の電力監視
- インテリジェント機器
- コンピュータ
- 携帯型およびバッテリ駆動の機器
- ビルディング・オートメーション：ビルディングのセキュリティ・システム、ビデオ監視
- ファクトリ・オートメーション：フィールド・トランスミッタ、位置および近接センサ
- モータ・ドライブ

3 概要

LP3470A デバイスは、温度範囲全体にわたってリセット・スレッショルドの 1% 以内の精度で電圧を監視するように設計された超低消費電力電圧監視回路であり、既存の TI デバイス LP3470 とピン互換です。LP3470A デバイスは高精度でナノパワー電圧を監視します。その際、遅延をプログラム可能です。

VCC 電源電圧がリセット・スレッショルドを下回ると、LP3470A はリセット信号をアサートします。リセットのタイムアウト時間は、外付けコンデンサを使用して調節できます。VCC がスレッショルド電圧にヒステリシスを加えた値を上回った後、リセットは一定の期間 (外付けコンデンサでプログラムします) アサート状態を維持します。

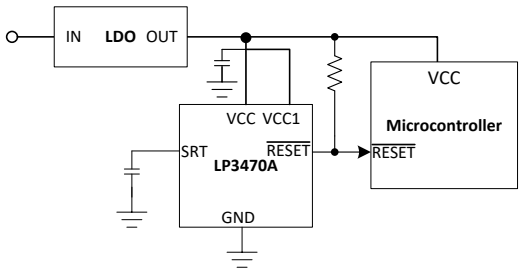
使用できるリセット・スレッショルド電圧の選択肢については、「*メカニカル、パッケージ、および注文情報*」を参照してください。

製品情報(1)

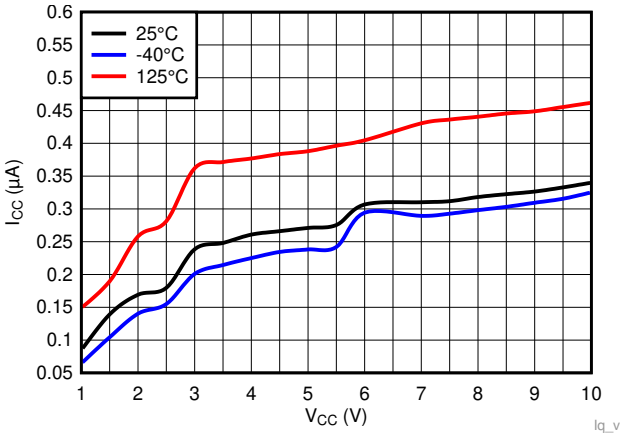
型番	パッケージ	本体サイズ (公称)
LP3470A	SOT-23 (5)	1.60mm×2.90mm

(1) 提供しているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

基本的な動作回路



LP3470A の標準的な消費電流



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (October 2019) から Revision B に変更 **Page**

- 「電気的特性」表に合わせて「非常に小さい静止電流」を 0.35 から 0.3 に 変更 ... 1
- Changed the typical value of I_{CC} in the Electrical Characteristics table from 300 to 0.3 to match with the units of µA ... 6

2019年7月発行のものから更新 **Page**

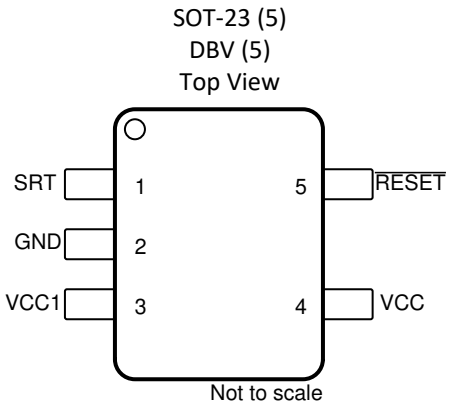
- 最初の公開リリース ... 1

5 Device Comparison Table

PART NUMBER	V_{IT-} (typ) (VCC RAMPING DOWN)	V_{IT+} (typ) (VCC RAMPING UP)
LP3470A263	2.63 V	2.73 V
LP3470A275	2.75 V	2.85 V
LP3470A293	2.93 V	3.03 V
LP3470A308	3.08 V	3.28 V
LP3470A365	3.65 V	3.85 V
LP3470A400	4.0 V	4.2 V
LP3470A438	4.38 V	4.58 V
LP3470A463	4.63 V	4.83 V

6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SRT	I	Set reset time-out. Connect a capacitor between this pin and ground to select the reset time-out period (t_D). $t_D = 619 \times C_1$ (C_{SRT} in µF and t_D in ms). If no capacitor is connected, leave this pin floating.
2	GND	—	Ground pin.
3	VCC1	I	Can be connected to VCC or left floating. DO NOT CONNECT TO GND.
4	VCC	I	Supply voltage, and reset threshold monitor input.
5	$\overline{\text{RESET}}$	O	Open-drain, active-low reset output. Connect to an external pullup resistor. $\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage (VCC) drops below the reset threshold voltage (V_{IT-}). Once VCC exceeds the reset threshold (V_{IT-}) + hysteresis (V_{HYS}), $\overline{\text{RESET}}$ remains low for the reset time-out period (t_D) and then deasserts to logic high.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VCC	–0.3	12	V
	$\overline{\text{RESET}}$	–0.3	12	
	SRT	–0.3	5.5	
Current	$\overline{\text{RESET}}$		±70	mA
Temperature(2)	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input supply voltage	0.95		10	V
$V_{\overline{RESET}}$, V_{RESET}	$\overline{\text{RESET}}$ pin voltage	0		10	V
$I_{\overline{RESET}}$, I_{RESET}	$\overline{\text{RESET}}$ pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LP3470A DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 0.95 V ≤ V_{CC} ≤ 10 V, SRT = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VCC, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input supply voltage		0.95		10	V
V_{IT-}	Negative-going input threshold accuracy	-40°C to 125°C	–1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.08 V to 4.63 V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 2.64 V to 2.93 V	75	100	125	mV
I_{CC}	Supply current into VCC pin	VCC = 0.95 V < V_{CC} < 10 V VCC > V_{IT+} (1) T_A = -40°C to 125°C		0.3	1	µA
R_{SRT}	SRT pin internal resistance (2)		350	500	650	kΩ
V_{POR}	Power on Reset Voltage(3)	$V_{OL(max)}$ = 0.2 V $I_{OUT\ (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{CC} < 5 V V_{CC} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{RESET}$ pin in High Impedance, V_{CC} = V_{RESET} = 5.5 V V_{IT+} < V_{CC}			90	nA

(1) V_{IT+} = V_{HYS} + V_{IT-}
(2) This parameter is guranteed by design and characterization
(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

7.6 Timing Requirements

At 0.95 V ≤ V_{CC} ≤ 10 V, SRT = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VCC, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, VCC slew rate < 100mV / us, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P_HL}	Propagation detect delay for VCC falling below V_{IT-}	V_{CC} = V_{IT+} to (V_{IT-}) - 10% (1)		15	30	µs
t_D	Reset time delay	SRT pin = open V_{CC} = (V_{IT-} -1V) to (V_{IT+} + 1V)			50	µs
		SRT pin = 10 nF(2)(3)		6.2		ms
		SRT pin = 1 µF(2)(3)		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(3)(4)		10		µs

(1) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL}
(2) Ideal capacitor
(3) Parameter is guranteed by design.
(4) Overdrive % = [(V_{CC}/ V_{IT-}) - 1] × 100%

7.7 Typical Characteristics

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at $T_A = T_J = 25°C$ (unless otherwise noted).

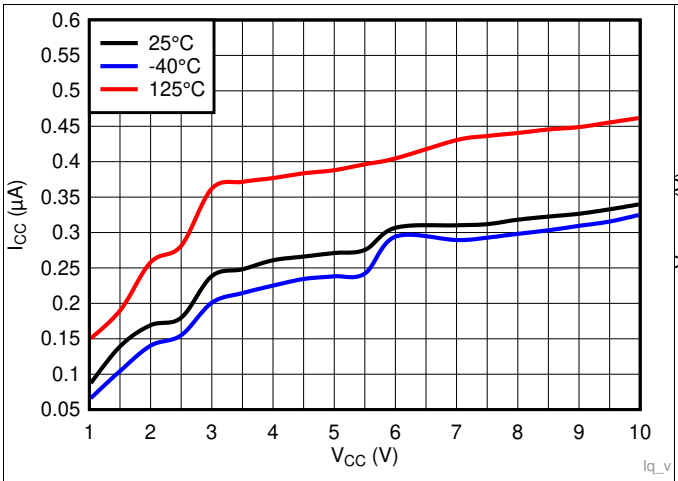


図 1. Supply Current vs Supply Voltage

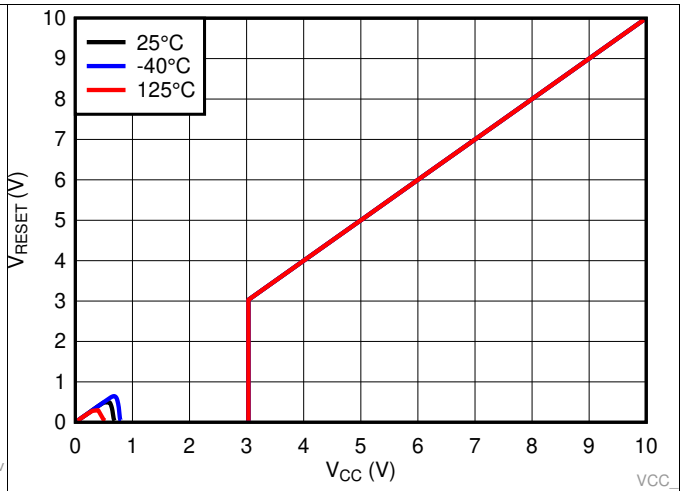


図 2. Output Voltage vs Supply Voltage for LP3470A293

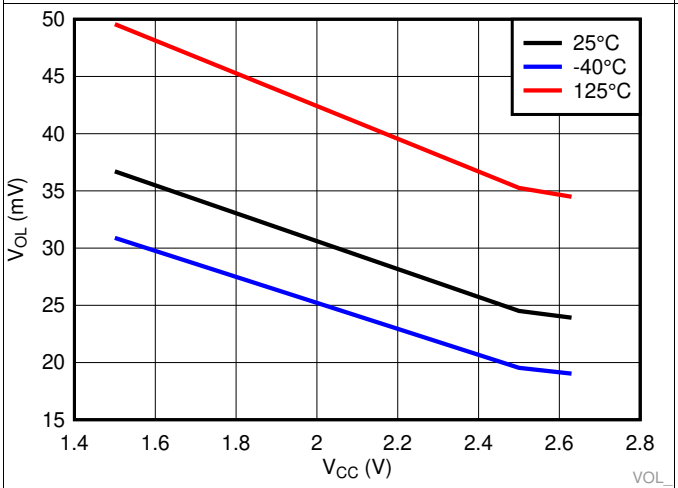


図 3. Low Level Output Voltage vs Supply Voltage

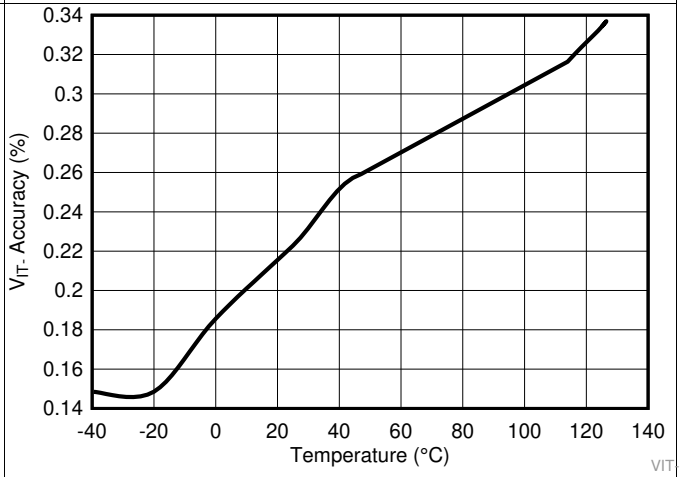


図 4. Negative-going Input Threshold V_{IT-} Accuracy vs Temperature

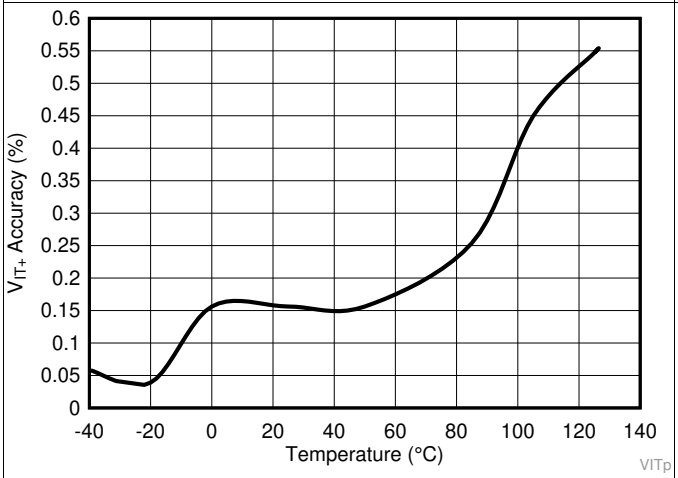


図 5. Positive-going Input Threshold V_{IT+} Accuracy vs Temperature

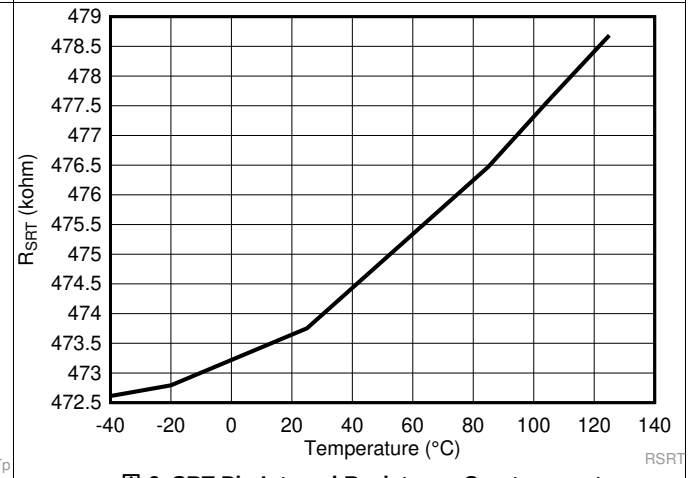


図 6. SRT Pin Internal Resistance Overtemperature

Typical Characteristics (continued)

Typical characteristics show the typical performance of the LP3470A device. Test conditions are at $T_A = T_J = 25°C$ (unless otherwise noted).

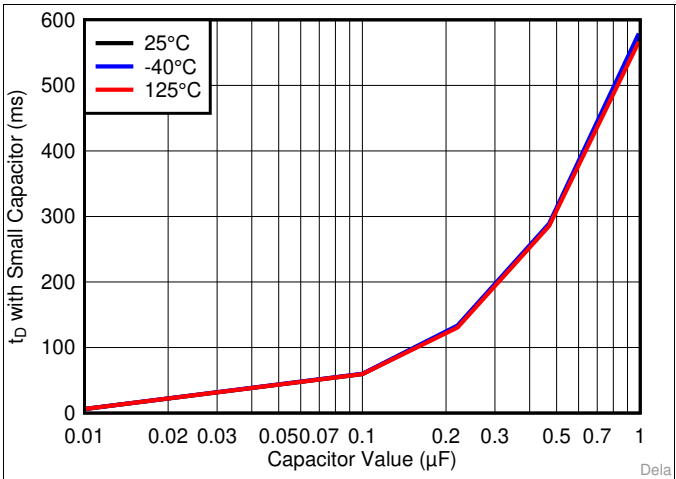


図 7. Reset Time Delay vs Small Capacitor Values

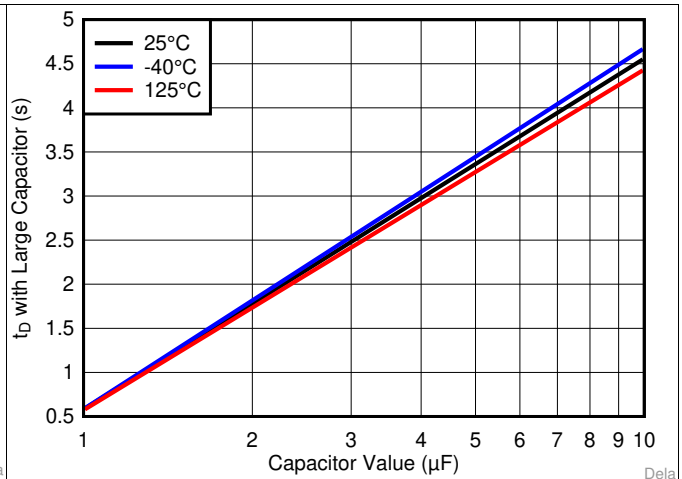


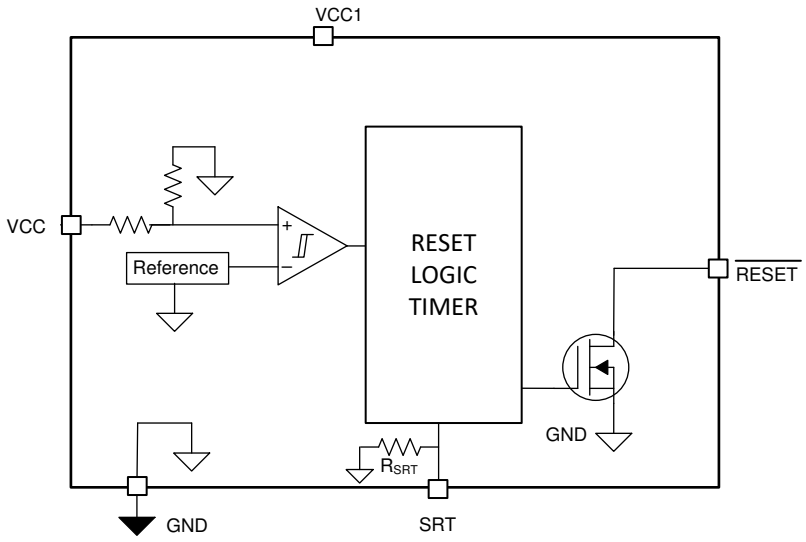
図 8. Reset Time Delay vs Large Capacitor Values

8 Detailed Description

8.1 Overview

The LP3470A micropower voltage supervisory circuit provides a simple solution to monitor the power supplies in microprocessor and digital systems and provides a reset controlled by the factory-programmed reset threshold on the VCC supply voltage pin. When the voltage declines below the reset threshold, the reset signal is asserted and remains asserted for an interval programmed by an external capacitor after VCC has risen above the threshold voltage. The reset threshold options are 2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Time-Out Period

The reset time delay can be set to a minimum value of 50 µs by leaving the SRT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between SRT pin and GND.

The relationship between external capacitor (C_{SRT}) in Farads at SRT pin and the time delay (t_D) in seconds is given by 式 1.

$$t_D = -\ln(0.29) \times R_{SRT} \times C_{SRT} + t_D \text{ (no cap)} \quad (1)$$

式 1 is simplified to 式 2 by plugging R_{SRT} and $t_{D(no\ cap)}$ given in *Electrical Characteristics* section:

$$t_D = 618937 \times C_{SRT} + 50\ \mu s \quad (2)$$

式 3 solves for external capacitor value (C_{SRT}) in units of Farads where t_D is in units of seconds

$$C_{SRT} = (t_D - 50\ \mu s) \div 618937 \quad (3)$$

The reset delay varies according to three variables: the external capacitor variance (C_{SRT}), SRT pin internal resistance (R_{SRT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in Equation 5 and Equation 6.

$$t_{D\ (minimum)} = -\ln(0.36) \times R_{SRT\ (min)} \times C_{SRT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (4)$$

$$t_{D\ (maximum)} = -\ln(0.26) \times R_{SRT\ (max)} \times C_{SRT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (5)$$

Feature Description (continued)

The recommended maximum delay capacitor for the LP3470A is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

8.3.2 $\overline{\text{RESET}}$ Output

In applications like microprocessor (µP) systems, errors might occur in system operation during power up, power down, or brownout conditions. It is imperative to monitor the power supply voltage to prevent these errors from occurring.

The LP3470A asserts a reset signal whenever the VCC supply voltage is below a threshold (V_{IT-}) voltage. $\overline{\text{RESET}}$ is ensured to be a logic low for VCC > 0.95 V. Once VCC exceeds the reset threshold plus a hysteresis voltage, the reset is kept asserted for a time period (t_D) programmed by an external capacitor (C_{SRT}); after this interval $\overline{\text{RESET}}$ goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold), $\overline{\text{RESET}}$ goes low. When VCC returns above the reset threshold plus a hysteresis voltage, $\overline{\text{RESET}}$ remains low for a time period t_D before going to logic high. 図 9 shows this behavior.

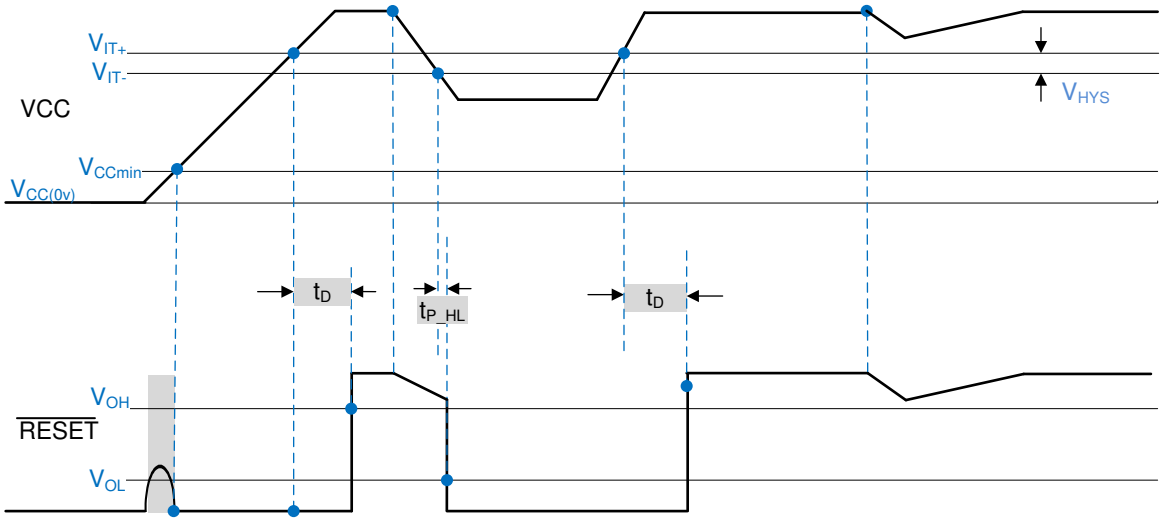


図 9. $\overline{\text{RESET}}$ Output Timing Diagram

8.3.3 Pull-up Resistor Selection

The $\overline{\text{RESET}}$ output structure of the LP3470A is an open-drain N-channel MOSFET switch. A pull-up resistor ($R_{pull-up}$) must be connected to VCC to keep the output logic high when $\overline{\text{RESET}}$ is not asserted.

Connect the pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 10 V independent of the VCC voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. $R_{pull-up}$ must be large enough to limit the current through the output within the recommended operating conditions. The pull-up resistor value determines the actual VOL, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$). A typical pull-up resistor value of 20 kΩ is sufficient in most applications.

8.3.4 VCC Transient Immunity

The LP3470A is immune to quick voltage transients or excursions on VCC. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VCC deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 6. A 0.1-µF bypass capacitor mounted close to VCC provides additional transient immunity.

$$\text{Overdrive} = | (V_{CC} / V_{IT-} - 1) \times 100\% | \quad (6)$$

Feature Description (continued)

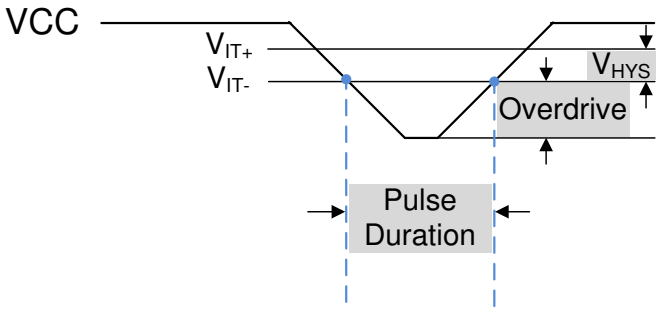


図 10. Overdrive vs Pulse Duration

8.4 Device Functional Modes

8.4.1 $\overline{\text{RESET}}$ Output Low

When the VCC supply voltage is below the reset threshold (V_{IT-}), the $\overline{\text{RESET}}$ pin will output logic low. $\overline{\text{RESET}}$ is ensured to be a logic low for VCC > 0.95 V.

8.4.2 $\overline{\text{RESET}}$ Output High

When the VCC supply voltage exceeds the reset threshold (V_{IT-}) plus the hysteresis voltage (V_{HYS}), the $\overline{\text{RESET}}$ remains asserted for a time period (t_D) programmed by an external capacitor (C_{SRT}); after this interval $\overline{\text{RESET}}$ goes to logic high.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3470A is a micropower CMOS voltage supervisor that is ideal for use in battery-powered microprocessor and other digital systems. It is small in size and provides voltage monitoring and supervisory functions with nano-Iq and programmable delay, making it a good solution in a variety of applications. The LP3470A is available in six standard reset threshold voltage options, and the reset time-out period is adjustable using an external capacitor providing maximum flexibility in any application. This device can ensure system reliability and ensures that a connected microprocessor will operate only when a minimum voltage supply is satisfied.

9.2 Typical Application

The LP3470A can be used as a simple supervisor circuit to monitor the input supply to a microprocessor as shown in 図 11.

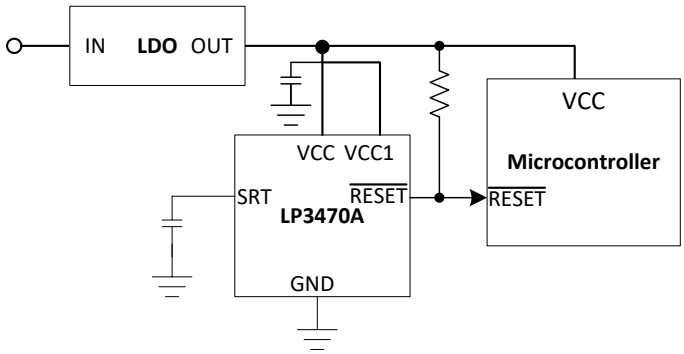


図 11. Power-On Reset Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input supply voltage	0.95 to 10 V
Reset threshold voltage	2.63 V, 2.75 V, 2.93 V, 3.08 V, 3.65 V, 4 V, 4.38 V, 4.63 V
External pullup resistor	0.68 to 68 kΩ
External reset time-out period capacitor	C_{SRT} = 1 nF
Reset time-out period	619 µs

9.2.2 Detailed Design Procedure

The minimum application circuit requires the LP3470A Power-On Reset Circuit IC and a pullup resistor connecting the reset pin to VCC. The reset delay can be programmed with an additional capacitor connected from the SRT pin to GND. See *RESET Time-Out Period* and *Pull-up Resistor Selection* for information on choosing specific values for components.

9.2.3 Application Curves

Two capacitor values for C_{SRT} (0.1 µF and 1 µF) are used as examples to show the programmability of the output time delay as shown in 図 12 and 図 13.

図 12. Reset Delay Time with 0.1-µF Capacitor at SRT

図 13. Reset Delay Time with 1-µF Capacitor at SRT

10 Power Supply Recommendations

The input of the LP3470A is designed to handle up to the supply voltage absolute maximum rating of 12 V. If the input supply is susceptible to any large transients above the maximum rating, then take extra precautions. An input capacitor is optional but not required to help avoid false reset output triggers due to noise.

11 Layout

11.1 Layout Guidelines

- Good analog design practice recommends placing a minimum of 0.1-µF ceramic capacitor as near as possible to the VCC pin.
- Place components as close as possible to the IC
- Keep traces short between the IC and the C_{SRT} capacitor to ensure the timing delay is as accurate as possible.
- For VCC slew rate > 100 mV/µs, increase input capacitance and pull-up resistor value

11.2 Layout Example

図 14 shows a layout example.

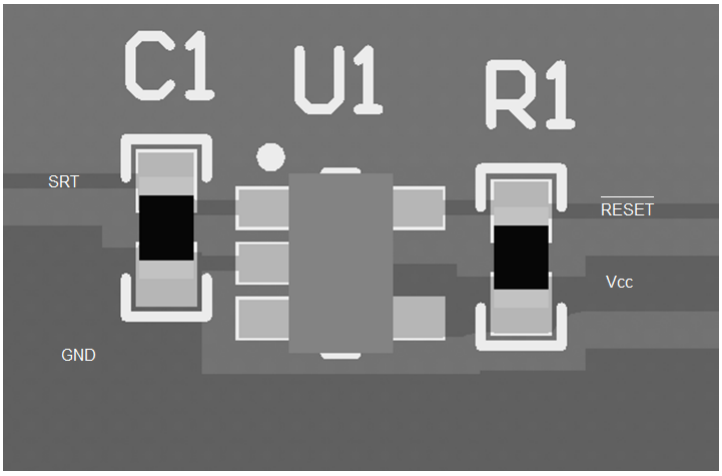


図 14. LP3470A Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商標

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12.4 静電気放電に関する注意事項

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3470A263DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D263
LP3470A263DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D263
LP3470A275DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D275
LP3470A275DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D275
LP3470A293DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D293
LP3470A293DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D293
LP3470A308DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D308
LP3470A308DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D308
LP3470A365DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D365
LP3470A365DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D365
LP3470A400DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D400
LP3470A400DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D400
LP3470A438DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D438
LP3470A438DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D438
LP3470A463DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	D463
LP3470A463DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D463

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

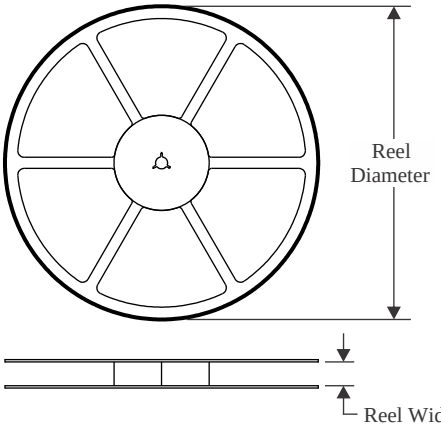
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

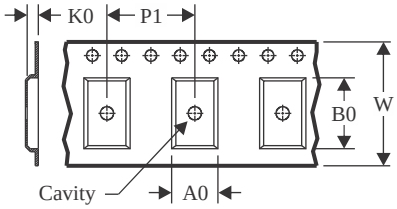
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

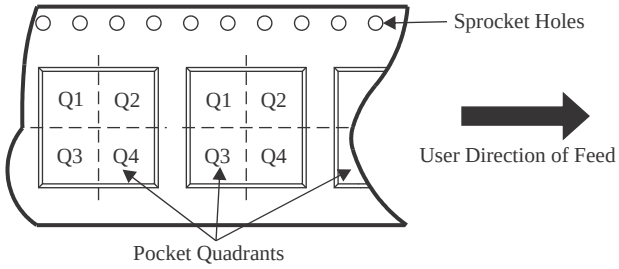


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

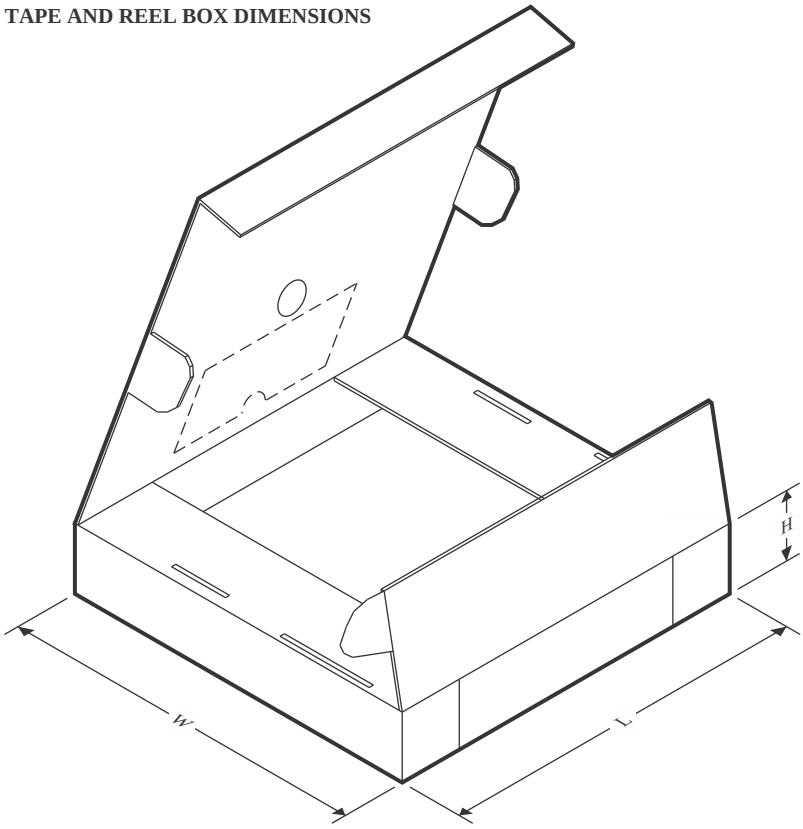
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3470A263DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A275DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A293DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A308DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A365DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A400DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A438DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP3470A463DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

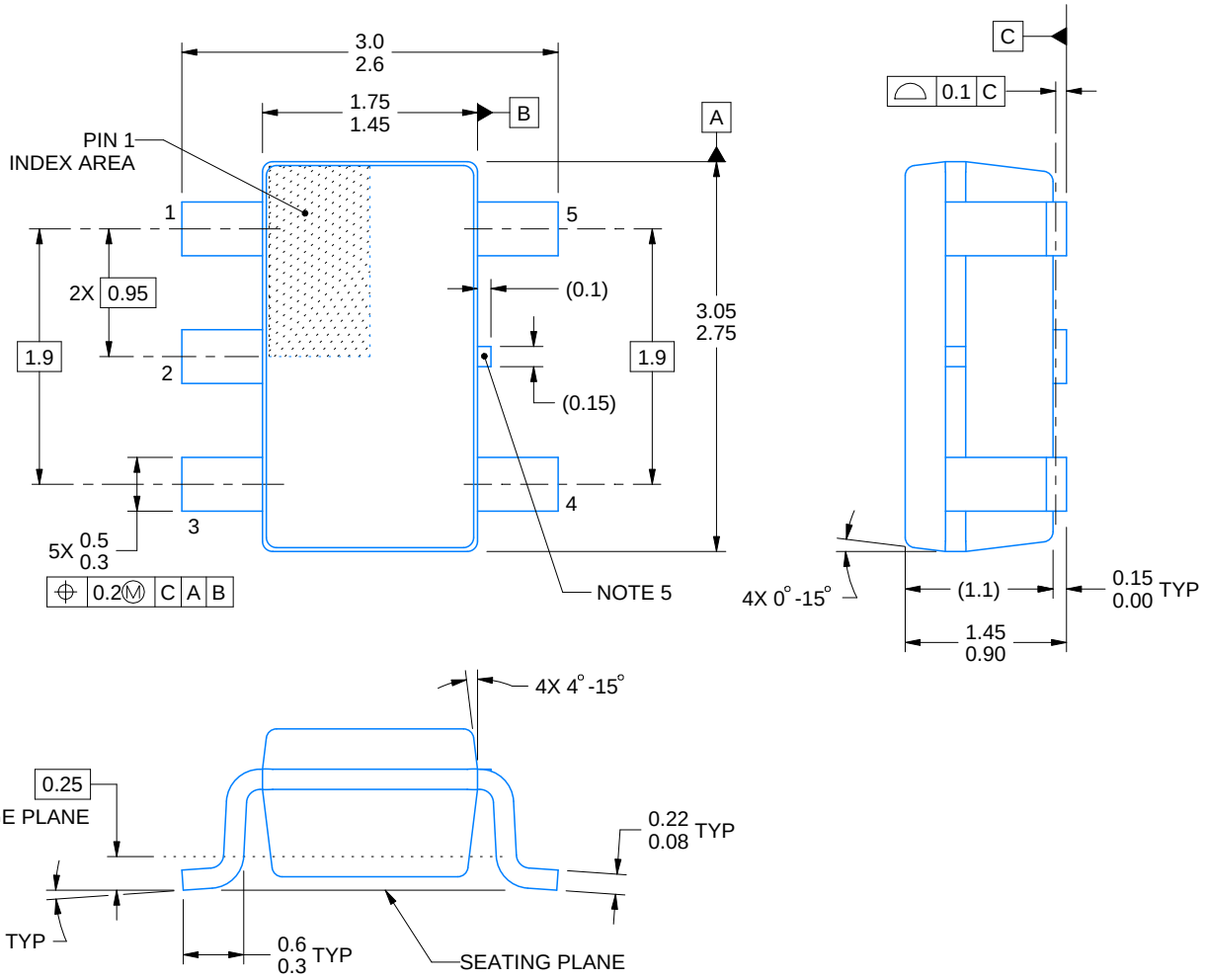
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3470A263DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A275DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A293DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A308DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A365DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A400DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A438DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP3470A463DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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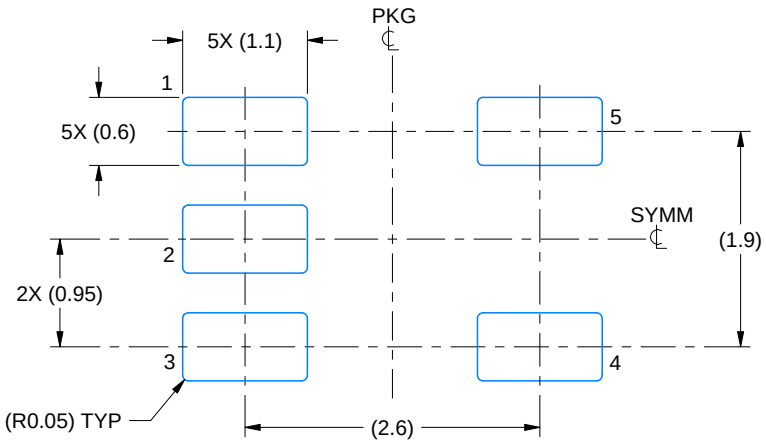
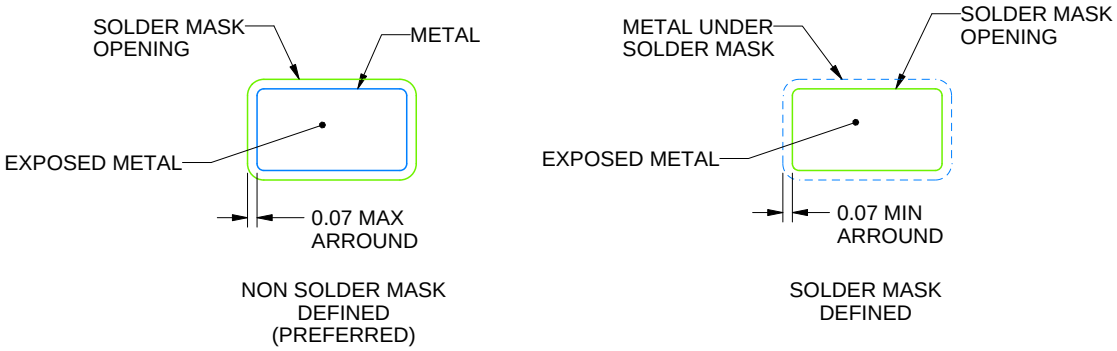
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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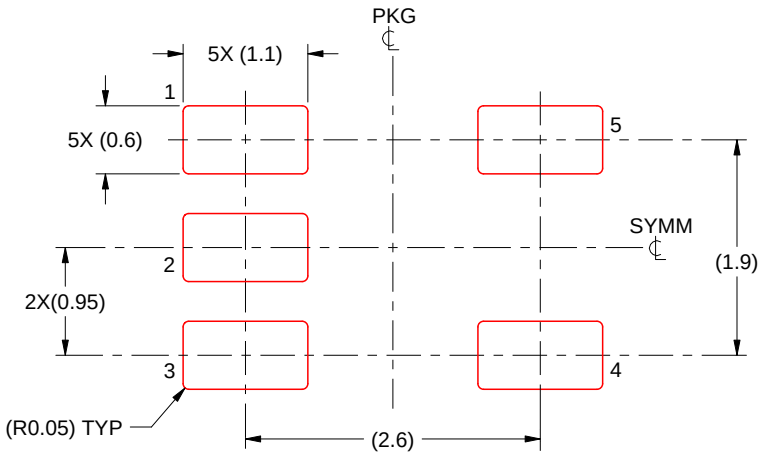
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月