

LP5907 250mA、低ノイズ、低 I_Q LDO

1 特長

- ポートフォリオの最新デバイスについては、[TPS7A20](#) を参照してください
- 入力電圧範囲: 2.2V~5.5V
- 出力電圧範囲: 1.2V~4.5V
- 1 μ F のセラミック入力および出力コンデンサで安定動作
- ノイズ バイパス コンデンサが不要
- 出力コンデンサのリモート配置
- 過熱および短絡保護
- 動作時接合部温度: -40°C~125°C
- 低い出力電圧ノイズ: 6.5 μ V_{RMS} 未満
- PSRR: 1kHz 時に 82dB
- 出力電圧許容誤差: \pm 2%
- 超低 I_Q (イネーブル): 12 μ A
- 低いドロップアウト: 120mV (標準値)
- [WEBENCH® Power Designer](#) により LP5907 を使用するカスタム設計を作成

2 アプリケーション

- [スマートフォン](#)
- [タブレット](#)
- [通信機器](#)
- [デジタル スチル カメラ](#)
- [ファクトリ オートメーション](#)

3 概要

LP5907 は、最大 250mA の出力電流を供給できる低ノイズ LDO です。RF/アナログ回路の要件を満たすよう設計された LP5907 は、低ノイズ、高 PSRR、低静止電流、高速ライン/負荷過渡応答といった特徴を備えています。革新的な設計手法の採用により、ノイズ バイパス用コンデンサなしでクラス最高レベルの優れたノイズ特性を実現し、出力コンデンサのリモート配置にも対応します。

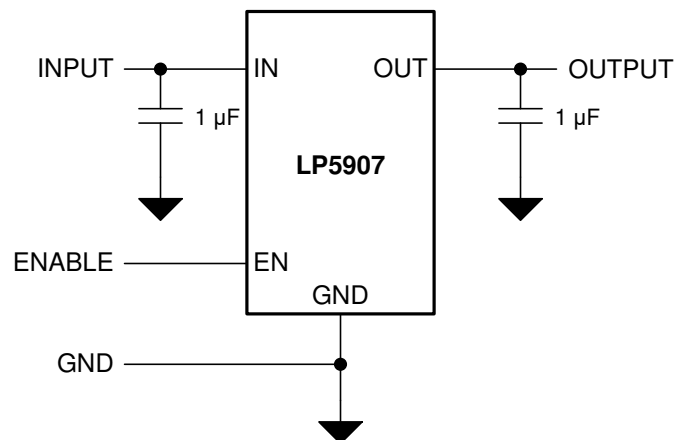
このデバイスは、入力および出力に 1 μ F のセラミック コンデンサを使用して動作するよう設計されています (個別にノイズ バイパス コンデンサを用意する必要はありません)。

このデバイスでは、1.2V~4.5V (25mV ステップ) の固定出力電圧を使用できます。具体的な電圧オプションについては、テキサス・インスツルメンツの販売部門までお問い合わせください。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
LP5907	YKE, YKG, YKM, YCR (DSBGA, 4)	0.685mm × 0.685mm
	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DQN (X2SON, 4)	1mm × 1mm

- (1) 詳細については、「[メカニカル、パッケージ、および注文情報](#)」を参照してください。
- (2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



Table of Contents

1 特長	1	6.4 Device Functional Modes.....	12
2 アプリケーション	1	7 Application and Implementation	13
3 概要	1	7.1 Application Information.....	13
4 Pin Configuration and Functions	3	7.2 Typical Application.....	13
5 Specifications	4	7.3 Power Supply Recommendations.....	16
5.1 Absolute Maximum Ratings.....	4	7.4 Layout.....	17
5.2 ESD Ratings.....	4	8 Device and Documentation Support	19
5.3 Recommended Operating Conditions.....	4	8.1 Documentation Support.....	19
5.4 Thermal Information.....	5	8.2 ドキュメントの更新通知を受け取る方法.....	19
5.5 Electrical Characteristics.....	5	8.3 サポート・リソース.....	19
5.6 Output and Input Capacitors.....	6	8.4 Trademarks.....	19
5.7 Typical Characteristics.....	7	8.5 静電気放電に関する注意事項.....	19
6 Detailed Description	11	8.6 用語集.....	19
6.1 Overview.....	11	9 Revision History	20
6.2 Functional Block Diagram.....	11	10 Mechanical, Packaging, and Orderable Information	20
6.3 Feature Description.....	11		

4 Pin Configuration and Functions

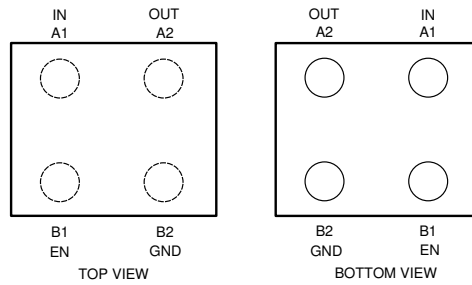


図 4-1. YKE, YKG, YKM, and YCR Packages, 4-Pin DSBGA

表 4-1. Pin Functions: DSBGA

PIN		TYPE	DESCRIPTION
DSBGA	NAME		
A1	IN	I	Input voltage supply. Connect a 1μF capacitor at this input.
A2	OUT	O	Regulated output voltage. Connect a minimum 1μF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
B1	EN	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230Ω pulldown resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1MΩ pulldown resistor to hold the regulator off by default.
B2	GND	—	Common ground

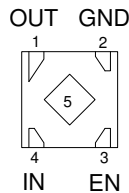


図 4-2. DQN Package, 4-Pin X2SON (Bottom View)

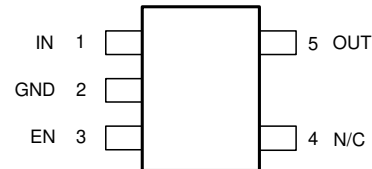


図 4-3. DBV Package, 5-Pin SOT-23 (Top View)

表 4-2. Pin Functions: X2SON, SOT-23

PIN			TYPE	DESCRIPTION
NAME	X2SON	SOT-23		
EN	3	3	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230Ω pulldown resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1MΩ pulldown resistor to hold the regulator off by default.
GND	2	2	—	Common ground.
IN	4	1	I	Input voltage supply. Connect a 1μF capacitor at this input.
N/C	—	4	—	No internal electrical connection.
OUT	1	5	O	Regulated output voltage. Connect a minimum 1μF low-ESR capacitor to this pin. Connect this output to the load circuit. An internal 230Ω (typical) pulldown resistor prevents a charge remaining on V_{OUT} when the regulator is in shutdown mode (V_{EN} low).
Thermal Pad	5	—	—	Thermal pad for the X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
V _{IN}	Input voltage	-0.3	6	V
V _{OUT}	Output voltage	-0.3	See ⁽²⁾	V
V _{EN}	Enable input voltage	-0.3	6	V
	Continuous power dissipation ⁽⁴⁾	Internally limited		W
T _{JMAX}	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Abs Max V_{OUT} is the lessor of V_{IN} + 0.3V, or 6V.
- (3) All voltages are with respect to the GND pin.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Input supply voltage	2.2	5.5	V
V _{EN}	Enable input voltage	0	5.5	V
I _{OUT}	Output current	0	250	mA
T _J	Junction temperature	-40	125	°C
T _A	Ambient temperature ⁽³⁾	-40	85	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) In applications where high power dissipation and poor package thermal resistance is present, the maximum ambient temperature can need to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the device or package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}). See the [Application and Implementation](#) section.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP5907						UNIT
		DBV (SOT-23)	DQN (X2SON)	YCR (DSBGA)	YKE (DSBGA)	YKG (DSBGA)	YKM (DSBGA)	
		5 PINS	4 PINS	4 PINS	4 PINS	4 PINS	4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	193.4	216.1	189.4	206.1	191.6	194.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	102.1	161.7	2.4	1.5	2.4	3.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	45.8	162.1	56.6	37.0	58.9	62.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.4	5.1	1.1	15.0	1.1	1.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	45.3	161.7	56.5	36.8	58.9	62.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

V_{IN} = V_{OUT(NOM)} + 1V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1μF, and C_{OUT} = 1μF (unless otherwise noted)^{(1) (2) (3)}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage	T _A = 25°C	2.2		5.5	V
ΔV _{OUT}	Output voltage tolerance	V _{IN} = (V _{OUT(NOM)} + 1V) to 5.5V, I _{OUT} = 1mA to 250mA	-2		2	%V _{OUT}
		V _{IN} = (V _{OUT(NOM)} + 1V) to 5.5V, I _{OUT} = 1mA to 250mA (V _{OUT} < 1.8V, SOT-23, X2SON packages)	-3		3	
	Line regulation	V _{IN} = (V _{OUT(NOM)} + 1V) to 5.5V, I _{OUT} = 1mA		0.02		%/V
	Load regulation	I _{OUT} = 1mA to 250mA		0.001		%/mA
I _{LOAD}	Load current	See ⁽⁴⁾	0		250	mA
	Maximum output current		250			
I _Q	Quiescent current ⁽⁵⁾	V _{EN} = 1.2V, I _{OUT} = 0mA		12	25	μA
		V _{EN} = 1.2V, I _{OUT} = 250mA		250	425	
		V _{EN} = 0.3V (disabled)		0.2	1	
I _G	Ground current ⁽⁶⁾	V _{EN} = 1.2V, I _{OUT} = 0mA		14		μA
V _{DO}	Dropout voltage ⁽⁷⁾	I _{OUT} = 100mA		50		mV
		I _{OUT} = 250mA (DSBGA package)		120	200	
		I _{OUT} = 250mA (SOT-23, X2SON packages)			250	
I _{SC}	Short-circuit current limit	T _A = 25°C ⁽⁸⁾	250	500		mA
PSRR	Power-supply rejection ratio ⁽⁹⁾	f = 100Hz, I _{OUT} = 20mA		90		dB
		f = 1kHz, I _{OUT} = 20mA		82		
		f = 10kHz, I _{OUT} = 20mA		65		
		f = 100kHz, I _{OUT} = 20mA		60		
e _N	Output noise voltage ⁽⁹⁾	BW = 10Hz to 100kHz	I _{OUT} = 1mA		10	μV _{RMS}
			I _{OUT} = 250mA		6.5	
R _{AD}	Output automatic discharge pulldown resistance	V _{EN} < V _{IL} (output disabled)		230		Ω
T _{SD}	Thermal shutdown	T _J rising		160		°C
	Thermal hysteresis	T _J falling from shutdown		15		
LOGIC INPUT THRESHOLDS						

5.5 Electrical Characteristics (続き)

$V_{IN} = V_{OUT(NOM)} + 1V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, and $C_{OUT} = 1\mu F$ (unless otherwise noted)^{(1) (2) (3)}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low input threshold	$V_{IN} = 2.2V$ to $5.5V$, V_{EN} falling until the output is disabled			0.4	V
V_{IH}	High input threshold	$V_{IN} = 2.2V$ to $5.5V$ V_{EN} rising until the output is enabled	1.2			V
I_{EN}	Input current at EN pin ⁽¹⁰⁾	$V_{EN} = 5.5V$ and $V_{IN} = 5.5V$		5.5		μA
		$V_{EN} = 0V$ and $V_{IN} = 5.5V$		0.001		
TRANSIENT CHARACTERISTICS						
ΔV_{OUT}	Line transient ⁽⁹⁾	$V_{IN} = (V_{OUT(NOM)} + 1V)$ to $(V_{OUT(NOM)} + 1.6V)$ in $30\mu s$	-1			mV
		$V_{IN} = (V_{OUT(NOM)} + 1.6V)$ to $(V_{OUT(NOM)} + 1.6V)$ in $30\mu s$			1	
	Load transient ⁽⁹⁾	$I_{OUT} = 1mA$ to $250mA$ in $10\mu s$	-40			
		$I_{OUT} = 250mA$ to $1mA$ in $10\mu s$			40	
	Overshoot on start-up ⁽⁹⁾	Stated as a percentage of $V_{OUT(NOM)}$			5%	
Overshoot on start-up with EN ⁽⁹⁾	Stated as a percentage of $V_{OUT(NOM)}$, $V_{IN} = V_{OUT} + 1V$ to $5.5V$, $0.7\mu F < C_{OUT} < 10\mu F$, $0mA < I_{OUT} < 250mA$, EN rising until the output is enabled			1%		
t_{ON}	Turn-on time	From $V_{EN} > V_{IH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$, $T_A = 25^\circ C$		80	150	μs

- (1) All voltages are with respect to the device GND terminal, unless otherwise stated.
- (2) Minimum and maximum limits are specified through test, design, or statistical correlation over the junction temperature (T_J) range of $-40^\circ C$ to $125^\circ C$, unless otherwise stated. Typical values represent the most likely parametric norm at $T_A = 25^\circ C$, and are provided for reference purposes only.
- (3) In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature can possibly have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ C$), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$. See the [Application and Implementation](#) section.
- (4) The device maintains a stable, regulated output voltage without a load current.
- (5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT} .
- (6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
- (7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below the nominal value.
- (8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100mV below the nominal voltage.
- (9) This specification is verified by design.
- (10) There is a $1M\Omega$ resistor between EN and ground on the device.

5.6 Output and Input Capacitors

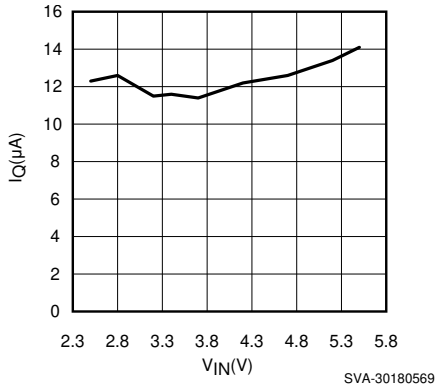
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX	UNIT
C_{IN}	Input capacitance ⁽²⁾	Capacitance for stability	0.7	1		μF
C_{OUT}	Output capacitance ⁽²⁾		0.7	1	10	μF
ESR	Output/Input capacitance ⁽²⁾		5		500	m Ω

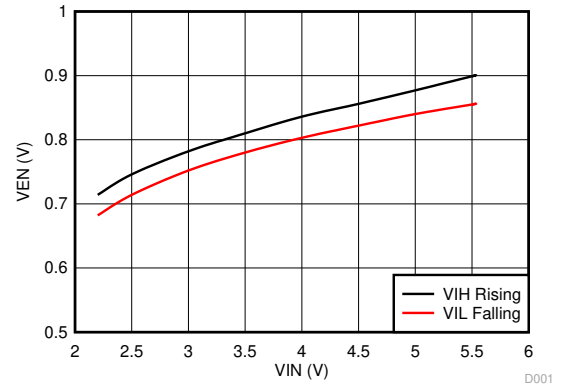
- (1) The minimum capacitance must be greater than $0.5\mu F$ over the full range of operating conditions. The capacitor tolerance must be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application must be considered during device selection to make sure this minimum capacitance specification is met. X7R capacitors are recommended, however capacitor types X5R, Y5V, and Z5U can be used with consideration of the application and conditions.
- (2) This specification is verified by design.

5.7 Typical Characteristics

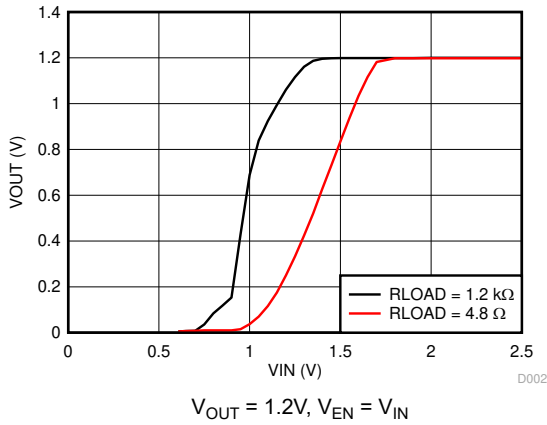
$V_{IN} = 3.7V$, $V_{OUT} = 2.8V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)



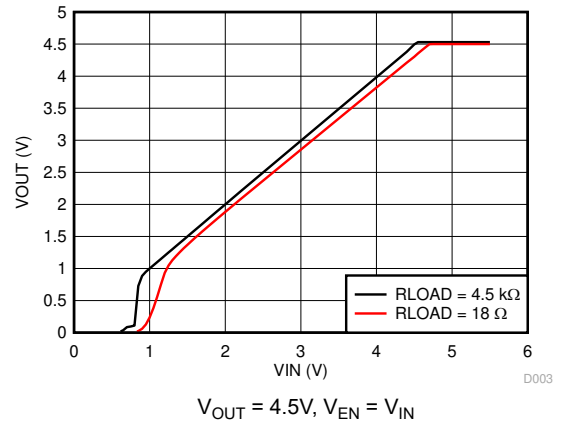
5-1. Quiescent Current vs Input Voltage



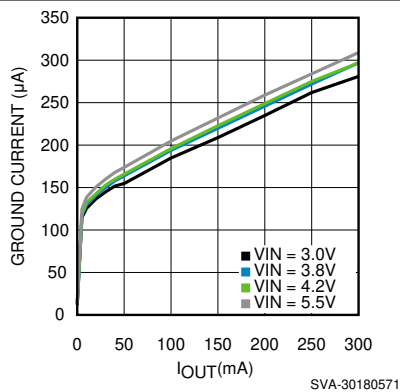
5-2. V_{EN} Thresholds vs V_{IN}



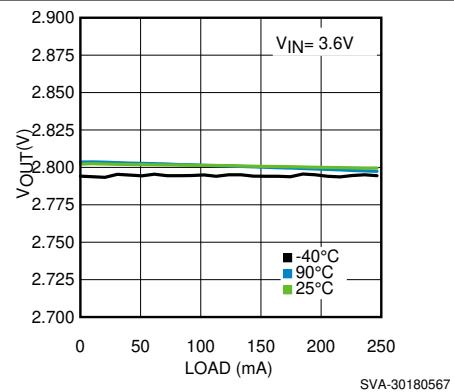
5-3. V_{OUT} vs V_{IN}



5-4. V_{OUT} vs V_{IN}



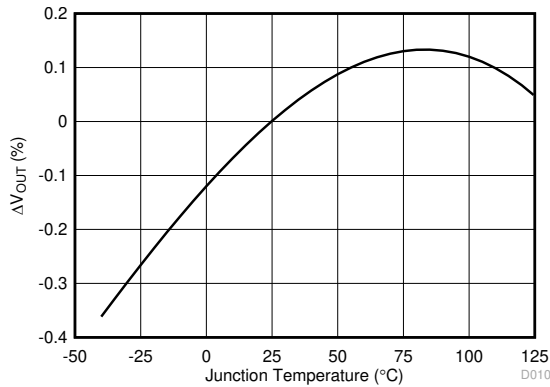
5-5. Ground Current vs Output Current



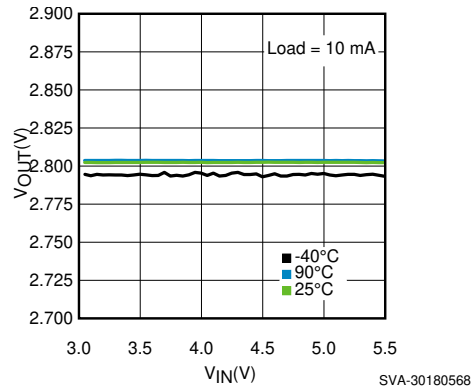
5-6. Load Regulation

5.7 Typical Characteristics (continued)

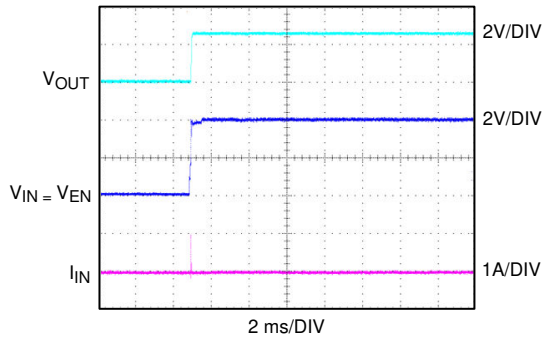
$V_{IN} = 3.7V$, $V_{OUT} = 2.8V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)



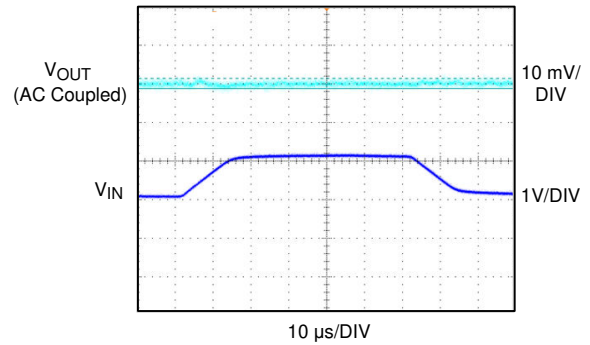
5-7. ΔV_{OUT} vs Temperature



5-8. Line Regulation

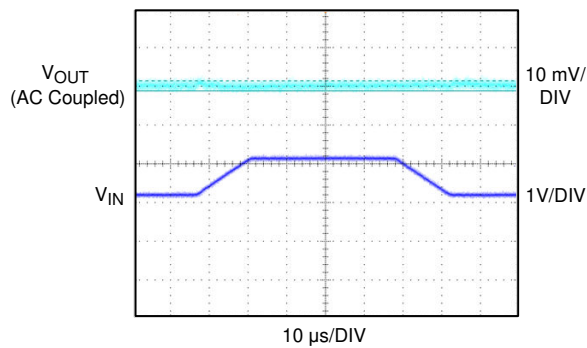


5-9. Inrush Current



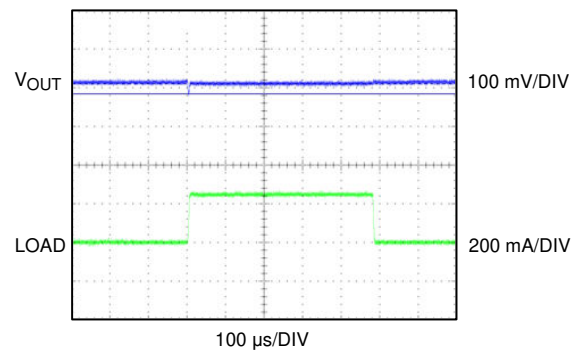
$V_{IN} = 3.2V \leftrightarrow 4.2V$, load = 1mA

5-10. Line Transient



$V_{IN} = 3.2V \leftrightarrow 4.2V$, load = 250mA

5-11. Line Transient

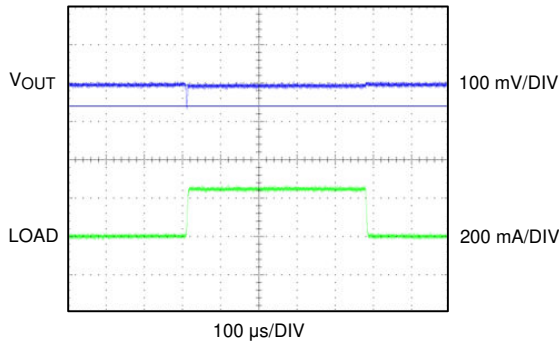


Load = 0mA \leftrightarrow 250mA, $-40^\circ C$

5-12. Load Transient

5.7 Typical Characteristics (continued)

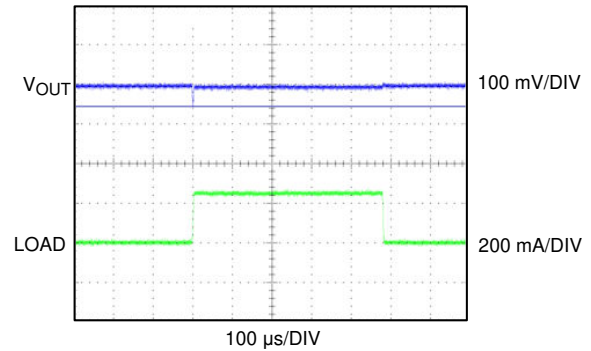
$V_{IN} = 3.7V$, $V_{OUT} = 2.8V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)



SVA-30180513

Load = 0mA ↔ 250mA, 90°C

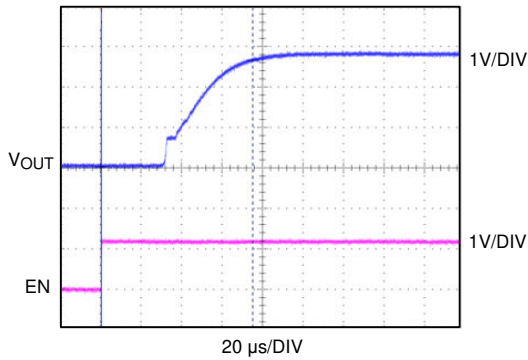
☒ 5-13. Load Transient



SVA-30180514

Load = 0mA ↔ 250mA, 25°C

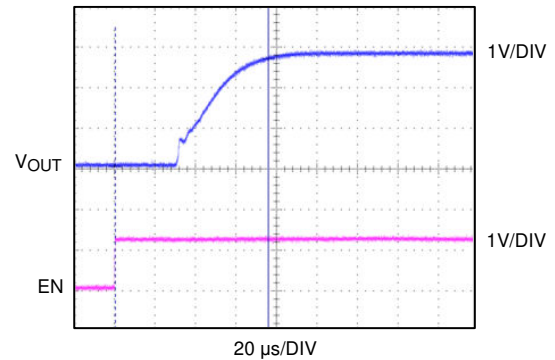
☒ 5-14. Load Transient



SVA-30180515

Load = 0mA

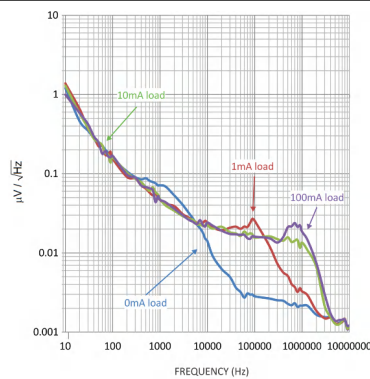
☒ 5-15. Start-Up



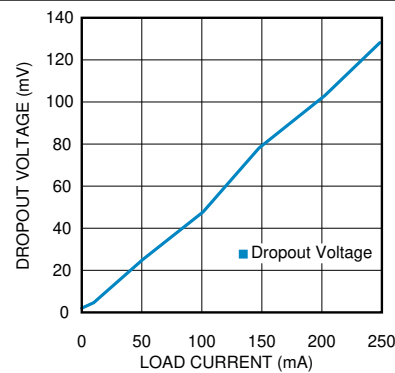
SVA-30180516

Load = 250mA

☒ 5-16. Start-Up



☒ 5-17. Noise Density Test

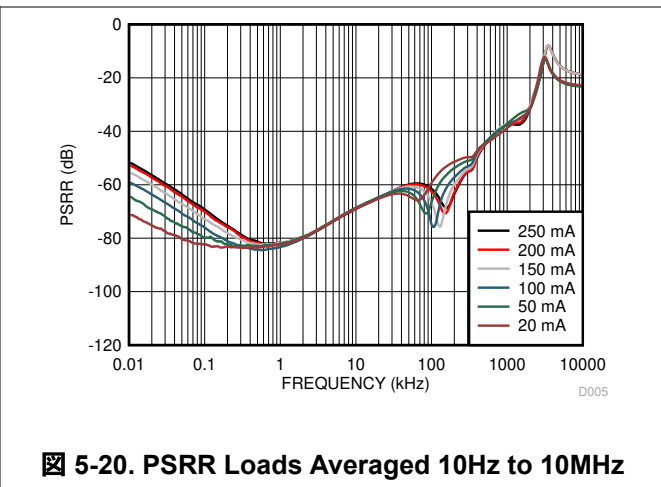
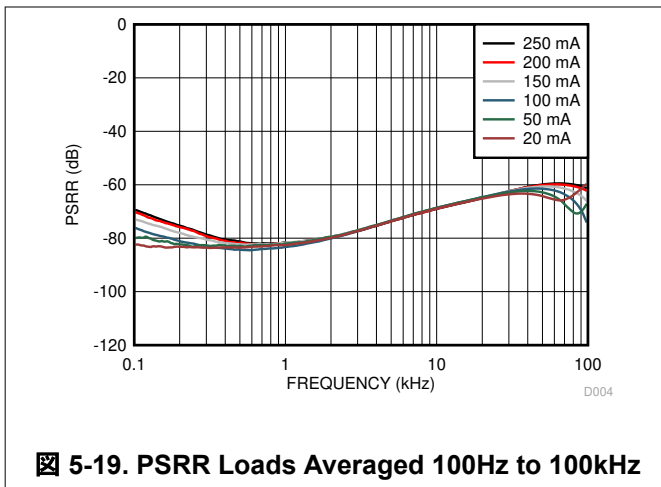


SVA-30180573

☒ 5-18. Dropout Voltage vs Load Current

5.7 Typical Characteristics (continued)

$V_{IN} = 3.7V$, $V_{OUT} = 2.8V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, and $T_A = 25^\circ C$ (unless otherwise noted)



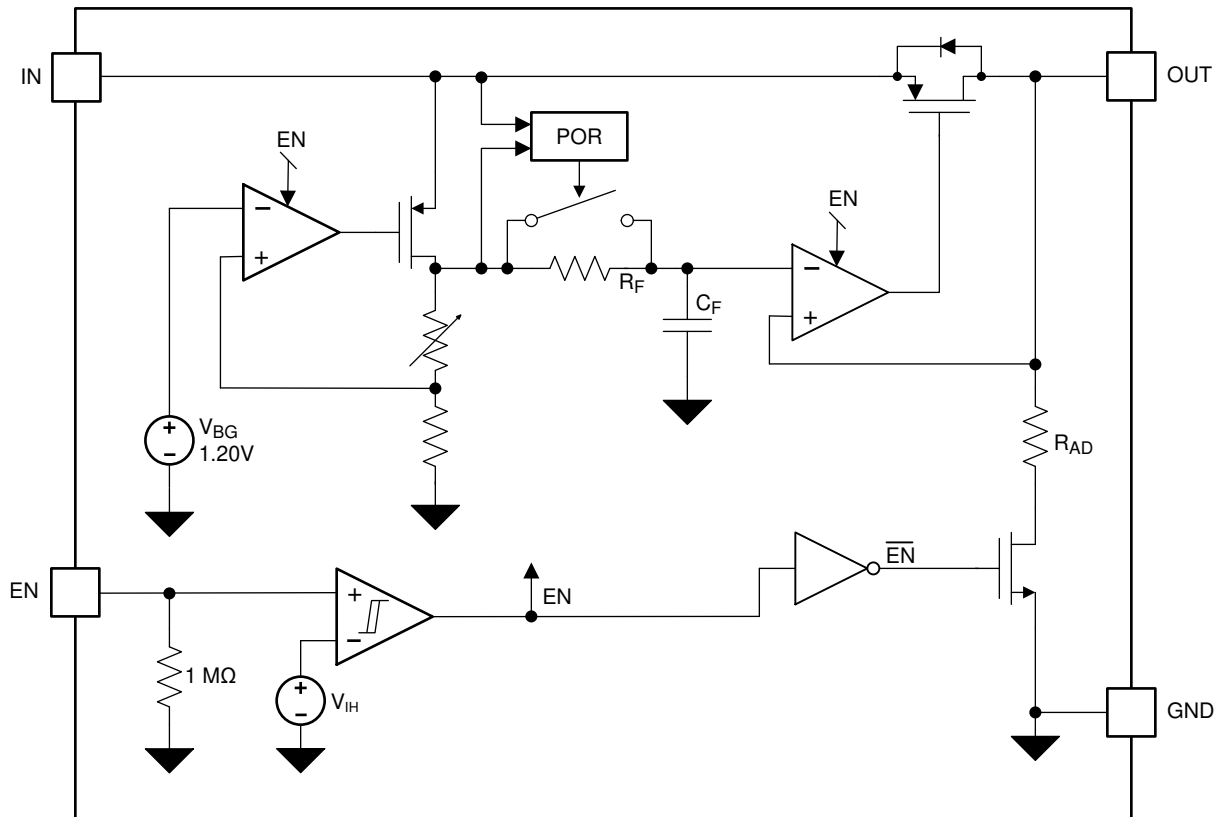
6 Detailed Description

6.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, and low line and load transient response figures. Using innovative design techniques, the LP5907 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907 is designed to perform with a single $1\mu\text{F}$ input capacitor and a single $1\mu\text{F}$ ceramic output capacitor. With a reasonable PCB layout, the single $1\mu\text{F}$ ceramic output capacitor can be placed up to 10cm away from the LP5907 device.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Enable (EN)

The LP5907 EN pin is internally held low by a $1\text{M}\Omega$ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to make sure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to make sure that the device is fully disabled and the automatic output discharge is activated.

6.3.2 Low Output Noise

Any internal noise at the LP5907 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a -3-dB cut-off frequency of approximately 0.1Hz .

6.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230Ω (typical) pulldown resistance to discharge the output when the EN pin is low and the device is disabled.

6.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1 μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the OUT pin. In practical designs, the output capacitor can be located up to 10cm away from the LDO.

6.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C, which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This thermal cycling limits the dissipation of the regulator, and protects the regulator from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 is designed to protect against temporary thermal overload conditions. The T_{SD} circuitry is not intended to replace proper heat-sinking. Continuously running the LP5907 into thermal shutdown can degrade device reliability.

6.4 Device Functional Modes

6.4.1 Enable (EN)

The LP5907 enable (EN) pin is internally held low by a 1M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to make sure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230 Ω (typical) pulldown resistance.

6.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2V or ($V_{OUT} + V_{DO}$).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of $1\mu\text{F}$. The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of -40°C to 125°C .

7.2 Typical Application

図 7-1 shows the typical application circuit for the LP5907. Input and output capacitances can be increased, if needed, above the $1\mu\text{F}$ minimum for some applications.

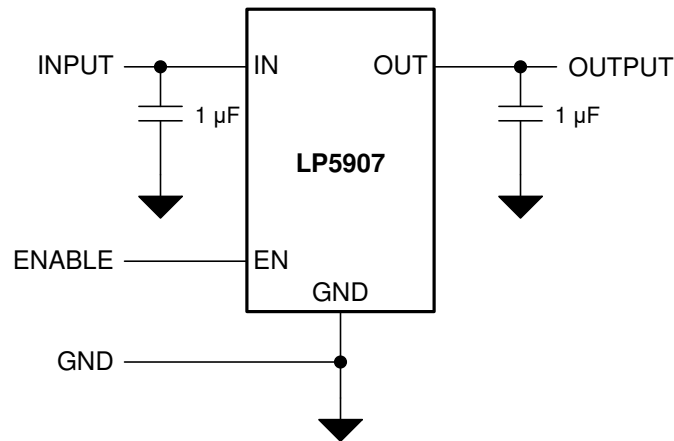


図 7-1. LP5907 Typical Application

7.2.1 Design Requirements

表 7-1 summarizes the design requirements for 図 7-1.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2V to 5.5V
Output voltage	1.8V
Output current	200mA
Output capacitor range	$0.7\mu\text{F}$ to $10\mu\text{F}$
Input/output capacitor ESR range	$5\text{m}\Omega$ to $500\text{m}\Omega$

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the LP5907 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [式 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by [式 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed in regards to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Use these two equations to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) can be increased.

In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) can be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the device or package in the application ($R_{\theta JA}$), as given by [式 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if T_{A-MAX} cannot be derated, the P_D value must be reduced. This reduction can be accomplished by reducing V_{IN} in the $V_{IN}-V_{OUT}$ term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

7.2.2.3 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

7.2.2.4 Input Capacitor

An input capacitor is required for stability. The input capacitor must be at least equal to, or greater than, the output capacitor for good load transient performance. Connect at least a 1 μ F capacitor between the LP5907 input pin and ground for stable operation over the full load current range. Basically, having more output capacitance than input is acceptable, as long as the input is at least 1 μ F.

The input capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor can be used at the input.

注

To provide stable operation, good PCB practices must be used to minimize ground impedance and to keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP5907, increase the input capacitor to at least 10 μ F. Also, tantalum capacitors can suffer catastrophic failures resulting from surge current when connected to a low-impedance source of power (such as a battery or a very large capacitor). If a tantalum capacitor is used at the input, verify by the manufacturer that the capacitor has a surge current rating sufficient for the application. The initial tolerance, applied voltage derating, and temperature coefficient must all be considered when selecting the input capacitor to make sure that the actual capacitance is never less than 0.7 μ F over the entire operating range.

7.2.2.5 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 μ F. A ceramic capacitor (dielectric types X5R or X7R) in the 1 μ F to 10 μ F range, and with ESR between 5m Ω to 500m Ω , is suitable in the LP5907 application circuit. For this device, connect the output capacitor between the OUT pin with a good connection back to the GND pin.

Tantalum or film capacitors can also be used at the device output, V_{OUT} , but these are not as attractive for reasons of size and cost (see the [Capacitor Characteristics](#) section).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range of 5m Ω to 500m Ω for stability. Like the input capacitor, the initial tolerance, applied voltage derating, and temperature coefficient must all be considered when selecting the input capacitor to make sure that the actual capacitance is never less than 0.7 μ F over the entire operating range.

7.2.2.6 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits these components offer. For capacitance values in the range of 1 μ F to 10 μ F, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high-frequency noise. The ESR of a typical 1 μ F ceramic capacitor is in the range of 20m Ω to 40m Ω , which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within $\pm 15\%$ over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μ F to 10 μ F range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. Which means that although a tantalum capacitor can possibly be found with an ESR value within the stable range, the capacitor must be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases by approximately 2:1 when the temperature goes from 25 $^{\circ}$ C down to -40 $^{\circ}$ C, so some guard band must be allowed.

7.2.2.7 Remote Capacitor Operation

The LP5907 requires at least a 1 μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor can be located up to 10cm away from the LDO. Which means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (such as a capacitor at the input of supplied device). The remote capacitor feature helps minimize the number of capacitors in the system.

In general, keep the wiring parasitic inductance at a minimum, which means use traces as wide as possible from the LDO output to the capacitors, thus keeping the LDO output trace layer as close to ground layer as possible and avoiding vias on the path. If vias must be used, use as many vias as possible between the connection layers. Keep parasitic wiring inductance less than 35nH. For applications with fast load transients, use an input capacitor equal to or larger to the sum of the capacitance at the output node for best load transient performance.

7.2.2.8 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

7.2.2.9 Enable Control

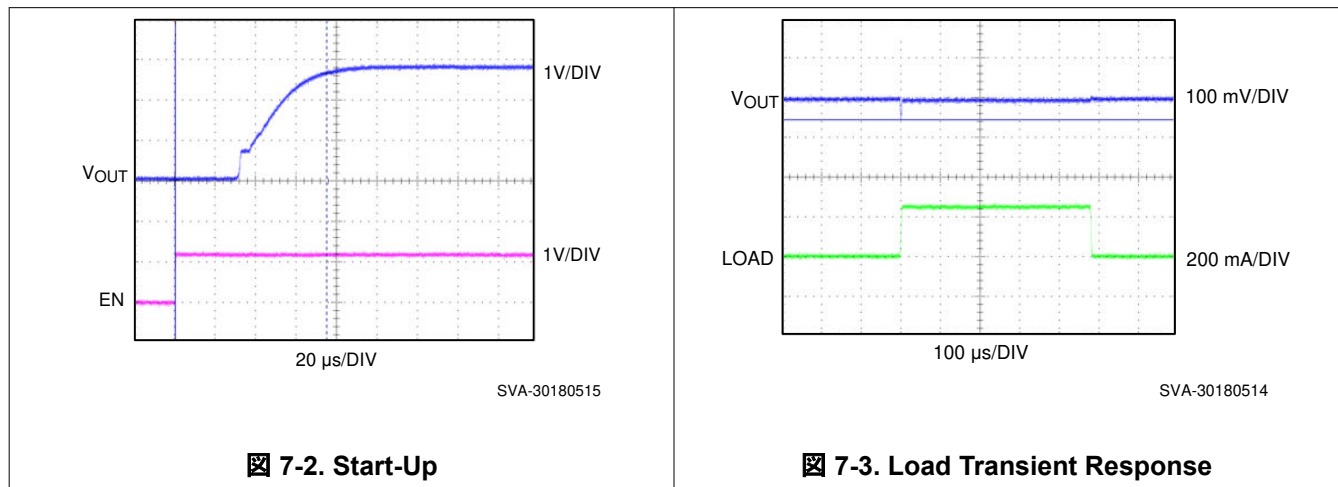
The LP5907 can be switched on or off by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, and a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 μ A. Additionally, an output pulldown circuit is activated that makes sure any charge stored on C_{OUT} is discharged to ground.

If the application does not require the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1M Ω pulldown resistor ties the EN input to ground, making sure the device remains off if the EN pin is left open circuit. To provide proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on or turn-off voltage thresholds listed in the [Electrical Characteristics](#) under V_{IL} and V_{IH} .

7.2.3 Application Curves



7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2V to 5.5V. The input supply must be well regulated and free of spurious noise. To make sure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT} + 1V$. A minimum capacitor value of 1 μ F is required to be within 1cm of the IN pin.

7.4 Layout

7.4.1 Layout Guidelines

The dynamic performance of the LP5907 is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs can degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close to the package as practical. The ground connections for C_{IN} and C_{OUT} must route back to the LP5907 ground pin using as wide and short of a copper trace as practical.

Connections using long trace lengths, narrow trace widths, and connections through vias must be avoided. These connections add parasitic inductances and resistance that results in inferior performance, especially during transient conditions.

7.4.1.1 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the [QFN/SON PCB Attachment application note](#).

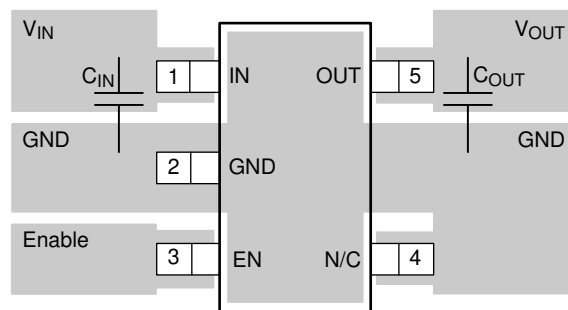
7.4.1.2 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in [AN-1112 DSBGA Wafer Level Chip Scale Package application note](#). For best results during assembly, alignment ordinals on the PC board can be used to facilitate placement of the DSBGA device.

7.4.1.3 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light can cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if these sources are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

7.4.2 Layout Examples



☒ 7-4. SOT-23 Typical Layout

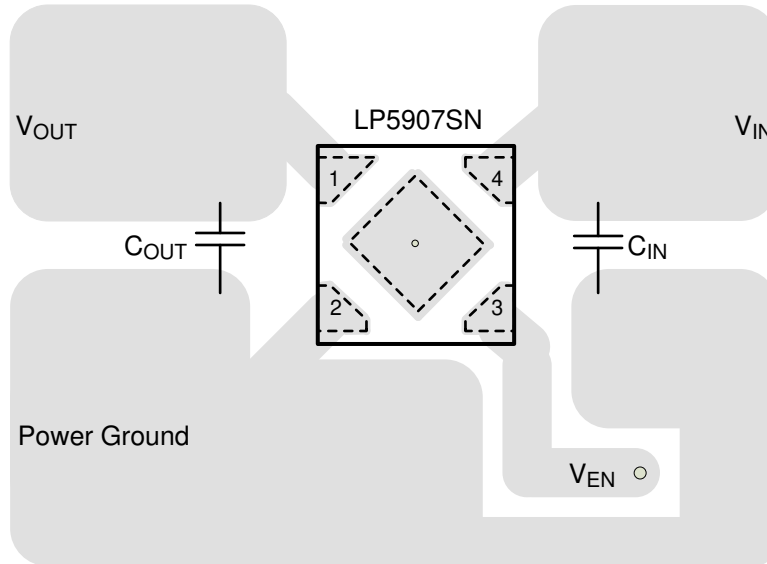


図 7-5. X2SON Typical Layout

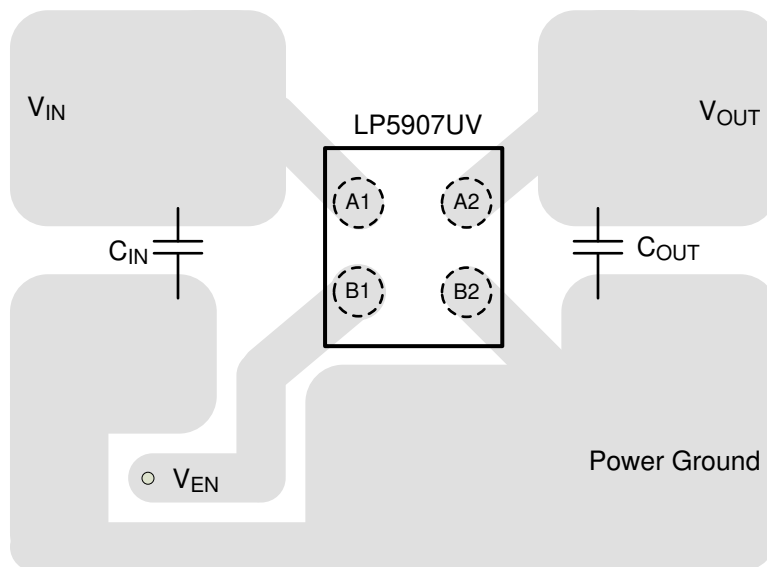


図 7-6. DSBGA Typical Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LP5907 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.1.2 Related Documentation

For related documentation, see the following:

- Texas Instruments, [AN-1112 DSBGA Wafer Level Chip Scale Package application note](#)
- Texas Instruments, [QFN/SON PCB Attachment application note](#)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

WEBENCH® is a registered trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision O (June 2020) to Revision P (January 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• Added YCR to pinout caption of <i>Pin Configuration and Functions</i> section.....	3
• Added YCR column to <i>Thermal Information</i> table.....	5

Changes from Revision N (April 2018) to Revision O (June 2020)	Page
• 「アプリケーション」セクションを変更	1
• 「製品情報」の表の DSBGA 本体サイズを変更	1
• Added YKG to pinout caption of <i>Pin Configuration and Functions</i> section.....	3
• Added YKG column to <i>Thermal Information</i> table.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5907A28YKMR	Active	Production	DSBGA (YKM) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 125	Q
LP5907A33YKMR	Active	Production	DSBGA (YKM) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 125	N
LP5907MFX-1.2/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLTB
LP5907MFX-1.5/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LN8B
LP5907MFX-1.8/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLUB
LP5907MFX-2.5/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LN7B
LP5907MFX-2.8/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLYB
LP5907MFX-2.9/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1E5X
LP5907MFX-3.0/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLZB
LP5907MFX-3.1/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LN5B
LP5907MFX-3.2/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LN6B
LP5907MFX-3.3/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLVB
LP5907MFX-4.5/NOPB	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LLXB
LP5907SNX-1.2/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
LP5907SNX-1.8/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG
LP5907SNX-1.9	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3Z
LP5907SNX-2.2/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP
LP5907SNX-2.5/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9
LP5907SNX-2.7/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH
LP5907SNX-2.75	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HI
LP5907SNX-2.8/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI
LP5907SNX-2.9/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV
LP5907SNX-3.0/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK
LP5907SNX-3.1/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
LP5907SNX-3.2/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM
LP5907SNX-3.3/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN
LP5907SNX-4.0/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU
LP5907SNX-4.5/NOPB	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO
LP5907UVE-1.2/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5907UVE-1.8/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S
LP5907UVE-2.8/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U
LP5907UVE-3.0/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
LP5907UVE-3.1/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X
LP5907UVE-3.2/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
LP5907UVE-3.3/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D
LP5907UVE-4.5/NOPB	Active	Production	DSBGA (YKE) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z
LP5907UVX-1.2/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R
LP5907UVX-1.8/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S
LP5907UVX-2.5/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E
LP5907UVX-2.8/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U
LP5907UVX-3.0/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B
LP5907UVX-3.1/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X
LP5907UVX-3.2/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C
LP5907UVX-3.3/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SAC396 SNAGCU	Level-1-260C-UNLIM	-40 to 125	D
LP5907UVX-4.5/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z
LP5907UVX19/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8
LP5907UVX37/NOPB	Active	Production	DSBGA (YKE) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP5907YKGR-2.8	Active	Production	DSBGA (YKG) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 125	3
LP5907YKGR-2.825	Active	Production	DSBGA (YKG) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 125	5
LP5907YKGR-2.85	Active	Production	DSBGA (YKG) 4	3000 LARGE T&R	Yes	SAC396	Level-1-260C-UNLIM	-40 to 125	P

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5907 :

- Automotive : [LP5907-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907A28YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A33YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	2.0	8.0	Q1
LP5907YKGR-2.8	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.825	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1
LP5907YKGR-2.85	DSBGA	YKG	4	3000	178.0	9.2	0.72	0.72	0.39	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907A28YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A33YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.9	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.75	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.75	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	210.0	185.0	35.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	208.0	191.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	208.0	191.0	35.0
LP5907YKGR-2.8	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.825	DSBGA	YKG	4	3000	220.0	220.0	35.0
LP5907YKGR-2.85	DSBGA	YKG	4	3000	220.0	220.0	35.0

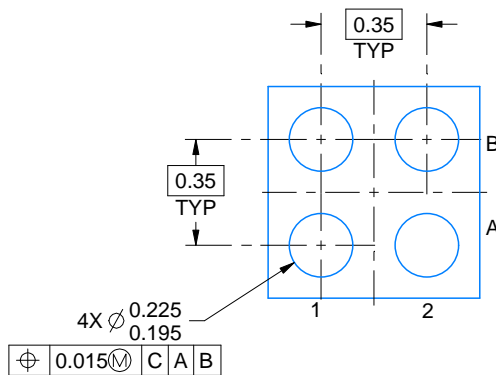
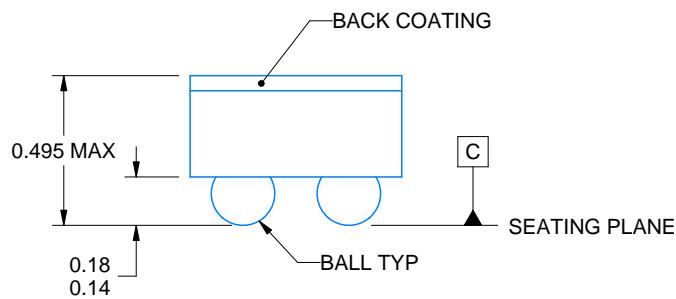
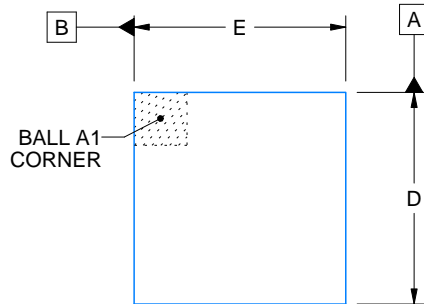
YKM0004



PACKAGE OUTLINE

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min = 0.615 mm
 E: Max = 0.675 mm, Min = 0.615 mm

4223494/A 11/2014

NOTES:

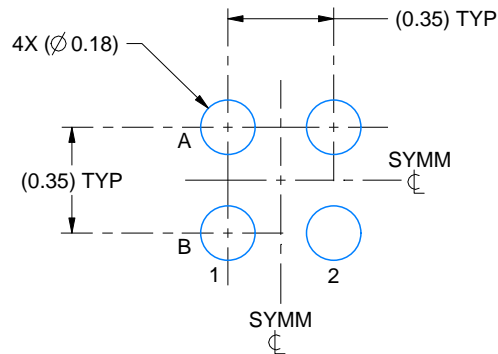
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

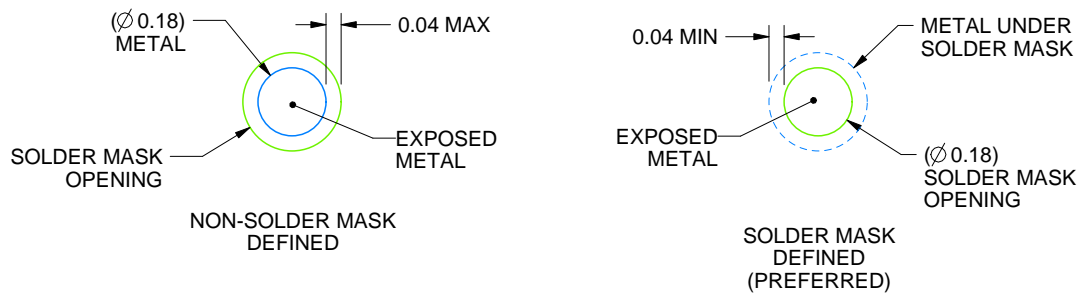
YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223494/A 11/2014

NOTES: (continued)

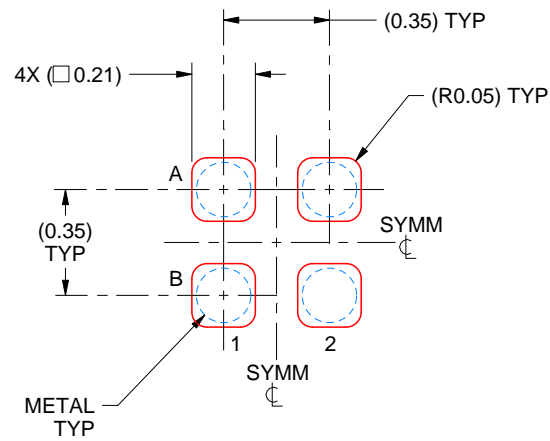
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKM0004

DSBGA - 0.495 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4223494/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

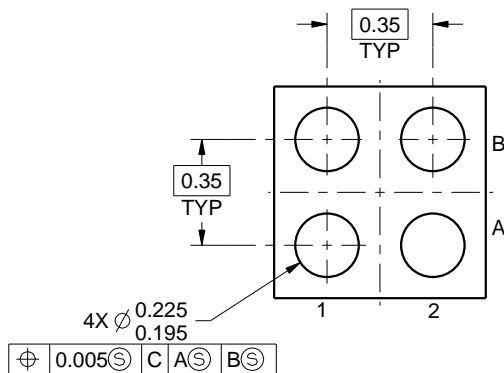
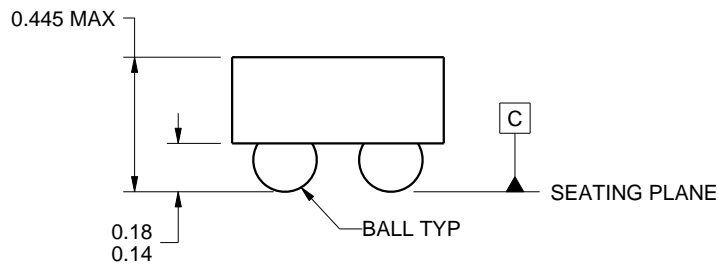
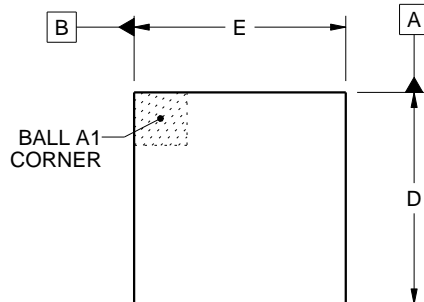


YKE0004

PACKAGE OUTLINE

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min = 0.615 mm
E: Max = 0.675 mm, Min = 0.615 mm

4220102/A 11/2014

NOTES:

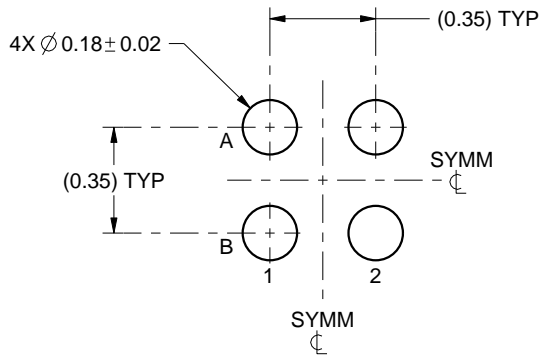
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

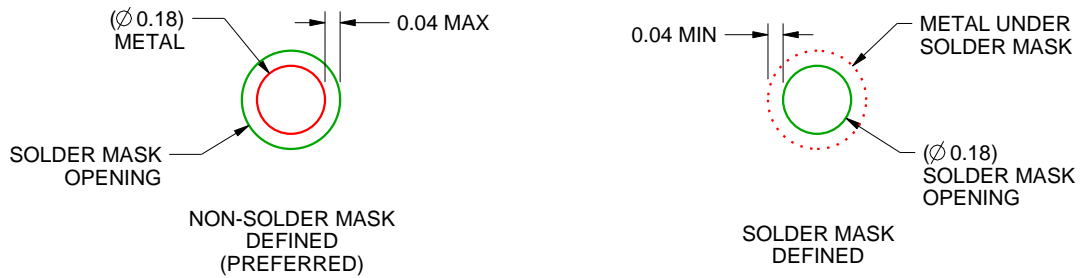
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4220102/A 11/2014

NOTES: (continued)

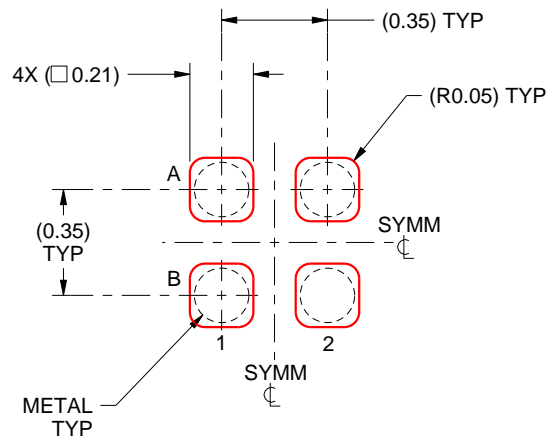
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY

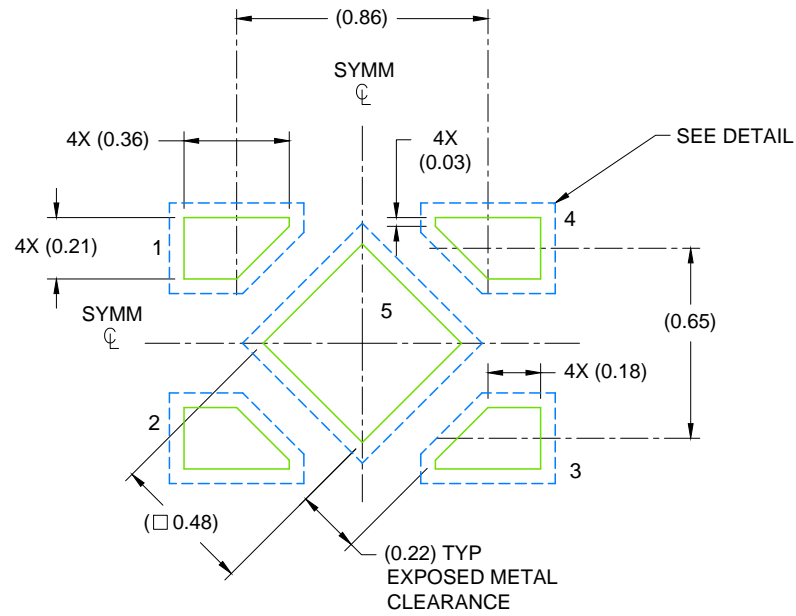


SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

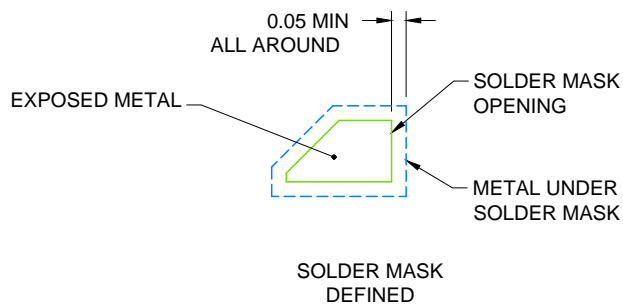
4220102/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



LAND PATTERN EXAMPLE
SCALE: 40X

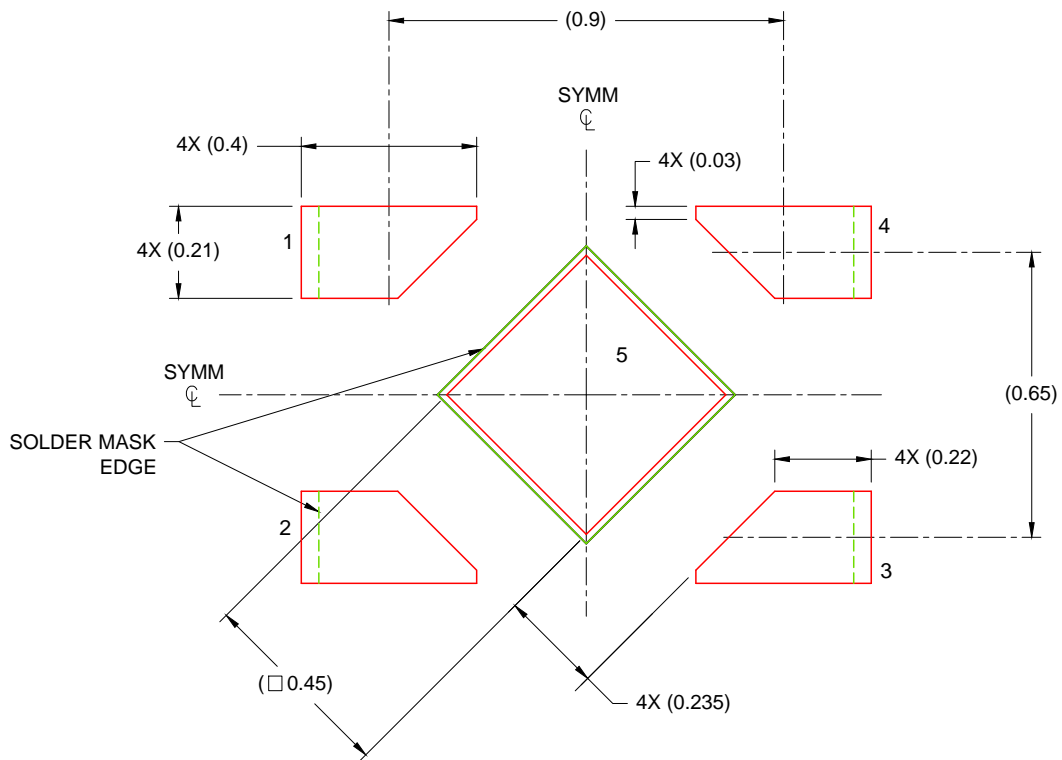


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.075 - 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

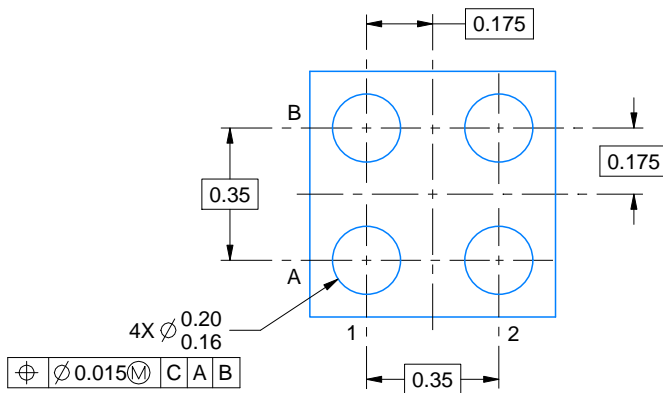
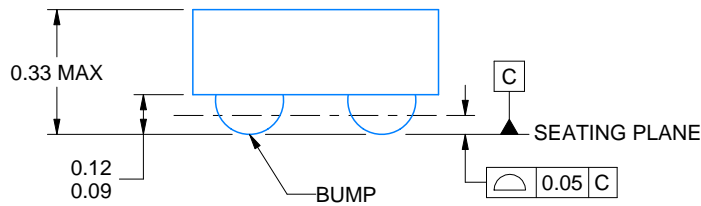
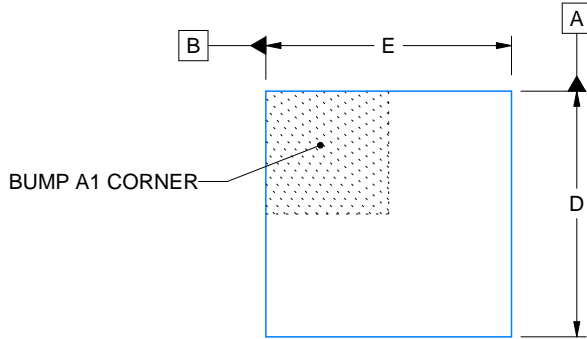
YKG0004



PACKAGE OUTLINE

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min = 0.615 mm
 E: Max = 0.675 mm, Min = 0.615 mm

4218366/E 05/2020

NOTES:

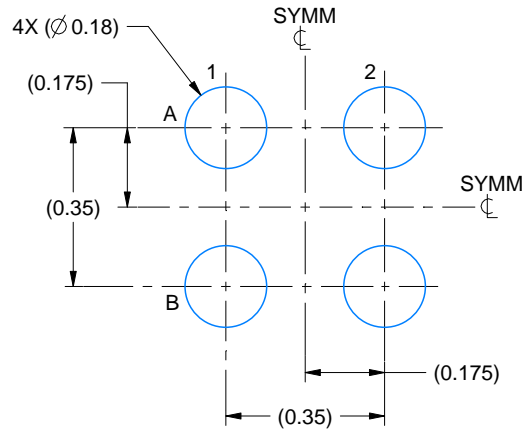
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

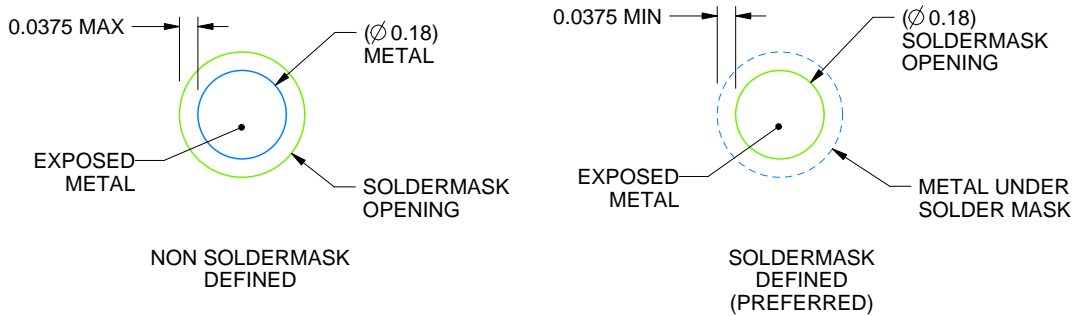
YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDERMASK DETAILS
NOT TO SCALE

4218366/E 05/2020

NOTES: (continued)

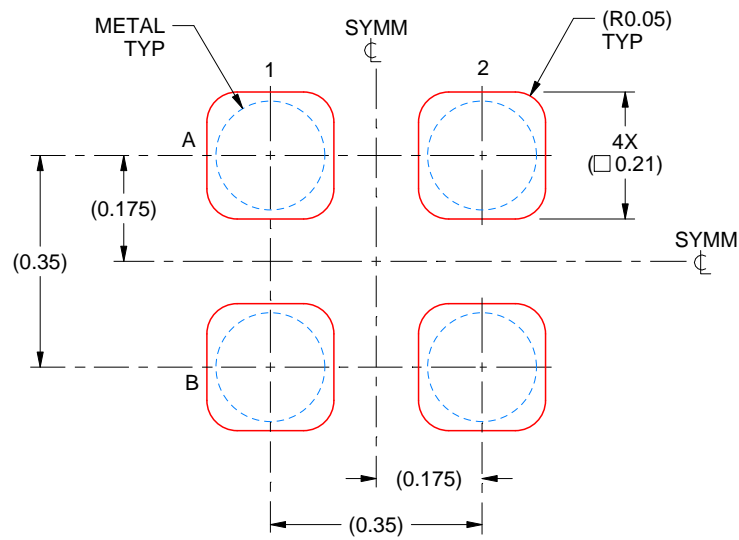
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKG0004

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



SOLDERPASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE:80X

4218366/E 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、ます。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated