

3V~5.5V、マルチチャンネル RS-232 ラインドライバおよびレシーバ、±15kV ESD 保護

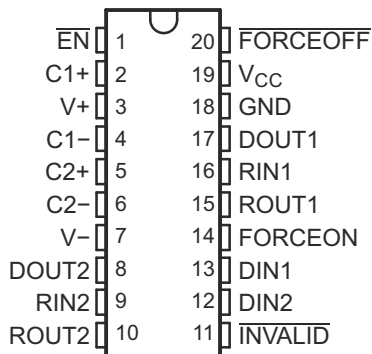
1 特長

- RS-232 バス・ピン用 ESD 保護機能
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC 61000-4-2、接触放電
 - ±15kV IEC 61000-4-2、エアギャップ放電
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V~5.5V の V_{CC} 電源で動作
- 最大 500kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- 小さいスタンバイ電流: 1μA (標準値)
- 外付けコンデンサ: 4 × 0.1μF
- 3.3V 電源で 5V ロジック入力を許容
- SNx5C3223E 代替の高速ピン互換デバイス (1Mbit/s)

2 アプリケーション

- バッテリー駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

DB, DW, OR PW PACKAGE
(TOP VIEW)



3 概要

MAX3223E は 2 つのラインドライバ、2 つのラインレシーバ、1 つのデュアルチャージポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート・コネクタの間の電気的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。このデバイスは最大 500kbit/s のデータ信号速度、最大 30V/μs のドライバ出力スルーレイトで動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ FORCEOFF が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、有効な RS-232 信号を検出しない場合、ドライバ出力はディセーブルになります。FORCEOFF を LOW に設定しかつ EN を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1mA に減少します。シリアルポートを切り離れた場合、またはペリフェラルドライバをオフにした場合、自動パワー・ダウンが作動します。FORCEON と FORCEOFF を HIGH にすると、自動パワー・ダウンを無効にできます。自動パワー・ダウンが有効な場合、いずれかのレシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。INVALID 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知する目的で使用されます。INVALID は、いずれかのレシーバの入力電圧が 2.7V を上回っている場合、-2.7V を下回っている場合、-0.3V と 0.3V の間にあった期間が 30μs 未満である場合のいずれかの場合、HIGH (有効データ) になります。INVALID は、レシーバの入力電圧が 30μs を超える期間 -0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 5-4 を参照してください。

パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
MAX3223E	SOIC (DW, 20)	12.8mm × 10.3mm
	SSOP (DB, 20)	7.2mm × 7.8mm
	TSSOP (PW, 20)	6.5 mm × 6.4 mm

- 詳細については、セクション 10 を参照してください。
- パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V
V+ - V-	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)		V
		Receiver		
V _O	Output voltage range	Driver		V
		Receiver (INVALID)		
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

4.2 Recommended Operating Conditions

See [7-1](#), and ⁽¹⁾

		MIN	NOM	MAX	UNIT	
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, EN, FORCEOFF, FORCEON		V _{CC} = 3.3 V	2	V
				V _{CC} = 5 V	2.4	
V _{IL}	Driver and control low-level input voltage	DIN, EN, FORCEOFF, FORCEON			0.8	V
V _I	Driver and control input voltage	DIN, EN, FORCEOFF, FORCEON		0	5.5	V
	Receiver input voltage			-25	25	V
T _A	Operating free-air temperature	MAX3223EC		0	70	°C
		MAX3223EI		-40	85	

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

4.3 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000
			±15000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.4 ESD Ratings - IEC Specifications

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge ⁽¹⁾	±8000
		IEC 61000-4-2 Air-gap Discharge ⁽¹⁾	±15,000

(1) A minimum of 1-μF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

4.5 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SOIC)	DW (SOIC)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	87.2	76.8	89.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	41.1	39.6	29.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.3	41.5	41.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.2	12.6	1.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.7	40.9	41.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#)) and ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
I _I	Input leakage current	EN, FORCEOFF, FORCEON		±0.01	±1	μA	
I _{CC}	Supply current	Auto-powerdown disabled	V _{CC} = 3.3 V or 5 V, T _A = 25°C, No load, FORCEOFF and FORCEON at V _{CC}		0.3	1.3	mA
		Powered off	No load, FORCEOFF at GND		1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

4.7 Driver Section

4.7.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#)) and ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	DOOUT at R _L = 3 kΩ to GND	–5	–5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V				
r _o	Output resistance	V _{CC} , V+, and V– = 0 V, V _O = ±2 V	300	10M		Ω
I _{OZ}	Output leakage current	FORCEOFF = GND, V _{CC} = 3 V to 3.6 V, V _O = ±12 V			±25	μA
		FORCEOFF = GND, V _{CC} = 4.5 V to 5.5 V, V _O = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

4.7.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#)) and ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	$C_L = 1000 \text{ pF}$, One DOUT switching,	$R_L = 3 \text{ k}\Omega$, See 5-1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew ⁽³⁾	$C_L = 150 \text{ pF}$ to 2500 pF , See 5-2	$R_L = 3 \text{ k}\Omega$ to $7 \text{ k}\Omega$,		100		ns
SR(tr)	Slew rate, transition region (See 5-1)	$R_L = 3 \text{ k}\Omega$ to $7 \text{ k}\Omega$, $V_{CC} = 3.3 \text{ V}$	$C_L = 150 \text{ pF}$ to 1000 pF	6		30	V/ μs
			$C_L = 150 \text{ pF}$ to 2500 pF	4		30	

(1) Test conditions are C_1 – $C_4 = 0.1 \text{ }\mu\text{F}$ at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C_1 = 0.047 \text{ }\mu\text{F}$, C_2 – $C_4 = 0.33 \text{ }\mu\text{F}$ at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

(2) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

4.7.3 ESD Protection

		TYP	UNIT
Driver outputs (DOUTx)	Human-Body Model (HBM)	± 15	kV
	IEC61000-4-2, Air-Gap Discharge	± 15	
	IEC61000-4-2, Contact Discharge	± 8	

4.8 Receiver Section

4.8.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [7-1](#)) and ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$		$V_{CC} - 0.6$	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.6 \text{ mA}$				0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3 \text{ V}$			1.6	2.4	V
		$V_{CC} = 5 \text{ V}$			1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3 \text{ V}$		0.6	1.1		V
		$V_{CC} = 5 \text{ V}$		0.6	1.4		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)				0.5		V
I_{OZ}	Output leakage current	$\overline{EN} = V_{CC}$			± 0.05		μA
r_i	Input resistance	$V_I = \pm 3 \text{ V}$ to $\pm 25 \text{ V}$		3	5		k Ω

(1) Test conditions are C_1 – $C_4 = 0.1 \text{ }\mu\text{F}$ at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C_1 = 0.047 \text{ }\mu\text{F}$, C_2 – $C_4 = 0.33 \text{ }\mu\text{F}$ at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

(2) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

4.8.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		TYP ⁽²⁾	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150 \text{ pF}$, See 5-3		150	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 150 \text{ pF}$, See 5-3		150	ns
t_{en}	Output enable time	$C_L = 150 \text{ pF}$, $R_L = 3 \text{ k}\Omega$, See 5-4		200	ns
t_{dis}	Output disable time	$C_L = 150 \text{ pF}$, $R_L = 3 \text{ k}\Omega$, See 5-4		200	ns
$t_{sk(p)}$	Pulse skew ⁽³⁾	See 5-3		50	ns

(1) Test conditions are C_1 – $C_4 = 0.1 \text{ }\mu\text{F}$ at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $C_1 = 0.047 \text{ }\mu\text{F}$, C_2 – $C_4 = 0.33 \text{ }\mu\text{F}$ at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

(2) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

4.8.3 ESD Protection

		TYP	UNIT
Receiver inputs (RINx)	Human-Body Model (HBM)	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

4.9 Auto-Powerdown Section

4.9.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#))

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{T+} (valid)	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}		2.7	V
V_{T} (valid)	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}	-2.7		V
V_{T} (invalid)	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND,	FORCEOFF = V_{CC}	-0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = 1\text{ mA}$, FORCEOFF = V_{CC}	FORCEON = GND,	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6\text{ mA}$, FORCEOFF = V_{CC}	FORCEON = GND,		0.4	V

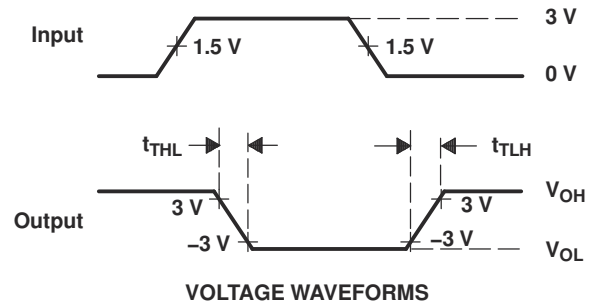
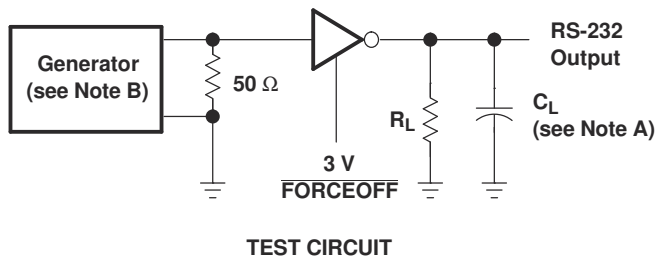
4.9.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
t_{invalid}	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

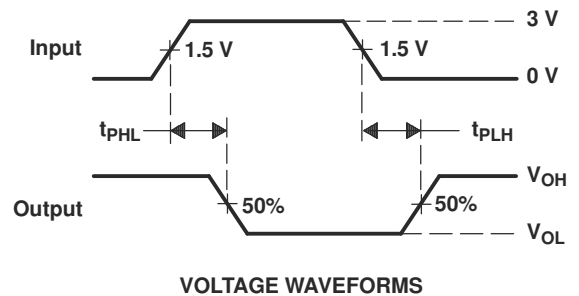
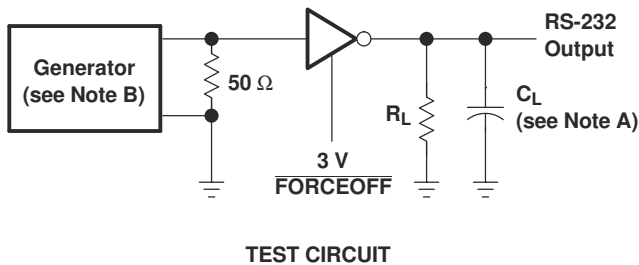
5 Parameter Measurement Information



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

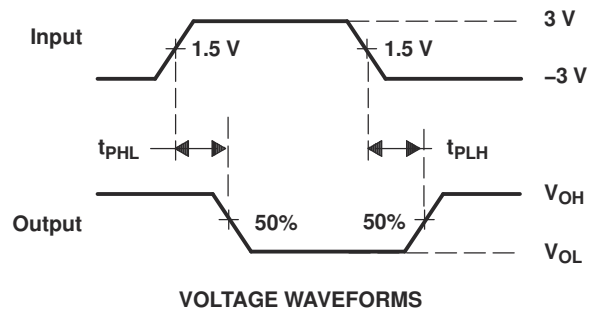
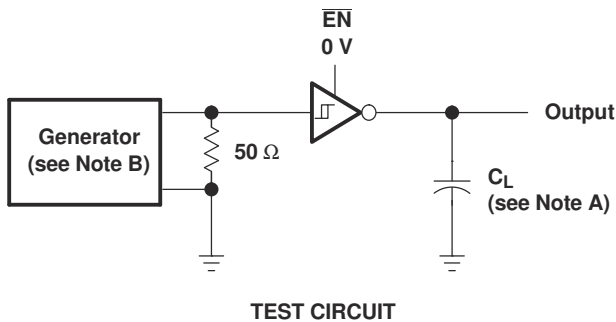
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

5-1. Driver Slew Rate



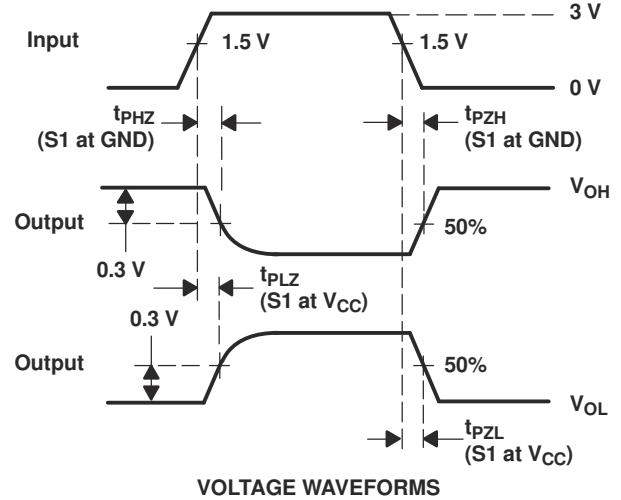
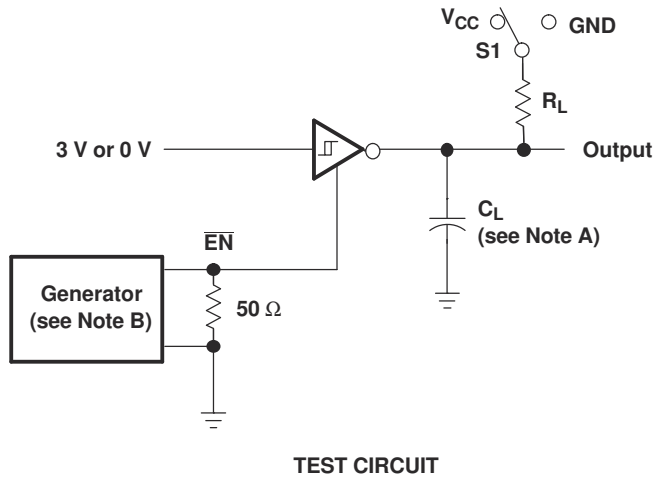
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

5-2. Driver Pulse Skew



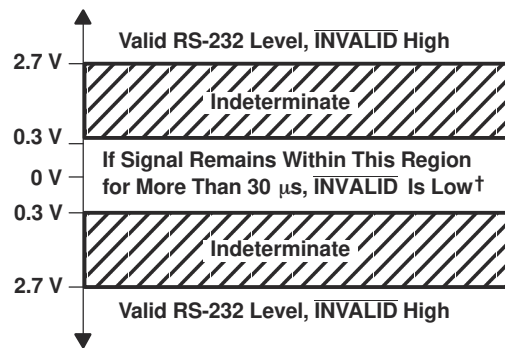
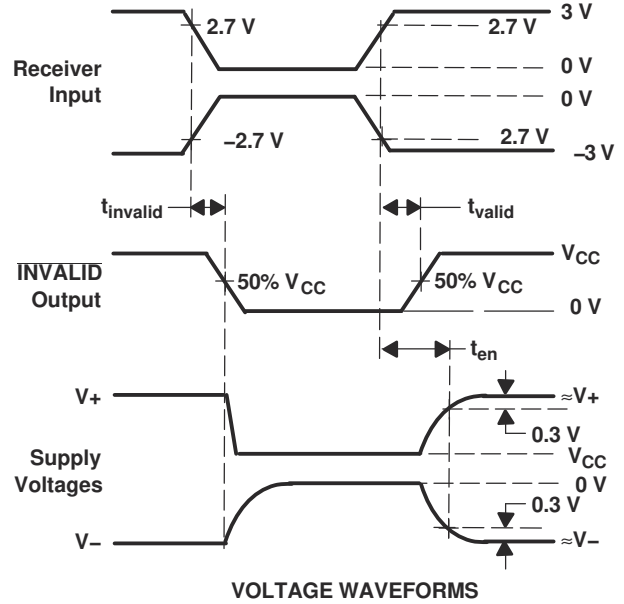
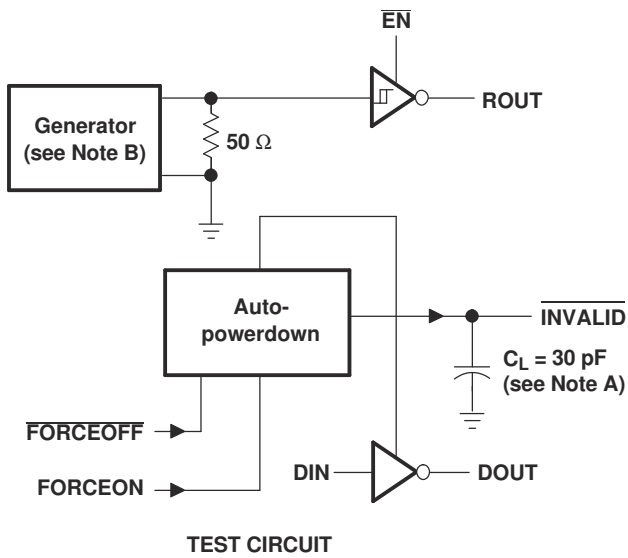
- A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

5-3. Receiver Propagation Delay Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.

5-4. Receiver Enable and Disable Times



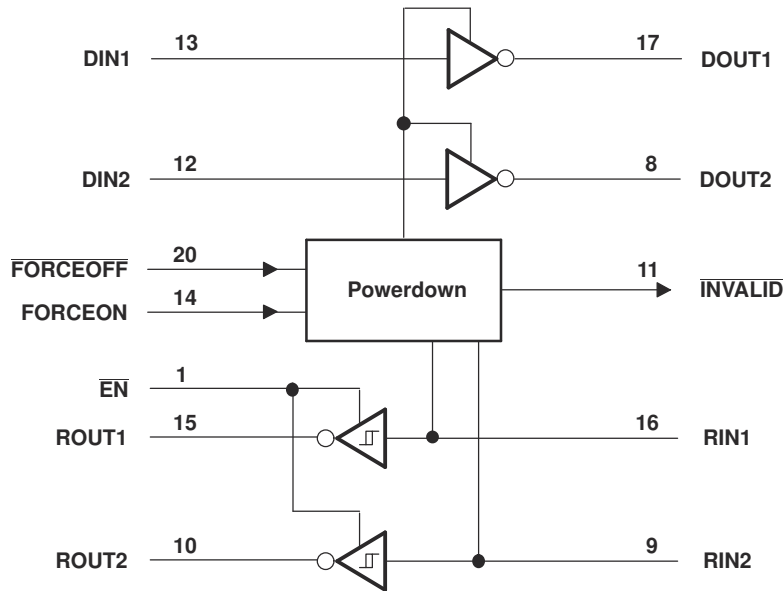
† Auto-powerdown disables drivers and reduces supply current to 1 μ A

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

5-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

6 Detailed Description

6.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

 **6-1. Logic diagram (positive logic)**

6.2 Device Functional Modes

Function Table (Each Driver)

INPUTS ⁽¹⁾				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Function Table (Each Receiver)

INPUTS ⁽¹⁾			OUTPUT DOUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

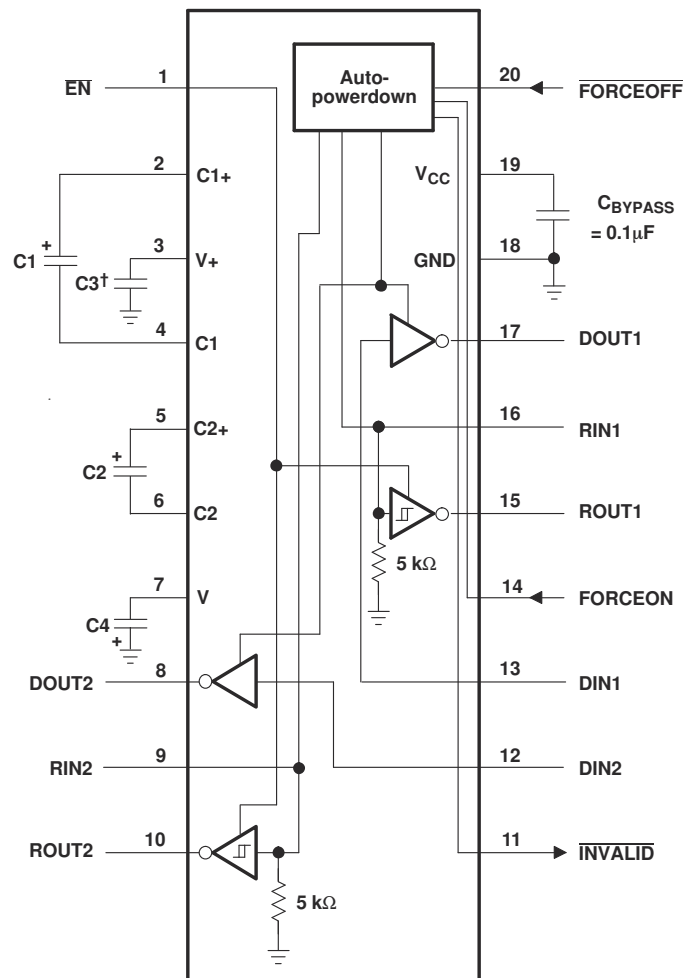
(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

7 Application and Implementation

注

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7.1 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

図 7-1. Typical Operating Circuit and Capacitor Values

7.1.1 Detailed Design Procedure

MAX3223E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors

(1)

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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8.3 Trademarks

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8.4 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2009) to Revision B (December 2023)	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1
Added the <i>ESD Ratings</i> tables.....	3
Added the <i>Thermal Information</i> table.....	4
Changed the I _{CC} Auto-powerdown disabled max value from 1 mA to 1.3 mA in the <i>Electrical Characteristics</i>	4

Changes from Revision * (January 2006) to Revision A (September 2009)	Page
RHL のピン配置図を削除.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3223ECDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223EC	Samples
MAX3223ECDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223EC	Samples
MAX3223EIDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	Samples
MAX3223EIDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223EI	Samples
MAX3223EIDWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223EI	Samples
MAX3223EIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3223ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3223ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223EIDBR	SSOP	DB	20	2000	356.0	356.0	35.0
MAX3223EIDBR	SSOP	DB	20	2000	353.0	353.0	32.0
MAX3223EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223EIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX3223ECDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223EIDW	DW	SOIC	20	25	507	12.83	5080	6.6

PW0020A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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