OPAx317-Q1ゼロドリフト、低オフセット、レール・ツー・レールI/O オペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容で　AEC-Q100　認定済み：
  - デバイス温度グレード1: 動作時周囲温度範囲 –40°C～+125°C
  - デバイスHBM ESD分類レベル3A
  - デバイスCDM ESD分類レベルC6
- 電源電圧: 1.8V～5.5V
- microPackage:
  - シングル: SOT23-5
  - デュアル: VSSOP-8
  - クワッド: TSSOP-14
- 低いオフセット電圧: 20µV (標準値)
- CMRR: 108dB (標準値) PSRR
- 静止電流: 35µA (最大値)
- ゲイン帯域幅: 300kHz
- レール・ツー・レール入出力
- 内部的なEMIおよびRFIフィルタリング

2 アプリケーション

- HEV-EVパワートレイン
- 先進運転支援システム(ADAS)
- 自動環境制御
- 低ノイズ、低消費電力の回路
- 航空電子工学、着陸装置
- 医療用計測装置
- 電流感知

3 概要

OPA317-Q1シリーズのCMOSオペアンプは、求めやすい価格でありながら高精度の性能を実現します。これらのデバイスは、ゼロドリフト・ファミリのアンプのメンバーで、専用の自動較正技術を使用して、低いオフセット電圧(最大90µV)、時間と温度に対してゼロに近いドリフト、わずか35µA (最大値)の静止電流を同時に実現しています。

OPA317-Q1ファミリは、レール・ツー・レールの入出力に加えて、フラットに近い1/fノイズが特長で、多くのアプリケーションに理想的なアンプであり、システムの設計に簡単に組み込めます。これらのデバイスは、最小1.8V (±0.9V)、最大5.5V (±2.75V)の低電圧での動作に最適化されています。

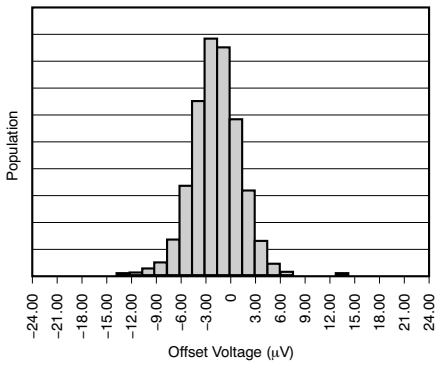
OPA317-Q1 (シングル・バージョン)はSOT23-5パッケージで利用可能です。OPA2317-Q1 (デュアル・バージョン)はVSSOP-8パッケージで利用可能です。OPA4317-Q1はTSSOP-14パッケージで利用可能です。どのバージョンも、-40℃～+125℃での動作が保証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA317-Q1	SOT-23 (5)	1.60mm×2.90mm
OPA2317-Q1	VSSOP (8)	3.00mm×3.00mm
OPA4317-Q1	TSSOP (14)	4.40mm×5.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

オフセット電圧の分布



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4 改訂履歴

日付	改訂内容	注
2016年7月	*	初版

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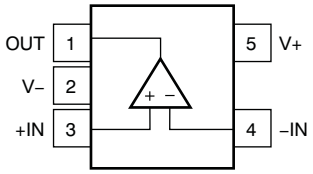
5 Pin Configuration and Functions

OPA317-Q1: DBV Package
5-Pin SOT-23
Top View



Pin Functions: OPA317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	SOT-23		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

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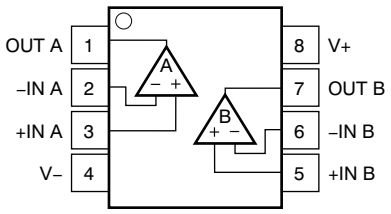
OPA2317-Q1: DGK Package
8-Pin VSSOP
Top View



Pin Functions: OPA2317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	VSSOP		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

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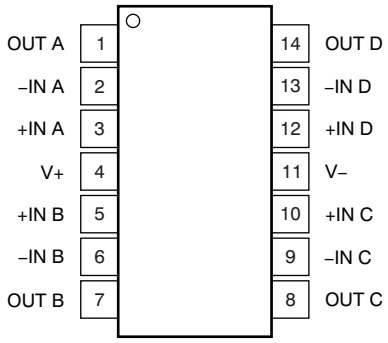
OPA4317-Q1: SW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4317-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
	TSSOP		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
+IN C	10	I	Noninverting input, channel C
–IN C	9	I	Inverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
V_S = (V+) – (V–)	Supply voltage		7	V
	Signal input terminals (2)	(V–) – 0.3	(V+) + 0.3	V
	Signal input terminals(2)	–10	10	mA
	Output short circuit(3)	Continuous		
T_A	Operating temperature	–40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±4000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
(V+ – V–)	Supply voltage	1.8 (±0.9)	5.5 (±2.25)	V
T_A	Specified temperature	–40	125	°C

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6.4 Thermal Information: OPA317-Q1

THERMAL METRIC(1)		OPA317-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2317-Q1

THERMAL METRIC(1)		OPA2317-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4317-Q1

THERMAL METRIC(1)		OPA4317-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics: V_S = 1.8 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		20	±90	µV
		T_A = –40°C to +125°C, V_S = 5 V			±100	
dV_{OS}/dT	Input offset voltage vs temperature	T_A = –40°C to +125°C		0.05		µV/°C
PSRR	Input offset voltage vs power supply	T_A = –40°C to +125°C, V_S = 1.8 V to 5.5 V		1	10	µV/V
	Long-term stability(1)			See (1)		
	Channel separation, DC			5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±275		pA
		OPA4317-Q1		±155		
		T_A = –40°C to +125°C		±300		
I_{OS}	Input offset current			±400		pA
		OPA4317-Q1		±140		
NOISE						
e_n	Input voltage noise density	f = 1 kHz		55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz		1.1		
i_n	Input current noise	f = 10 Hz		100		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	95	108		dB
		OPA4317 T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	95	108		
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, R_L = 10 kΩ (V–) + 100 mV < V_O < (V+) – 100 mV	100	110		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		300		kHz
SR	Slew rate	G = 1		0.15		V/µs
OUTPUT						
	Voltage output swing from rail	T_A = –40°C to +125°C		30	100	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive		See the *Typical Characteristics* section			
	Open-loop output impedance	f = 350 kHz, I_O = 0		2		kΩ
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
I_Q	Quiescent current per amplifier	T_A = –40°C to +125°C, I_O = 0		21	35	µA
	Turnon time	V_S = 5 V		100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

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6.8 Typical Characteristics

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

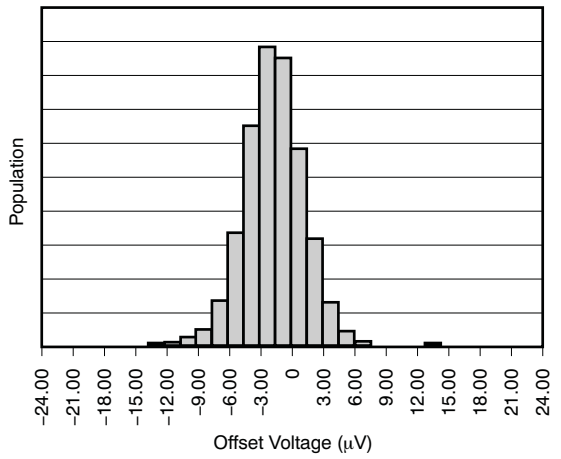

Figure 1. Offset Voltage Production Distribution

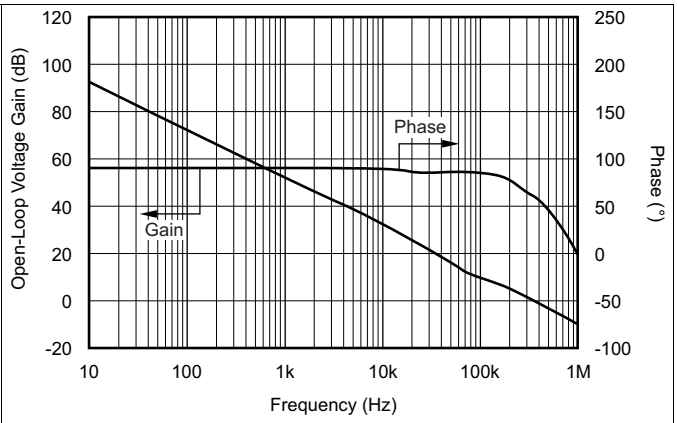

Figure 2. Open-Loop Gain vs Frequency

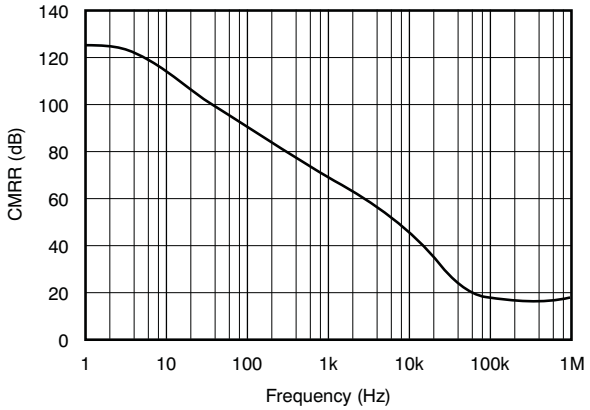

Figure 3. Common-Mode Rejection Ratio vs Frequency

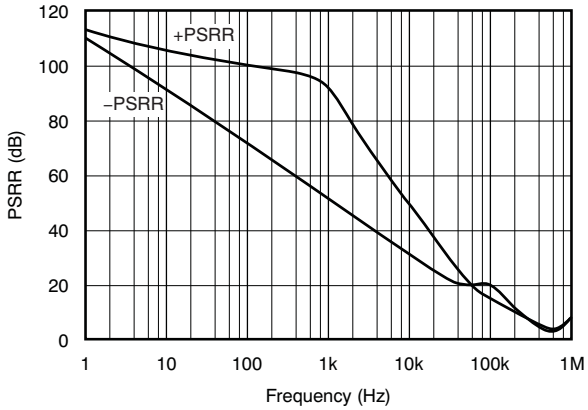

Figure 4. Power-Supply Rejection Ratio vs Frequency

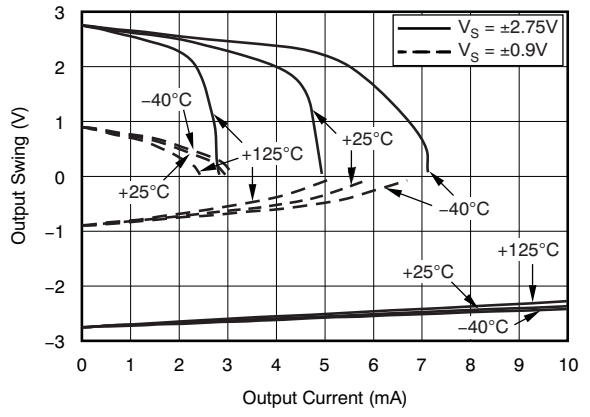

Figure 5. Output Voltage Swing vs Output Current

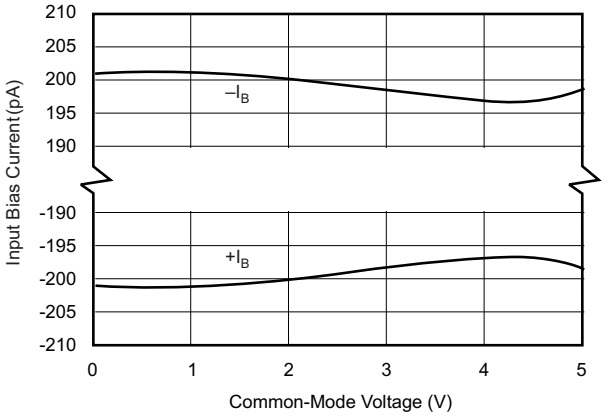

Figure 6. Input Bias Current vs Common-Mode Voltage

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Typical Characteristics (continued)

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

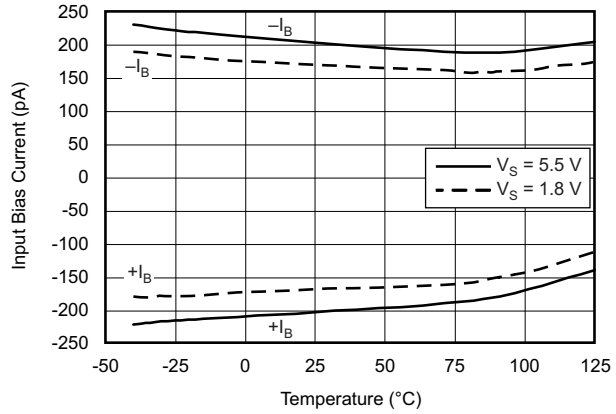


Figure 7. Input Bias Current vs Temperature

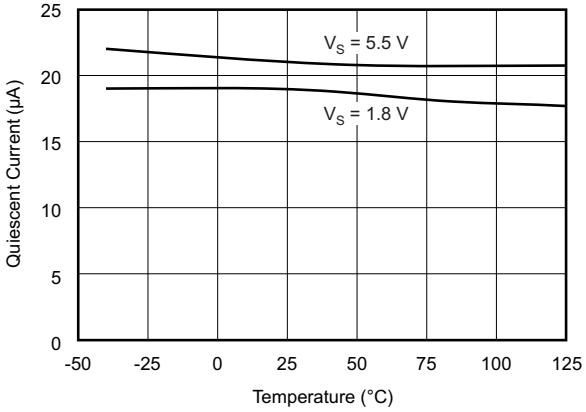
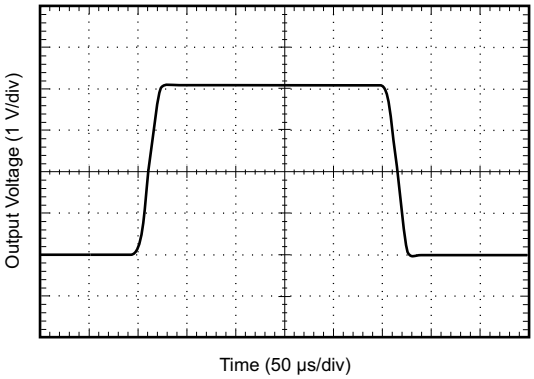
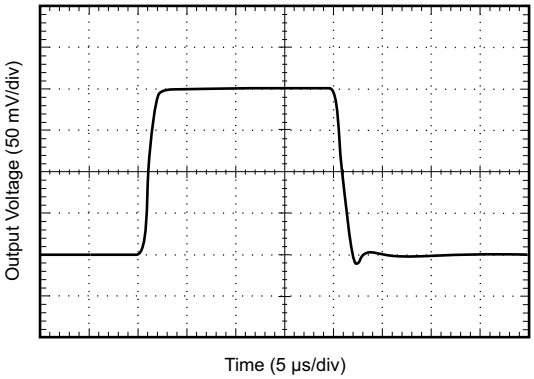


Figure 8. Quiescent Current vs Temperature



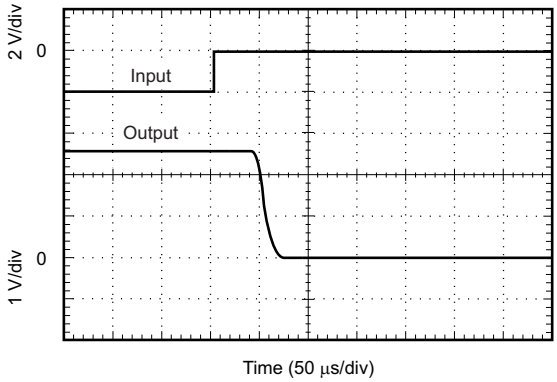
G = 1 R_L = 10 kΩ

Figure 9. Large-Signal Step Response



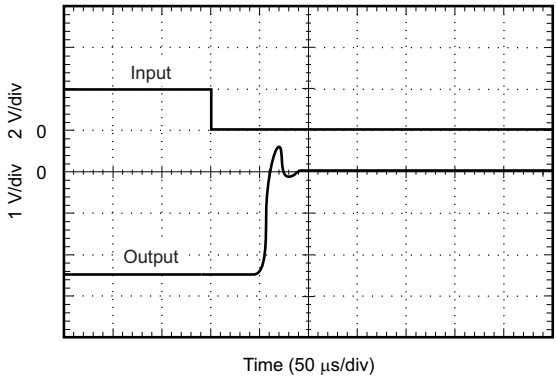
G = 1 R_L = 10 kΩ

Figure 10. Small-Signal Step Response



See Figure 18

Figure 11. Positive Overvoltage Recovery



See Figure 18

Figure 12. Negative Overvoltage Recovery

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Typical Characteristics (continued)

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

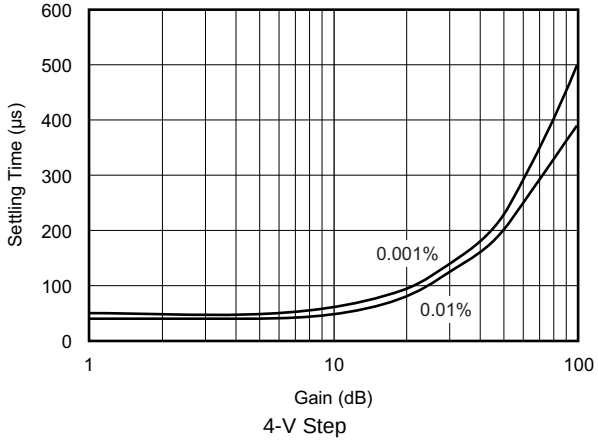


Figure 13. Settling Time vs Closed-Loop Gain

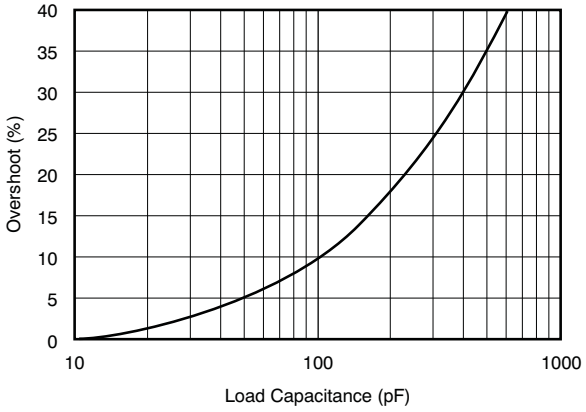


Figure 14. Small-Signal Overshoot vs Load Capacitance

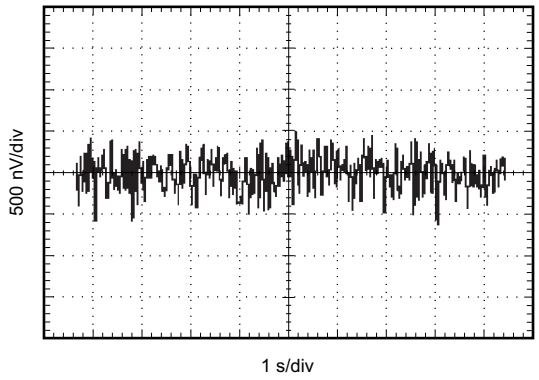


Figure 15. 0.1-Hz to 10-Hz Noise

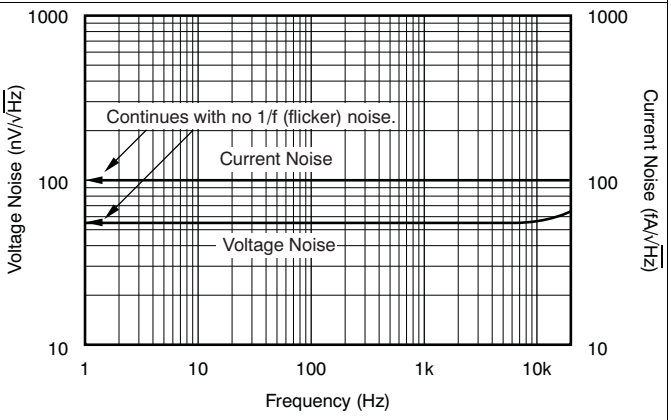
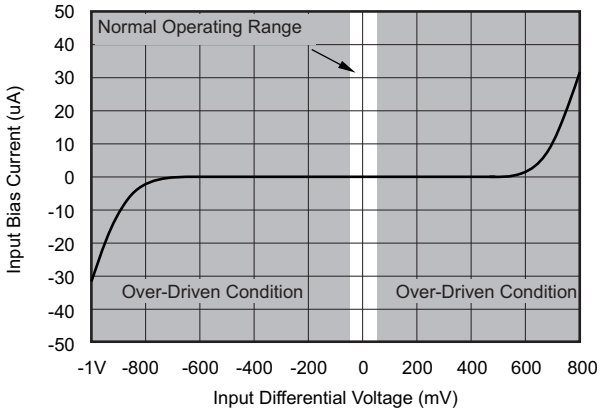


Figure 16. Current and Voltage Noise Spectral Density vs Frequency



See the *Input Differential Voltage* section

Figure 17. Input Bias Current vs Input Differential Voltage

7 Parameter Measurement Information

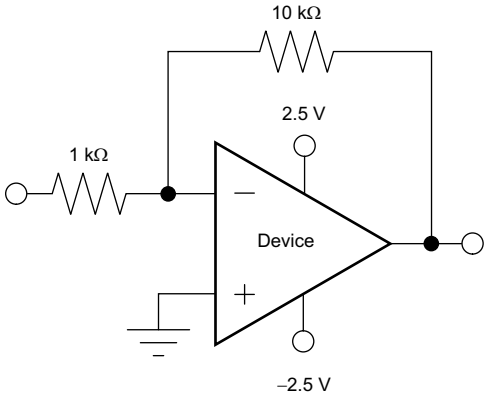


Figure 18. Overvoltage Recovery Circuit

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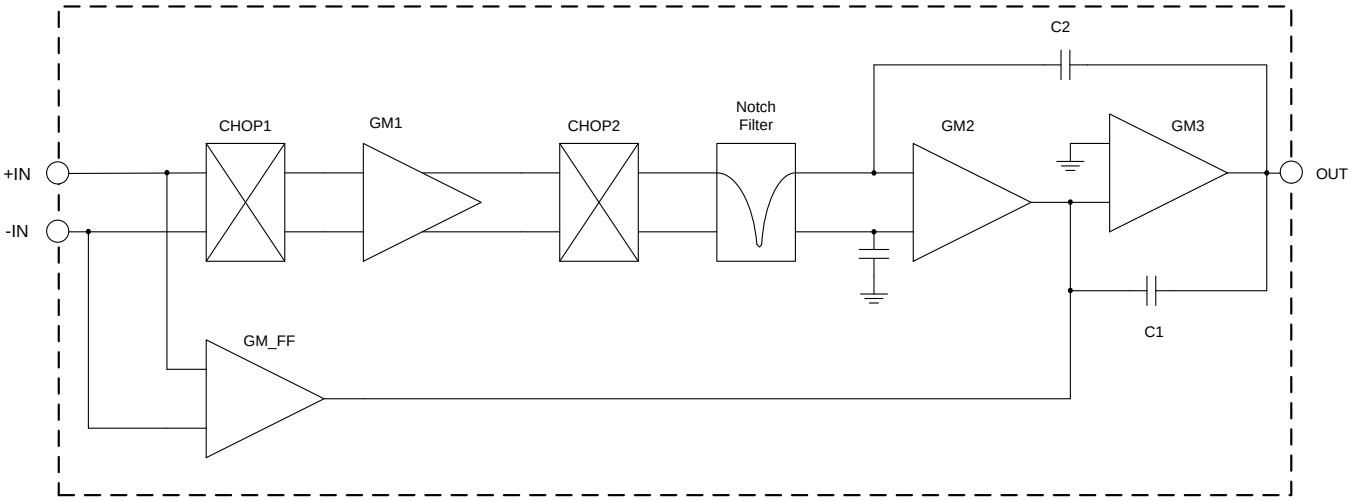
8 Detailed Description

8.1 Overview

The OPA317-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the OPA317 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The OPA317-Q1 series of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 1.8 V (±0.9 V) up to 5.5 V (±2.75 V).

CAUTION

Supply voltages greater than 7 V can permanently damage the device.

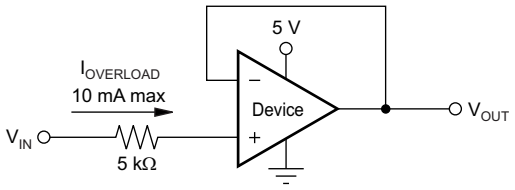
See the *Absolute Maximum Ratings* table. Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section.

Feature Description (continued)

8.3.2 Input Voltage

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA317-Q1 device is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is about 200 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 19.



NOTE: Current limiting resistor required if input voltage exceeds supply rails by ≥ 0.3 V.

Figure 19. Input Current Protection

8.3.3 Input Differential Voltage

The typical input bias current of the OPA317-Q1 during normal operation is approximately 200 pA. In overdriven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied, and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 20.

NOTE

The input bias current remains within specification within the linear region.

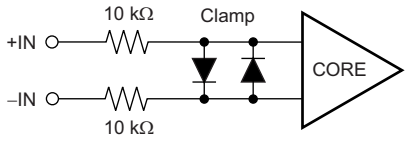


Figure 20. Equivalent Input Circuit

8.3.4 Internal Offset Correction

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 operational amplifiers use an auto-calibration technique with a time-continuous, 125-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA317-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a roll-off of 20 dB per decade.

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8.4 Device Functional Modes

The OPAx317-Q1 family of devices are powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. Proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA317-Q1 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high impedance inputs that have a common-mode range 100 mV beyond the supplies, and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The OPA317-Q1 series are precision amplifiers for cost-sensitive applications.

9.1.1 Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative power supply than the operational amplifier negative supply. A pulldown resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 21.

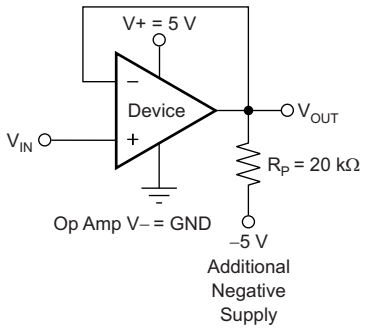

Figure 21. For V_{OUT} Range to Ground

The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA317-Q1, OPA2317-Q1, and OPA4317-Q1 have been characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. This configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns as the output drives back up above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Use resistances as low as 10 kΩ to achieve excellent accuracy down to –10 mV.

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9.2 Typical Applications

The circuit shown in Figure 22 is a high-side voltage-to-current (V-I) converter. It translates an input voltage of 0 V to 2 V to an output current of 0 mA to 100 mA. Figure 23 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA317 facilitate excellent DC accuracy for the circuit.

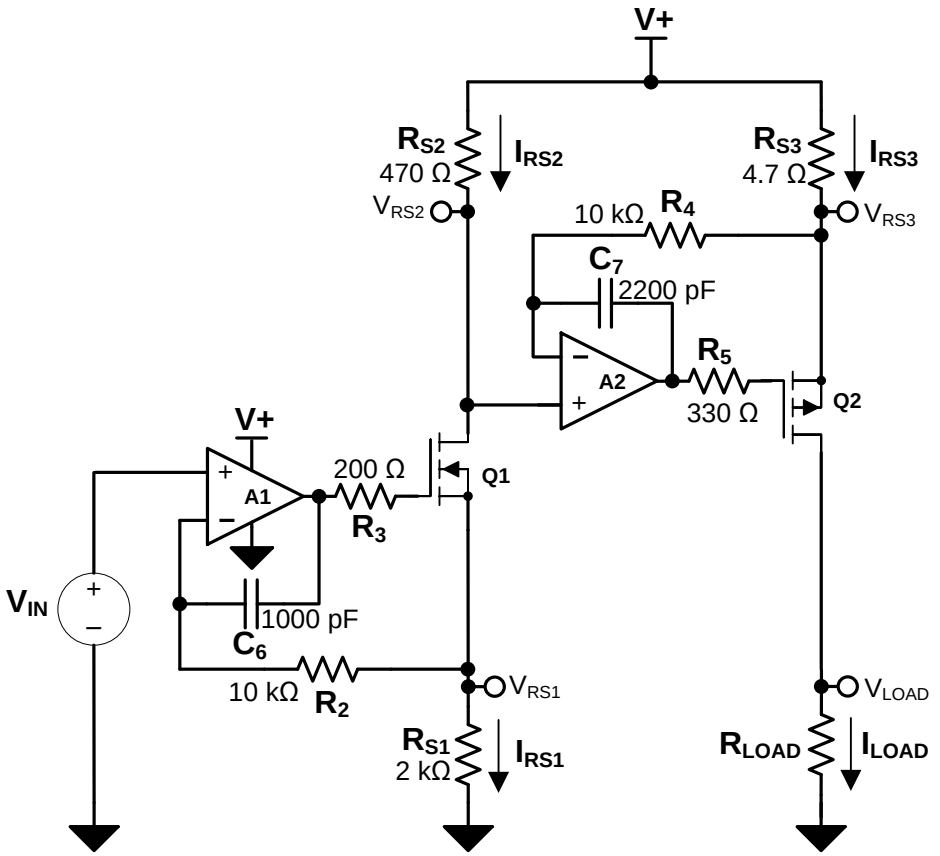

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Figure 22. High-Side Voltage-to-Current (V-I) Converter

9.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5-V DC
- Input: 0-V to 2-V DC
- Output: 0-mA to 100-mA DC

9.2.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current-sensing resistors: R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

Typical Applications (continued)

For a successful design, pay close attention to the DC characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2317 CMOS operational amplifier is a high-precision, 5-μV offset, 0.05-μV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 50 mV of the positive rail. The OPA2317 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise DC control. The rail-to-rail output stage of the OPA2317 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

9.2.3 Application Curve

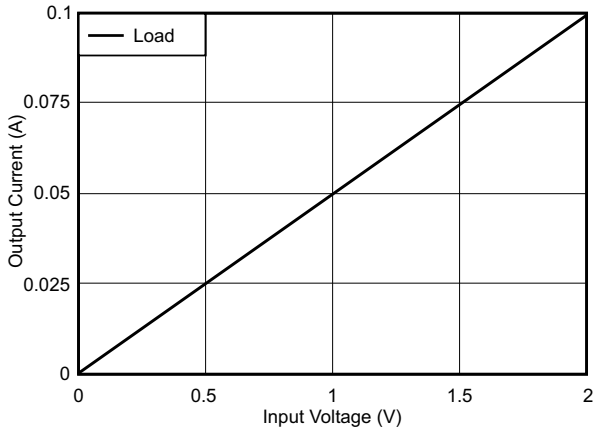

Figure 23. Measured Transfer Function for High-Side V-I Converter

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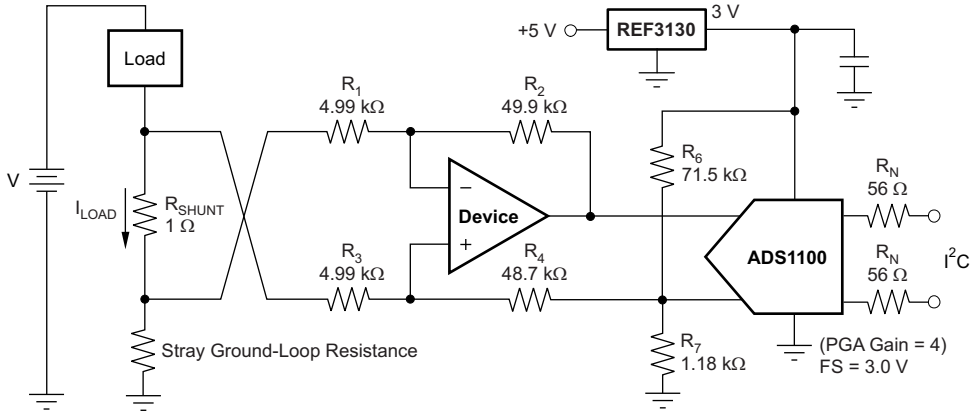
9.3 System Example

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 device is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 device may be omitted.



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NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 24. Low-Side Current Monitor

10 Power Supply Recommendations

The OPAx317-Q1 device is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Electrical Characteristics: V_S = 1.8 V to 5.5 V* table presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings*) table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Optimize circuit layout and mechanical conditions for lowest offset voltage and precision performance. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 μV/°C or higher, depending on the materials used.

11.2 Layout Example

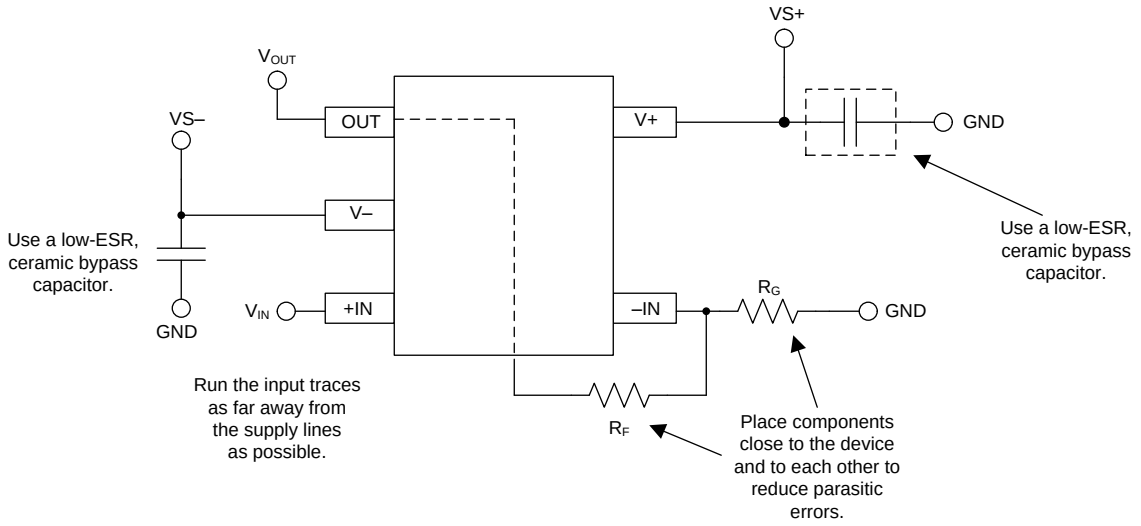

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Figure 25. OPAx317-Q1 Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください：

- 『セルフ・キャリブレーション、16 ビットA/Dコンバータ』、
- 『最大15ppm/℃、100μA、SOT23-3シリーズ 基準電圧』、

12.2 ドキュメントの更新通知を受け取る方法

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12.3 関連リンク

次に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA317-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2317-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4317-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2317QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2317
OPA2317QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2317
OPA317QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	317Q
OPA317QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	317Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2317-Q1, OPA317-Q1 :

- Catalog : OPA2317, OPA317

NOTE: Qualified Version Definitions:

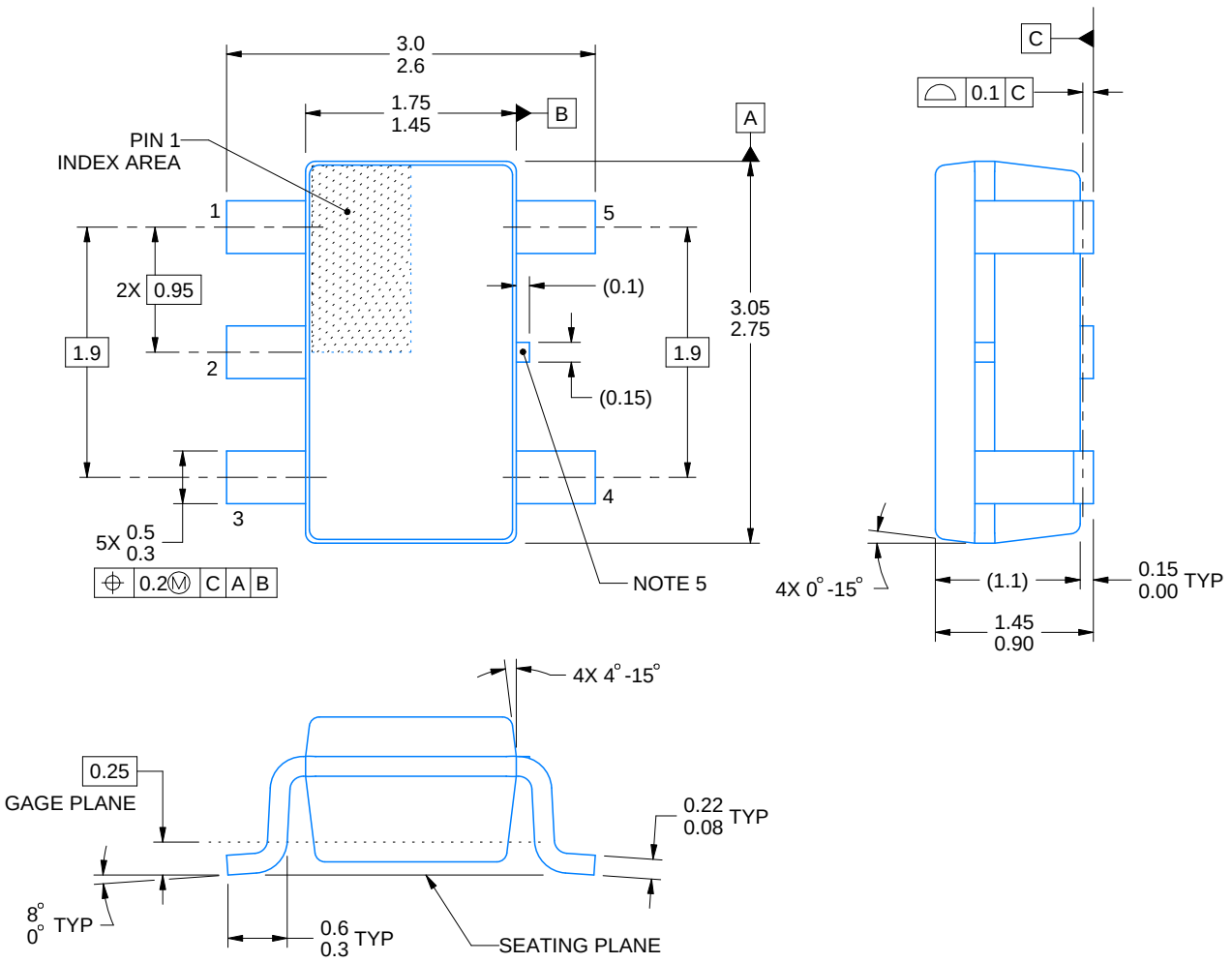
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

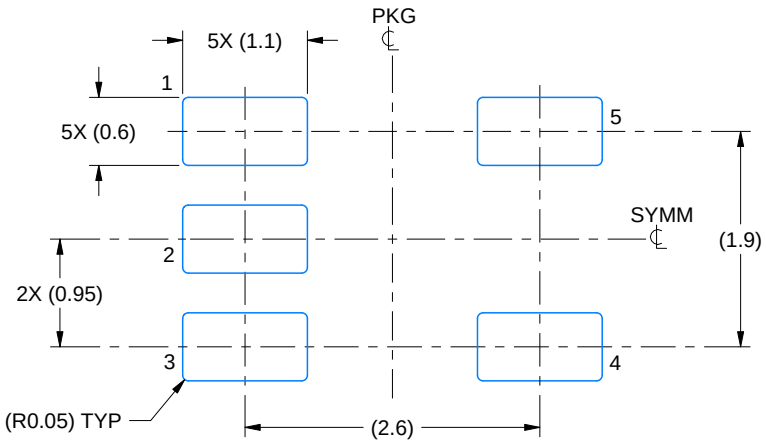
SMALL OUTLINE TRANSISTOR



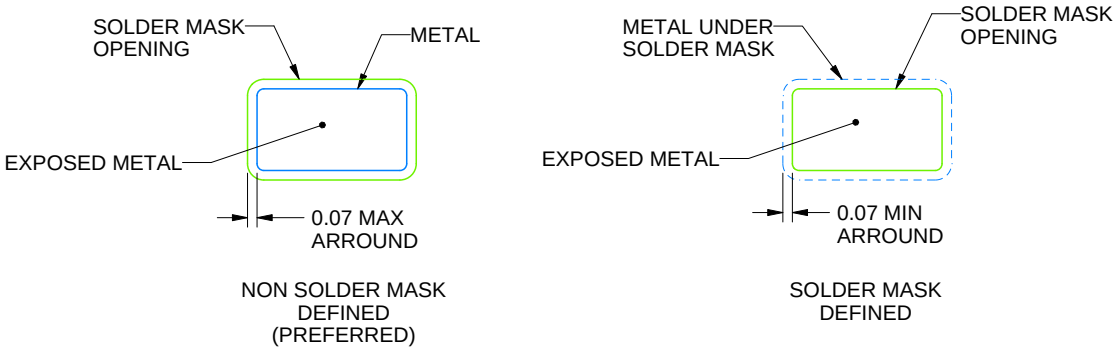
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

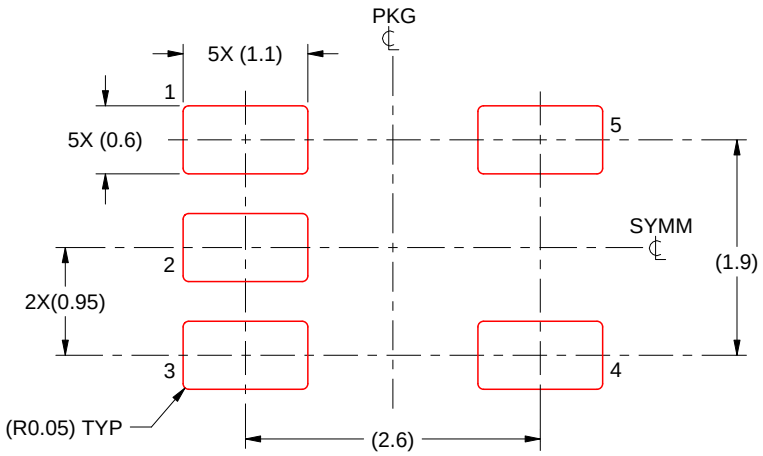


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

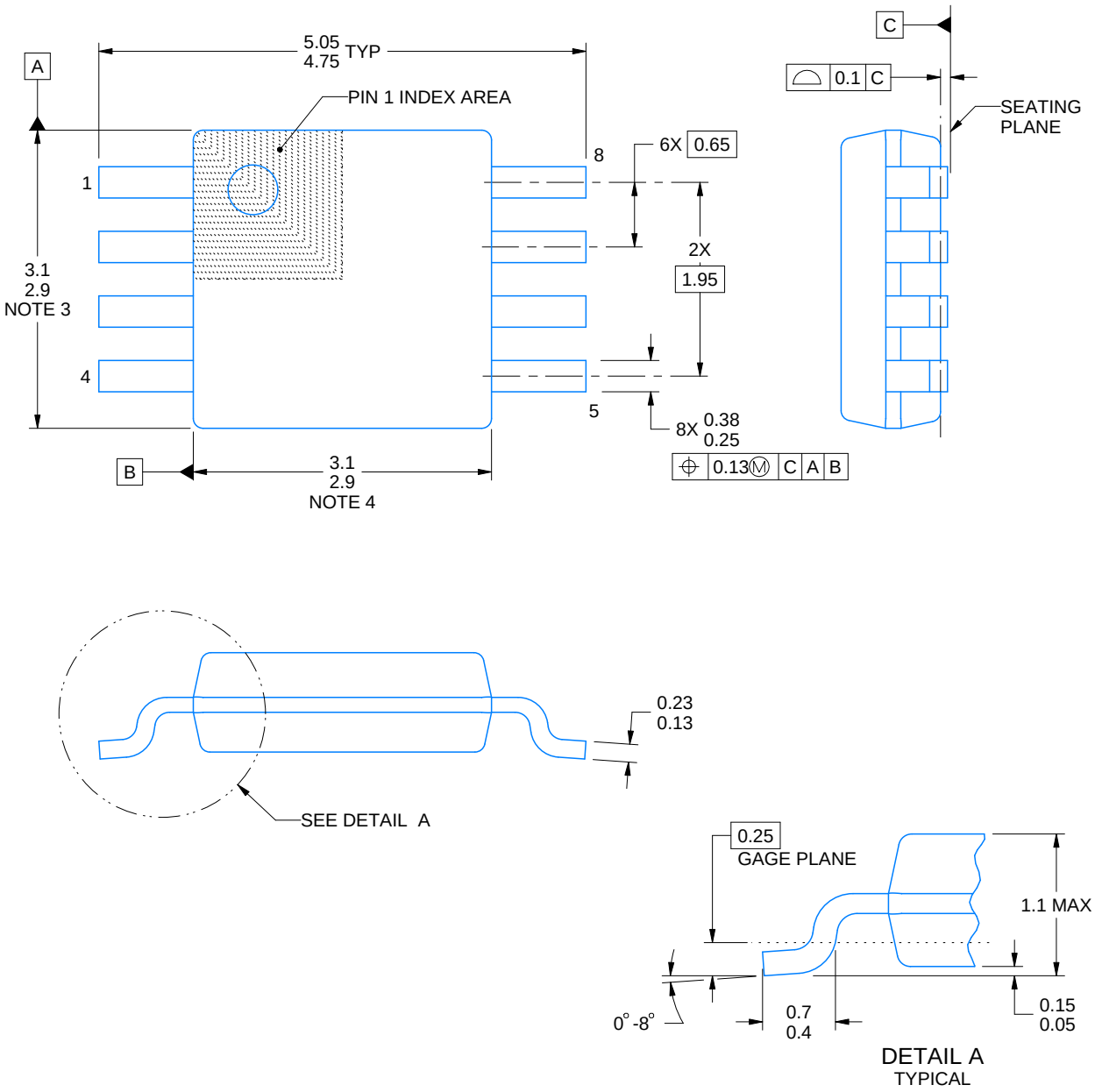
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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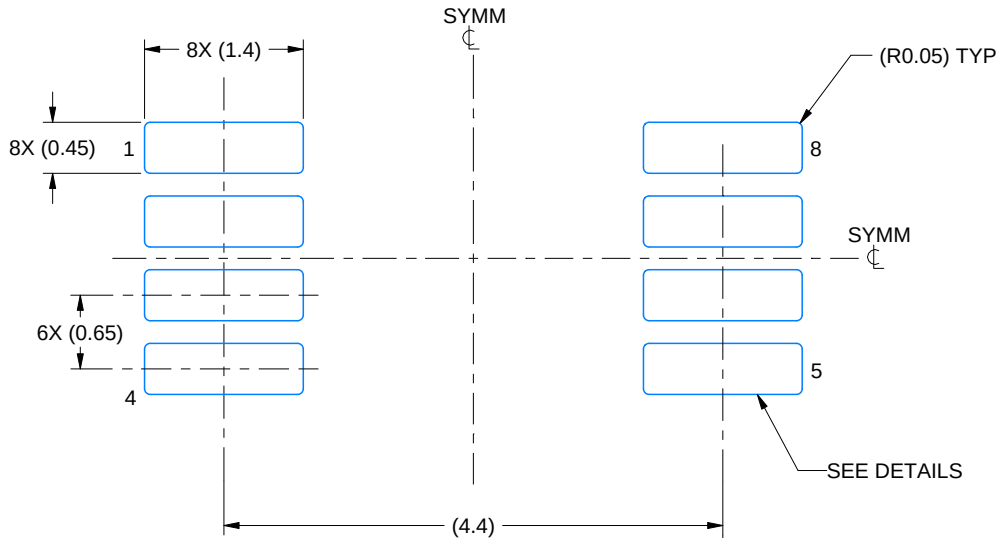
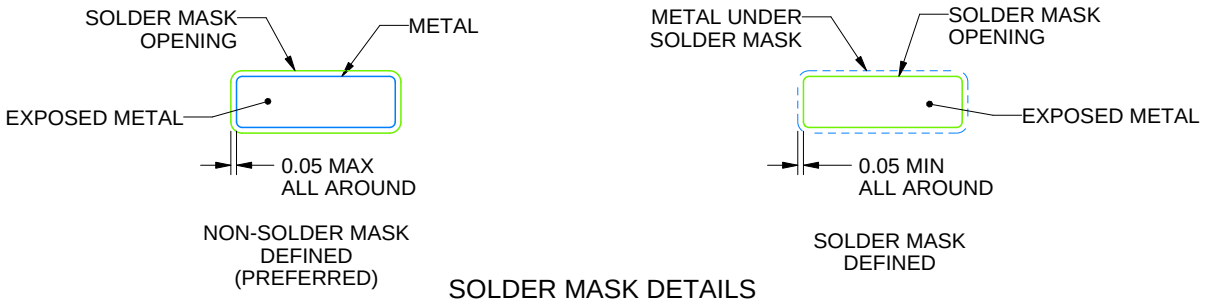
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

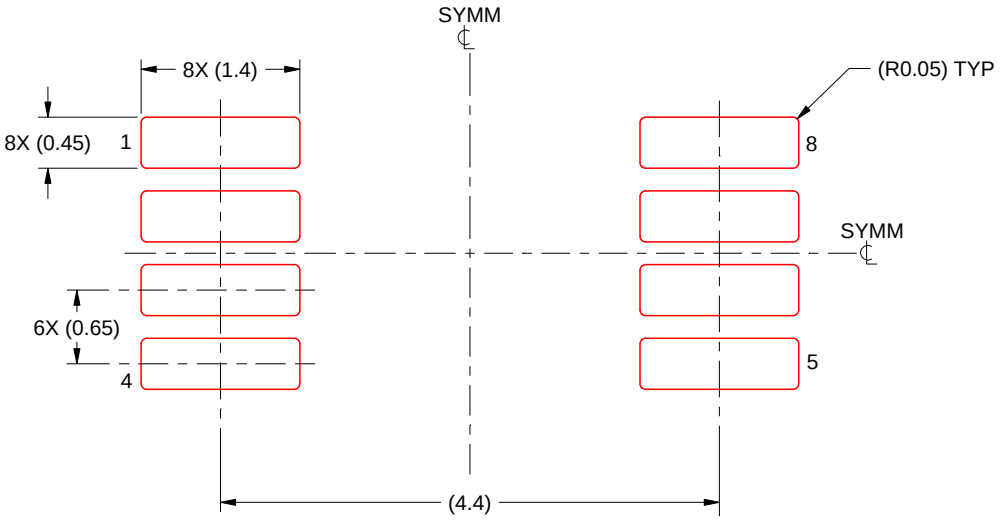


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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