Quad, Low-Power, Single-Supply, Wideband Operational Amplifier

FEATURES

- **HIGH BANDWIDTH:**
  280MHz (G = +1)
  120MHz (G = +2)
- **LOW SUPPLY CURRENT:**
  3.9mA/ch (V_S = +5V)
- **FLEXIBLE SUPPLY RANGE:**
  ±1.4V to ±5.5V Dual Supply
  +2.8V to +11V Single Supply
- **INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY**
- **4.91V OUTPUT SWING ON +5V SUPPLY**
- **HIGH SLEW RATE: 560V/µs**
- **LOW INPUT VOLTAGE NOISE: 9.2nV/√Hz**
- **AVAILABLE IN A TSSOP-14 PACKAGE**

APPLICATIONS

- **SINGLE-SUPPLY ANALOG-TO-DIGITAL CONVERTER (ADC) INPUT BUFFERS**
- **SINGLE-SUPPLY VIDEO LINE DRIVERS**
- **CCD IMAGING CHANNELS**
- **ACTIVE FILTERS**
- **PLL INTEGRATORS**
- **PORTABLE CONSUMER ELECTRONICS**

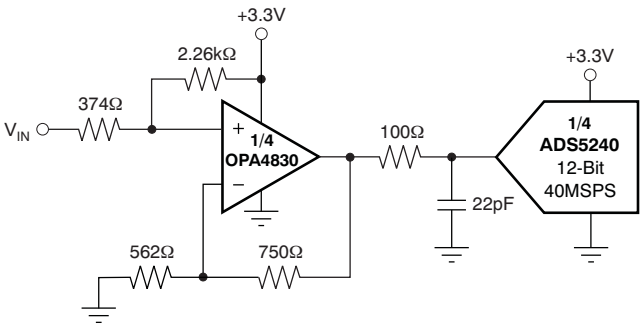


Figure 1. DC-Coupled, +3.3V ADC Driver

DESCRIPTION

The OPA4830 is a quad, low-power, single-supply, wideband, voltage-feedback amplifier designed to operate on a single +3V or +5V supply. Operation on ±5V or +10V supplies is also supported. The input range extends below the negative supply and to within 1.8V of the positive supply. Using complementary common-emitter outputs provides an output swing to within 220mV of either supply while driving 150Ω. High output drive current (±80mA) and low differential gain and phase errors also make this amplifier an excellent choice for single-supply consumer video products.

Low distortion operation is ensured by the high gain bandwidth product (110MHz) and slew rate (560V/µs), making the OPA4830 an ideal input buffer stage to 3V and 5V CMOS analog-to-digital converters (ADCs). Unlike other low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.2nV/√Hz input voltage noise supports wide dynamic range operation.

The OPA4830 is available in an industry-standard quad pinout TSSOP-14 package.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail	OPA830	OPA2830	—	—
Rail-to-Rail Fixed-Gain	OPA832	OPA2832	OPA3832	—
General-Purpose (1800V/µs slew rate)	OPA690	OPA2690	OPA3690	—
Low-Noise, High DC Precision	OPA820	OPA2822	—	OPA4820

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA4830	TSSOP-14	PW	–40°C to +85°C	OPA4830	OPA4830IPW	Rail, 90
					OPA4830IPWR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

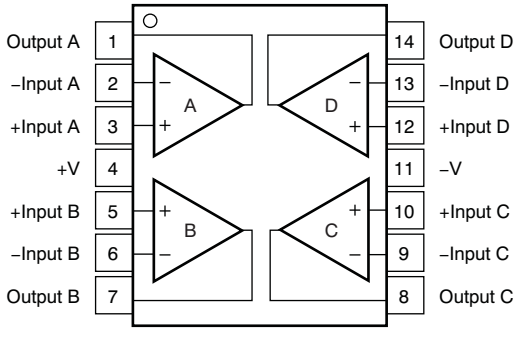
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$12V_{DC}$
Internal Power Dissipation	See Thermal Analysis
Differential Input Voltage	±2.5V
Input Voltage Range (Single Supply)	$–0.5V$ to $+V_S + 0.3V$
Storage Temperature Range: D, PW	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Maximum Junction Temperature (T_J):	
Peak	+150°C
Continuous Operation, Long-Term Reliability	+140°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1500V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress Ratings only, and functional operations of the device at these and any other conditions beyond those specified is not supported.

PIN CONFIGURATION

Top View **TSSOP**



OPA4830

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted.

		OPA4830IPW						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE (see Figure 74)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.2V_{PP}	280				MHz	typ	C
	G = +2, V_O ≤ 0.2V_{PP}	120	66	64	61	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	23	16	14	13	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	11	8	7	6	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	110	80	77	75	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.2V_{PP}	6				dB	typ	C
Slew Rate	G = +2, 2V Step	560	275	265	255	V/µs	min	B
Rise Time	0.5V Step	3.4	5.9	5.95	6.0	ns	max	B
Fall Time	0.5V Step	3.6	6.0	6.05	6.1	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	43	64	66	67	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	–60	–53	–51	–50	dBc	max	B
	R_L ≥ 500Ω	–68	–58	–57	–56	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–59	–50	–49	–48	dBc	max	B
	R_L ≥ 500Ω	–77	–65	–62	–55	dBc	max	B
Input Voltage Noise	f > 1MHz	9.5	10.6	11.1	11.6	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.7	4.8	5.3	5.8	pA/√Hz	max	B
NTSC Differential Gain		0.07				%	typ	C
NTSC Differential Phase		0.17				°	typ	C
DC PERFORMANCE(4)	R_L = 150Ω							
Open-Loop Voltage Gain		74	**66**	65	64	dB	min	A
Input Offset Voltage		±2	**±8**	±9.4	±9.8	mV	max	A
Average Offset Voltage Drift				±30	±30	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±44	±46	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.2	**±1.1**	±1.3	±1.5	µA	max	A
Input Offset Current Drift		—		±5	±5	nA/°C	max	B
INPUT								
Negative Input Voltage(5)		–5.5	**–5.4**	–5.3	–5.2	V	max	A
Positive Input Voltage(5)		3.2	**3.1**	3.0	2.9	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	71	dB	min	A
Input Impedance								
Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Output Voltage Swing	G = +2, R_L = 1kΩ to GND	±4.88	**±4.86**	±4.85	±4.84	V	min	A
	G = +2, R_L = 150Ω to GND	±4.64	**±4.60**	±4.58	±4.56	V	min	A
Current Output, Sinking and Sourcing		±82	**±63**	±58	±53	mA	min	A
Short-Circuit Current	Output Shorted to Ground	±150				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +19°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C.**
At T_A = +25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted.

PARAMETER	CONDITIONS	OPA4830IPW				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)			
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	typ	C
Maximum Operating Voltage			**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	V_S = ±5V, All Channels	17	**19**	21.4	23.8	mA	max	A
Minimum Quiescent Current	V_S = ±5V, All Channels	17	**16**	14.4	13.2	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: IPW		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
PW TSSOP-14		95				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At T_A = +25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/2, unless otherwise noted.

		OPA4830IPW						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE (see Figure 72)								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.2V_{PP}	230				MHz	typ	C
	G = +2, V_O ≤ 0.2V_{PP}	100	70	68	66	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	21	15	14	13	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	10	7	6	5	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	100	75	65	59	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.2V_{PP}	5				dB	typ	C
Slew Rate	G = +2, 2V Step	500	270	260	250	V/µs	min	B
Rise Time	0.5V Step	3.4	5.8	5.9	6.0	ns	max	B
Fall Time	0.5V Step	3.4	5.8	5.9	6.0	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	44	65	67	68	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, f = 5MHz							
2nd-Harmonic	R_L = 150Ω	–56	–50	–49	–48	dBc	max	B
	R_L ≥ 500Ω	–62	–56	–55	–54	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–58	–50	–49	–48	dBc	max	B
	R_L ≥ 500Ω	–84	–65	–62	–60	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2	10.3	10.8	11.3	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.6	5.1	5.6	pA/√Hz	max	B
NTSC Differential Gain		0.08				%	typ	C
NTSC Differential Phase		0.09				°	typ	C
All Hostile Crosstalk, Input-Referred	3 Channels Driven at 5MHz, 1V_{PP}, 4th Channel Measured	–62				dB	typ	C
DC PERFORMANCE[4]	R_L = 150Ω							
Open-Loop Voltage Gain		72	**66**	65	64	dB	min	A
Input Offset Voltage		±0.5	**±6**	±7	±7.5	mV	max	A
Average Offset Voltage Drift				±24	±24	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift				±44	±46	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.2	**±0.9**	±1.1	±1.3	µA	max	A
Input Offset Current Drift				±5	±6	nA/°C	max	B
INPUT								
Least Positive Input Voltage[5]		–0.5	**–0.4**	–0.3	–0.2	V	max	A
Most Positive Input Voltage[5]		3.2	**3.1**	3.0	2.8	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**76**	74	71	dB	min	A
Input Impedance								
Differential-Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	0.09	**0.11**	0.12	0.13	V	max	A
	G = +5, R_L = 150Ω to 2.5V	0.21	**0.24**	0.25	0.26	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 2.5V	4.91	**4.89**	4.88	4.87	V	min	A
	G = +5, R_L = 150Ω to 2.5V	4.78	**4.75**	4.73	4.72	V	min	A
Current Output, Sourcing and Sinking		±75	**±58**	±53	±50	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	±140				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.06				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +9°C at high temperature limit for over temperature specifications.
(4) Current considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**
At T_A = +25°C, G = +2, R_F = 750Ω, and R_L = 150Ω to V_S/2, unless otherwise noted.

		OPA4830IPW						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	typ	C
Maximum Operating Voltage			**+11**	+11	+11	V	max	A
Maximum Quiescent Current	V_S = +5V, All Channels	15.6	**16.6**	19.4	22.2	mA	max	A
Minimum Quiescent Current	V_S = +5V, All Channels	15.6	**14.8**	13.6	12.0	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: IPW		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
PW TSSOP-14		95				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +3V

Boldface limits are tested at **+25°C.**
At T_A = +25°C, G = +2, and R_L = 150Ω to V_S/3, unless otherwise noted.

		OPA4830IPW					
		TYP	MIN/MAX OVER TEMPERATURE				
PARAMETER	CONDITIONS	+25°C	+25°C(2)	0°C to +70°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE (see Figure 73)							
Small-Signal Bandwidth	G = +2, V_O ≤ 0.2V_{PP}	100	70	66	MHz	min	B
	G = +5, V_O ≤ 0.2V_{PP}	21	15	14	MHz	min	B
	G = +10, V_O ≤ 0.2V_{PP}	10	7.5	6.5	MHz	min	B
Gain-Bandwidth Product	G ≥ +10	100	75	65	MHz	min	B
Slew Rate	1V Step	220	135	105	V/µs	min	B
Rise Time	0.5V Step	3.4	5.6	5.7	ns	max	B
Fall Time	0.5V Step	3.4	5.6	5.7	ns	max	B
Settling Time to 0.1%	1V Step	46	73	88	ns	max	B
Harmonic Distortion	V_O = 1V_{PP}, f = 5MHz						
2nd-Harmonic	R_L = 150Ω	–60	–56	–54	dBc	max	B
	R_L ≥ 500Ω	–65	–59	–57	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–68	–59	–58	dBc	max	B
	R_L ≥ 500Ω	–76	–65	–64	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2	10.3	10.8	nV/√Hz	max	B
Input Current Noise	f > 1MHz	3.5	4.6	5.1	pA/√Hz	max	B
DC PERFORMANCE(4)							
Open-Loop Voltage Gain		72	**66**	65	dB	min	A
Input Offset Voltage		±1.5	**±7.5**	±8.7	mV	max	A
Average Offset Voltage Drift				±27	µV/°C	max	B
Input Bias Current	V_{CM} = 1.0V	+5	**+10**	+12	µA	max	A
Input Bias Current Drift				±44	nA/°C	max	B
Input Offset Current	V_{CM} = 1.0V	±0.2	**±1.1**	±1.3	µA	max	A
Input Offset Current Drift				±5	nA/°C	max	B
INPUT							
Least Positive Input Voltage(5)		–0.45	**–0.4**	–0.27	V	max	A
Most Positive Input Voltage(5)		1.2	**1.1**	1.0	V	min	A
Common-Mode Rejection Ratio (CMRR)	Input-Referred	80	**74**	72	dB	min	A
Input Impedance							
Differential-Mode		10 || 2.1			kΩ || pF	typ	C
Common-Mode		400 || 1.2			kΩ || pF	typ	C
OUTPUT							
Least Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	0.08	**0.11**	0.125	V	max	A
	G = +5, R_L = 150Ω to 1.5V	0.17	**0.39**	0.40	V	max	A
Most Positive Output Voltage	G = +5, R_L = 1kΩ to 1.5V	2.91	**2.88**	2.85	V	min	A
	G = +5, R_L = 150Ω to 1.5V	2.82	**2.74**	2.70	V	min	A
Current Output, Sourcing and Sinking		±30	**±20**	±18	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	±45			mA	typ	C
Closed-Loop Output Impedance	See Figure 73, f < 100kHz	0.06			Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +5°C at high temperature limit for over temperature specifications.
(4) Current considered positive out of pin.
(5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +3V (continued)

Boldface limits are tested at **+25°C.**
At T_A = +25°C, G = +2, and R_L = 150Ω to V_S/3, unless otherwise noted.

PARAMETER	CONDITIONS	OPA4830IPW			UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE				
		+25°C	+25°C(2)	0°C to +70°C(3)			
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	min	B
Maximum Operating Voltage			**+11**	+11	V	max	A
Maximum Quiescent Current	V_S = +3V, All Channels	15	**16.4**	17.6	mA	max	A
Minimum Quiescent Current	V_S = +3V, All Channels	15	**13.2**	12.4	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	64	**60**	58	dB	min	A
THERMAL CHARACTERISTICS							
Specification: IPW		–40 to +85			°C	typ	C
Thermal Resistance, θ_{JA}							
PW TSSOP-14		95			°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 74).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

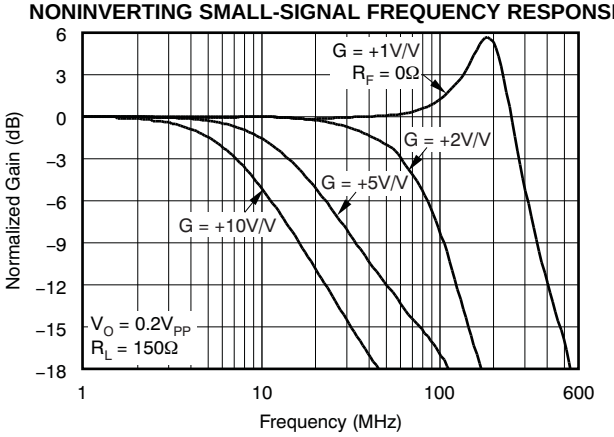


Figure 2.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

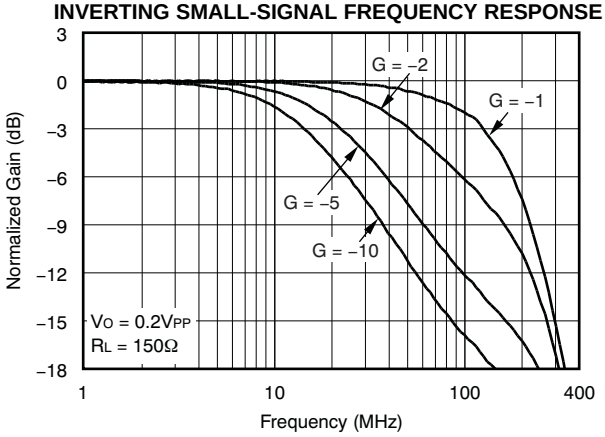


Figure 3.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

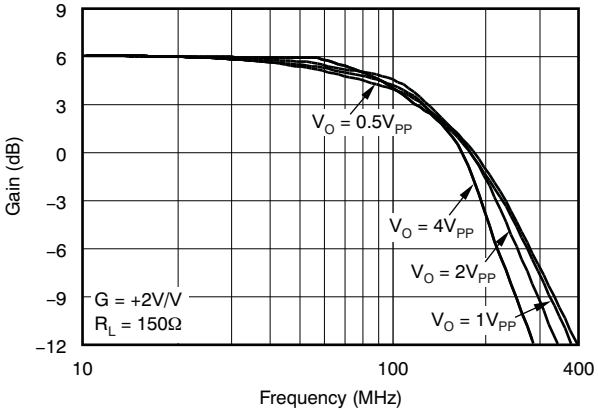


Figure 4.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

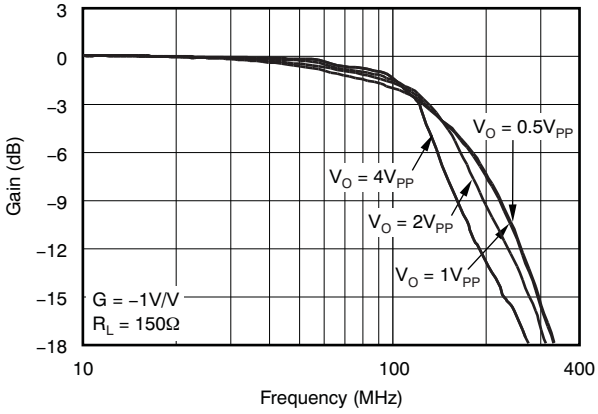


Figure 5.

NONINVERTING PULSE RESPONSE

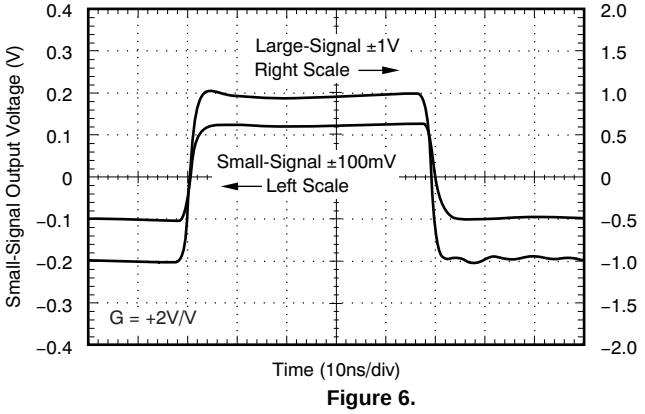


Figure 6.

INVERTING PULSE RESPONSE

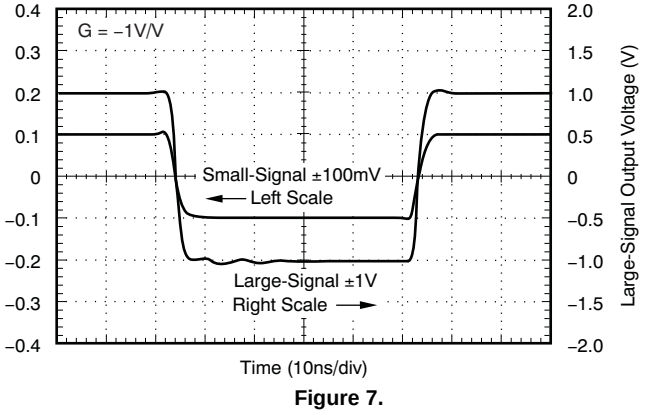


Figure 7.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 74).

HARMONIC DISTORTION vs LOAD RESISTANCE

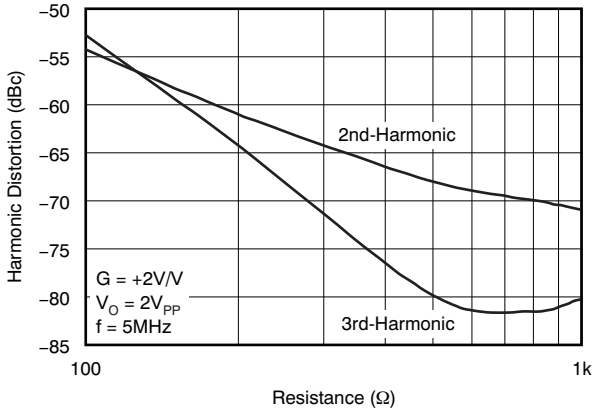


Figure 8.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

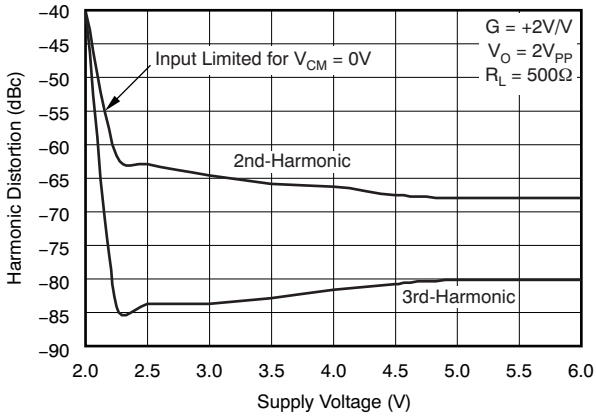


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

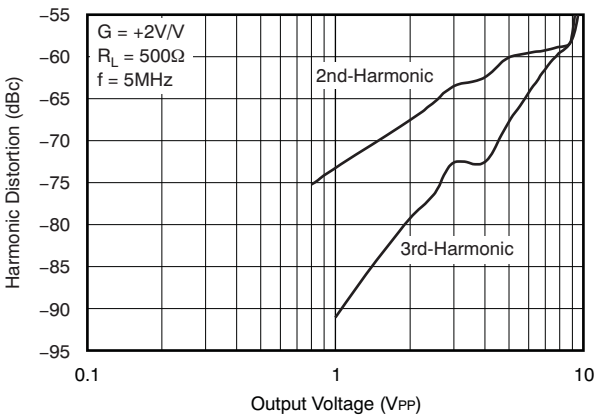


Figure 10.

HARMONIC DISTORTION vs FREQUENCY

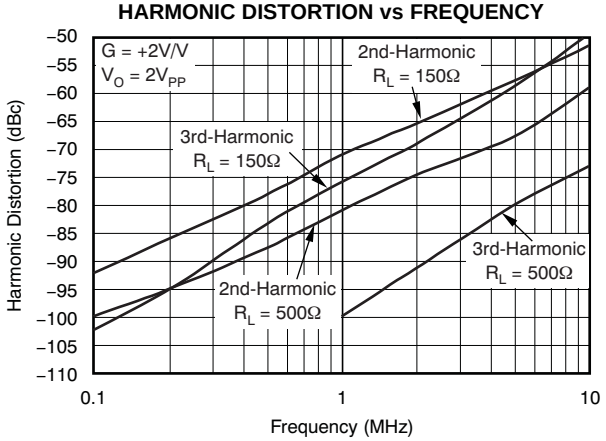


Figure 11.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

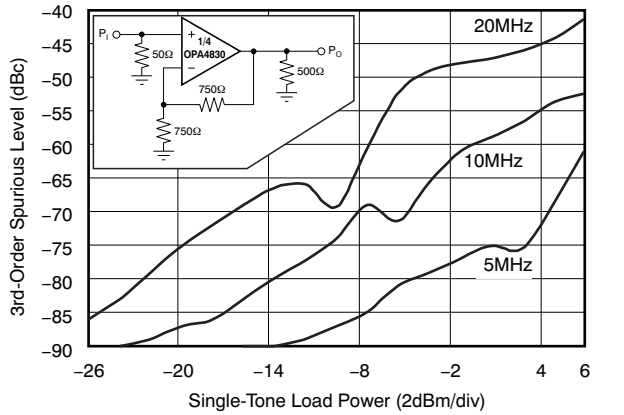


Figure 12.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

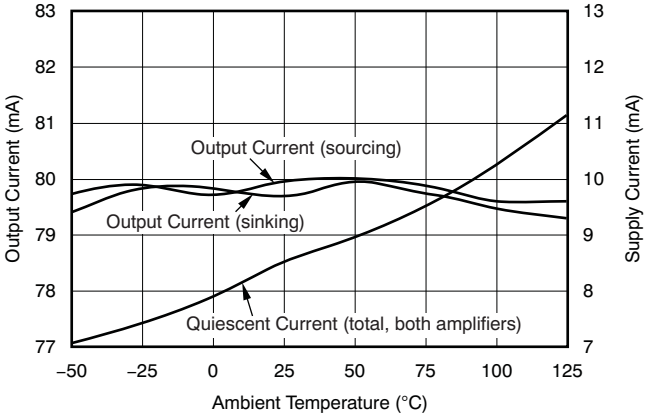


Figure 13.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω, and R_L = 150Ω to GND, unless otherwise noted (see Figure 74).

FREQUENCY RESPONSE vs CAPACITIVE LOAD

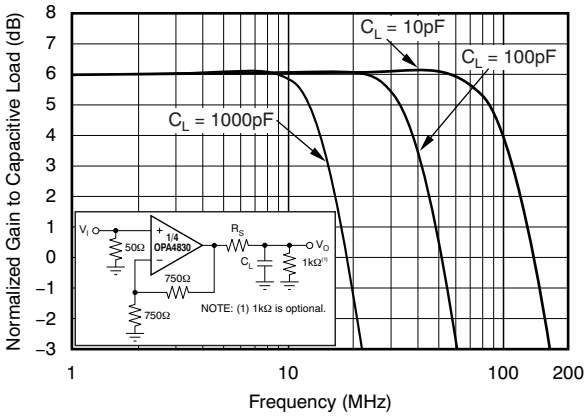


Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

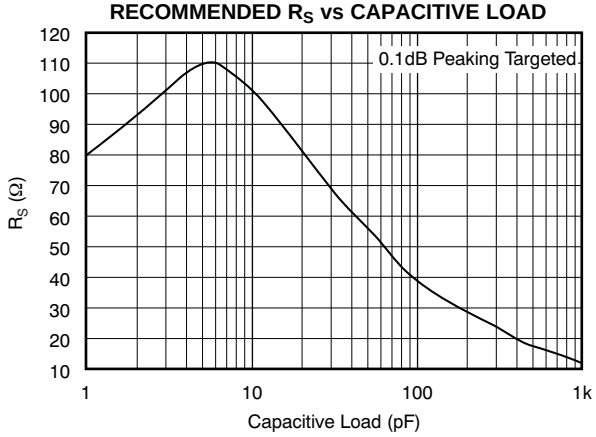


Figure 15.

OUTPUT SWING vs LOAD RESISTANCE

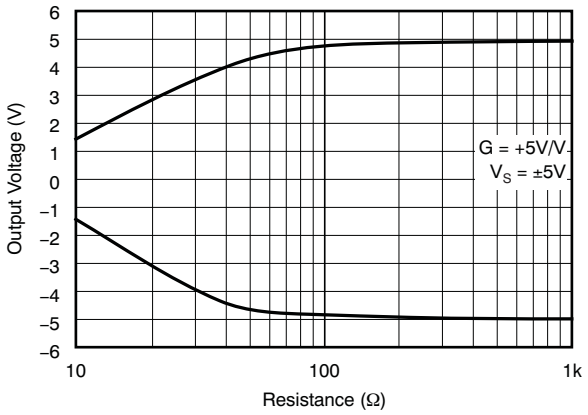


Figure 16.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

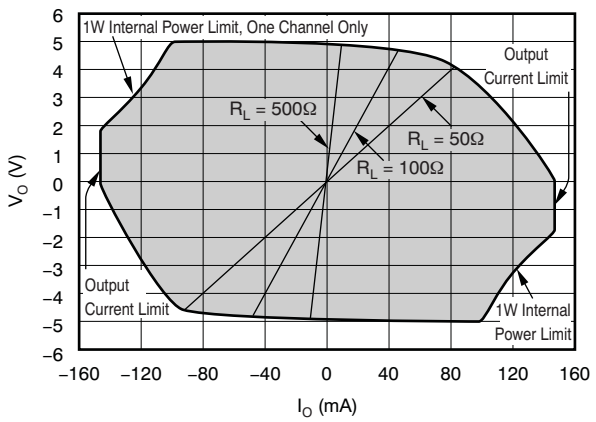


Figure 17.

TYPICAL CHARACTERISTICS: V_S = ±5V, Differential Configuration

At T_A = +25°C, R_F = 604Ω (as shown in Figure 18), and R_L = 500Ω, unless otherwise noted.

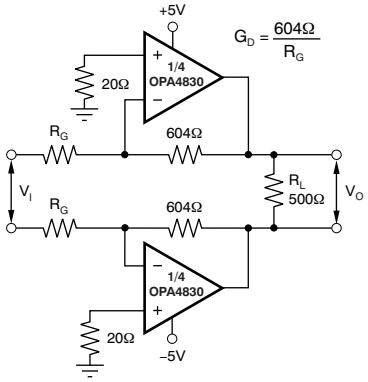


Figure 18.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

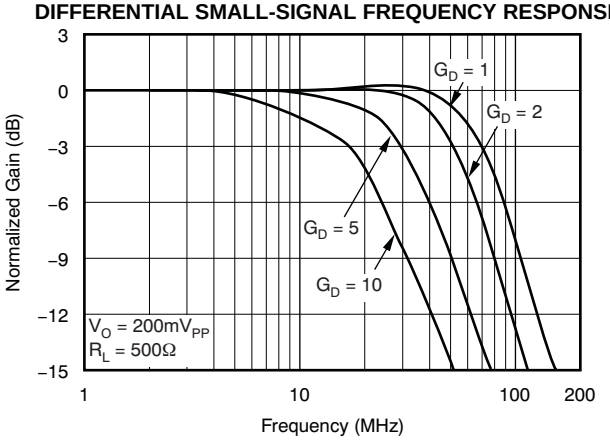


Figure 19.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

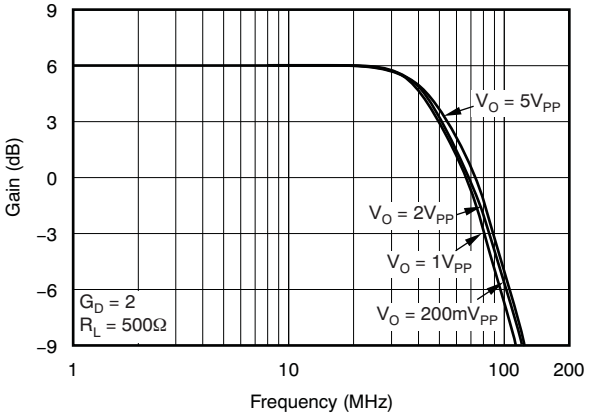


Figure 20.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

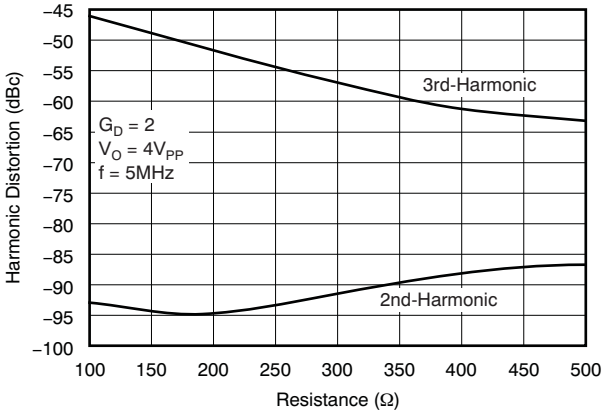


Figure 21.

DIFFERENTIAL DISTORTION vs FREQUENCY

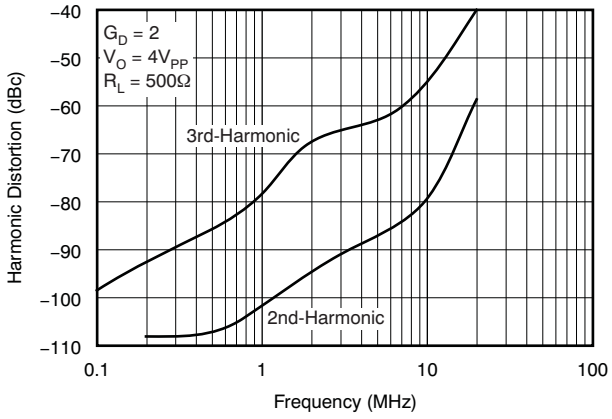


Figure 22.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

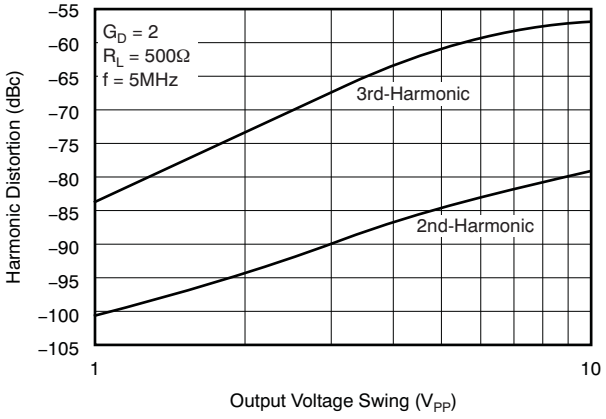


Figure 23.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2V/V, R_F = 750Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 72).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

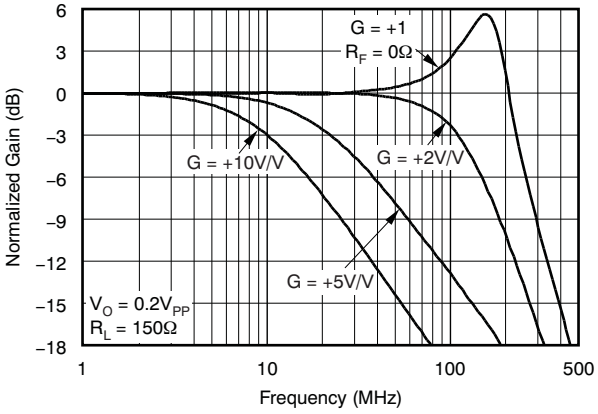


Figure 24.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

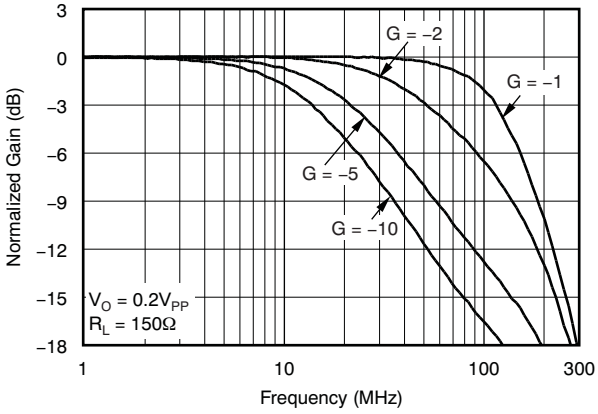


Figure 25.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

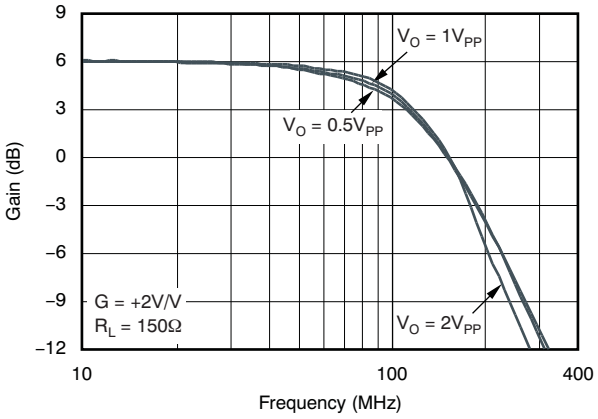


Figure 26.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

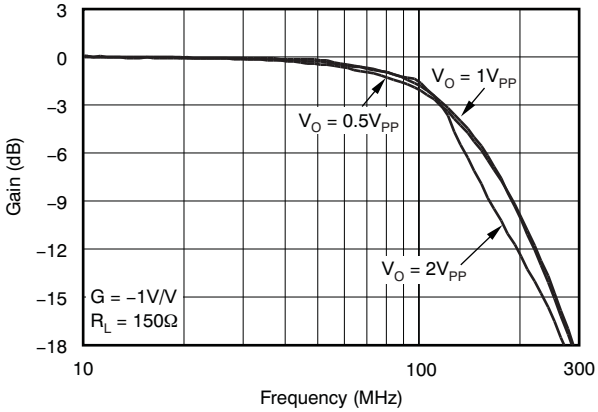


Figure 27.

NONINVERTING PULSE RESPONSE

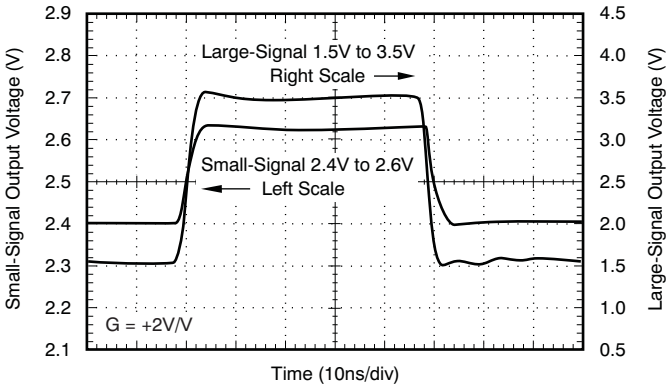


Figure 28.

INVERTING PULSE RESPONSE

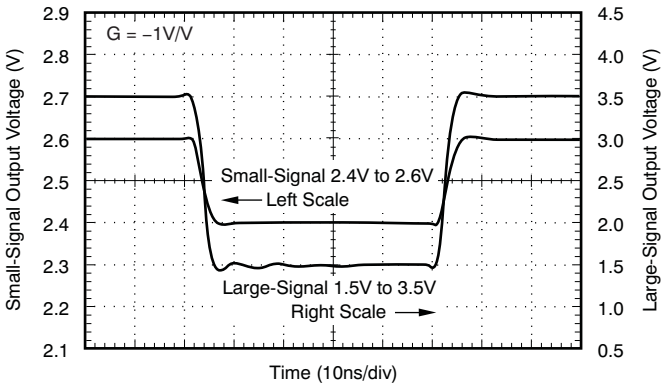


Figure 29.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 72).

HARMONIC DISTORTION vs LOAD RESISTANCE

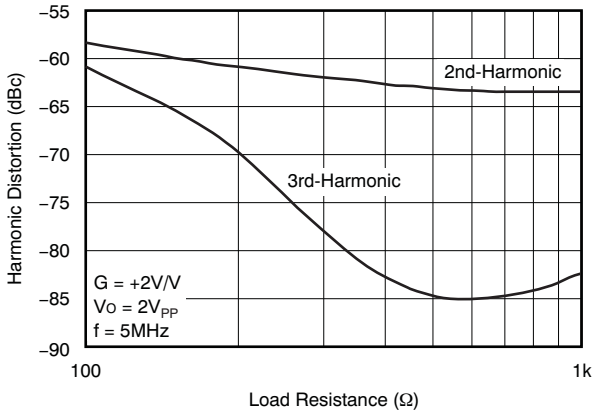


Figure 30.

HARMONIC DISTORTION vs FREQUENCY

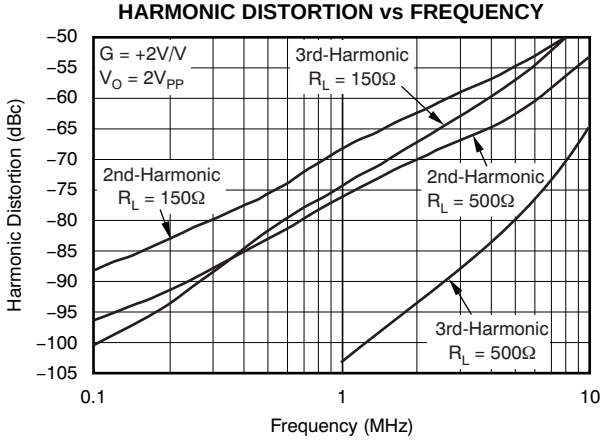


Figure 31.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

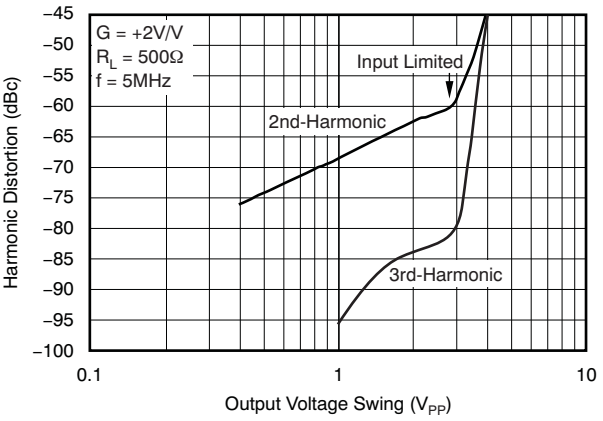


Figure 32.

HARMONIC DISTORTION vs NONINVERTING GAIN

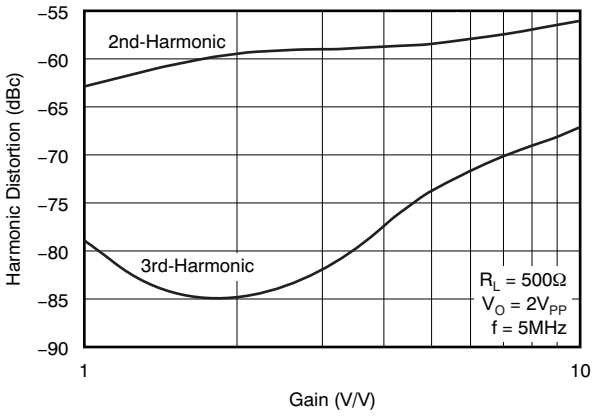


Figure 33.

HARMONIC DISTORTION vs INVERTING GAIN

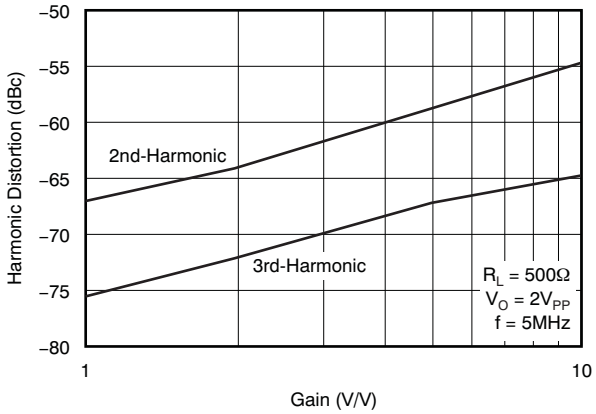


Figure 34.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

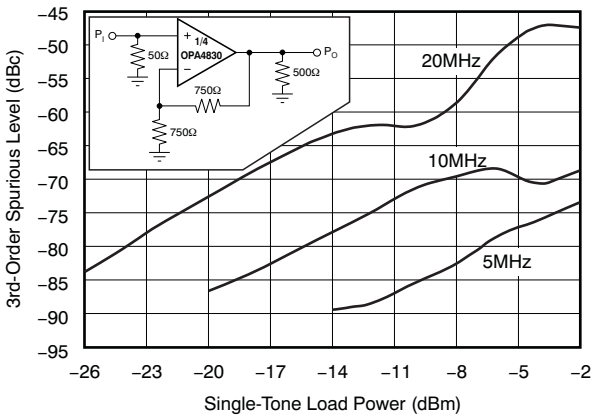


Figure 35.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 72).

INPUT VOLTAGE AND CURRENT NOISE DENSITY

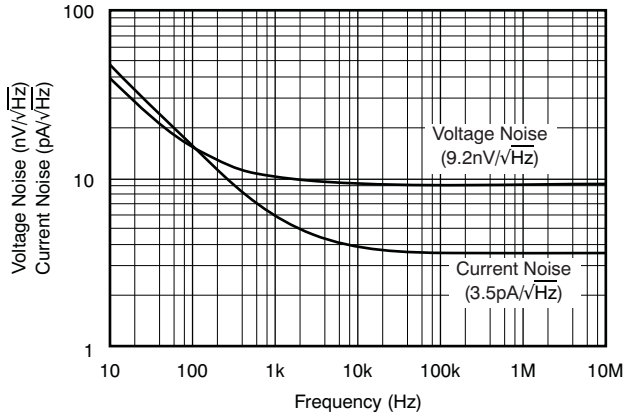


Figure 36.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

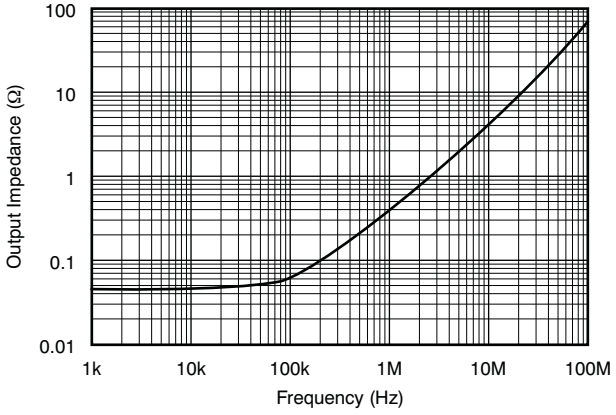


Figure 37.

RECOMMENDED R_S vs CAPACITIVE LOAD

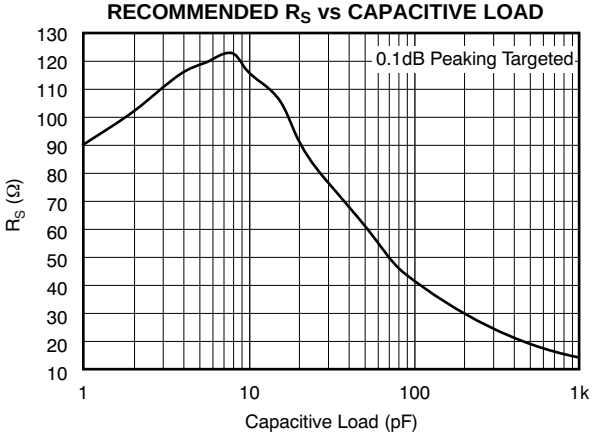


Figure 38.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

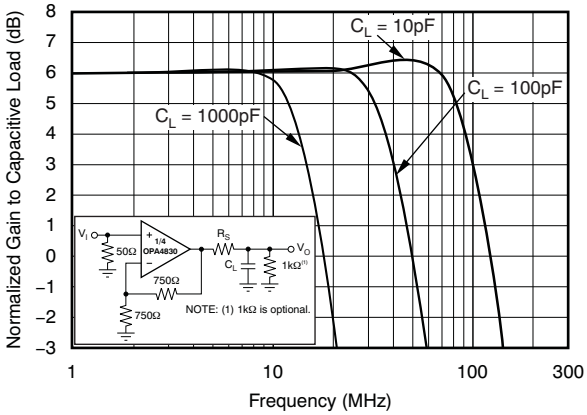


Figure 39.

OPEN-LOOP GAIN AND PHASE

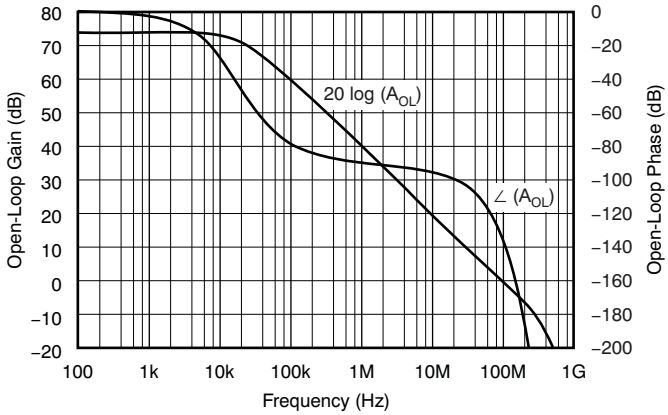


Figure 40.

VOLTAGE RANGES vs TEMPERATURE

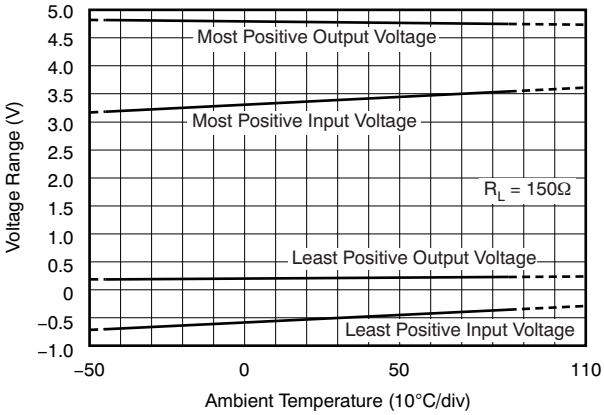


Figure 41.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 750Ω to V_S/2, and input V_{CM} = 2.5V, unless otherwise noted (see Figure 72).

TYPICAL DC DRIFT OVER TEMPERATURE

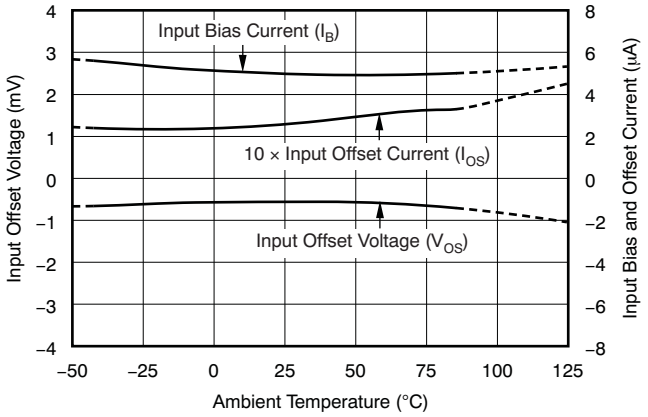


Figure 42.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

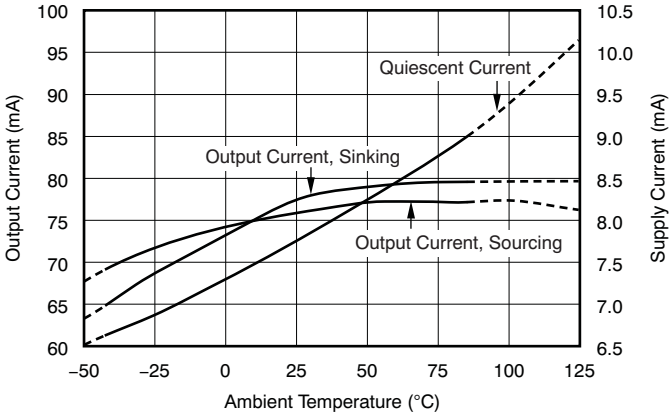


Figure 43.

CMRR AND PSRR vs FREQUENCY

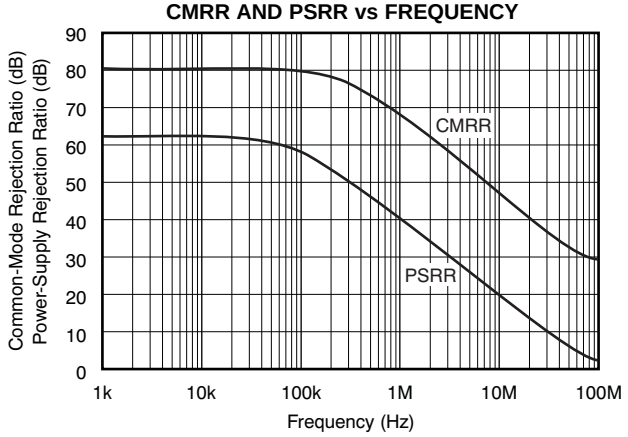


Figure 44.

OUTPUT SWING vs LOAD RESISTANCE

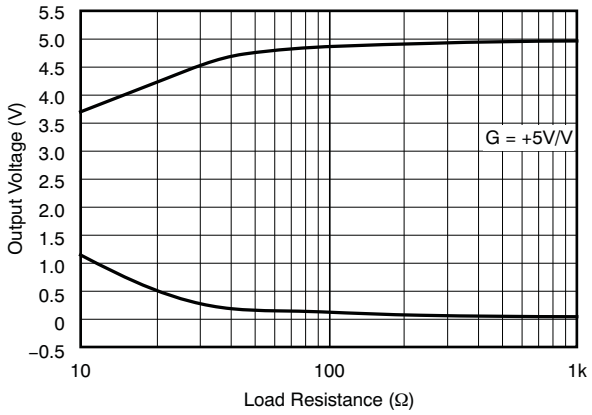


Figure 45.

CROSSTALK vs FREQUENCY

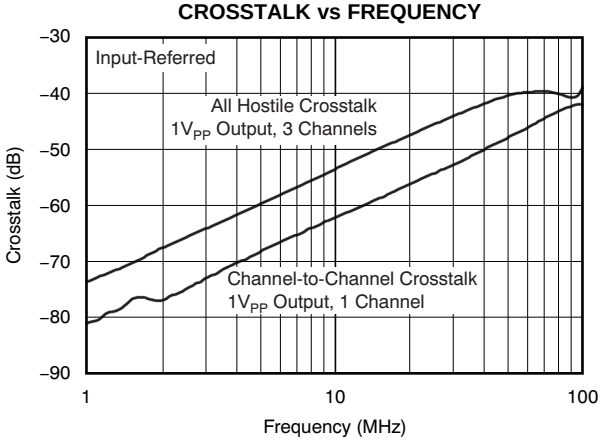


Figure 46.

TYPICAL CHARACTERISTICS: V_S = +5V, Differential Configuration

At T_A = +25°C, R_F = 604Ω, and R_L = 500Ω differential (as shown in Figure 47), unless otherwise noted.

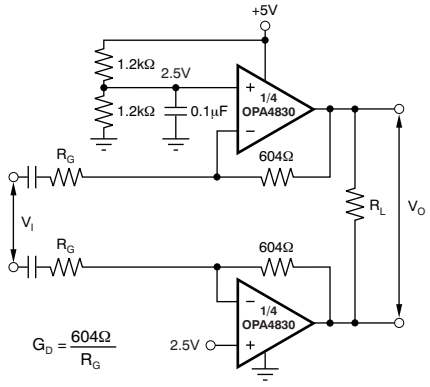


Figure 47.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

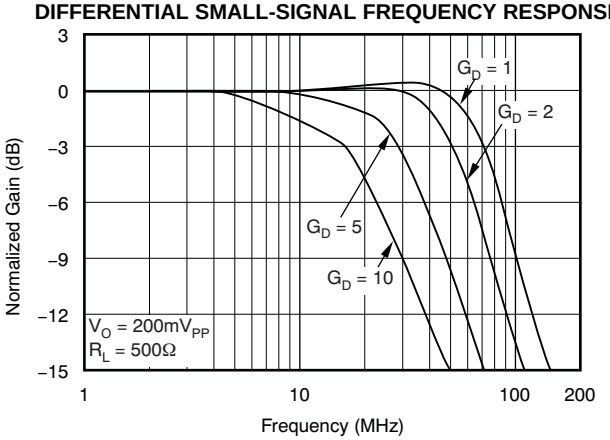


Figure 48.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

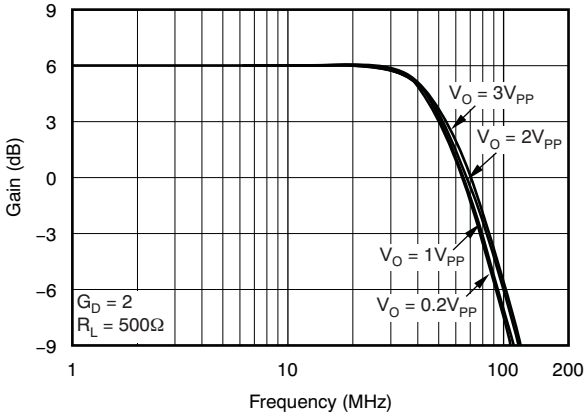


Figure 49.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

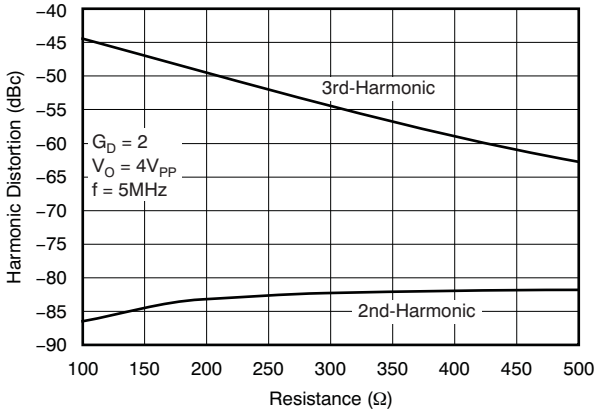


Figure 50.

DIFFERENTIAL DISTORTION vs FREQUENCY

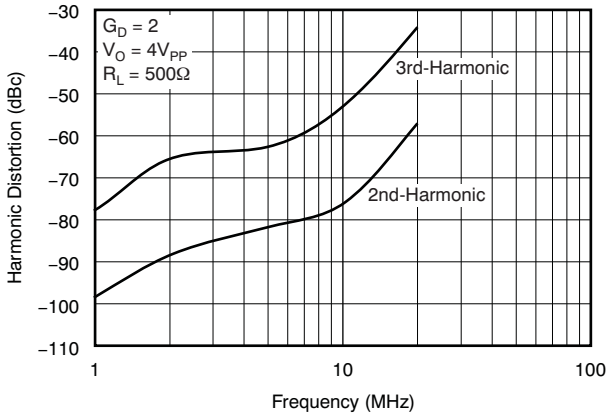


Figure 51.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

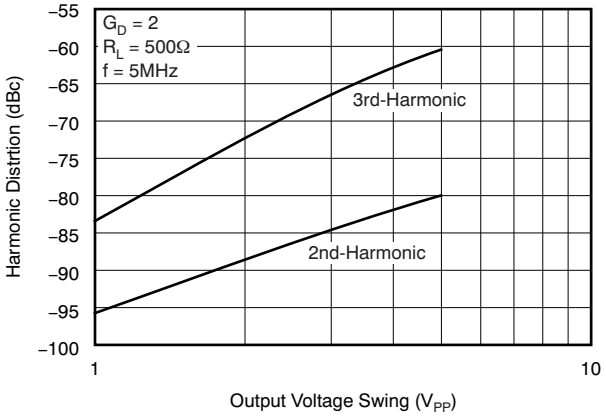


Figure 52.

TYPICAL CHARACTERISTICS: V_S = +3V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 73).

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

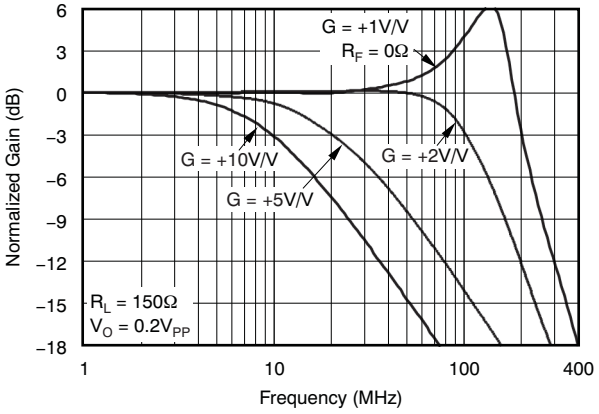


Figure 53.

INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

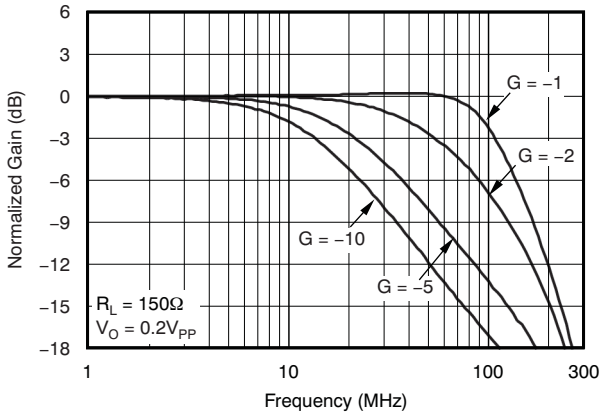


Figure 54.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

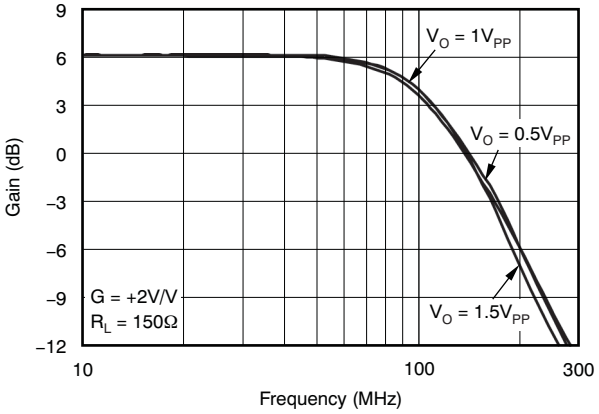


Figure 55.

INVERTING LARGE-SIGNAL FREQUENCY RESPONSE

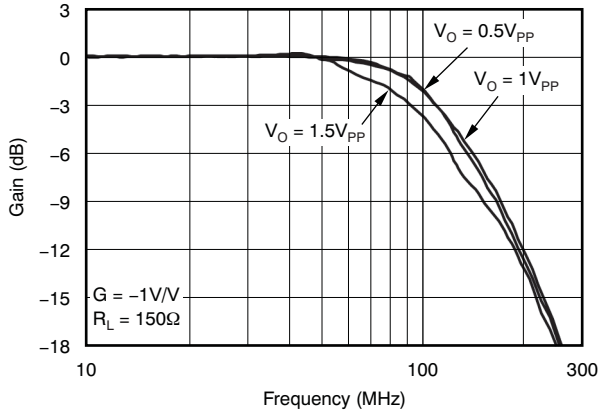


Figure 56.

NONINVERTING PULSE RESPONSE

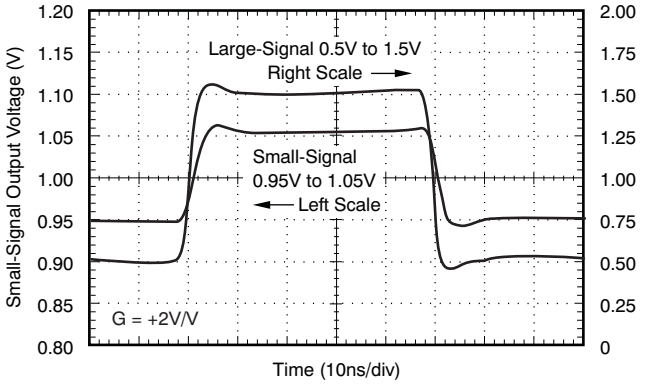


Figure 57.

INVERTING PULSE RESPONSE

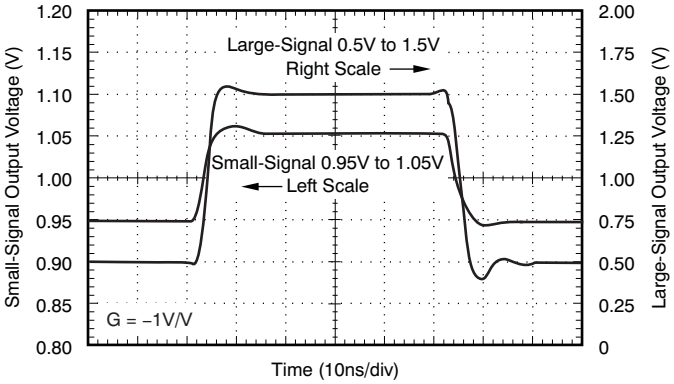


Figure 58.

TYPICAL CHARACTERISTICS: V_S = +3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 73).

HARMONIC DISTORTION vs LOAD RESISTANCE

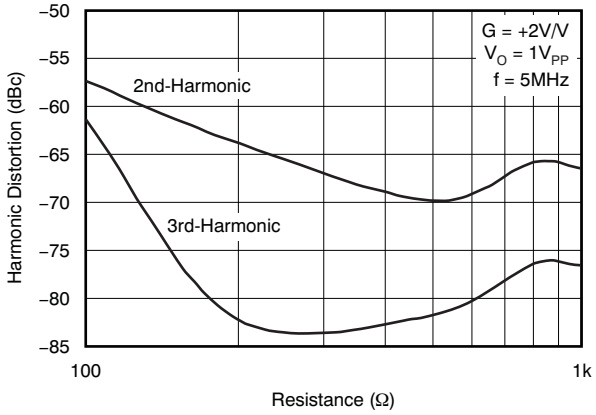


Figure 59.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

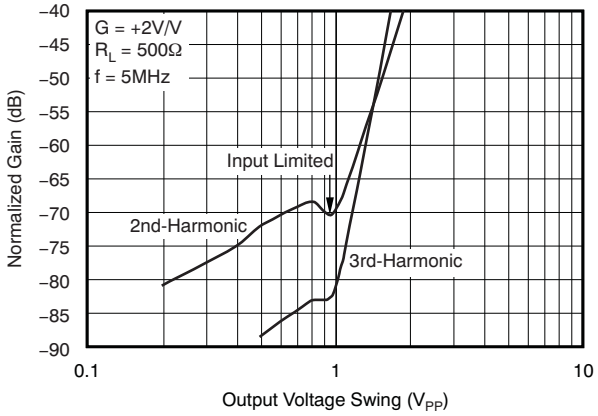


Figure 60.

HARMONIC DISTORTION vs FREQUENCY

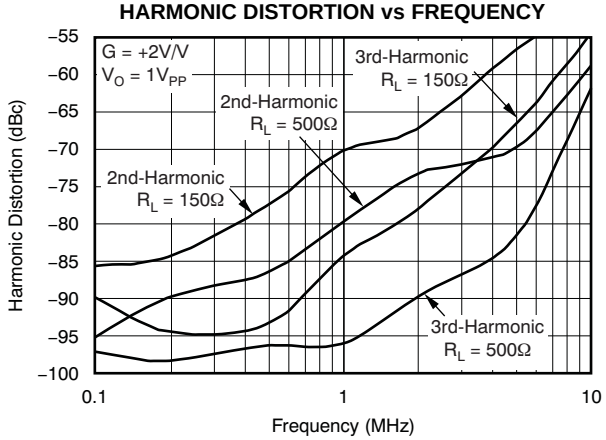


Figure 61.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

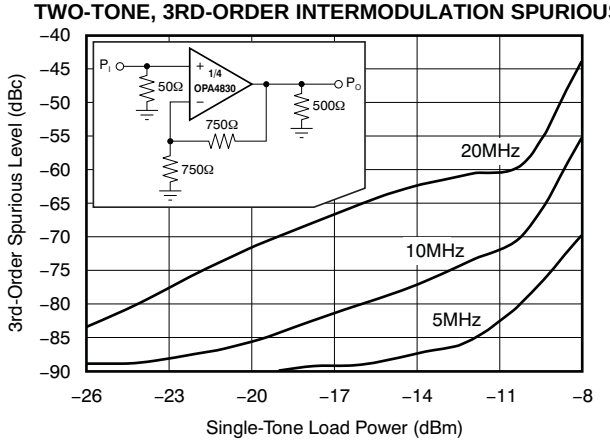


Figure 62.

RECOMMENDED R_S vs CAPACITIVE LOAD

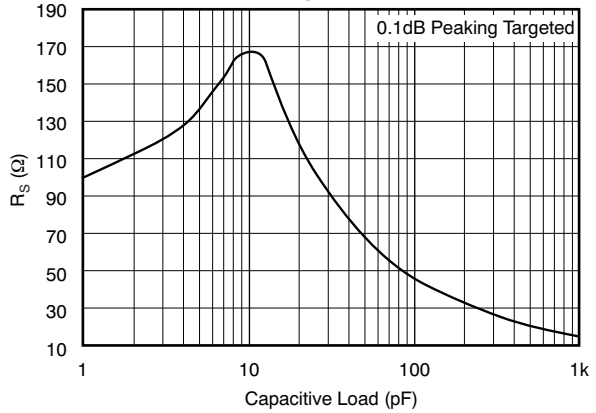


Figure 63.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

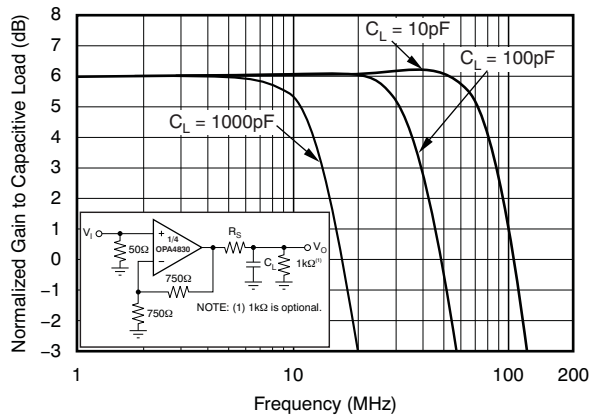


Figure 64.

TYPICAL CHARACTERISTICS: V_S = +3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_S/3, unless otherwise noted (see Figure 73).

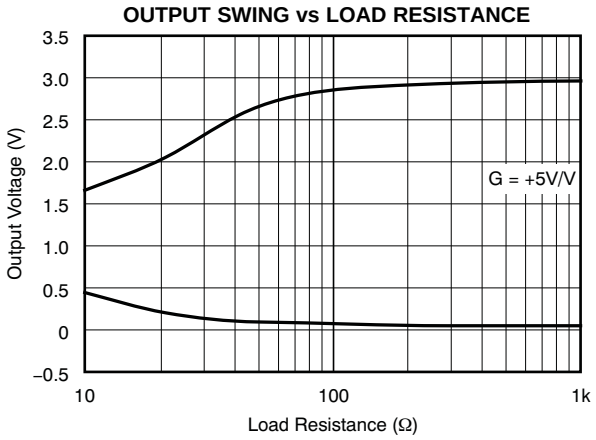


Figure 65.

TYPICAL CHARACTERISTICS: V_S = +3V, Differential Configuration

At T_A = +25°C, R_F = 604Ω, and R_L = 500Ω differential (as shown in Figure 66), unless otherwise noted.

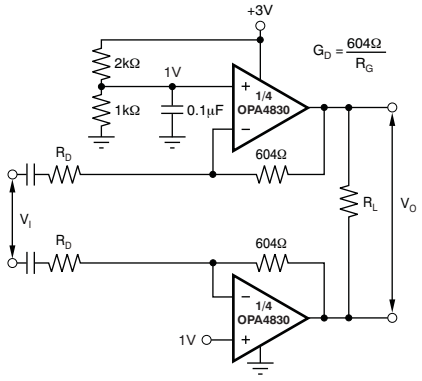


Figure 66.

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

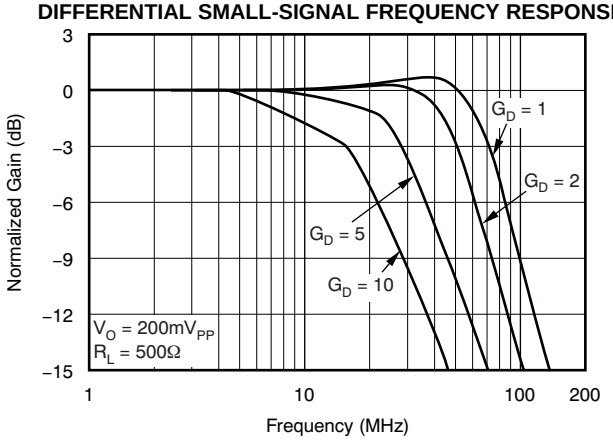


Figure 67.

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

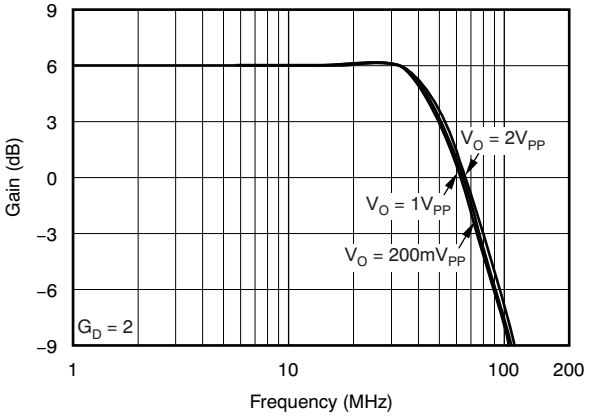


Figure 68.

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

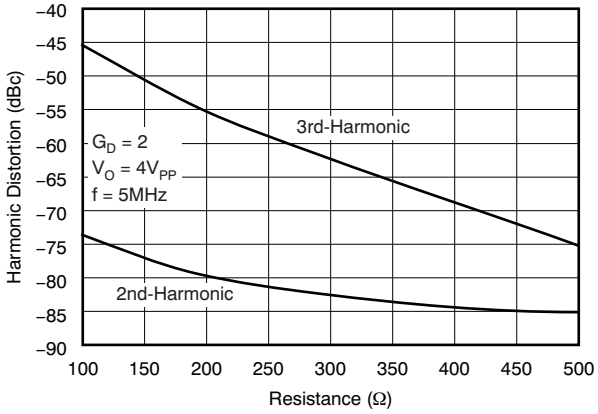


Figure 69.

DIFFERENTIAL DISTORTION vs FREQUENCY

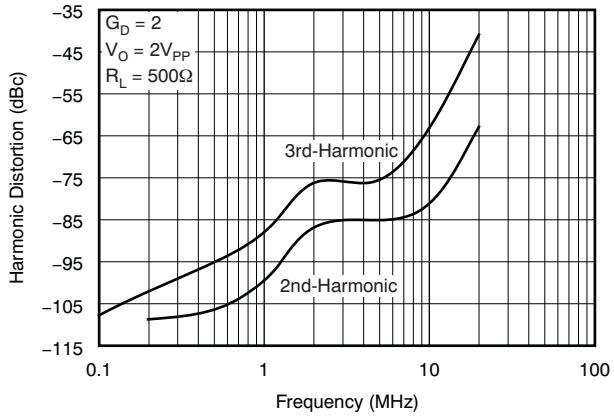


Figure 70.

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

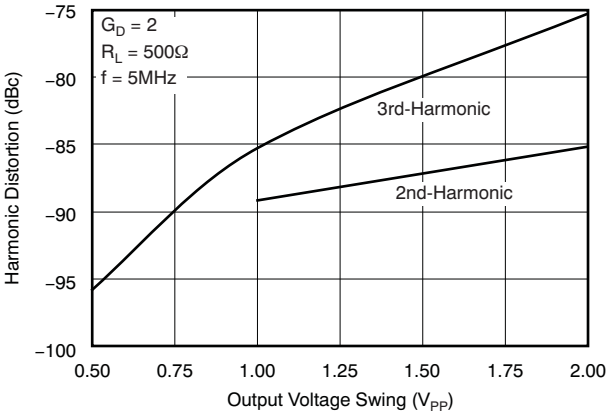


Figure 71.

APPLICATION INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA4830 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +10V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA4830 is compensated to provide stable operation with a wide range of resistive loads.

Figure 72 shows the ac-coupled, gain of +2V/V configuration used for the +5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 72, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.5kΩ resistors at the noninverting input provide the common-mode bias voltage. This parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset because of input bias current.

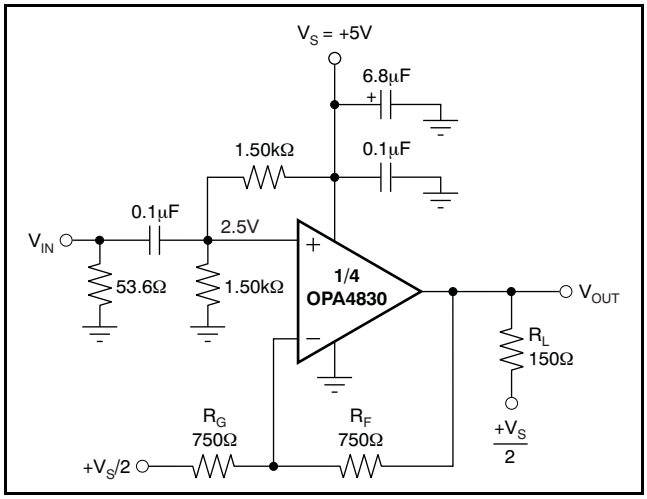


Figure 72. AC-Coupled, G = +2V/V, +5V Single-Supply Specification and Test Circuit

Figure 73 shows the ac-coupled, gain of +2V/V configuration used for the +3V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 73, the total effective load on the output at high frequencies is 150Ω || 1500Ω. The 1.13kΩ and 2.26kΩ resistors at the noninverting input provide the common-mode bias voltage. The parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset as a result of input bias current.

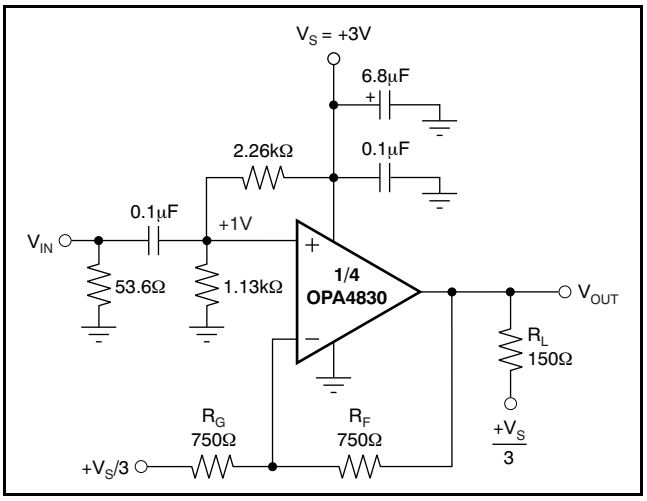


Figure 73. AC-Coupled, G = +2V/V, +3V Single-Supply Specification and Test Circuit

Figure 74 illustrates the dc-coupled, gain of +2V/V, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 74, the total effective load is 150Ω ‖ 1.5kΩ. Two optional components are included in Figure 74. An additional resistor (348Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 375Ω source resistance seen at the inverting input (see the DC Accuracy and Offset Control section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board layouts, this optional capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

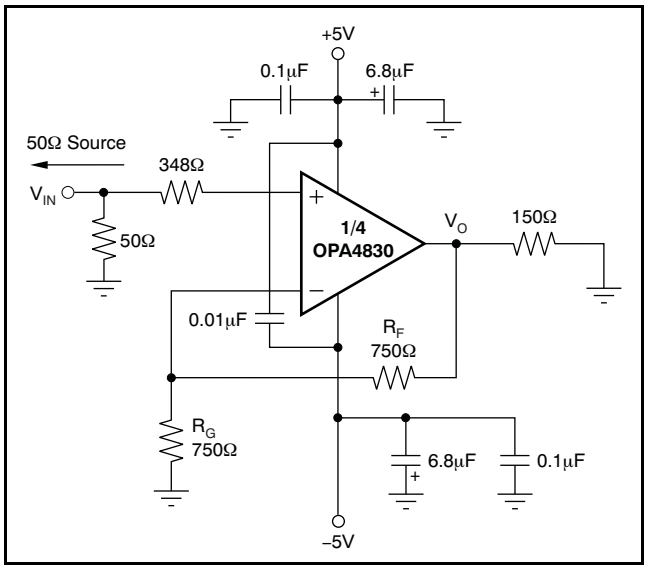


Figure 74. DC-Coupled, G = +2V/V, Bipolar Supply Specification and Test Circuit

DC LEVEL-SHIFTING

Figure 75 shows a DC-coupled noninverting amplifier that level-shifts the input up to accommodate the desired output voltage range. Given the desired signal gain (G), and the amount V_{OUT} needs to be shifted up (ΔV_{OUT}) when V_{IN} is at the center of its range, Equation 1 and Equation 2 give the resistor values that produce the desired performance. Assume that R_4 is between 200Ω and 1.5kΩ.

$$NG = G + V_{OUT}/V_S$$
$$R_1 = R_4/G$$
$$R_2 = R_4/(NG - G)$$
$$R_3 = R_4/(NG - 1) \quad (1)$$

where:

$$NG = 1 + R_4/R_3$$
$$V_{OUT} = (G)V_{IN} + (NG - G)V_S \quad (2)$$

Make sure that V_{IN} and V_{OUT} stay within the specified input and output voltage ranges.

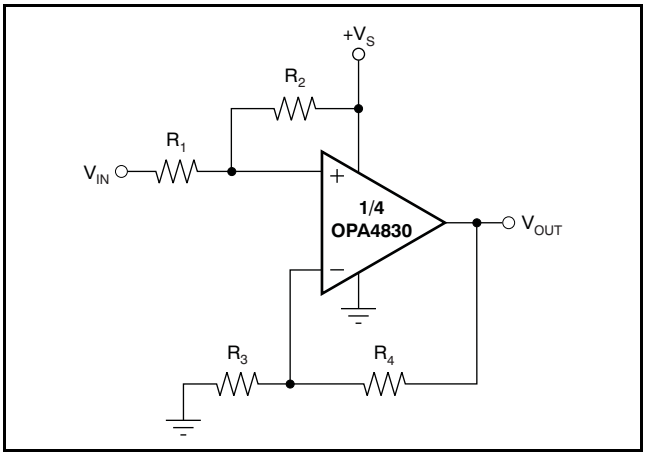


Figure 75. DC Level-Shifting

The circuit on the front page is a good example of this type of application. It was designed to take V_{IN} between 0V and 0.5V and produce V_{OUT} between 1V and 2V when using a +3V supply. This output means G = 2.00, and ΔV_{OUT} = 1.50V – G × 0.25V = 1.00V. Plugging these values into Equation 1 and Equation 2 (with R_4 = 750Ω) gives: NG = 2.33, R_1 = 375Ω, R_2 = 2.25kΩ, and R_3 = 563Ω. The resistors were changed to the nearest standard values for the front page circuit.

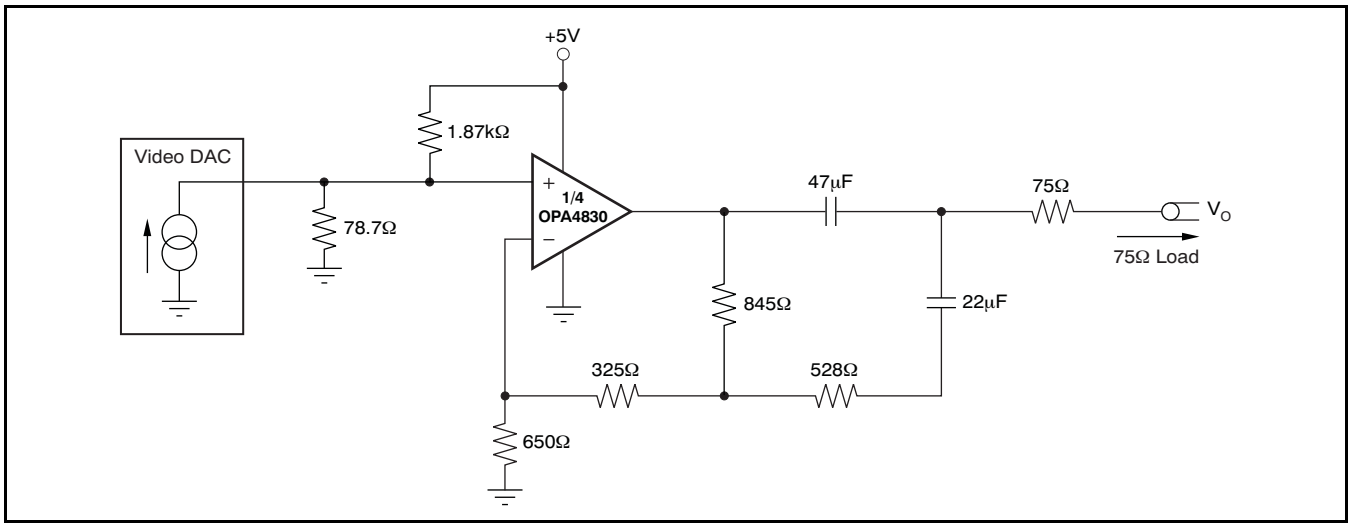


Figure 76. Video Line Driver with SAG Correction

AC-COUPLED OUTPUT VIDEO LINE DRIVER

Low-power and low-cost video line drivers often buffer digital-to-analog converter (DAC) outputs with a gain of 2V/V into a doubly-terminated line. Those interfaces typically require a dc blocking capacitor. For a simple solution, that interface often has used a very large value blocking capacitor (220µF) to limit tilt, or SAG, across the frames. One approach to creating a very low high-pass pole location using much lower capacitor values is shown in Figure 76. This circuit gives a voltage gain of 2 at the output pin with a high-pass pole at 8Hz. Given the 150Ω load, a simple blocking capacitor approach would require a 133µF value. The two much lower valued capacitors give this same low-pass pole using this simple SAG correction circuit of Figure 76.

The input is shifted slightly positive in Figure 76 using the voltage divider from the positive supply. This configuration gives about a 200mV input dc offset that shows up at the output pin as a 400mV dc offset when the DAC output is at zero current during the sync tip portion of the video signal. This offset acts to hold the output in its linear operating region. This circuit then passes on any power-supply noise to the output with a gain of approximately –20dB, so good supply decoupling is recommended on the power-supply pin. Figure 77 shows the frequency response for the circuit of Figure 76. This plot shows the 8Hz low-frequency high-pass pole and a high-end cutoff at approximately 100MHz.

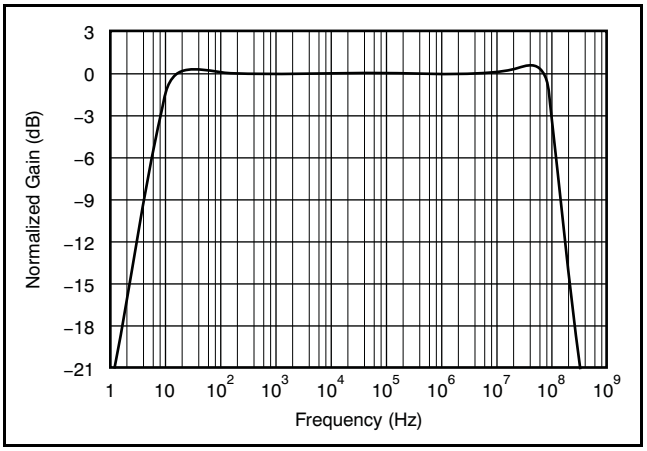


Figure 77. Video Line Driver Response to Matched Load

NONINVERTING AMPLIFIER WITH REDUCED PEAKING

Figure 78 shows a noninverting amplifier that reduces peaking at low gains. The resistor RC compensates the OPA4830 to have higher noise gain (NG), which reduces the ac response peaking (typically 5dB at G = +1V/V without RC) without changing the dc gain. V_{IN} needs to be a low-impedance source, such as an op amp. The resistor values are low in order to reduce noise. Using both R_T and R_F helps minimize the impact of parasitic impedances.

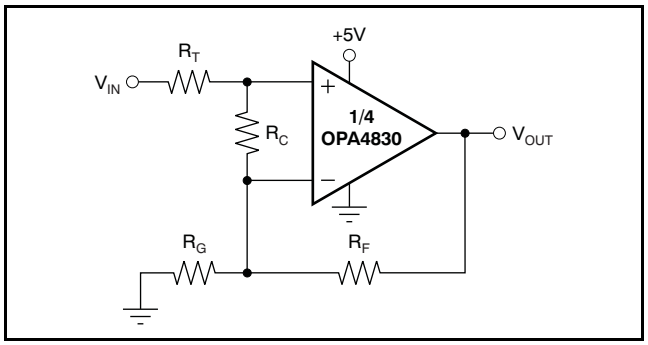


Figure 78. Compensated Noninverting Amplifier

The noise gain can be calculated as shown in Equation 3, Equation 4, and Equation 5:

$$G_1 = 1 + \frac{R_F}{R_G} \quad (3)$$

$$G_2 = 1 + \frac{R_T + \frac{R_F}{G_1}}{R_C} \quad (4)$$

$$NG = G_1 \times G_2 \quad (5)$$

A unity-gain buffer can be designed by selecting R_T = R_F = 20.0Ω and R_C = 40.2Ω (do not use R_G). This circuit gives a noise gain of 2V/V, so the response is similar to the characteristics plots with G = +2V/V. Decreasing R_C to 20.0Ω increases the noise gain to 3V/V, which typically gives a flat frequency response, but with less bandwidth.

The circuit in Figure 72 can be redesigned to have less peaking by increasing the noise gain to 3. This increase is accomplished by adding R_C = 2.55kΩ across the op amp inputs.

SINGLE-SUPPLY ACTIVE FILTER

The OPA4830, while operating on a single +3V or +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. Figure 79 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are ac-coupled using 0.1µF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 32kHz for the component values shown). As discussed for Figure 72, this configuration allows the midpoint bias formed by the two 1.87kΩ resistors to appear at both the input and output pins. The midband signal gain is set to +4 (12dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +4, the OPA4830 on a single supply shows 30MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit show a precise 1MHz, –3dB point with a maximally-flat passband (above the 32kHz ac-coupling corner), and a maximum stop band attenuation of 36dB at the amplifier –3dB bandwidth of 30MHz.

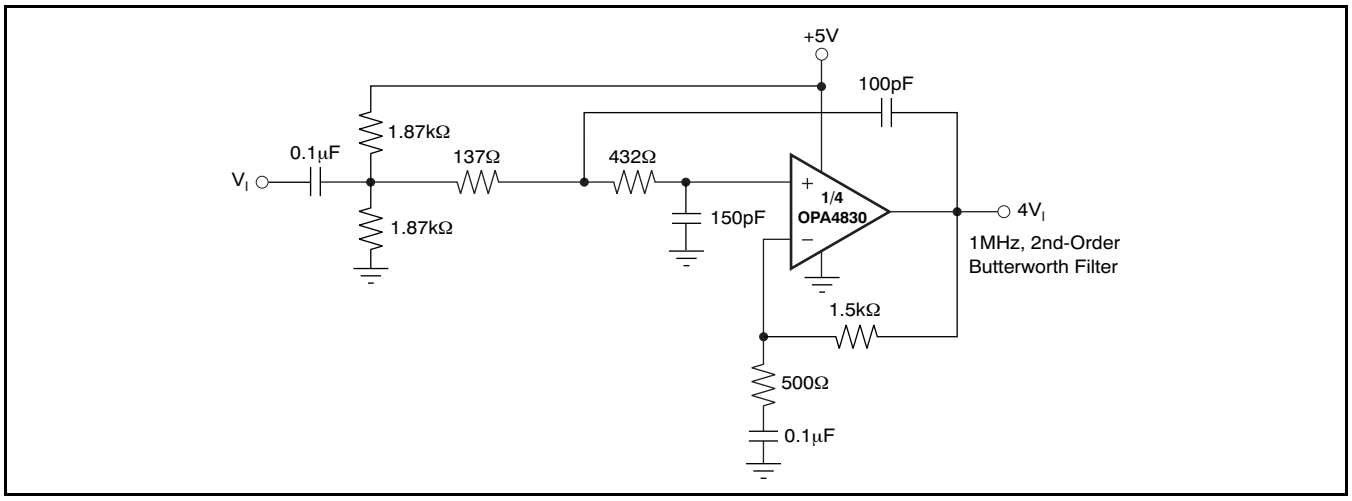


Figure 79. Single-Supply, High-Frequency Active Filter

DIFFERENTIAL INTERFACE APPLICATIONS

Dual and quad op amps are particularly suitable to differential input to differential output applications. Typically, these op amps fall into either ADC input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Because the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA4830. Each has its advantages and disadvantages. Figure 80 shows a basic starting point for noninverting differential I/O applications.

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the amplifier gain. The differential signal gain for the circuit of Figure 80 is shown in Equation 6:

$$\frac{V_O}{V_I} = A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (6)$$

Figure 80 shows the recommended value of 750Ω. However, the gain may be adjusted using just the R_G resistor.

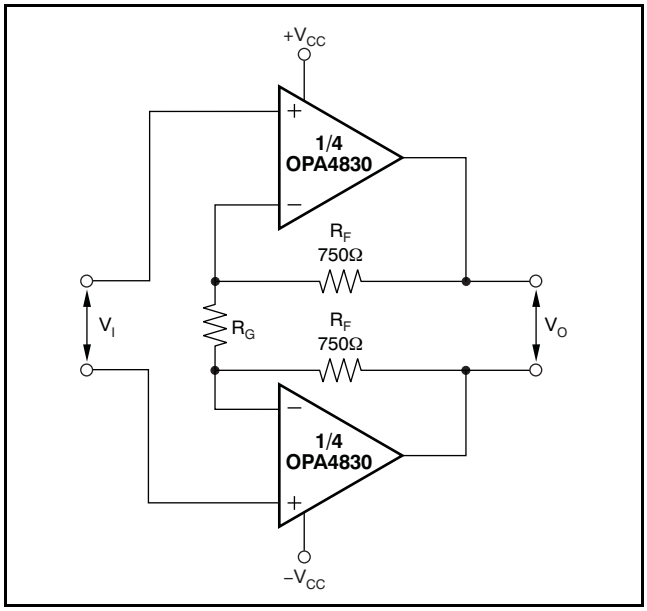


Figure 80. Noninverting Differential I/O Amplifier

Various combinations of single-supply or ac-coupled gains can also be delivered using the basic circuit of Figure 80. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1V/V because an equal dc voltage at each inverting node creates no current through R_G, giving that voltage a common-mode gain of 1 to the output.

Figure 81 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become the input resistance for the source. This configuration provides a better noise performance than the noninverting configuration, but does limit the flexibility in setting the input impedance separately from the gain.

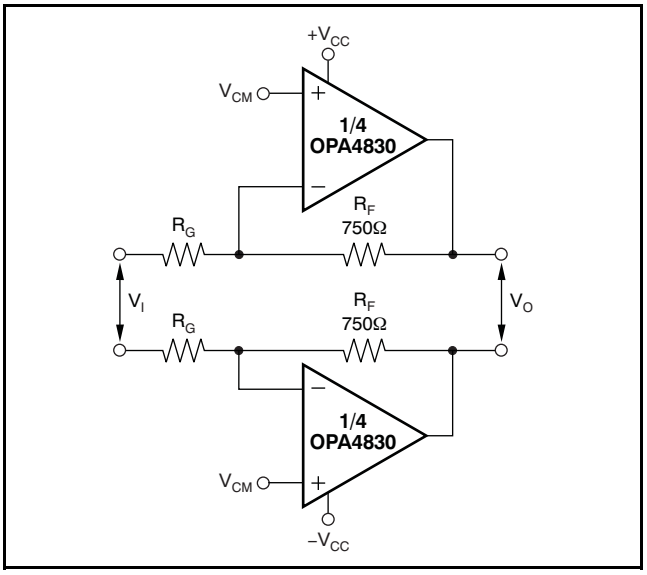


Figure 81. Inverting Differential I/O Amplifier

The two noninverting inputs provide an easy common-mode control input. This control is particularly useful if the source is ac-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving an easy common-mode control for single-supply operation. The input resistors may be adjusted to the desired gain but also change the input impedance as well. The differential gain for this circuit is shown in Equation 7:

$$\frac{V_O}{V_I} = -\frac{R_F}{R_G} \quad (7)$$

DC-COUPLED SINGLE-TO-DIFFERENTIAL CONVERSION

The previous differential output circuits were set up to receive a differential input as well as provide a differential output. Figure 82 illustrates one way to provide a single-to-differential conversion, with dc coupling, and independent output common-mode control using a quad op amp.

The circuit of Figure 82 provides several useful features for isolating the input signal from the final outputs. Using the first amplifier as a simple noninverting stage gives an independent adjustment on R_I (to set the source loading) while the gain can be easily adjusting in this stage using the R_G resistor. The next stage allows a separate output common-mode level to be set up. The desired output common-mode voltage, V_{CM}, is cut in half and applied to the noninverting input of the second stage. The signal path in this stage sees a gain of –1V/V while this (1/2 × V_{CM}) voltage sees a gain of +2V/V. The output of this second stage is then the original common-mode voltage plus the inverted signal from the output of the first stage. The 2nd stage output appears directly at the output of the noninverting final stage. The inverting node of the inverting output stage is also biased to the common-mode voltage, equal to the common-mode voltage appearing at the output of the second stage, creating no current flow and placing the desired V_{CM} at the output of this stage as well.

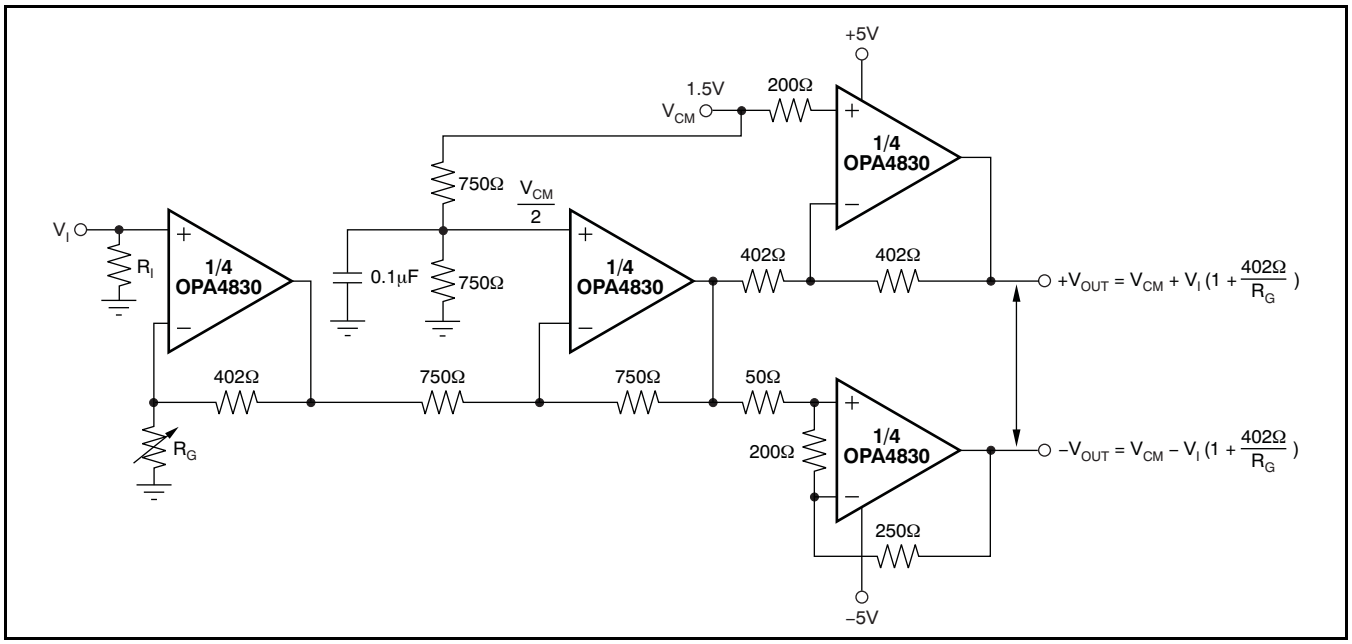


Figure 82. Wideband, DC-Coupled, Single-to-Differential Conversion

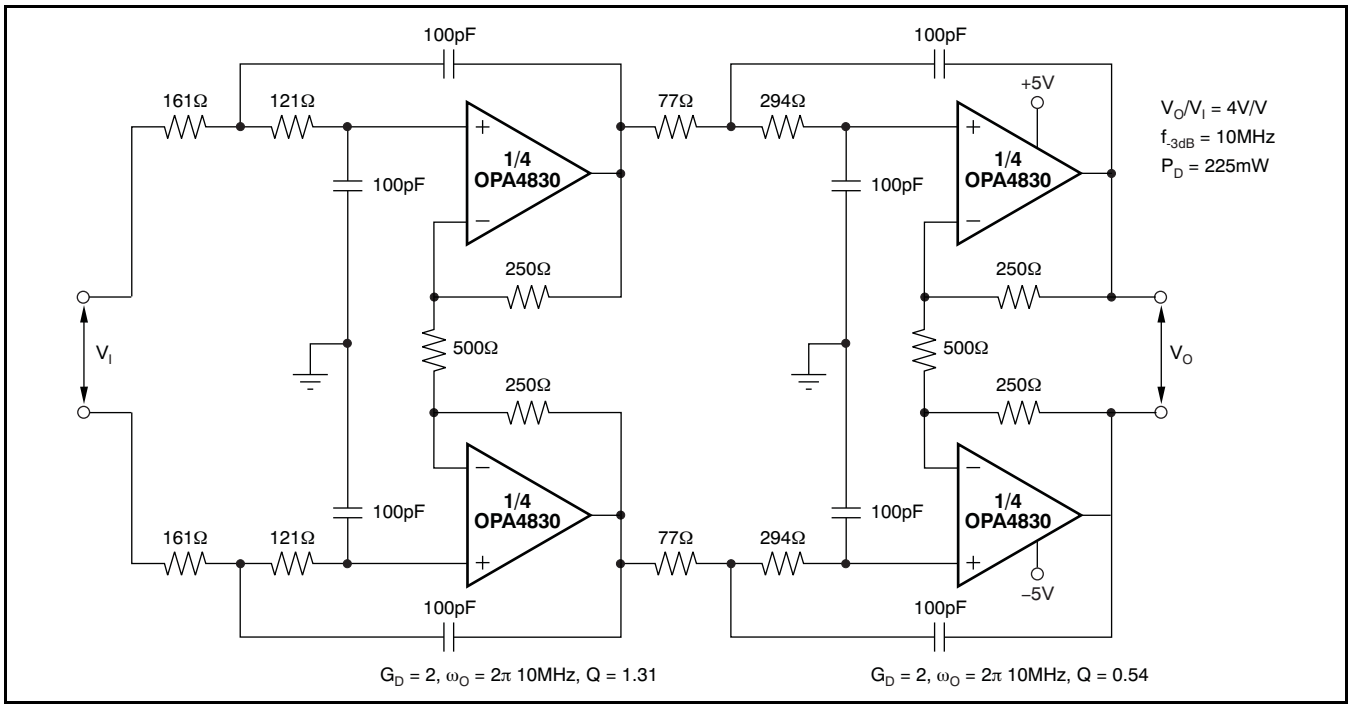


Figure 83. Low-Power, Differential I/O, 4th-Order Butterworth Active Filter

LOW-POWER, DIFFERENTIAL I/O, 4th-ORDER ACTIVE FILTER

The OPA4830 can give a very capable gain block for active filters. The quad design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. See Figure 83 for an example of a 10MHz, 4th-order Butterworth, low-pass Sallen-Key filter. The design places the higher Q stage first to allow the lower Q 2nd stage to roll off the peaked noise of the first stage. The resistor values have been adjusted slightly to account for the amplifier group delay.

While this circuit is bipolar, using ±5V supplies, it can easily be adapted to single-supply operation. This configuration adds two real zeroes in the response, transforming this circuit into a bandpass. The frequency response for the filter of Figure 83 is illustrated in Figure 84.

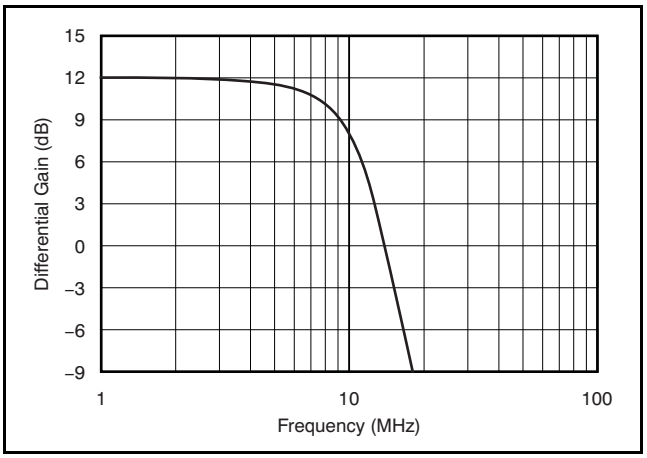


Figure 84. Differential 4th-Order, 10MHz Butterworth Filter

DUAL-CHANNEL, DIFFERENTIAL ADC DRIVER

Where a low-noise, single-supply, interface to a differential input +5V ADC is required, the circuit of Figure 85 can provide a high dynamic range, medium gain interface for dual high-performance ADCs. The circuit of Figure 85 uses two amplifiers in the differential inverting configuration. The common-mode voltage is set on the noninverting inputs to the supply midscale. In this example, the input signal is coupled in through a 1:2 transformer. This design provides both signal gain, single to differential conversion, and a reduction in noise figure. To show a 50Ω input impedance at the input to the transformer, two 200Ω resistors are required on the transformer secondary. These two resistors are also the amplifier gain elements. Because the same dc voltage appears on both inverting nodes in the circuit of Figure 85, no dc current will flow through the transformer, giving a dc gain of 1 to the output for this common-mode voltage, V_{CM}.

The circuit of Figure 85 is particularly suitable for a moderate resolution dual ADC used as I/Q samplers. The optional 500Ω resistors to ground on each amplifier output can be added to improve the 2nd- and 3rd-harmonic distortion by >15dB if higher dynamic range is required.

The 5mA added output stage current significantly improves linearity if that is required. The measured 2nd-harmonic distortion is consistently lower than the 3rd-harmonics for this balanced differential design. It is particularly helpful for this low-power design if there are no grounds in the signal path after the low-level signal at the transformer input. The two pull-down resistors do show a signal path ground and should be connected at the same physical point to ground, in order to eliminate imbalanced ground return currents from degrading 2nd-harmonic distortion.

VIDEO LINE DRIVING

Most video distribution systems are designed with 75Ω series resistors to drive a matched 75Ω cable. In order to deliver a net gain of 1 to the 75Ω matched load, the amplifier is typically set up for a voltage gain of +2V/V, compensating for the 6dB attenuation of the voltage divider formed by the series and shunt 75Ω resistors at either end of the cable.

The circuit of Figure 72 applies to this requirement if all references to 50Ω resistors are replaced by 75Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional dc loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 72 to be reduced from 750Ω to 625Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA4830 provide exceptional results in video distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA4830, with the typical 150Ω load of a single matched video cable, shows less than 0.07%/0.17° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for multiple video signals (see Figure 86).

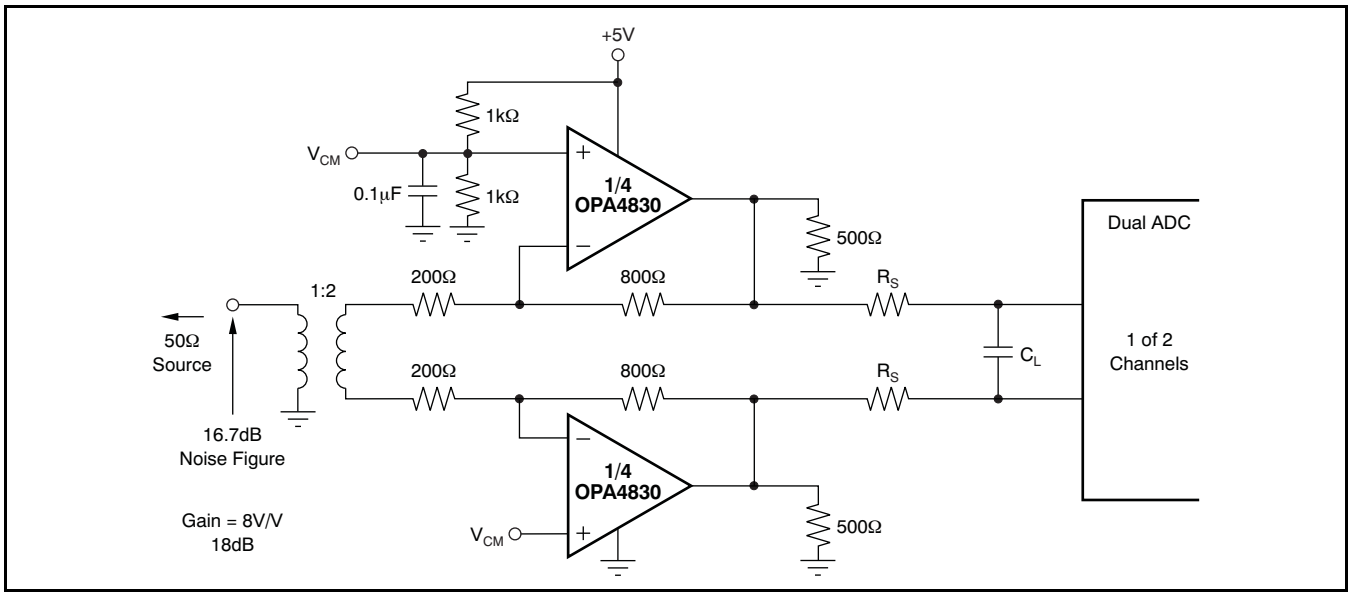


Figure 85. Single-Supply Differential ADC Driver (1 of 2 channels)

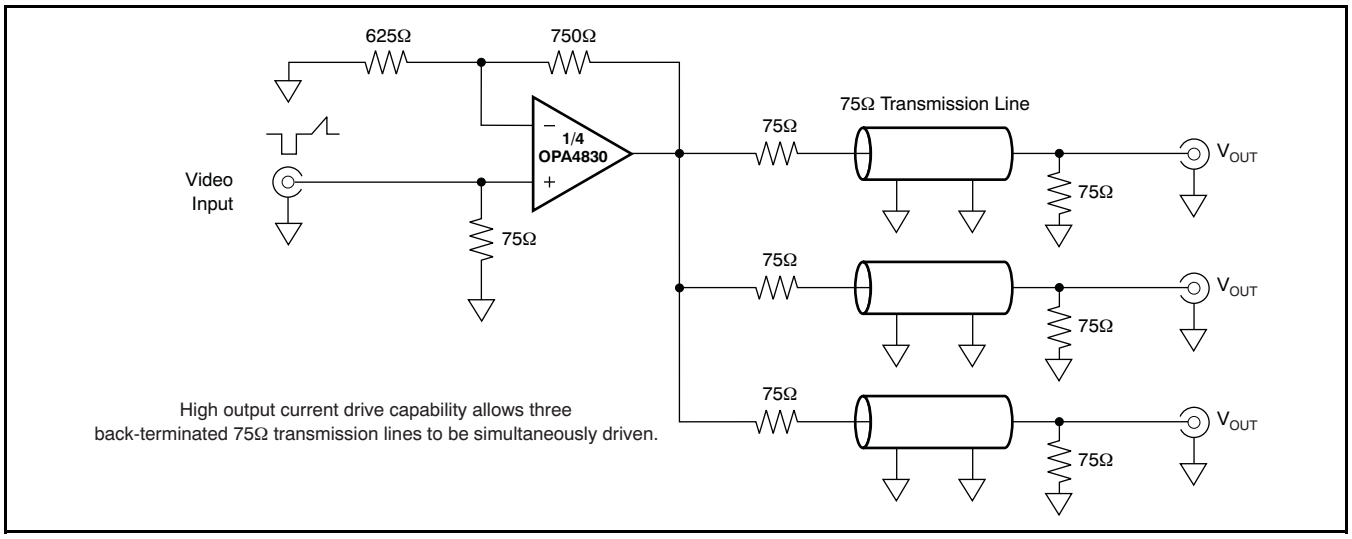


Figure 86. Video Distribution Amplifier

4-CHANNEL DAC TRANSIMPEDANCE AMPLIFIER

High-frequency Digital-to-Analog Converters (DACs) require a low-distortion output amplifier to retain the SFDR performance into real-world loads. Figure 87 illustrates a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground-summing junction of the OPA4830, which is set up as a transimpedance stage or I-V converter. The unused current output of the DAC is connected to ground. If the DAC requires its outputs to be terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the noninverting input of the OPA4830.

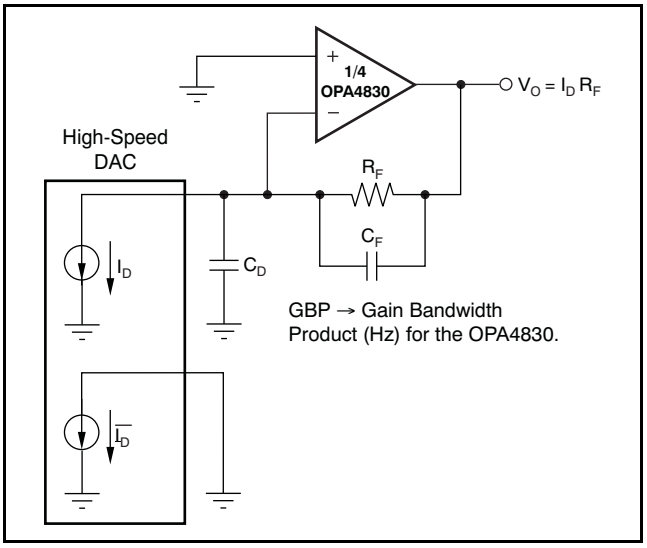


Figure 87. Wideband, Low-Distortion DAC Transimpedance Amplifier

The dc gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D) produces a zero in the noise gain for the OPA4830 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}}$$

which gives a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}}$$

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA4830. The fixture is offered free of charge as unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 2.

Table 2. Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA4830IPW	TSSOP-14	DEM-OPA-TSSOP-4A	SBOU017

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA4830 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA4830 and its circuit designs. This approach is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA4830 is available through the TI web page (www.ti.com). Note that this model is the OPA830 model applied to the OPA4830 quad version. The applications department is also available for design assistance. These models predict typical small-signal ac, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. This model does not attempt to distinguish between the package types in their small-signal ac performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Because the OPA4830 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a direct short.

Below 200Ω, the feedback network presents additional output loading that can degrade the harmonic distortion performance of the OPA4830. Above 1kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 74) to be less than about 400Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G <$ 400Ω keeps this pole above 200MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This increase is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50Ω input matching resistor (= R_G) would require a 100Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 88). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

BANDWIDTH VS GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this calculation only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most amplifiers exhibit a more complex response with lower phase margin. The OPA4830 is compensated to give a slightly peaked response in a noninverting gain of 2V/V (see Figure 74). This compensation results in a typical gain of +2V/V bandwidth of 110MHz, far exceeding that predicted by dividing the 110MHz GBP by 2V/V. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10V/V, the 11MHz bandwidth illustrated in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 110MHz.

Frequency response in a gain of +2V/V may be modified to achieve exceptional flatness simply by increasing the noise gain to 3V/V. One way to do this, without affecting the +2V/V signal gain, is to add a 2.55kΩ resistor across the two inputs (see Figure 78). A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 750Ω feedback resistor along with a 750Ω resistor across the two op amp inputs, the voltage follower response is similar to the gain of +2V/V response of Figure 73. Further reducing the value of the resistor across the op amp inputs further dampens the frequency response because of increased noise gain. The OPA4830 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This minimal reduction is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins changes.

INVERTING AMPLIFIER OPERATION

All of the familiar op amp application circuits are available with the OPA4830 to the designer. See Figure 88 for a typical inverting configuration where the I/O impedances and signal gain from Figure 72 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. It also allows the input to be biased at $V_S/2$ without any headroom issues. The output voltage can be independently moved to be within the output voltage range with coupling capacitors, or bias adjustment resistors.

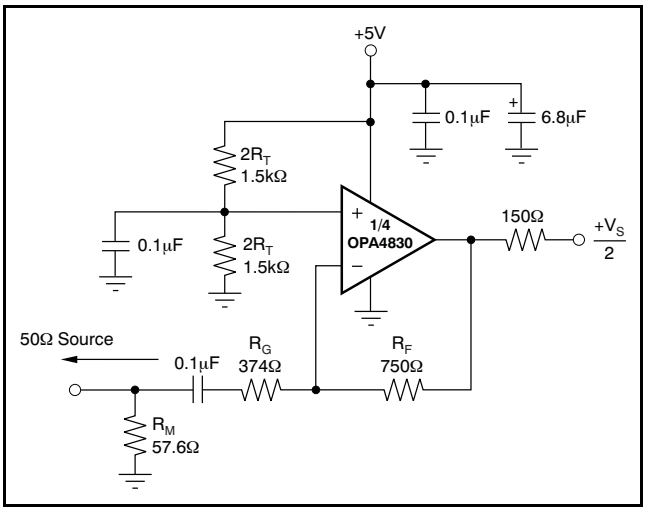


Figure 88. AC-Coupled, G = –2V/V Example Circuit

In the inverting configuration, three key design considerations must be noted. The first consideration is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PCB trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This approach is the simplest and results in optimum bandwidth and noise performance.

However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback resistor. This configuration has the interesting advantage of the noise gain becoming equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered above. The amplifier output now sees the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values, as shown in Figure 88, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and thus influences the bandwidth. For the example in Figure 88, the R_M value combines in parallel with the external 50Ω source impedance (at high frequencies), yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain. The resulting noise gain is 2.87 for Figure 88, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth is therefore lower for the gain of –2 circuit of Figure 88 (NG = +2.87) than for the gain of +2 circuit of Figure 72.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistors on the noninverting input (a parallel combination of R_T = 750Ω). If this resistor is set equal to the total dc resistance looking out of the inverting node, the output dc error (as a result of the input bias currents) is reduced to (input offset current) times R_F. With the dc blocking capacitor in series with R_G, the dc source impedance looking out of the inverting mode is simply R_F = 750Ω for Figure 88. To reduce the additional high-frequency noise introduced by this resistor and power-supply feed-through, R_T is bypassed with a capacitor.

OUTPUT CURRENT AND VOLTAGES

The OPA4830 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup does the output current and voltage decrease to the numbers shown in the specification tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications, because the output stage junction temperatures are higher than the minimum specified operating ambient temperature.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This absence of protection is not normally a problem, because most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages), in most cases, destroys the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This resistor reduces the available output voltage swing under heavy output loads.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA4830 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA4830. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the Board Layout Guidelines section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain also reduces the peaking (see Figure 78).

DISTORTION PERFORMANCE

The OPA4830 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 74) this is sum of $R_F + R_G$, while in the inverting configuration, only R_F needs to be included in parallel with the actual load. Running differential suppresses the 2nd-harmonic, as shown in the Differential Typical Characteristics.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA4830 however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.8pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 89 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

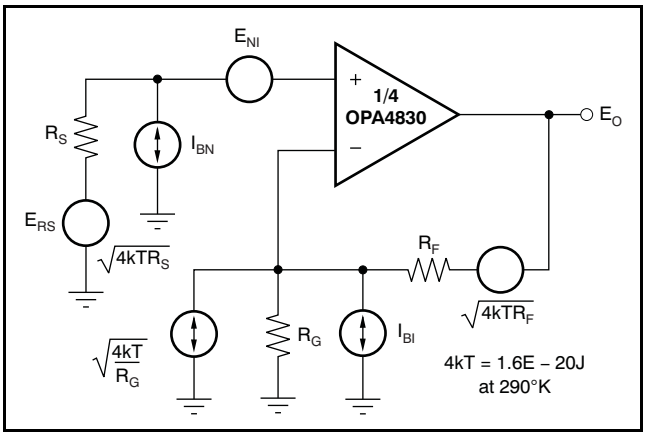


Figure 89. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 8 shows the general form for the output noise voltage using the terms shown in Figure 89:

$$E_O = \sqrt{(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (8)$$

Dividing this expression by the noise gain [NG = (1 + R_F/R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input; this result is shown in Equation 9:

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (9)$$

Evaluating these two equations for the circuit and component values shown in Figure 72 gives a total output spot noise voltage of 19.3nV/√Hz and a total equivalent input spot noise voltage of 9.65nV/√Hz. This value is including the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/√Hz specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA4830 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5μA out of each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. This reduction is achieved by matching the dc source resistances appearing at the two inputs. Evaluating the configuration of Figure 74 (which has matched dc input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to Equation 10:

(NG = noninverting signal gain at dc)
$\pm(NG \times V_{OS(MAX)}) + (R_F \times I_{OS(MAX)})$
$= \pm(2 \times 8mV) \times (375\Omega \times 1.1\mu A)$
$= \pm 16.41mV$ (10)

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques are based on adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the dc offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This configuration ensures that the adjustment circuit has minimal effect on the loop gain and therefore the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature sets the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; though, for resistive loads connected to mid-supply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(16 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA4830 (TSSOP-14 package) in the circuit of Figure 72 operating at the maximum specified ambient temperature of +85°C and driving a 150Ω load at mid-supply.

$P_D = 5V \times 19mA + 4 \times 5^2/(4 \times (150\Omega \parallel 750\Omega)) = 295mW$

Maximum $T_J = +85°C + (0.295W \times 95°C/W) = +113°C$

Although this value is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation occurs if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA4830 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 750Ω feedback used in the Typical Characteristics is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve Recommended R_S vs Capacitive Load (Figure 15, Figure 38, or Figure 63). Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA4830 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA4830 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve Recommended R_S vs Capacitive Load (Figure 15, Figure 38, or Figure 63). This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA4830 directly onto the board.

INPUT AND ESD PROTECTION

The OPA4830 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 90.

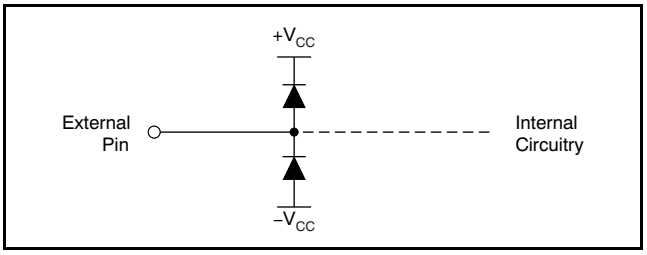


Figure 90. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA4830), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

Revision History

Changes from Original (December 2006) to Revision A	Page
• Changed rating for storage temperature range in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4830IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4830	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

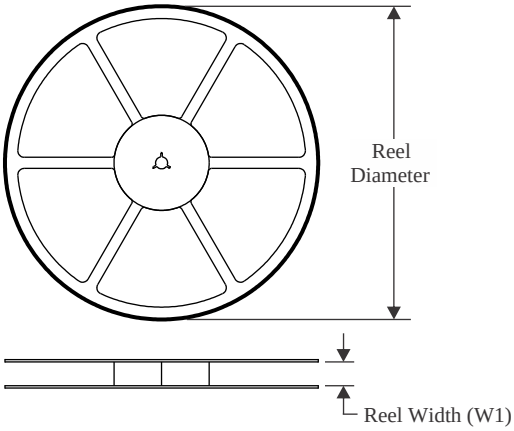
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

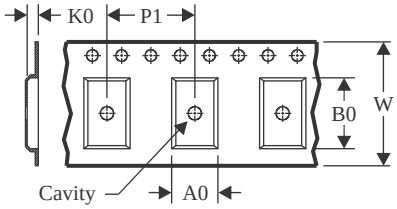
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

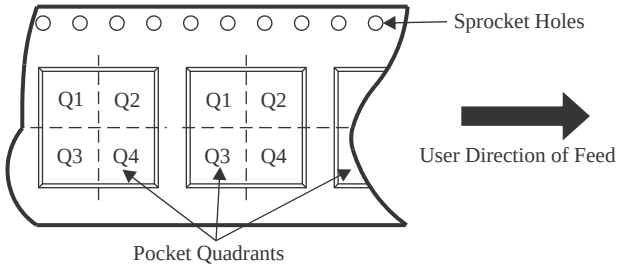


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

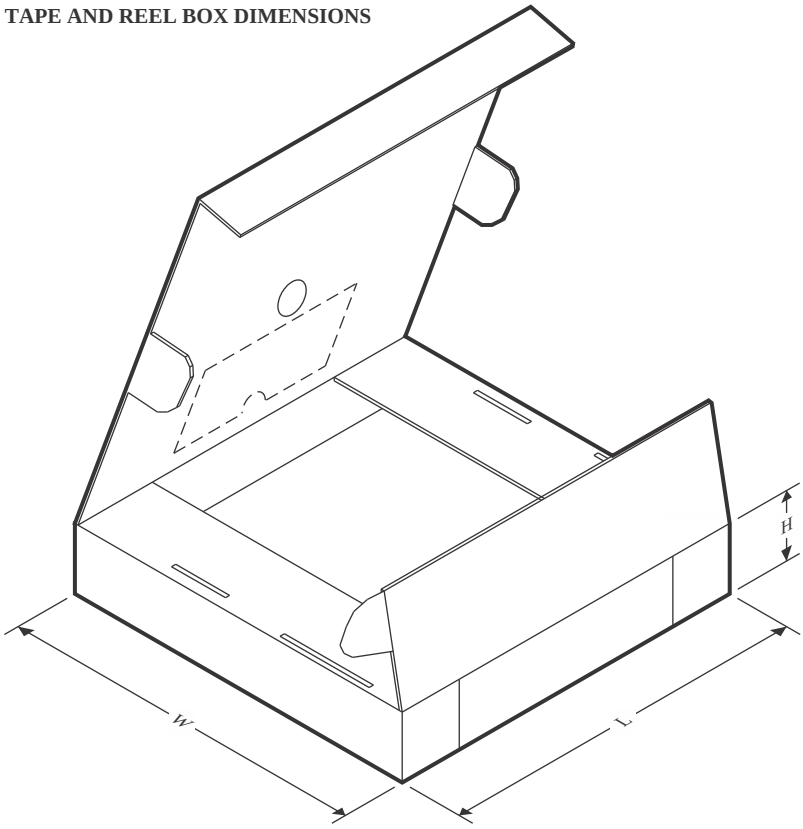
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4830IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

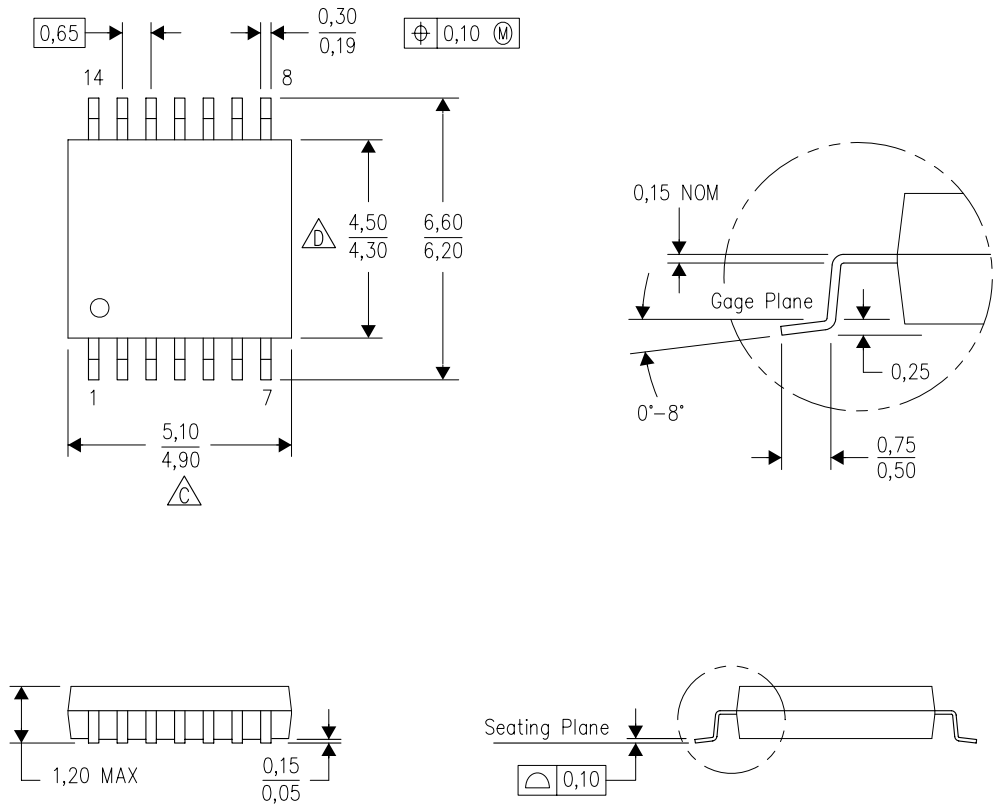
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4830IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265