SN6505A-Q1, SN6505B-Q1, SN6505D-Q1
JAJSGH0D – NOVEMBER 2018 – REVISED OCTOBER 2020

SN6505x-Q1 絶縁電源用の低ノイズ、1A 変圧器ドライバ

1 特長

- 車載アプリケーション用に AEC-Q100 (グレード 1) 認定済み
  - デバイス温度グレード 1:-40℃～+125℃、T_A
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能:SN6505A-Q1、SN6505B-Q1、SN6505D-Q1
- トランス用のプッシュプル・ドライバ
- 広い入力電圧範囲:2.25V～5.5V
- 高い出力駆動能力:5V 電源で 1A
- 低い R_{ON}:4.5V 電源で最大値 0.25Ω
- 伝導および放射 EMI の低減
- 拡散スペクトラムによるクロック供給
- 高精度内部発振器のオプション:160kHz (SN6505A-Q1) および 420kHz (SN6505B-Q1 および SN6505D-Q1)
- 外部クロック入力により複数のデバイスを同期
- スルー・レート制御
- 1.7A の電流制限
- 低シャットダウン電流:1μA 未満
- サーマル・シャットダウン
- 小型の 6 ピン SOT23 (DBV) パッケージ
- ソフトスタート・イネーブル (SN6505A-Q1 および SN6505B-Q1) により突入電流を低減、ソフトスタート・ディセーブル (SN6505D-Q1) により高速にスタートアップ

2 アプリケーション

- 次の用途の絶縁電源
  - トラクション・インバータおよびモーター制御
  - DC/DC コンバータ
  - バッテリ管理システム (BMS)
  - オンボード・チャージャ (OBC)

3 概要

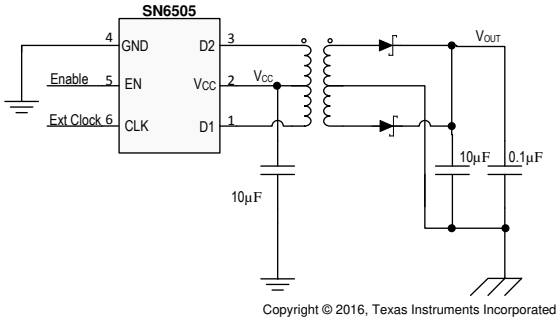
SN6505x-Q1 は低ノイズ、低 EMI のプッシュプル変圧器ドライバで、小型の絶縁電源に特化して設計されています。低背のセンター・タップ付き変圧器を 2.25V～5V の DC 電源で駆動できます。

出力スイッチ電圧のスルー・レート制御と、スペクトラム拡散クロック (SSC) により、きわめて低いノイズと EMI を実現しています。SN6505x-Q1 は、発振器と、それに続くゲート・ドライブ回路とで構成され、ゲート・ドライブ回路はグランドを基準とする N チャネル電源スイッチを駆動するための補完出力信号を供給します。このデバイスには、重負荷時のスタートアップを保証するため、2 つの 1A パワー MOSFET スイッチが内蔵されています。スイッチャの高調波を正しく配置するため、または複数の変圧器ドライバを使用して動作する場合に、スイッチング・クロックを外部から供給することもできます。内部保護機能として、1.7A の電流制限、低電圧誤動作防止、サーマル・シャットダウン、Break-Before-Make 回路が搭載されています。SN6505A-Q1 と SN6505B-Q1 にはソフトスタート機能が搭載されており、大きな負荷コンデンサを使用しているときに過大な突入電流の発生を防止します。高速な出力スタートアップを必要とするアプリケーション向けに、SN6505D-Q1 ではソフトスタート機能が無効になっています。SN6505A-Q1 には、放射の最小化を必要とするアプリケーション向けに 160kHz の内部発振器が搭載されています。これに対して、SN6505B-Q1 と SN6505D-Q1 には、高効率とサイズの小さい変圧器を必要とするアプリケーション向けに 420kHz の内部発振器が搭載されています。SN6505x-Q1 は、小型の 6 ピン SOT23/DBV パッケージで供給されます。このデバイスは、-40℃～125℃の温度範囲で動作が特性付けされています。

製品情報

部品番号 (1)	パッケージ	本体サイズ (公称)
SN6505A-Q1	SOT23 (6 ピン)	2.90mm × 1.60mm
SN6505B-Q1		
SN6505D-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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簡略回路図

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics, SN6505A-Q1 ... 7
6.8 Typical Characteristics, SN6505B-Q1 or SN6505D-Q1 ... 9
7 Parameter Measurement Information ... 13
8 Detailed Description ... 15
8.1 Overview ... 15
8.2 Functional Block Diagram ... 15
8.3 Feature Description ... 15
8.4 Device Functional Modes ... 17
9 Application and Implementation ... 18
9.1 Application Information ... 18
9.2 Typical Application ... 19
10 Power Supply Recommendations ... 29
11 Layout ... 30
11.1 Layout Guidelines ... 30
11.2 Layout Example ... 30
12 Device and Documentation Support ... 31
12.1 Device Support ... 31
12.2 Documentation Support ... 31
12.3 Related Links ... 31
12.4 ドキュメントの更新通知を受け取る方法 ... 31
12.5 サポート・リソース ... 31
12.6 Trademarks ... 31
12.7 静電気放電に関する注意事項 ... 31
12.8 用語集 ... 32
13 Mechanical, Packaging, and Orderable Information ... 32

4 Revision History

Changes from Revision C (August 2019) to Revision D (October 2020) — **Page**

- 機能安全の箇条書き項目を追加 ... 1

Changes from Revision B (July 2019) to Revision C (August 2019) — **Page**

- Added UNIT V to EN, CLK Voltage specification in **Absolute Maximum Ratings** table ... 4
- Changed '<' or 'less than' sign to '≤' or 'less than or equal' sign in V_{CC} range description at multiple location for better clarity ... 5
- Added **Revision History** comments for data sheet Revision B ... 6
- Added 'Power up time' or t_{PWRUP} specification for two V_{CC} TEST CONDITIONS ... 6

Changes from Revision A (April 2019) to Revision B (July 2019) — **Page**

- Split 'Soft-start time' or t_{SS} specification for SN6505A-Q1 and SN6505B-Q1 ... 6

Changes from Revision * (November 2018) to Revision A (April 2019) — **Page**

- デバイスのステータスを「量産データ」に変更 ... 1
- Added DA2303-AL transformer to 表 9-3 table ... 25
- Added DA2304-AL transformer to 表 9-3 table ... 25

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5 Pin Configuration and Functions

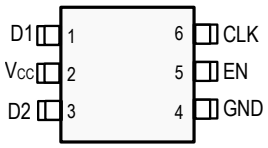

図 5-1. DBV Package SOT-23 (6 Pin) Top View

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
D1	1	O	Open drain output of the first power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
V_{CC}	2	P	This is the device supply pin. It should be bypassed with a 4.7 µF or greater, low ESR capacitor. When $V_{CC} \leq 2.25$ V, an internal undervoltage lockout circuit trips and turns both outputs off.
D2	3	O	Open drain output of the second power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
GND	4	P	GND is connected to the source of the power MOSFET switches via an internal sense circuit. Because large currents flow through it, the GND terminals must be connected to a low-inductance quality ground plane.
EN	5	I	The EN pin turns the device on or off. Grounding or leaving this pin floating disables all internal circuitry. If unused this pin should be tied directly to V_{CC}.
CLK	6	I	This pin is used to run the device with external clock. Internally it is pulled down to GND. If valid clock is not detected on this pin, the device shifts automatically to internal clock.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1). All typical values are at T_A = 25°C, V_{CC} = 5 V.

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC}	–0.5	6	V
Voltage	EN, CLK	–0.5	V_{CC} + 0.5(3)	V
Output switch voltage	D1, D2		16	V
Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$		2.4	A
Junction temperature, T_J		-40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *セクション 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND) and are peak voltage values.
(3) Maximum voltage must not exceed 6V. A strongly driven EN or CLK input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 3A	±6000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.25		5.5	V
I_{D1}, I_{D2}	Output switch current - Primary side	2.25 V ≤ V_{CC} ≤ 2.8 V			0.75	A
		2.8 V < V_{CC} ≤ 5.5 V			1	
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN6505x-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over full-range of recommended operating conditions, unless otherwise noted. All typical values are at T_A = 25°C, V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE SUPPLY						
$I_{(Vcc)}$	Supply Current (2.8 V ≤ V_{CC} ≤ 5.5 V) (SN6505A-Q1)	R_L = 50 Ω		1	1.4	mA
	Supply Current (2.8 V ≤ V_{CC} ≤ 5.5 V) (SN6505B-Q1 and SN6505D-Q1)	R_L = 50 Ω		1.56	2.3	mA
I_{IH}	Leakage Current on EN and CLK pin	EN / CLK = V_{CC}		10	20	µA
I_{DIS}	V_{CC} current for EN = 0			0.1		µA
$I_{LKG(D1)}$ $I_{LKG(D2)}$	Leakage Current on D1, D2 for EN=0	Voltage of D1, D2 = V_{CC}		0.1		µA
$V_{CC+ (UVLO)}$	Positive-going UVLO threshold				2.25	V
$V_{CC- (UVLO)}$	Negative-going UVLO threshold		1.7			V
$V_{HYS (UVLO1)}$	UVLO threshold hysteresis			0.3		V
$V_{IN(ON)}$	EN, CLK pin logic high threshold				0.7	V_{CC}
$V_{IN(OFF)}$	EN, CLK pin logic low threshold		0.3			V_{CC}
$V_{IN(HYS)}$	EN, CLK pin threshold hysteresis			0.2		V_{CC}
CLK						
F_{SW}	D1, D2 average switching Frequency (SN6505A-Q1)	R_L = 50 Ω to V_{CC}; Refer to 図 7-3	138	160	203	Khz
	D1, D2 average switching Frequency (SN6505B-Q1 and SN6505D-Q1)	R_L = 50 Ω to V_{CC}; Refer to 図 7-3.	363	424	517	kHz
$F_{(EXT)}$	External clock frequency on CLK pin (SN6505A-Q1)		100		600	kHz
	External clock frequency on CLK pin (SN6505B-Q1 and SN6505D-Q1)		100		1600	kHz
OUTPUT STAGE						
DMM	Average ON time mismatch between D1 and D2	R_L = 50 Ω		0%		
$R_{(ON)}$	Output switch on resistance	V_{CC} = 4.5 V, I_{D1}, I_{D2} = 1 A		0.16	0.25	Ω
		V_{CC} = 2.8 V, I_{D1}, I_{D2} = 1 A		0.19	0.31	Ω
		V_{CC} = 2.25 V, I_{D1}, I_{D2} = 0.5 A		0.21	0.45	Ω
$V_{(SLEW)}$	Voltage slew rates on D1 and D2 for SN6505A-Q1	R_L = 50 Ω to V_{CC}; Refer to 図 7-3		48		V/µs
$I_{(SLEW)}$	Current slew rates at D1 and D2 for SN6505A-Q1	R_L = 5 Ω through transformer; Refer to 図 7-4		11		A/µs
$V_{(SLEWHF)}$	Voltage slew rates on D1 and D2 for SN6505B-Q1 and SN6505D-Q1	R_L = 50 Ω to V_{CC}; Refer to 図 7-3		152		V/µs
$I_{(SLEWHF)}$	Current slew rates at D1 and D2 for SN6505B-Q1 and SN6505D-Q1	R_L = 5 Ω through transformer; Refer to 図 7-4		41		A/µs
I_{LIM}	Current clamp limit (2.8 V < V_{CC} ≤ 5.5V)		1.42	1.75	2.15	A
	Current clamp limit (2.25 V ≤ V_{CC} ≤ 2.8 V)		0.65		1.85	A
THERMAL SHUT DOWN						
T_{SD+}	T_{SD} turn on temperature		154	168	181	°C
T_{SD-}	T_{SD} turn off temperature		135	150	166	°C
T_{SD-}	T_{SD} hysteresis		13	17		°C

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6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
CLK						
$t_{CLKTIMER}$	Duration after which device switches to internal clock in case of invalid external clock		10		25	µs
OUTPUT STAGE						
t_{BBM}	Break-before-make time(SN6505A-Q1)	Measured as voltage with R_L = 50 Ω to V_{CC}, Refer to 図 7-3		115		ns
	Break-before-make time (SN6505B-Q1 and SN6505D-Q1)	Measured as voltage with R_L = 50 Ω to V_{CC}, Refer to 図 7-3		90		ns
SOFT-START ENABLED (SN6505A-Q1 AND SN6505B-Q1)						
t_{SS}	Soft-start time (SN6505A-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40 µF R_L = 5 Ω	1	2.2	8	ms
	Soft-start time (SN6505B-Q1)	10% to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40 µF R_L = 5 Ω	1	4.25	8	ms
$t_{SSdelay}$	Soft-start time delay	From power up to 90% transition time on V_{OUT} With transformer C_{LOAD} = 40 µF R_L = 5 Ω	3.5	8.5	18	ms
SOFT-START DISABLED (SN6505D-Q1)						
t_{PWRUP}	Power up time	From EN=1 to full drive-current available at D1 and D2; 2.25 V ≤ V_{CC} < 3 V		75	160	µs
		From EN=1 to full drive-current available at D1 and D2; 3 V ≤ V_{CC} ≤ 5.5 V		60	100	µs
t_{PWRDN}	Power down time	From EN=0 to output MOSFETs off (no current on D1 and D2)		1	5	µs

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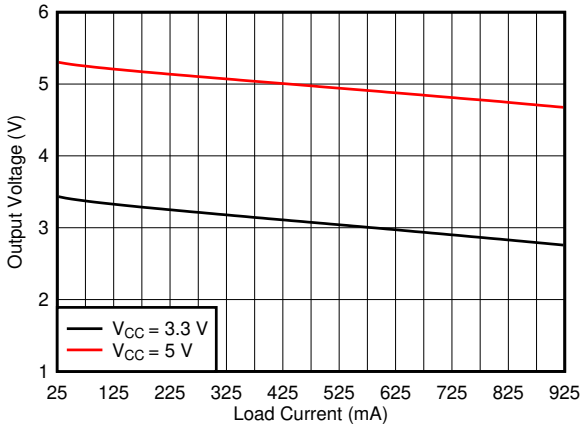
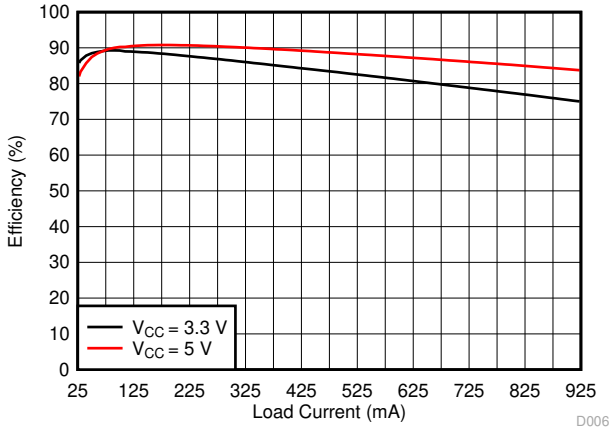
6.7 Typical Characteristics, SN6505A-Q1



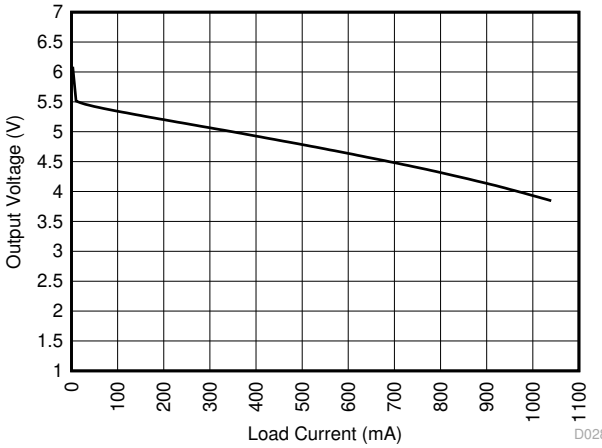
SN6505A-Q1 + Wurth 750315240

図 6-1. Output Voltage vs Load Current



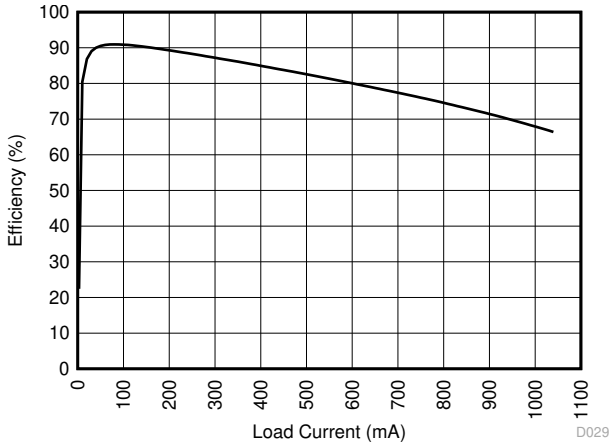
SN6505A-Q1 + Wurth 750315240

図 6-2. Efficiency vs Load Current



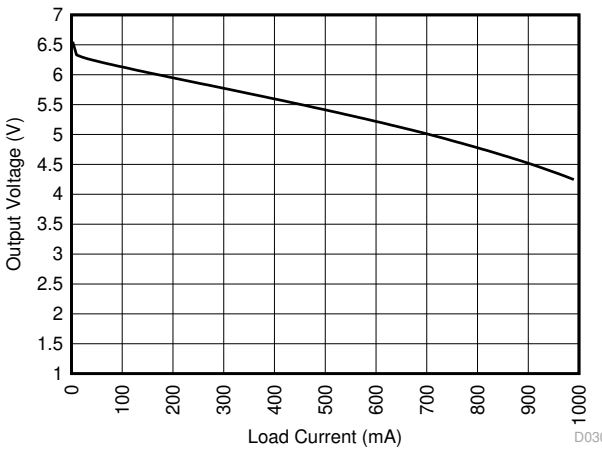
SN6505A-Q1 + Wurth 750316031 V_{CC} = 3.3 V

図 6-3. Output Voltage vs Load Current



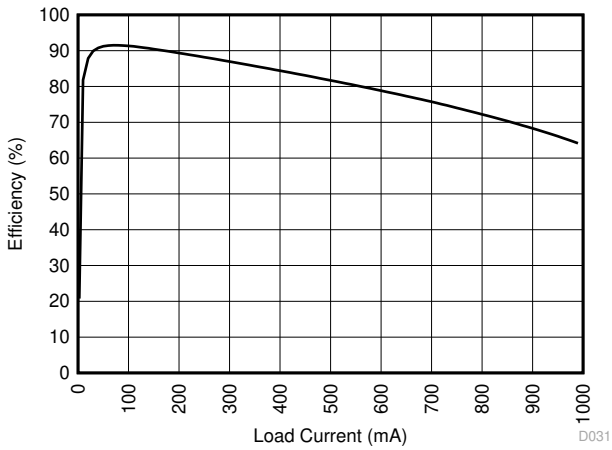
SN6505A-Q1 + Wurth 750316031 V_{CC} = 3.3 V

図 6-4. Efficiency vs Load Current



SN6505A-Q1 + Wurth 750316032 V_{CC} = 3.3 V

図 6-5. Output Voltage vs Load Current



SN6505A-Q1 + Wurth 750316032 V_{CC} = 3.3 V

図 6-6. Efficiency vs Load Current

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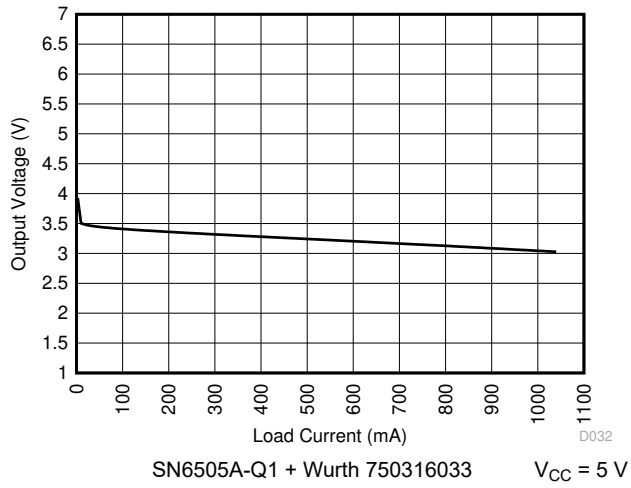

図 6-7. Output Voltage vs Load Current

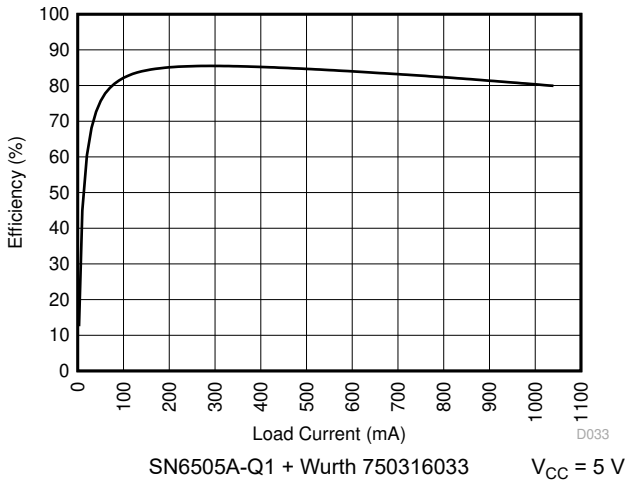

図 6-8. Efficiency vs Load Current

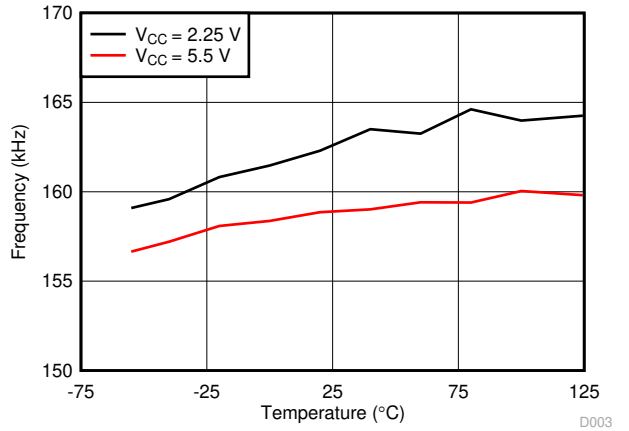

図 6-9. Frequency vs Free-Air Temperature

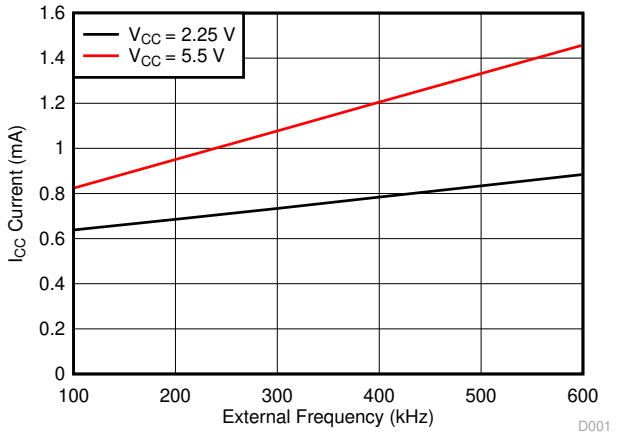

図 6-10. Current vs External Frequency

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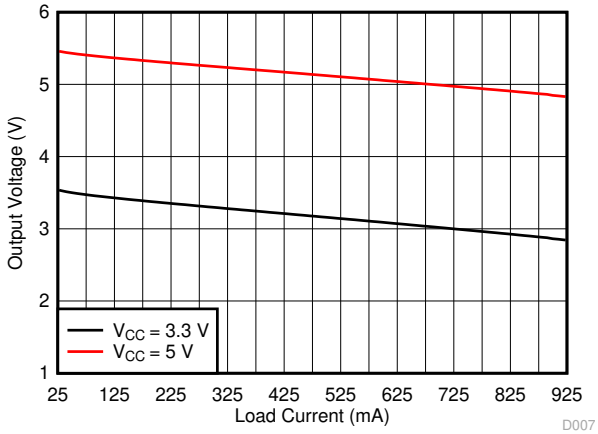
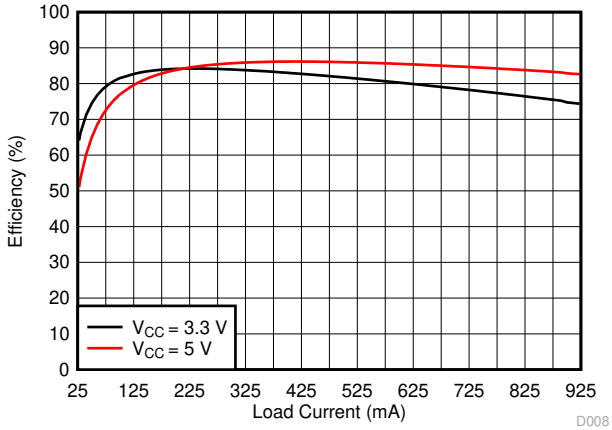
6.8 Typical Characteristics, SN6505B-Q1 or SN6505D-Q1



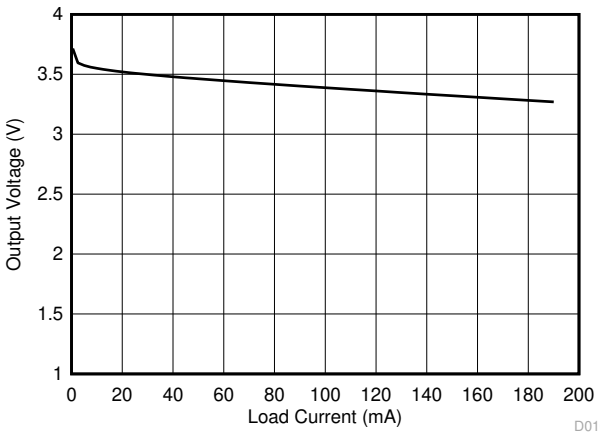
SN6505B/D-Q1 + Wurth 750315371

図 6-11. Output Voltage vs Load Current



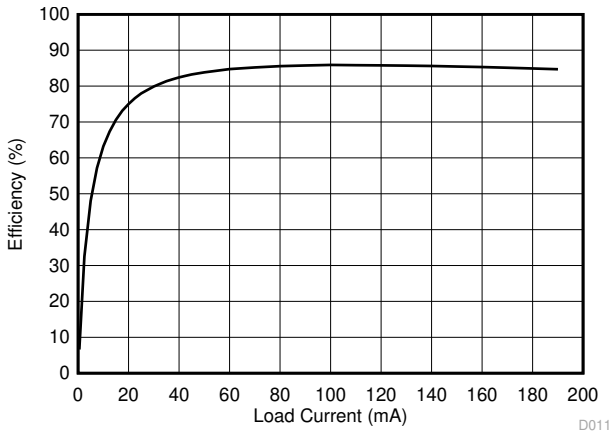
SN6505B/D-Q1 + Wurth 750315371

図 6-12. Efficiency vs Load Current



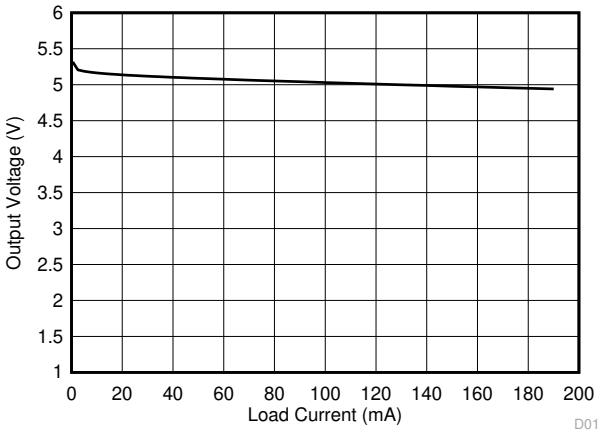
SN6505B/D-Q1 + Wurth 760390011 V_{CC} = 3.3 V

図 6-13. Output Voltage vs Load Current



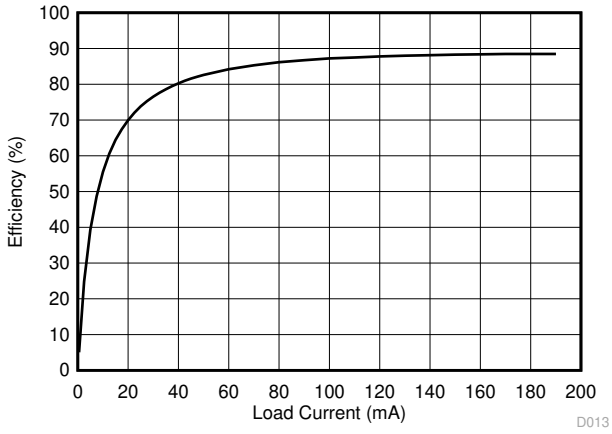
SN6505B/D-Q1 + Wurth 760390011 V_{CC} = 3.3 V

図 6-14. Efficiency vs Load Current



SN6505B/D-Q1 + Wurth 760390012 V_{CC} = 5 V

図 6-15. Output Voltage vs Load Current



SN6505B/D-Q1 + Wurth 760390012 V_{CC} = 5 V

図 6-16. Efficiency vs Load Current

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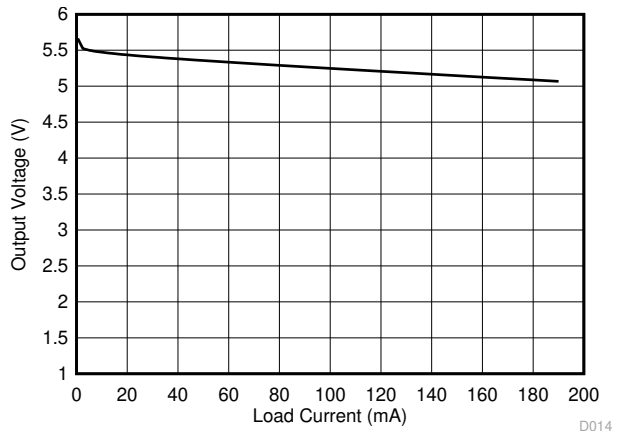
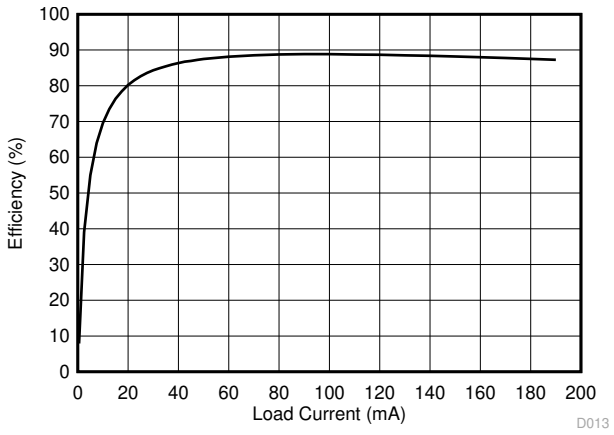


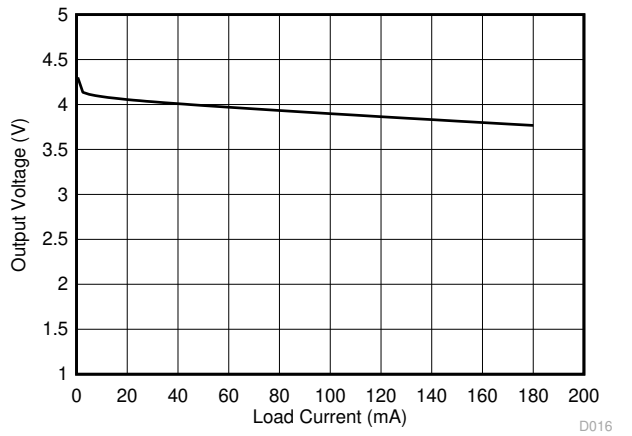
SN6505B/D-Q1 + Wurth 760390013 V_{CC} = 3.3 V

図 6-17. Output Voltage vs Load Current



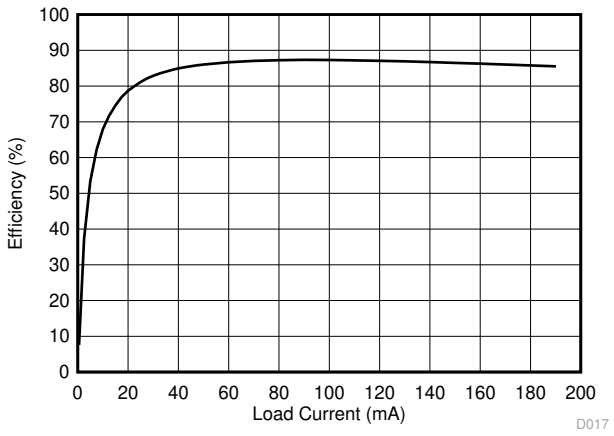
SN6505B/D-Q1 + Wurth 760390013 V_{CC} = 3.3 V

図 6-18. Efficiency vs Load Current



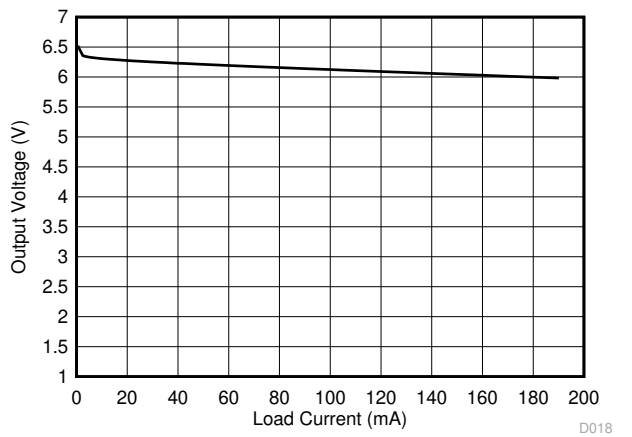
SN6505B/D-Q1 + Wurth 760390014 V_{CC} = 3.3 V

図 6-19. Output Voltage vs Load Current



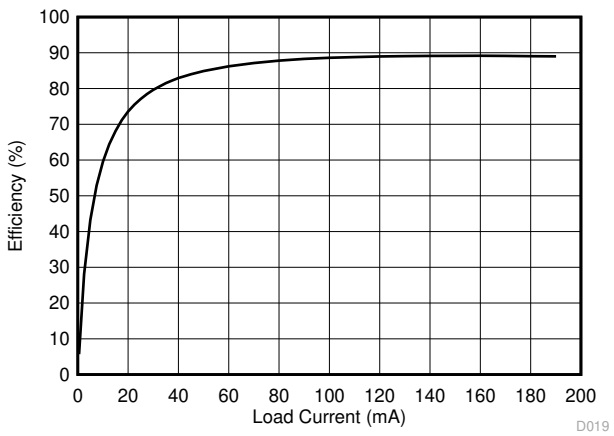
SN6505B/D-Q1 + Wurth 760390014 V_{CC} = 3.3 V

図 6-20. Efficiency vs Load Current



SN6505B/D-Q1 + Wurth 760390014 V_{CC} = 5 V

図 6-21. Output Voltage vs Load Current



SN6505B/D-Q1 + Wurth 760390014 V_{CC} = 5 V

図 6-22. Efficiency vs Load Current

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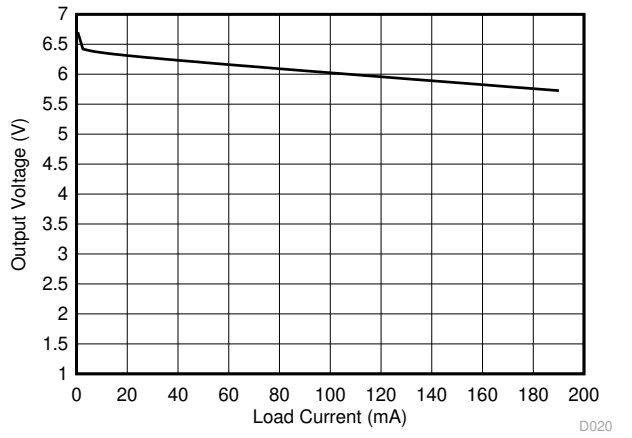
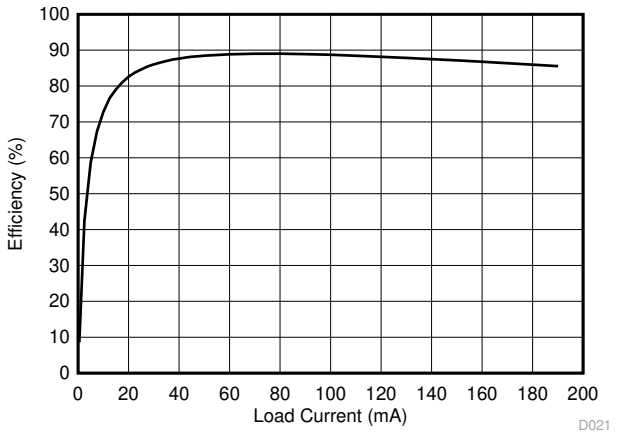


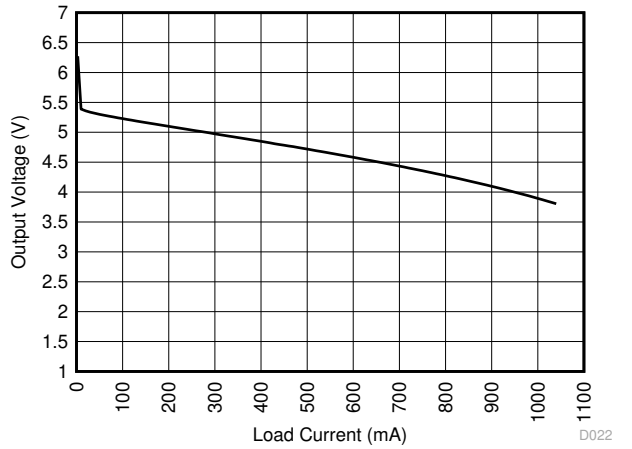
SN6505B/D-Q1 + Wurth 760390015 V_{CC} = 3.3 V

図 6-23. Output Voltage vs Load Current



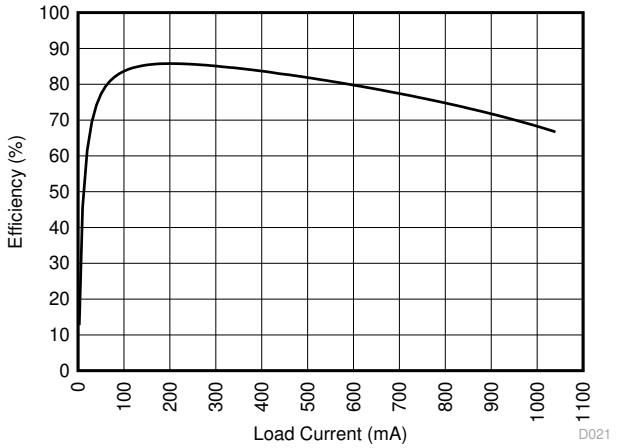
SN6505B/D-Q1 + Wurth 760390015 V_{CC} = 3.3 V

図 6-24. Efficiency vs Load Current



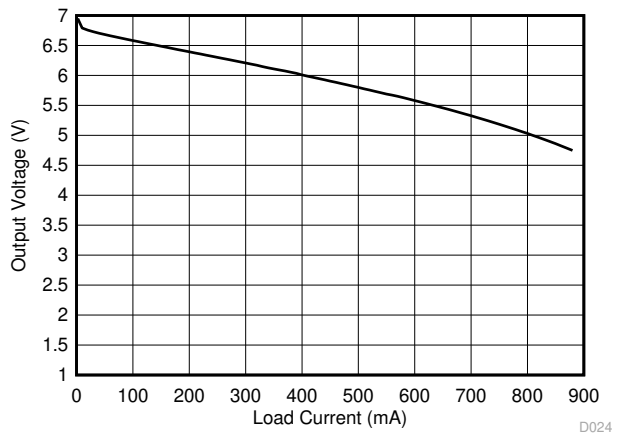
SN6505B/D-Q1 + Wurth 750316028 V_{CC} = 3.3 V

図 6-25. Output Voltage vs Load Current



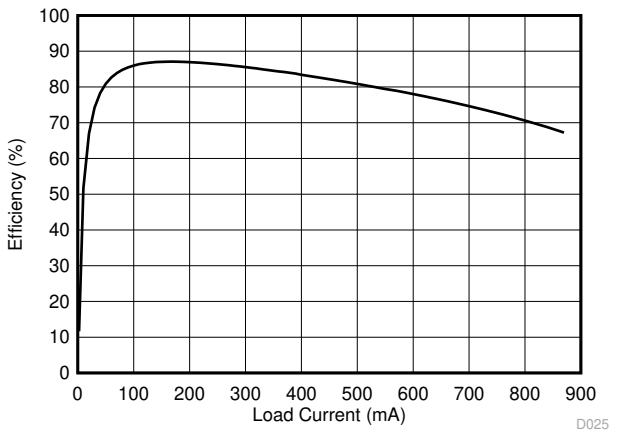
SN6505B/D-Q1 + Wurth 750316028 V_{CC} = 3.3 V

図 6-26. Efficiency vs Load Current



SN6505B/D-Q1 + Wurth 750316029 V_{CC} = 3.3 V

図 6-27. Output Voltage vs Load Current



SN6505B/D-Q1 + Wurth 750316029 V_{CC} = 3.3 V

図 6-28. Efficiency vs Load Current

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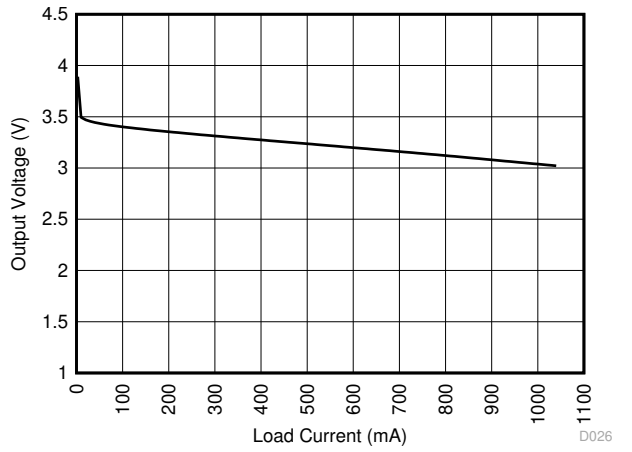

図 6-29. Output Voltage vs Load Current

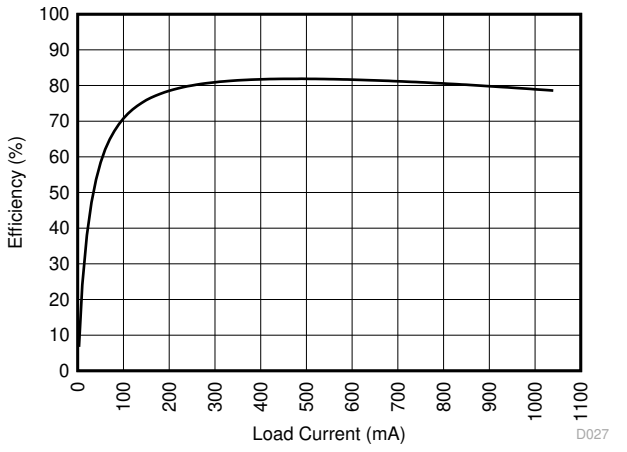

図 6-30. Efficiency vs Load Current

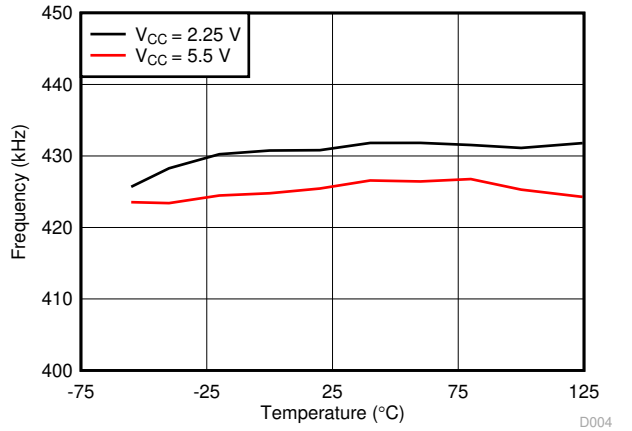

図 6-31. Frequency vs Free-Air Temperature

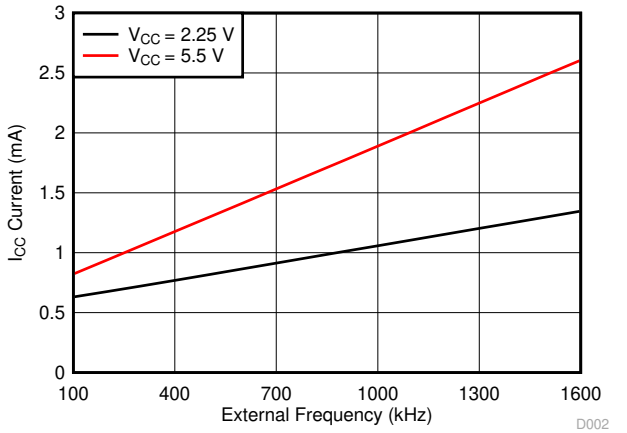

図 6-32. Current vs External Frequency

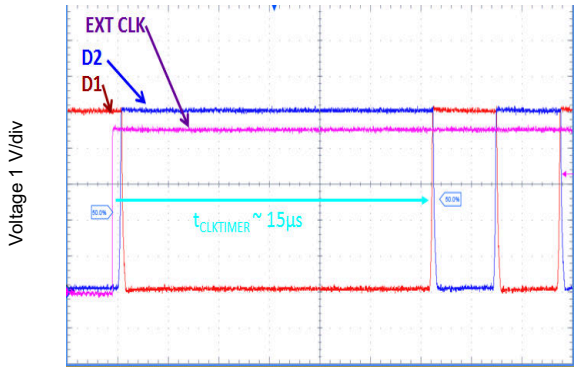

図 6-33. Scope Capture of SN6505 Switching from External to Internal Clock

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7 Parameter Measurement Information

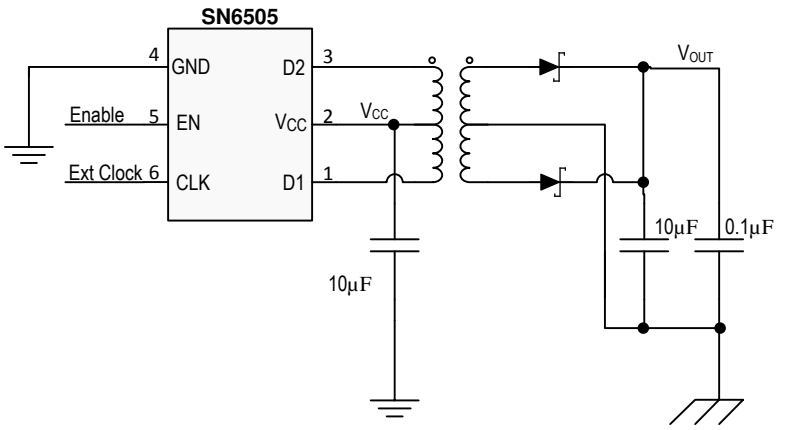

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図 7-1. Measurement Circuit for Unregulated Output (TP1)

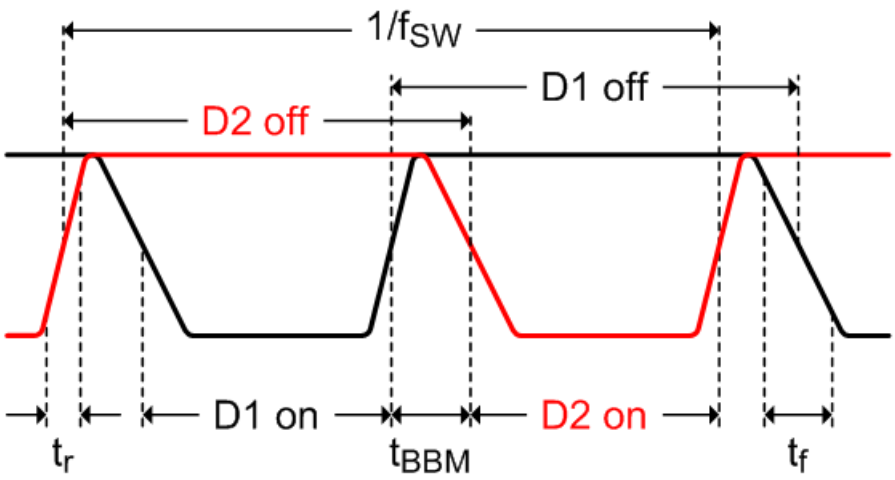

図 7-2. Timing Diagram

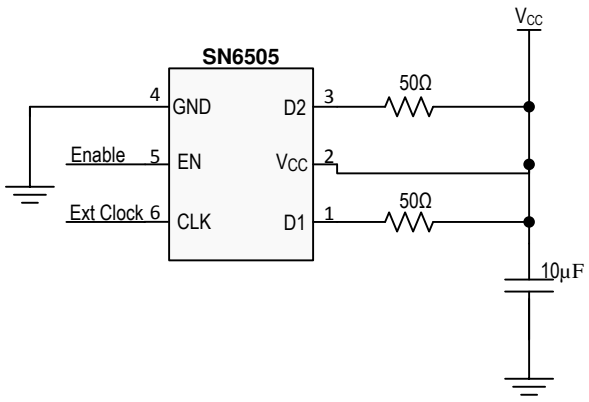

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図 7-3. Test Circuit for F_{SW}, $V_{(slew)}$, t_{BBM}

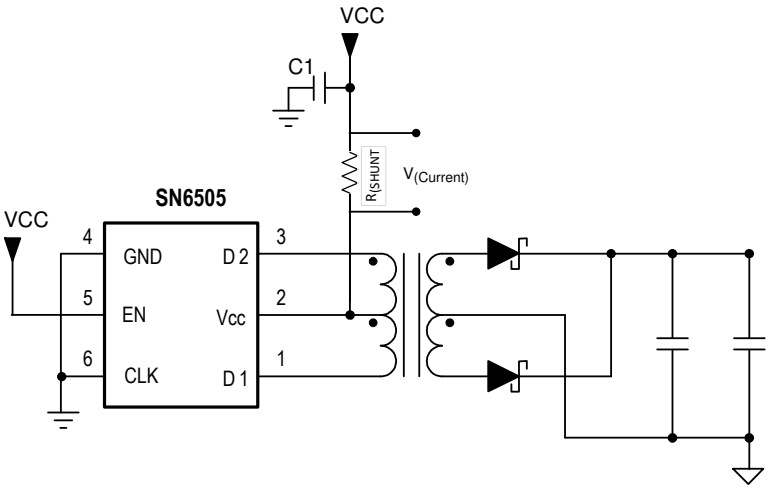

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図 7-4. $I_{(slew)}$ Test Setup

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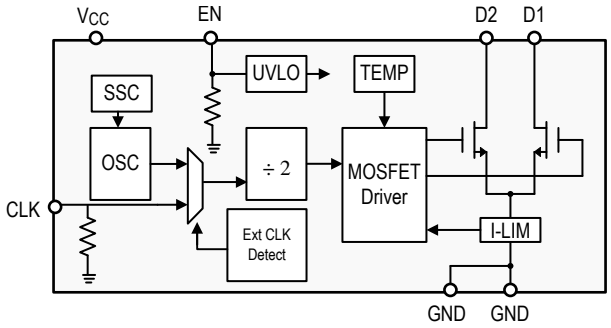
8 Detailed Description

8.1 Overview

The SN6505x-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

The output frequency of the oscillator is divided down by two . A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. Before either one of the gates can assume logic high, the BBM logic ensures a short time period during which both signals are low and both transistors are high-impedance. This short period, is required to avoid shorting out both ends of the primary. The resulting output signals, present the gate-drive signals for the output transistors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see 図 8-1).

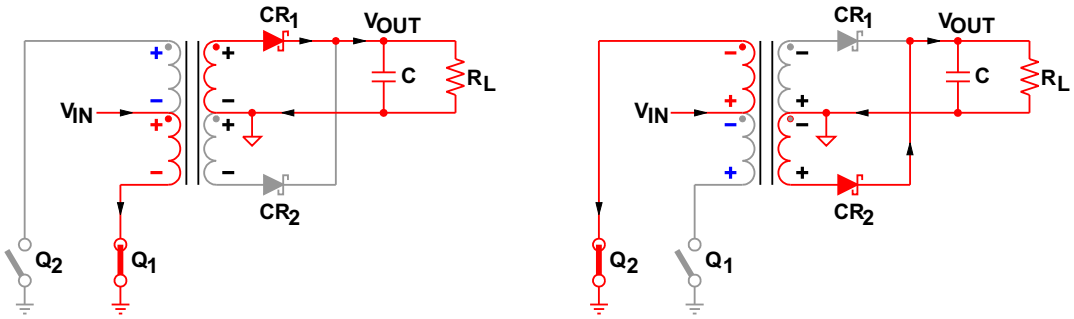


図 8-1. Switching Cycles of a Push-Pull Converter

When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

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When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2 \times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

8.3.2 Core Magnetization

図 8-2 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A', and when Q_2 conducts the flux is pulled back from A' to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, it is applied to the primary: $B \approx V_P \times t_{ON}$.

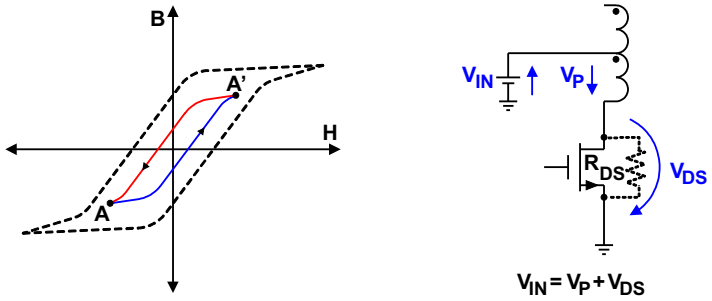

図 8-2. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

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8.4 Device Functional Modes

The functional modes of the device are divided into start-up, operating, and off-mode.

8.4.1 Start-Up Mode

When the supply voltage at V_{CC} ramps up to 2.25 V , the internal oscillator starts operating . The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached its full maximum yet.

8.4.1.1 Soft-Start

SN6505A-Q1 and SN6505B-Q1 devices support soft-start feature. Upon power up or when EN pin transitions from Low to High, the gate drive of the output power-MOSFET is gradually increased over a period of time from 0 V to V_{CC}. Soft-start prevents high inrush current from V_{CC} while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up. For applications that need quick power-up, the SN6505D-Q1, that has soft-start disabled, can be used.

8.4.2 Operating Mode

When the device supply has reached its nominal value ±10% the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

8.4.3 Shutdown-Mode

The device has a dedicated enable pin to put the device in very low power mode to save power when not in use. Enable pin has an internal pull down resistor which keeps device disabled when not driven. When disabled or when V_{CC} is < 1.7 V , both drain outputs, D1 and D2, are tri-stated.

8.4.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. SN6505 addresses this by modulating its internal clock in such a way that the emitting energy is spread over multiple frequency bins. This Spread Spectrum clocking feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

8.4.5 External Clock Mode

The SN6505x-Q1 has a CLK pin which can be used to synchronize the device with system clock and in turn with other SN6505x-Q1 devices so that the system can control the exact switching frequency of the device. The Rising edge of the CLK is used to divide a clock by two and used to drive the gates. 図 9-2 shows the timing diagram for the same. The device also has external clock fail safe feature which automatically switches the device to the internal clock if a valid input clock is not present for long ($t_{CLKTIMER}$). The in-built emissions reduction scheme of Spread Spectrum clocking is disabled when external clock is present.

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9 Application and Implementation

注

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9.1 Application Information

The SN6505x-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters using the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

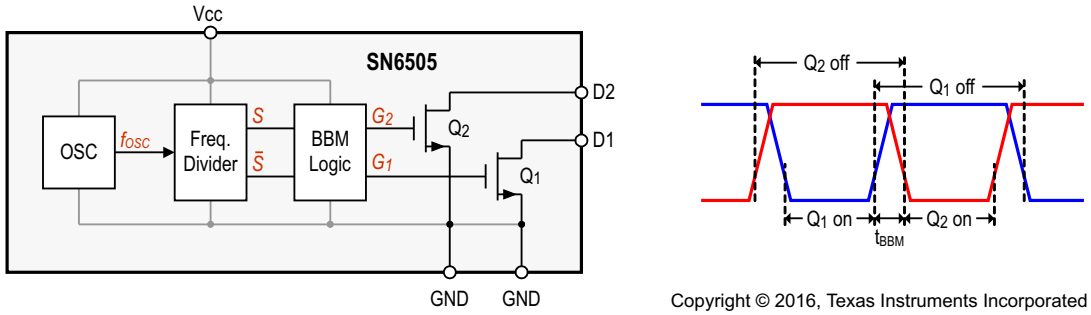

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図 9-1. Block Diagram and Output Timing With Break-Before-Make Action

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and $\overline{S}$, with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, G_1 and G_2, present the gate-drive signals for the output transistors Q_1 and Q_2. As shown in 図 9-2, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

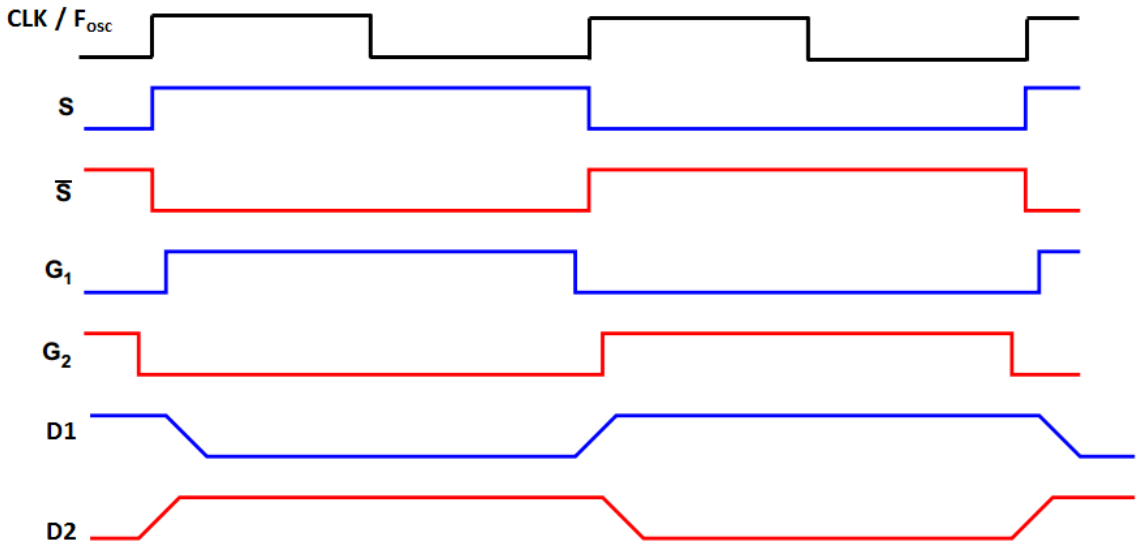

図 9-2. Detailed Output Signal Waveforms

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9.2 Typical Application

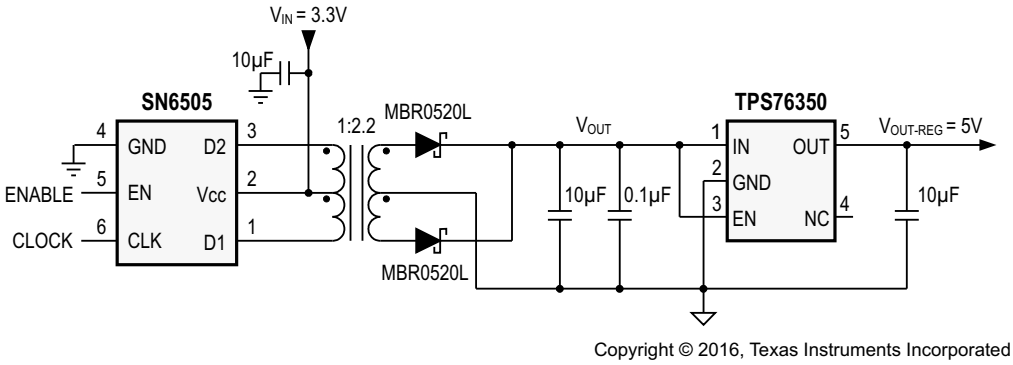

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図 9-3. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as design parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.3 V ± 3%
Output voltage	5 V
Maximum load current	100 mA

9.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in 図 6-1 and 図 6-11 for example, shows that the difference between V_{OUT} at minimum load and V_{OUT} at maximum load exceeds a transceiver's supply range. Therefore, in order to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

The final converter circuit is shown in 図 9-8. The measured V_{OUT} and efficiency characteristics for the regulated and unregulated outputs are shown in 図 6-2 and 図 6-12.

9.2.2.1 Drive Capability

The transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 2.25 V to 5.5 V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios don't lead to primary currents that exceed the specified current limits of the device.

9.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 600 mA, choose a 600 mA to 750 mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current should be as low as possible to maintain efficiency. For a low-cost 750 mA LDO, a V_{DO} of 600 mV at 750 mA is common. Be aware; however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (1)$$

This means in order to determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (that is, 600 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If it is not, the LDO will lose line-regulation and any variations at the input passes straight through to the output. Hence, below $V_{I\text{-}min}$ the output voltage follows the input and the regulator behaves like a simple conductor.

- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches its maximum voltage of

$$V_{S\text{-}max} = V_{IN\text{-}max} \times n \quad (2)$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. 表 9-2 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

表 9-2. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

PUSH-PULL CONVERTER				LDO
CONFIGURATION	$V_{IN\text{-}max}$ [V]	TURNS-RATIO	$V_{S\text{-}max}$ [V]	$V_{I\text{-}max}$ [V]
3.3 V_{IN} to 3.3 V_{OUT}	3.6	1.5 ± 3%	5.6	6 to 10
3.3 V_{IN} to 5 V_{OUT}	3.6	2.2 ± 3%	8.2	10
5 V_{IN} to 5 V_{OUT}	5.5	1.5 ± 3%	8.5	10

9.2.2.3 Diode Selection

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the SN6505x-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275 mV at 100-mA forward current. For higher output voltages such as ±10 V and above use the MBR0530 which provides a higher DC blocking voltage of 30 V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. This can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168MM-40.

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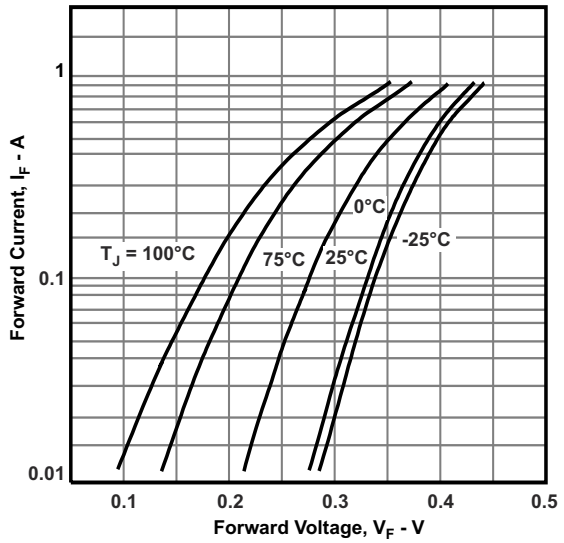

図 9-4. Diode Forward Characteristics for MBR0520L

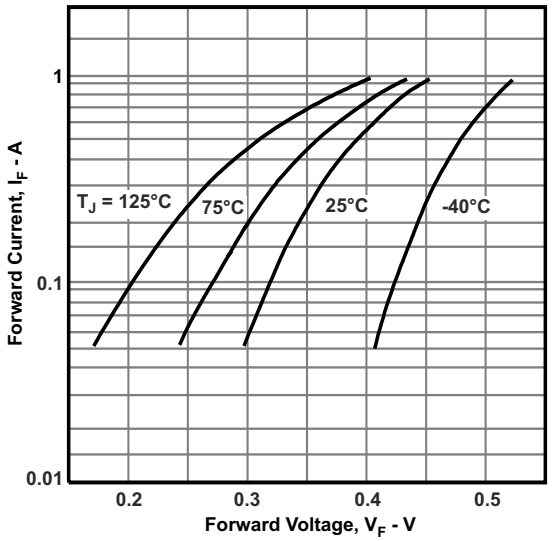

図 9-5. Diode Forward Characteristics MBR0530

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9.2.2.4 Capacitor Selection

The capacitors in the converter circuit in 図 9-8 are multi-layer ceramic chip (MLCC) capacitors.

As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10 nF to 100 nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1 µF to 10 µF. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and V_{IN}, the capacitor can be placed at the supply entrance of the board. To ensure low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1 µF to 10 µF.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7 µF to 10 µF will satisfy these requirements.

9.2.2.5 Transformer Selection

9.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined through:

$$Vt_{min} \geq V_{IN\text{-}max} \times \frac{T_{max}}{2} = \frac{V_{IN\text{-}max}}{2 \times f_{min}} \tag{3}$$

Taking an example of f_{min} as 138 kHz for SN6505A-Q1 and 363 kHZ for SN6505B-Q1 or SN6505D-Q1 with a 5 V supply, 式 3 yields the minimum V-t products of:

$$Vt_{min} \geq \frac{5.5\ V}{2 \times 138\ kHz} = 20\ V\mu s \quad \text{for SN6505A-Q1, and}$$

$$Vt_{min} \geq \frac{5.5\ V}{2 \times 363\ kHz} = 7.6\ V\mu s \quad \text{for SN6505B/D-Q1 applications.} \tag{4}$$

Common V-t values for low-power center-tapped transformers range from 22 Vµs to 150 Vµs with typical footprints of 10 mm x 12 mm. However, transformers specifically designed for PCMCIA applications provide as little as 11 Vµs and come with a significantly reduced footprint of 6 mm x 6 mm only.

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

9.2.2.5.2 Turns Ratio Estimate

Assume the rectifier diodes and linear regulator has been selected. Also, it has been determined that the transformer chosen must have a V-t product of at least 11 Vµs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer's typical efficiency of 97% into account:

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$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \quad (5)$$

$V_{S\text{-}min}$ must be large enough to allow for a maximum voltage drop, $V_{F\text{-}max}$, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the *セクション 9.2.2.2* section, this minimum input voltage is known and by adding $V_{F\text{-}max}$ gives the minimum secondary voltage with:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max} \quad (6)$$

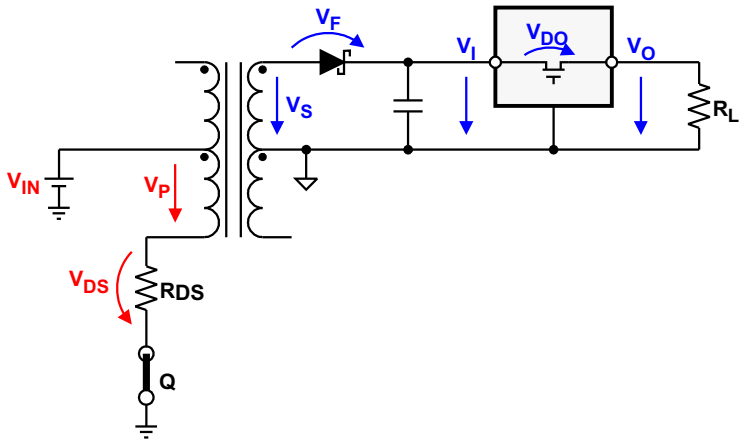

図 9-6. Establishing the Required Minimum Turns Ratio Through $N_{min} = 1.031 \times V_{S\text{-}min} / V_{P\text{-}min}$

Then calculating the available minimum primary voltage, $V_{P\text{-}min}$, involves subtracting the maximum possible drain-source voltage of the device, $V_{DS\text{-}max}$, from the minimum converter input voltage $V_{IN\text{-}min}$:

$$V_{P\text{-}min} = V_{IN\text{-}min} – V_{DS\text{-}max} \quad (7)$$

$V_{DS\text{-}max}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the data sheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax} \quad (8)$$

Then inserting 式 8 into 式 7 yields:

$$V_{P\text{-}min} = V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{Dmax} \quad (9)$$

and inserting 式 9 and 式 6 into 式 5 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max}}{V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{D\text{-}max}} \quad (10)$$

Example:

For a 3.3 V_{IN} to 5 V_{OUT} converter using the rectifier diode MBR0520L and the 5 V LDO, the data sheet values taken for a load current of 600 mA and a maximum temperature of 85°C are $V_{F\text{-}max}$ = 0.2 V, $V_{DO\text{-}max}$ = 0.5 V, and $V_{O\text{-}max}$ = 5.1 V.

Then assuming that the converter input voltage is taken from a 3.3 V controller supply with a maximum ±2% accuracy makes $V_{IN\text{-}min}$ = 3.234 V. Finally the maximum values for drain-source resistance and drain current at 3.3 V are taken from the data sheet with $R_{DS\text{-}max}$ = 0.31 Ω and $I_{D\text{-}max}$ = 1 A.

Inserting the values above into 式 10 yields a minimum turns ratio of:

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$$n_{min} = 1.031 \times \frac{0.2\ V + 0.5\ V + 5.1\ V}{3.234\ V - 0.31\ \Omega \times 1\ A} = 2.05 \quad (11)$$

Most commercially available transformers for 3-to-5 V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of ±3%.

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9.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in 図 9-7 or standard configuration in 図 9-8.

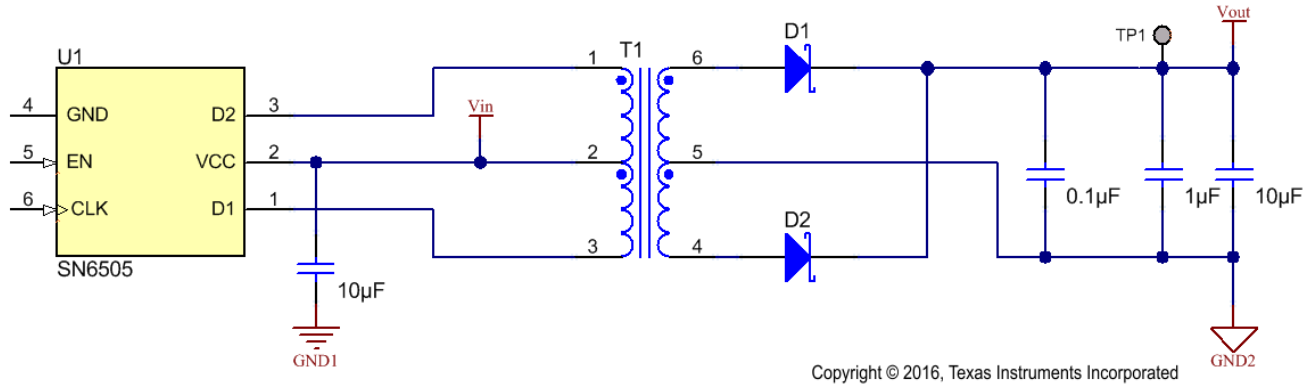

図 9-7. Unregulated Output for Low-Current Loads With Wide Supply Range

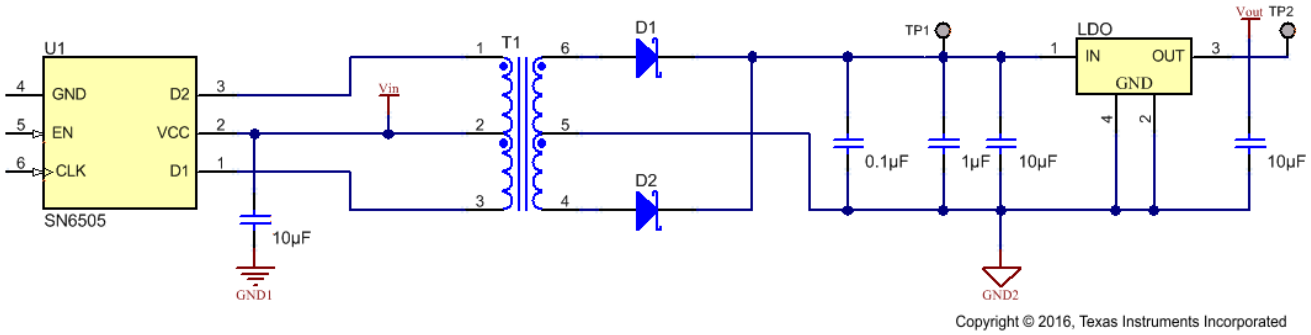

図 9-8. Regulated Output for Stable Supplies and High Current Loads

The Wurth Electronics Midcom isolation transformers in 表 9-3 are optimized designs for the device, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

表 9-3. Recommended Isolation Transformers Optimized for the Device

TURNS RATIO	V × T (Vμs)	ISOLATION (V_{RMS})	DIMENSIONS (mm)	APPLICATION	LDO(1)	ORDER NO.	MANUFACTURER
1:1.1 ±2%	7	2500	6.73 x 10.05 x 4.19	3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 Refer to 図 6-13 and 図 6-14	No	760390011	Wurth Electronics / Midcom
1:1.1 ±2%	11			5 V → 5 V, 100mA, SN6505B/D-Q1 Refer to 図 6-15 and 図 6-16		760390012	
1:1.7 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1 Refer to 図 6-17 and 図 6-18		760390013	
1:1.3 ±2%				3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 Refer to 図 6-19 and 図 6-20	Yes	760390014	
1:1.3 ±2%				5 V → 5 V, 100mA, SN6505B/D-Q1 Refer to 図 6-21 and 図 6-22		760390014	
1:2.1 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1 Refer to 図 6-23 and 図 6-24		760390015	
1.23:1 ±2%				5 V → 3.3 V, 100mA, SN6505B/D-Q1		750313710	
1:1.7 ±2%	8.9		8.3 x 12.6 x 4.1	3.3 V → 3.3 V, 1A, SN6505B/D-Q1 Refer to 図 6-25 and 図 6-26		750316028	
1:2.1 ±2%				3.3 V → 5 V, 1A, SN6505B/D-Q1 Refer to 図 6-27 and 図 6-28	No	750316029	
1.3:1 ±2%	10.8			5 V → 3.3 V, 1A, SN6505B/D-Q1 Refer to 図 6-29 and 図 6-30		750316030	
1:1.1 ±2%	8.6			3.3 V → 3.3 V , 1A , SN6505B/D-Q1 5 V → 5 V , 1A , SN6505B/D-Q1 Refer to 図 6-11 and 図 6-12		750315371	
1:1.1 ±2%	11	5000	9.14 x 12.7 x 7.37	3.3 V → 3.3 V, 100mA, SN6505B/D-Q1		750313734	
1:1.1 ±2%				5 V → 5 V, 100mA, SN6505B/D-Q1		750313734	
1:1.7 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1		750313769	
1:1.3 ±2%				3.3 V → 3.3 V, 100mA, SN6505B/D-Q1 5 V → 5 V, 100mA, SN6505B/D-Q1	Yes	750313638	
1:2.1 ±2%				3.3 V → 5 V, 100mA, SN6505B/D-Q1		750313626	
1.3:1 ±2%				5 V → 3.3 V, 100mA , SN6505B/D-Q1	No	750313638	
1:1.75 ±2%	41		12.32 x 15.41 x 11.05	3.3 V → 3.3 V, 1A, SN6505A-Q1 Refer to 図 6-3 and 図 6-4	Yes	750316031	
1:2 ±2%				3.3 V → 5 V, 1A, SN6505A-Q1 Refer to 図 6-5 and 図 6-6	No	750316032	
1.3:1 ±2%	42			5.0 V → 3.3 V, 1A, SN6505A-Q1 Refer to 図 6-7 and 図 6-8		750316033	
1:1.1 ±2%	23		12.32 x 15.41 x 11.89	3.3 V → 3.3 V, 1A, SN6505A-Q1 5 V → 5 V, 1A , SN6505A-Q1 Refer to 図 6-1 and 図 6-2		750315240	
1:1.3 ±3%	11	5000	10.4 x 12.2 x 6.1	3.3 V → 3.3 V, 300mA, SN6505B/D-Q1 5 V → 5 V, 300mA , SN6505B/D-Q1	No	HCT-SM-1.3-8-2	Bourns
1:1.5 ±3%	34.4	2500	10 x 12.07 x 5.97	3.3 V → 3.3 V, 1A, SN6505A/B/D-Q1 5 V → 5 V, 1A , SN6505A/B/D-Q1	Yes	DA2303-AL	Coilcraft
1:2.2 ±3%	21.5	2500	10 x 12.07 x 5.97	3.3 V → 5 V, 1A, SN6505A/B/D-Q1		DA2304-AL	

(1) For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out. Figures show the voltage and efficiency at the LDO input.

9.2.3 Application Curves

See the *セクション 6.7* and *セクション 6.8* for application curves with transformers optimized for the device, providing high efficiency and small form factor at low-cost.

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9.2.4 System Examples

9.2.4.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide high output voltages of up to 30 V, or bipolar outputs of up to ±15 V. Using commercially available center-tapped transformers, with their rather low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. 図 9-9 to 図 9-11 show some of these topologies together with their respective open-circuit output voltages.

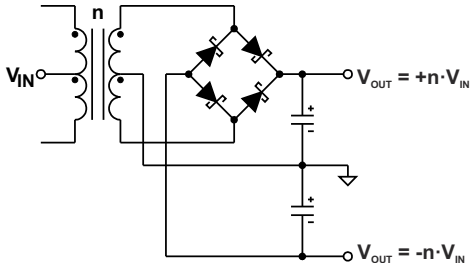

図 9-9. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

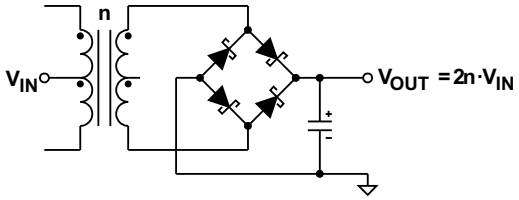

図 9-10. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Dodoubling

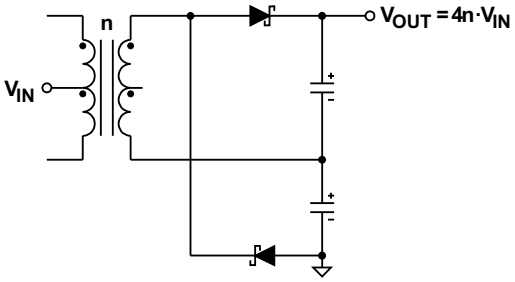

図 9-11. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

9.2.4.2 Application Circuits

The following application circuits are shown for a 3.3 V input supply commonly taken from the local, regulated microcontroller supply. For 5 V input voltages requiring different turn ratios refer to the transformer manufacturers and their web sites listed in 表 9-4.

表 9-4. Transformer Manufacturers

MANUFACTURER	MORE INFORMATION
Coilcraft Inc.	http://www.coilcraft.com
Halo-Electronics Inc.	http://www.haloelectronics.com
Murata Power Solutions	http://www.murata-ps.com
Wurth Electronics Midcom Inc	http://www.midcom-inc.com

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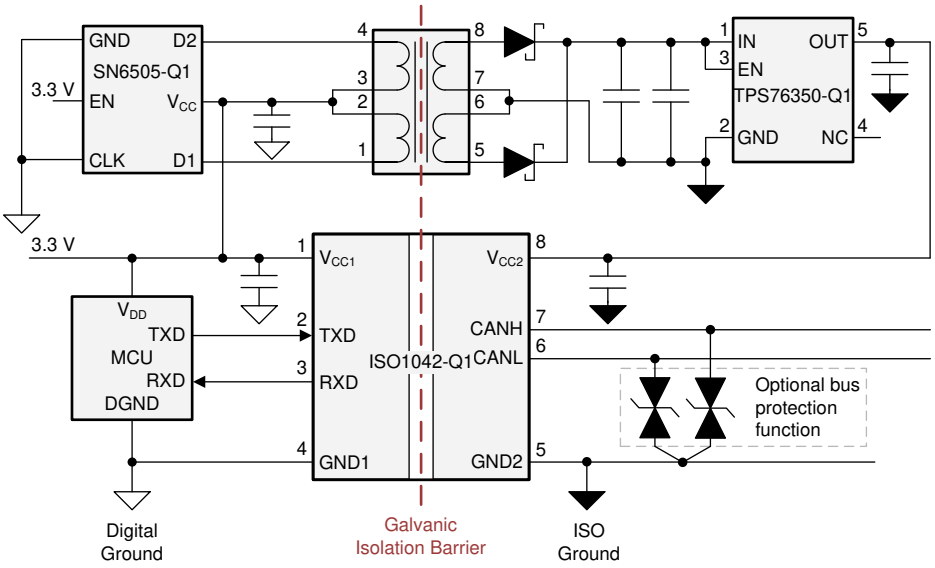

図 9-12. Isolated CAN Interface

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10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5 V nominal. This input supply must be regulated within ±10%. If the input supply is located more than a few inches from the device, a 0.1 µF by-pass capacitor should be connected as close as possible to the device V_{CC} pin and a 10 µF capacitor should be connected close to the transformer center-tap pin.

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11 Layout

11.1 Layout Guidelines

- The V_{IN} pin must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 µF to 10 µF. The capacitor must have a voltage rating of 10 V minimum and a X5R or X7R dielectric.
- The optimum placement is closest to the V_{IN} and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin. See 図 11-1 for a PCB layout example.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device V_{CC} pin and the transformer center-tap must be as close as possible for minimum trace inductance.
- The connection of the device V_{CC} pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1µF to 10 µF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.
- The device GND pins must be tied to the PCB ground plane using two vias for minimum inductance.
- The ground connections of the capacitors and the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage in the 10 mA to 100 mA current range to maximize efficiency.
- The V_{OUT} pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1µF to 10 µF. The capacitor must have a voltage rating of 16 V minimum and a X5R or X7R dielectric.

11.2 Layout Example

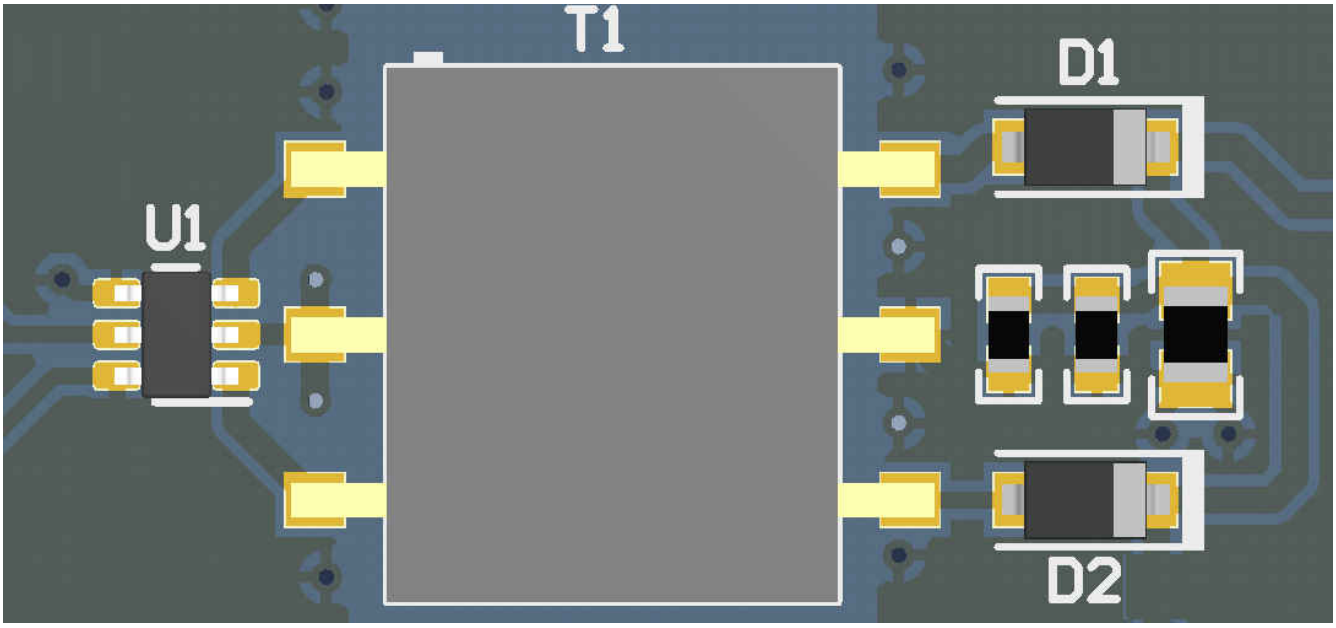

図 11-1. Layout Example of a 2-Layer Board

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12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to Isolate Signal and Power in Isolated CAN Systems* TI TechNote
- Texas Instruments, *Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for 3-Phase Inverter* TI Design

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN6505A-Q1	Click here	Click here	Click here	Click here	Click here
SN6505B-Q1	Click here	Click here	Click here	Click here	Click here
SN6505D-Q1	Click here	Click here	Click here	Click here	Click here

12.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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12.8 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN6505AQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ
SN6505AQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ
SN6505AQDBVTQ1	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ
SN6505AQDBVTQ1.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65AQ
SN6505BQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ
SN6505BQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ
SN6505BQDBVTQ1	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ
SN6505BQDBVTQ1.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65BQ
SN6505DQDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ
SN6505DQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ
SN6505DQDBVTQ1	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ
SN6505DQDBVTQ1.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	65DQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN6505A-Q1, SN6505B-Q1 :

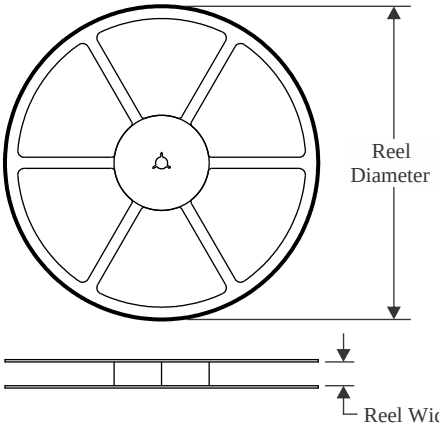
- Catalog : SN6505A, SN6505B

NOTE: Qualified Version Definitions:

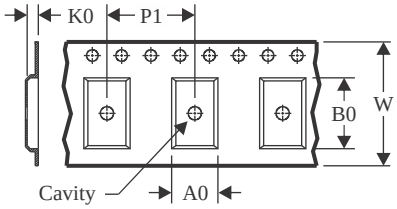
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

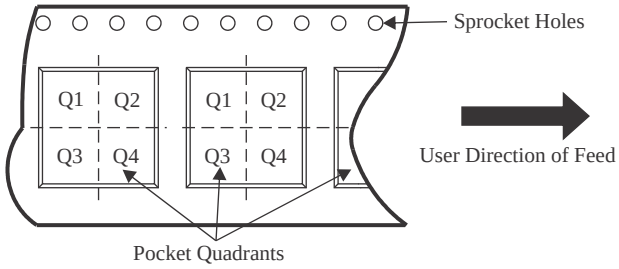


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

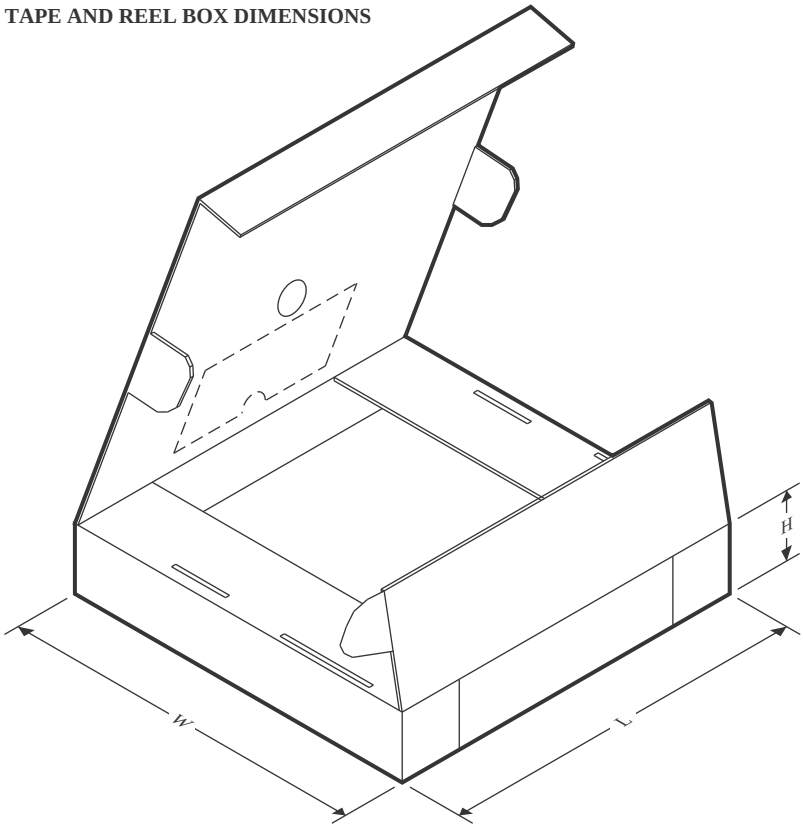
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN6505AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN6505AQDBVTQ1	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN6505BQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN6505BQDBVTQ1	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN6505DQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN6505DQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN6505DQDBVTQ1	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

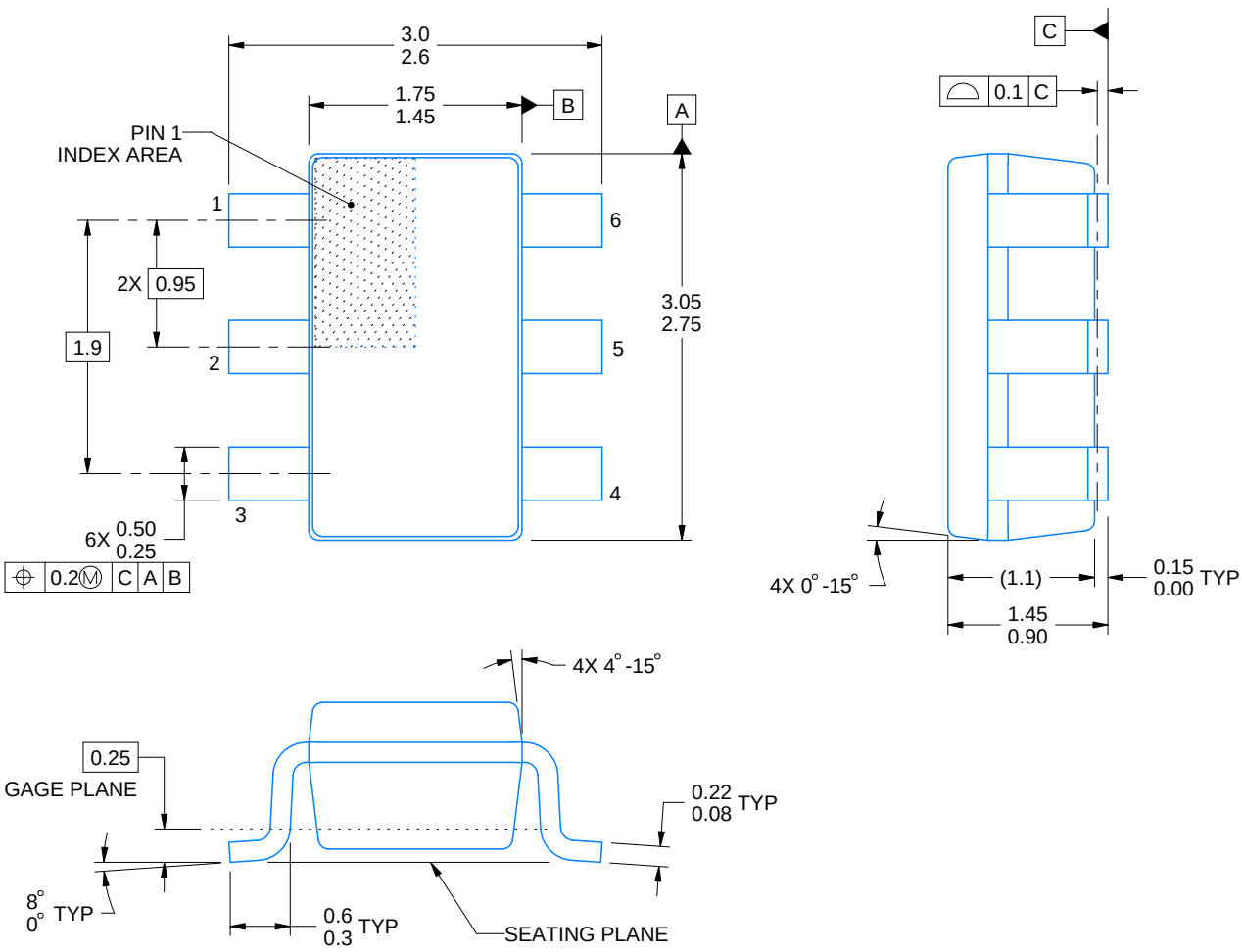
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN6505AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN6505AQDBVTQ1	SOT-23	DBV	6	250	210.0	185.0	35.0
SN6505BQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN6505BQDBVTQ1	SOT-23	DBV	6	250	210.0	185.0	35.0
SN6505DQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN6505DQDBVRQ1	SOT-23	DBV	6	3000	213.0	191.0	35.0
SN6505DQDBVTQ1	SOT-23	DBV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

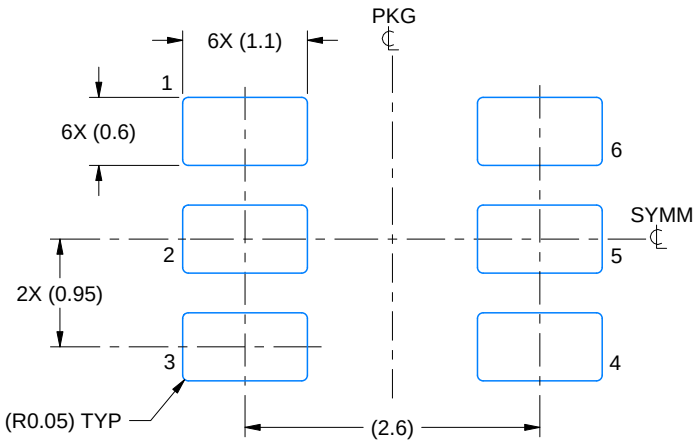
SMALL OUTLINE TRANSISTOR



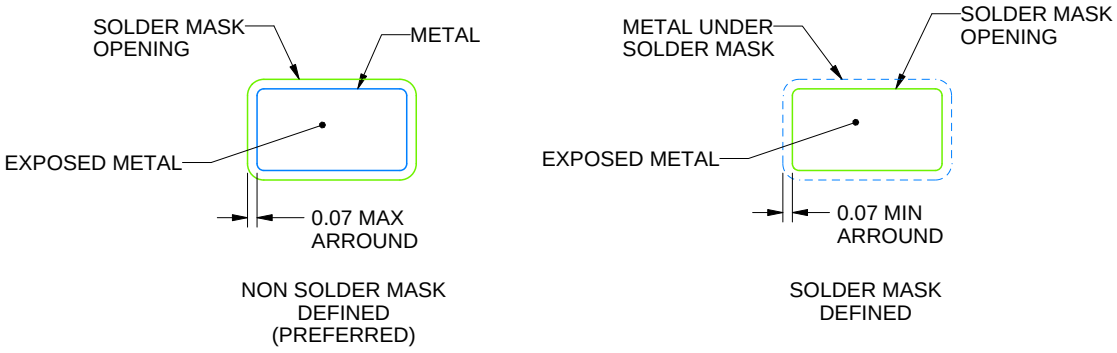
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

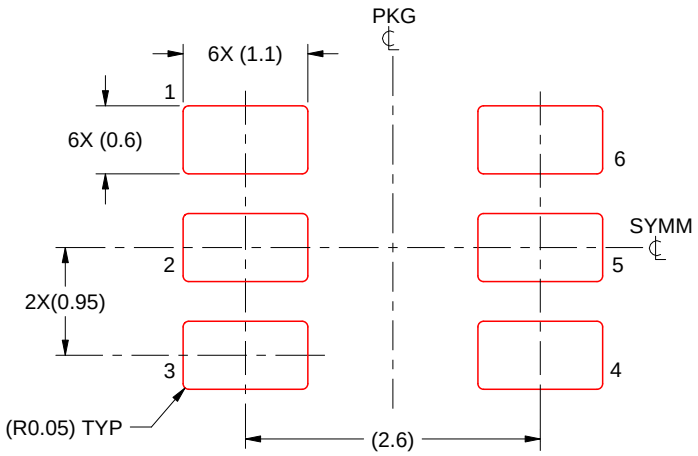


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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