SN74GTL2007
12-BIT GTL-/GTL/GTL+ TO LVTTL TRANSLATOR

- Operates as a GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator
- Series Termination on TTL Outputs of 30 Ω
- Latch-Up Testing Done to JEDEC Standard JESD 78
- ESD Performance Tested Per JEDEC Standard
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**description/ordering information**

The SN74GTL2007 is a 12-bit translator to interface between the 3.3-V LVTTL chip set I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VREF</td>
<td>GTL reference voltage</td>
</tr>
<tr>
<td>2-6, 8, 10-13, 15, 23</td>
<td>ENn nAn</td>
<td>Data and enable inputs/outputs (LVTTL)</td>
</tr>
<tr>
<td>7, 9, 16, 17-22, 24-27</td>
<td>nBn</td>
<td>Data inputs/outputs (GTL-/GTL/GTL+)</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>Ground (0 V)</td>
</tr>
<tr>
<td>28</td>
<td>VCC</td>
<td>Positive supply voltage</td>
</tr>
</tbody>
</table>

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>TSSOP – PW</td>
<td>SN74GTL2007PW</td>
<td>GK2007</td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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### Function Tables

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN1 1BI/2BI</td>
<td>1AO/2AO</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN2 3BI/4BI</td>
<td>3AO/4AO</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUT 9BI</th>
<th>OUTPUT 9AO</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>10A1/10A2 9BI</td>
<td>10BO1/10BO2</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INPUT/OUTPUT 5A/6A (OPEN DRAIN)</th>
<th>OUTPUT 7BO1/7BO2</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN2 5BI/6BI</td>
<td>L‡</td>
<td>L‡</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H†</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUT 11BI</th>
<th>INPUT/OUTPUT 11A (OPEN DRAIN)</th>
<th>OUTPUT 11BO</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L‡</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

H = High voltage level
L = Low voltage level

† The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

‡ Open-drain input/output terminal is driven to a logic-low state by an external driver.
NOTE A: The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage range, \( V_{CC} \) .............................................................. -0.5 to 4.6 V
Input voltage range, \( V_I \) (see Note 2): A port (LVTTL) ........................................ -0.5 to 4.6 V
B port (GTL) .................................................. -0.5 to 4.6 V
Output voltage range, \( V_O \) (output in OFF or HIGH state)(see Note 2): A port ........ -0.5 to 4.6 V
B port ........................................ -0.5 to 4.6 V
Input diode current, \( I_{IK} \) \((V_I < 0)\) .............................................................. -50 mA
Output diode current, \( I_{OK} \) \((V_O < 0)\) .............................................................. -50 mA
Current into any output in the LOW state: A port ........................................ 32 mA
B port .................................................. 30 mA
Current into any output in the HIGH state, A port ........................................ -32 mA
Package thermal impedance, \( \theta_{JA} \) (see Note 1) ........................................ 62°C/W
Storage temperature range, \( T_{stg} \) .............................................................. -60 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Voltages are referenced to GND (ground = 0 V).
NOTES: 1. The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions

<table>
<thead>
<tr>
<th>( V_{CC} ) Supply voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{TT} ) Termination voltage</td>
<td>GTL–</td>
<td>0.85</td>
<td>0.9</td>
<td>0.95</td>
</tr>
<tr>
<td></td>
<td>GTL</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
</tr>
<tr>
<td></td>
<td>GTL+</td>
<td>1.35</td>
<td>1.5</td>
<td>1.65</td>
</tr>
<tr>
<td>( V_{REF} ) Reference voltage</td>
<td>Overall</td>
<td>0.5</td>
<td>2/3 ( V_{TT} )</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>GTL–</td>
<td>0.5</td>
<td>0.6</td>
<td>0.63</td>
</tr>
<tr>
<td></td>
<td>GTL</td>
<td>0.76</td>
<td>0.8</td>
<td>0.84</td>
</tr>
<tr>
<td></td>
<td>GTL+</td>
<td>0.87</td>
<td>1</td>
<td>1.1</td>
</tr>
<tr>
<td>( V_I ) Input voltage</td>
<td>A port</td>
<td>0</td>
<td>3.3</td>
<td>3.6</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>0</td>
<td>( V_{TT} )</td>
<td>3.6</td>
</tr>
<tr>
<td>( V_{IH} ) HIGH-level input voltage</td>
<td>A port</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>( V_{REF} + 50 \text{ mV} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) LOW-level input voltage</td>
<td>A port</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>( V_{REF} - 50 \text{ mV} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OH} ) HIGH-level output current</td>
<td>A port</td>
<td>-16</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OL} ) LOW-level output current</td>
<td>A port</td>
<td>16</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( T_A ) Operating free-air temperature range</td>
<td>-40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
## Electrical Characteristics Over Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>–40°C TO +85°C</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$†</td>
<td>$V_{CC} = 3$ V to 3.6 V, $I_{OH} = –100$ µA $V_{CC} – 0.2$</td>
<td>$2.1$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$‡</td>
<td>$V_{CC} = 3$ V, $I_{OL} = 16$ mA</td>
<td>$0.8$</td>
<td>V</td>
</tr>
<tr>
<td>$I_I$</td>
<td>$V_{CC} = 3.6$ V, $V_I = V_{CC}$ $±1$</td>
<td>$±1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC} = 3.6$ V, $V_I = 0$ V</td>
<td>$±1$</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{ICQ}$§</td>
<td>$V_{CC} = 3.6$ V, $I_{ICQ} = 16$ mA</td>
<td>$12$</td>
<td>mA</td>
</tr>
<tr>
<td>$C_{IO}$</td>
<td>$V_O = 3$ V or $0$ V</td>
<td>$5$</td>
<td>pF</td>
</tr>
</tbody>
</table>

† All typical values are measured at $V_{CC} = 3.3$ V and $T_A = 25°C$.
‡ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
§ This is the increase in supply current for each input that is at the specified LVTTL voltage, rather than $V_{CC}$ or GND.

### Switching Characteristics Over Recommended Operating Free-Air Temperature Range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>WAVEFORM</th>
<th>GTL–</th>
<th>GTL</th>
<th>GTL+</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>$A$ to $B_n$</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>$B_n$ to $A$</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>9 BI to 10 BO n</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>11 BI to 11 BO</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$B_n$ to $B_n$</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>ENn to $A$</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>$B_n$ to $A$ (I/O)</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>EN2 to $A$ (I/O)</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.6$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 0.8$ V</td>
<td>$V_{CC} = 3.3$ V, $V_{REF} = 1$ V</td>
<td>ns</td>
</tr>
</tbody>
</table>

† All typical values are measured at $V_{CC} = 3.3$ V and $T_A = 25°C$.
‡ Includes –7.6-ns RC rise time of test-load pullup on 11-A, 1.5-kΩ pullup, and 21-pF load on 11-A has approximately 23-ns RC rise time.
PARAMETER MEASUREMENT INFORMATION

\[ V_{TT} = 1.2 \text{ V}, \ V_{REF} = 0.8 \text{ V} \text{ for GTL} \] and \[ V_{TT} = 1.5 \text{ V}, \ V_{REF} = 1 \text{ V} \text{ for GTL+} \]

From Output Under Test

\[ C_L = 50 \text{ pF} \]

(see Note A)

\[ \begin{array}{|c|c|}
\hline
\text{TEST} & \text{S1} \\
\hline
\text{tPLH/tPHL} & \text{Open} \\
\text{tPLZ/tPZL} & 2 \times V_{CC} \\
\hline
\end{array} \]

From Output Under Test

\[ C_L = 30 \text{ pF} \]

(see Note A)

LOAD CIRCUIT FOR A OUTPUTS

\[ \begin{array}{c}
\text{Input} \\
\text{(see Note B)} \\
\end{array} \]

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{V}_{\text{REF}} \]

\[ \text{V}_{\text{REF}} \]

\[ \text{V}_{\text{TT}} \]

\[ \text{V}_{\text{OL}} \]

\[ \text{V}_{\text{OH}} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{V}_{\text{REF}} \]

\[ \text{V}_{\text{REF}} \]

\[ \text{V}_{\text{TT}} \]

\[ \text{V}_{\text{OL}} \]

\[ \text{V}_{\text{OH}} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

\[ 1.5 \text{ V} \]

\[ \text{Input} \]

(see Note B)

\[ 1.5 \text{ V} \]

\[ 1.5 \text{ V} \]

\[ 3 \text{ V} \]

\[ 0 \text{ V} \]

\[ \text{Output} \]

\[ \text{S1 at } 2 \times V_{\text{CC}} \]

\[ 1.5 \text{ V} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{V}_{\text{OL}} \]

† All control inputs are LVTTL levels.

NOTES:

A. \( C_L \) includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: \( PRR \leq 10 \text{ MHz}, Z_O = 50 \Omega, t_r \leq 2.5 \text{ ns}, t_f \leq 2.5 \text{ ns} \).

C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms
Frequently Asked Questions

**Question 1:** On the GTL2007 LVTTL input, specifically 10AI1 and 10AI2, when the GTL2007 is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high impedance when the device is powered down, and will there be any leakage?

**Answer 1:** When the device is powered down, the LVTTL inputs are in a high-impedance state and do not leak to V\textsubscript{DD} if they are pulled high while the device is powered down.

**Question 2:** Do all the LVTTL inputs have the same powered-down characteristic?

**Answer 2:** Yes

**Question 3:** What is the condition of the other GTL I/O and LVTTL output pins when the device is powered down?

**Answer 3:** The open-drain outputs, both GTL and LVTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTL totem-pole outputs, however, are not open-drain type outputs, and there is no current flow on these pins if they are pulled high when V\textsubscript{DD} is at ground.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2007PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>28</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>GK2007</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74GTL2007PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>28</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>GK2007</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) RoHS: TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

**RoHS Exempt:** TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Depth (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2007PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>28</td>
<td></td>
<td>330.0</td>
<td>16.4</td>
<td>6.9</td>
<td>10.2</td>
<td>1.8</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2007PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>28</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
△ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
△ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate design.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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