SN74LVC2G08-Q1 デュアル 2 入力正論理 AND ゲート

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1：–40℃ ~ +125℃の周囲動作温度範囲 (DCU パッケージ)
  - デバイス温度グレード 3：–40℃ ~ +85℃の周囲動作温度範囲 (DCT パッケージ)
- 5V V_{CC} 動作に対応
- 5.5V までの入力電圧に対応
- 低消費電力、最大 I_{CC} 10μA
- 3.3V において ±24mA の出力駆動能力
- I_{off} により部分的パワーダウン・モード動作をサポート
- 最高 5.5V の入力を V_{CC} レベルに変換する降圧トランスレータとして使用可能
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- 複数の電力レールのパワー・グッド信号を結合
- 条件が真になるまで信号の通過を抑止
- アクティブ LOW エラー信号の結合

3 概要

このデュアル 2 入力の正論理 AND ゲートは、1.65V ~ 5.5V の V_{CC} で動作するように設計されています。

SN74LVC2G08-Q1 はブール関数 $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ を正論理で実行します

このデバイスは、I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off} 回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

製品情報 (1) (0 ページ)

型番	パッケージ	本体サイズ (公称)
SN74LVC2G08DCT-Q1	SM8 (8)	2.95mm × 2.80mm
SN74LVC2G08DCU-Q1	VSSOP (8)	2.30mm × 2.00mm

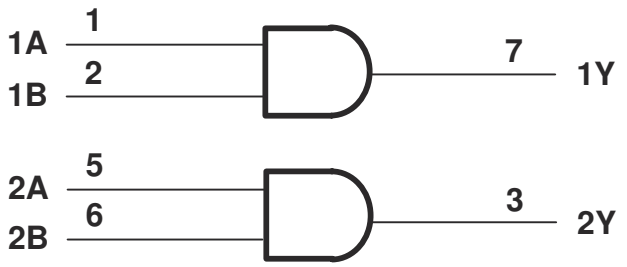


図 3-1. 論理図 (正論理)

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (March 2010) to Revision E (October 2020) **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「概要」セクションから「標準 V_{OLP} (出力グランド・バウンス) < 0.8V (V_{CC} = 3.3V、T_A = 25℃)」を削除 ... 1
- 「概要」セクションから「標準 V_{OHV} (出力 V_{OHV} アンダーシュート) > 2V (V_{CC} = 3.3V、T_A = 25℃)」を削除 ... 1
- 「*概要*」セクションから「注文情報」表を削除 ... 1
- 「*概要*」セクションに「製品情報」表を追加 ... 1
- 「*概要*」セクションに「論理図 (正論理)」図を追加 ... 1
- Added the *Pin Configuration and Functions* section ... 3
- Added SN74LVC2G08DCT-Q1 and SN74LVC2G08DCU-Q1 minimum and maximum operating free-air temperature ranges to the *Recommended Operating Conditions* section ... 5
- Added the T_A temperature ranges (–40°C to 85°C and –40°C to 125°C) for the t_{pd} parameter to the *Switching Characteristics* section ... 6
- Added the *Typical Characteristics* section ... 7
- Added the *Overview* section ... 9
- Added the *Functional Block Diagram* section ... 9
- Added the *Features Description* section ... 9
- Added the *Device Funcational Modes* section ... 10
- Added the *Application and Implementation* section ... 11
- Added the *Application Information* section ... 11
- Added the *Power Supply Recommendations* section ... 12
- Added the *Layout* section ... 12
- Added the *Layout Guidelines* section ... 12
- Added the *Layout Example* section ... 12
- Updated the *Device and Documentation Support* section ... 13

5 Pin Configuration and Functions

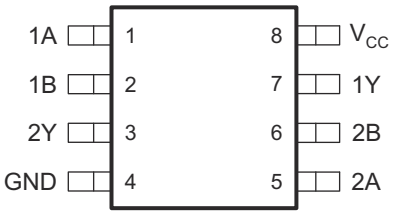


図 5-1. DCT Package
8-Pin SM8
Top View

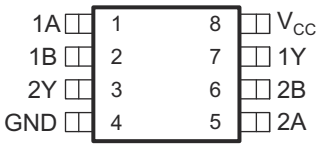


図 5-2. DCU Package
8-Pin VSSOP
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1 logic input
1B	2	I	Channel 1 logic input
1Y	7	O	Logic level output
2A	5	I	Channel 2 logic input
2B	6	I	Channel 2 logic input
2Y	3	O	Logic level output
GND	4	—	Ground
V_{CC}	8	—	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	6.5	V
V_I	Input voltage range(1)	–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(1)	–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(1) (2)	–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current		–50	mA
I_{OK}	Output clamp current		–50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(2) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature	SN74LVC2G08DCU-Q1	–40	125	°C
		SN74LVC2G08DCT-Q1	–40	85	

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC2G08-Q1		UNIT
		DCT (SM8)	DCU (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	201.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.2	91.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	100	122.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	42.4	31.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	98.9	122.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA	1.65 V	1.2			
		I_{OH} = –8 mA	2.3 V	1.9			
		I_{OH} = –16 mA	3 V	2.4			
		I_{OH} = –24 mA		2.3			
		I_{OH} = –32 mA	4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA				0.55	
		I_{OL} = 32 mA	4.5 V			0.55	
I_I	A or B inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND, T_A = –40°C to 85°C	3 V to 5.5 V			500	µA
C_i		V_I = V_{CC} or GND, T_A = –40°C to 85°C	3.3 V		5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A	V_{CC}	MIN	MAX	UNIT
t_{pd}	A or B	Y	–40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	2.6	9	ns
				V_{CC} = 2.5 V ± 0.2 V	1	5.1	
				V_{CC} = 3.3 V ± 0.3 V	1	4.7	
				V_{CC} = 5 V ± 0.5 V	1	3.8	
			–40°C to 125°C	V_{CC} = 1.8 V ± 0.15 V	2.6	9.8	
				V_{CC} = 2.5 V ± 0.2 V	1	5.8	
				V_{CC} = 3.3 V ± 0.3 V	1	5.3	
				V_{CC} = 5 V ± 0.5 V	1	4.8	

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	17	17	17	20	pF

7 Typical Characteristics

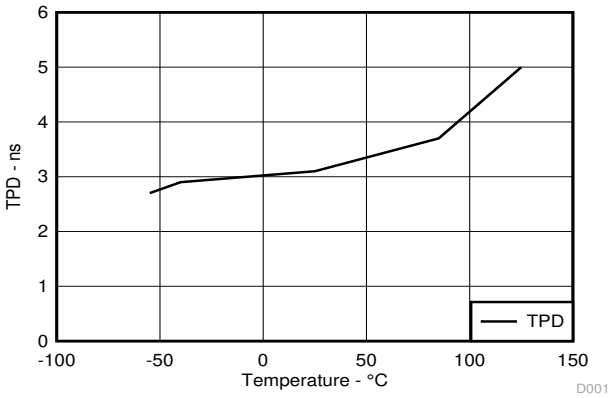


図 7-1. t_{PD} Across Temperature at 3.3-V V_{CC}

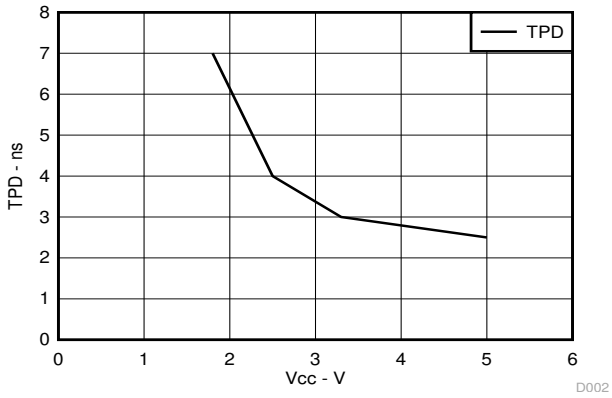
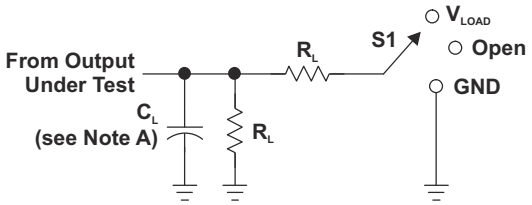


図 7-2. t_{PD} Across V_{CC} at 25°C

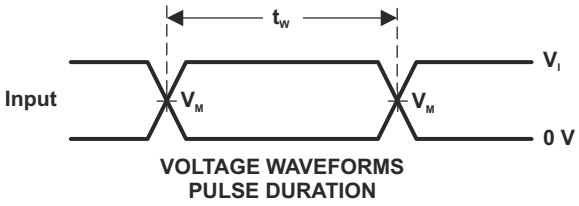
8 Parameter Measurement Information



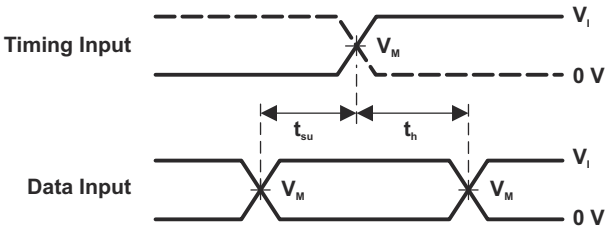
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

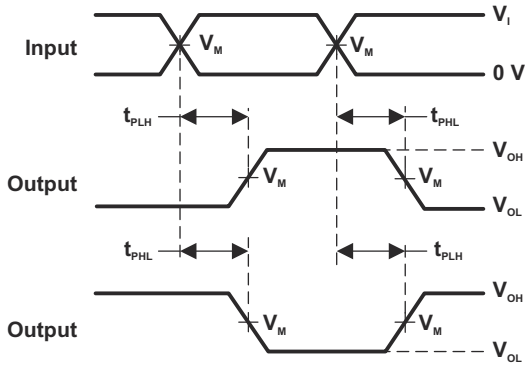
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 W	0.3 V



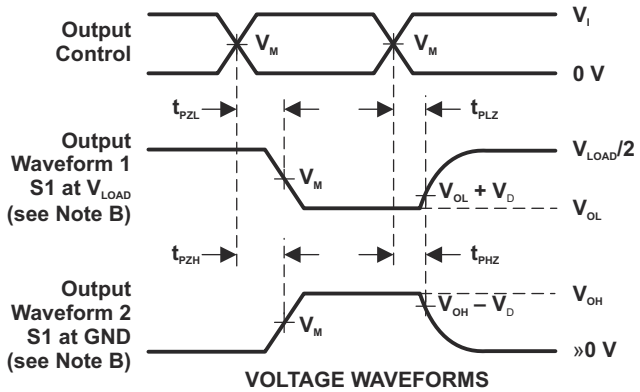
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.

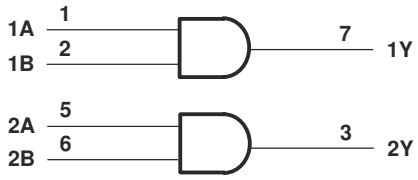
図 8-1. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVC2G08-Q1 device contains two 2-input positive AND gates and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

9.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in Implications of Slow or Floating CMOS Inputs.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10-kΩ resistor is recommended and will typically meet all requirements.

9.3.3 Clamp Diode Structure

The inputs and outputs to this device have negative clamping diodes only as depicted in 図 9-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

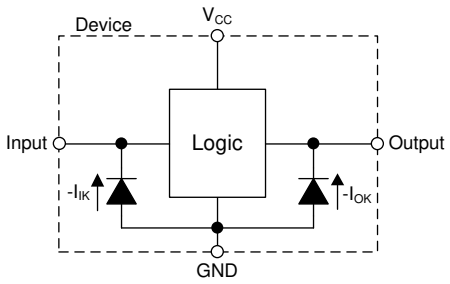


図 9-1. Electrical Placement of Clamping Diodes for Each Input and Output

9.3.4 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

9.4 Device Functional Modes

表 9-1 lists the functional modes of the SN74LVC2G08-Q1.

表 9-1. Function Table

INPUTS		OUTPUT
A	**B**	**Y**
H	H	H
L	X	L
X	L	L

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74LVC2G08-Q1 is a high-drive CMOS device that can be used for implementing AND logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V, making it Ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate down to V_{CC}.

10.2 Typical Application

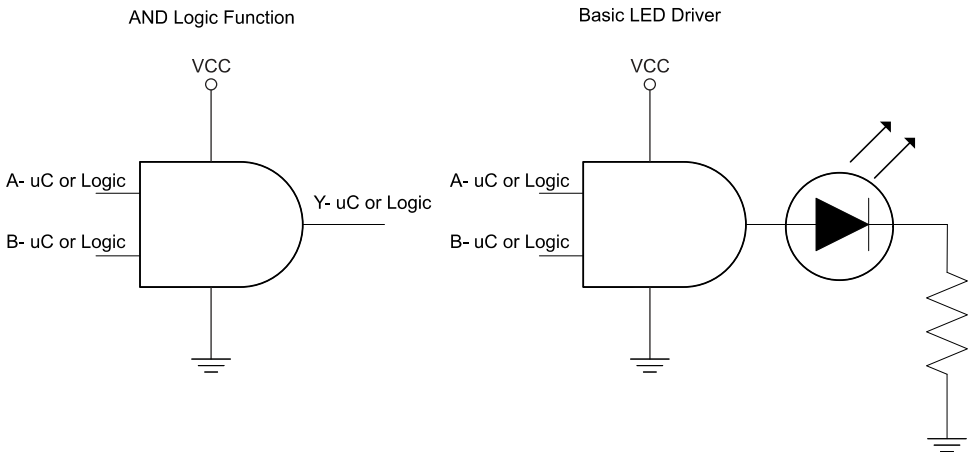


図 10-1. Typical Application

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions must be considered to prevent ringing.

10.2.1.1 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I maximum) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents must not exceed (I_O maximum) per output and must not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the *Recommended Operating Conditions* table.
   - Outputs must not be pulled above V_{CC} in normal operating conditions.

11 Application Curves

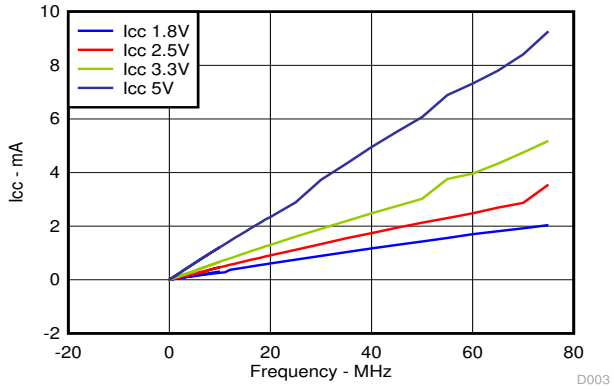


図 11-1. I_{CC} vs Frequency

12 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results

13 Layout

13.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

13.2 Layout Example

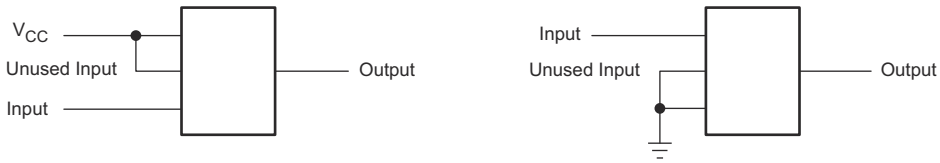


図 13-1. Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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14.3 Trademarks

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14.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2G08IDCTRQ1	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C08 Z
SN74LVC2G08QDCURQ1	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HLRQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC2G08-Q1 :

- Catalog : SN74LVC2G08

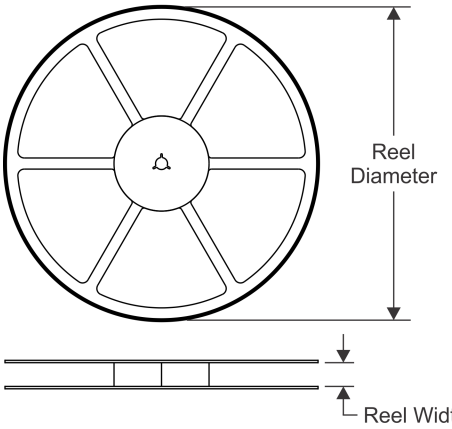
- Enhanced Product : SN74LVC2G08-EP

NOTE: Qualified Version Definitions:

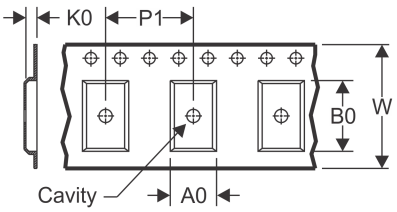
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

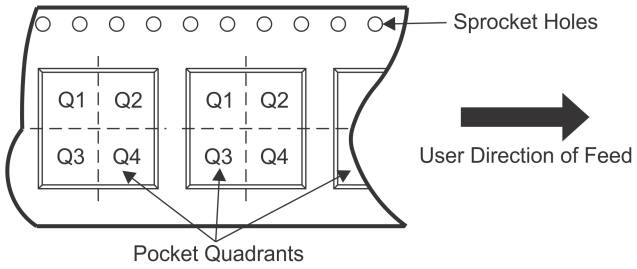


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

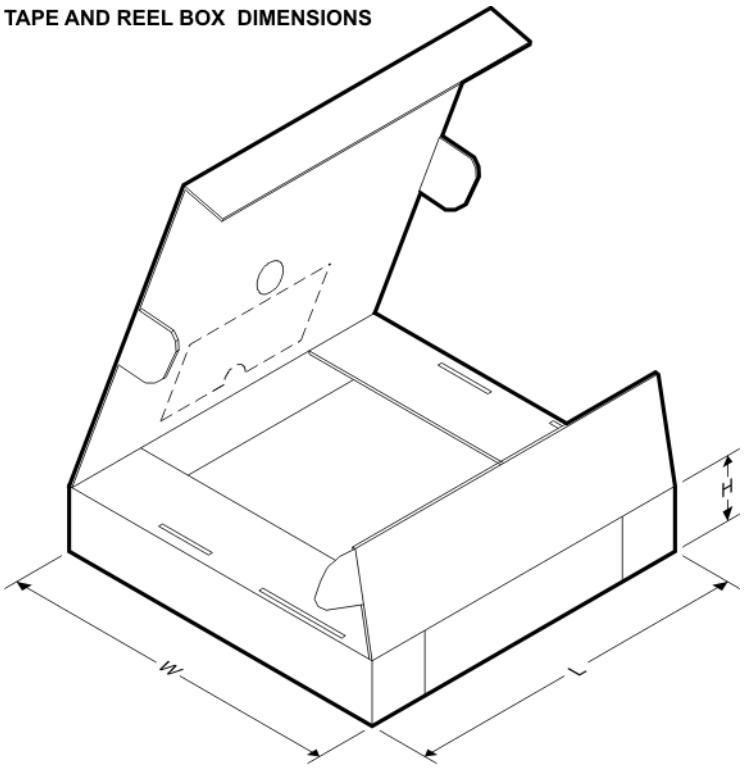
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

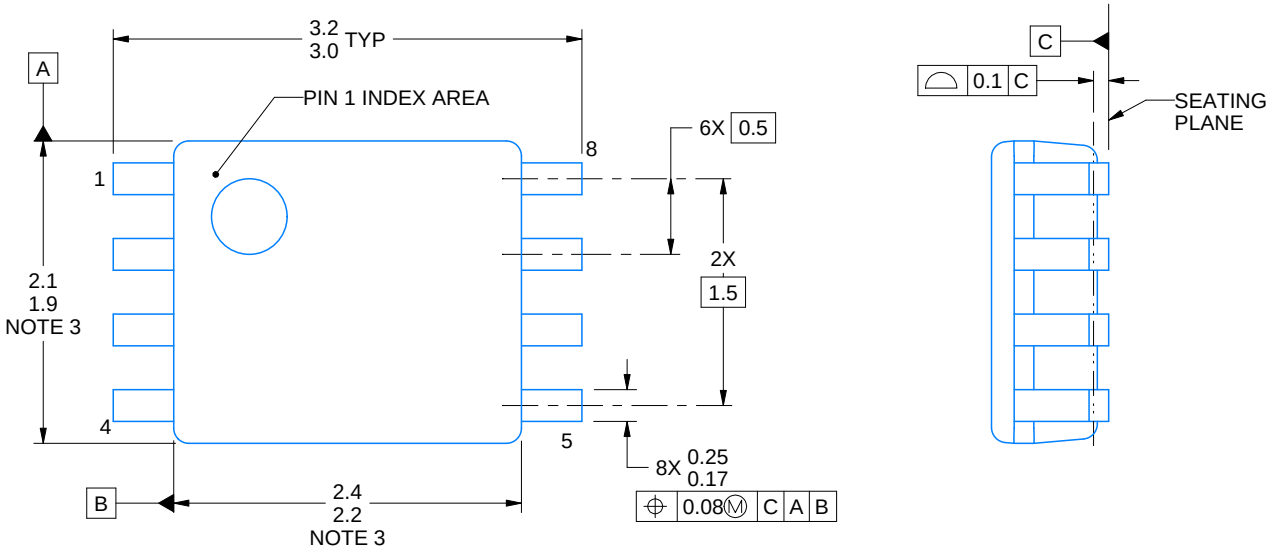
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G08QDCURQ1	VSSOP	DCU	8	3000	183.0	183.0	20.0

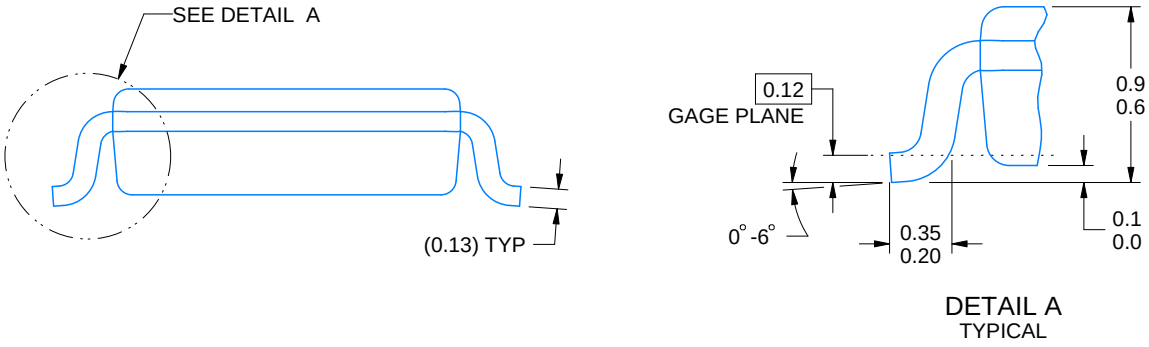
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

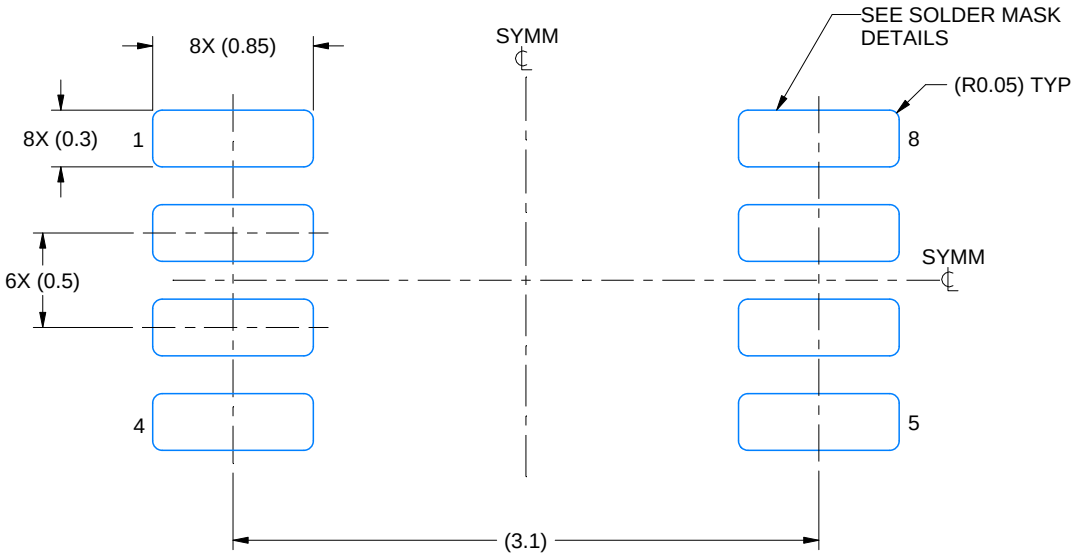




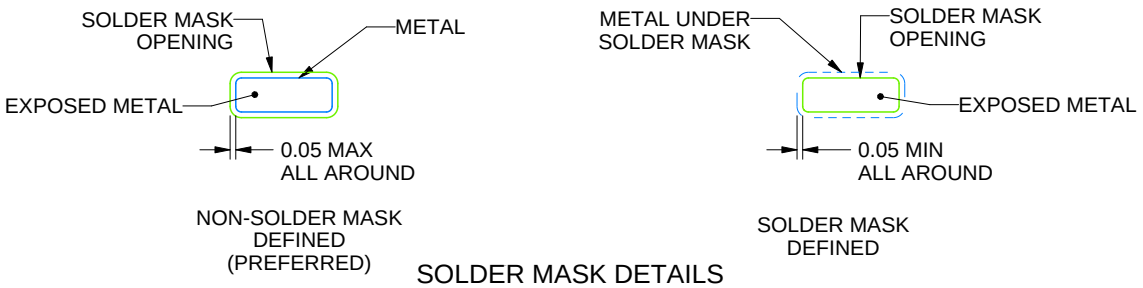
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

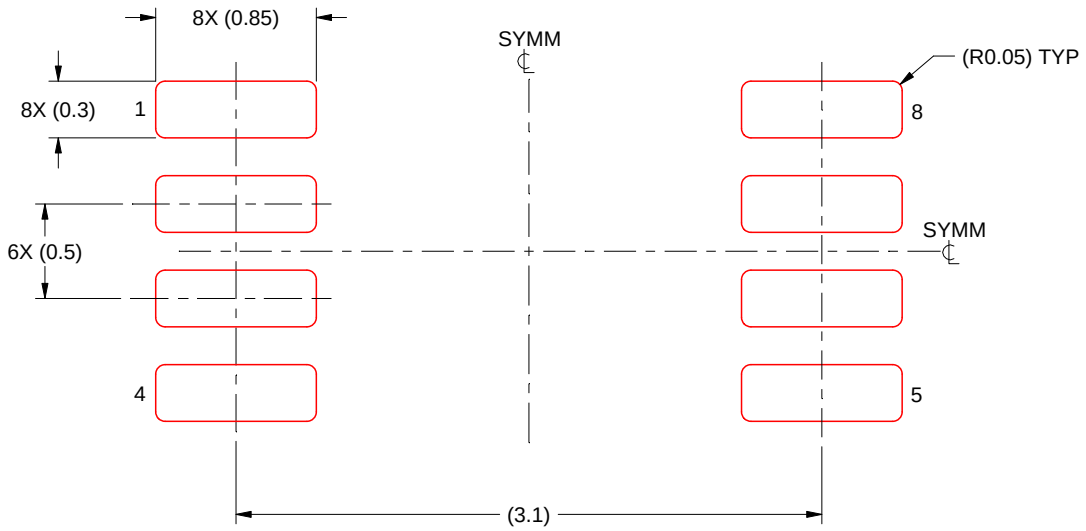


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

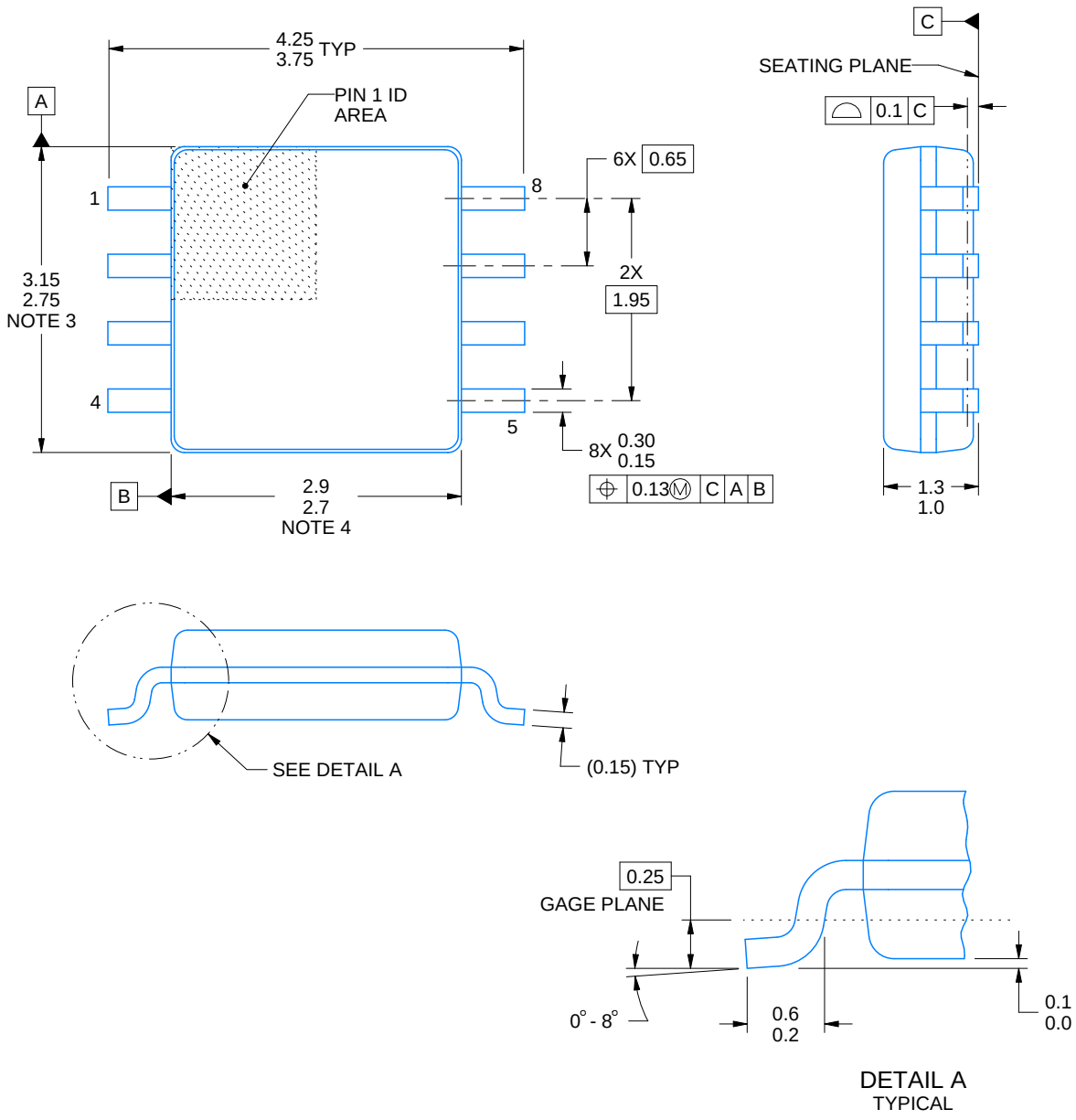
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

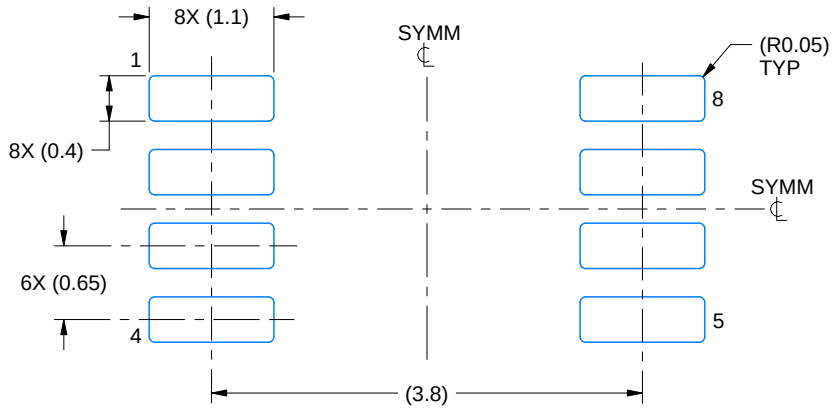
SMALL OUTLINE PACKAGE



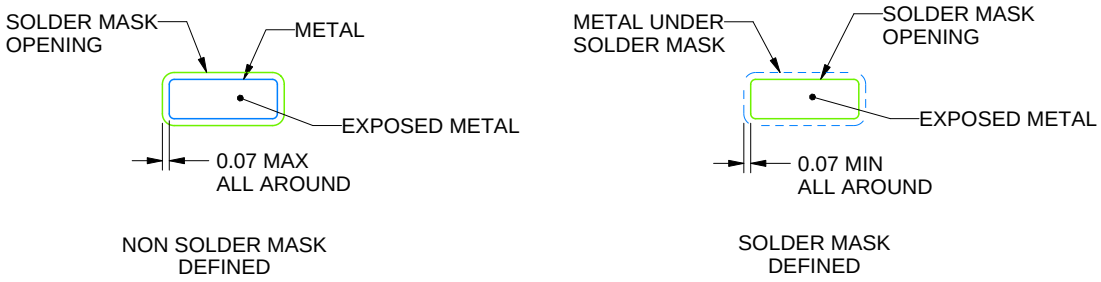
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

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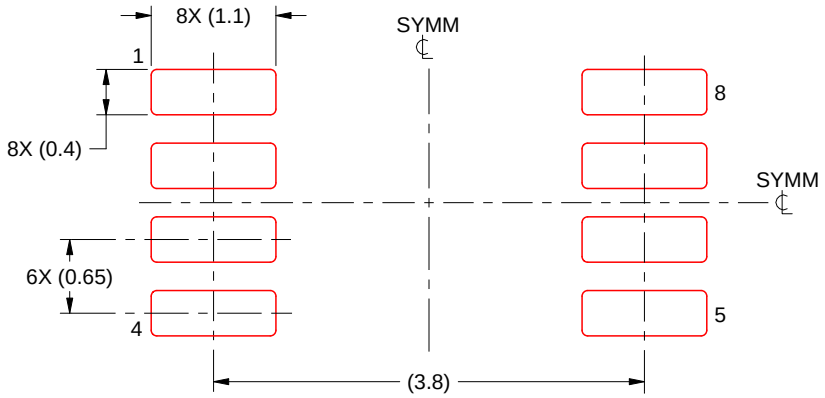
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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