TEXAS INSTRUMENTS
TAS5827
JAJSSI1 – DECEMBER 2023

TAS5827 Class-H アルゴリズムを実装した、47W 高効率のステレオ、デジタル入力、閉ループ Class-D アンプ

1 特長

- 複数の出力構成をサポート
  - BTL モードで 2 × 57W (6Ω、25V、THD+N = 10%)
  - BTL モードで 2 × 55W (4Ω、21V、THD+N = 10%)
  - BTL モードで 2 × 47W (6Ω、25V、THD+N = 1%)
  - BTL モードで 2 × 45W (4Ω、21V、THD+N = 1%)
  - PBTL モードで 1 × 112W (3Ω、25V、THD+N = 10%)
  - PBTL モードで 1 × 94W (3Ω、25V、THD+N = 1%)
- 柔軟なオーディオ I/O:
  - 32、44.1、48、88.2、96、192kHz のサンプル レートをサポート
  - I²S、LJ、RJ、4～16 チャネル TDM 入力
  - SDOUT によるオーディオ モニタ、サブチャネル、エコー キャンセル
  - 3 線式のデジタル オーディオ インターフェイスをサポート (MCLK 不要)
- 高効率 Class-D 変調
  - 90% を超える電力効率、70mΩ の $R_{DS}on$
- 優れたオーディオ性能:
  - THD+N ≤ 0.03% (1W、1kHz、PVDD = 12V)
  - SNR ≥ 110dB (A-weighted)、ICN ≤ 40μVrms
- 柔軟な処理機能
  - 3 バンドの高度な DRC + 2 EQ + AGL + 2 EQ
  - チャネルごとに 12 の BQ、レベル メーター
  - 96kHz、192kHz のプロセッサ サンプリング
  - ミキサ、ボリューム、動的 EQ、出力クロスバー
  - PVDD センシングと Class-H アルゴリズム オーディオ信号トラッキング
- 柔軟な電源構成
  - PVDD:4.5V～26.4V
  - DVDD および I/O:1.8V または 3.3V
- 優れた自己保護機能を内蔵:
  - 過電流エラー (OCE)
  - サイクルごとの電流制限は、4 つの選択可能な OC レベルをサポート
  - 過熱警告 (OTW)
  - 過熱エラー (OTE)
  - 低電圧 / 過電圧誤動作防止 (UVLO/OVLO)
  - PVDD 電圧降下検出
- システム統合が簡単
  - I²C ソフトウェア制御 (TAS5827 は、高速モードと高速モード プラスの両方をサポート) またはハードウェア モード
  - 開ループ デバイスと比べて少ない受動部品数

2 アプリケーション

- バッテリ駆動スピーカー
- ワイヤレス Bluetooth スピーカー
- サウンドバーとサブウーファー
- スマート スピーカ

3 概要

TAS5827 は高性能のステレオ、閉ループの Class-D アンプで、オーディオ プロセッサと最高 192kHz のオーディオ サポートが内蔵されています。

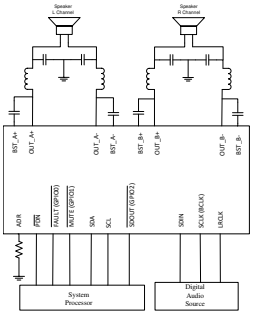
ソフトウェア制御モードで起動すると、TAS5827 は従来の BQ、3 バンド DRC、AGL だけでなく、独自のオーディオ エンベロープ トラッキング Class-H 制御アルゴリズムも実装しています。Class-H アルゴリズムは、必要なオーディオ電力の需要を検出し、GPIO ピンにより DC-DC コンバータに PWM 形式の制御信号を出力します。TAS5827 は、BTL モードで最大 5ms、PBTL モードで最大 10ms の遅延バッファをサポートしており、Class-H 制御はシステム効率の向上に大きく役立ちます。

デバイスをハードウェア制御モードに設定する場合、TAS5827 は、ピン設定によるスイッチング周波数、アナログ ゲイン、BTL/PBTL モード、サイクル単位の電流制限スレッショルドの選択をサポートしています。このモードは、エンド システムのソフトウェア ドライバの統合に手間がかからないように設計されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TAS5827	VQFN (32) RHB	5.00mm × 5.00mm

(1) 利用可能なパッケージについては、データシートの末尾にある注文情報を参照してください。



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4 Pin Configuration and Functions

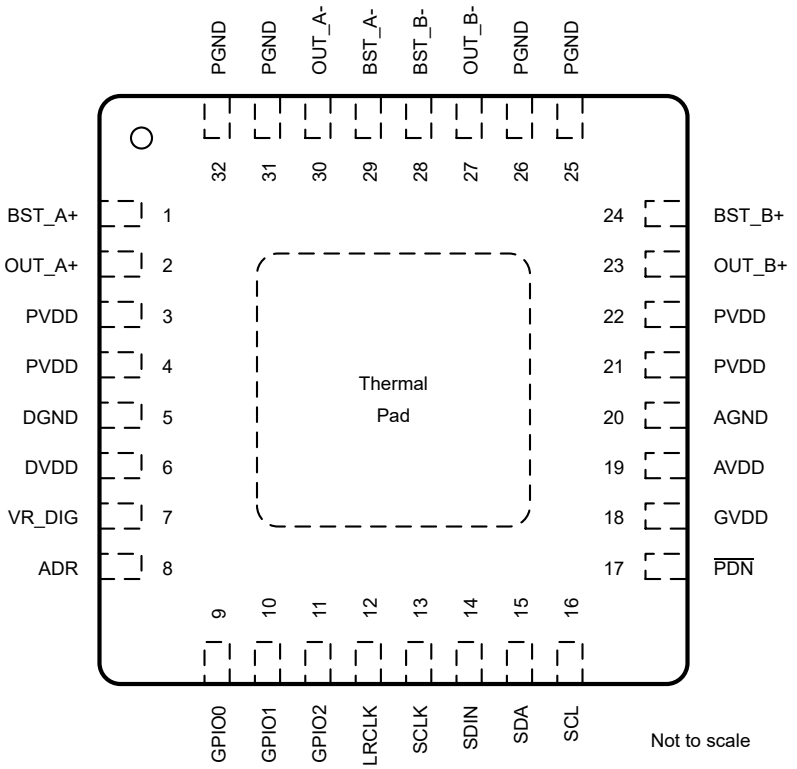


図 4-1. RHB (VQFN) Package, 32-Pin PadDown, Software Mode, Top View

表 4-1. Pin Functions - Software Mode

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ADR	8	DI	A table of resistor value (Pull down to GND) decides the device I2C address. See 表 6-5.
AGND	20	G	Analog ground.
AVDD	19	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices.
BST_A+	1	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
BST_A-	29	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B+	24	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
BST_B-	28	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.

表 4-1. Pin Functions - Software Mode (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DGND	5	G	Digital ground.
DVDD	6	P	3.3-V or 1.8-V digital power supply.
GPIO0	9	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x61h). Can be configured to be open drain output or push-pull output.
GPIO1	10	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x62h). Can be configured to be open drain output or push-pull output.
GPIO2	11	DI/O	General-purpose input/output, function of this pin can be programmed by register (Register Address 0x60h and 0x63h). Can be configured to be open drain output or push-pull output.
LRCLK	12	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
OUT_A+	2	PO	Positive pin for differential speaker amplifier output A.
OUT_A-	30	NO	Negative pin for differential speaker amplifier output A.
OUT_B+	23	PO	Positive pin for differential speaker amplifier output B.
OUT_B-	27	NO	Negative pin for differential speaker amplifier output B.
$\overline{PDN}$	17	DI	Power down, active-low. $\overline{PDN}$ place the amplifier in Shutdown, turn off all internal regulators.
PGND	25	G	Ground reference for power device circuitry. Connect this pin to system ground.
	26	G	
	31	G	
	32	G	
PVDD	3	P	PVDD voltage input.
	4	P	
	21	P	
	22	P	
SDA	15	DI/O	I^2C serial control data interface input/output.
SDIN	14	DI	Data line to the serial data port.
SCL	16	DI	I^2C serial control clock input.
SCLK	13	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
VR_DIG	7	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices.
PowerPAD™		G	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0 V)

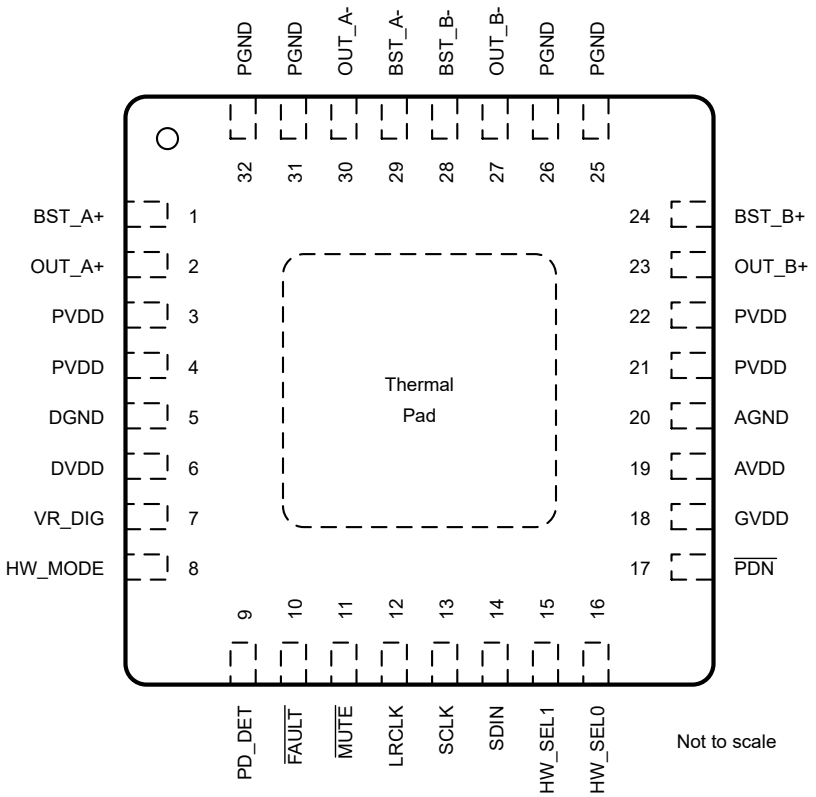


図 4-2. RHB (VQFN) Package, 32-Pin PadDown, Hardware Mode,Top View

表 4-2. Pin Functions - Hardware Mode

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	20	G	Analog ground.
AVDD	19	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices.
BST_A+	1	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+.
BST_A-	29	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-.
BST_B+	24	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+.
BST_B-	28	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-.
DGND	5	G	Digital ground.
DVDD	6	P	3.3-V or 1.8-V digital power supply.
$\overline{\text{FAULT}}$	10	DO	Fault terminal,which is pulled LOW when an internal fault occurs.
GVDD	18	P	Gate drive internal regulator output. This pin must not be used to drive external devices.
HW_MODE	8	DI	Connect to DVDD directly to ensure device enter into Hardware Control Mode.
HW_SEL0	16	DI	Analog gain and BTL/PBTL mode selection in Hardware Mode . Pull up to DVDD or Pull down to ground with different resistor. See 表 6-4.
HW_SEL1	15	DI	PWM Switching Frequency and Spread Spectrum Enable/Disable selection in Hardware Mode. Pull up to DVDD or Pull down to ground with different resistor. See 表 6-3.

表 4-2. Pin Functions - Hardware Mode (続き)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LRCLK	12	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
$\overline{\text{MUTE}}$	11	DI	Speaker amplifier Mute. Which must be pulled low (connect to DGND) to MUTE the device and pulled high (connected to DVDD) to exit MUTE state. In Mute state, device output keep in Hi-Z state.
OUT_A+	2	PO	Positive pin for differential speaker amplifier output A.
OUT_A-	30	NO	Negative pin for differential speaker amplifier output A.
OUT_B+	23	PO	Positive pin for differential speaker amplifier output B.
OUT_B-	27	NO	Negative pin for differential speaker amplifier output B.
PD_DET	9	DO	PVDD Drop detection, which is pulled LOW when the PVDD drop below 8V.
$\overline{\text{PDN}}$	17	DI	Power down, active-low. $\overline{\text{PDN}}$ place the amplifier in Shutdown, turn off all internal regulators.
PGND	25	G	Ground reference for power device circuitry. Connect this pin to system ground.
	26	G	
	31	G	
	32	G	
PVDD	3	P	PVDD voltage input.
	4	P	
	21	P	
	22	P	
SCLK	13	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
SDIN	14	DI	Data line to the serial data port.
VR_DIG	7	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices.
PowerPAD™		G	Ground, connect to grounded heat sink for best system performance.

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), PO = Positive output, NO = Negative output, P = Power, G = Ground (0 V)

5 Specifications

5.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature	–40	85	°C
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, $\overline{\text{PDN}}$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002.(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	PVDD	4.5		26.4	V
		DVDD	1.62		3.63	V
R_{SPK}	Minimum Speaker Load	4.5V-24V Operating PVDD Range, BTL Mode	3.2			Ω
		4.5V-24V Operating PVDD Range, PBTL Mode	1.6			Ω
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs		0.9 × V_{DVDD}		DVDD	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs				0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			µH

5.4 Thermal Information

THERMAL METRIC(1)		TAS5827 - VQFN32 (RHB) - 32 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
$R_{\theta JA(top)}$	Junction-to-ambient thermal resistance	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.5	°C/W
$R_{\theta JB(top)}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = V_{DVDD}			10	uA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = 0 V			–10	uA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4 mA			20%	V_{DVDD}
I^2C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, support both fast & fast plus mode		400	1000	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
AMPLIFIER OPERATING MODE AND DC PRAMETERS						
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V, Play mode, General Audio Process flow with full DSP running		23		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V,Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 2 V, DVDD = 3.3 V,Deep Sleep mode		1		mA
I_{CC}	Quiescent supply current of DVDD	$\overline{PDN}$ = 0.8 V, DVDD = 3.3 V,Shutdown mode		16		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 18 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, 1SPW Modulation, Play Mode		39		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 18 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Output Hi-Z Mode		11		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 18 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Sleep Mode		7.5		mA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 18 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Deep Sleep Mode		10		uA
I_{CC}	Quiescent supply current of PVDD	$\overline{PDN}$ = 2 V, PVDD = 18 V, No Load, LC filter = 10 µH + 0.68 µF, FSW = 384 kHz, Shutdown Mode		10		uA
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD Measured at 0 dB input(1FS)	13.75		29.4	dBV
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 26.4 dBV		0.5		dB

5.5 Electrical Characteristics (続き)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPK_AMP}	Switching frequency of the speaker amplifier.	Software Mode		384		kHz
				480		kHz
				576		kHz
				768		kHz
				1024		kHz
		Hardware Mode		480		kHz
				768		kHz
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD}=24 V, $I_{(OUT)}$=500 mA, T_J=25 ℃		70		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold (Speaker current)	Speaker Output Current (Post LC filter), Speaker current, LC Filter=10 uH+0.68 uF, BTL Mode	7.5	8	8.5	A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold		3.7	4	4.2	V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold		27	28.1	29.2	V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		3.3		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		570		ms
OTE_{THRES}	Over temperature error threshold			170		℃
$OTE_{Hysteresis}$	Over temperature error hysteresis			10		℃
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit0		106		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit1		130		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit2		140		°C
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit3		154		°C

5.5 Electrical Characteristics (続き)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMACNE (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4 dBV analog gain, V_{PVDD} range:12 V~24 V	–5		5	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 10%		41		W
		V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 1%		33		W
		V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		31		W
		V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		25		W
		V_{PVDD} = 21 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 10%		55		W
		V_{PVDD} = 21 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 4 Ω, f = 1 kHz, THD+N = 1%		45		W
		V_{PVDD} = 25 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 10%		57		W
		V_{PVDD} = 25 V, LC Filter=10 uH+0.68 uF, R_{SPK} = 6 Ω, f = 1 kHz, THD+N = 1%		47		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz)	V_{PVDD} = 18 V,LC Filter=10 uH+0.68 uF, Load=4 Ω		0.05		%
		V_{PVDD} = 25 V,LC Filter=10 uH+0.68 uF,Load=6 Ω		0.03		%
$ICN_{(SPK)}$	Idle channel noise(Aweighted, AES17)	V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, Load=4 Ω, Fsw=576 kHz, BD Modulation		40		µVrms
		V_{PVDD} = 18 V, LC Filter=10 uH+0.68 uF, Load=4 Ω, Fsw=384 kHz, 1SPW Modulation		35		µVrms
		V_{PVDD} = 25 V, LC Filter=10 uH+0.68 uF, Load=6 Ω, Fsw=384kHz, 1SPW Modulation		40		µVrms
		V_{PVDD} = 25 V, LC Filter=3.3 uH+1 uF, Load=6 Ω, Fsw=1024 kHz, BD Modulation		37		µVrms
DR	Dynamic range	A-Weighted, -60 dBFS method. V_{PVDD} = 25 V, Load=6 Ω, Analog Gain = 29.4 dBV		115		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=25 V, load=6 Ω		115		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=18 V, Load=4 Ω		115		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 kHz, 1 Vrms, V_{PVDD} = 25 V, input audio signal = digital zero		85		dB
$Cross\text{-}talk_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 kHz, based on Inductor (SPM10040T-100M) from TDK		100		dB

5.5 Electrical Characteristics (続き)

Free-air room temperature 25°C, 1SPW Mode, LC filter=10uH+0.68uF, Fsw=384kHz, Class D Bandwidth=80kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE (MONO PBTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV Analog gain, V_{PVDD} = 12V-25V range, 1SPW mode	–5		5	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 25 V, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 1%		94		W
		V_{PVDD} = 25 V, R_{SPK} = 3 Ω, f = 1 kHz, THD+N = 10%		112		W
		V_{PVDD} = 18 V, R_{SPK} = 2 Ω, f = 1 kHz, THD+N = 1%		67		W
		V_{PVDD} = 18 V, R_{SPK} = 2 Ω, f = 1 kHz, THD+N = 10%		83		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 kHz)	V_{PVDD} = 18 V, LC-filter=10 uH+0.68 uF, R_{SPK} = 2 Ω		0.07		%
		V_{PVDD} = 25 V, LC-filter=10 uH+0.68 uF, R_{SPK} = 3 Ω		0.05		%
DR	Dynamic range	A-Weighted, -60 dBFS method, V_{PVDD}=25 V, R_{SPK} = 3 Ω.		113		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=25 V, R_{SPK} = 3 Ω		113		dB
		A-Weighted,referenced to 1% THD+N Output Level, V_{PVDD}=18 V, R_{SPK} = 2 Ω		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 kHz, 1 Vrms,V_{PVDD} = 18 V, input audio signal = digital zero		80		dB

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing - Target Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^2C Bus Timing – Fast Mode Plus					
f_{SCL}	SCL clock frequency			1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HI}	High period of the SCL clock	0.26			µs
t_{RS-SU}	Setup time for (repeated) START condition	0.26			µs
t_{S-HD}	Hold time for (repeated) START condition	0.26			µs
t_{D-SU}	Data setup time	50			ns
t_{D-HD}	Data hold time	0			ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		120	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		120	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		120	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		120	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		120	ns
t_{P-SU}	Setup time for STOP condition	0.26			µs
C_b	Capacitive load for each bus line			550	pf
I^2C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_b	Capacitive load for each bus line			400	pf

5.7 Typical Characteristics

5.7.1 Bridge Tied Load (BTL) Configuration Curves with BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576kHz, 175 kHz Class D Amplifier Loop Bandwidth, LC filter with 10µH / 0.68 µF, unless otherwise noted.

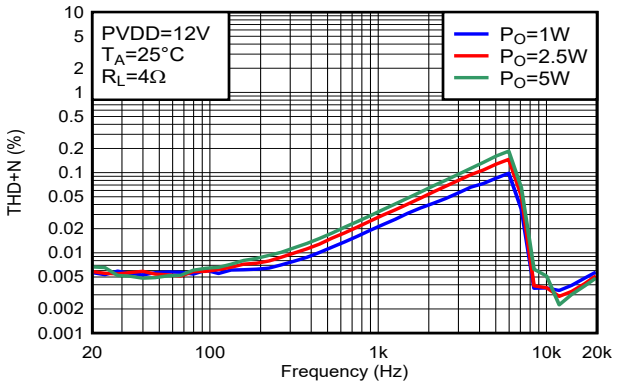


図 5-1. THD+N vs Frequency-BTL

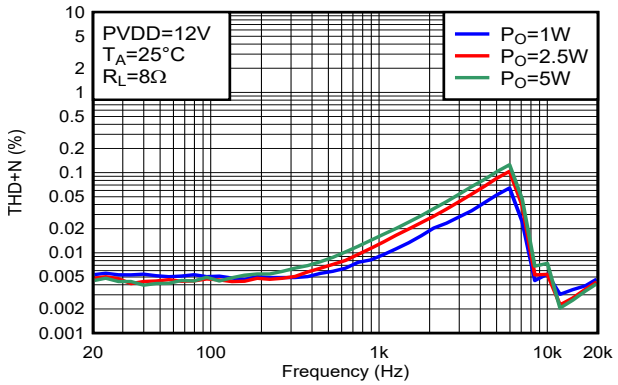


図 5-2. THD+N vs Frequency-BTL

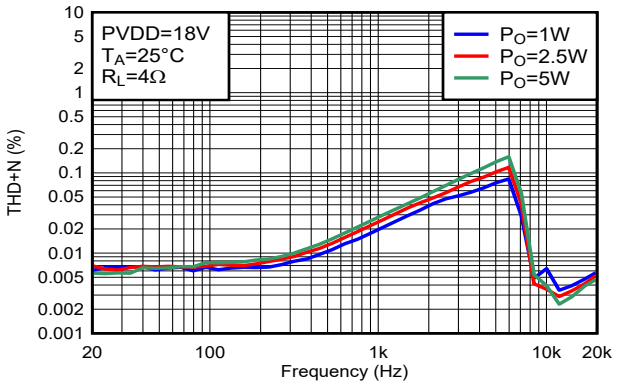


図 5-3. THD+N vs Frequency-BTL

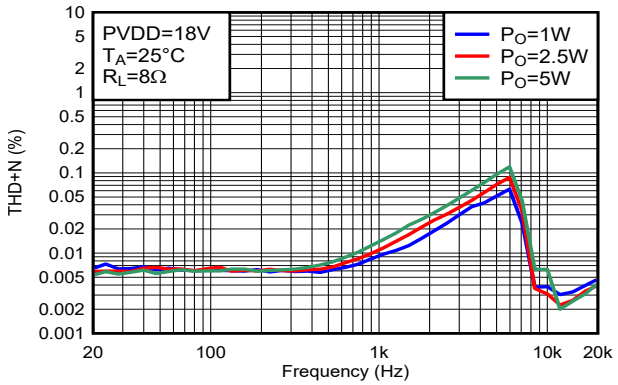


図 5-4. THD+N vs Frequency-BTL

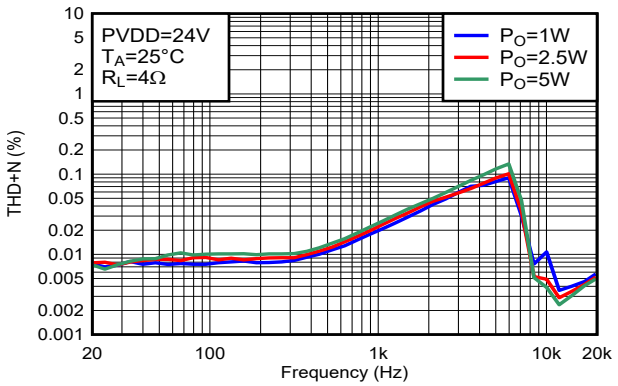


図 5-5. THD+N vs Frequency-BTL

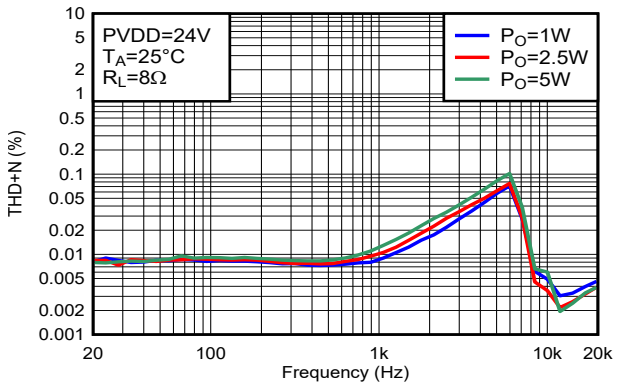


図 5-6. THD+N vs Frequency-BTL

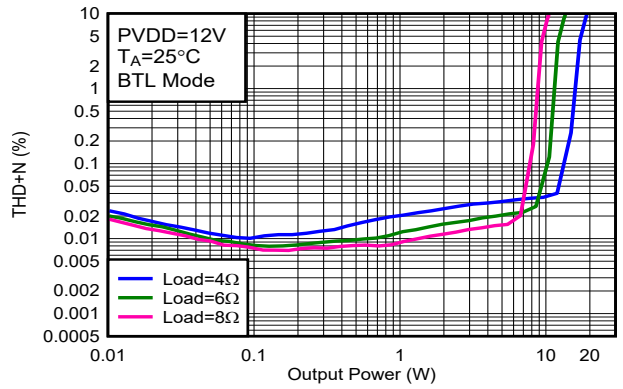


図 5-7. THD+N vs Output Power-BTL

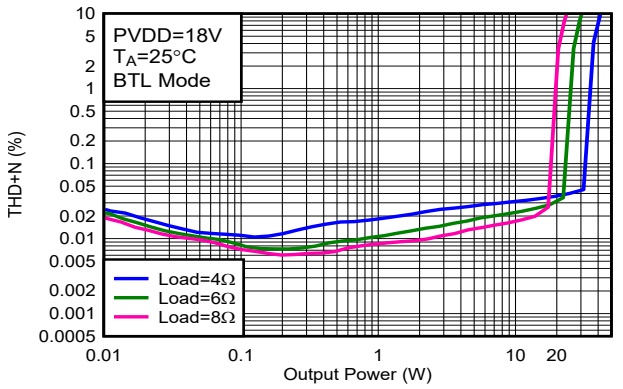


図 5-8. THD+N vs Output Power-BTL

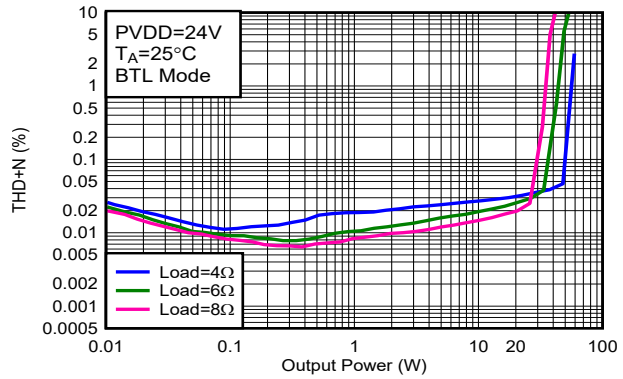
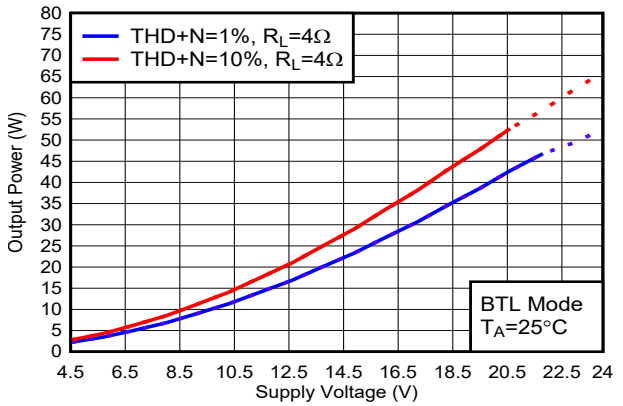


図 5-9. THD+N vs Output Power-BTL



A. Dashed lines represent thermally limited region.

図 5-10. Output Power vs Supply Voltage

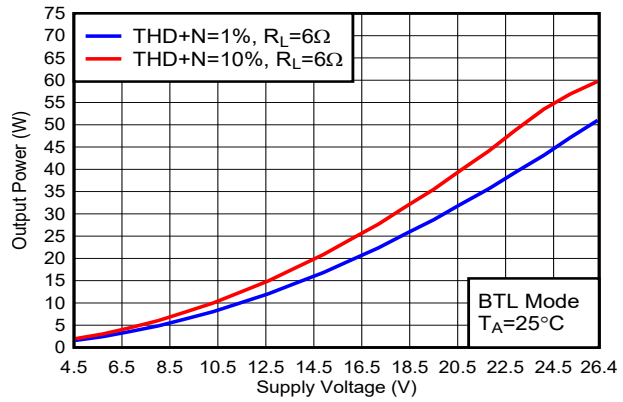


図 5-11. Output Power vs Supply Voltage

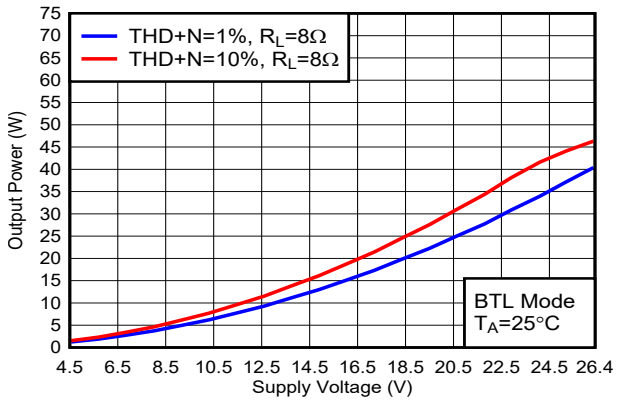
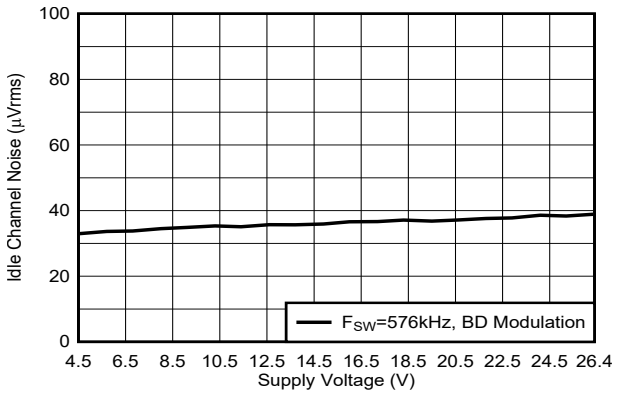
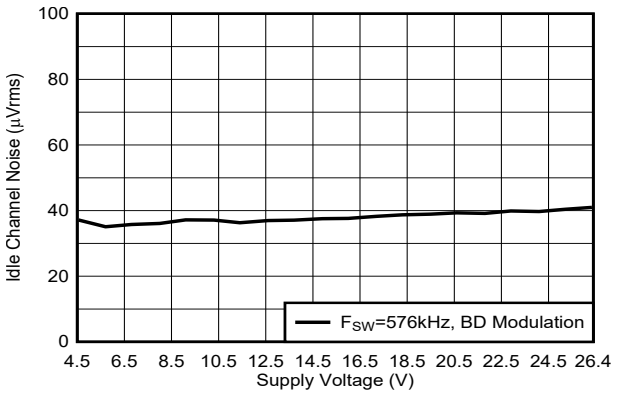


図 5-12. Output Power vs Supply Voltage



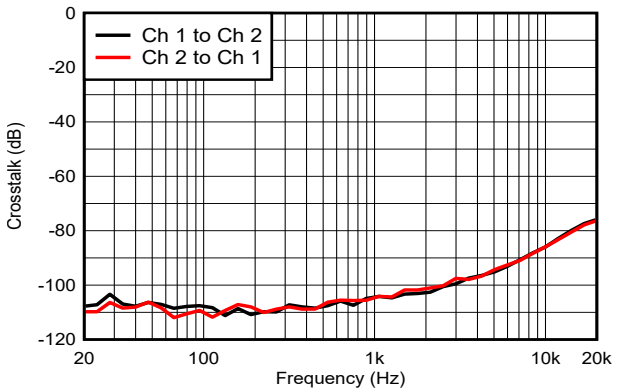
4 Ω Load

図 5-13. Idle Channel Noise vs Supply Voltage



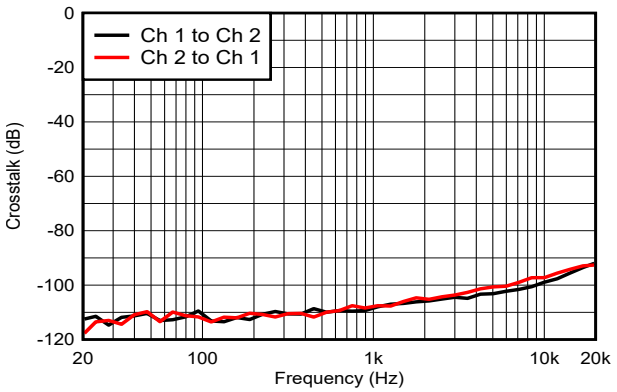
8 Ω Load

図 5-14. Idle Channel Noise vs Supply Voltage



PVDD = 24 V R_L = 4 Ω P_O = 1W

図 5-15. Crosstalk



PVDD = 24 V R_L = 8 Ω P_O = 1W

図 5-16. Crosstalk

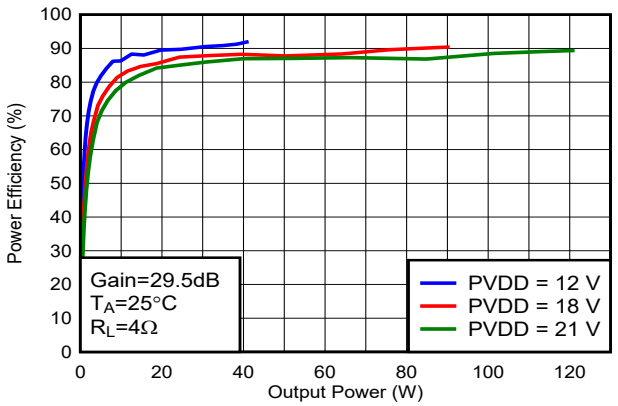


図 5-17. Efficiency vs Output Power

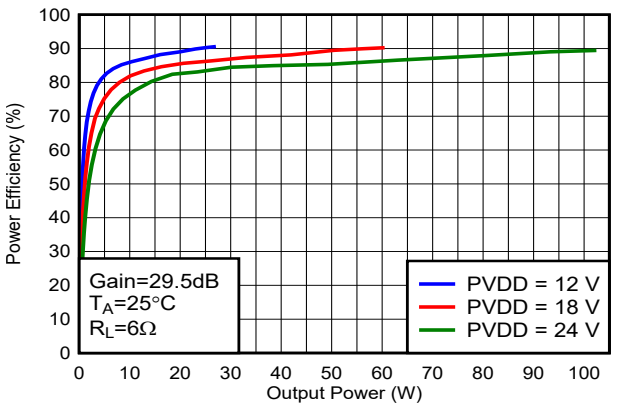


図 5-18. Efficiency vs Output Power

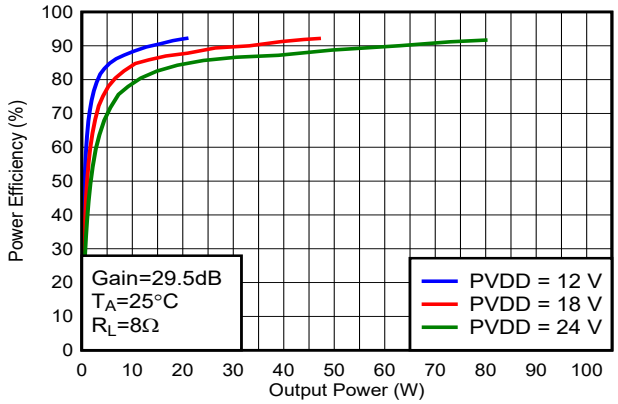


図 5-19. Efficiency vs Output Power

5.7.2 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, 80 kHz Class D Loop Bandwidth, the LC filter used was 10 µH / 0.68 µF, unless otherwise noted.

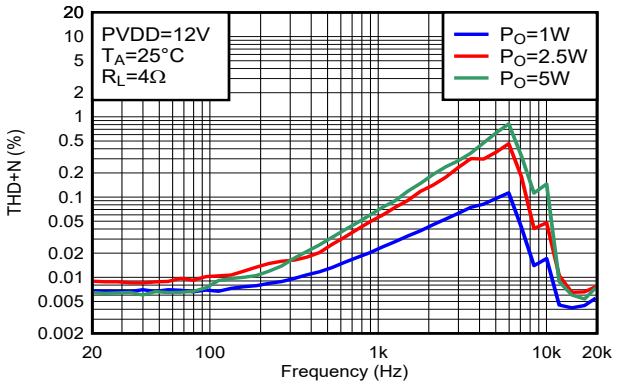


図 5-20. THD+N vs Frequency-BTL

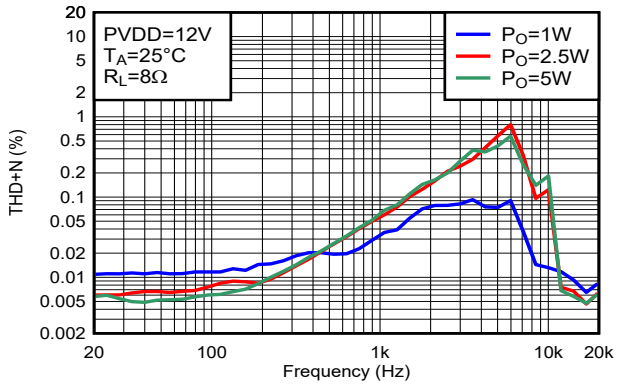


図 5-21. THD+N vs Frequency-BTL

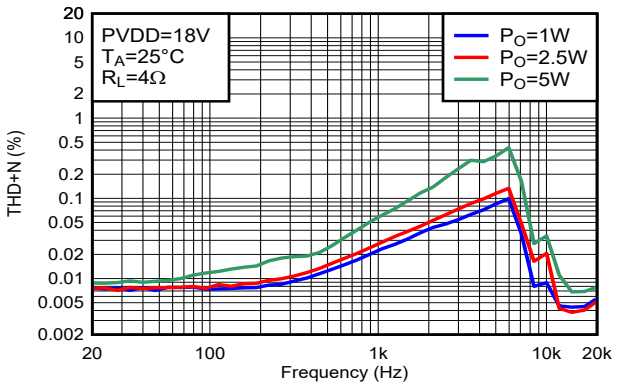


図 5-22. THD+N vs Frequency-BTL

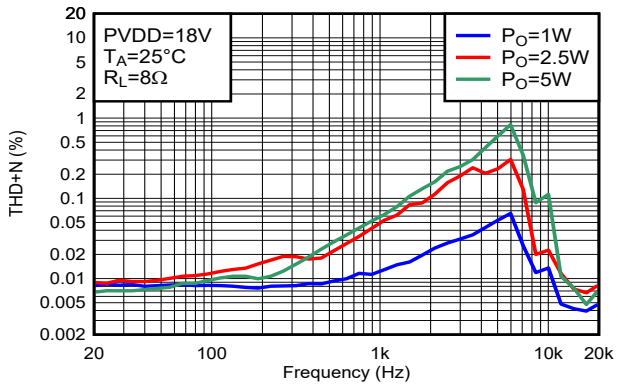


図 5-23. THD+N vs Frequency-BTL

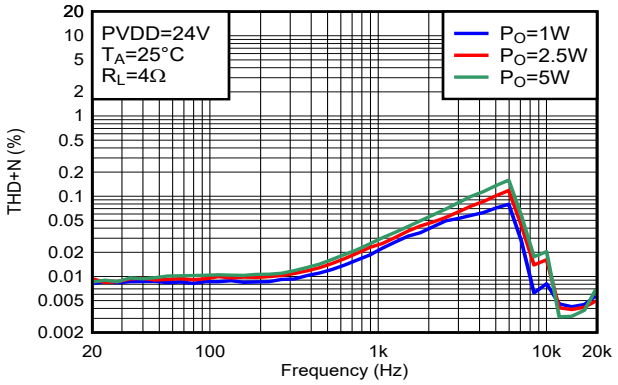


図 5-24. THD+N vs Frequency-BTL

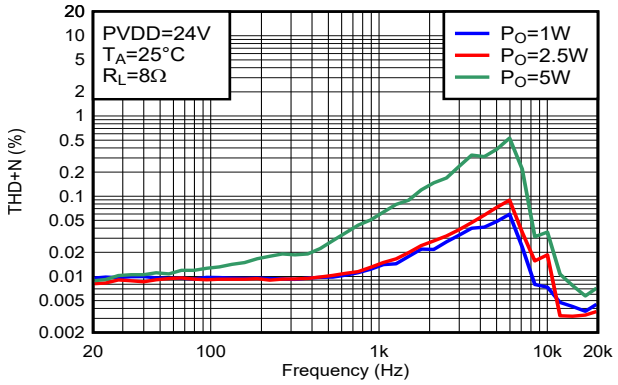


図 5-25. THD+N vs Frequency-BTL

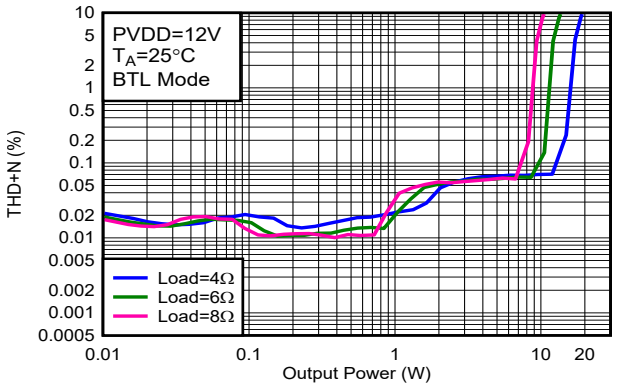


図 5-26. THD+N vs Output Power-BTL

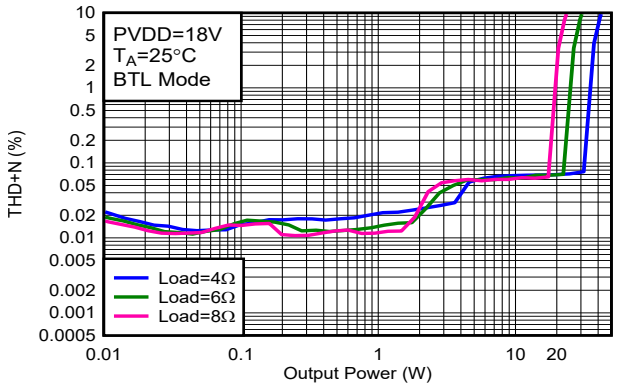


図 5-27. THD+N vs Output Power-BTL

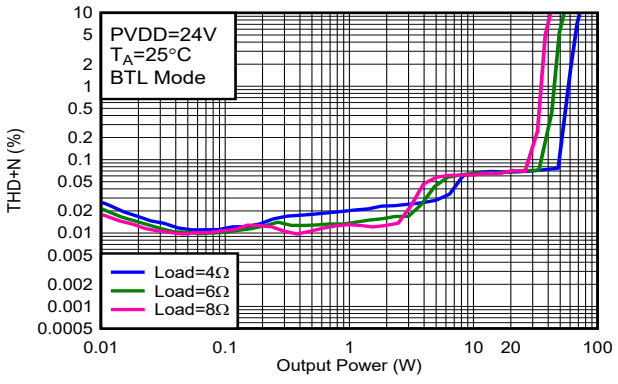


図 5-28. THD+N vs Output Power-BTL

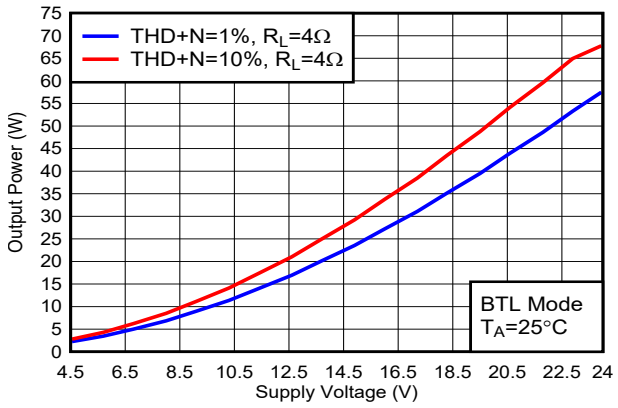


図 5-29. Output Power vs Supply Voltage

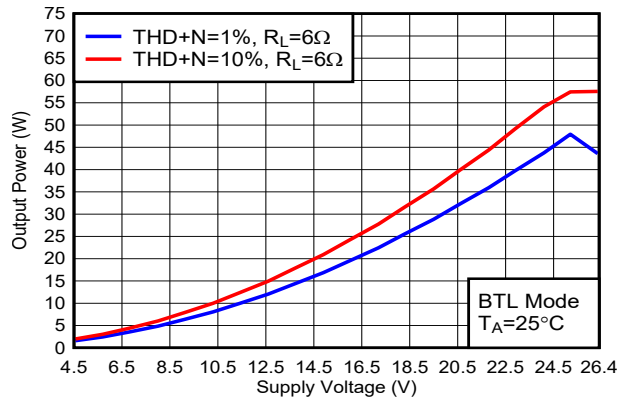


図 5-30. Output Power vs Supply Voltage

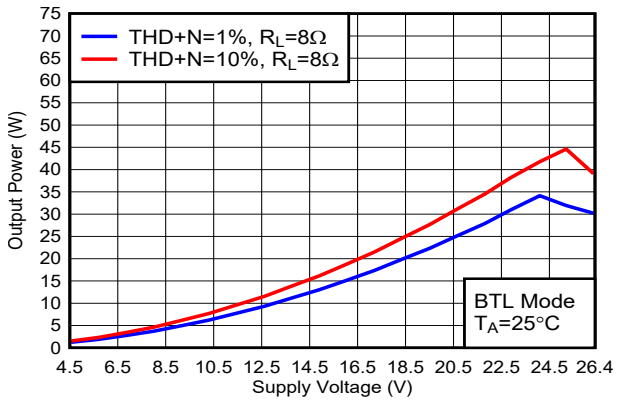
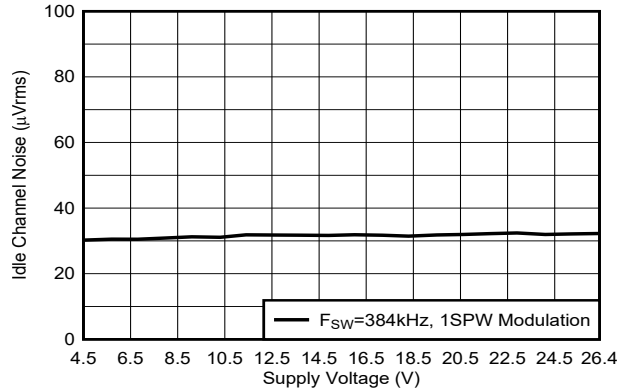
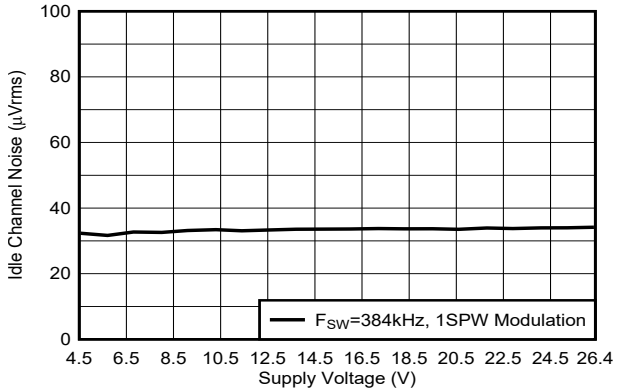


図 5-31. Output Power vs Supply Voltage



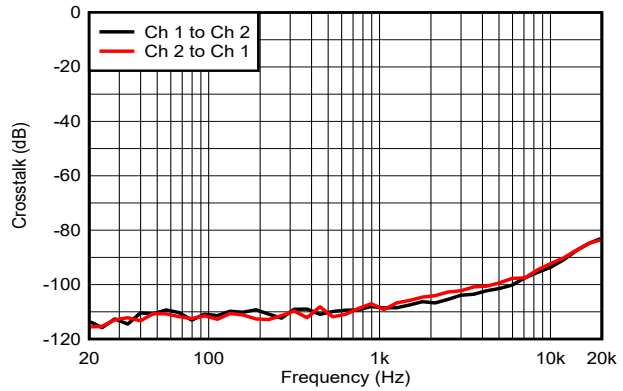
4 Ω Load

図 5-32. Idle Channel Noise vs Supply Voltage



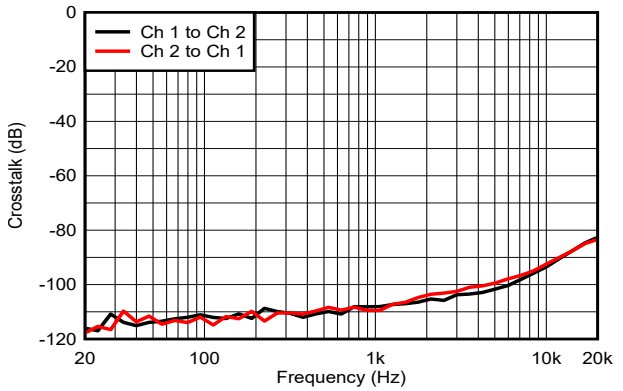
8 Ω Load

図 5-33. Idle Channel Noise vs Supply Voltage



PVDD = 24 V R_L = 4 Ω P_O = 1W

図 5-34. Crosstalk



PVDD = 24 V R_L = 8 Ω P_O = 1W

図 5-35. Crosstalk

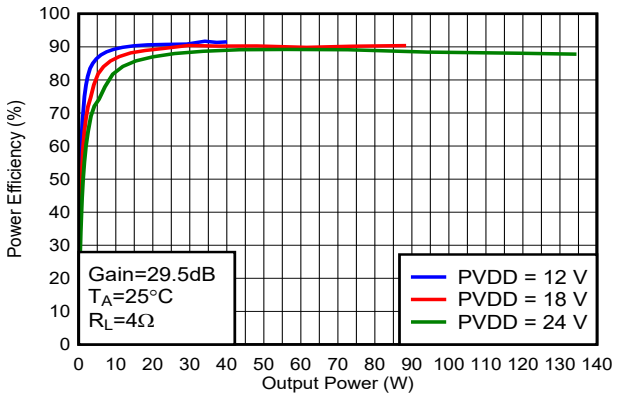


図 5-36. Efficiency vs Output Power

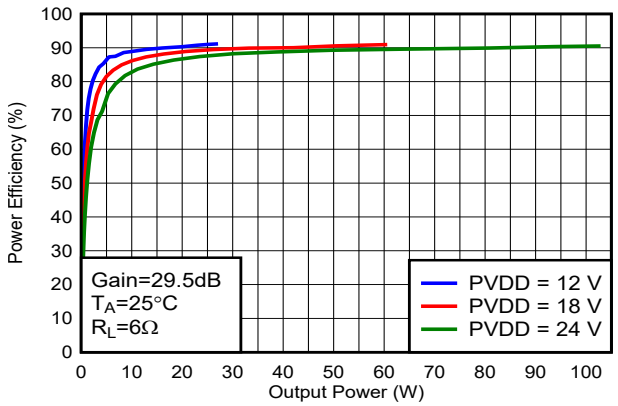


図 5-37. Efficiency vs Output Power

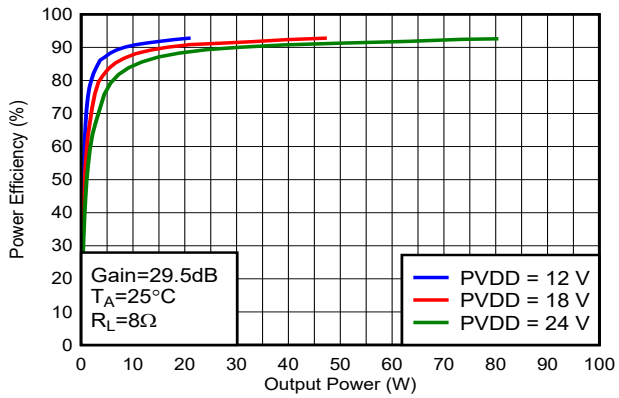


図 5-38. Efficiency vs Output Power

5.7.3 Parallel Bridge Tied Load (PBTL) Configuration With BD Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 576 kHz, 175 kHz Class D Amplifier Loop Bandwidth, LC filter with 10 µH / 0.68 µF（Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see details in セクション 7.1.2）, unless otherwise noted.

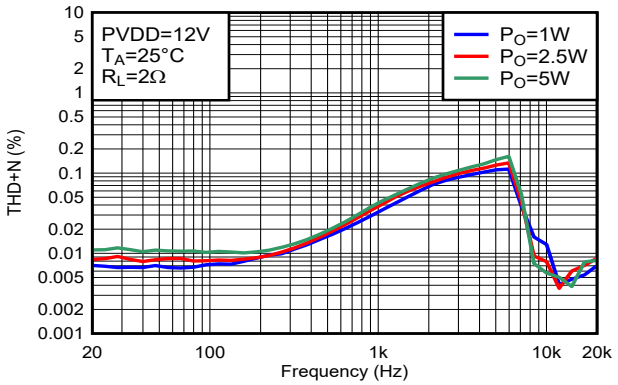


図 5-39. THD+N vs Frequency-PBTL

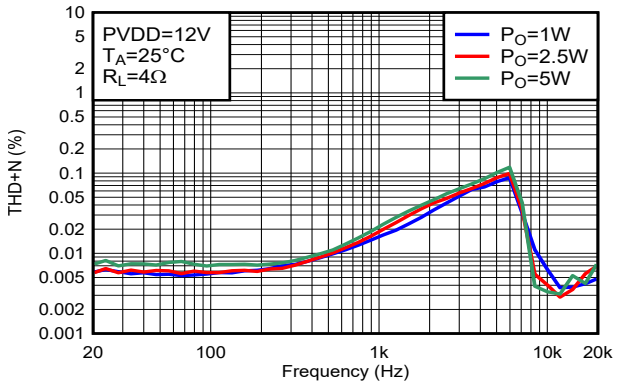


図 5-40. THD+N vs Frequency-PBTL

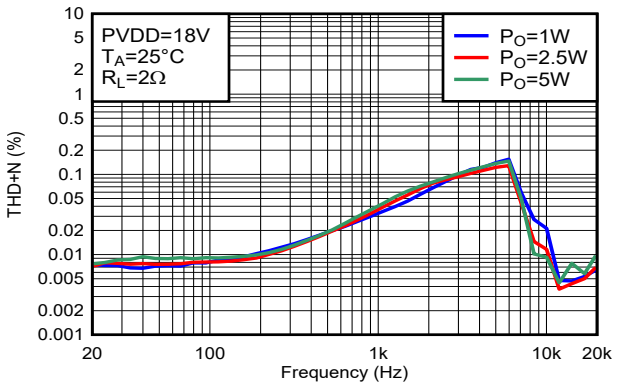


図 5-41. THD+N vs Frequency-PBTL

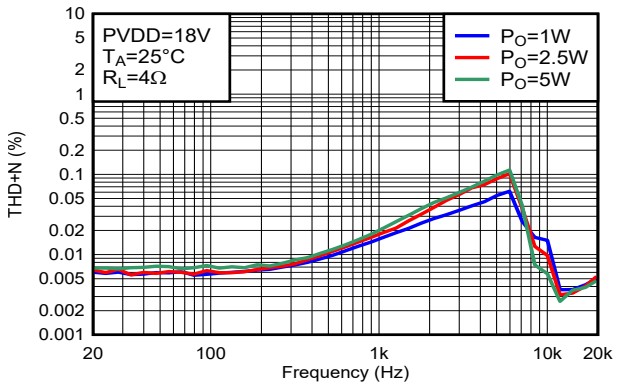


図 5-42. THD+N vs Frequency-PBTL

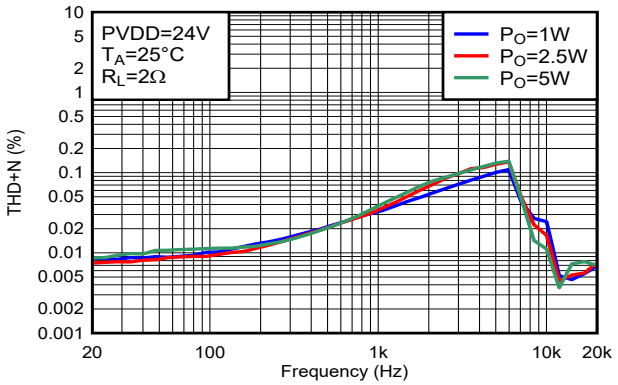


図 5-43. THD+N vs Frequency-PBTL

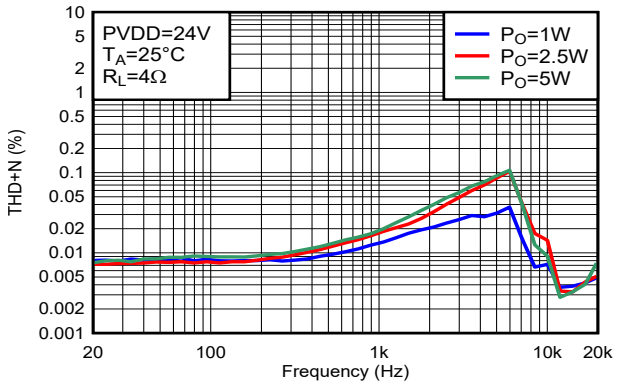


図 5-44. THD+N vs Frequency-PBTL

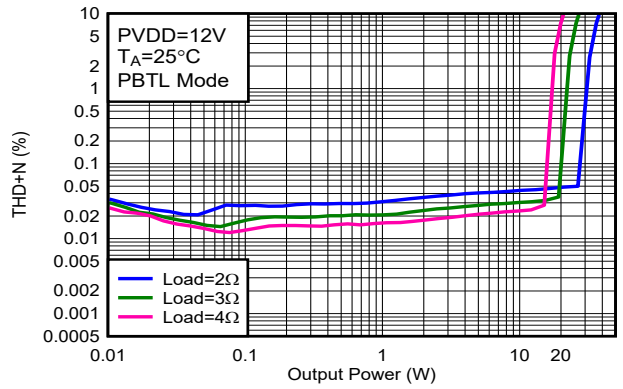


図 5-45. THD+N vs Output Power-PBTL

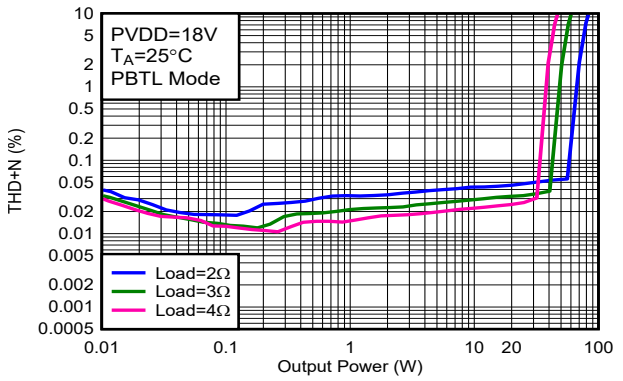


図 5-46. THD+N vs Output Power-PBTL

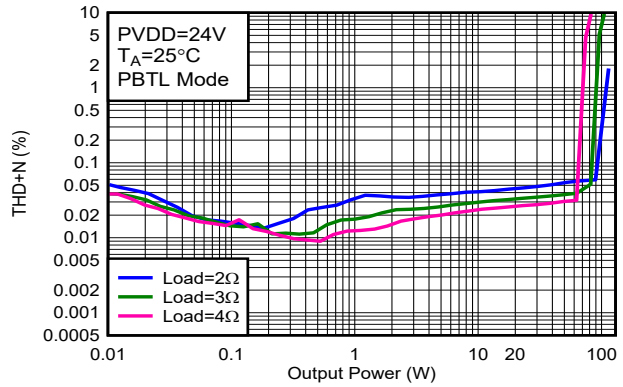
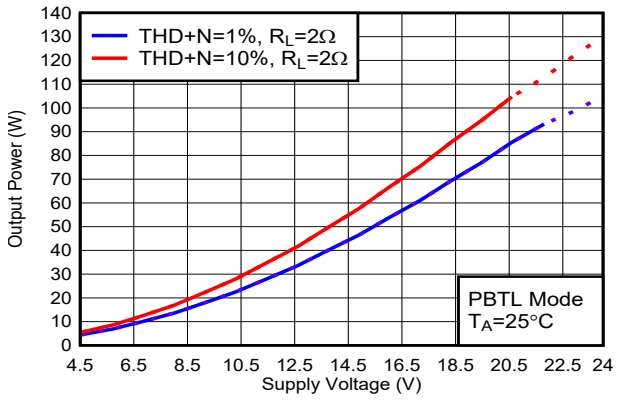


図 5-47. THD+N vs Output Power-PBTL



Dashed lines represent thermally limited region.

図 5-48. Output Power vs Supply Voltage

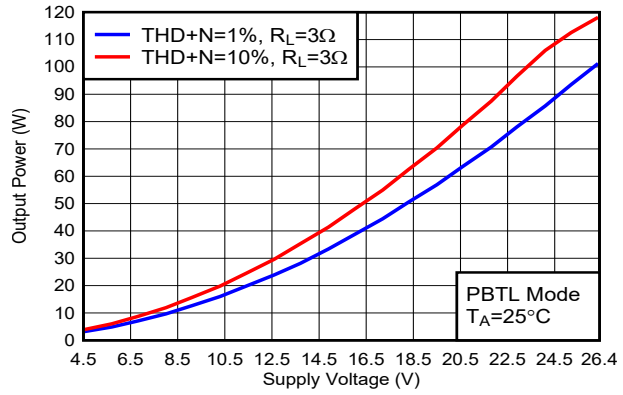


図 5-49. Output Power vs Supply Voltage

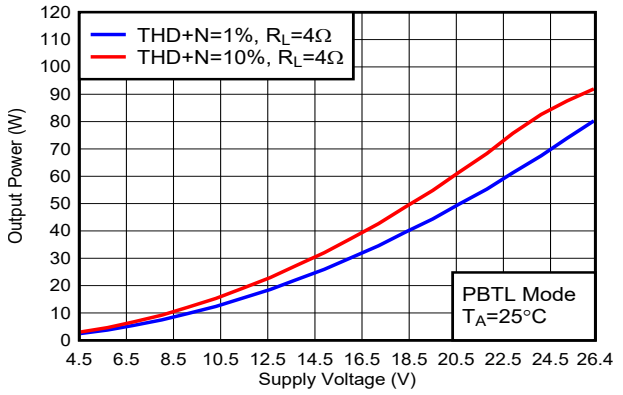
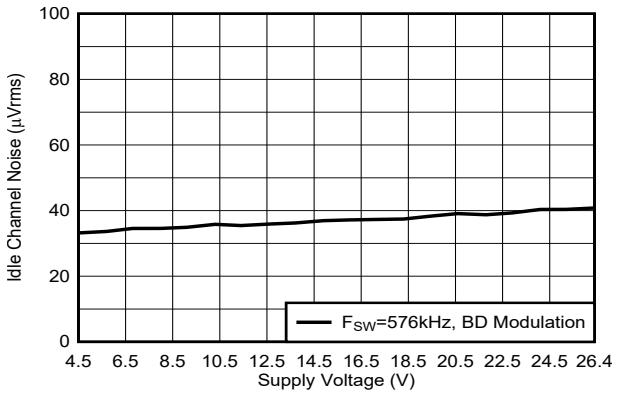
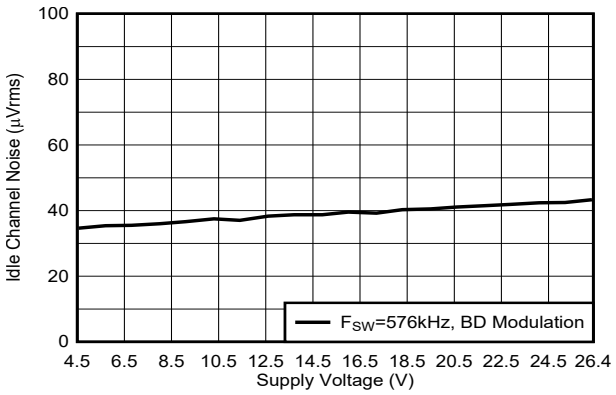


図 5-50. Output Power vs Supply Voltage



2 Ω Load

図 5-51. Idle Channel Noise vs Supply Voltage



4 Ω Load

図 5-52. Idle Channel Noise vs Supply Voltage

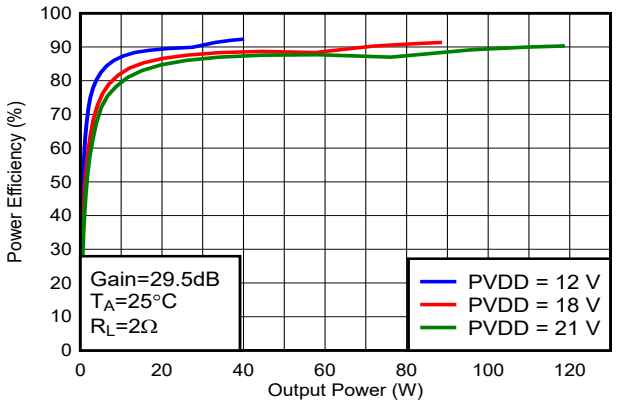


図 5-53. Efficiency vs Output Power

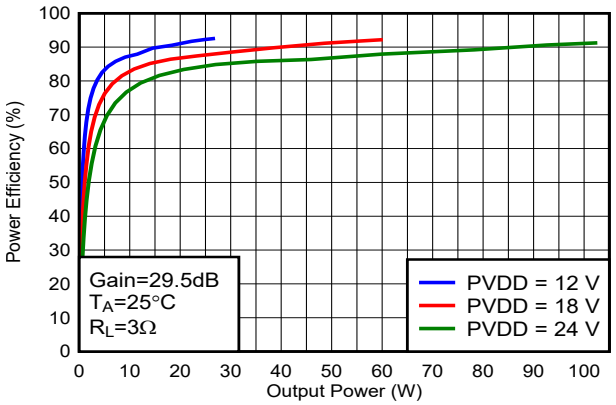


図 5-54. Efficiency vs Output Power

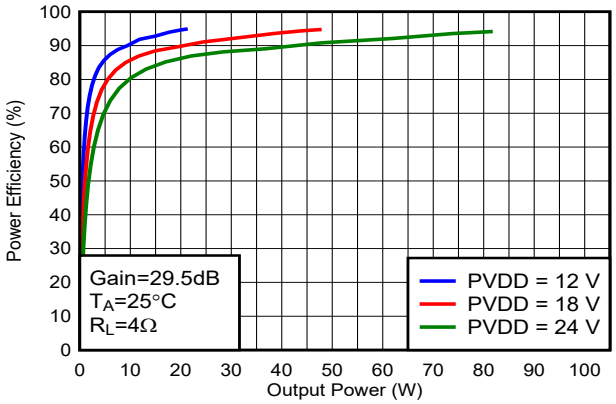


図 5-55. Efficiency vs Output Power

5.7.4 Parallel Bridge Tied Load (PBTL) Configuration With 1SPW Modulation

Free-air room temperature 25°C (unless otherwise noted). Measurements were made using Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 384 kHz, 80 kHz Class D Amplifier Loop Bandwidth, the LC filter used was 10 µH / 0.68 µF（Post-Filter PBTL, the merging of the two output channels after the inductor portion of the output filter, see connect method in セクション 7.1.2）, unless otherwise noted.

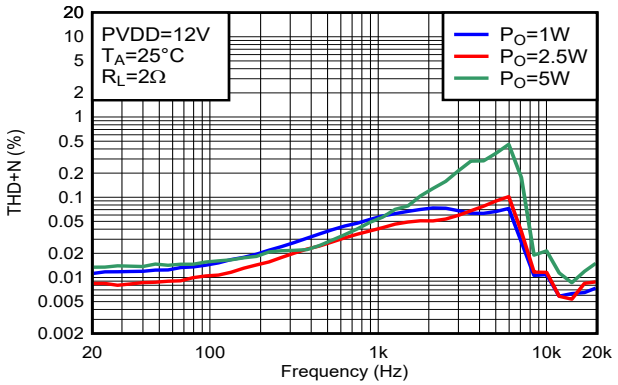


図 5-56. THD+N vs Frequency-PBTL

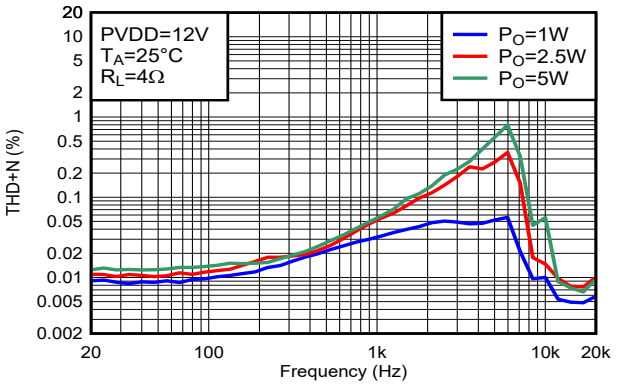


図 5-57. THD+N vs Frequency-PBTL

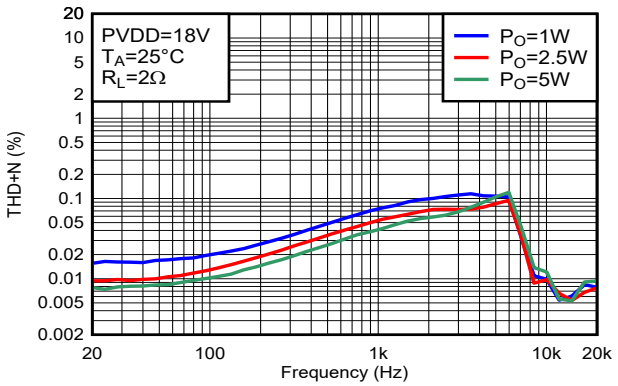


図 5-58. THD+N vs Frequency-PBTL

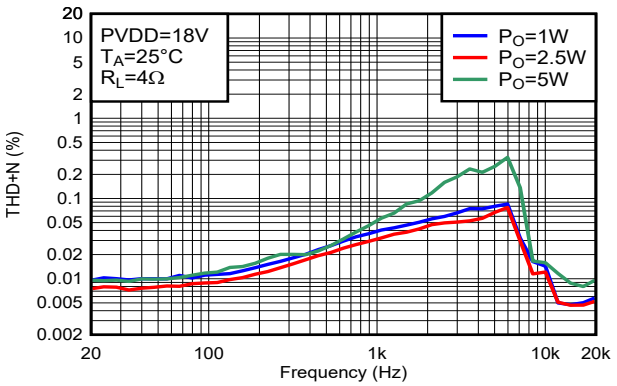


図 5-59. THD+N vs Frequency-PBTL

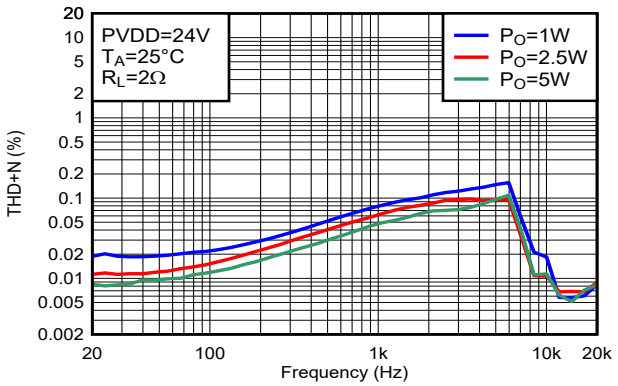


図 5-60. THD+N vs Frequency-PBTL

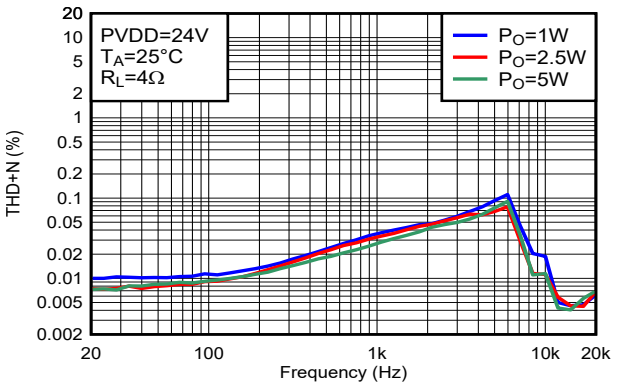


図 5-61. THD+N vs Frequency-PBTL

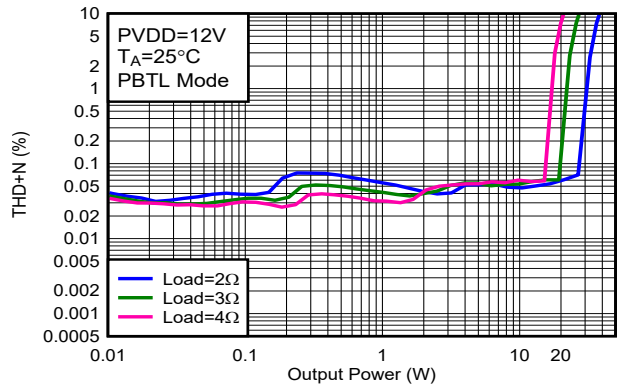


図 5-62. THD+N vs Output Power-PBTL

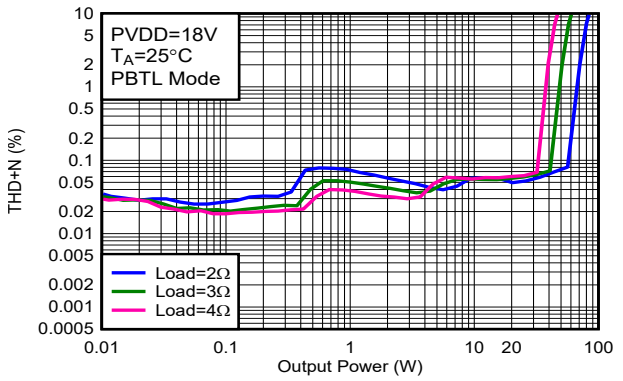


図 5-63. THD+N vs Output Power-PBTL

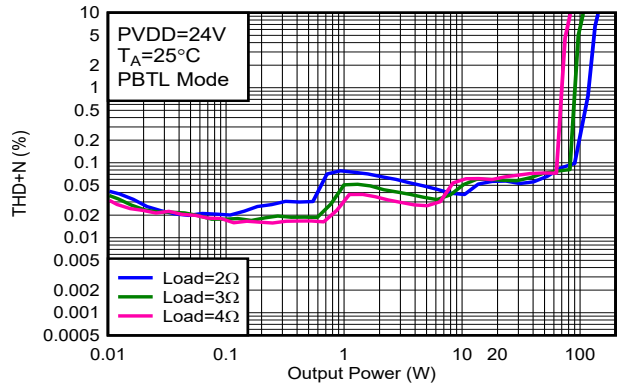


図 5-64. THD+N vs Output Power-PBTL

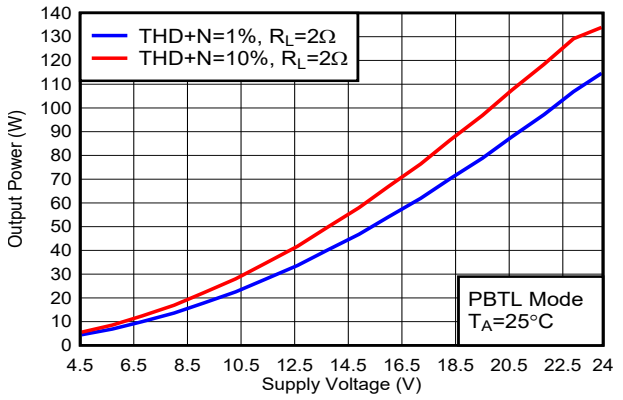


図 5-65. Output Power vs Supply Voltage

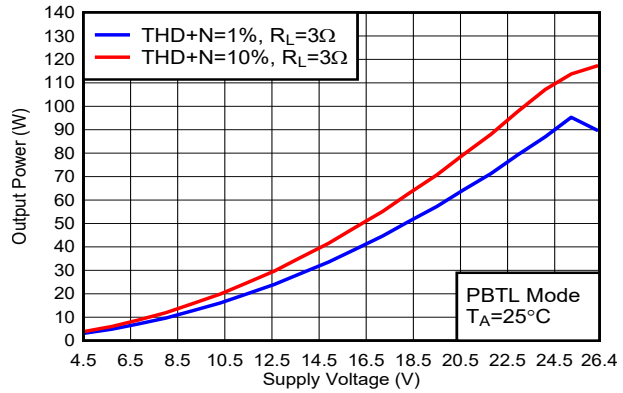


図 5-66. Output Power vs Supply Voltage

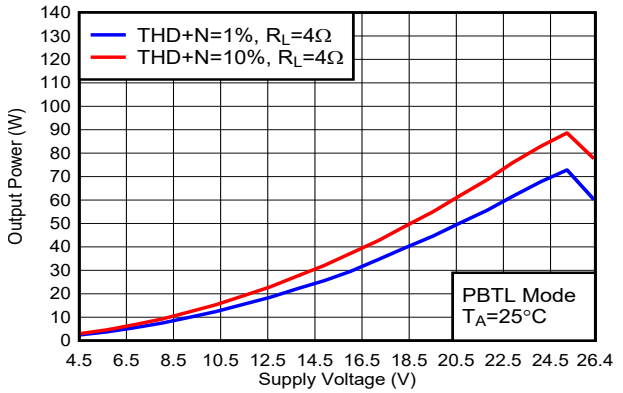
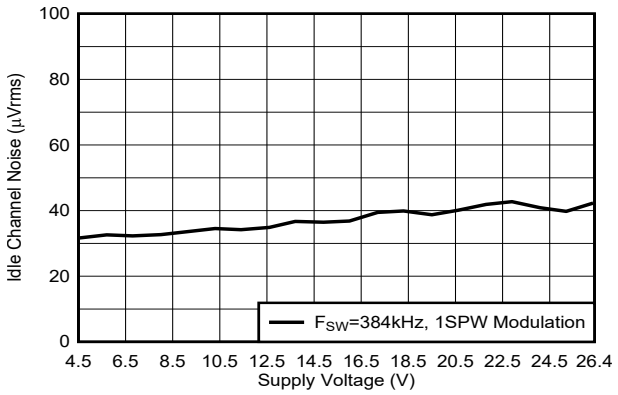
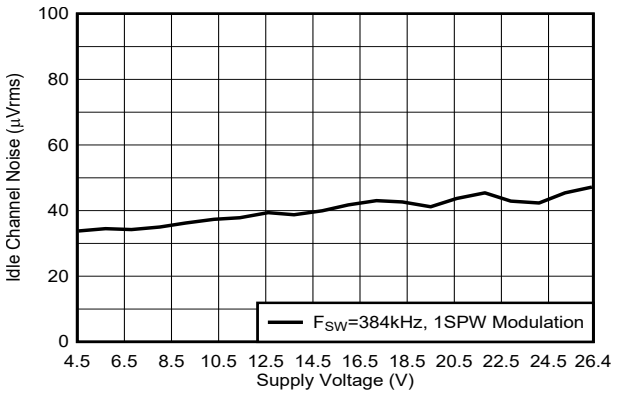


図 5-67. Output Power vs Supply Voltage



2 Ω Load

図 5-68. Idle Channel Noise vs Supply Voltage



4 Ω Load

図 5-69. Idle Channel Noise vs Supply Voltage

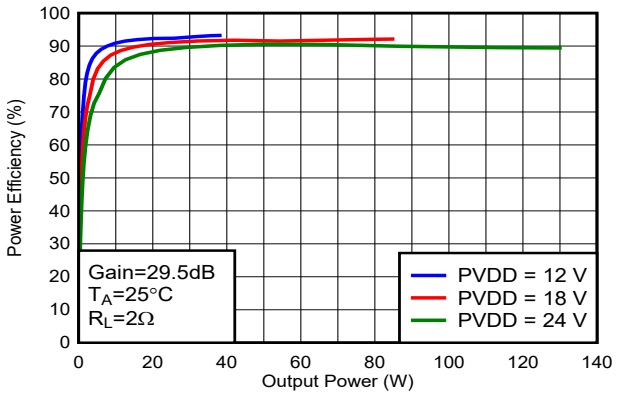


図 5-70. Efficiency vs Output Power

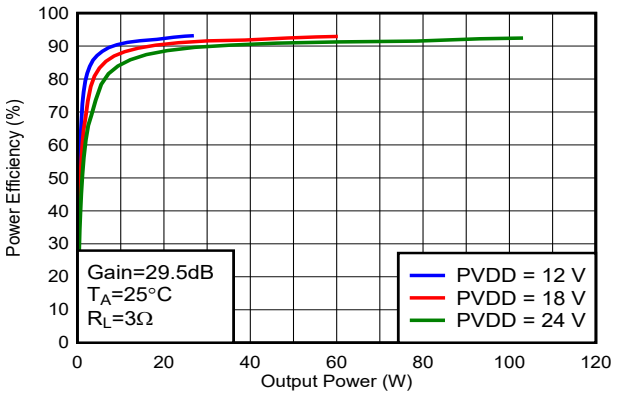


図 5-71. Efficiency vs Output Power

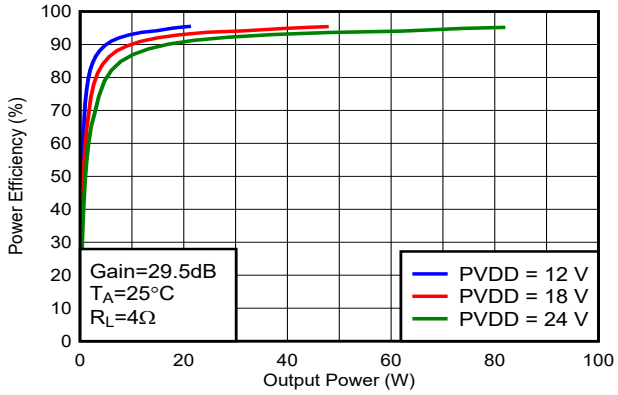


図 5-72. Efficiency vs Output Power

6 Detailed Description

6.1 Overview

The TAS5827 device combines 4 main building blocks into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo digital to PWM modulator, then PWM modulator to power stage.
- An Audio DSP subsystem.
- A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low-voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. Two internal LDOs convert PVDD to 5 V for GVDD and AVDD, One internal LDO converts DVDD to 1.5 V for VR_DIG.

6.2 Functional Block Diagram

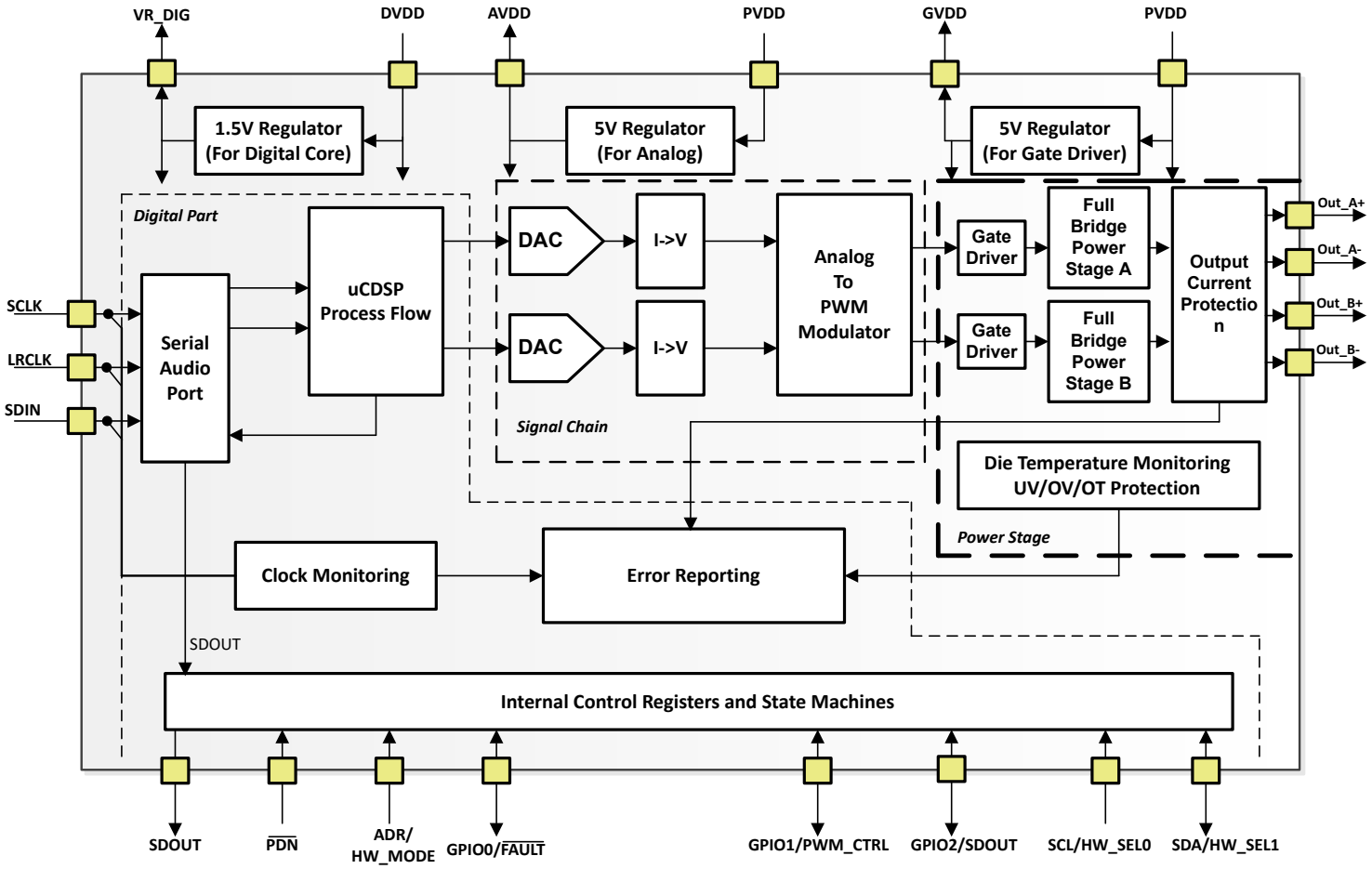


図 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Power Supplies

For system design, TAS5827 needs a 3.3-V or 1.8-V supply in addition to the (typical) 12-V or 24-V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. To provide good electrical

and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (GVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

6.3.2 Device Clocking

The TAS5827 devices have flexible systems for clocking. Internally, the device requires several clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

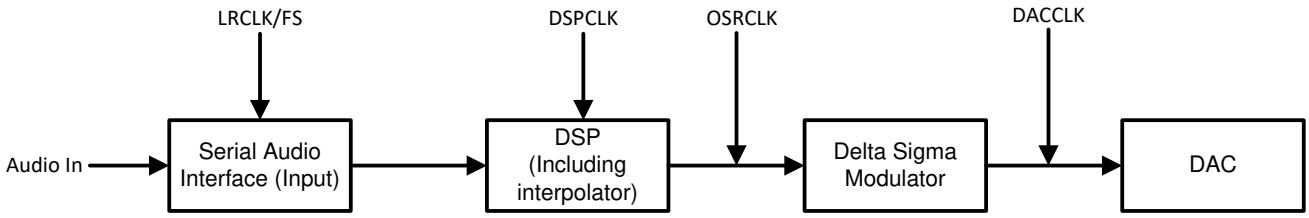


図 6-2. Audio Flow with Respective Clocks

図 6-2 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left/Right Word Clock or Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher-rate clocks required by the DSP and the DAC clock.

The TAS5827 device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32 kHz, 44.1 kHz – 48 kHz, 88.2 kHz – 96 kHz, and 176.4 kHz – 192 kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

If the input LRCLK/SCLK stopped during music playing, the TAS5827 DSP switches to sleep state and waits for the clock recovery (Class D output switches to Hi-Z automatically), once LRCLK/SCLK recovered, TAS5827 auto recovers to the play mode. There is no need to reload the DSP code.

6.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK , and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5827 device with SCLK. The LRCLK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

表 6-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 192	64, 32

表 6-1. Audio Data Formats, Bit Depths and Clock Rates (続き)

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256
		192	128

When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

6.3.4 Clock Halt Auto-recovery

Certain host processors will halt the I^2S clock when there is no audio playing. When the clock is halted, the device puts all channels into the Hi-Z state and issues a latched clock error in Register GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] - D[2]. After audio clocks recovery, the device automatically returns to the previous state.

6.3.5 Sample Rate on the Fly Change

TAS5827 supports an on-the-fly change of the LRCLK(FS) rate. When changing LRCLK(FS) from 48kHz to 96kHz, the host processor seeds to put LRCLK(FS)/SCLK to a halt state for at least 100us before changing to the new sample rate.

6.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[5:4]). If the high width of LRCLK/FS in TDM/DSP mode is less than 8 cycles of SCK, the register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in 図 6-3 through 図 6-7. The word length are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[1:0]). The offsets of data are selected via Register (SAP_CTRL1 Register (Offset = 33h) [Reset = 02h] -D[7]) and Register (SAP_CTRL2 Register (Offset = 34h) [Reset = 00h] -D[7:0]). Default setting is I2S and 24 bit word length.

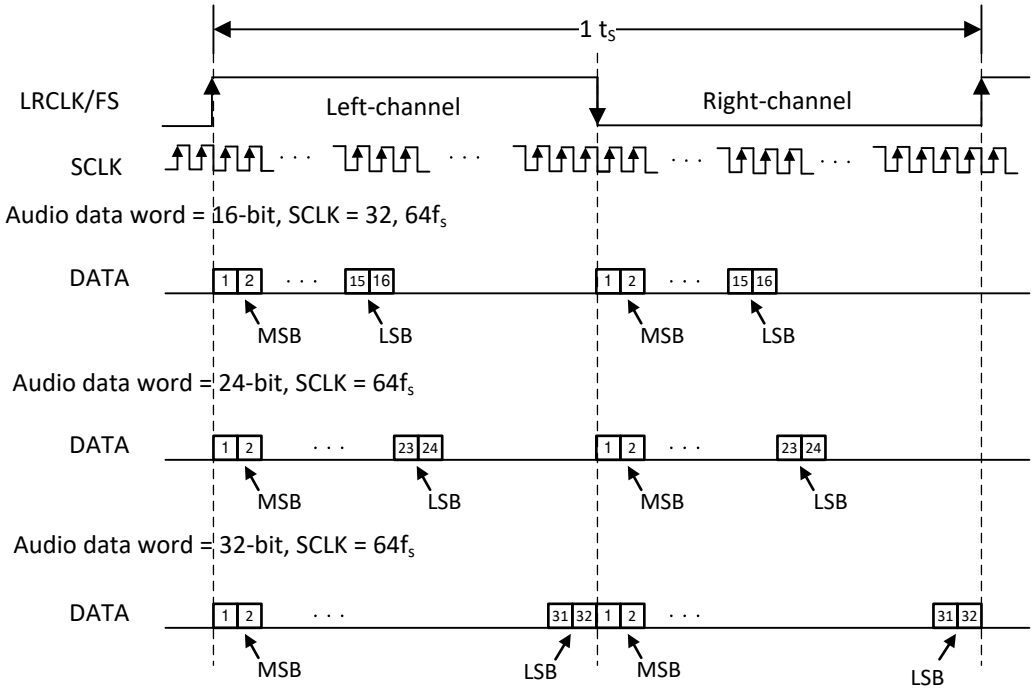
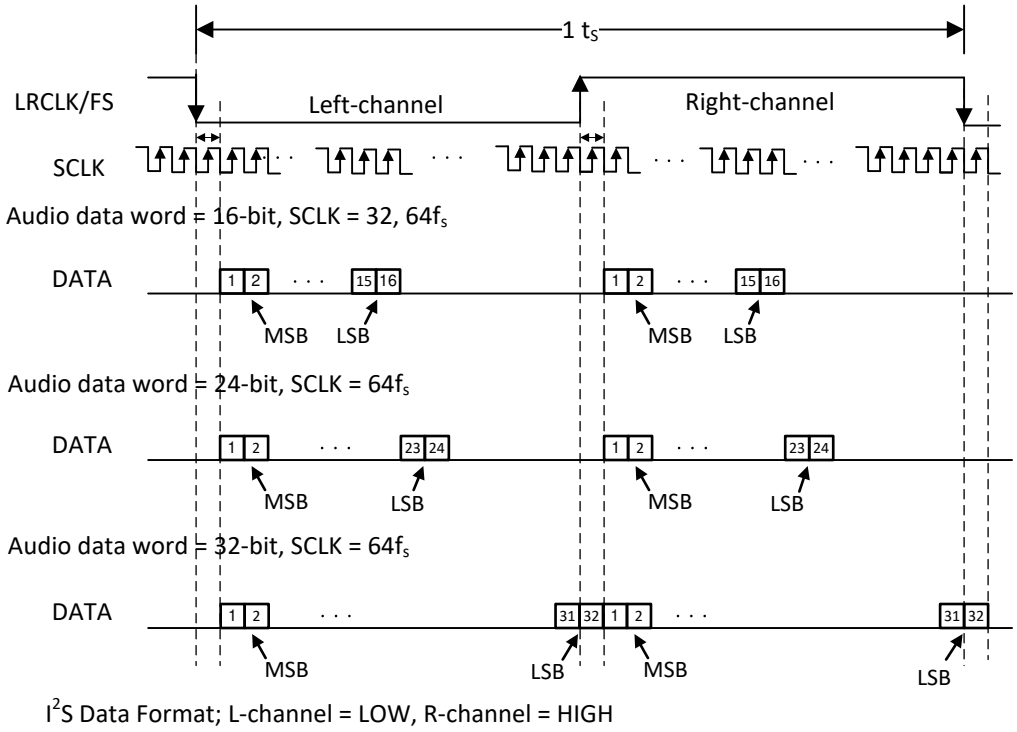
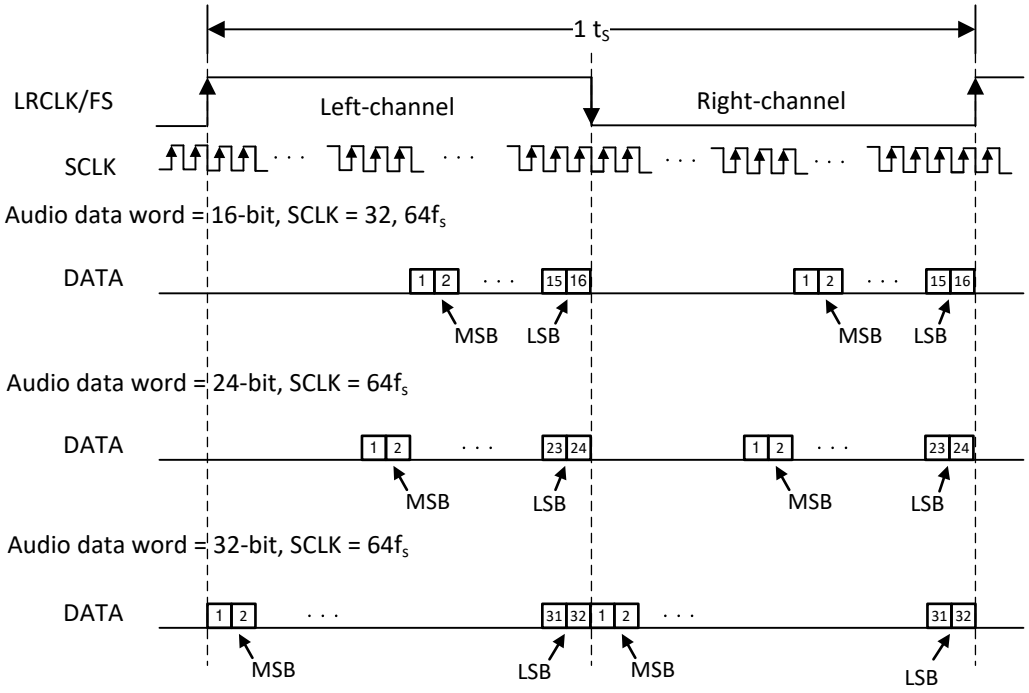


図 6-3. Left Justified Audio Data Format



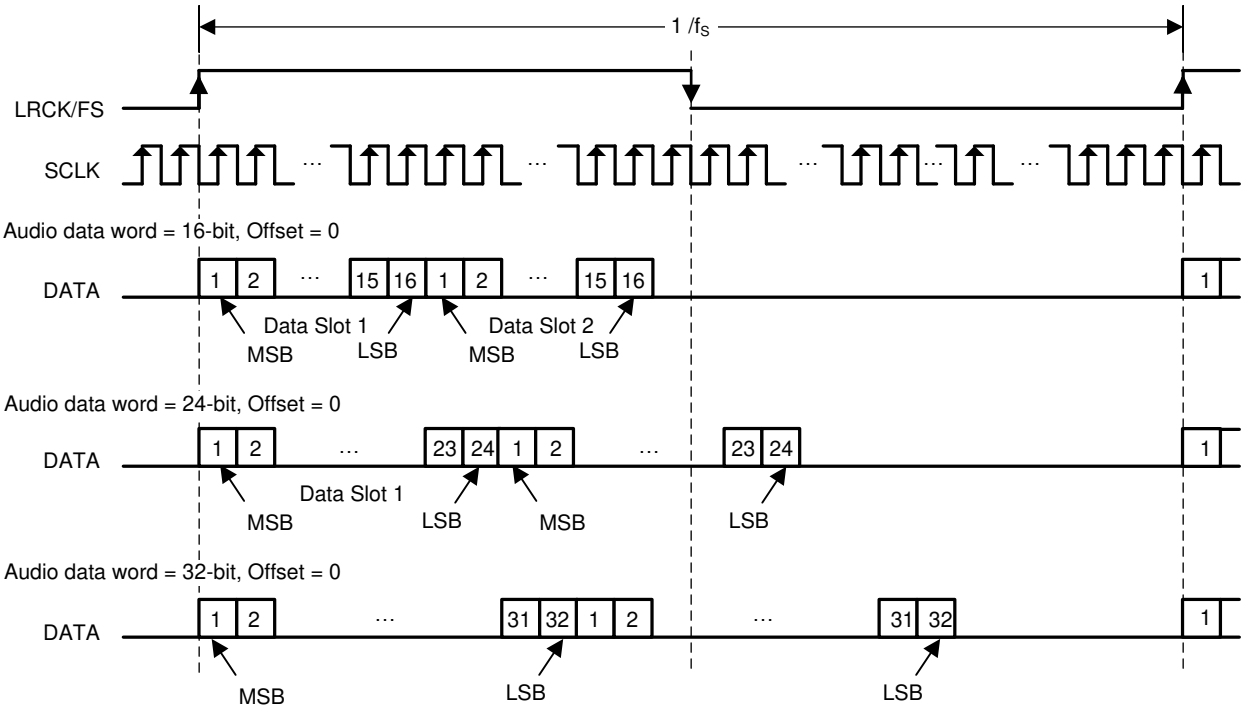
I2S Data Format; L-channel = LOW, R-channel = HIGH

図 6-4. I²S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

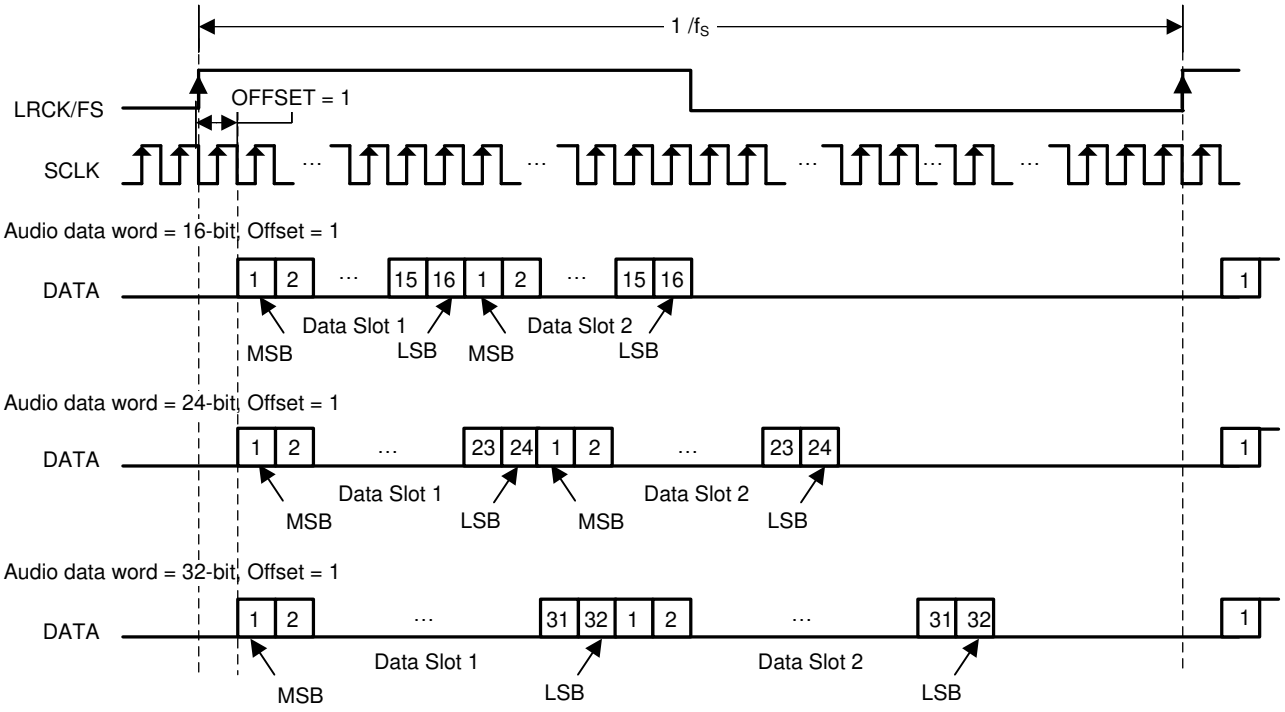
図 6-5. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

図 6-6. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

図 6-7. TDM 2 Audio Data Format

6.4 Device Functional Modes

6.4.1 Software Control

The TAS5827 device is configured via an I²C communication port.

The I2C Communication Protocol is detailed in the I²C Communication Port section. The I²C timing requirements are described in theTiming Requirements - I²C Bus Timing.

6.4.2 Speaker Amplifier Operating Modes

The TAS5827 device can be configured as two different amplifier configurations through Register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] -D[2]:

- BTL Mode
- PBTL Mode

6.4.2.1 BTL Mode

In BTL mode, the TAS5827 amplifies two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on the differential output pair shown as OUT_A+ and OUT_A-, and the amplified right signal is presented on the differential output pair shown as OUT_B+ and OUT_B-.

6.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe an operation in which the two outputs of the device are placed in parallel with one another to increase the power-sourcing capabilities of the device. On the output side of the TAS5827 device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. The process is called Post-Filter

PBTL. On the input side of the TAS5827 device, the input signal to the PBTL amplifier is the left frame of I2S or TDM data.

6.4.3 Low EMI Modes

TAS5827 employs several modes to minimize EMI while playing audio, and they can be used based on different applications.

6.4.3.1 Spread Spectrum

Spread spectrum modulation is a PWM modulation technique that reduces the peaks seen in EMI measurements by varying the output PWM frequency, resulting in a wider spectrum but lower level. The TAS5827 supports Spread Spectrum both of triangle and random mode.

The user needs to configure register RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h] to Enable triangle mode and enable spread spectrum, select spread spectrum frequency and range with RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h] . For 768 kHz F_{SW} which is configured by DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] , the spread spectrum frequency and range are described in 表 6-2.

表 6-2. Triangle Mode Spread Spectrum Frequency and Range Selection

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example: Central Switching Frequency is 768 kHz, Triangle Frequency is 48 kHz.

Register 0x02 = 0x41 // 768 kHz Fsw, BTL Mode, 1SPW mode.

Register 0x6b = 0x03 // Enable Spread Spectrum

Register 0x6c = 0x03 // SS_CTRL[3:0]=0011, Triangle Frequency = 48 kHz, Spread Spectrum Range should be 10% (729 kHz~807 kHz)

6.4.3.2 Channel to Channel Phase Shift

This device supports channel-to-channel 180-degree PWM phase shift to minimize the EMI. Bit 0 of ANA_CTRL Register (Offset = 53h) [Reset = 00h] can be used to disable or enable the phase shift.

6.4.3.3 Multi-Devices PWM Phase Synchronization

TAS5827 supports up to 4 phases of selection for the multi-device application system. For example, when a system integrates 4 TAS5827 devices, the user can select phase 0/1/2/3 for each device by registering RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] , which means there is a 45-degree phase shift between each device to minimize the EMI.

There are two methods for Multi-Device PWM phase synchronization. Phase Synchronization With I²S Clock In Startup Phase or Phase Synchronization With GPIO.

6.4.3.3.1 Phase Synchronization With I²S Clock In Startup Phase

1. Step 1, Halt I²S clock.
2. Step 2, Configure each device phase selection and enable the phase synchronization. For example: Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x03 for device 0; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x07 for device 1; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x0B for device 2; Register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] =0x0F for device 3.
3. Step 3, Configure each device into HIZ mode.
4. Step 4, Provide I²S to each device. Phase synchronization for all 4 devices is automatically done by internal sequence.
5. Step 5, Initialize the DSP code (This step can be skipped if only need to do the Phase Synchronization).

6. Step 6, Device to Device PWM phase shift should be fixed with 45 degrees.

6.4.3.3.2 Phase Synchronization With GPIO

1. Step 1, Connect the GPIOx pin of each device to the SOC GPIO pin on PCB.
2. Step 2, Configure each device GPIOx as phase sync input usage by registers GPIO_CTRL Register (Offset = 60h) [Reset = 00h] and GPIO_INPUT_SEL Register (Offset = 64h) [Reset = 00h] .
3. Step 3, Select a different phase for each device and enable phase synchronization by register RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h] .
4. Step 4, Configure each device into PLAY mode by register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] and monitoring the POWER_STATE Register (Offset = 68h) [Reset = 00h] until device changes to HIZ state.
5. Step 5, Give a 0 to 1 toggle on SOC GPIO. Then all 4 devices enter into PLAY mode, and the device-to-device PWM phase shift should be fixed at 45 degrees.
6. Step 6, Phase Synchronization has been finished. Configure the GPIOx pin to another function based on the application.

6.4.4 Thermal Foldback

The Thermal Foldback (TFB) is designed to protect TAS5827 from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5827 to play as loud as possible without triggering an unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (TAS5827 has four different temperature thresholds, each threshold is indicated in I^2C register WARNING Register (Offset = 73h) [Reset = 00h] bits 0,1,2 and 3), an internal AGL (Automatic Gain Limiter) reduces the digital gain gradually, lower value of OTW, smaller attenuation added, with the OTW waring goes higher, more attenuation added. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed (attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5827 App in PurePath™ Console3.

6.4.5 Device State Control

Except Shutdown Mode, TAS5827 has other 4 states for different power dissipation which are listed in the *Electrical Characteristics Table*.

- Deep Sleep Mode. Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=00, Device stays in Deep Sleep Mode. In this mode, I^2 C block keeps working. This mode can be used to extend the battery lifetime in some portable speaker application cases, once the host processor stops playing audio for a long time, TAS5827 can be set to Deep Sleep Mode to minimize power dissipation until the host processor starts playing audio again. The device returns to Play Mode by setting Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0] to 11. Compared with Shutdown Mode (Pull $\overline{PDN}$ Low), enter or exit Deep Sleep Mode, DSP keeps active.
- Sleep Mode. Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=01, Device stays in Sleep Mode. In this mode, I^2 C block, Digital core, DSP Memory, and 5 V Analog LDO keep working. Compared with Shutdown Mode (Pull $\overline{PDN}$ Low), enter or exit Sleep Mode, DSP keeps active.
- Output Hiz Mode. Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=10, Device stays in Hiz Mode. In this mode, Only the output driver is set to be Hiz state, all other blocks work normally.
- Play Mode. Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=11, Device stays in Play Mode.

6.4.6 Device Modulation

TAS5827 has 3 modulation schemes: BD modulation, 1SPW modulation, and Hybrid modulation. Select modulation schemes for TAS5827 with Register DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h] D[1:0]-DAMP_MOD.

6.4.6.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

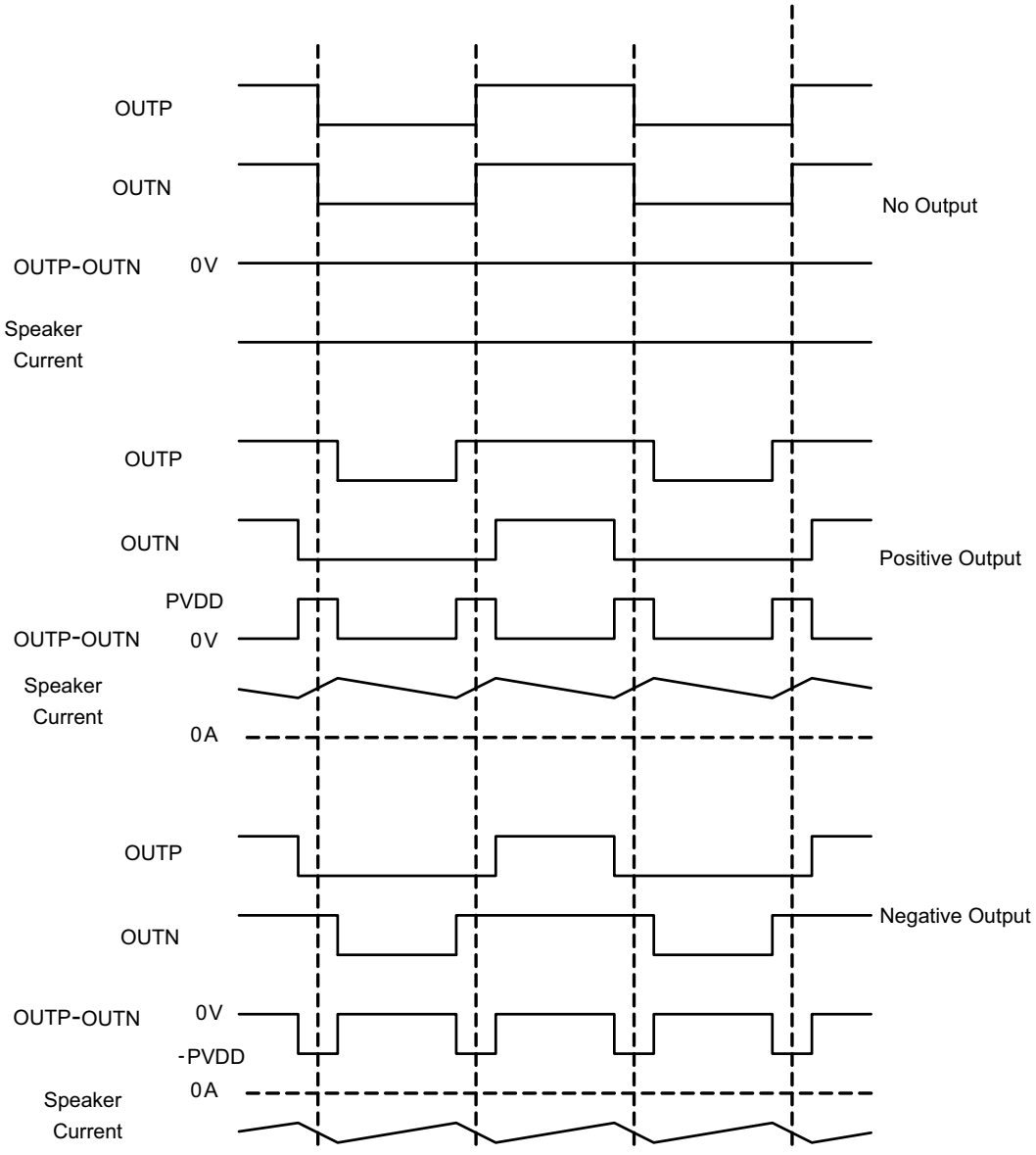


図 6-8. BD Mode Modulation

6.4.6.2 1SPW Modulation

The 1SPW mode alters the typical modulation scheme to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode, the outputs operate at ~17% modulation during idle conditions. When an audio signal is applied, one output decreases, and one increases. The decreasing output signal rails to GND. At this point, all the audio modulation takes place through the rising output. The result is that only one output is switching during the bulk of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

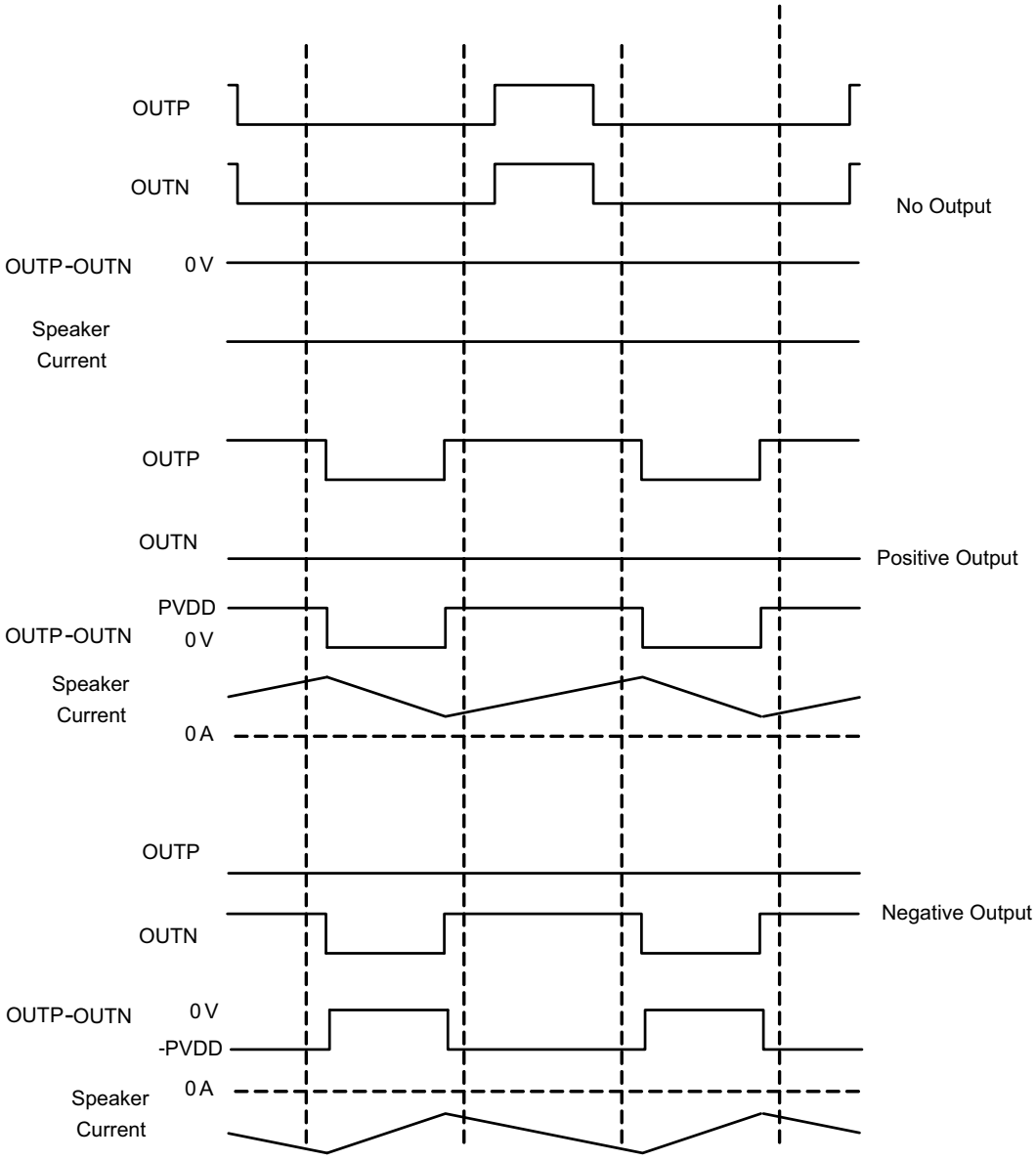


図 6-9. 1SPW Mode Modulation

6.4.6.3 Hybrid Modulation

Hybrid Modulation is designed for minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation, TAS5827 detects the input signal level and adjusts the PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra-low idle current and maintains the same audio performance level as the BD Modulation.

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Hybrid Modulation needs the internal DSP to detect the input signal level and adjust the PWM duty cycle dynamically. To use the Hybrid Modulation, users need to select the corresponding process flows which support Hybrid Modulation in TAS5827 PPC3 App. Look into TAS5827 PPC3 App for more information about TAS5827 flexible audio process flows.

6.4.7 Programming and Control

6.4.7.1 I²C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with I²C bus protocol and supports Standard-mode, Fast-mode(FM) and Fast-mode Plus(FM+) data transfer rates for random and sequential write and read operations as a target device. Because the TAS5827 register map and DSP memory spans multiple pages, the user should change from page to page before writing to the individual registers or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255. All registers listed in TAS5827 Datasheet belongs to Page 0

6.4.7.2 Hardware Control Mode

For systems that do not require the advanced flexibility of the I²C registers control or does not have an available I²C host controller, the TAS5827 can be used in Hardware Control Mode. Then the device operates in Hardware mode default configurations and any change is accomplished via the Hardware control pins. The audio performance between Hardware and Software Control modes with the same configuration is identical, however, more features are accessible under Software Control Mode through registers.

Several I/O's on the TAS5827 needs to be taken into consideration during schematic design for desired startup settings. The method for going into Hardware Control Mode is to pull high HW_MODE pin 8 to DVDD.

The TAS5827 default Hardware configuration is BTL mode, 768-kHz switching frequency, 1SPW mode, 175 kHz Class D amplifier loop bandwidth, 29.5 Vp/FS analog gain, CBC threshold with 80% of OCP threshold. It requires the HW_SEL0 pin 16 and HW_SEL1 pin 15 directly tied to GND.

表 6-3. Hardware Control - HW_SEL0 Pin16

Pin Configuration	Analog Gain	H-Bridge Output Configuration
0 Ω to GND	29.5 V_P/FS	BTL
1 kΩ to GND	20.9 V_P/FS	BTL
4.7 kΩ to GND	14.7 V_P/FS	BTL
15 kΩ to GND	7.4 V_P/FS	BTL
33 kΩ to DVDD	7.4 V_P/FS	PBTL
6.8 kΩ to DVDD	14.7 V_P/FS	PBTL
1.5 kΩ to DVDD	20.9 V_P/FS	PBTL
0 Ω to DVDD	29.5 V_P/FS	PBTL

表 6-4. Hardware Control - HW_SEL1 Pin15

Pin Configuration	F_{SW}&Class D Loop Bandwidth	Cycle By Cycle Current Limit Threshold	Spread Spectrum	Modulation
0 Ω to GND	768 kHz F_{SW}, 175 kHz BW	CBC Threshold = 80% OCP	Disable	1SPW
1 kΩ to GND	768 kHz F_{SW}, 175 kHz BW	CBC Disable	Disable	1SPW
4.7 kΩ to GND	768 kHz F_{SW}, 175 kHz BW	CBC Threshold = 40% OCP	Disable	1SPW
15 kΩ to GND	768 kHz F_{SW}, 175 kHz BW	CBC Threshold = 60% OCP	Disable	1SPW
33 kΩ to DVDD	480 kHz F_{SW}, 100 kHz BW	CBC Disable	Enable	BD

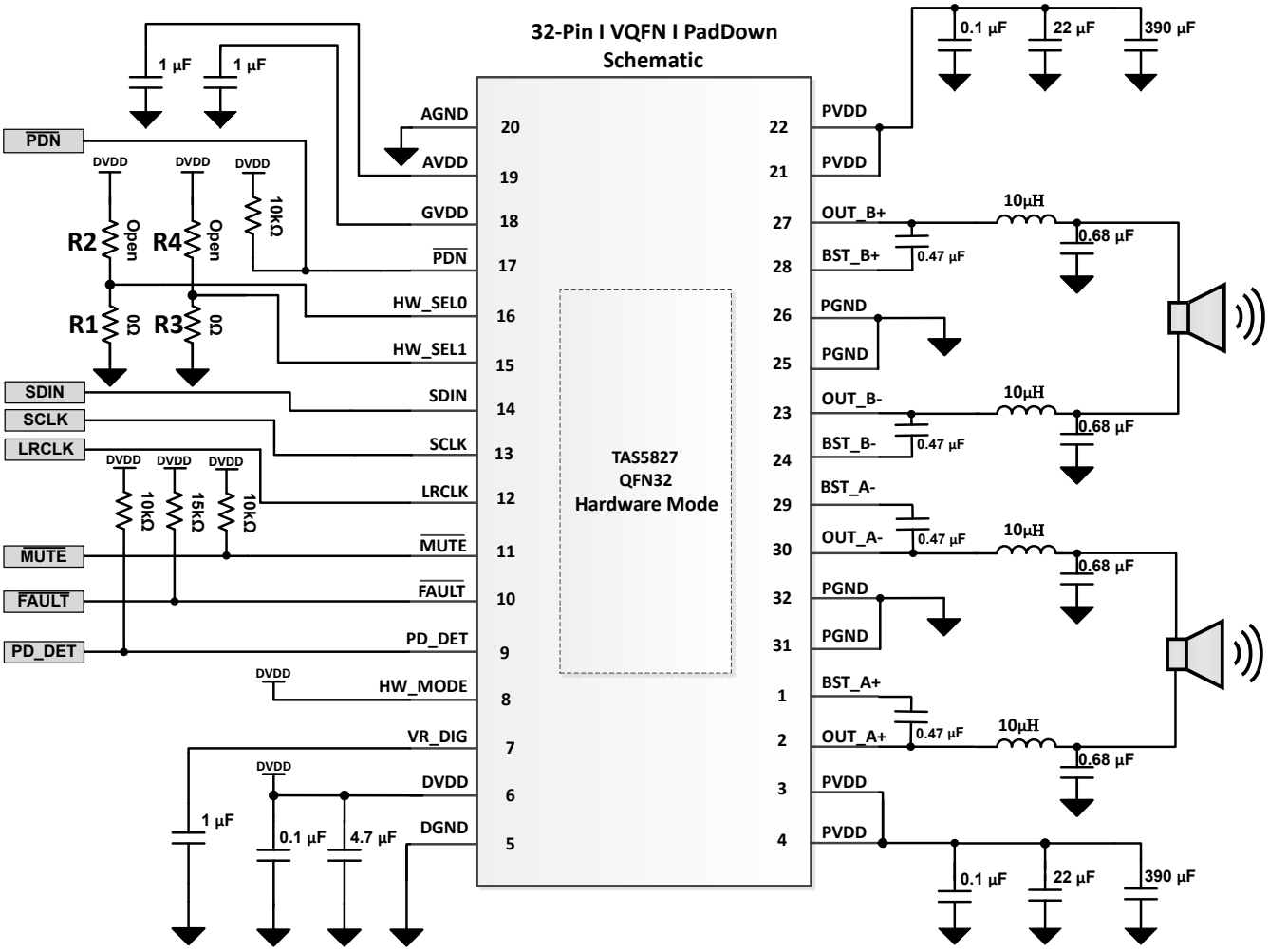
表 6-4. Hardware Control - HW_SEL1 Pin15 (続き)

Pin Configuration	F_{SW}&Class D Loop Bandwidth	Cycle By Cycle Current Limit Threshold	Spread Spectrum	Modulation
6.8 kΩ to DVDD	480 kHz F_{SW}, 100 kHz BW	CBC Threshold = 80% OCP	Enable	BD
1.5 kΩ to DVDD	480 kHz F_{SW}, 100 kHz BW	CBC Threshold = 40% OCP	Enable	BD
0 Ω to DVDD	480 kHz F_{SW}, 100 kHz BW	CBC Threshold = 60% OCP	Enable	BD

Example 1:

BTL Mode, FSW = 768 kHz, 1SPW Modulation, 175 kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5 V_P/FS, Spread spectrum disabled.

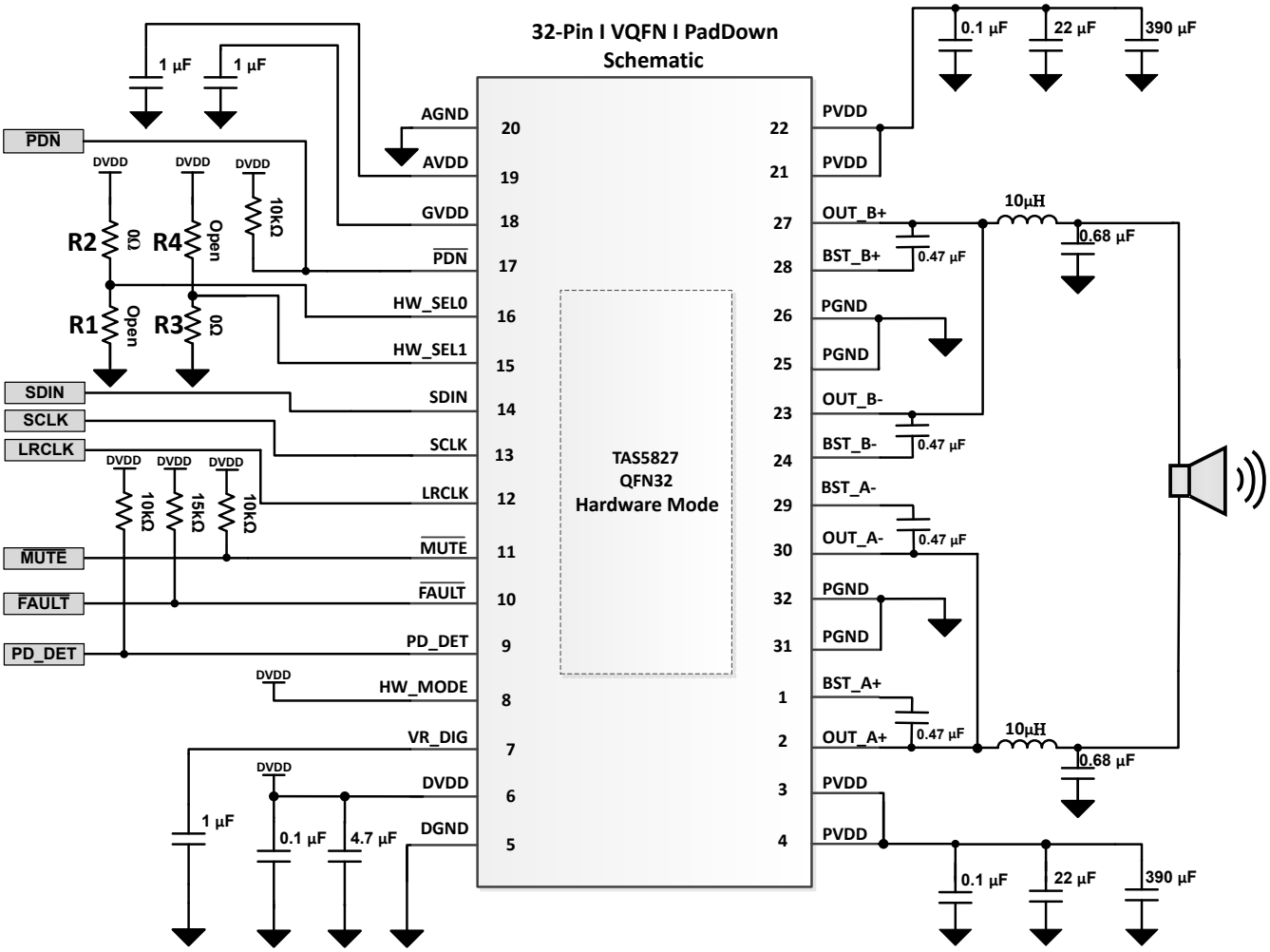
図 6-10. Typical Hardware Control Mode Application Schematic-BTL Mode



Example 2:

PBTL Mode, FSW = 768 kHz, 1 SPW Moduzlation, 175 kHz Loop Bandwidth, CBC Threshold = 80% OCP, Analog Gain = 29.5 V_P/FS, Spread spectrum disabled.

図 6-11. Typical Hardware Control Mode Application Schematic-PBTL Mode



6.4.7.3 I²C Target Address

The TAS5827 device has 7 bits for the target address. The user-defined address through ADR pin is listed in 表 6-5.

表 6-5. I² C Target Address Configuration

ADR PIN Configuration	MSBs				User Define			LSB
0 Ω to GND	1	1	0	0	0	0	0	R/ $\overline{W}$
1kΩ to GND	1	1	0	0	0	0	1	R/ $\overline{W}$
4.7kΩ to GND	1	1	0	0	0	1	0	R/ $\overline{W}$
15kΩ to GND	1	1	0	0	0	1	1	R/ $\overline{W}$
33kΩ to DVDD	1	1	0	0	1	0	0	R/ $\overline{W}$
6.8kΩ to DVDD	1	1	0	0	1	0	1	R/ $\overline{W}$

6.4.7.3.1 Random Write

As shown in 図 6-12, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

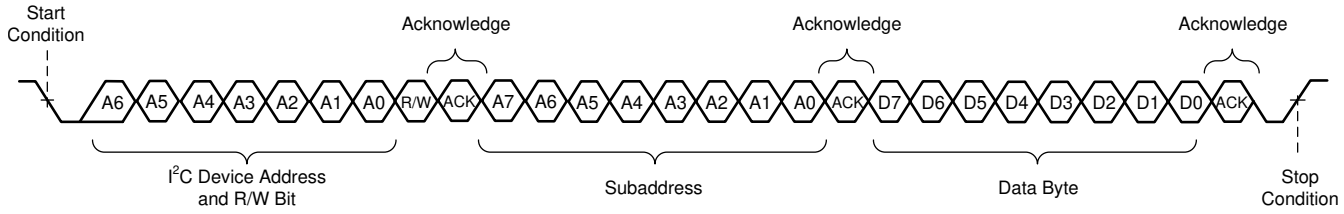


図 6-12. Random Write Transfer

6.4.7.3.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in 図 6-13. After receiving each data byte, the device responds with an acknowledge bit and the I² subaddress is automatically incremented by one.

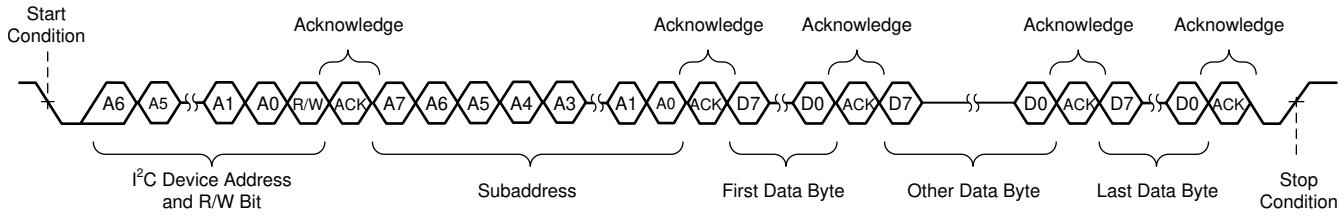


図 6-13. Sequential Write Transfer

6.4.7.3.3 Random Read

As shown in 図 6-14, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

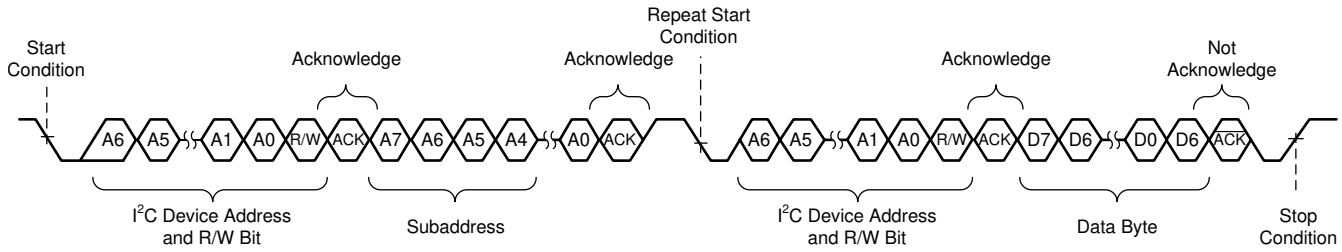


図 6-14. Random Read Transfer

6.4.7.3.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in 図 6-15. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C sub address by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

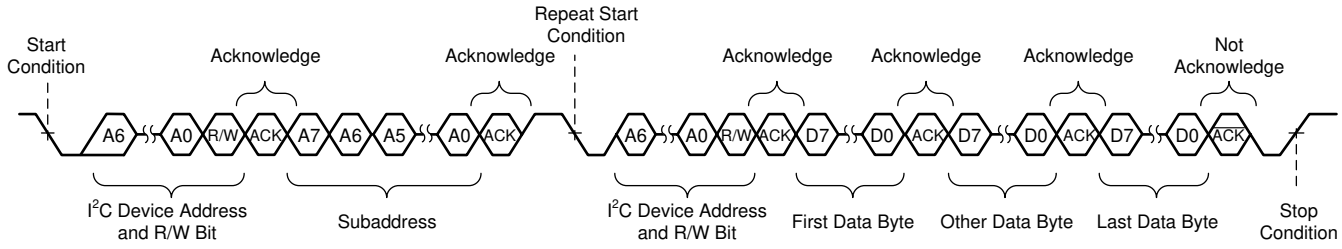


図 6-15. Sequential Read Transfer

6.4.7.3.5 DSP Memory Book, Page and BQ update

On Page 0x00 of each book, Register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a Page first write 0x00 to Register 0x00 to switch to Page 0 then write the book number to Register 0x7f on Page 0. To switch between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest address. The address of all Biquad Filters can be found in Register Maps

All DSP/Audio Process Flow Related Register are listed in Application Note, TAS5827M Process Flows

6.4.7.3.6 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers changes the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

6.4.7.3.6.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I^2C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

6.4.7.3.6.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

6.4.7.4 Control via Software

- Startup Procedures
- Shutdown Procedures

6.4.7.4.1 Startup Procedures

1. Configure ADR pin with proper setting for I²C device address or Hardware Mode with proper HW_SEL0 and HW_SEL1 settings.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once power supplies are stable, wait at least 100 µs, bring up $\overline{\text{PDN}}$ to High to enable internal LDO.
4. I²C control port to configure desired settings. This process includes Deep Sleep to Hi-Z, register map configurations, DSP coefficients, and set into Play mode. Hardware Mode does not need this step I²C writing.
5. Once I²S clocks are stable, TAS5827 is going to normal operation music playing.

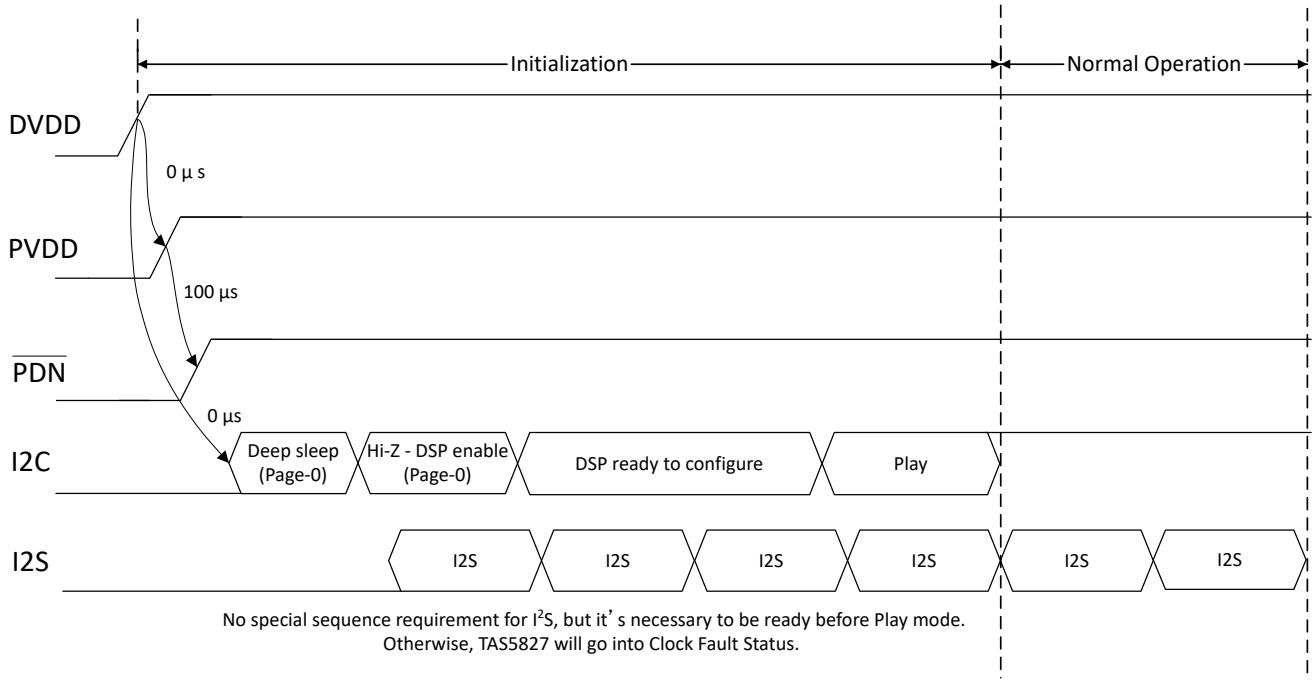
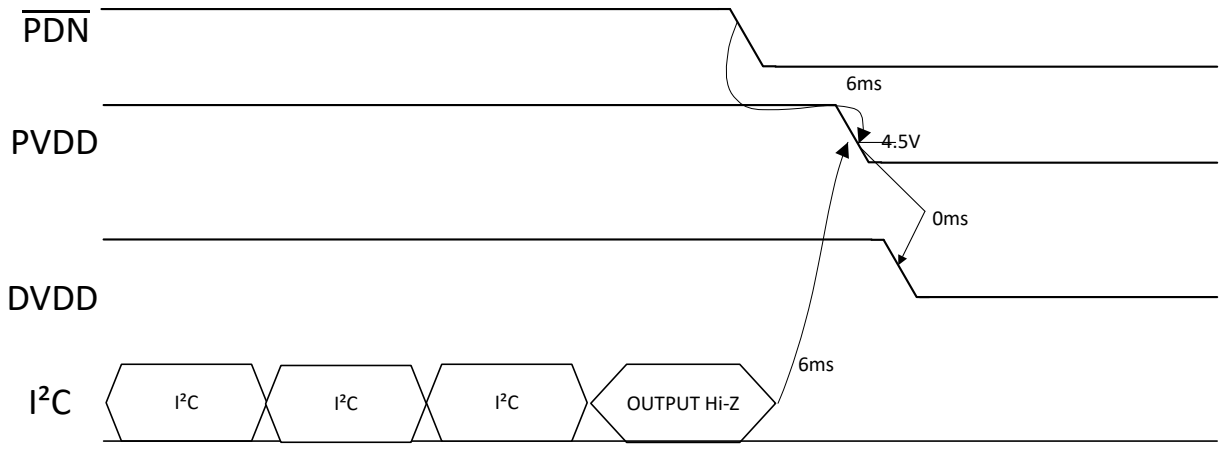


図 6-16. TAS5827 Startup Sequence

6.4.7.4.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h] -D[1:0]=10 (Hi-Z) via the I²C control port or Pull $\overline{PDN}$ low.
3. Wait at least 6ms (this time depends on the LRCLK rate, digital volume, and digital volume ramp-down rate).
4. Bring down power supplies.
5. The device is now fully shut down and powered off.



Before PVDD/DVDD power down, Class D Output driver needs to be disabled by PDN or by I²C.
At least 6ms delay needed based on LRCLK(Fs) = 48kHz, digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume = 24dB. Change the value of register 0x4C and 0x4E or change LRCLK rate, the delay changes.

図 6-17. Power-Down Sequence

6.4.7.5 Protection and Monitoring

6.4.7.5.1 Overcurrent Limit (Cycle-By-Cycle)

Instead of direct Overcurrent Shutdown to mute audio output, TAS5827 also provides CBC current limiting protection. The purpose is to reduce output current ahead of the Overcurrent Shutdown level by inserting pulse into PWM switching, and the threshold (list in Electrical Characteristics - OCE_{THRES}) is configurable through Register CBC_CONTROL Register (Offset = 77h) [Reset = 00h] -D[4:3] Reg_CBC_Level_Sel.

The overall effect on the audio is quite similar to a voltage-clipping, which temporarily limits music signal peak power to maintain continuous music playing without disruption on the removal of the overload.

6.4.7.5.2 Overcurrent Shutdown (OCSD)

If there is a severe short-circuit event, such as output short to PVDD or ground, the TAS5827 starts the shutdown process less than 100 ns once the peak-current detector is over the Overcurrent Threshold (list in Electrical Characteristics - OCE_{THRES}). The shutdown speed depends on several factors, such as the impedance of the short circuit, supply voltage, and switching frequency.

If an OCSD event occurs, the fault GPIO is pulled low and I^2C fault register fault status (CHAN_FAULT Register (Offset = 70h) [Reset = 00h] -D[1:0]) is reported, then outputs transfer to high impedance Hi-Z status, signifying a fault. This is a latched error, and the user needs to restart output via I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1.

6.4.7.5.3 DC Detect Error

If the TAS5827 detects a DC offset in the output voltage cross speaker over DC error protection threshold DCR_{THRES}, and this status period is over T_{DCDET} (list in Electrical Characteristics - Protection), the FAULTZ line is pulled low and the OUTxx outputs transition to high impedance, signifying a fault. This latched DC Protection error requires I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1 to restart the audio output.

6.4.7.5.4 Overtemperature Shutdown (OTSD)

The TAS5827 device continues to monitor die temperature to ensure it does not exceed the over-temperature threshold specified in Electrical Characteristics - OCE_{THRES}. If an OTE event occurs, the fault GPIO is pulled low and I^2C fault status (GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h] -D[0]) is reported, then audio output transfers to high impedance Hi-Z mode, signifying a fault. This is a latched error, and it requires I^2C clear fault operation by setting FAULT_CLEAR Register (Offset = 78h) [Reset = 00h] -D[0] = 1 to restart the audio playing.

6.4.7.5.5 PVDD Overvoltage and Undervoltage Error

If the voltage presented on the PVDD supply rises over the $OVE_{THRES(PVDD)}$ or drops below the $UVE_{THRES(PVDD)}$ listed in Electrical Characteristics - Protection, the fault GPIO is pulled to low and I^2C fault status (GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] -D[1:0]) is reported, then the audio output transfers to high impedance Hi-Z mode. These are self-clearing errors, which means that once the PVDD level is back to normal operation, the device resumes audio playing.

6.4.7.5.6 PVDD Drop Detection

TAS5827 not only provides PVDD Undervoltage Shutdown protection but also optional PVDD drop detection. Based on internal PVDD real-time sensing voltage, TAS5827 can be configured to expected behavior, which could toggle pin10 PD_DET from high to low to indicate PVDD drops below a specific level (default 8 V), and whether TAS5827 automatically goes into Hi-Z mode to shut down the audio output.

The purpose is to feedback on PVDD voltage drop information through GPIO to the user product control system, which can implement a flexible protection strategy. For example, SOC could start the audio volume fade-out process once the PD_DET pin goes too low. This process could provide effective pop-click free control shutdown.

6.4.7.5.7 Clock Fault

When a clock error is detected on the incoming data clock, the TAS5827 device switches to an internal oscillator and continues to the driving DAC, which attenuates the data from the last known value. Once this process is completed, the DAC output is hard-muted to the ground, and the audio output stops. This non-latched clock fault status is reported I^2C fault status (GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h] -D[2]), and the device automatically returns to play mode once the correct clock is back.

6.5 Register Maps

6.5.1 reg_map Registers

表 6-6 lists the memory-mapped registers for the reg_map registers. All register offset addresses not listed in 表 6-6 should be considered as reserved locations and the register contents should not be modified.

表 6-6. REG_MAP Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Reset control	Go
2h	DEVICE_CTRL1	Device control 1	Go
3h	DEVICE_CTRL2	Device control 2	Go
4h	PVDD_UV_CONTROL	PVDD UV Control	Go
Fh	I2C_PAGE_AUTO_INC	I2C DSP memory access page auto increment	Go
28h	SIG_CH_CTRL	Signal chain control	Go
29h	CLOCK_DET_CTRL	Clock detection control	Go
30h	SDOUT_SEL	SDOUT selection	Go
31h	I2S_CTRL	I2S control 0	Go
33h	SAP_CTRL1	I2S control 1	Go
34h	SAP_CTRL2	I2S control 2	Go
35h	SAP_CTRL3	I2S control 3	Go
37h	FS_MON	FS monitor	Go
38h	BCLK_MON	BCLK monitor	Go
39h	CLKDET_STATUS	Clock detection status	Go
40h	DSP_PGM_MODE	DSP program mode	Go
46h	DSP_CTRL	DSP control	Go
4Ch	DIG_VOL_LEFT	Left digital volume	Go
4Dh	DIG_VOL_RIGHT	Right digital volume	Go
4Eh	DIG_VOL_CTRL2	Digital volume control 2	Go
4Fh	DIG_VOL_CTRL3	Digital volume control 3	Go
50h	AUTO_MUTE_CTRL	Auto mute control	Go
51h	AUTO_MUTE_TIME	Auto mute time	Go
53h	ANA_CTRL	Analog control	Go
54h	AGAIN	Analog gain	Go
5Eh	ADC_RPT	ADC(PVDD voltage) report	Go
60h	GPIO_CTRL	GPIO control	Go
61h	GPIO0_SEL	GPIO0 output selection	Go
62h	GPIO1_SEL	GPIO1 output selection	Go
63h	GPIO2_SEL	GPIO2 output selection	Go
64h	GPIO_INPUT_SEL	GPIO input selection	Go
65h	MISC_CTRL1	misc control 1	Go
66h	MISC_CTRL2	misc control 2	Go
67h	DIE_ID	DIE ID	Go
68h	POWER_STATE	Power State	Go
69h	AUTOMUTE_STATE	Auto mute state	Go
6Ah	RAMP_PHASE_CTRL	Switching clock phase control	Go
6Bh	RAMP_SS_CTRL0	Spread spectrum control 0	Go
6Ch	RAMP_SS_CTRL1	Spread spectrum control 1	Go
70h	CHAN_FAULT	Channel fault	Go

表 6-6. REG_MAP Registers (続き)

Offset	Acronym	Register Name	Section
71h	GLOBAL_FAULT1	Global fault 1	Go
72h	GLOBAL_FAULT2	Global fault 2	Go
73h	WARNING	Warning	Go
74h	PIN_CONTROL1	Pin control 1	Go
75h	PIN_CONTROL2	Pin control 2	Go
76h	MISC_CONTROL3	MISC control 3	Go
77h	CBC_CONTROL	CBC control	Go
78h	FAULT_CLEAR	Fault clear	Go

Complex bit access types are encoded to fit into small table cells. 表 6-7 shows the codes that are used for access types in this section.

表 6-7. reg_map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.5.1.1 RESET_CTRL Register (Offset = 1h) [Reset = 00h]

RESET_CTRL is shown in 図 6-18 and described in 表 6-8.

Return to the Summary Table.

Reset control

図 6-18. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
W-0h			W-0h	W-0h			W-0h

表 6-8. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	W	0h	
4	RST_MOD	W	0h	WRITE CLEAR BIT Reset Modules This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in Hi-Z mode. **0: Normal** 1: Reset modules
3-1	RESERVED	W	0h	
0	RST_REG	W	0h	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. The RAM content is not cleared. This bit is auto cleared and must be set only when the DAC is in Hi-Z mode (resetting registers when the DAC is running is prohibited and not supported). **0: Normal** 1: Reset mode registers

6.5.1.2 DEVICE_CTRL1 Register (Offset = 2h) [Reset = 00h]

DEVICE_CTRL1 is shown in 図 6-19 and described in 表 6-9.

Return to the Summary Table.

Device control 1

図 6-19. DEVICE_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	PBTL_MODE	MODULATION	
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	

表 6-9. DEVICE_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	FSW_SEL	R/W	0h	Select PWM switching frequency(Fsw) **3'b 000:384kHz** 3'b 010:480kHz 3'b 011:576kHz 3'b 100:768kHz 3'b 101:1.024MHz Others reserved
3	RESERVED	R/W	0h	
2	PBTL_MODE	R/W	0h	**0: Set device to BTL mode** 1:Set device to PBTL mode
1-0	MODULATION	R/W	0h	**00:BD mode** 01:1SPW mode 10:Hybrid mode 11: Reserved

6.5.1.3 DEVICE_CTRL2 Register (Offset = 3h) [Reset = 10h]

DEVICE_CTRL2 is shown in 図 6-20 and described in 表 6-10.

Return to the Summary Table.

Device control 2

図 6-20. DEVICE_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			DSP_RST	CH1_MUTE	CH2_MUTE	STATE_CTL	
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	

表 6-10. DEVICE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	DSP_RST	R/W	1h	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation **1: Reset the DSP**
3	CH1_MUTE	R/W	0h	Mute Channel 1 This bit issues soft mute request for the ch1. The volume will be smoothly ramped down/up to avoid pop/click noise. **0: Normal volume** 1: Mute
2	CH2_MUTE	R/W	0h	Mute Channel 2 This bit issues soft mute request for the ch2. The volume will be smoothly ramped down/up to avoid pop/click noise. **0: Normal volume** 1: Mute
1-0	STATE_CTL	R/W	0h	Device state control register **00: Deep Sleep** 01: Sleep 10: Hi-Z 11: PLAY

6.5.1.4 PVDD_UV_CONTROL Register (Offset = 4h) [Reset = 00h]

PVDD_UV_CONTROL is shown in 図 6-21 and described in 表 6-11.

Return to the Summary Table.

PVDD UV Control

図 6-21. PVDD_UV_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				UV_SEQ	UV_AVG		UV_BYP
R/W-0h				R/W-0h	R/W-0h		R/W-0h

表 6-11. PVDD_UV_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	UV_SEQ	R/W	0h	**0: Disable when have PVDD UV, device jump to Hi-Z** 1: Enable when have PVDD UV, device jump to Hi-Z
2-1	UV_AVG	R/W	0h	**00: cycle by cycle, no average** 01: 16 samples 10: 32 samples 11: 64 samples
0	UV_BYP	R/W	0h	**0: Disable PVDD drop function** 1: Enable PVDD drop function

6.5.1.5 I2C_PAGE_AUTO_INC Register (Offset = Fh) [Reset = 00h]

I2C_PAGE_AUTO_INC is shown in 図 6-22 and described in 表 6-12.

Return to the Summary Table.

I2C DSP memory access page auto increment

図 6-22. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_INC	RESERVED		
R/W-0h				R/W-0h	R/W-0h		

表 6-12. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	PAGE_INC	R/W	0h	Page auto increment disable Disable page auto increment mode. for non-zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. **0: Enable Page auto increment** 1: Disable Page auto increment
2-0	RESERVED	R/W	0h	

6.5.1.6 SIG_CH_CTRL Register (Offset = 28h) [Reset = 00h]

SIG_CH_CTRL is shown in 図 6-23 and described in 表 6-13.

Return to the Summary Table.

Signal chain control

図 6-23. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCLK_RATIO				FS_MODE			
R/W-0h				R/W-0h			

表 6-13. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCLK_RATIO	R/W	0h	These bits indicate the configured BCLK ratio, the number of BCLK clocks in one audio frame. **4'b0000: Auto detection** 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS Others reserved.
3-0	FS_MODE	R/W	0h	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. **4'b0000 Auto detection** 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 44.1kHz 4'b1001 48kHz 4'b1010 88.2kHz 4'b1011 96kHz 4'b1100 176.4kHz 4'b1101 192kHz Others Reserved

6.5.1.7 CLOCK_DET_CTRL Register (Offset = 29h) [Reset = 00h]

CLOCK_DET_CTRL is shown in 図 6-24 and described in 表 6-14.

Return to the Summary Table.

Clock detection control

図 6-24. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DET_PLL	BCLK_RANGE	DET_FS	DET_BCLK	DET_BCLKMISS	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

表 6-14. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	DET_PLL	R/W	0h	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. **0: Regard PLL overrate detection** 1: Ignore PLL overrate detection
5	BCLK_RANGE	R/W	0h	Ignore BCLK Range Detection This bit controls whether to ignore the BCLK range detection. The BCLK must be stable between 256kHz and 50MHz or an error will be reported. When ignored, a BCLK range error will not cause a clock error. **0: Regard BCLK Range detection** 1: Ignore BCLK Range detection
4	DET_FS	R/W	0h	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error. But CLKDET_STATUS will report fs error. **0: Regard FS detection** 1: Ignore FS detection
3	DET_BCLK	R/W	0h	Ignore BCLK Detection This bit controls whether to ignore the BCLK detection against LRCLK. The BCLK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCLK error will not cause a clock error. **0: Regard BCLK detection** 1: Ignore BCLK detection
2	DET_BCLKMISS	R/W	0h	Ignore BCLK Missing Detection This bit controls whether to ignore the BCLK missing detection. When ignored an BCLK missing will not cause a clock error. **0: Regard BCLK missing detection** 1: Ignore BCLK missing detection
1-0	RESERVED	R/W	0h	

6.5.1.8 SDOUT_SEL Register (Offset = 30h) [Reset = 00h]

SDOUT_SEL is shown in 図 6-25 and described in 表 6-15.

Return to the Summary Table.

SDOUT selection

図 6-25. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
R/W-0h							R/W-0h

表 6-15. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SDOUT_SEL	R/W	0h	SDOUT Select This bit selects what is being output as SDOUT via GPIO pins. **0: SDOUT is the DSP output (post-processing)** 1: SDOUT is the DSP input (pre-processing)

6.5.1.9 I2S_CTRL Register (Offset = 31h) [Reset = 00h]

I2S_CTRL is shown in 図 6-26 and described in 表 6-16.

Return to the Summary Table.

I2S control 0

図 6-26. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_INV	RESERVED				
R/W-0h		R/W-0h	R/W-0h				

表 6-16. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	BCLK_INV	R/W	0h	BCLK Polarity This bit sets the inverted BCLK mode. In inverted BCLK mode, the DAC assumes that the LRCLK and DIN edges are aligned to the rising edge of the BCLK. Normally they are assumed to be aligned to the falling edge of the BCLK. **0: Normal BCLK mode** 1: Inverted BCLK mode
4-0	RESERVED	R/W	0h	

6.5.1.10 SAP_CTRL1 Register (Offset = 33h) [Reset = 02h]

SAP_CTRL1 is shown in 図 6-27 and described in 表 6-17.

Return to the Summary Table.

I2S control 1

図 6-27. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2SSHIFT_MSB	RESERVED	DATA_FMT		LRCLK_PULSE		FRAME_LENGTH	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-2h	

表 6-17. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2SSHIFT_MSB	R/W	0h	I2S Shift MSB. Combine with the 8 bits in low register 34h.
6	RESERVED	R/W	0h	
5-4	DATA_FMT	R/W	0h	I2S Data Format These bits control both input and output audio interface formats for DAC operation. **00: I2S** 01: DSP/TDM 10: RTJ 11: LTJ
3-2	LRCLK_PULSE	R/W	0h	If the LRCLK pulse is shorter than 8 x BCLK, set bit 0-1 to '01' Otherwise, keep these bits as default value '00' 00: High width of LRCLK pulse is equal or greater than 8 cycles of BCLK 01: High width of LRCLK pulse is less than 8 cycles of BCLK
1-0	FRAME_LENGTH	R/W	2h	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits **10: 24 bits** 11: 32 bits

6.5.1.11 SAP_CTRL2 Register (Offset = 34h) [Reset = 00h]

SAP_CTRL2 is shown in 図 6-28 and described in 表 6-18.

Return to the Summary Table.

I2S control 2

図 6-28. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2SSHIFT_LSB							
R/W-0h							

表 6-18. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2SSHIFT_LSB	R/W	0h	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. **8'b00000000: offset = 0 BCLK (no offset)** 8'b00000001: ofsset = 1 BCLK 8'b00000010: offset = 2 BCLKs … 8'b11111111: offset = 512 BCLKs

6.5.1.12 SAP_CTRL3 Register (Offset = 35h) [Reset = 11h]

SAP_CTRL3 is shown in 図 6-29 and described in 表 6-19.

Return to the Summary Table.

I2S control 3

図 6-29. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CH1_DAC		RESERVED		CH2_DAC	
R/W-0h		R/W-1h		R/W-0h		R/W-1h	

表 6-19. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	CH1_DAC	R/W	1h	Channel 1 DAC Data Path These bits control the channel 1 audio data path connection. 00: Zero data (mute) **01: Ch1 data** 10: Ch2 data 11: Reserved (do not set)
3-2	RESERVED	R/W	0h	
1-0	CH2_DAC	R/W	1h	Channel 2 DAC Data Path These bits control the channel 2 audio data path connection. 00: Zero data (mute) **01: Ch2 data** 10: Ch1 data 11: Reserved (do not set)

6.5.1.13 FS_MON Register (Offset = 37h) [Reset = 00h]

FS_MON is shown in 図 6-30 and described in 表 6-20.

Return to the Summary Table.

FS monitor

図 6-30. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLKRATIO_MSB		FS_MON			
R-0h		R-0h		R-0h			

表 6-20. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	BCLKRATIO_MSB	R	0h	2 MSB of detected BCLK ratio. These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. Combine with the 8 bits in low register 38h. BCLK = 32 FS~512 FS
3-0	FS_MON	R	0h	These bits indicate the currently detected audio sampling rate. **4'b0000 FS Error** 4'b0010 8kHz 4'b0100 16kHz 4'b0110 32kHz 4'b1000 Reserved 4'b1001 48kHz 4'b1011 96kHz 4'b1101 192kHz Others Reserved

6.5.1.14 BCLK_MON Register (Offset = 38h) [Reset = 00h]

BCLK_MON is shown in 図 6-31 and described in 表 6-21.

Return to the Summary Table.

BCLK monitor

図 6-31. BCLK_MON Register

7	6	5	4	3	2	1	0
BCLKRATIO_LSB							
R-0h							

表 6-21. BCLK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLKRATIO_LSB	R	0h	These bits indicate the currently detected BCLK ratio, the number of BCLK clocks in one audio frame. BCLK = 32 FS~512 FS

6.5.1.15 CLKDET_STATUS Register (Offset = 39h) [Reset = 00h]

CLKDET_STATUS is shown in 図 6-32 and described in 表 6-22.

Return to the Summary Table.

Clock detection status

図 6-32. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_OVERRATE	PLL_OVERRATE	PLL_LOCKED	BCLK_MISSING	BCLK_VALID	FS_VALID
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 6-22. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	BCLK_OVERRATE	R	0h	This bit indicates whether the BCLK is overrate or underrate. 0: BCLK is underrate 1: BCLK is overrate
4	PLL_OVERRATE	R	0h	This bit indicates whether the PLL is overrate or not. 0: PLL is underrate 1: PLL is overrate
3	PLL_LOCKED	R	0h	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled. 0: PLL is locked 1: PLL is not locked
2	BCLK_MISSING	R	0h	This bit indicates whether the BCLK is missing or not. 0: BCLK is normal 1: BCLK is missing
1	BCLK_VALID	R	0h	This bit indicates whether the BCLK is valid or not. The BCLK ratio must be stable and in the range of 32-512FS to be valid. 0: BCLK is valid 1: BCLK is not valid
0	FS_VALID	R	0h	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid. In non auto detection mode(reg_fsmode!=0), FS error indicates that configured sampling frequency set by LRCLK(FS) is different with detected sampling frequency. Even if FS Error Detection Ignore is set, this flag will be also asserted. 0: Sampling rate is valid 1: Not valid

6.5.1.16 DSP_PGM_MODE Register (Offset = 40h) [Reset = 01h]

DSP_PGM_MODE is shown in 図 6-33 and described in 表 6-23.

Return to the Summary Table.

DSP program mode

図 6-33. DSP_PGM_MODE Register

7	6	5	4	3	2	1	0
RESERVED				CH1_HIZ	CH2_HIZ	DSP_MODE	
R/W-0h				R/W-0h	R/W-0h	R/W-1h	

表 6-23. DSP_PGM_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	CH1_HIZ	R/W	0h	1: Force CH1 to Hi-Z mode **0: Normal operation**
2	CH2_HIZ	R/W	0h	1: Force CH2 to Hi-Z mode **0: Normal operation**
1-0	DSP_MODE	R/W	1h	DSP Program Selection These bits select the DSP program to use for audio processing. 00: RAM mode **01: ROM mode** Others reserved.

6.5.1.17 DSP_CTRL Register (Offset = 46h) [Reset = 01h]

DSP_CTRL is shown in 図 6-34 and described in 表 6-24.

Return to the Summary Table.

DSP control

図 6-34. DSP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			PROC_RATE		RESERVED	IRAM_BOOT	DEF_COEF
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-1h

表 6-24. DSP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	PROC_RATE	R/W	0h	**00:input** 01:48kHz 10:96kHz 11:192kHz
2	RESERVED	R/W	0h	
1	IRAM_BOOT	R/W	0h	DSP boots from IRAM When set DSP will boot from IRAM instead of IROM **0: Boot DSP from IROM** 1: Boot DSP from IRAM
0	DEF_COEF	R/W	1h	Use default coefficients from ZROM This bit controls whether to use default coefficients from ZROM or use the non-default coefficients downloaded to device by the Host 0 : Don't use default coefficients from ZROM **1 : Use default coefficents from ZROM**

6.5.1.18 DIG_VOL_LEFT Register (Offset = 4Ch) [Reset = 30h]

DIG_VOL_LEFT is shown in 図 6-35 and described in 表 6-25.

Return to the Summary Table.

Left digital volume

図 6-35. DIG_VOL_LEFT Register

7	6	5	4	3	2	1	0
CH1_PGA							
R/W-30h							

表 6-25. DIG_VOL_LEFT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1_PGA	R/W	30h	Channel 1 Volume These bits control the ch1 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB … 8'b00101111: +0.5 dB **8'b00110000: 0.0 dB** 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

6.5.1.19 DIG_VOL_RIGHT Register (Offset = 4Dh) [Reset = 30h]

DIG_VOL_RIGHT is shown in 図 6-36 and described in 表 6-26.

Return to the Summary Table.

Right digital volume

図 6-36. DIG_VOL_RIGHT Register

7	6	5	4	3	2	1	0
CH2_PGA							
R/W-30h							

表 6-26. DIG_VOL_RIGHT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2_PGA	R/W	30h	Channel 2 Volume These bits control the ch2 digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 8'b00000000: +24.0 dB 8'b00000001: +23.5 dB … 8'b00101111: +0.5 dB **8'b00110000: 0.0 dB** 8'b00110001: -0.5 dB ... 8'b11111110: -103 dB 8'b11111111: Mute

6.5.1.20 DIG_VOL_CTRL2 Register (Offset = 4Eh) [Reset = 33h]

DIG_VOL_CTRL2 is shown in 図 6-37 and described in 表 6-27.

Return to the Summary Table.

Digital volume control 2

図 6-37. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
VNUS		VNUF		VNDS		VNDF	
R/W-0h		R/W-3h		R/W-0h		R/W-3h	

表 6-27. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VNUS	R/W	0h	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VNUF	R/W	3h	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update **11: Decrement by 0.5 dB for each update**
3-2	VNDS	R/W	0h	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	VNDF	R/W	3h	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update **11: Increment by 0.5 dB for each update**

6.5.1.21 DIG_VOL_CTRL3 Register (Offset = 4Fh) [Reset = 30h]

DIG_VOL_CTRL3 is shown in 図 6-38 and described in 表 6-28.

Return to the Summary Table.

Digital volume control 3

図 6-38. DIG_VOL_CTRL3 Register

7	6	5	4	3	2	1	0
VEDS		VEDF		RESERVED			
R/W-0h		R/W-3h		R/W-0h			

表 6-28. DIG_VOL_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VEDS	R/W	0h	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute **00: Update every 1 FS period** 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	VEDF	R/W	3h	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update **11: Decrement by 0.5 dB for each update**
3-0	RESERVED	R/W	0h	

6.5.1.22 AUTO_MUTE_CTRL Register (Offset = 50h) [Reset = 07h]

AUTO_MUTE_CTRL is shown in 図 6-39 and described in 表 6-29.

Return to the Summary Table.

Auto mute control

図 6-39. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					AM_CTL	AMUTE_CH2	AMUTE_CH1
R/W-0h					R/W-1h	R/W-1h	R/W-1h

表 6-29. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	AM_CTL	R/W	1h	0: Auto mute ch1 and ch2 independently **1: Auto mute ch1 and ch2 only when both channels are about to be auto muted**
1	AMUTE_CH2	R/W	1h	Auto Mute Channel 2 This bit enables or disables auto mute on Channel 2 0: Disable Channel 2 auto mute **1: Enable Channel 2 auto mute**
0	AMUTE_CH1	R/W	1h	Auto Mute Channel 1 This bit enables or disables auto mute on Channel 1 0: Disable Channel 1 auto mute **1: Enable Channel 1 auto mute**

6.5.1.23 AUTO_MUTE_TIME Register (Offset = 51h) [Reset = 00h]

AUTO_MUTE_TIME is shown in 図 6-40 and described in 表 6-30.

Return to the Summary Table.

Auto mute time

図 6-40. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	CH1_AMT			RESERVED	CH2_AMT		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

表 6-30. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	CH1_AMT	R/W	0h	Auto Mute Time for Channel 1 These bits specify the length of consecutive zero samples at ch1 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. **000: 11.5 ms** 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0h	
2-0	CH2_AMT	R/W	0h	Auto Mute Time for Channel 2 These bits specify the length of consecutive zero samples at ch2 before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. **000: 11.5 ms** 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

6.5.1.24 ANA_CTRL Register (Offset = 53h) [Reset = 00h]

ANA_CTRL is shown in 図 6-41 and described in 表 6-31.

Return to the Summary Table.

Analog control

図 6-41. ANA_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	BW_CTL			RESERVED			PHASE_CTL
R/W-0h	R/W-0h			R/W-0h			R/W-0h

表 6-31. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-5	BW_CTL	R/W	0h	Class D Loop Bandwidth **00: 100kHz** 01: 80kHz 10: 120kHz 11: 175kHz When Fsw=384kHz, 100kHz bandwidth is selected for high audio performance. With Fsw=768kHz, 175kHz bandwidth should be selected for high audio performance.
4-1	RESERVED	R/W	0h	
0	PHASE_CTL	R/W	0h	**0: Out of phase** 1: In phase

6.5.1.25 AGAIN Register (Offset = 54h) [Reset = 00h]

AGAIN is shown in 図 6-42 and described in 表 6-32.

Return to the Summary Table.

Analog gain

図 6-42. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			AGAIN				
R/W-0h			R/W-0h				

表 6-32. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-0	AGAIN	R/W	0h	Analog Gain Control This bit controls the analog gain **00000: 0 dB** 00001:-0.5 dB …… 11111: -15.5 dB

6.5.1.26 ADC_RPT Register (Offset = 5Eh) [Reset = 00h]

ADC_RPT is shown in 図 6-43 and described in 表 6-33.

Return to the Summary Table.

ADC(PVDD voltage) report

図 6-43. ADC_RPT Register

7	6	5	4	3	2	1	0
PVDD_RPT							
R-0h							

表 6-33. ADC_RPT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PVDD_RPT	R	0h	PVDD ADC reading. Each LSB means 0.12V For PVDD = 12V, the AD data = 8'b 01100100 For PVDD = 24V, the AD data = 8'b 11001000

6.5.1.27 GPIO_CTRL Register (Offset = 60h) [Reset = 00h]

GPIO_CTRL is shown in 図 6-44 and described in 表 6-34.

Return to the Summary Table.

GPIO control

図 6-44. GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					GPIO2OE	GPIO1OE	GPIO0OE
R/W-0h					R/W-0h	R/W-0h	R/W-0h

表 6-34. GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	GPIO2OE	R/W	0h	GPIO2 Output Enable This bit sets the direction of the GPIO2 pin **0: GPIO2 is input** 1: GPIO2 is output
1	GPIO1OE	R/W	0h	GPIO1 Output Enable This bit sets the direction of the GPIO1 pin **0: GPIO1 is input** 1: GPIO1 is output
0	GPIO0OE	R/W	0h	GPIO0 Output Enable This bit sets the direction of the GPIO0 pin **0: GPIO0 is input** 1: GPIO0 is output

6.5.1.28 GPIO0_SEL Register (Offset = 61h) [Reset = 00h]

GPIO0_SEL is shown in 図 6-45 and described in 表 6-35.

Return to the Summary Table.

GPIO0 output selection

図 6-45. GPIO0_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO0SEL			
R/W-0h				R/W-0h			

表 6-35. GPIO0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO0SEL	R/W	0h	**4'b0000: off (low)** 4'b1000: GPIO0 as WARNZ output 4'b1011: GPIO0 as FAULTZ output 4'b1100: GPIO0 as PVDD_DROP_DETECTION 4'b1101: GPIO0 as Serial audio interface data output (SDOUT) 4'b1110: GPIO0 as RAMP clk Others reserved

6.5.1.29 GPIO1_SEL Register (Offset = 62h) [Reset = 00h]

GPIO1_SEL is shown in 図 6-46 and described in 表 6-36.

Return to the Summary Table.

GPIO1 output selection

図 6-46. GPIO1_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO1SEL			
R/W-0h				R/W-0h			

表 6-36. GPIO1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO1SEL	R/W	0h	**0000: off (low)** 1000: GPIO1 as WARNZ output 1011: GPIO1 as FAULTZ output 1100: GPIO1 as PVDD_UV_DETECTION 1101: GPIO1 as Serial audio interface data output (SDOUT) 1110: GPIO1 as RAMP clk Others reserved

6.5.1.30 GPIO2_SEL Register (Offset = 63h) [Reset = 00h]

GPIO2_SEL is shown in 図 6-47 and described in 表 6-37.

Return to the Summary Table.

GPIO2 output selection

図 6-47. GPIO2_SEL Register

7	6	5	4	3	2	1	0
RESERVED				GPIO2_SEL			
R/W-0h				R/W-0h			

表 6-37. GPIO2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-0	GPIO2_SEL	R/W	0h	**4'b0000: off (low)** 4'b1000: GPIO2 as WARNZ output 4'b1011: GPIO2 as FAULTZ output 4'b1100: GPIO2 as PVDD_DROP_DETECTION 4'b1101: GPIO2 as Serial audio interface data output (SDOUT) 4'b1110: GPIO2 as RAMP clk 4'b1111: Reserved

6.5.1.31 GPIO_INPUT_SEL Register (Offset = 64h) [Reset = 00h]

GPIO_INPUT_SEL is shown in 図 6-48 and described in 表 6-38.

Return to the Summary Table.

GPIO input selection

図 6-48. GPIO_INPUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED		GPIOSYNC_SEL		GPIORST_SEL		GPIOM_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

表 6-38. GPIO_INPUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-4	GPIOSYNC_SEL	R/W	0h	**00: N/A** 01: GPIO0 10: GPIO1 11: GPIO2
3-2	GPIORST_SEL	R/W	0h	**00: N/A** 01: GPIO0 10: GPIO1 11: GPIO2
1-0	GPIOM_SEL	R/W	0h	**00: N/A** 01: GPIO0 10: GPIO1 11: GPIO2

6.5.1.32 MISC_CTRL1 Register (Offset = 65h) [Reset = 00h]

MISC_CTRL1 is shown in 図 6-49 and described in 表 6-39.

Return to the Summary Table.

misc control 1

図 6-49. MISC_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED					GPIO_OUTPUT		
R/W-0h					R/W-0h		

表 6-39. MISC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2-0	GPIO_OUTPUT	R/W	0h	Writing 3 bits for GPIO output

6.5.1.33 MISC_CTRL2 Register (Offset = 66h) [Reset = 00h]

MISC_CTRL2 is shown in 図 6-50 and described in 表 6-40.

Return to the Summary Table.

misc control 2

図 6-50. MISC_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED						GPIO_INV	
R/W-0h						R/W-0h	

表 6-40. MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2-0	GPIO_INV	R/W	0h	Enable GPIO output invert by setting this bit to '1' Default disable the invert function of GPIO output.

6.5.1.34 DIE_ID Register (Offset = 67h) [Reset = A9h]

DIE_ID is shown in 図 6-51 and described in 表 6-41.

Return to the Summary Table.

DIE ID

図 6-51. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-A9h							

表 6-41. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	A9h	Die ID for TAS5827.

6.5.1.35 POWER_STATE Register (Offset = 68h) [Reset = 00h]

POWER_STATE is shown in 図 6-52 and described in 表 6-42.

Return to the Summary Table.

Power State

図 6-52. POWER_STATE Register

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R-0h						R-0h	

表 6-42. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1-0	STATE_RPT	R	0h	**00: Deep sleep** 01: Sleep 10: Hi-Z 11: Play others: reserved

6.5.1.36 AUTOMUTE_STATE Register (Offset = 69h) [Reset = 00h]

AUTOMUTE_STATE is shown in 図 6-53 and described in 表 6-43.

Return to the Summary Table.

Auto mute state

図 6-53. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						CH2MUTE_STATUS	CH1MUTE_STATUS
R-0h						R-0h	R-0h

表 6-43. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	CH2MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 2. **0: Not auto muted** 1: Auto muted
0	CH1MUTE_STATUS	R	0h	This bit indicates the auto mute status for Channel 1. **0: Not auto muted** 1: Auto muted

6.5.1.37 RAMP_PHASE_CTRL Register (Offset = 6Ah) [Reset = 00h]

RAMP_PHASE_CTRL is shown in 図 6-54 and described in 表 6-44.

Return to the Summary Table.

Switching clock phase control

図 6-54. RAMP_PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMPPHASE_SEL		RAMPSYNC_SEL	RAMPSYNC_EN
R/W-0h				R/W-0h		R/W-0h	R/W-0h

表 6-44. RAMP_PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3-2	RAMPPHASE_SEL	R/W	0h	Select ramp clock phase when multi devices are integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. **00: 0 degree** 01: 45 degree 10: 90 degree 11: 135 degree all of above have a 45 degree of phase shift
1	RAMPSYNC_SEL	R/W	0h	Ramp phase sync source **0: GPIO sync** 1: Internal sync
0	RAMPSYNC_EN	R/W	0h	1: Enable ramp phase sync **0: Disable ramp phase sync**

6.5.1.38 RAMP_SS_CTRL0 Register (Offset = 6Bh) [Reset = 00h]

RAMP_SS_CTRL0 is shown in 図 6-55 and described in 表 6-45.

Return to the Summary Table.

Spread spectrum control 0

図 6-55. RAMP_SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED						RDM_EN	TRI_EN
R/W-0h						R/W-0h	R/W-0h

表 6-45. RAMP_SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	RDM_EN	R/W	0h	1: Random SS enable **0: Random SS disable**
0	TRI_EN	R/W	0h	1: Triangle SS enable **0: Triangle SS disable**

6.5.1.39 RAMP_SS_CTRL1 Register (Offset = 6Ch) [Reset = 00h]

RAMP_SS_CTRL1 is shown in 図 6-56 and described in 表 6-46.

Return to the Summary Table.

Spread spectrum control 1

図 6-56. RAMP_SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RDM_CTL			TRI_CTL			
R/W-0h	R/W-0h			R/W-0h			

表 6-46. RAMP_SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6-4	RDM_CTL	R/W	0h	Random SS range control For Fsw of 384kHz **3'b000: SS range +/- 0.62%** 3'b010: SS range +/- 1.88% 3'b011: SS range +/- 4.38% 3'b100: SS range +/- 9.38% 3'b101: SS range +/- 19.38% Others: reserved For Fsw of 576kHz 3'b000: SS range +/- 0.95% 3'b010: SS range +/- 2.86% 3'b011: SS range +/- 6.67% 3'b100: SS range +/- 14.29% 3'b101: SS range +/- 29.52% Others: reserved
3-0	TRI_CTL	R/W	0h	Triangle SS frequency and range control **4'b0000: 24kHz SS +/- 5%** 4'b0001: 24kHz SS +/- 10% 4'b0010: 24kHz SS +/- 20% 4'b0011: 24kHz SS +/- 25% 4'b0100: 48kHz SS +/- 5% 4'b0101: 48kHz SS +/- 10% 4'b0110: 48kHz SS +/- 20% 4'b0111: 48kHz SS +/- 25% 4'b1000: 32kHz SS +/- 5% 4'b1001: 32kHz SS +/- 10% 4'b1010: 32kHz SS +/- 20% 4'b1011: 32kHz SS +/- 25% 4'b1100: 16kHz SS +/- 5% 4'b1101: 16kHz SS +/- 10% 4'b1110: 16kHz SS +/- 20% 4'b1111: 16kHz SS +/- 25%

6.5.1.40 CHAN_FAULT Register (Offset = 70h) [Reset = 00h]

CHAN_FAULT is shown in 図 6-57 and described in 表 6-47.

Return to the Summary Table.

Channel fault

図 6-57. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1DC	CH2DC	CH1OC	CH2OC
R-0h				R-0h	R-0h	R-0h	R-0h

表 6-47. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CH1DC	R	0h	Channel 1 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
2	CH2DC	R	0h	Channel 2 DC fault. Once there is a DC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	CH1OC	R	0h	Channel 1 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	CH2OC	R	0h	Channel 2 over current fault. Once there is a OC fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

6.5.1.41 GLOBAL_FAULT1 Register (Offset = 71h) [Reset = 00h]

GLOBAL_FAULT1 is shown in 図 6-58 and described in 表 6-48.

Return to the Summary Table.

Global fault 1

図 6-58. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
RESERVED	BQWRTFAULT_FLAG	EEPROMFAULT_FLAG	RESERVED		CLKFAULT_FLAG	PVDDOV_FLAG	PVDDUV_FLAG
R-0h	R-0h	R-0h	R-0h		R-0h	R-0h	R-0h

表 6-48. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	BQWRTFAULT_FLAG	R	0h	**0: The recent BQ is written successfully** 1: The recent BQ writed failed
5	EEPROMFAULT_FLAG	R	0h	**0: EEPROM boot load was done successfully** 1: EEPROM boot load was done unsuccessfully
4-3	RESERVED	R	0h	
2	CLKFAULT_FLAG	R	0h	Clock fault. Once there is a Clock fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
1	PVDDOV_FLAG	R	0h	PVDD OV fault. Once there is a OV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.
0	PVDDUV_FLAG	R	0h	PVDD UV fault. Once there is a UV fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). UV fault works with an auto-recovery mode, once the UV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

6.5.1.42 GLOBAL_FAULT2 Register (Offset = 72h) [Reset = 00h]

GLOBAL_FAULT2 is shown in 図 6-59 and described in 表 6-49.

Return to the Summary Table.

Global fault 2

図 6-59. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					CH2CBC_FLAG	CH1CBC_FLAG	OTSD_FLAG
R-0h					R-0h	R-0h	R-0h

表 6-49. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	CH2CBC_FLAG	R	0h	**0: No CBC fault on Channel 2** 1: CBC fault triggered on Channel 2
1	CH1CBC_FLAG	R	0h	**0: No CBC fault on Channel 1** 1: CBC fault triggered on Channel 1
0	OTSD_FLAG	R	0h	Over temperature shut down fault Once there is a OT fault, the fault is latched and this bit is set to be 1. Class D output is set to Hi-Z. Report by FAULT pin (GPIO). OV fault works with an autorecovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Fault_clear Register (78h) to 1 or this bit keeps 1.

6.5.1.43 WARNING Register (Offset = 73h) [Reset = 00h]

WARNING is shown in 図 6-60 and described in 表 6-50.

Return to the Summary Table.

Warning

図 6-60. WARNING Register

7	6	5	4	3	2	1	0
RESERVED		CH1CBCW_FLAG	CH2CBCW_FLAG	OTW4_FLAG	OTW3_FLAG	OTW2_FLAG	OTW1_FLAG
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 6-50. WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	CH1CBCW_FLAG	R	0h	**0: No CBC warning on Channel 1** 1: CBC warning triggered on Channel 1
4	CH2CBCW_FLAG	R	0h	**0: No CBC warning on Channel 2** 1: CBC warning triggered on Channel 2
3	OTW4_FLAG	R	0h	**0: No temperature level 4 warning** 1: Over temperature warning level 4 is triggered
2	OTW3_FLAG	R	0h	**0: No temperature level 3 warning** 1: Over temperature warning level 3 is triggered
1	OTW2_FLAG	R	0h	**0: No temperature level 2 warning** 1: Over temperature warning level 2 is triggered
0	OTW1_FLAG	R	0h	**0: No temperature level 1 warning** 1: Over temperature warning level 1 is triggered

6.5.1.44 PIN_CONTROL1 Register (Offset = 74h) [Reset = 00h]

PIN_CONTROL1 is shown in 図 6-61 and described in 表 6-51.

Return to the Summary Table.

Pin control 1

図 6-61. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	MASK_DVDDUV	MASK_DVDDOV	MASK_CLKERROR	MASK_PVDDUV	MASK_PVDDOV	MASK_DC	MASK_OC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

表 6-51. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0h	**0: Enable OTSD fault report** 1: Mask OTSD fault report
6	MASK_DVDDUV	R/W	0h	**0: Enable DVDD UV fault report** 1: Mask DVDD UV report
5	MASK_DVDDOV	R/W	0h	**0: Enable DVDD OV fault report** 1: Mask DVDD OV fault report
4	MASK_CLKERROR	R/W	0h	**0: Enable CLK fault report** 1: Mask CLK fault report
3	MASK_PVDDUV	R/W	0h	**0: Enable UV fault report** 1: Mask UV fault report
2	MASK_PVDDOV	R/W	0h	**0: Enable OV fault report** 1: Mask OV fault report
1	MASK_DC	R/W	0h	**0: Enable DC fault report** 1: Mask DC fault report
0	MASK_OC	R/W	0h	**0: Enable OC fault report** 1: Mask OC fault report

6.5.1.45 PIN_CONTROL2 Register (Offset = 75h) [Reset = F8h]

PIN_CONTROL2 is shown in 図 6-62 and described in 表 6-52.

Return to the Summary Table.

Pin control 2

図 6-62. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
CBCFAULTLATCH_EN	CBCWARNLATCH_EN	CLKFAULTLATCH_EN	OTSDLATCH_EN	OTWLATCH_EN	MASK_OTW	MASK_CBCWARN	MASK_CBCFAULT
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

表 6-52. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CBCFAULTLATCH_EN	R/W	1h	0: Disable CBC fault latch **1: Enable CBC fault latch**
6	CBCWARNLATCH_EN	R/W	1h	0: Disable CBC warning latch **1: Enable CBC warning latch**
5	CLKFAULTLATCH_EN	R/W	1h	0: Disable CLK fault latch **1: Enable CLK fault latch**
4	OTSDLATCH_EN	R/W	1h	0: Disable OTSD fault latch **1: Enable OTSD fault latch**
3	OTWLATCH_EN	R/W	1h	0: Disable OTW warning latch **1: Enable OTW warning latch**
2	MASK_OTW	R/W	0h	**0: Enable OTW warning report** 1: Mask OTW warning report
1	MASK_CBCWARN	R/W	0h	**0: Enable CBC warning report** 1: Mask CBC warning report
0	MASK_CBCFAULT	R/W	0h	**0: Enable CBC fault report** 1: Mask CBC fault report

6.5.1.46 MISC_CONTROL3 Register (Offset = 76h) [Reset = 00h]

MISC_CONTROL3 is shown in 図 6-63 and described in 表 6-53.

Return to the Summary Table.

MISC control 3

図 6-63. MISC_CONTROL3 Register

7	6	5	4	3	2	1	0
CLKDET_LATCH	RESERVED		OTSD_AUTOREC	RESERVED			
R/W-0h	R/W-0h		R/W-0h	R/W-0h			

表 6-53. MISC_CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKDET_LATCH	R/W	0h	1:Latch clock detection status **0:No latch clock detection status**
6-5	RESERVED	R/W	0h	
4	OTSD_AUTOREC	R/W	0h	**0: Disable OTSD auto recovery** 1: Enable OTSD auto recovery
3-0	RESERVED	R/W	0h	

6.5.1.47 CBC_CONTROL Register (Offset = 77h) [Reset = 00h]

CBC_CONTROL is shown in 図 6-64 and described in 表 6-54.

Return to the Summary Table.

CBC control

図 6-64. CBC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED			CBCLEVEL_SEL		CBC_EN	CBCWARN_EN	CBCFAULT_EN
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

表 6-54. CBC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	CBCLEVEL_SEL	R/W	0h	These bits set Cycle-By-Cycle current limiting level, which is a percentage of the Over-Current Threshold: **2b'00: 80%** 2b'10: 60% 2b'01: 40% 2b'11: reserved
2	CBC_EN	R/W	0h	**0: Disable CBC function** 1: Enable CBC function
1	CBCWARN_EN	R/W	0h	**0: Disable CBC warning** 1: Enable CBC warning
0	CBCFAULT_EN	R/W	0h	**0: Disable CBC fault** 1: Enable CBC fault

6.5.1.48 FAULT_CLEAR Register (Offset = 78h) [Reset = 00h]

FAULT_CLEAR is shown in 図 6-65 and described in 表 6-55.

Return to the Summary Table.

Fault clear

図 6-65. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED						
W-0h	W-0h						

表 6-55. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT_CLR	W	0h	WRITE CLEAR BIT **0: No fault clear** 1: Clear analog fault
6-0	RESERVED	W	0h	

7 Application and Implementation

注

以下のアプリケーション情報は、テキサス・インスツルメンツの製品仕様に含まれるものではなく、テキサス・インスツルメンツはその正確性も完全性も保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Typical Applications

7.1.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

図 7-1 shows the 2.0 (Stereo BTL) system application.

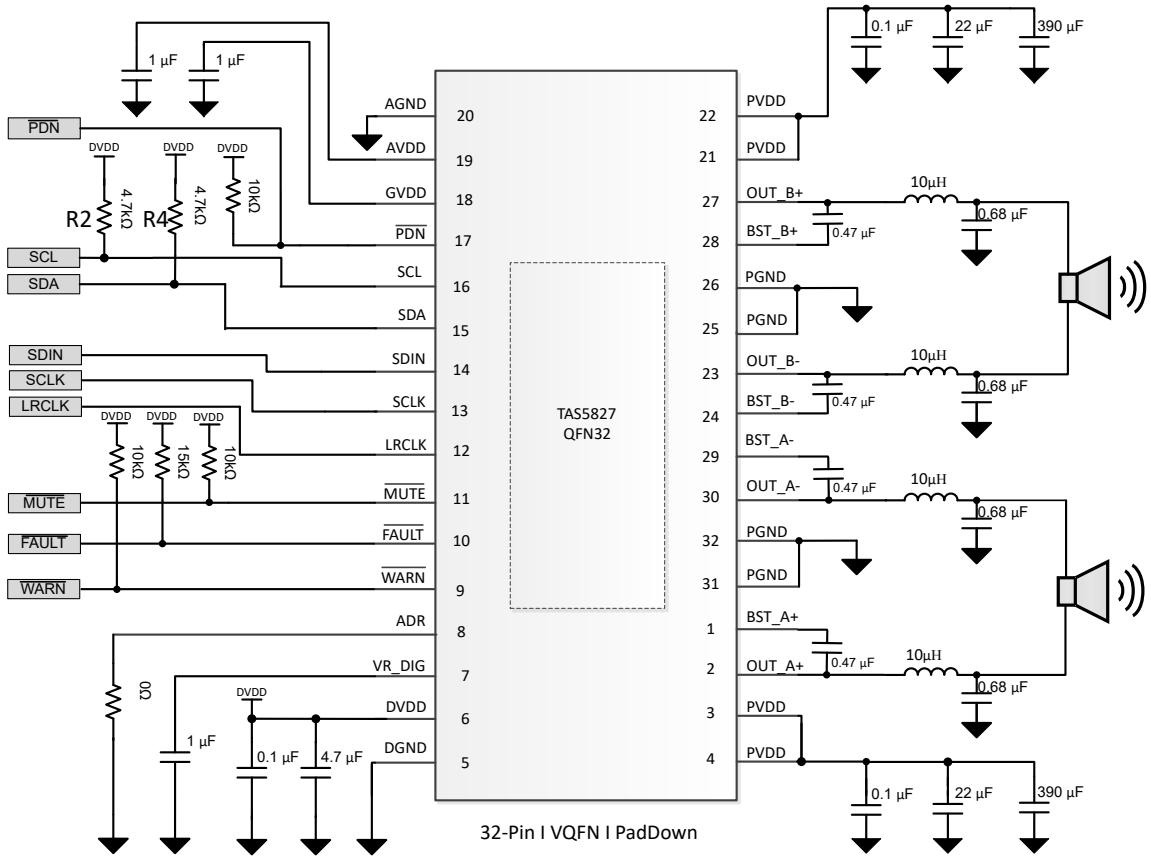


図 7-1. 2.0 (Stereo BTL) System Application Schematic

7.1.2 Mono (PBTL) Systems

In Mono mode, TAS5827 can be used as PBTL mode to drive sub-woofer with more output power.

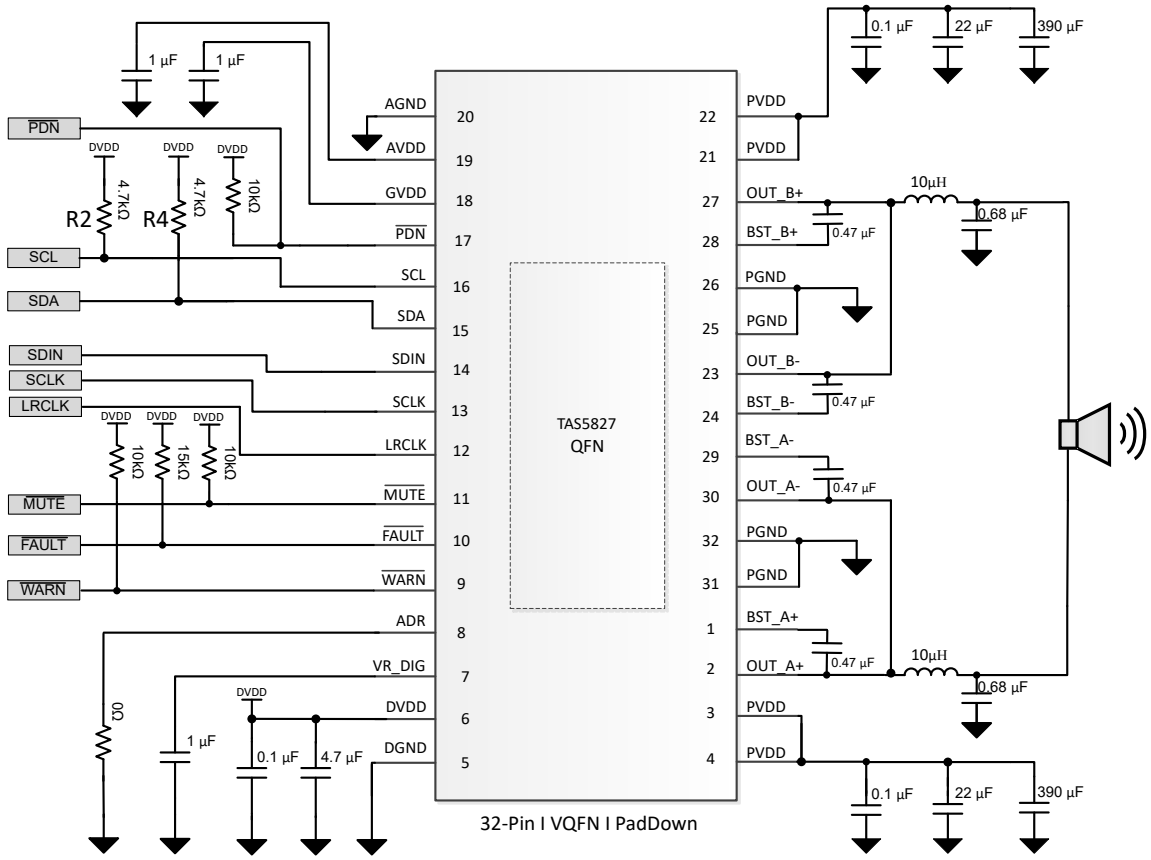


図 7-2. Sub-woofer (PBTL) Application Schematic

7.1.3 Layout Guidelines

7.1.3.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

The guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in *セクション 7.1.3.4*. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, TI recommends to start from the guidance shown in *セクション 7.1.3.4* and work with TI field application engineers or through the E2E community to modify the example based upon the application specific goals.

7.1.3.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD, GVDD and PVDD. However, the capacitors on the PVDD net for the TAS5827 device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5827 device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the Absolute Maximum Ratings table, damaging the deice . For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Example* section.

7.1.3.3 Optimizing Thermal Performance

Follow the layout example shown in the セクション 7.1.1 to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer must make sure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

7.1.3.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips must be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5827 device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5827 device away from the edge of the PCB when possible to make sure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5827 device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient the pads so that the narrow end of the passive component is facing the TAS5827 device.
- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

7.1.3.3.2 Stencil Pattern

The recommended drawings for the TAS5827 device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to be an excellent choice for the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance can be too conservative and advanced PCB design techniques can be used to improve thermal performance of the system.

注

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

7.1.3.3.3 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5827 device is soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. TI recommends to

make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5827 device, be made no smaller than what is specified in the package addendum. This method makes sure that the TAS5827 device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in *Layout Example*, this interface can benefit from improved thermal performance.

注

Vias can obstruct heat flow if the vias are not constructed properly.

More notes on the construction and placement of vias are as follows:

- Remove thermal reliefs on thermal vias, because the thermal reliefs impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drill must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes must be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing must be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias must be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in *Layout Example*.
- Make sure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5827 device to open up the current path to and from the device.

7.1.3.3.4 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste leads to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Example* section. Make sure that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

7.1.3.4 Layout Example

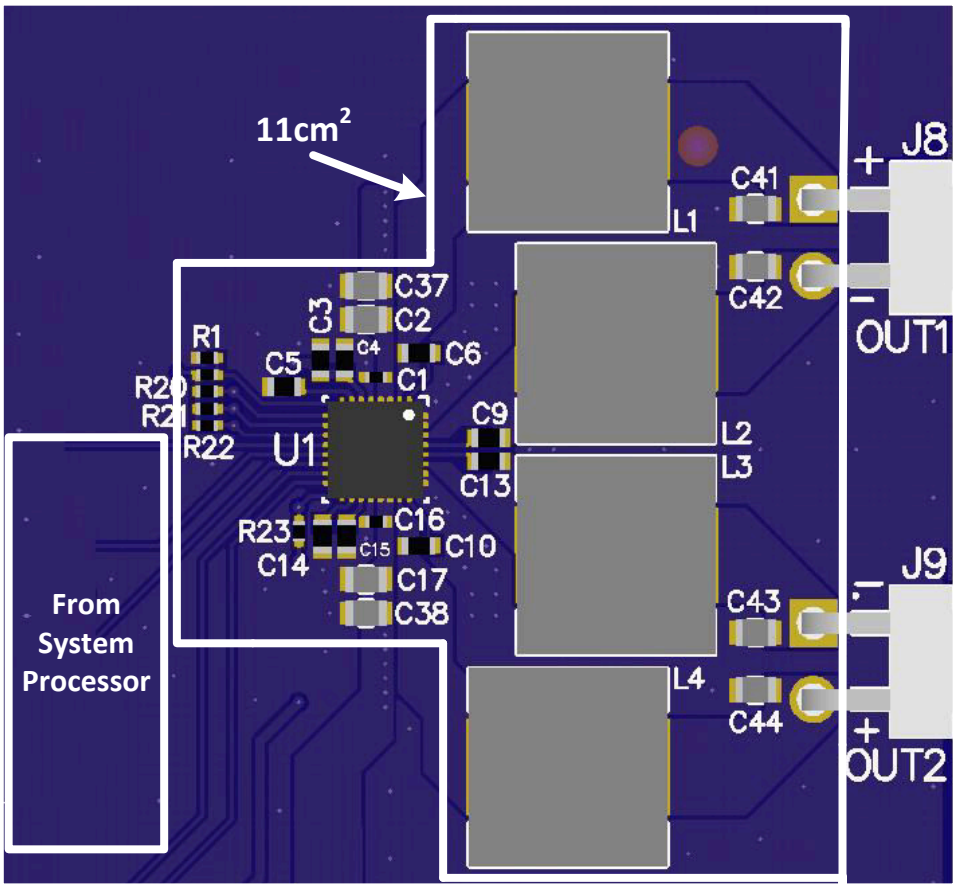


図 7-3. 2.0 (Stereo BTL) 3-D View

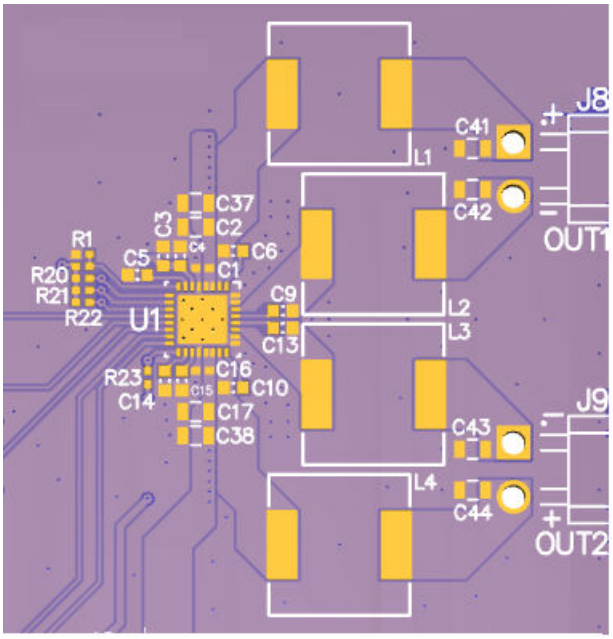


図 7-4. 2.0 (Stereo BTL) Top Copper View

8 Power Supply Recommendations

The TAS5827 device requires two power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the Recommended Operating Conditions table. The two power supplies do not have a required power up sequence. The power supplies can be powered on in any order.

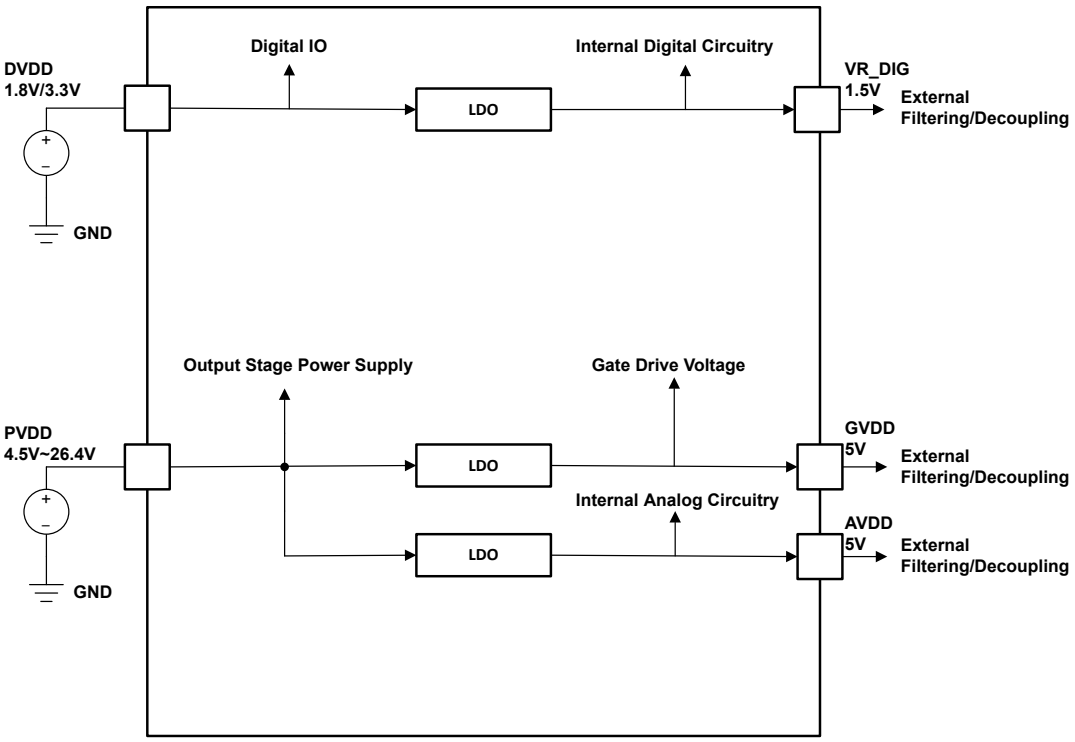


図 8-1. Power Supply Function Block Diagram

8.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in 図 8-1, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *セクション 7* section and the *セクション 7.1.3.4* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5827 device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to

support the current requirements of the internal circuitry, and should not be used to power any additional external circuity. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

8.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TAS5827EVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5827 device *Importance of PVDD Bypass Capacitor Placement on PVDD Network*. Lack of proper decoupling, like that shown in the *Importance of PVDD Bypass Capacitor Placement on PVDD Network*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply that is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5827 internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

The glossary section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor (also known as System Processor, Scalar, Host, or System Controller) refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. This device often configures the controls of the audio processing devices (like the TAS5827) in the audio path in order to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$r_{DS(on)}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static controls/Static configurations are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

9.1.2 Development Support

For RDGUI software, please consult your local field support engineer.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

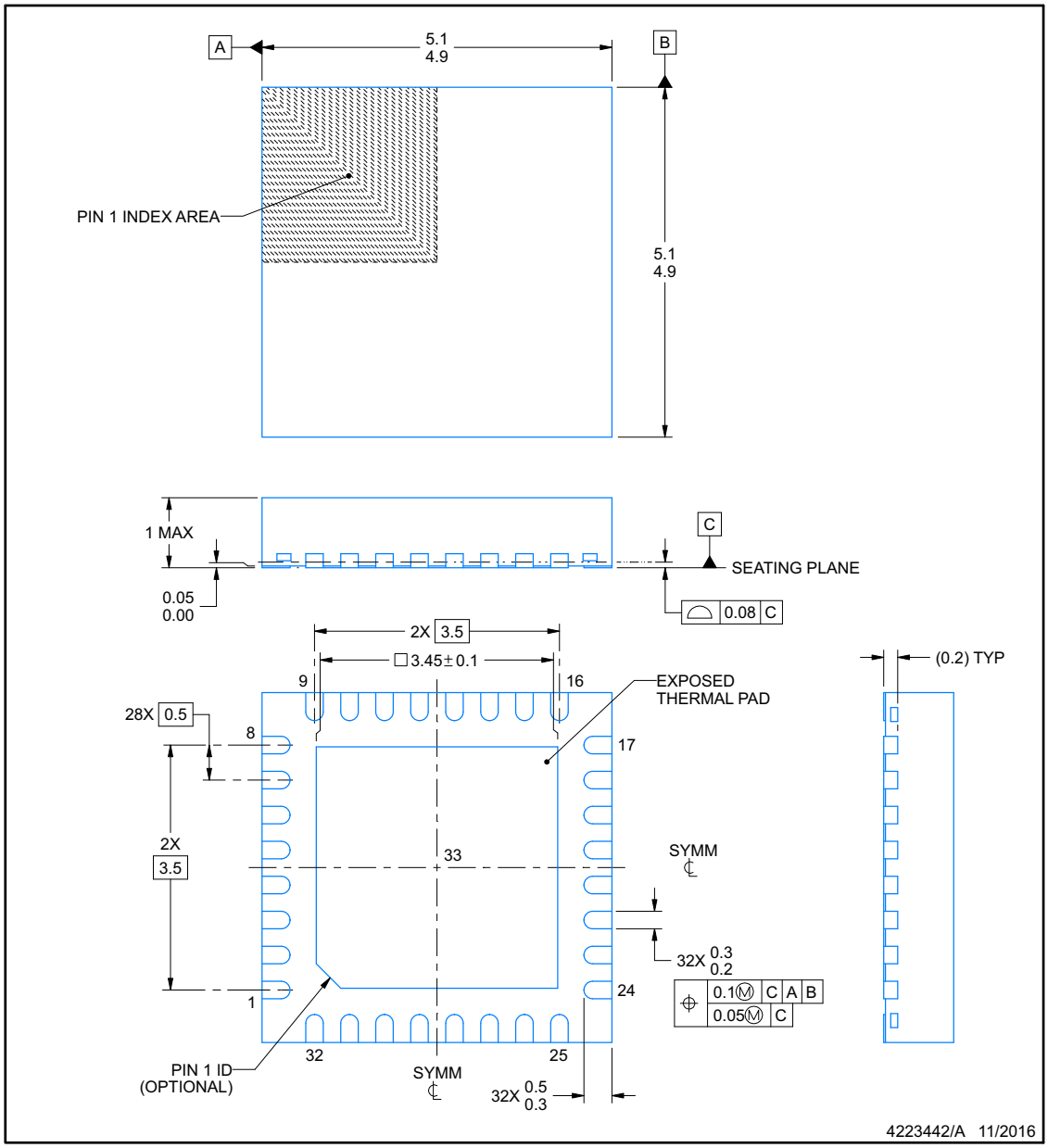
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



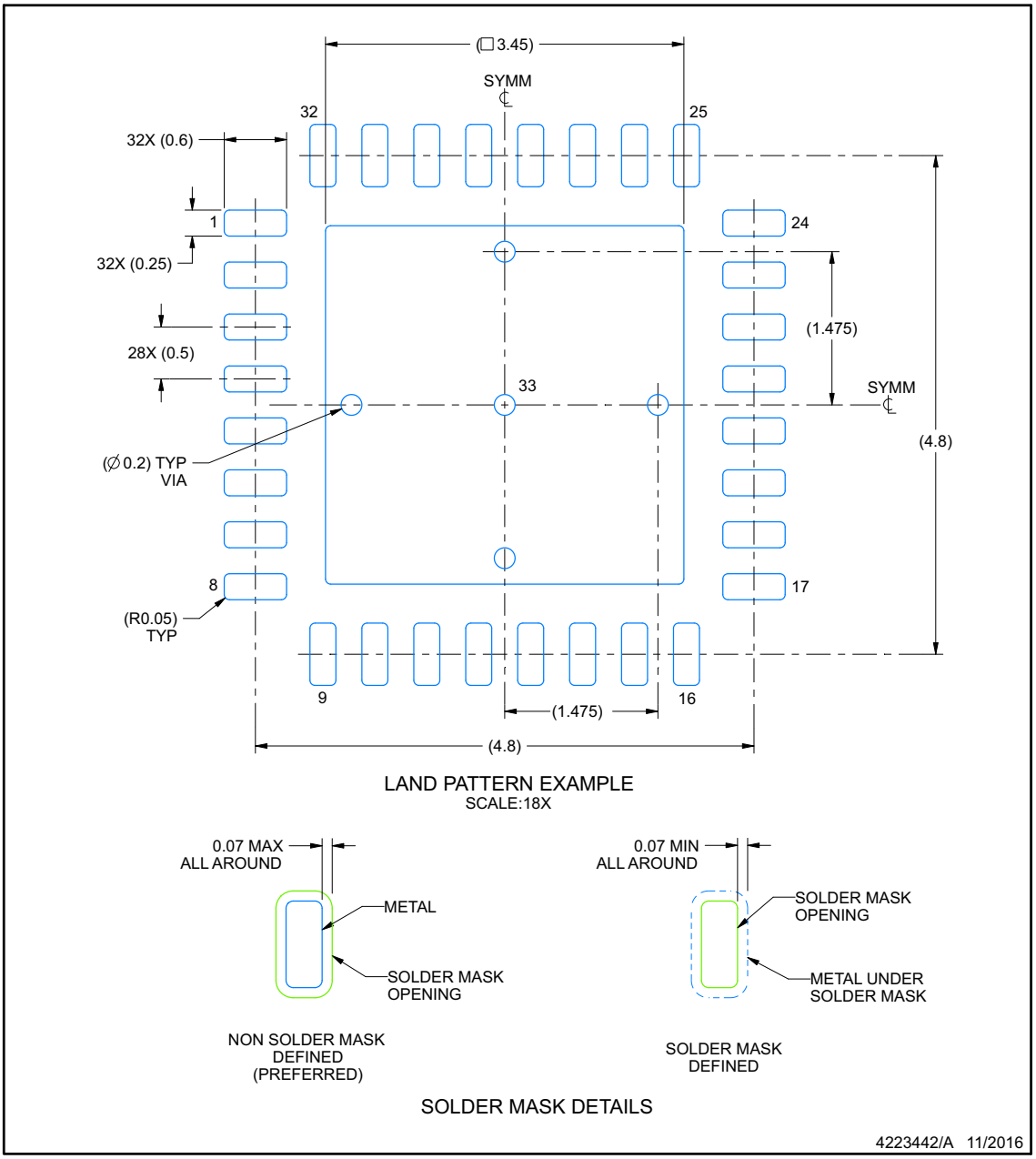
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

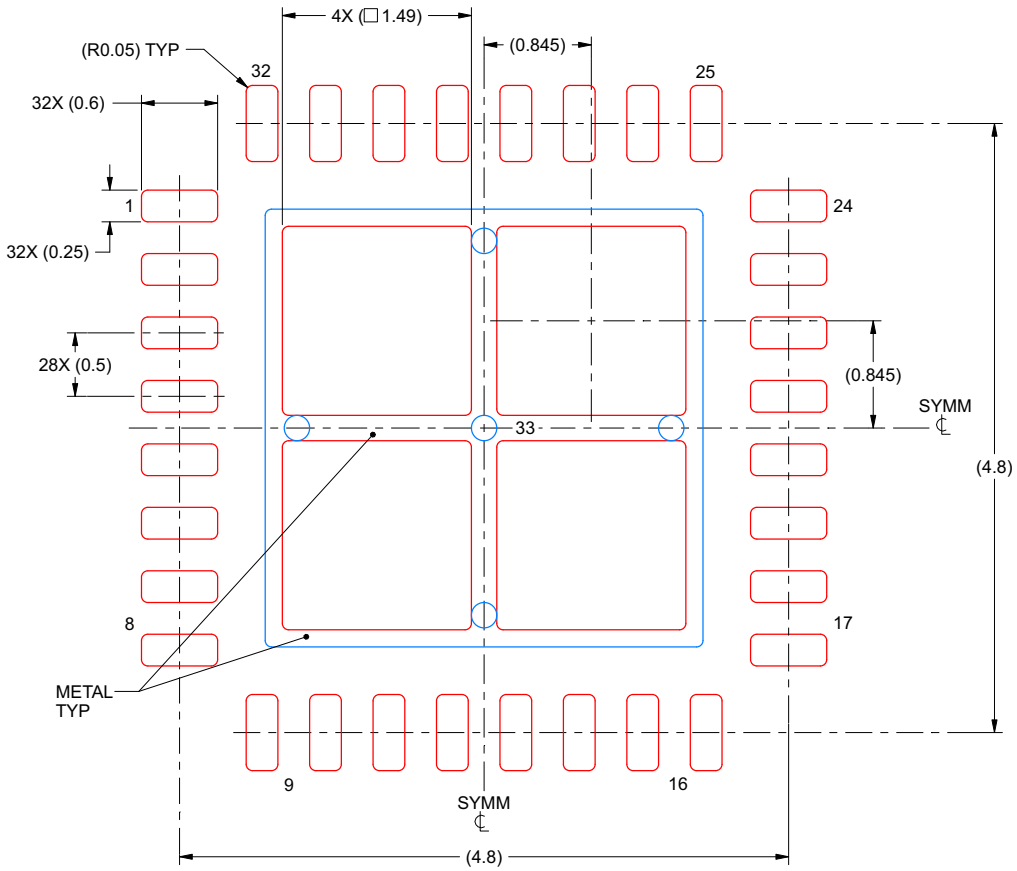
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5827RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TAS 5827

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

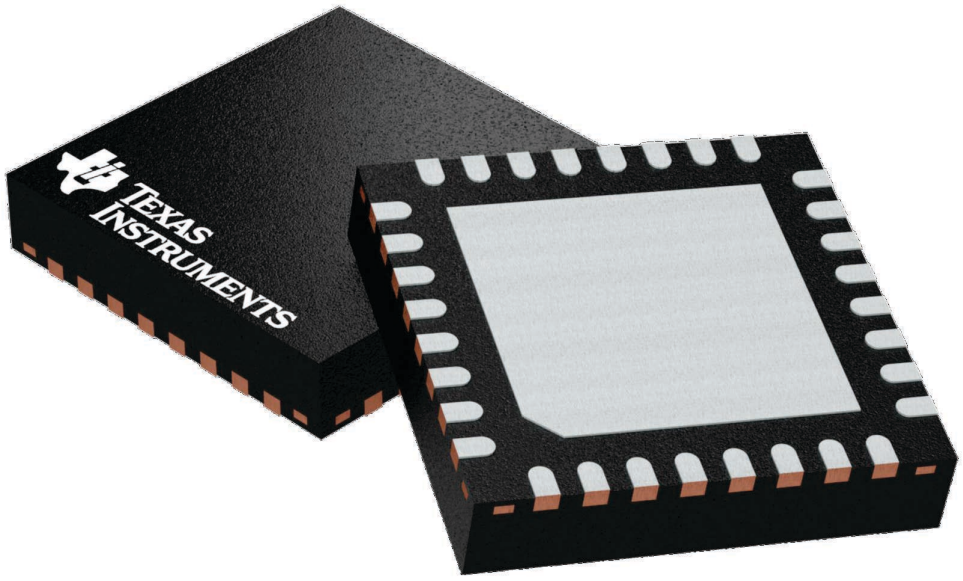
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

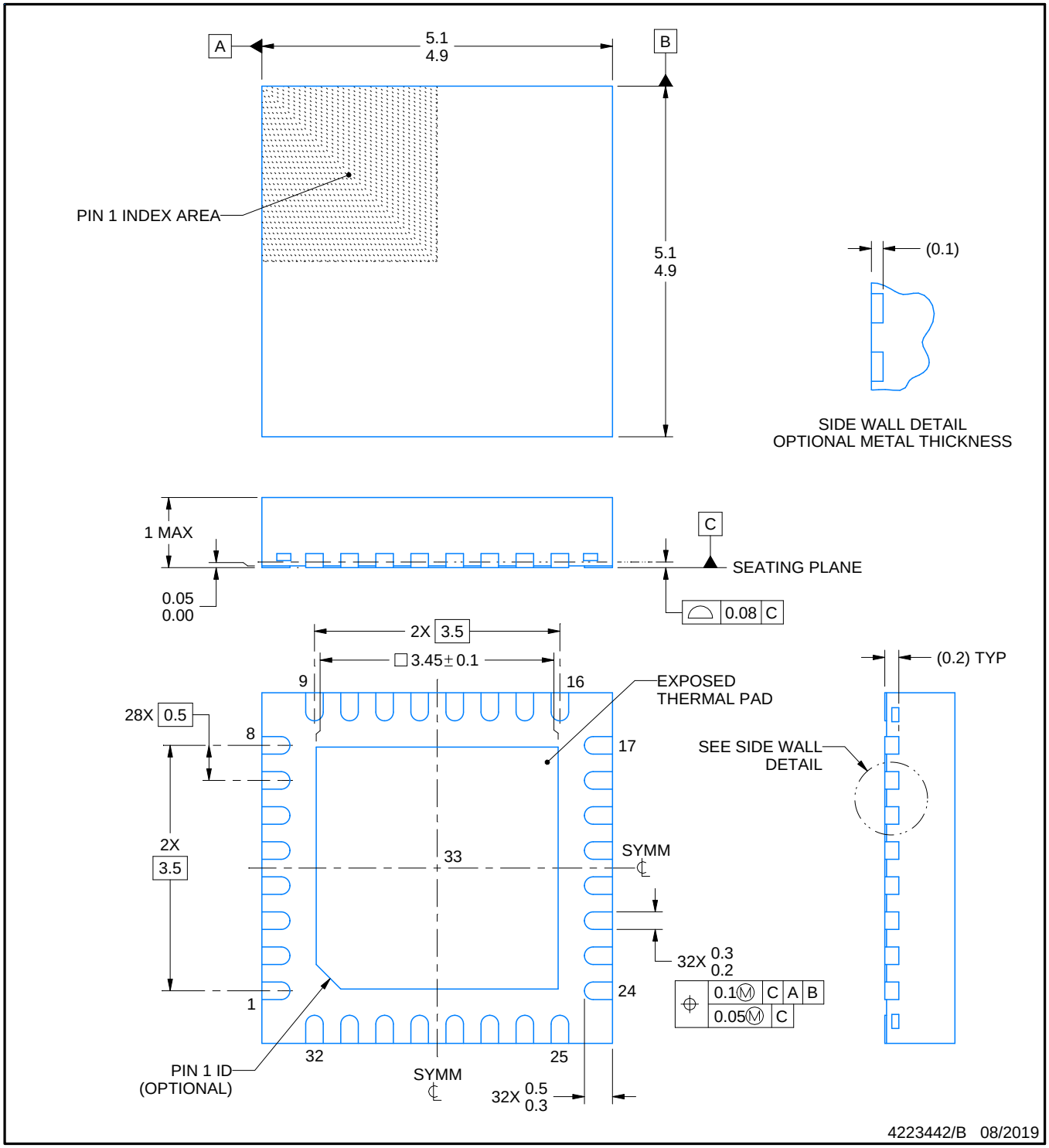
4224745/A

RHB0032E

PACKAGE OUTLINE

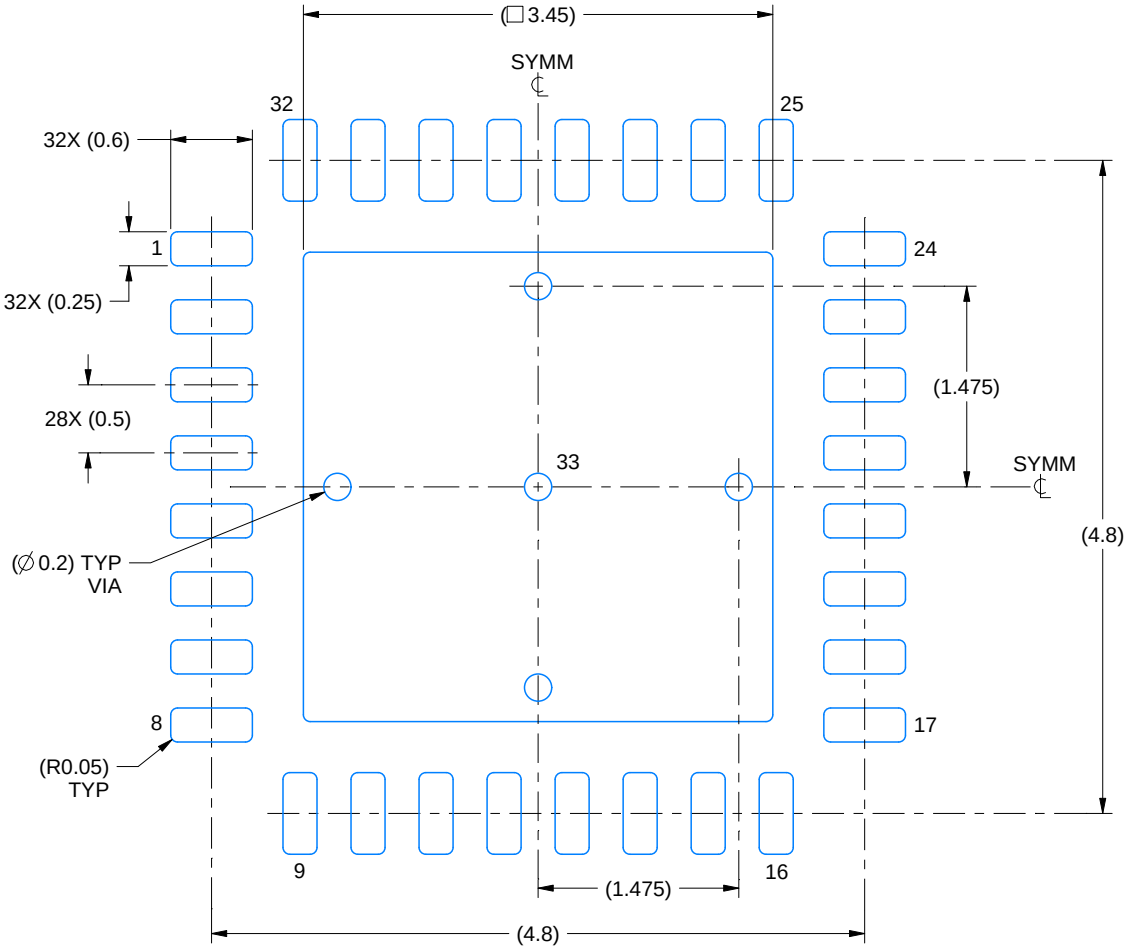
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

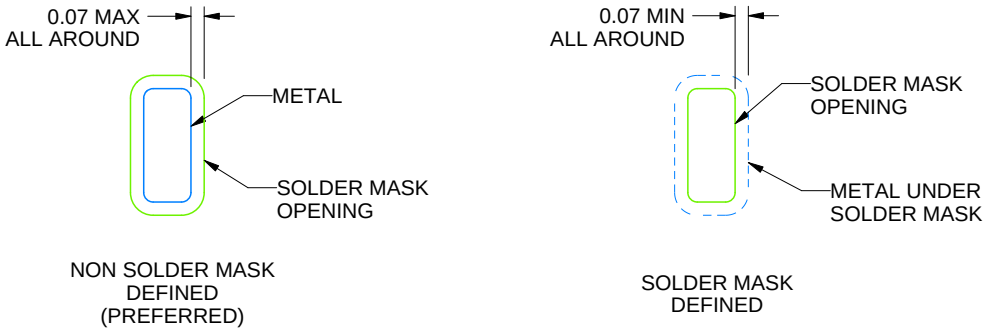


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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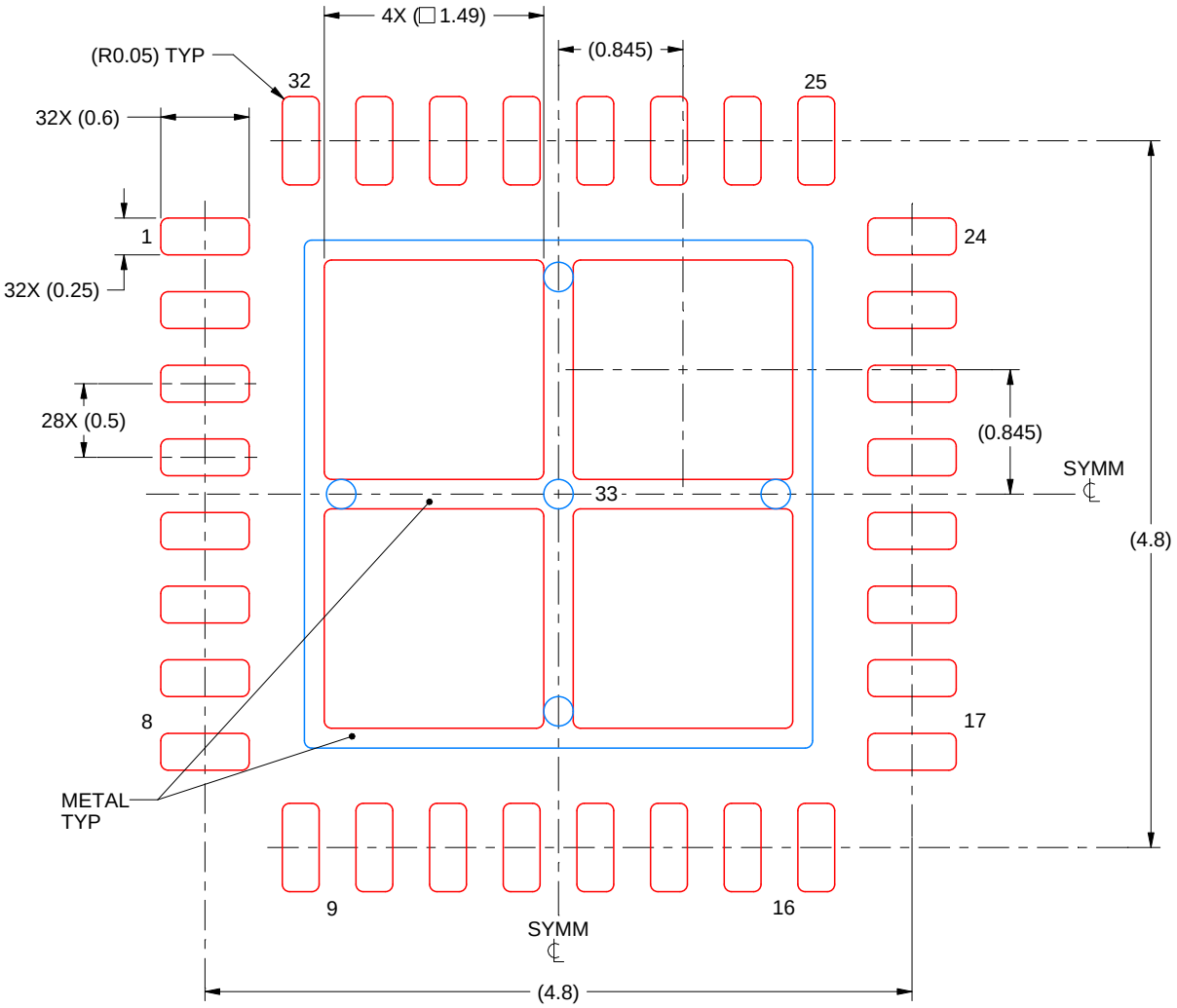
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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